ORIENT DISPLAY
MAKE THINGS POSSIBLE

Specification for E-Paper

AED648480A00-5.83ENRS4

Revision 2.0

A	Orient Display
ED	E-Paper
648480	Resolution 648x 480
A00	Revision A00
5.83	Diagonal: 5.83’’, Module: 125.40 × 99.50 × 1.20 mm
E	EPD - Electrophoretic Display (Active Matrix)
N	Top: 0°C~+40°C; Tstr: -25°C~+70
R	Reflective Polarizer
S	3-/4-wire SPI Interface
4	Four Colors - White, Black, Red, Yellow
/	Controller JD79665CA Or Compatible
/	ZIF FPC
/	Ultra Wide Viewing Angle
/	Ultra Low Power Consumption

Revision History

Version	Content	Date	Producer
2.0	New release	2025/12/10	

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1. Over View

AED648480A00-5.83ENRS4 is an Active Matrix EPD all-in-one driver with timing controller for ESL. The sources have 2-bit outputs per pixel to support white/black/red/yellow. The 5.83 inch active area contains 648 × 480 pixels. The module is a TFT-array driving electrophoresis display, with

integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆648*480 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I^2C signal master interface to read external temperature sensor
- ◆Built-in temperature sensor

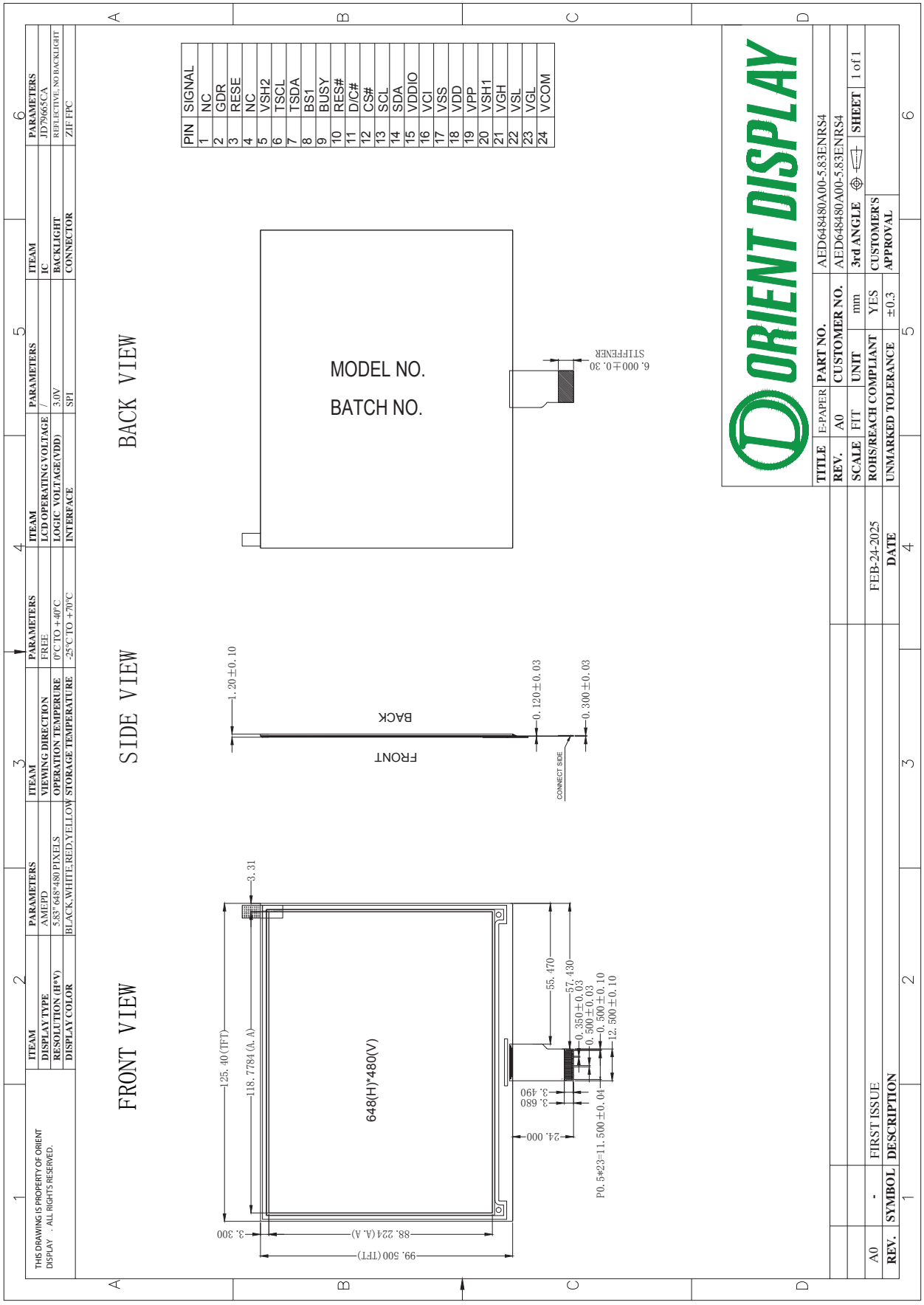
3. Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	5.83	Inch	
Display Resolution	648(H) ×480(V)	Pixel	DPI:138
Active Area	118.78（H）×88.22(V)	mm	
Pixel Pitch	0.1833×0.1838	mm	
Pixel Configuration	Rectangle		
Outline Dimension	125.40(H)×99.50 (V) ×1.20(D)	mm	
Weight	28.22±0.5	g	

温度		0~3	3~6	6~9	9~12	12~15	15~19	19~24	24~29	29~34	34~40
		8 fonts can be clearly seen									
	L*	62≤L≤67（0~9：TYP≤66；9~40：TYP≤65）									
	A*	T0≤0(24H ≤1)									
	b*	≤2.5									
	Ghosting(△E2000)	≤2									
	L*	≤11（TYP≤9）						≤11.5（TYP≤9）		≤11（TYP≤9）	
	A*	≤9						≤8		≤10	
	b*	≤0.5									
	Ghosting(△E2000)	≤2									
	L*	≥23						≥24		≥23	
	A*	≥34（0~9：TYP≥36；9~19：TYP≥38）						≥38（TYP≥40）			
	b*	≤34									
	Ghosting(△E2000)	≤2									
	L*	≥50						≥54			
	A*	≤18									
	b*	≥53（TYP≥55）			≥56（TYP≥63）			≥60（TYP≥66）			
	Ghosting(△E2000)	≤2									

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

4. Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	CSB2(NC)		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep Open
5	VSHR	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	Note 5-6
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	Note 5-6
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY_N	O	Busy state output pin	Note 5-4
10	RST_N	I	Reset signal input. Active Low.	Note 5-3
11	DC	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VDD	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD_18V	C	Core logic power pin VDD_18V can be regulated internally from VDD. A capacitor should be connected between VDD_18V and VSS	
19	COTP	P	FOR TEST	Keep Open
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU

communication only when CSB is pulled LOW.

Note 5-2: This pin is (DC) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

Note 5-6:This pin connect to the VSS if there is no external temperature sensor.

External pull up resistor is required when connecting to I2C slave.

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD,VDDIO	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VDDIO +0.3	V
Operating Temp range	TOPR	0 to +40	ºC.
Storage Temp range	TSTG	-25 to +70	ºC.
Optimal Storage Temp	TSTGo	23±3	ºC.
Optimal StorageHumidity	HSTGo	55±10	%RH

Note:

1. Maximum ratings are those values beyond which damages to the device may occur.Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

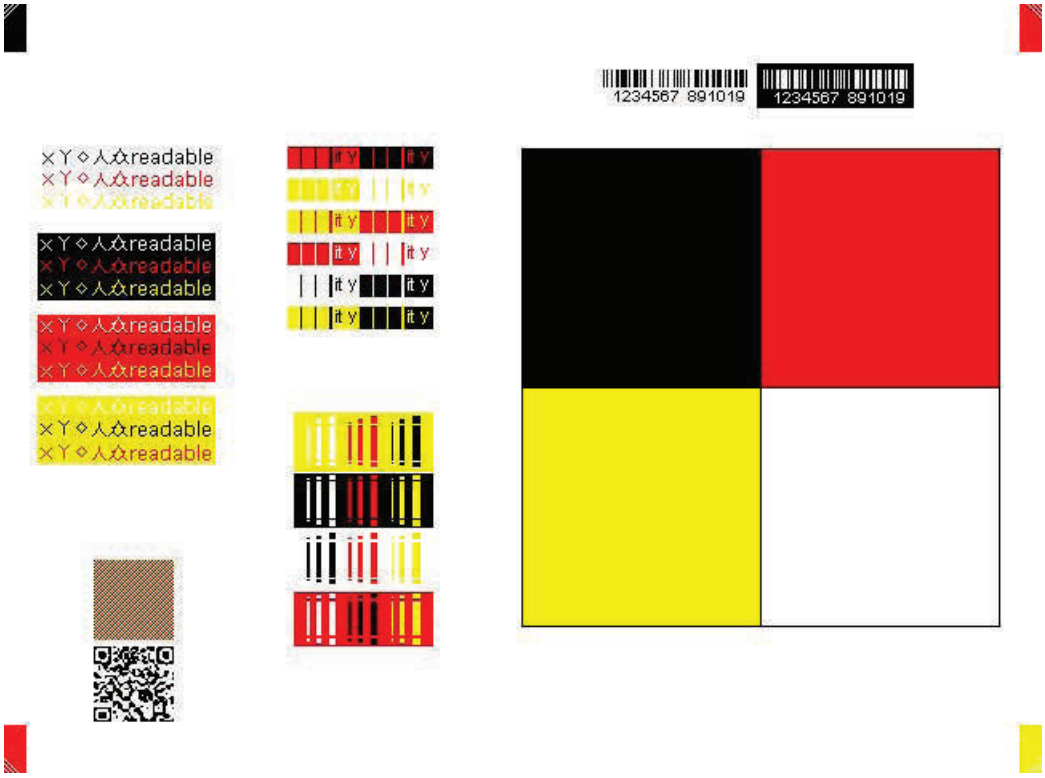
2. The display screen should be kept white and face up during storage. Please refer to the [Reliability Test] section.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{DD}	-	VDD	2.2	3.0	3.6	V
Power for interface logic pins	V_{DDIO}	-	VDDIO	2.2	-	3.6	V
Core logic voltage	V_{DD_18V}		VDD_18V	1.35	1.5	1.65	V
VCOM_DC output voltage	V_{com}	-	VCOM	-	-	-	V
High level input voltage	V_{IH}	-	-	0.7 VDDIO	-	VDDIO	V
Low level input voltage	V_{IL}	-	-	VSS	-	0.3 VDDIO	V
High level output voltage	V_{OH}	IOH = 400uA	-	VDDIO -0.4	-	-	V
Low level output voltage	V_{OL}	IOL = -400uA	-	VSS	-	VSS +0.4	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	36	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.0012	-	mW
Typical operating current	$Iopr_VCI$	V_{CI} =3.0V	-	-	12	- -	mA
Image update time	-	23 ºC	-	-	20	-	sec
Deep sleep mode current	$Idslp_VCI$	DC/DC off No clock No input load Ram data not retain	-	-	0.4	1	uA

Notes: 1. The typical power measurement method is as follows, and the output is reported according to the test screen provided by the ODNA.



The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by ODNA.

Electrical measurement：Tektronix oscilloscope - MSO44，

Tektronix current probe－TCP312A.

6.3 MCU Interface

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	DC	RST_N
BS1=L 4-wire SPI	SDA	SCL	CSB	DC	RST_N
BS1=H 3-wire SPI	SDA	SCL	CSB	L	RST_N

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

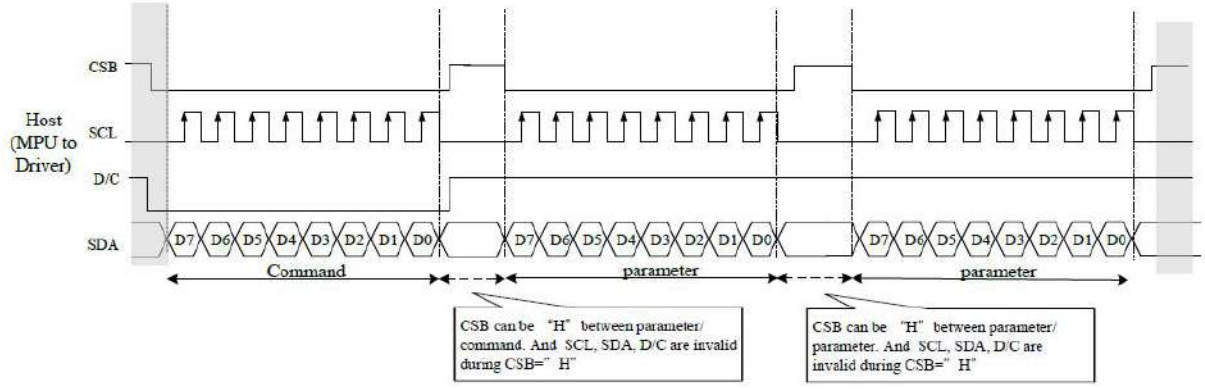
The serial interface consists of serial clock SCL, serial data SDA, DC, CSB. This interface supports Write mode and Read mode.

Function	CSB	DC	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1: 4-wire SPI mode



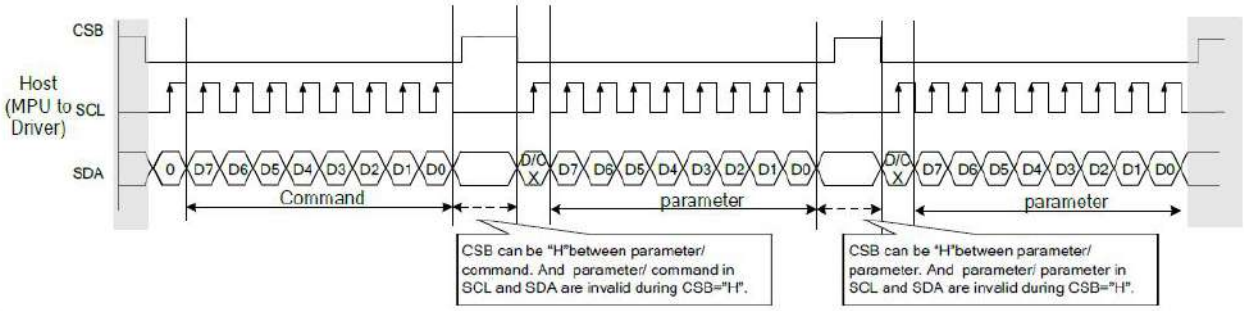
6.3.3 MCU Serial Interface (3-wire SPI)

Function	CSB	DC	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

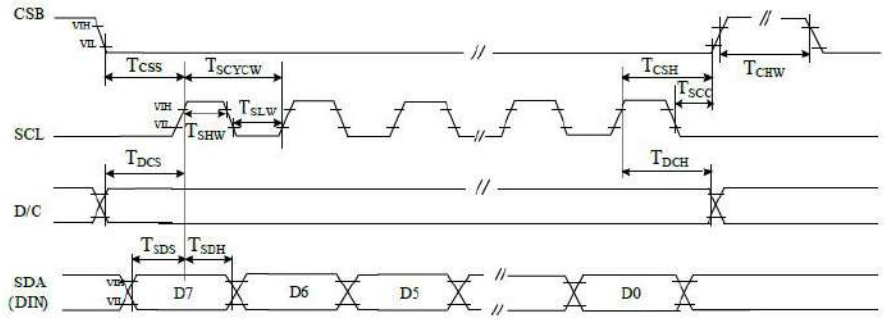
Table 6-3-3: Control pins of 3-wire Serial Peripheral interface

Note：↑ stands for rising edge of signal

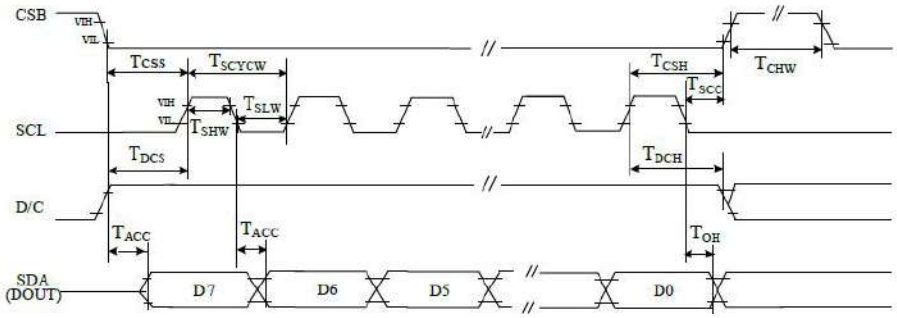
Figure 6-3-2: 3-wire SPI mode



6.3.4 Interface Timing



4 pin serial interface characteristics(write mode)



Serial Interface Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL "H" pulse width (Write)
	T_{SLW}	35			ns	SCL "L" pulse width (Write)
	T_{SCYCR}	250			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL "H" pulse width (Read)
	T_{SLR}	60			ns	SCL "L" pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time

7.Command Table

R/W: 0:Write Cycle 1:Read Cycle D/CX:0:Command/1:Data D7~D0:-:Don’t Care

1)R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source / Border / Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →...→S2→Last data=S1. 1: Shift right: First data=S1→S2 →...→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →...→G2→Last line=G1. 1:Scan up; First line=G1→G2 →...→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 800x600(default) 01: Display resolution is 720x540 10: Display resolution is 640x480 11: Display resolution is 600x448

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display, the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction	

2) R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	BD_EN	-	-	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)

5	BD_EN	**Border LDO enable** (when TPS=LOW) 0:Border LDO disable(default)

code	Border level selection
00	VCOM
01	VSP
10	VSN
11	VSPL

1:Border LDO enable

code	Border level selection
00	VCOM
01	VSP+VCOM
10	VSN+VCOM
11	VSPL+VCOM

Border LDO enable (when TPS=HIGH)
0:Border LDO disable(default)

code	Border level selection
00	VCOM
01	VSP
10	VSN
11	VSPL

1:Border LDO enable

code	Border level selection
00	VCOM
01	VSP+VCOM
10	VSN+VCOM
11	VSPL+VCOM

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	Internal VSP & VSPL power selection.

Bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	Internal VSN power selection.

Bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
3. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	+10v	+10v
	VGN	-10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)
	VCOMDC	-2v	-2v

4. Voltage setting limit: VSP_0 ≥ VSPL_0 , VSP_1 ≥ VSPL_1

Restriction

3)R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	•The command defines as : R02h = 0x00h ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

4)(R04H) (PON):Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence(base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

5）R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description		Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
	Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
		000001	Period2	010111	Period24	101101	Period46
		000010	Period3	011000	Period25	101110	Period47
		000011	Period4	011001	Period26	101111	Period48
		000100	Period5	011010	Period27	110000	Period49
		000101	Period6	011011	Period28	110001	Period50
		000110	Period7	011100	Period29	110010	Period51
		000111	Period8	011101	Period30	110011	Period52
		001000	Period9	011110	Period31	110100	Period53
		001001	Period10	011111	Period32	110101	Period54
		001010	Period11	100000	Period33	110110	Period55
		001011	Period12	100001	Period34	110111	Period56
		001100	Period13	100010	Period35	111000	Period57
		001101	Period14	100011	Period36	111001	Period58
		001110	Period15	100100	Period37	111010	Period59
		001111	Period16	100101	Period38	111011	Period60
		010000	Period17	100110	Period39	111100	Period61
		010001	Period18	100111	Period40	111101	Period62
		010010	Period19	101000	Period41	111110	Period63
		010011	Period20	101001	Period42	111111	Period64
		010100	Period21	101010	Period43		
		010101	Period22	101011	Period44		
Restriction							

6) R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

7）**R10H (DTM): Data Start transmission Register**

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM_master	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
⋮	W	1	⋮		⋮		⋮		⋮		00h
Mth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel. Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1,Pixel[1:0]=01 ->Gray level select=Gray1,follow LUT data output from IP output port"ogray01".

When DDX=0,Pixel[1:0]=11 ->Gray level select=Gray0,follow LUT data output from IP output port"ogray00"

Restriction	

8)R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter:

Bit	Name	Description
7	Data_flag	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.

After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

Restriction	This command only actives when BUSY_N = "1".

9)R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R12H=0x00 While users send this command, driver will refresh display base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

10) R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

11）R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

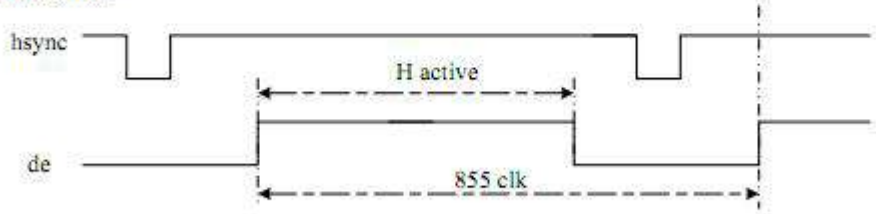
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

bit3	Dynamic frame rate
0	Disable(default)
1	Enable

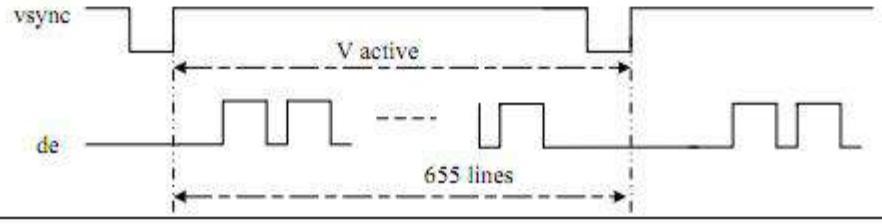
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



Restriction

12)R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

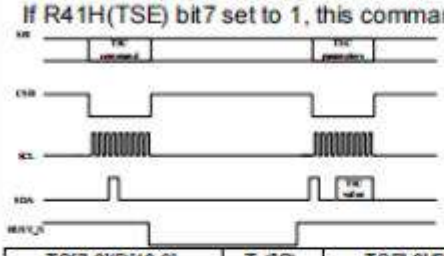
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[9:8]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction

This command only actives when BUSY_N = "1".

13)R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +0.5℃ 0010: +1℃ 0011: +1.5℃ 0100: +2℃ 0101: +2.5℃ 0110: +3℃ 0111: +3.5℃ 1000: -4℃ 1001: -3.5℃ 1010: -3℃ 1011: -2.5℃ 1100: -2℃ 1101: -1.5℃ 1110: -1℃ 1111: -0.5℃
4	TO[4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

14)R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3rd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction

This command only actives after R04H(PON)

15)R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

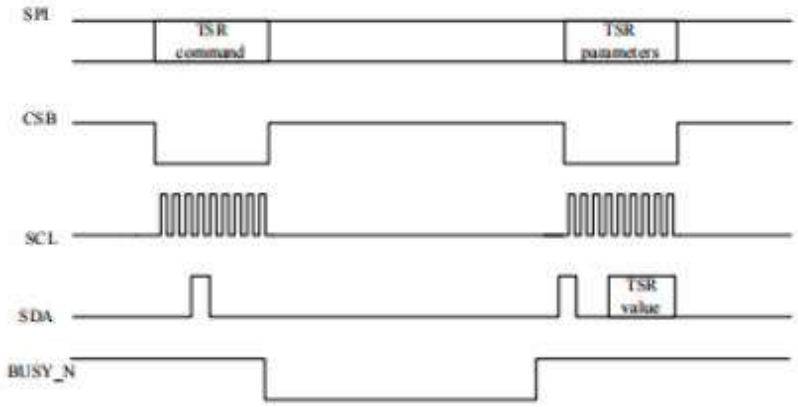
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction

This command only actives after R04H(PON)

16)R50H (CDI): VCOM and DATA interval setting Register

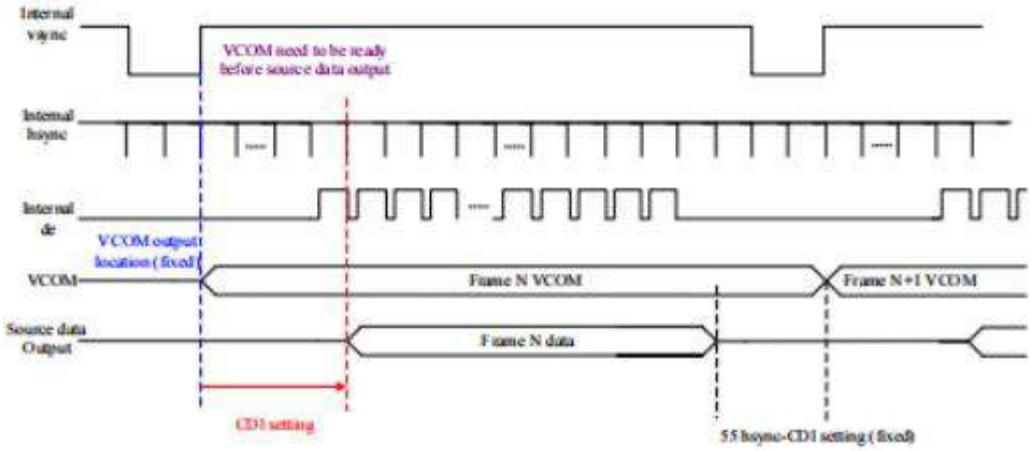
R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)
:
CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.

Boarder output will follow FOPT definition being defined in R00h.

Restriction

17）R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

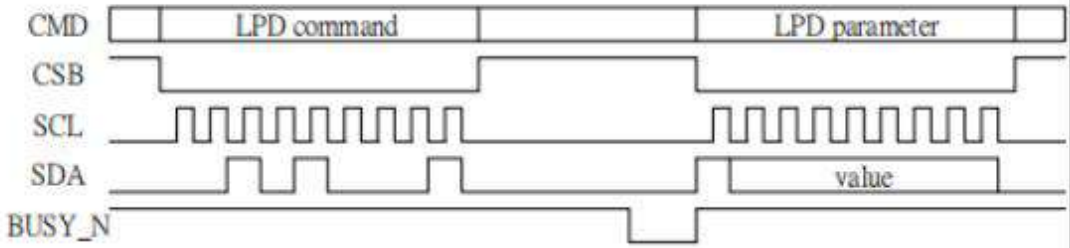
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the input power condition. Host can read this data to understand the battery's condition.
When LPD="1", system input power is normal.
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status.



Restriction

This command only actives when BUSY_N = "1".

18)R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3th Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Note: No matter HRES[1:0] value being filled, it's always be 00b. Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1 EX :800X600 GD: First G active = G0 LAST active GD= 0+600-1= 599; (G599) SD : First active channel: =S0 LAST active SD=0+200*4-1=799; (S799)
Restriction	Horizontal resolution should be 4-multiple.

19) R65H(GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3rd Parameter	W	1	-	-	-	-	-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Note: No matterS_start [1:0] value being filled, it's always be 00 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line
Restriction	S_Start should be the multiple of 4

20)R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	1	0	0	0	1	1	1	0	8Eh
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st & 2nd & 3rd Parameter:

Bit	Description
7-0	CHIP_REV

Restriction	

21)R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

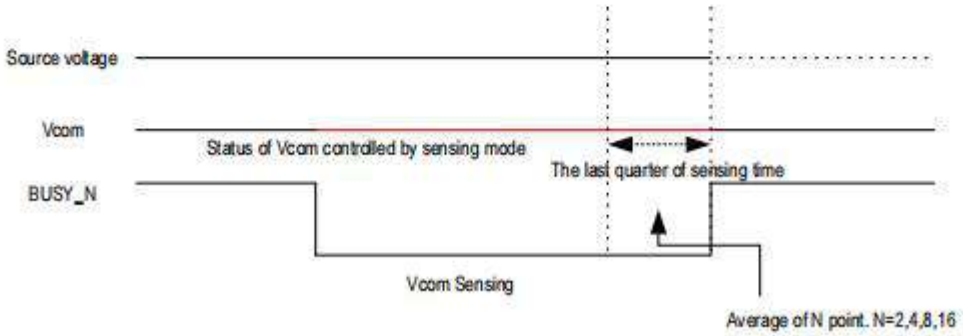
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s
7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16



Restriction

This command only actives when BUSY_N = "1".

22)R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter: (when TPS=LOW)

Bit	Name	Description
6-0	VV[6:0]	VCOM value

VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other	-4	
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

1st Parameter: (when TPS=HIGH)

Bit	Name	Description
6-0	VV[6:0]	VCOM value

VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	1.4	0111000	38h	2.8
0000001	01h	0.05	0011101	1Dh	1.45	0111001	39h	2.85
0000010	02h	0.1	0011110	1Eh	1.5	0111010	3Ah	2.9
0000011	03h	0.15	0011111	1Fh	1.55	0111011	3Bh	2.95
0000100	04h	0.2	0100000	20h	1.6	0111100	3Ch	3
0000101	05h	0.25	0100001	21h	1.65	0111101	3Dh	3.05
0000110	06h	0.3	0100010	22h	1.7	0111110	3Eh	3.1
0000111	07h	0.35	0100011	23h	1.75	0111111	3Fh	3.15
0001000	08h	0.4	0100100	24h	1.8	1000000	40h	3.2
0001001	09h	0.45	0100101	25h	1.85	1000001	41h	3.25
0001010	0Ah	0.5	0100110	26h	1.9	1000010	42h	3.3
0001011	0Bh	0.55	0100111	27h	1.95	1000011	43h	3.35
0001100	0Ch	0.6	0101000	28h	2	1000100	44h	3.4
0001101	0Dh	0.65	0101001	29h	2.05	1000101	45h	3.45
0001110	0Eh	0.7	0101010	2Ah	2.1	1000110	46h	3.5
0001111	0Fh	0.75	0101011	2Bh	2.15	1000111	47h	3.55
0010000	10h	0.8	0101100	2Ch	2.2	1001000	48h	3.6
0010001	11h	0.85	0101101	2Dh	2.25	1001001	49h	3.65
0010010	12h	0.9	0101110	2Eh	2.3	1001010	4Ah	3.7
0010011	13h	0.95	0101111	2Fh	2.35	1001011	4Bh	3.75
0010100	14h	1	0110000	30h	2.4	1001100	4Ch	3.8
0010101	15h	1.05	0110001	31h	2.45	1001101	4Dh	3.85
0010110	16h	1.1	0110010	32h	2.5	1001110	4Eh	3.9
0010111	17h	1.15	0110011	33h	2.55	1001111	4Fh	3.95
0011000	18h	1.2	0110100	34h	2.6	1010000	50h	4
0011001	19h	1.25	0110101	35h	2.65	other		4
0011010	1Ah	1.3	0110110	36h	2.7			
0011011	1Bh	1.35	0110111	37h	2.75			

Restriction	

23)R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter: (when TPS=LOW)

Bit	Name	Description
6-0	VDCS[6:0]	VCOM value

VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

1st Parameter: (when TPS=HIGH)

Bit	Name	Description
6-0	VDCS[6:0]	VCOM value

VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	1.4	0111000	38h	2.8
0000001	01h	0.05	0011101	1Dh	1.45	0111001	39h	2.85
0000010	02h	0.1	0011110	1Eh	1.5	0111010	3Ah	2.9
0000011	03h	0.15	0011111	1Fh	1.55	0111011	3Bh	2.95
0000100	04h	0.2	0100000	20h	1.6	0111100	3Ch	3
0000101	05h	0.25	0100001	21h	1.65	0111101	3Dh	3.05
0000110	06h	0.3	0100010	22h	1.7	0111110	3Eh	3.1
0000111	07h	0.35	0100011	23h	1.75	0111111	3Fh	3.15
0001000	08h	0.4	0100100	24h	1.8	1000000	40h	3.2
0001001	09h	0.45	0100101	25h	1.85	1000001	41h	3.25
0001010	0Ah	0.5	0100110	26h	1.9	1000010	42h	3.3
0001011	0Bh	0.55	0100111	27h	1.95	1000011	43h	3.35
0001100	0Ch	0.6	0101000	28h	2	1000100	44h	3.4
0001101	0Dh	0.65	0101001	29h	2.05	1000101	45h	3.45
0001110	0Eh	0.7	0101010	2Ah	2.1	1000110	46h	3.5
0001111	0Fh	0.75	0101011	2Bh	2.15	1000111	47h	3.55
0010000	10h	0.8	0101100	2Ch	2.2	1001000	48h	3.6
0010001	11h	0.85	0101101	2Dh	2.25	1001001	49h	3.65
0010010	12h	0.9	0101110	2Eh	2.3	1001010	4Ah	3.7
0010011	13h	0.95	0101111	2Fh	2.35	1001011	4Bh	3.75
0010100	14h	1	0110000	30h	2.4	1001100	4Ch	3.8
0010101	15h	1.05	0110001	31h	2.45	1001101	4Dh	3.85
0010110	16h	1.1	0110010	32h	2.5	1001110	4Eh	3.9
0010111	17h	1.15	0110011	33h	2.55	1001111	4Fh	3.95
0011000	18h	1.2	0110100	34h	2.6	1010000	50h	4
0011001	19h	1.25	0110101	35h	2.65	other		4
0011010	1Ah	1.3	0110110	36h	2.7			
0011011	1Bh	1.35	0110111	37h	2.75			

Restriction	

24）R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	PTH_ENB	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode
PTH_ENB	0:Source output enable follow HRST and HRED 1:Source output disable

Note:
No matter HRST[1:0] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

Gates scan both inside and outside of the partial window.

Restriction

25）R8FH (AREA_EN): MTP Area Enable Setting Register

R8FH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	0	1	1	1	1	8FH
1st Parameter	W	1	0	0	0	0	AREA[3]	AREA[3]	AREA[3]	AREA[3]	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for fast refresh application. This fast LUT can be placed in an Area other than the normal LUT.

According to the current LUT usage(normal/fast), select the Area to use and decompress it to the SRAM.

AREA[3:0]	MTP Area
0000	Area0
0001	Area1
0010	Area2
0011	Area3
0100	Area4
0101	Area5
0110	Area6
0111	Area7
1000	Area8
1001	Area9
1010	Area10
1011	Area11
1100	Area12
1101	Area13
Other	Disable

Ex: MTP Area

Area0	Normal LUT
Area1	
Area2	
Area3	
Area4	Fast LUT
Area5	
Area6	-
Area7	-
Area8	-
Area...	...

Note:
When using the R8FH CMD, please make sure it's in sleep state (P-OFF).

Restriction

This command only actives when BUSY_N = "1".

26) R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

27)R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

28)R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	.....								-
mth Parameter	R	1	The data of address (n) in the MTP								-

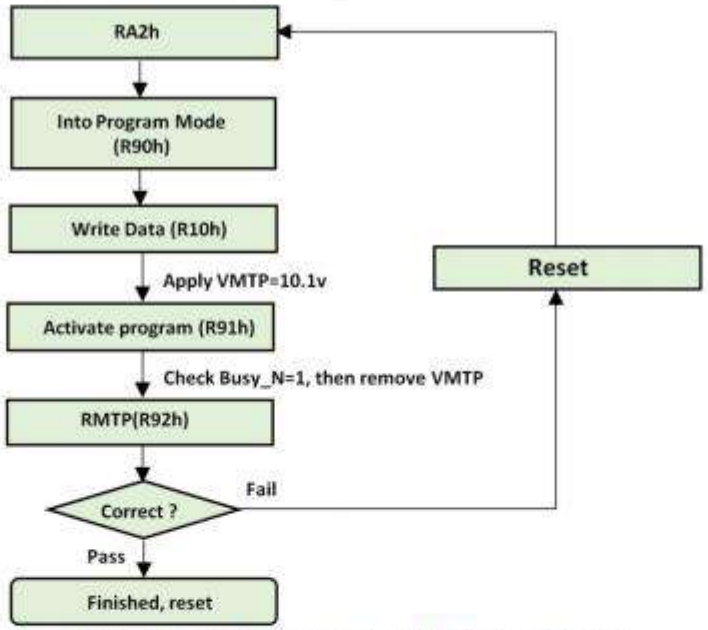
NOTE: "-" Don't care, can be set to VDD or GND level

Description

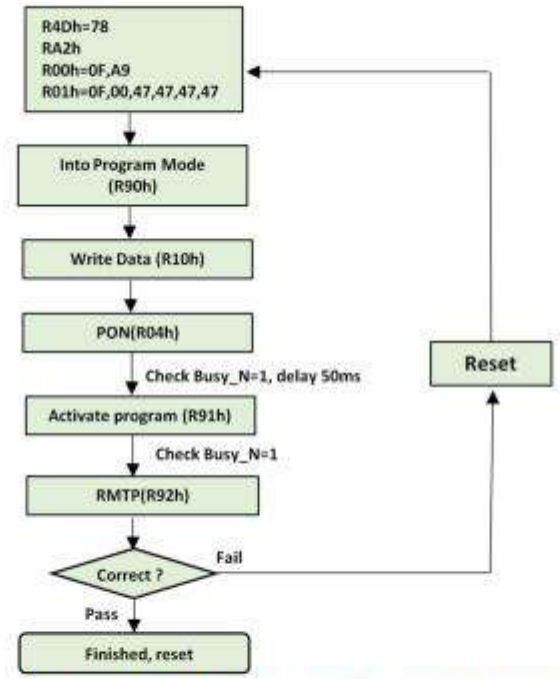
The command define as follows:

-The command is used for reading the content of MTP for checking the data of programming,

-The value of (n) is depending on the amount of programmed data, the max address= 0xFFF



The sequence of programming MTP(External power)



The sequence of programming MTP(Internal power)

Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

29) R9FH (RMRB) Read MTP Reserved Bytes

R9FH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMRB	W	0	1	0	0	1	1	1	1	1	9FH
1st Parameter	R	1	Dummy								00h
2nd Parameter	R	1	The data of address 0x1500 in the MTP								00h
3rd Parameter	R	1	:								00h
:	R	1	:								00h
222th Parameter	R	1	:								00h
223th Parameter	R	1	:								00h
224th Parameter	R	1	The data of address 0x15DF in the MTP								00h

Description	-The command define as follows: The command is used for reading the content of MTP Reserved Byte for checking the data of programming. This command could read these information from MTP directly. Note: 1. The R9Fh can only read the range from 0x1500 to 0x15DF.
Restriction	

30) RA2H (PGM_CFG): MTP Program Config Register

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM_CFG	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
2nd Parameter	W	1	PGM_SADDR[15:8]								00h
3rd Parameter	W	1	PGM_SADDR[7:0]								00h
4th Parameter	W	1	PGM_DSIZE[15:8]								17h
5th Parameter	W	1	PGM_DSIZE[7:0]								84h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for setting configuration of MTP

1st Parameter:

Bit	Name	Description
0	S_dis	0: slave enable some command (default) 1: slave disable some command
1	M_dis	0: master enable some command (default) 1: master disable some command
4	VMTPSEL	0:External VMTP (default) 1:Internal VMTP

Bit[0] enable/disable some command when IC sets slave (MS pin is low)
Bit[1] enable/disable some command when IC sets master (MS pin is high)

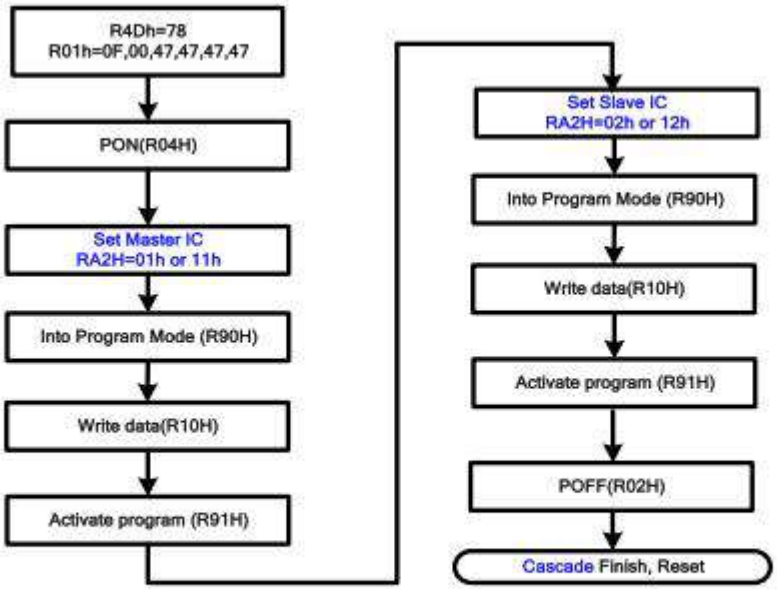
Note:
Some command define: R00H(Parameter 1) (PSR), R10H(DTM), R90H(PGM), R91H(APG), R83H(PTLW)

Command read

M_dis	S_dis	Description
0	0	command read from master
0	1	command read from master
1	0	command read from slave
1	1	command read from slave

2nd & 3rd Parameters: Program and Read MTP start address PGM_SADDR[15:0]
4th & 5th Parameters: Program data size PGM_DSIZE[15:0]

Note:
If user program Area0 (0x00~0x017F), PGM_SADDR[15:0] will be set 0x0000, PGM_DSIZE[15:0] will be set 0x0180.

	Cascade MTP Flow 
Restriction	

31) RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	-	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter: Bit: 0 Name: CCEIN Description: Output clock enable/disable. 0: Output 0V at SyncC pin. (default) 1: Output clock at SyncC pin for slave chip.
Restriction	

32) RE3H (PWS): Power Saving Register

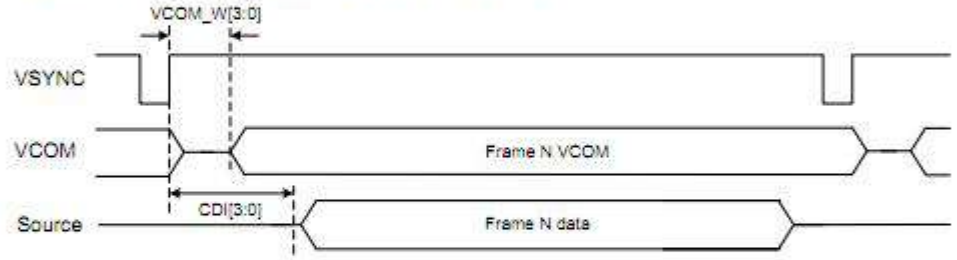
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h
2st Parameter	W	1	-	GD_WR[2:0]			-	GD_WF[2:0]			00h

NOTE: "-" Don't care, can be set to VDD or GND level

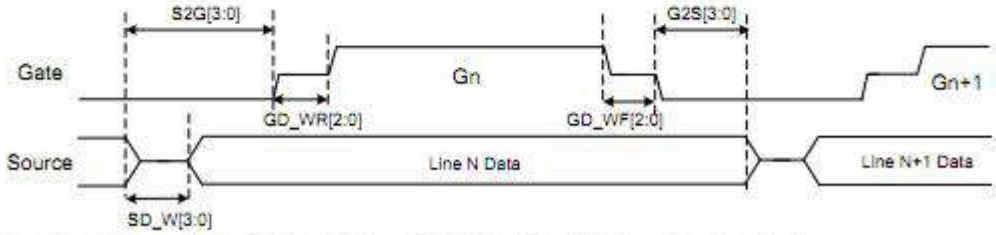
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 500nS), SD_W<=S2G
GD_WR/GD_WF: Gate power saving width (unit = 500nS)



Gon_T = 1 line period – S2G – G2S – GD_WR – GD_WF, Gon_T min= 2 units.

Restriction

33) RE4H (LVSEL): LVD Voltage Select Register

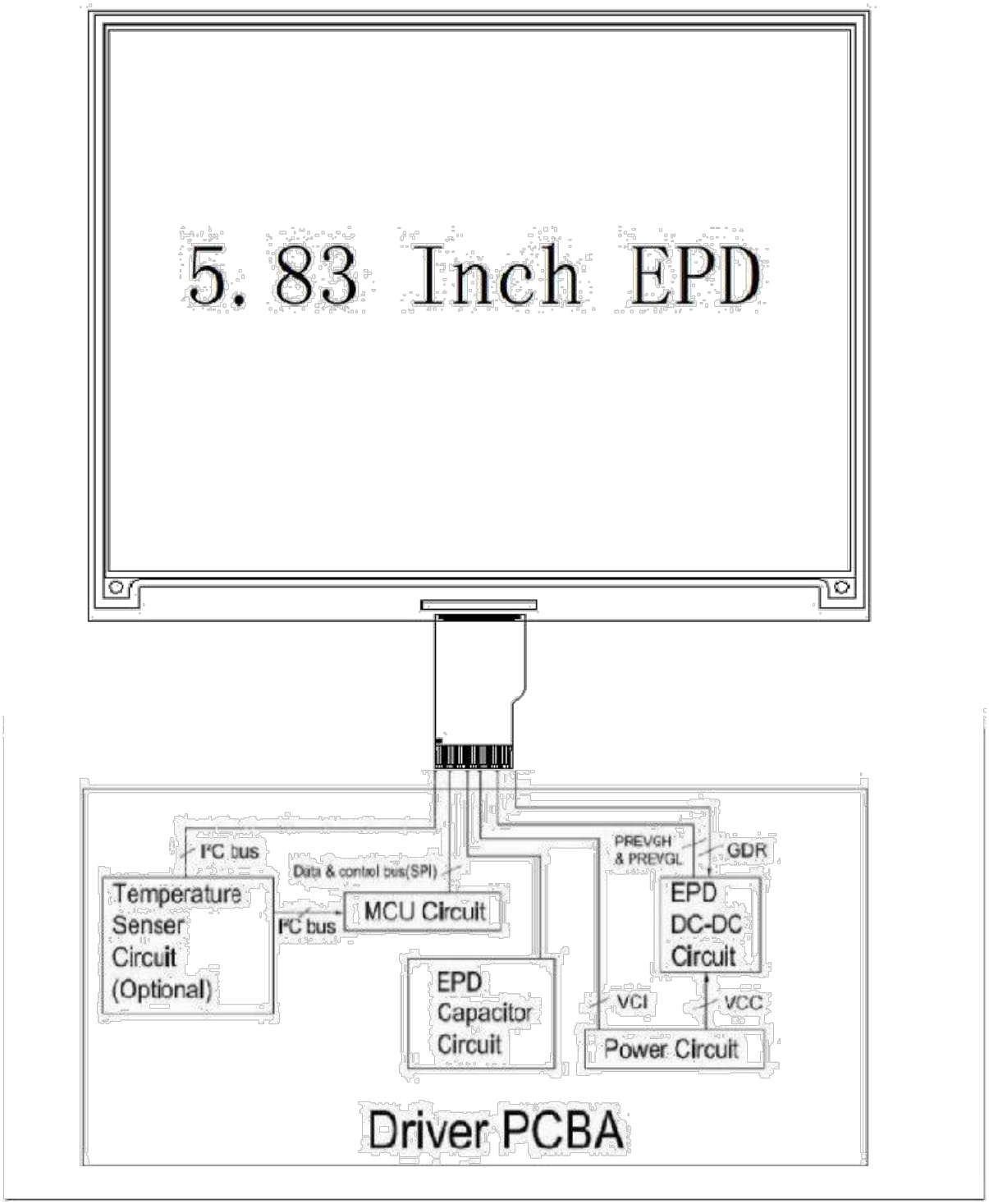
RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

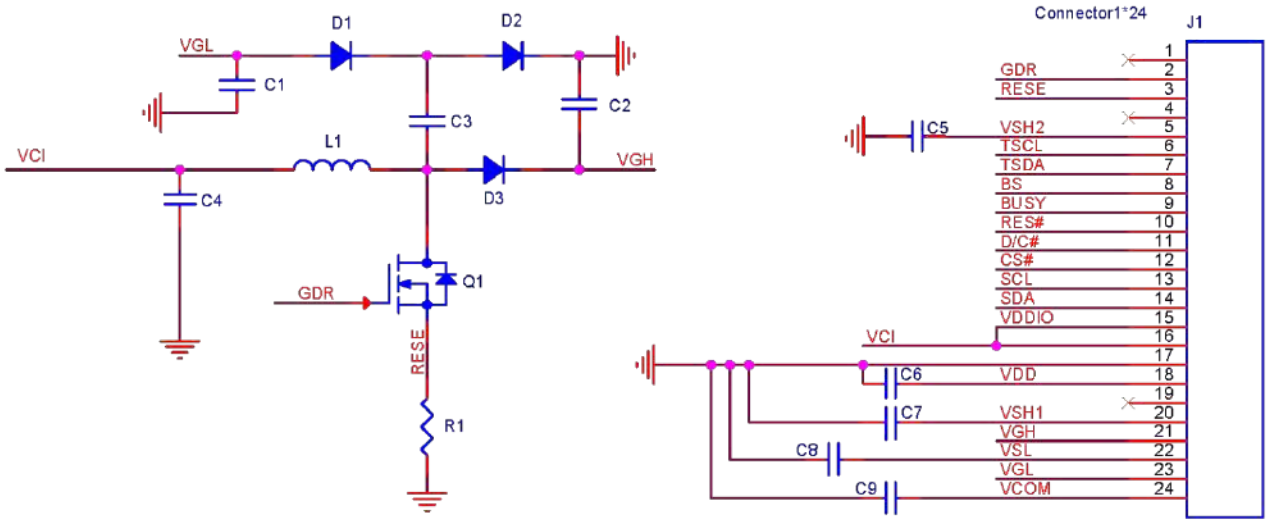
Description	LVD_SEL[1:0]: Low Power Voltage Selection
Restriction	

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

8. Block Diagram



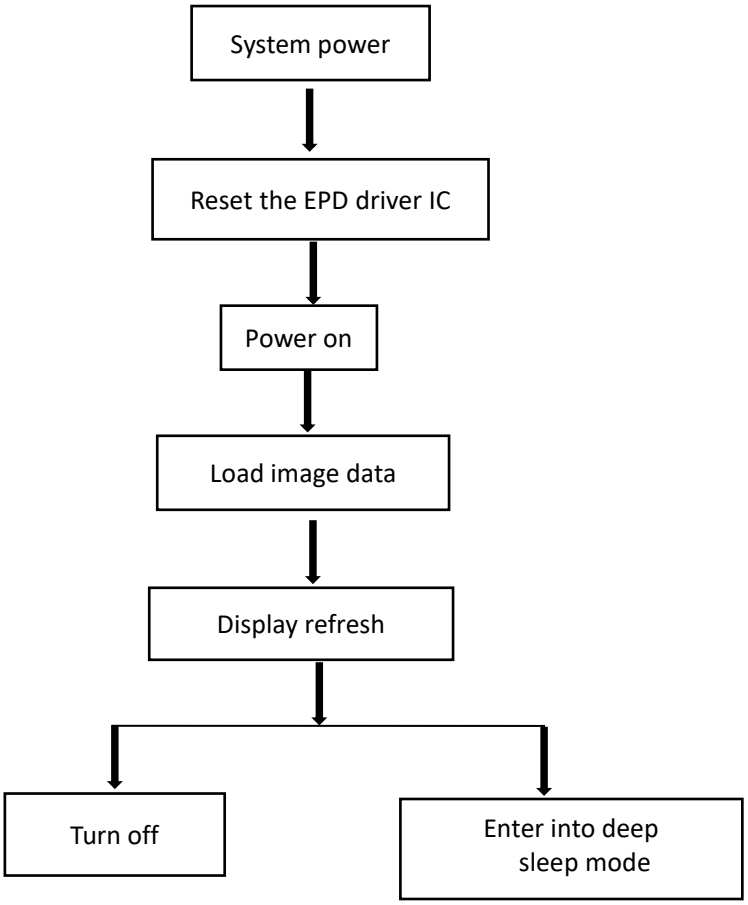
9. Typical Application Circuit with SPI Interface



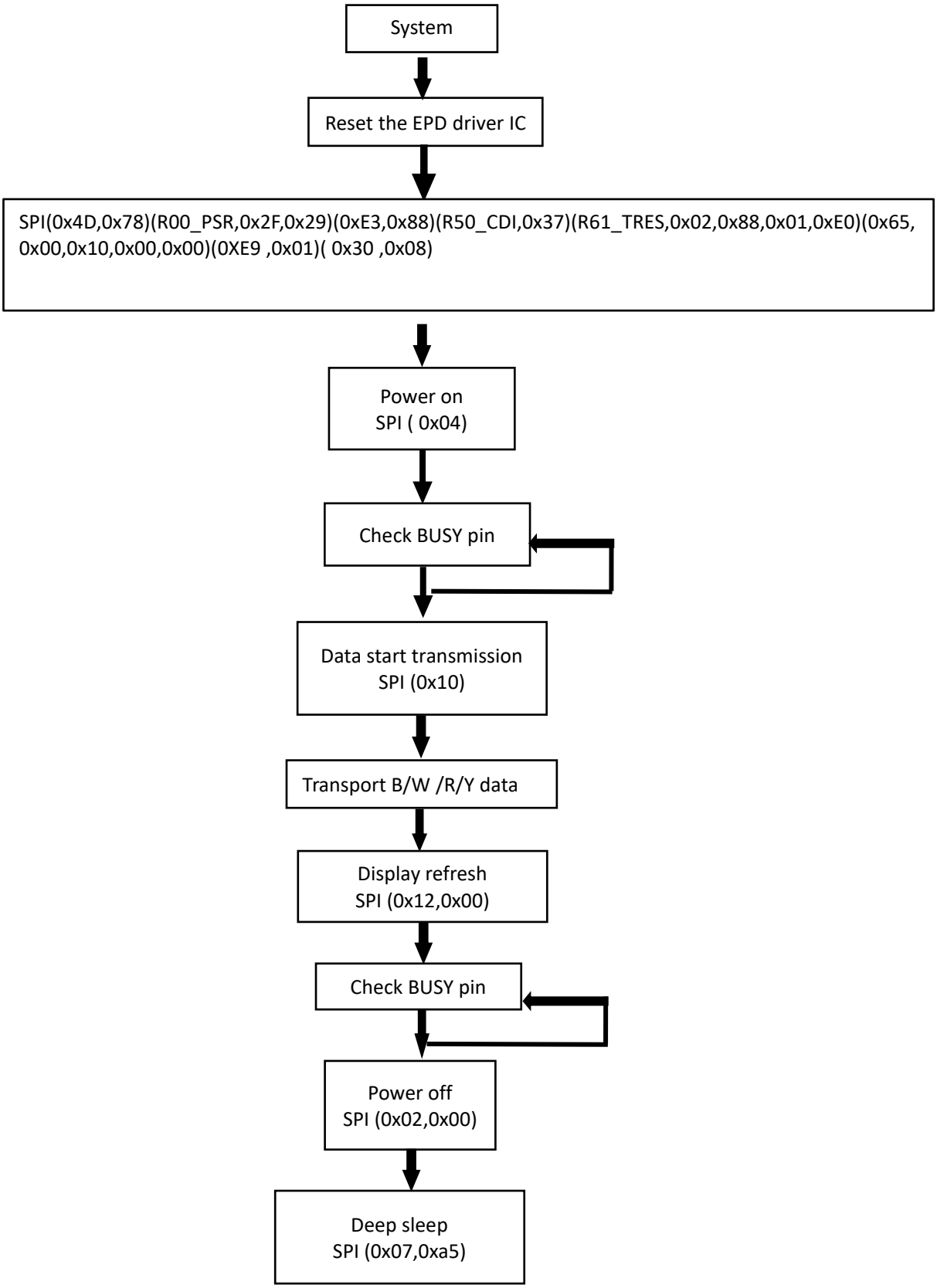
Part Name	Value	Reference Part
C3 C4 C6 C9	1uF	0603, X5R/X7R, voltage rating : 25V
C1C2	4.7uF	0603, X5R/X7R, voltage rating : 35V
C5C7C8	4.7uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
D1 D2 D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47UH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ

10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 OTP Operation Reference Program Code



11. Reliability Test

NO	Test items	Test condition
	Low-Temperature Storage	T = -25°C，500 h Test in white pattern
	High-Temperature Storage	T=60ºC，RH=35%，500h Test in white pattern
	High-Temperature Operation	T=40ºC，RH=35%， 500h
	Low-Temperature Operation	0ºC，500h
	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，500h
	High-Temperature, High-Humidity Storage	T=60ºC，RH=80%，500h Test in white pattern
	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 100 cycles Test in white pattern
	ESD Gun	Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBMC:100pF;R:1.5k ohm) Contact+/-200V(MMC:200pF;R:0 ohm) (Naked EPD display,including IC and FPC area)
	Vibration test	Frequency: 10-500Hz Direction: X, Y, Z Duration: 1 hour in each direction
	Dropping test	The test height is determined by the weight of the test object. Weight ≤20KG, drop height 1000mm Weight ≤50KG, drop height 500mm Weight ≤100KG, drop height 250mm

Note：1. Stay white pattern for storage and non-operation test.

2. Operation is black→white→red→yellow pattern, the interval is 150s.

3. Put in 20℃--25℃ for 1hour after test finished, The function ,appearance and display performance is OK.

12.Quality Assurance

12.1 Environment

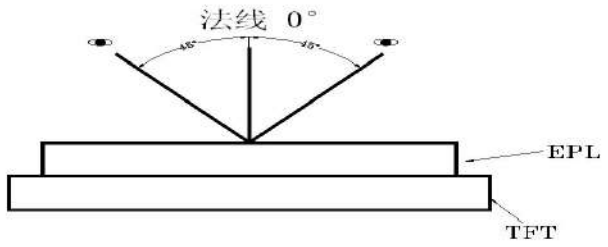
Temperature： 23±3℃

Humidity： 55±10%RH

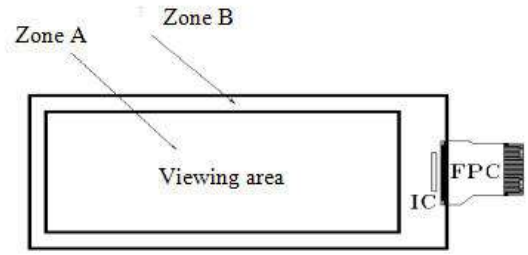
12.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

12.3 Inspect method

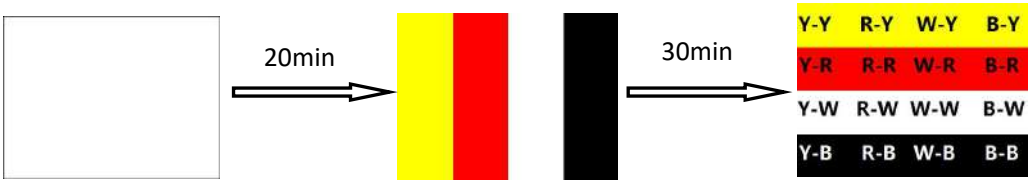


12.4 Display area



12.5 Ghosting test method

Four-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by ODNA.



1)Measurement Instruments：X-rite i1Pro

2)Ghosting formula:

W ghosting：△E= Max (Δ Eab(Y-W, R-W), Δ Eab(Y-W, W-W), Δ Eab(Y-W, B-W), Δ Eab(R-W, W-W), Δ Eab(R-W, B-W), Δ Eab(W-W, B-W))

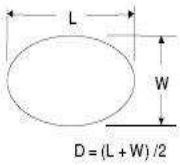
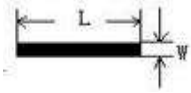
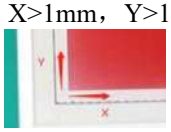
K ghosting：△E= Max (Δ Eab(Y-B, R-B), Δ Eab(Y-B, W-B), Δ Eab(Y-B, B-B), Δ Eab(R-B, W-B), Δ Eab(R-B, B-B), Δ Eab(W-B, B-B))

R ghosting：△E= Max (Δ Eab(Y-R, R-R), Δ Eab(Y-R, W-R), Δ Eab(Y-R, B-R), Δ Eab(R-R, W-R), Δ Eab(R-R, B-R), Δ Eab(W-R, B-R))

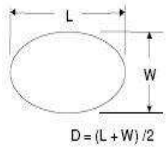
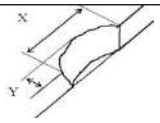
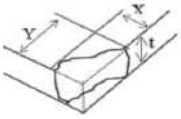
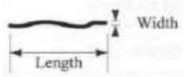
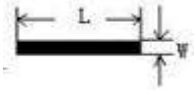
Y ghosting：△E= Max (Δ Eab(Y-Y, R-Y), Δ Eab(Y-Y, W-Y), Δ Eab(Y-Y, B-Y), Δ Eab(R-Y, W-Y), Δ Eab(R-Y, B-Y), Δ Eab(W-Y, B-Y))

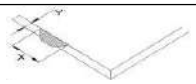
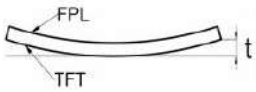
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display、 Display complete、Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.3mm，negligible 0.3mm＜D≤0.5mm, N≤5，Allowed 0.5mm＜D Not Allow	MI	Visual Inspection card	Zone A
3	Black/White lines (No switch)	 W≤0.2mm，negligible 0.2mm＜W≤0.4mm L≤8.0mm N≤4 allowable L＞8.0mm ,W＞0.4mm is not allowed	MI	Visual Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual	Zone A
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection card	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow	MA	Visual	Zone A
8	Corner mura	X>1mm，Y>1mm,not allow 	MI	Visual/Ruler	Zone A

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm，N≤5 D＞0.5mm，Not Allow	MI	Visual/ inspection Card	Zone A
2	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm t= not counted，and without affecting the electrode , permissible  X≤2mm or Y≤2mm t= not counted.and without affecting the electrode , permissible  W≤0.1mm,L≤5mm, without affecting the electrode , n≤2	MI	Visual / Ruler	Zone A/B
3	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A/B
4	Dirty/ foreign body	Allowed if can be removed	MI	Visual / clean cloth	Zone A / B
5	FPC broken/ FPC oxidation / scratch	 Not Allow	MA	Visual / Microscope	Zone B
6	B/W Line	 W≤0.2mm，negligible 0.2mm＜W≤0.4mm L≤8.0mm N≤4 allowable L＞8.0mm ,W＞0.4mm is not allowed	MI	Visual / Ruler	Zone A

7	TFT edge bulge /TFT chromatic aberration	 TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A/B
8	Electrostatic point	D≤0.5mm, allow 0.5mm＜D≤0.6mm , n≤5 allow D＞0.6mm is not allowed	MI	Visual /inspection card	Zone A
9	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MA	Visual / Ruler	Zone B
10	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives overflow onto protect film ≤1/2 FPL to PS Margin width Length excluding Edge adhesives seep in≤1/2 FPL Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤5.0mm。n≤5	MI	Visual / Ruler	Zone B
11	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual	Zone A/B
12	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC≤1.0mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual/Ruler	Zone B
13	Warp degree (TFT substrate)	 t≤1.5mm	MI	Ruler	Zone B
14	Color difference in COM area (Silver point area)	Allowed	MI	Visual	Zone B
15	Corner and edge damage of FPL	Corner and edge damage ≤ 1/2 border width 	MI	Visual / Ruler	Zone A

13. Packaging

TBA

14.Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
Transport environment	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	