Specification for OLED

AOM25664A0-3.12WW-ANO

Revision 1.0

AO	Orient Display Passive Matrix OLED
M	Monochrome
25664	Resolution 256 x 64
A0	Revision A0
3.12	Diagonal: 3.12’’, Module: 100.5(W) x33.5(H) x 6.3(T)mm
W	White Character
W	Top: -40~+80°C; Tstr: -40~+90°C
ANO	4-line SPI/Compatible Arduino
/	All Viewing Angle
/	Controller SSD1322UR1 Or Compatible

Table of Contents

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2019-02-09	First Release.	Written by HCX

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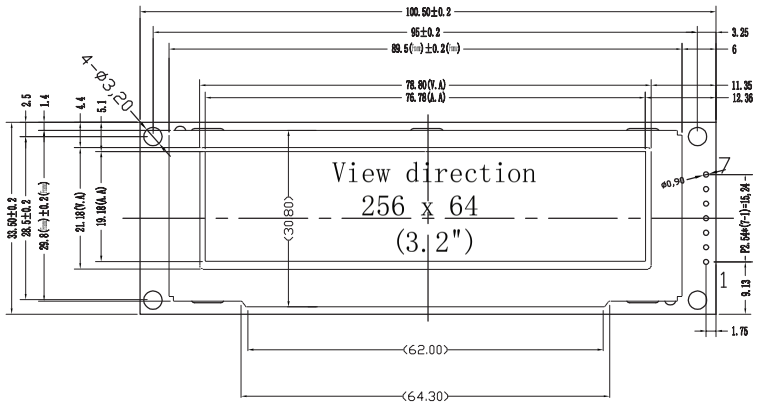
14925 SE Allen Road, Suite 203 B, Bellevue, WA 98006
Tel: (425)698-1938 Fax: (425)698-1852

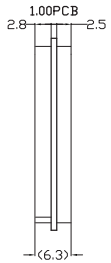
■ PHYSICAL DATA（物理参数）

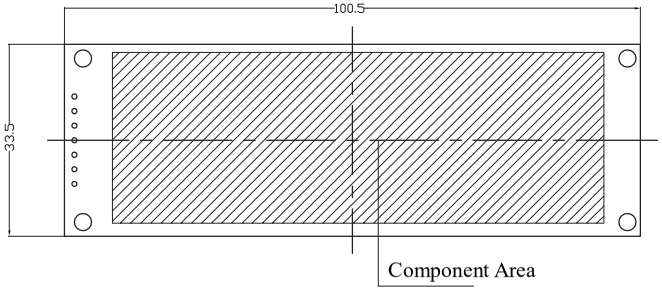
NO. 编号	Items 项目	Specification 规格	Unit 单位
1	Diagonal Size 尺寸	3.12	Inch
2	Resolution 分辨率	256x 64	Dots
3	Active Area 有效显示区域	76.78 (W) x 19.18 (H)	mm^2
4	Outline Dimension 外围尺寸	100.50 (W) x33.50 (H) x 6.3(T)	mm^2
5	Pixel Pitch 像素间距	0.30 (W) x 0.30 (H)	mm^2
6	Pixel Size 像素尺寸	0.28(W) x 0.28 (H)	mm^2
7	Driver IC 驱动 IC	SSD1322UR1	-
8	Display Color 显示色彩	White/Blue/Yellow/Green Optional	-
9	Gray Scale 灰阶	16	Bit
10	Interface 接口	SPI	-
11	IC Package Type IC 封装类型	COF	-
12	Module Connecting Type 模块连接方式	7 Header Pin	-
13	Thickness 厚度	6.30 ±0.3	mm
14	Weight 重量	TBD	g
15	Duty 占空比	1/64	-

ITEAM	PARAMETERS	ITEAM	PARAMETERS	ITEAM	PARAMETERS	ITEAM	PARAMETERS
DISPLAY TYPE	OLED	VIEWING DIRECTION	FREE	LCD OPERATING VOLTAGE	12.0V	IC	SSD1322UR1
RESOLUTION (H*V)	3.12" 256*64 PIXELS	OPERATION TEMPERURE	-40℃ TO +80℃	LOGIC VOLTAGE	/	BACKLIGHT	/
DISPLAY COLOR	WHITE/BLUE/YELLOW/GREEN	STORAGE TEMPERATURE	-40℃ TO +90℃	SURFACE LUMINANCE	140 Nits	CONNECTOR	7 HEADER PIN FPC

1. Outline Diagram







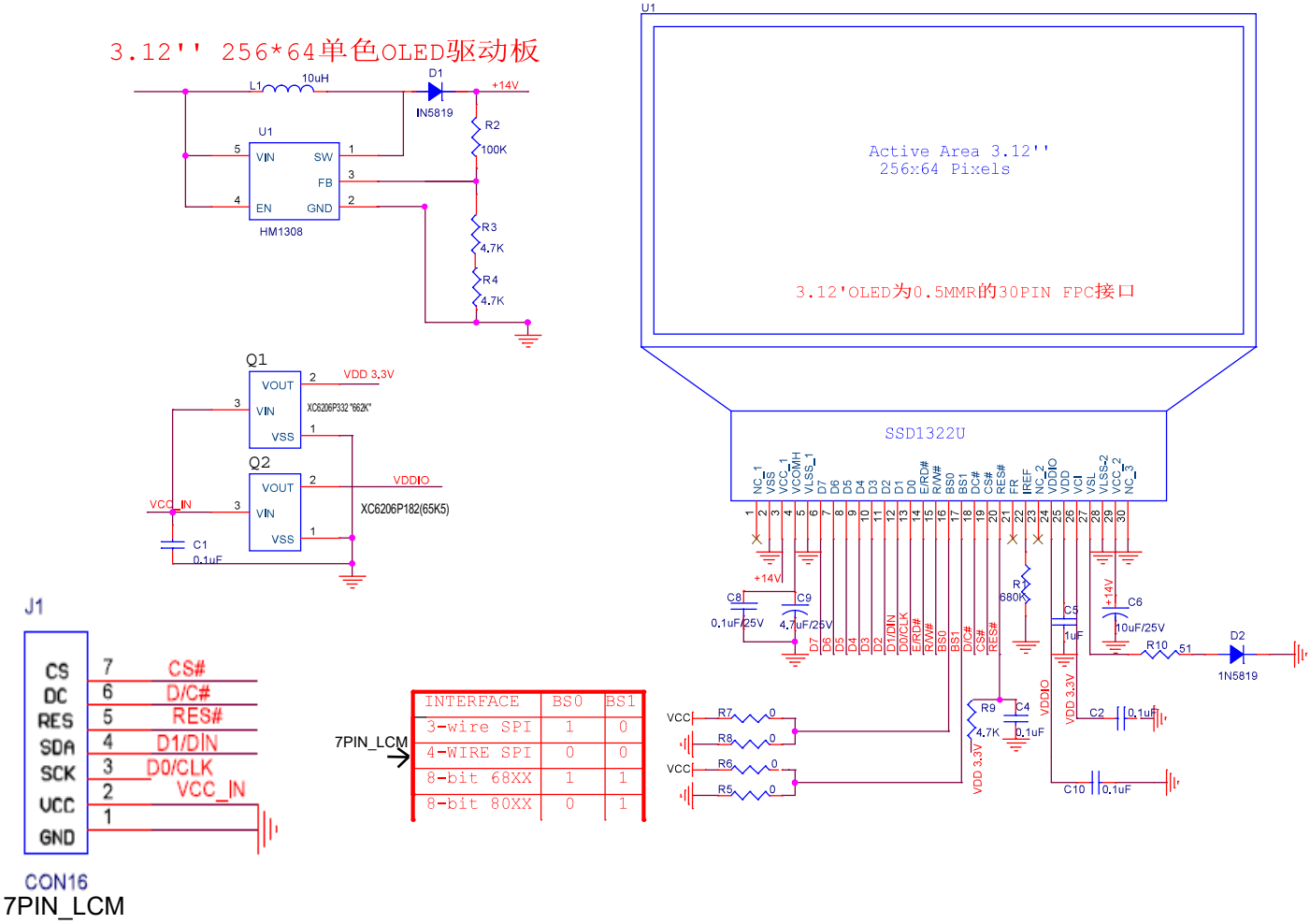
PIN	ASSIGNMENT
1	GND
2	VCC_IN
3	SCK
4	SDA
5	RES
6	DC
7	CS

ORIENT DISPLAY

TITLE	OLED	PART NO.	AOM25664A0-3.12WW-ANO		
REV.	V1.0	CUSTOMER NO.	AOM25664A0-3.12WW-ANO		
SCALE	FIT	UNIT	mm	3rd ANGLE	SHEET 1 of 1
ROHS/REACH COMPLIANT		YES	CUSTOMER'S APPROVAL		
UNMARKED TOLERANCE		±0.2			

REV.	SYMBOL	DESCRIPTION	DATE
V1.0	-	FIRST ISSUE	APR-30-2021

3. Schematic Diagram



注意：电路及元件值仅作参考

4. Interface Pin Definition

PIN	SYMBOL	Descriptions
1	GND	Ground of Logic Circuit
2	VDD	Power Supply for Logic
3	SCK	Serial clock input.
4	SDA	Serial data input.
5	RST	This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
6	DC	This pin is Data/Command control pin. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register.
7	CS	Chip Select. Chip is selected when CS0 = "L".

5. ELECTRICAL CHARACTERISTICS

5.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	651	12	12.5	V
High Level Input	V_{IH}		$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	26.3	32.9	mA
		Note 5	-	41.1	51.4	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		--	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$			1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{CI} = 2.8V, V_{CC} = 12V, 50% Display Area Turn on.
Note 5: V_{CI} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

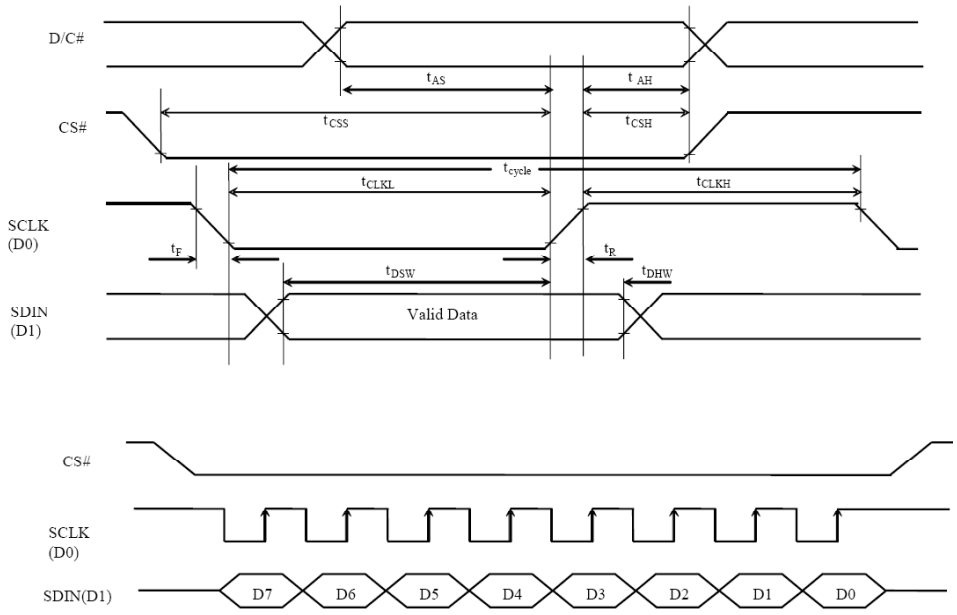
* Software configuration follows Section 4.4 Initialization.

5.2 AC Characteristics

Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



6. Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 00b, Disable Dual COM mode [reset] 01b, Enable Dual COM mode (MUX ≤ 63) **Note** (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>A2
A[6:0]</td><td>1
*</td><td>0
A_6</td><td>1
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Display Offset</td><td>Set vertical scroll by COM from 0-127
The value is reset to 00H after RESET</td></tr>
<tr><td>0</td><td>A4~A7</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Display Mode</td><td>A4h = Entire Display OFF, all pixels turns OFF in GS level 0

A5h = Entire Display ON, all pixels turns ON in GS level 15

A6h = Normal Display [reset]

A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)</td></tr>
<tr><td>0
1
1</td><td>A8
A[6:0]
B[6:0]</td><td>1
0
0</td><td>0
A_6
B_6</td><td>1
A_5
B_5</td><td>0
A_4
B_4</td><td>1
A_3
B_3</td><td>0
A_2
B_2</td><td>0
A_1
B_1</td><td>0
A_0
B_0</td><td>Enable Partial Display</td><td>This command turns ON partial mode. The partial mode display area is defined by the following two parameters,

A[6:0]: Address of start row in the display area
B[6:0]: Address of end row in the display area,
where B[6:0] must be ≥ A[6:0]</td></tr>
<tr><td>0</td><td>A9</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Exit Partial Display</td><td>This command is sent to exit the Partial Display mode</td></tr>
<tr><td>0
1</td><td>AB
A[0]</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
A_0</td><td>Function Selection</td><td>A[0]=0b, Select external V_{DD}
A[0]=1b, Enable internal V_{DD} regulator [reset]</td></tr>
<tr><td>0</td><td>AE~AF</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>X_0</td><td>Set Sleep mode ON/OFF</td><td>AEh = Sleep mode ON (Display OFF)
AFh = Sleep mode OFF (Display ON)</td></tr>
<tr><td>0
1</td><td>B1
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Phase Length</td><td>A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow:

<table><tr><th>A[3:0]</th><th>Phase 1 period</th></tr><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>5 DCLKs</td></tr><tr><td>0011</td><td>7 DCLKs</td></tr><tr><td>0100</td><td>9 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>31 DCLKs</td></tr></table>
A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow:

<table><tr><th>A[7:4]</th><th>Phase 2 period</th></tr><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>invalid</td></tr><tr><td>0011</td><td>3 DCLKs</td></tr><tr><td>:</td><td>:</td></tr><tr><td>0111</td><td>7 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>15 DCLKs</td></tr></table></td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>B3
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Front Clock Divider / Oscillator Frequency</td><td>A[3:0] [reset=0], divide by DIVSET where
<table><tr><th>A[3:0]</th><th>DIVSET</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
A[7:4] Oscillator frequency, frequency increases as level increases [reset=1100b]</td></tr>
<tr><td>0
1</td><td>B5
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set GPIO</td><td>A[1:0] GPIO0: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH

A[3:2] GPIO1: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH</td></tr>
<tr><td>0
1</td><td>B6
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Second Precharge Period</td><td>A[3:0] Second Pre-charge period
0000b 0 dclk
0001b 1 dclk
……
1000b 8 dclks [reset]
……
1111b 15 dclks</td></tr>
<tr><td>0
1
1
1
1
1
1
1</td><td>B8
A1[7:0]
A2[7:0]
.
.
.
A14[7:0]
A15[7:0]</td><td>1
$A1_7$
$A2_7$
.
.
.
$A14_7$
$A15_7$</td><td>0
$A1_6$
$A2_6$
.
.
.
$A14_6$
$A15_6$</td><td>1
$A1_5$
$A2_5$
.
.
.
$A14_5$
$A15_5$</td><td>1
$A1_4$
$A2_4$
.
.
.
$A14_4$
$A15_4$</td><td>1
$A1_3$
$A2_3$
.
.
.
$A14_3$
$A15_3$</td><td>0
$A1_2$
$A2_2$
.
.
.
$A14_2$
$A15_2$</td><td>0
$A1_1$
$A2_1$
.
.
.
$A14_1$
$A15_1$</td><td>0
$A1_0$
$A2_0$
.
.
.
$A14_0$
$A15_0$</td><td>Set Gray Scale Table</td><td>The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK’s (ranges from 0d ~ 180d)

A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2,
:
A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15

Note
[1] 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3 .... < Setting of GS14 < Setting of GS15

Refer to Section 8.8 for details

[2] The setting must be followed by the Enable Gray Scale Table command (00h)</td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>B9</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Select Default Linear Gray Scale table</td><td>The default Linear Gray Scale table is set in unit of DCLK's as follow

GS0 level pulse width = 0;
GS1 level pulse width = 0;
GS2 level pulse width = 8;
GS3 level pulse width = 16;
:
:
GS14 level pulse width = 104;
GS15 level pulse width = 112

Refer to Section 8.8 for details</td></tr>
<tr><td>0
1</td><td>BB
A[4:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Pre-charge voltage</td><td>Set pre-charge voltage level.[reset = 17h]
<table><tr><th>A[5:1]</th><th>Hex code</th><th>pre-charge voltage</th></tr><tr><td>00000</td><td>00h</td><td>0.20 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>11111</td><td>3Eh</td><td>0.60 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>BE
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>1
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set V_{COMH}</td><td>Set COM deselect voltage level [reset = 04h]
A[3:0] =
<table><tr><th>A[2:0]</th><th>Hex code</th><th>V_{COMH}</th></tr><tr><td>0000</td><td>00h</td><td>0.72 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>0100</td><td>04h</td><td>0.80 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>0111</td><td>07h</td><td>0.86 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>C1
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Contrast Current</td><td>A[7:0]: Contrast current value, range:00h~FFh,
i.e. 256 steps for I_{SEG} current [reset = 7Fh]</td></tr>
<tr><td>0
1</td><td>C7
A[3:0]</td><td>1
*</td><td>1
*</td><td>0
*</td><td>0
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Master Contrast Current Control</td><td>A[3:0] =
0000b, reduce output currents for all colors to 1/16
0001b, reduce output currents for all colors to 2/16
:
1110b, reduce output currents for all colors to 15/16
1111b, no change [reset]</td></tr>
<tr><td>0
1</td><td>CA
A[6:0]</td><td>1
*</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set MUX Ratio</td><td>A[6:0]: Set MUX ratio from 16MUX ~ 128MUX

A[6:0] = 15d represents 16MUX
:
A[6:0] = 127d represents 128MUX [reset]</td></tr>
<tr><td>0
1</td><td>FD
A[2]</td><td>1
0</td><td>1
0</td><td>1
0</td><td>1
1</td><td>1
0</td><td>1
A_2</td><td>0
1</td><td>1
0</td><td>Set Command Lock</td><td>A[2]: MCU protection status [reset = 12h]

A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset]
A[2] = 1b, Lock OLED driver IC MCU interface from entering command

Note
(1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command</td></tr>
</table>

Note

(1) "*" stands for "Don't care".

■ ELECTRO-OPTICAL CHARACTERISTICS (光电参数)

All data in below based the condition (Ta = 22±3℃, 60±10%RH).
以下参数均基于 Ta = 22±3℃,60±10%RH 的条件。

Items 项目		Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Operating Luminance 工作亮度		L	110	140	-	cd /m^2	All pixels ON
Power Consumption 功耗		P	-	260	325	mW	30% pixels ON
Frame Frequency 帧频		Fr	-	100	-	Hz	-
Color Coordinate 色坐标	Yellow	CIE x	0.45	0.49	0.53	CIE1931	Darkroom
		CIE y	0.46	0.50	0.54		
Response Time 响应时间	Rise	Tr	-	10	-	us	-
	Decay	Td	-	10	-	us	-
Contrast Ratio* 对比度		Cr	10000:1	-	-	-	Darkroom
Viewing Angle 可视角		Δθ	160	-	-	Degree	-
Operating Life Time* 工作寿命		Top	33000	-	-	Hours	L= 140 cd/m^2

Note(注意事项）:

1. 140 cd/m^2 is based on V_{CI}=2.8V, V_{CC}=12.0V, Contrast command setting 0x9F;

   140 cd/m^2 基于 V_{CI}=2.8V, V_{CC}=12.0V, 对比度设置为 0x9F;

2. **Contrast ratio** is defined as follows(对比度的定义如下):

$$\text{Contrast ratio 对比度} = \frac{\text{Photo – detector output with OLED being “white” OLED 显示全屏亮时的亮度}}{\text{Photo – detector output with OLED being “black” OLED 显示全屏黑时的亮度}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed). (The initial value should be closed to the typical value after adjusting.)
   寿命的定义为当亮度衰减到初始亮度 50%时所消耗的时间。 (奇数和偶数棋盘交替显示)。(初始亮度值应调试到接近典型值的大小)。

■ RELIABILITY TESTS（可靠性测试）

NO.	Item	Condition	Quantity
1	High Temperature Storage (HTS)	85±2℃, 200 hours	3
2	High Temperature Operating (HTO)	80±2℃, 96 hours	3
3	Low Temperature Storage (LTS)	-40±2℃, 200 hours	3
4	Low Temperature Operating (LTO)	-40±2℃, 96 hours	3
5	High Temperature / High Humidity Storage (HTHHS)	50±3℃, 90%±3%RH, 120 hours	3
6	Thermal Shock (Non-operation) (TS)	-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	3
7	Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1 Carton
8	Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle	1 Carton
9	ESD (finished product housing)	±4kVR:330Ω; C:150pF 10times,air discharge	3

Test and measurement conditions（测试与测量条件）

1. All measurements shall not be started until the specimens attain to temperature stability.
2. The degradation of Polarizer are ignored for item 1, 3 & 4.

Evaluation criteria（评估标准）

1. The function test is ok.
2. No addition to the defect.
3. The change of luminance should be within ±50% of initial value.
4. The change for the color must be within (±0.02)of initial value based on 1931 CIE coordinates.
5. The change of total current consumption should be within ±50% of initial value.
6. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.

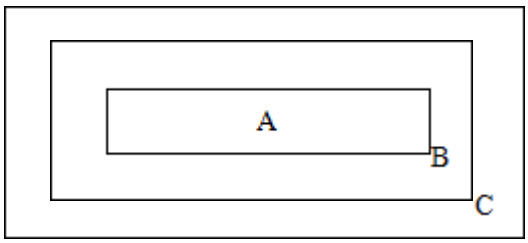
■ OUTGOING QUALITY CONTROL SPECIFICATION（出厂质量控制规范）

◆ Standard（标准）

According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆ Definition（定义）

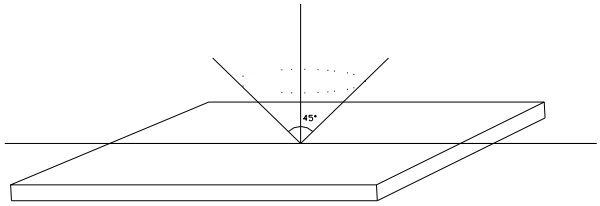
1. Major defect: The defect that greatly affect the usability of product.
2. Minor defect: The other defects, such as cosmetic defects, etc.
3. Definition of inspection zone:



Zone A: Active Area
Zone B: Viewing Area except Zone A
Zone C: Outside Viewing Area
Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆ Inspection Methods（检查方法）

1. The general inspection: under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



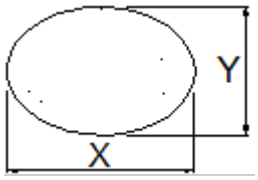
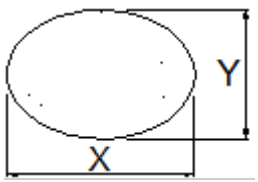
2. The luminance and color coordinate inspection: By CS2000/09A-OLED-117 or the equal equipment, in the dark room, under 25±5℃.

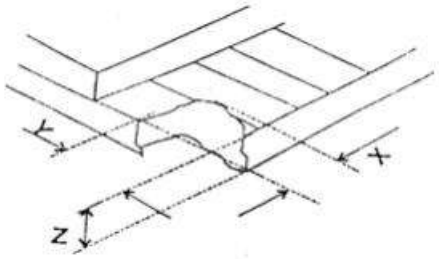
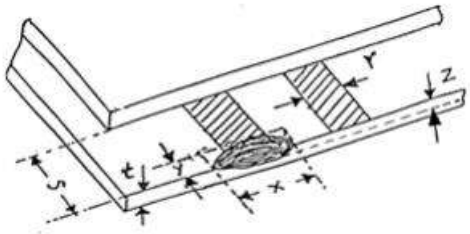
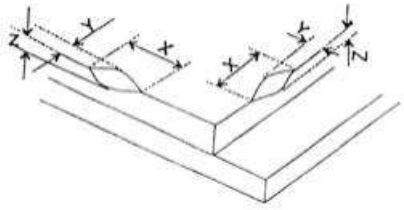
◆ Inspection Criteria（检查标准）

1. Major defect: AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2. Minor Defect: AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="6">Spot Defect
(dimming and
lighting spot)</td><td colspan="2" rowspan="2">Size (mm)</td><td colspan="2">Accepted Qty.</td></tr>
<tr><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.15＜Φ≦0. 20</td><td>1</td></tr>
<tr><td>0.20＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect
(dimming and
lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 PCS. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer
Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below:</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect
(Glass Chipped)</td><td>1. on the corner (mm)
 
<table>
<tr><td>x</td><td>≤ 1.5</td></tr>
<tr><td>y</td><td>≤ 1.5</td></tr>
<tr><td>z</td><td>≤ t</td></tr>
</table></td></tr>
<tr><td>2. On the bonding edge (mm)
 
<table>
<tr><td>x</td><td>≤ a/4</td></tr>
<tr><td>y</td><td>≤ s/3 & ≤0.7</td></tr>
<tr><td>z</td><td>≤ t</td></tr>
</table></td></tr>
<tr><td>3. On the other edges (mm)
 
<table>
<tr><td>x</td><td>≤ a / 8</td></tr>
<tr><td>y</td><td>≤ 0.7</td></tr>
<tr><td>z</td><td>≤ t</td></tr>
</table></td></tr>
<tr><td>Note: t: glass thickness; s: pad width; a: the length of the edge.</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec.</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample.</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample.</td></tr>
</table>