



ORIENT DISPLAY

MAKE THINGS POSSIBLE

Specification for OLED

AOM25664A0-2.8WW-ANO

Revision V1.0



AO	Orient Display Passive Matrix OLED
M	Monochrome
25664	Resolution 256 x 64
A0	Revision A0
2.8	Diagonal: 2.8", Module: 97.0 × 32.5 × 6.4 mm
W	White Character
W	Top: -30~+85°C; Tstr: -40~+90°C
ANO	4-line SPI/Compatible Arduino
/	All Viewing Angle
/	Controller SSD1322 Or Compatible



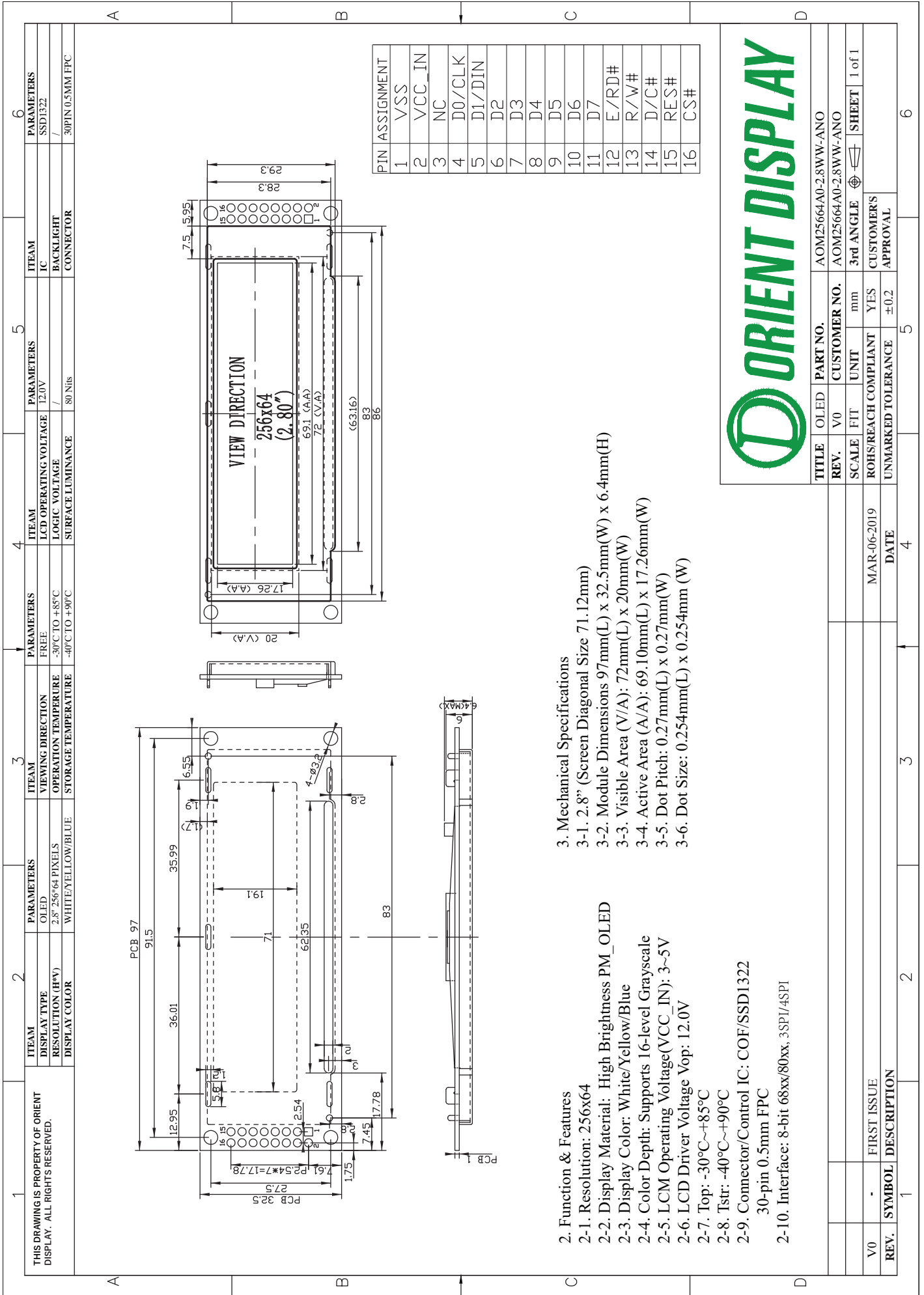
Revision Records

Model Number	Revisions	Details	Date
AOM25664A0-2.8WW-ANO	V1.0		2019-03-07

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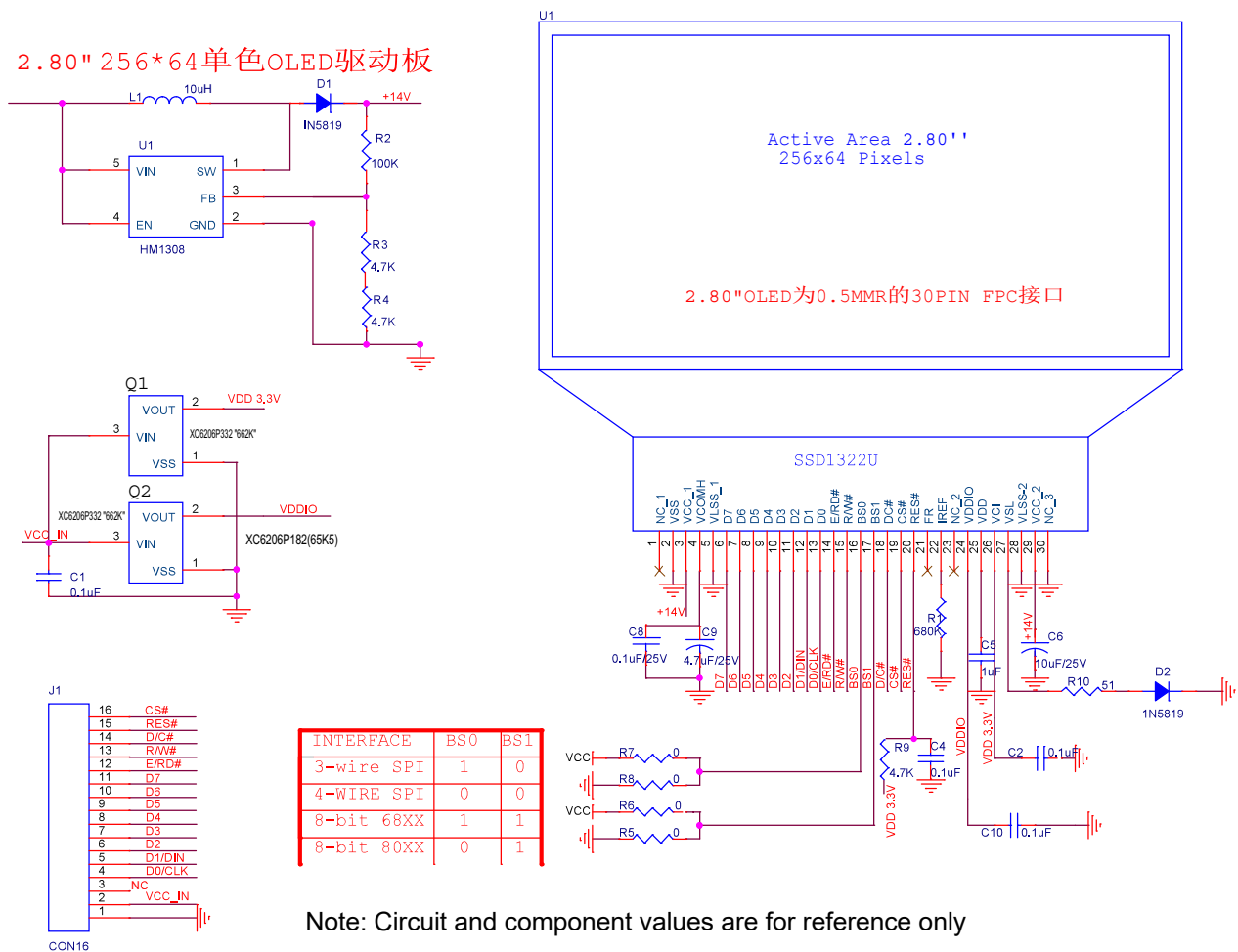
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1. Outline Diagram



	TITLE	OLED	PART NO.	AOM25664A0-2.8WW-ANO	
	REV.	V0	CUSTOMER NO.	AOM25664A0-2.8WW-ANO	
	SCALE	FIT	UNIT	mm	SHEET 1 of 1
V0	•	FIRST ISSUE	ROHS/REACH COMPLIANT	YES	CUSTOMER'S APPROVAL
REV.	SYMBOL DESCRIPTION	DATE	UNMARKED TOLERANCE	±0.2	
		MAR-06-2019			
1	2	3	4	5	6

4. Schematics



5. PIN Description

Pin No.	Symbol	Function
1		Power Ground
2	VCC_IN	Power Positive
3	NC	Empty
4	D0/CLK	Data Line/Serial Clock Line
5	D1/DIN	Data Line/Serial Data Line
6	D2	Data Line
7	D3	Data Line
8	D4	Data Line
9	D5	Data Line
10	D6	Data Line
11	D7	Data Line
12	E/RD#	Enable/Read
13	R/W#	Read/Write
14	D/C#	Data/Command
15	RES#	Reste
16	CS#	Chip Select

6. Optical and Electrical Characteristics

6.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	60	80	-	cd/m ²
C.I.E. (White)	(x)	Without Polarizer	0.28	0.32	0.36	
	(y)		0.29	0.33	0.37	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at $V_{CI} = 2.8V$, $V_{CC} = 12V$.
Software configuration follows Section 4.4 Initialization.

6.2 DC Characteristics • • • • • • • • • •

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	11.5	12	12.5	V
High Level Input	V_{IH}		$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DDIO}$	V
High Level Output	V_{OH}	$I_{out} = 100\mu A, 3.3MHz$	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	$I_{out} = 100\mu A, 3.3MHz$	0	-	$0.1 \times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	26.3	32.9	mA
		Note 5	-	41.1	51.4	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 4: $V_{CI} = 2.8V$, $V_{CC} = 12V$, 50% Display Area Turn on.

Note 5: $V_{CI} = 2.8V$, $V_{CC} = 12V$, 100% Display Area Turn on.

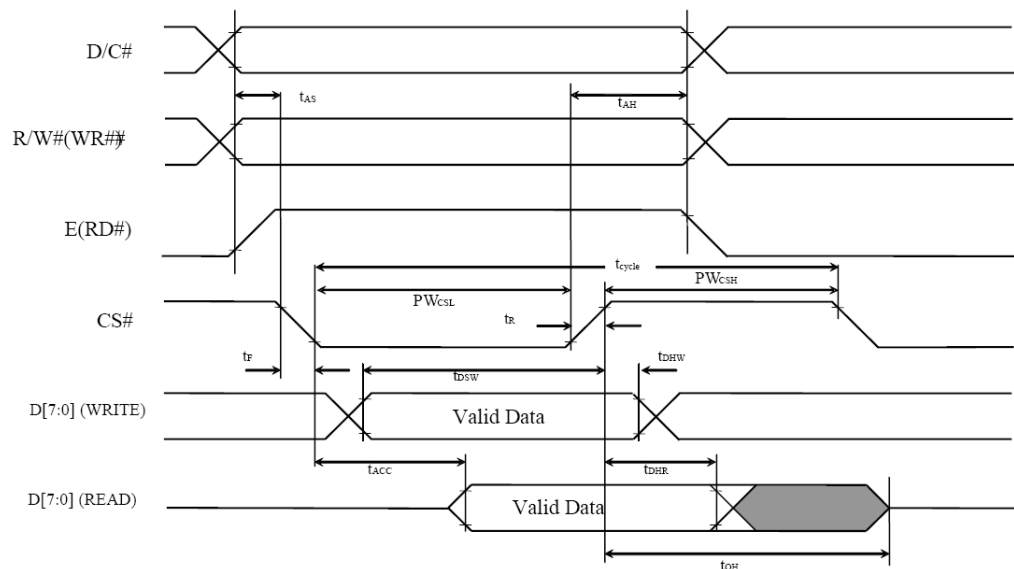
* Software configuration follows Section 4.4 Initialization.

6.3 AC Characteristics

6.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

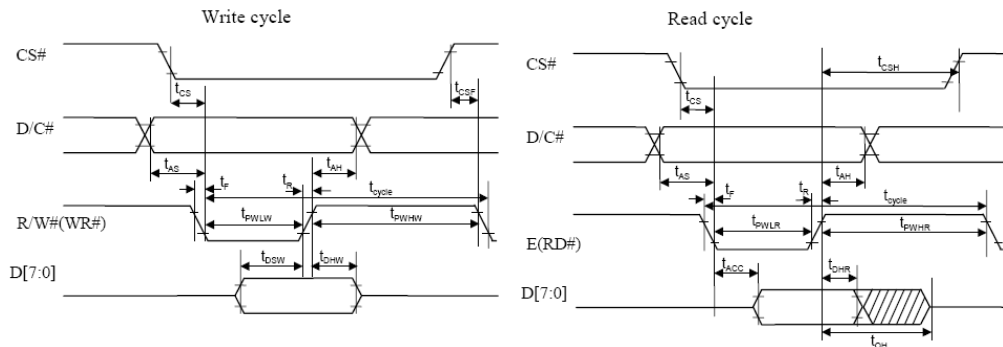
* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



6.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

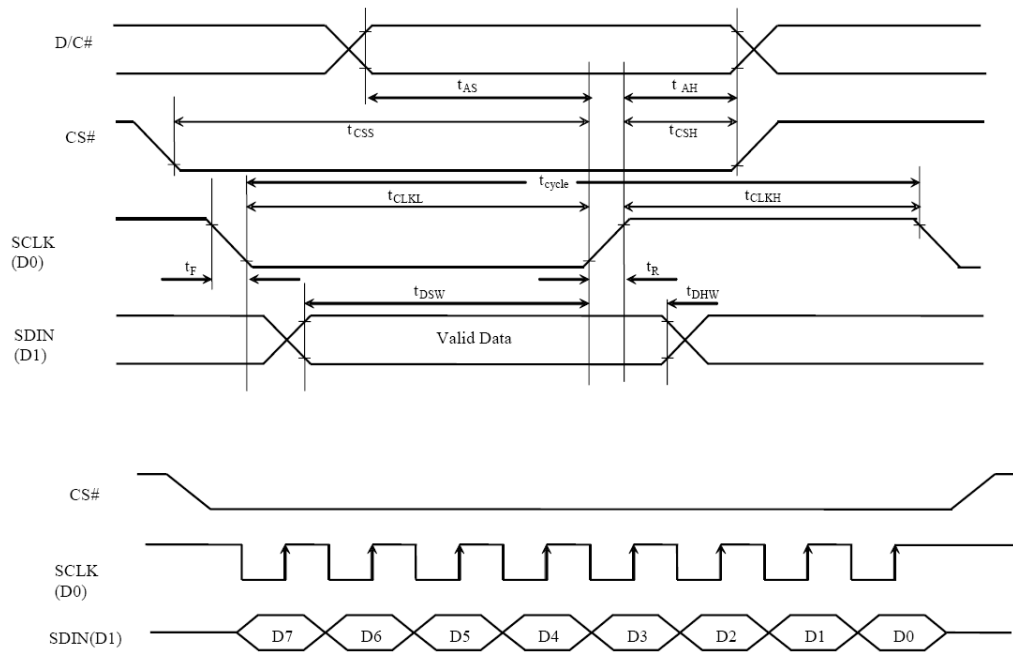
* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



6.3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

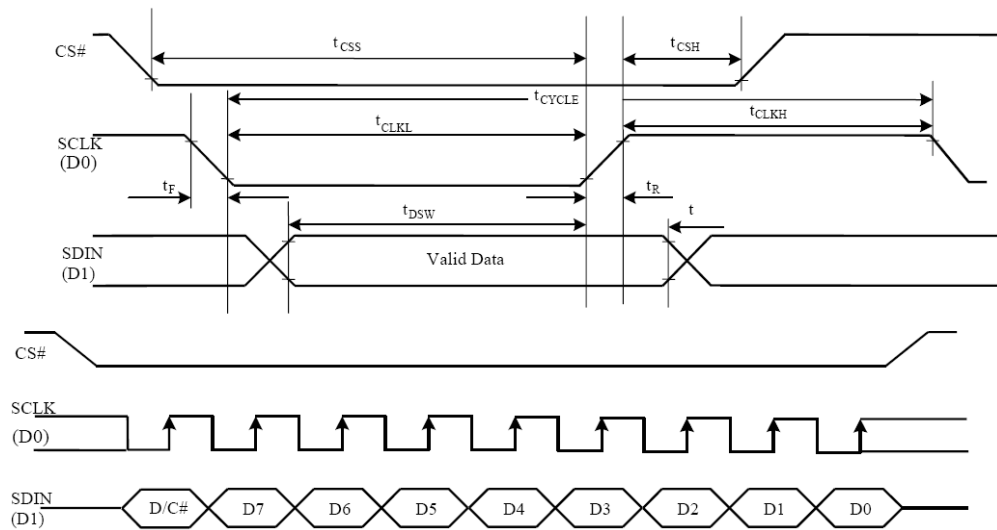
* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



6.3.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

* ($V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$, $V_{\text{DDIO}} = 1.6\text{V}$, $V_{\text{CI}} = 2.8\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



7 • (COMMAND TABLE)

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	A ₆ A ₆ B ₆	A ₅ A ₅ B ₅	A ₄ A ₄ B ₄	A ₃ A ₃ B ₃	A ₂ A ₂ B ₂	A ₁ A ₁ B ₁	A ₀ A ₀ B ₀	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	A ₆ A ₆ B ₆	A ₅ A ₅ B ₅	A ₄ A ₄ B ₄	A ₃ A ₃ B ₃	A ₂ A ₂ B ₂	A ₁ A ₁ B ₁	A ₀ A ₀ B ₀	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A ₅ 0	0 A ₄ B ₄	0 0 0	0 A ₂ 0	0 A ₁ 0	0 A ₀ 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N-1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 00b, Disable Dual COM mode [reset] 01b, Enable Dual COM mode (MUX ≤ 63) Note ⁽¹⁾ COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																																		
0 1	A2 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET																																		
0	A4~A7	1	0	1	0	0	X ₂	X ₁	X ₀	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, ...)																																		
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	1 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	0 A ₀ B ₀	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0]																																		
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode																																		
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A ₀	Function Selection	A[0]=0b, Select external V _{DD} A[0]=1b, Enable internal V _{DD} regulator [reset]																																		
0	AE~AF	1	0	1	0	1	1	1	X ₀	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)																																		
0 1	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: <table border="1" data-bbox="1023 1274 1426 1532"> <thead> <tr> <th>A[3:0]</th> <th>Phase 1 period</th> </tr> </thead> <tbody> <tr><td>0000</td><td>invalid</td></tr> <tr><td>0001</td><td>invalid</td></tr> <tr><td>0010</td><td>5 DCLKs</td></tr> <tr><td>0011</td><td>7 DCLKs</td></tr> <tr><td>0100</td><td>9 DCLKs [reset]</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>31 DCLKs</td></tr> </tbody> </table> A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow: <table border="1" data-bbox="1031 1684 1418 1973"> <thead> <tr> <th>A[7:4]</th> <th>Phase 2 period</th> </tr> </thead> <tbody> <tr><td>0000</td><td>invalid</td></tr> <tr><td>0001</td><td>invalid</td></tr> <tr><td>0010</td><td>invalid</td></tr> <tr><td>0011</td><td>3 DCLKs</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>0111</td><td>7 DCLKs [reset]</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>15 DCLKs</td></tr> </tbody> </table>	A[3:0]	Phase 1 period	0000	invalid	0001	invalid	0010	5 DCLKs	0011	7 DCLKs	0100	9 DCLKs [reset]	:	:	1111	31 DCLKs	A[7:4]	Phase 2 period	0000	invalid	0001	invalid	0010	invalid	0011	3 DCLKs	:	:	0111	7 DCLKs [reset]	:	:	1111	15 DCLKs
A[3:0]	Phase 1 period																																												
0000	invalid																																												
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0100	9 DCLKs [reset]																																												
:	:																																												
1111	31 DCLKs																																												
A[7:4]	Phase 2 period																																												
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1111	15 DCLKs																																												

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																										
0 1	B3 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Front Clock Divider / Oscillator Frequency	<p>A[3:0] [reset=0], divide by DIVSET where</p> <table border="1"> <thead> <tr> <th>A[3:0]</th> <th>DIVSET</th> </tr> </thead> <tbody> <tr><td>0000</td><td>divide by 1</td></tr> <tr><td>0001</td><td>divide by 2</td></tr> <tr><td>0010</td><td>divide by 4</td></tr> <tr><td>0011</td><td>divide by 8</td></tr> <tr><td>0100</td><td>divide by 16</td></tr> <tr><td>0101</td><td>divide by 32</td></tr> <tr><td>0110</td><td>divide by 64</td></tr> <tr><td>0111</td><td>divide by 128</td></tr> <tr><td>1000</td><td>divide by 256</td></tr> <tr><td>1001</td><td>divide by 512</td></tr> <tr><td>1010</td><td>divide by 1024</td></tr> <tr><td>>=1011</td><td>invalid</td></tr> </tbody> </table> <p>A[7:4] Oscillator frequency, frequency increases as level increases [reset=1100b]</p>	A[3:0]	DIVSET	0000	divide by 1	0001	divide by 2	0010	divide by 4	0011	divide by 8	0100	divide by 16	0101	divide by 32	0110	divide by 64	0111	divide by 128	1000	divide by 256	1001	divide by 512	1010	divide by 1024	>=1011	invalid
A[3:0]	DIVSET																																				
0000	divide by 1																																				
0001	divide by 2																																				
0010	divide by 4																																				
0011	divide by 8																																				
0100	divide by 16																																				
0101	divide by 32																																				
0110	divide by 64																																				
0111	divide by 128																																				
1000	divide by 256																																				
1001	divide by 512																																				
1010	divide by 1024																																				
>=1011	invalid																																				
0 1	B5 A[3:0]	1 *	0 *	1 *	1 *	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set GPIO	<p>A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH</p> <p>A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH</p>																										
0 1	B6 A[3:0]	1 *	0 *	1 *	1 *	0 A ₃	1 A ₂	1 A ₁	0 A ₀	Set Second Precharge Period	<p>A[3:0] Second Pre-charge period</p> <p>0000b 0 dclk 0001b 1 dclk 1000b 8 dclks [reset] 1111b 15 dclks</p>																										
0 1 1 1 1 1 1	B8 A1[7:0] A2[7:0] . . . A14[7:0] A15[7:0]	1 A1 ₇ A2 ₇ . . . A14 ₇ A15 ₇	0 A1 ₆ A2 ₆ . . . A14 ₆ A15 ₆	1 A1 ₅ A2 ₅ . . . A14 ₅ A15 ₅	1 A1 ₄ A2 ₄ . . . A14 ₄ A15 ₄	1 A1 ₃ A2 ₃ . . . A14 ₃ A15 ₃	0 A1 ₂ A2 ₂ . . . A14 ₂ A15 ₂	0 A1 ₁ A2 ₁ . . . A14 ₁ A15 ₁	0 A1 ₀ A2 ₀ . . . A14 ₀ A15 ₀	Set Gray Scale Table	<p>The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)</p> <p>A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15</p> <p>Note (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3 < Setting of GS14 < Setting of GS15</p> <p>Refer to Section 8.8 for details</p> <p>(2) The setting must be followed by the Enable Gray Scale Table command (00h)</p>																										

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description																		
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112 Refer to Section 8.8 for details																		
0 1	BB A[4:0]	1 *	0 *	1 *	1 A ₄	1 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h] <table border="1"> <thead> <tr> <th>A[5:1]</th> <th>Hex code</th> <th>pre-charge voltage</th> </tr> </thead> <tbody> <tr> <td>00000</td> <td>00h</td> <td>0.20 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>11111</td> <td>3Eh</td> <td>0.60 x V_{CC}</td> </tr> </tbody> </table>	A[5:1]	Hex code	pre-charge voltage	00000	00h	0.20 x V _{CC}	:	:	:	11111	3Eh	0.60 x V _{CC}						
A[5:1]	Hex code	pre-charge voltage																											
00000	00h	0.20 x V _{CC}																											
:	:	:																											
11111	3Eh	0.60 x V _{CC}																											
0 1	BE A[3:0]	1 *	0 *	1 *	1 A ₃	1 A ₂	1 A ₁	1 A ₀	0	Set V _{COMH}	Set COM deselect voltage level [reset = 04h] A[3:0] = <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Hex code</th> <th>V_{COMH}</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h</td> <td>0.72 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>0100</td> <td>04h</td> <td>0.80 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>0111</td> <td>07h</td> <td>0.86 x V_{CC}</td> </tr> </tbody> </table>	A[2:0]	Hex code	V _{COMH}	0000	00h	0.72 x V _{CC}	:	:	:	0100	04h	0.80 x V _{CC}	:	:	:	0111	07h	0.86 x V _{CC}
A[2:0]	Hex code	V _{COMH}																											
0000	00h	0.72 x V _{CC}																											
:	:	:																											
0100	04h	0.80 x V _{CC}																											
:	:	:																											
0111	07h	0.86 x V _{CC}																											
0 1	C1 A[7:0]	1 A ₇	1 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I _{SEG} current [reset = 7Fh]																		
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A ₃	1 A ₂	1 A ₁	1 A ₀	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]																		
0 1	CA A[6:0]	1 *	1 A ₆	0 A ₅	0 A ₄	1 A ₃	0 A ₂	1 A ₁	0 A ₀	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]																		
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A ₂	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command																		

Note

(1) "*" stands for "Don't care".

8. Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	90°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-30°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

8.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at $23 \pm 5^\circ\text{C}$; $55 \pm 15\%$ RH.

9. Outgoing Quality Control Specifications

9.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	$23 \pm 5^\circ\text{C}$
Humidity:	$55 \pm 15\%$ RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	$\geq 50\text{cm}$
Distance between the Panel & Eyes of the Inspector:	$\geq 30\text{cm}$
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

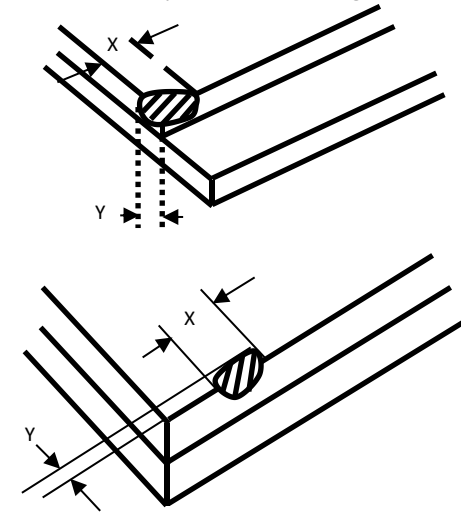
9.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

9.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

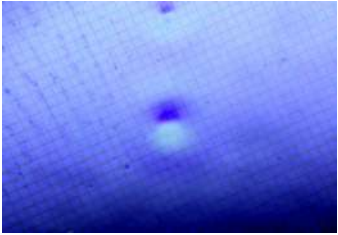
9.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	<p>X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)</p> 

9.3.2 Cosmetic Check (Display Off) in Active Area

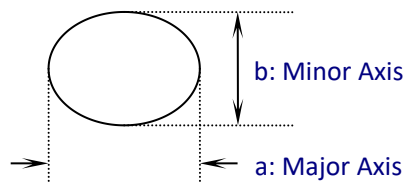
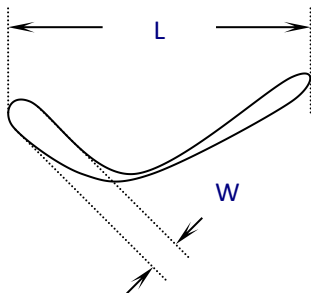
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer

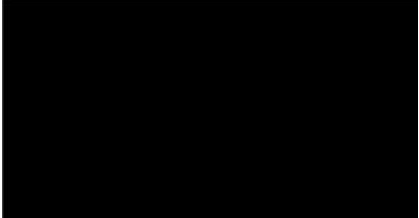
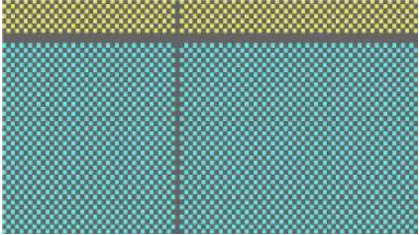
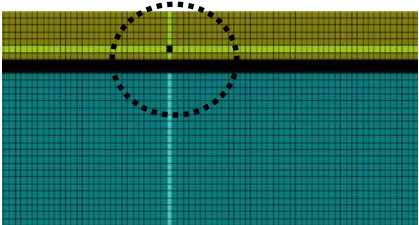
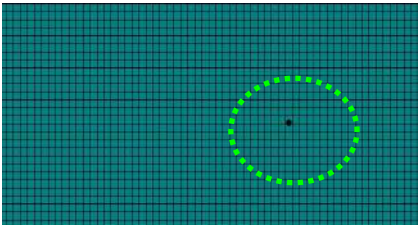
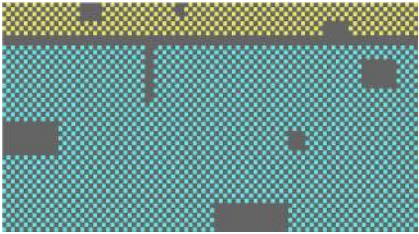
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ $W > 0.1$ $L \leq 2$ $L > 2$	Ignore $n \leq 1$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ $0.1 < \Phi \leq 0.25$ $0.25 < \Phi$	Ignore $n \leq 1$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$	$n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable	

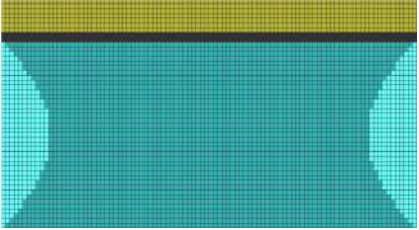
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



9.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	

Un-uniform	Major	
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Precautions

1. Handling Precautions

The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

The polarizer covering the display surface of the oled module is soft and easily scratched. Handle this polarizer carefully.

If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

Do not attempt to disassemble the oled Module.

If the logic circuit power is off, do not apply the input signals.

To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

Be sure to ground the body when handling the oled Modules.

Tools required for assembly, such as soldering irons, must be properly ground.

To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

The oled Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

Storage precautions

When storing the oled modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

The oled modules should be stored under the storage temperature range. If the oled modules will be stored for a long time, the recommend condition is:

The oled modules should be stored in the room without acid, alkali and harmful gas.

2 Transportation Precautions

The oled modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.