Specification for E-Paper

AEZ38401080A00-28.0ENRS

Revision 1.1

A	Orient Display
EZ	E-Paper
38401080	Resolution 3840 x 1080
A00	Revision A00
28.0	Diagonal: 28.0', Module: 698.6(H)*209.3(V)*0.953(D)mm
E	EPD - Electrophoretic Display (Active Matrix)
N	Top: -15°C ~ +65°C; Tstr: -25°C ~ +70°C
R	Reflective Polarizer
S	3-/4-wire SPI Interface
/	Controller Source COF: Himax HX-5271 Gate COF: Solomon SPD1652
/	ZIF FPC
/	Ultra Wide Viewing Angle
/	Ultra Low Power Consumption

REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	FEB.14.2022	New Creation	ALL	
1.1	MAY.29.2024	Add MTTF & MCTF	P23-24	

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1. General Description

AEZ38401080A00-28.0ENRS is a reflective electrophoretic technology display module based on active matrix TFT substrate. It has 28" active area with 3840 x 1080 pixels and 32:9 aspect ratio. The display is capable to display images at 16 Gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

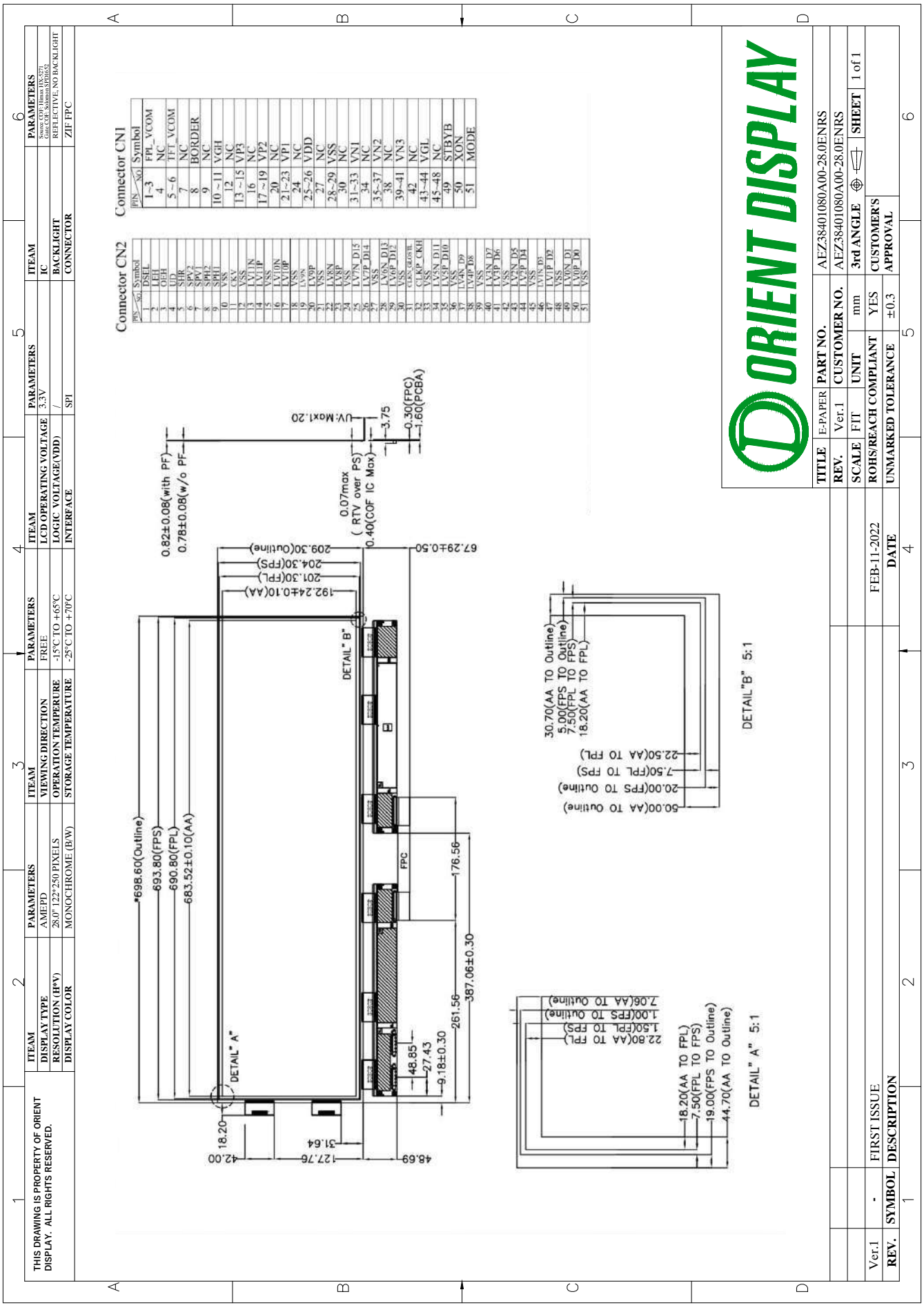
2. Features

- High contrast electrophoretic imaging film
- 3840 x 1080 display
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Landscape mode

3. Mechanical Specifications

Parameter	**Specifications**	**Unit**	**Remark**
Screen Size	28"	Inch	
Display Resolution	3840 (H)×1080(V)	Pixel	32:9
Active Area	683.52(H)×190.24(V)	mm	
Pixel Pitch	0.178	mm	
Pixel Configuration	Square		
Outline Dimension	698.6(H)*209.3(V)*0.953(D)	mm	
Module Weight	TBD	g	
Number of Gray	16 Gray Level		
Display operating mode	Reflective mode		
Glass Substrate	0.5mm	mm	
Surface Treatment	Anti-glare		
Driver IC	Source COF: Himax HX-5271 Gate COF: Solomon SPD1652		

4. Mechanical Drawing of EPD module



5. Input / Output Terminals

5-1) Connector type:

Item	Pin numbers	Pitch (mm)	Connector	Note
CN1	51	0.5	P-TWO 187059-51221-1	LVDS Type
CN2	51	0.5	P-TWO 187059-51221-1	LVDS Type

5-2) Pin Assignment

Connector CN1

Pin #	Signal	Description	Remark
1	FPL_VCOM	Common Voltage.	
2	FPL_VCOM	Common Voltage.	
3	FPL_VCOM	Common Voltage.	
4	NC	NO Connection	
5	TFT_VCOM	Common Voltage.	
6	TFT_VCOM	Common Voltage.	
7	NC	NO Connection	
8	BORDER	Border connection	
9	NC	NO Connection	
10	VGH	Positive power supply gate driver.	
11	VGH	Positive power supply gate driver.	
12	NC	NO Connection	
13	VP3	Positive power supply source driver.	
14	VP3	Positive power supply source driver.	
15	VP3	Positive power supply source driver.	
16	NC	NO Connection	
17	VP2	Positive power supply source driver.	
18	VP2	Positive power supply source driver.	
19	VP2	Positive power supply source driver.	
20	NC	NO Connection	
21	VP1	Positive power supply source driver.	
22	VP1	Positive power supply source driver.	
23	VP1	Positive power supply source driver.	
24	NC	NO Connection	
25	VDD	Logic power.	
26	VDD	Logic power.	
27	NC	NO Connection	
28	VSS	Ground	
29	VSS	Ground	
30	NC	NO Connection	
31	VN1	Negative power supply source driver.	
32	VN1	Negative power supply source driver.	
33	VN1	Negative power supply source driver.	
34	NC	NO Connection	
35	VN2	Negative power supply source driver.	
36	VN2	Negative power supply source driver.	
37	VN2	Negative power supply source driver.	
38	NC	NO Connection	
39	VN3	Negative power supply source driver.	
40	VN3	Negative power supply source driver.	
41	VN3	Negative power supply source driver.	
42	NC	NO Connection	
43	VGL	Negative power supply gate driver.	
44	VGL	Negative power supply gate driver.	
45	NC	NO Connection	
46	NC	NO Connection	

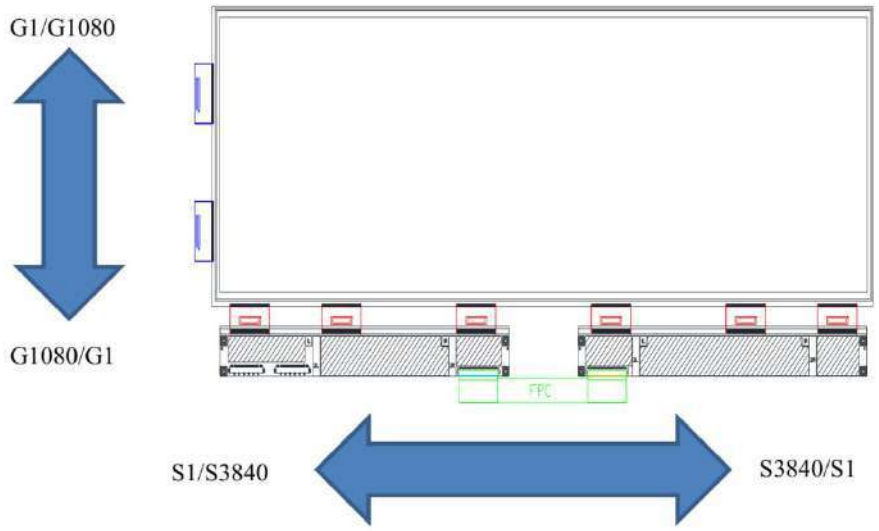
47	NC	NO Connection	
48	NC	NO Connection	
49	STBYB	mini-LVDS enable.	
50	XON	XON signal gate driver	
51	MODE	Output enable gate driver	

Connector CN2

<table>
<tr><th>Pin #</th><th>Signal</th><th>Description</th><th>Remark</th></tr>
<tr><td>1</td><td>DSEL</td><td>Data Input select</td><td></td></tr>
<tr><td>2</td><td>LEH</td><td>Latch enable source driver</td><td></td></tr>
<tr><td>3</td><td>OEH</td><td>Outputs enabled when OE is logic “H”,
Outputs forced to GND when OE is logic “L”.</td><td></td></tr>
<tr><td>4</td><td>UD</td><td>Shift direction control pin gate driver
UD = H: Data shift direction from G1 to G800.
UD = L: Data shift direction from G800 to G1.</td><td></td></tr>
<tr><td>5</td><td>SHR</td><td>Shift direction control pin source driver
SHR =H: Data inputs read sequentially from S800 to S1.
SHR =L: Data inputs read sequentially from S1 to S800.</td><td></td></tr>
<tr><td>6</td><td>SPV2</td><td>Start pulse gate driver<table><tr><td>UD</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPV1</td><td>SPV2</td></tr><tr><td>L</td><td>SPV2</td><td>SPV1</td></tr></table></td><td></td></tr>
<tr><td>7</td><td>SPV1</td><td>Start pulse gate driver<table><tr><td>UD</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPV1</td><td>SPV2</td></tr><tr><td>L</td><td>SPV2</td><td>SPV1</td></tr></table></td><td></td></tr>
<tr><td>8</td><td>SPH2</td><td>Start pulse source driver<table><tr><td>SHR</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPH2</td><td>SPH1</td></tr><tr><td>L</td><td>SPH1</td><td>SPH2</td></tr></table></td><td></td></tr>
<tr><td>9</td><td>SPH1</td><td>Start pulse source driver<table><tr><td>SHR</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPH2</td><td>SPH1</td></tr><tr><td>L</td><td>SPH1</td><td>SPH2</td></tr></table></td><td></td></tr>
<tr><td>10</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>11</td><td>CKV</td><td>Clock gate driver</td><td></td></tr>
<tr><td>12</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>13</td><td>LV11N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>14</td><td>LV11P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>15</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>16</td><td>LV10N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>17</td><td>LV10P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>18</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>19</td><td>LV9N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>20</td><td>LV9P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>21</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>22</td><td>LV8N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>23</td><td>LV8P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>24</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>25</td><td>LV7N_D15</td><td>Data signal source driver</td><td></td></tr>
<tr><td>26</td><td>LV7P_D14</td><td>Data signal source driver</td><td></td></tr>
<tr><td>27</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>28</td><td>LV6N_D13</td><td>Data signal source driver</td><td></td></tr>
<tr><td>29</td><td>LV6P_D12</td><td>Data signal source driver</td><td></td></tr>
<tr><td>30</td><td>VSS</td><td>Ground</td><td></td></tr>
</table>

31	CLKN_GLOSTL	Data signal source driver	
32	CLKP_CKH	Data signal source driver	
33	VSS	Ground	
34	LV5N_D11	Data signal source driver	
35	LV5P_D10	Data signal source driver	
36	VSS	Ground	
37	LV4N_D9	Data signal source driver	
38	LV4P_D8	Data signal source driver	
39	VSS	Ground	
40	LV3N_D7	Data signal source driver	
41	LV3P_D6	Data signal source driver	
42	VSS	Ground	
43	LV2N_D5	Data signal source driver	
44	LV2P_D4	Data signal source driver	
45	VSS	Ground	
46	LV1N_D3	Data signal source driver	
47	LV1P_D2	Data signal source driver	
48	VSS	Ground	
49	LV0N_D1	Data signal source driver	
50	LV0P_D0	Data signal source driver	
51	VSS	Ground	

5-3) Panel Scan direction



6. Electrical Characteristics

6-1) Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5.0	V	
Positive Supply Voltage	VP3	-0.3 to VN3+50	V	
	VP2	-0.3 to VP3	V	
	VP1	-0.3 to VP3	V	
Negative Supply Voltage	VN1	VN3 to + 0.3	V	
	VN2	VN3 to + 0.3	V	
	VN3	-25 to + 0.3	V	
Supply Voltage	VGH	-0.3 to +55	V	
Supply Voltage	VGL	-32 to +0.3	V	
Supply Range	VGH-VGL	-0.3 to +55	V	
Operating Temp. Range	TOTR	-15 to +65	℃	
Storage Temperature	TSTG	-25 to +70	℃	

6-2) Panel DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS			0		V
Logic voltage supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V			TBD	mA
Gate Negative supply	VGL		-19	-20	-21	V
	IGL	VGL=-20V			TBD	mA
Gate Positive supply	VGH		26	27	28	V
	IGH	VGH=27V			TBD	mA
Source Negative supply	VN1		-16	-15	-14	V
	IN1				TBD	mA
Source Negative supply	VN2		-13	-12	-11	V
	IN2				TBD	mA
Source Negative supply	VN3		-21	-20	-19	V
	IN3				TBD	mA
Source Positive supply	VP1		14	15	16	V
	IP1				TBD	mA
Source Positive supply	VP2		11	12	13	V
	IP2				TBD	mA
Source Positive supply	VP3		19	20	21	V
	IP3				TBD	mA
Border supply	-		-	-	-	V
Asymmetry source	Vasm	VP1+VN1	TBD		TBD	mV
Common voltage	Vcom_TFT		-3.5	Adjusted	-0.3	V
	Icom_TFT			TBD	TBD	mA

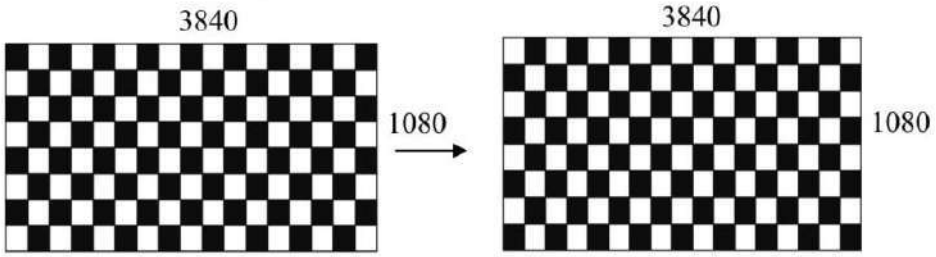
	Vcom_FPL		-3.5	Adjusted	-0.3	V
	Icom_FPL			TBD	TBD	mA
Maximum Power panel	Pmax				TBD	mW
Typical power panel	Ptyp			TBD		mW
Standby power panel	Pstby				TBD	mW
Maximum Currents (Note 5)	IP1	VP1 = 15V	-		TBD	mA
	IN1	VN1 = -15V	-		TBD	mA
	IGH	VGH = 27V	-		TBD	mA
	IGL	VGL =-20V	-		TBD	mA
	ICOM		-		TBD	mA

Note:

1. The maximum average Currents for power consumption are measured using 75 Hz waveform with following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
2. The Typical average current for power consumption is measured using 75 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern.(Note 6-2)
3. The standby power is the consumed power when the panel controller is in standby mode.
4. The Maximum Currents are measured using 75 Hz waveform with following pattern transition:from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
- It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
- The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
5. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by ODNA.
6. Vcom is recommended to be set in the range of assigned value ± 0.1 V
7. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024)
8. The maximum current is for reference only.

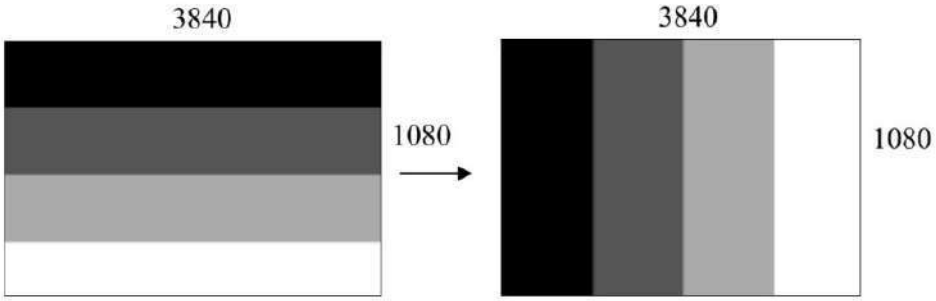
Note6-1

The maximum average current and Maximum Currents



Note6-2

The typical power consumption



Note6-3

The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
IDD	2.2uF x 14pcs / ±10%
IP1	2.2uF x 12pcs / ±10%
IP2	2.2uF x 12pcs / ±10%
IP3	2.2uF x 12pcs / ±10%
IN1	2.2uF x 12pcs / ±10%
IN2	2.2uF x 12pcs / ±10%
IN3	2.2uF x 12pcs / ±10%
IGH	2.2uF x 2pcs / ±10%
IGL	2.2uF x 3pcs / ±10%
ICOM	No Capacitor

6-3) Refresh Rate

The module is applied at a maximum screen refresh rate of 75Hz.

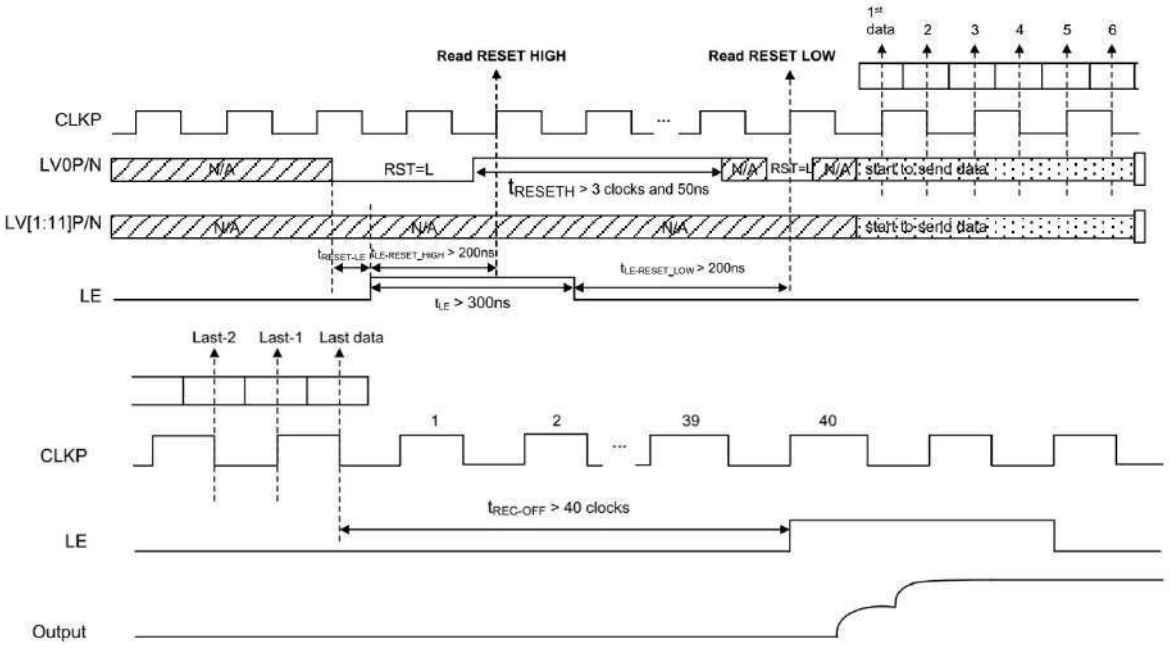
	Min	Max
Refresh Rate	-	75 Hz

6-4) Panel AC characteristics

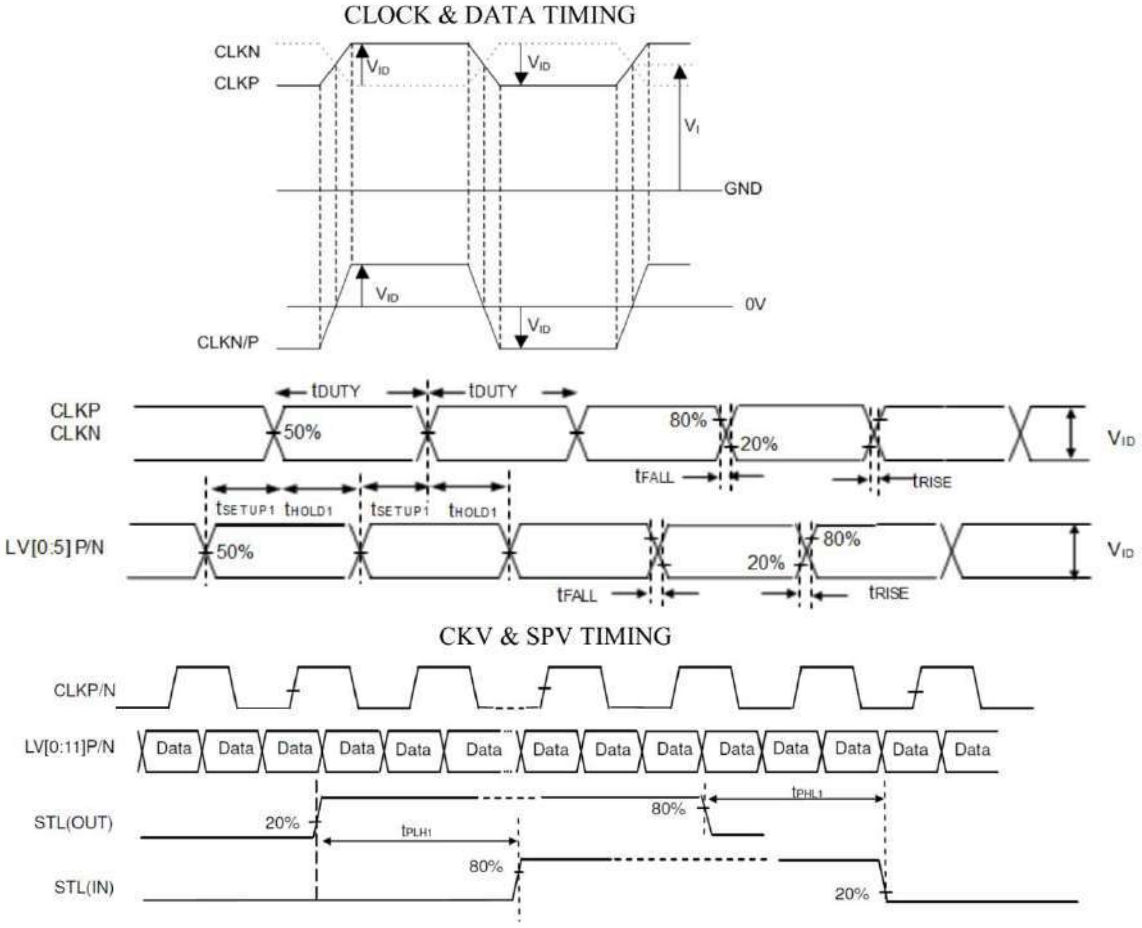
VDD=2.7V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
mini-LVDS differential voltage	V_{ID}	300	-	-	mV
mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V
Source Clock frequency	F_{CLK}	-	-	150	MHz
Source Clock duty	t_{DUTY}	45	-	55	%
Source Clock setup time	t_{SETUP1}	1.1	-	-	ns
Source Clock hold time	t_{HOLD1}	1.1	-	-	ns
Rise time	t_{RISE}	-	-	0.15	Unit interval
Fall time	t_{FALL}	-	-	0.15	Unit interval
LE rising to reset input time	$t_{LE\text{-}RESET\_HIGH}$	200	-	-	ns
LE falling to reset input time	$t_{LE\text{-}RESET\_LOW}$	200	-	-	ns
Start pulse delay time	t_{PLH1}	-	-	4	CLK
	t_{PHL1}	-	-	4	CLK
Reset high period	t_{RESETH}	3	-	-	CLK
Receiver off to LE timing	$t_{REC\text{-}OFF}$	40	-	-	CLK
LE width	t_{LE}	300	-	-	ns
Reset low to LE rising time	$t_{RESET\text{-}LE}$	0	-	-	ns
Gate clock frequency	f_{CLK}	-	-	200	kHz
Gate clock pulse high period	t_{CLKH}	500	-	-	ns
Gate clock pulse low period	t_{CLKL}	500	-	-	ns
Gate clock rise time	t_{IR_CLK}	-	-	100	ns
Gate clock fall time	t_{IF_CLK}	-	-	100	ns
Gate Start pulse setup time	t_{SU}	100	-	t_{CLKH}-100	ns
Gate Start pulse hold time	t_{HD}	100	-	t_{CLKL}-100	ns
Gate Start pulse rise time	t_{IR_STV}	-	-	100	ns
Gate Start pulse fall time	t_{IF_STV}	-	-	100	ns
Gate STV output delay from CLK	t_{OD_STV}	-	-	500	ns
Output delay time from CLK	t_{D_OUT}	-	-	2	us
Output rise time, output pins	t_{R_OUT}	-	-	1	us
Output fall time, output pins	t_{F_OUT}	-	-	1	us
XONL/R pulse width	t_{WXON}	10	-	-	us
Output delay time from XON	t_{DXON_OUT}	-	-	20	us

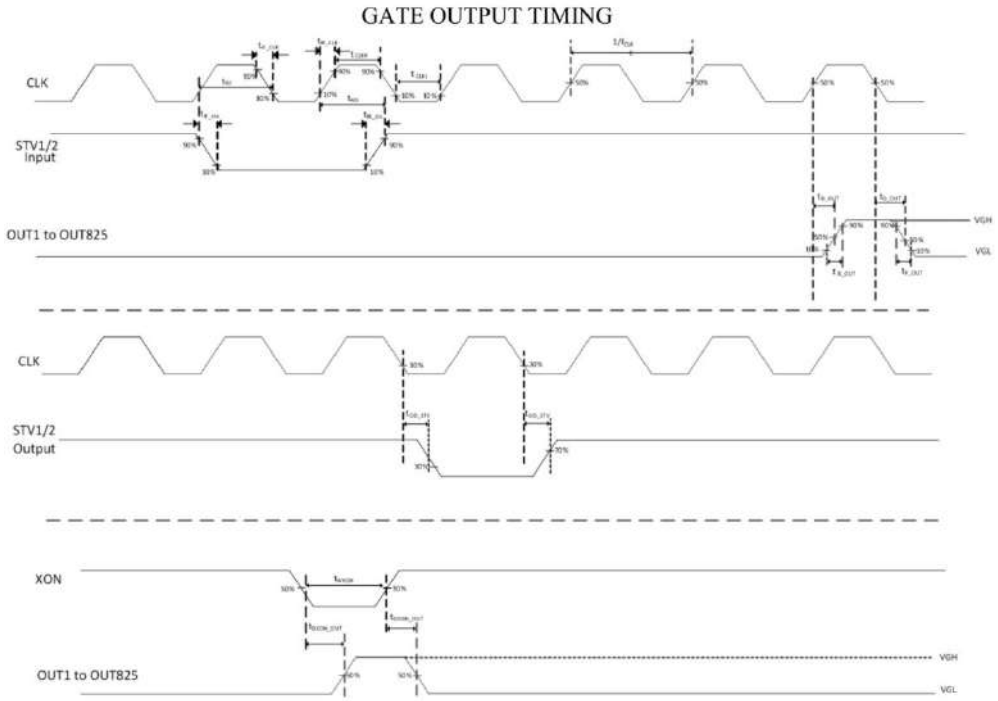
OUTPUT LATCH CONTROL SIGNALS



CLOCK & DATA TIMING



CKV & SPV TIMING



Note： First gate line on timing

After 5CLK, Gate OUT1 is on.

6-5) Controllers Timing

The timing mode is depicted on Figure 6.1 and Figure 6.2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

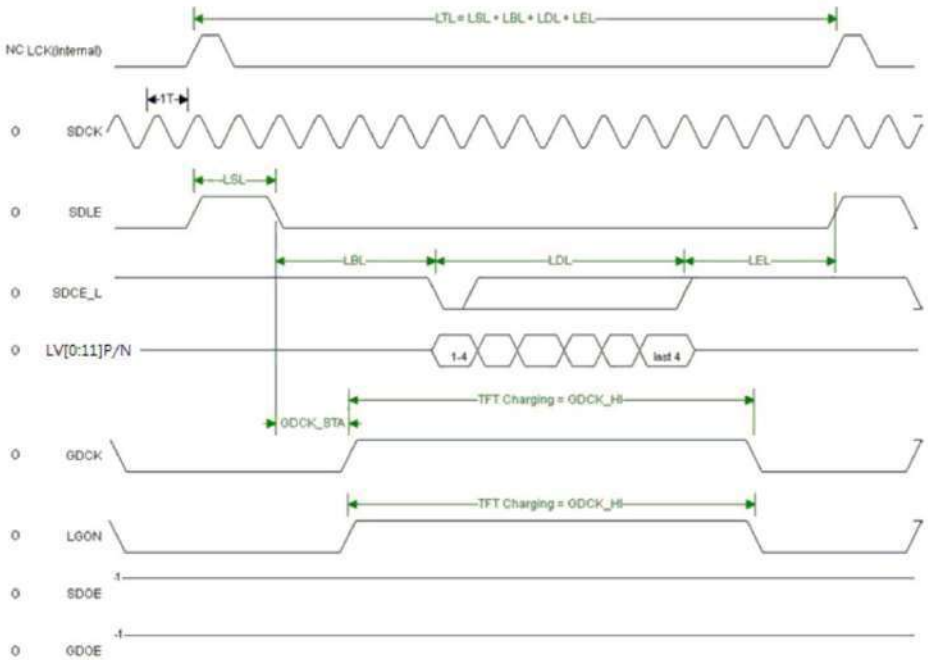


Figure 6.1 Line Timing in Mode 3

Note: LCK is an internal signal and it is shown for reference only.

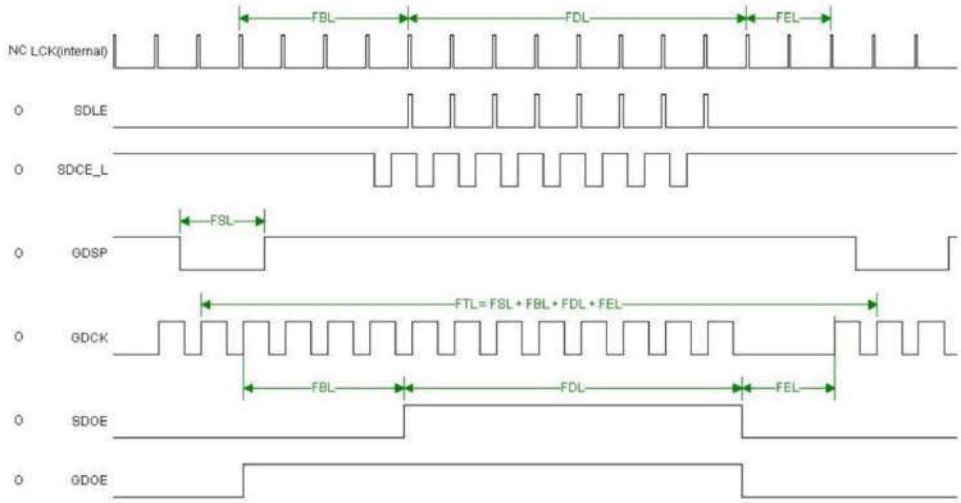


Figure 6.2 Frame Timing in Mode 3

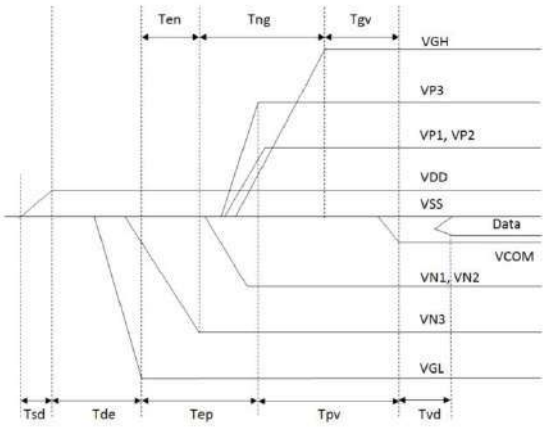
Note 1: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL
Note 2:SDCLK = XCL
LV[0:11]P/N = LV0P~LV11N
SDCE_L = XSTL
GDCK = CKV
GDSP = SPV
GDOE = Mode1
SDOE = XOE

7. Power on Sequence

Power Rails must be sequenced in the following order：

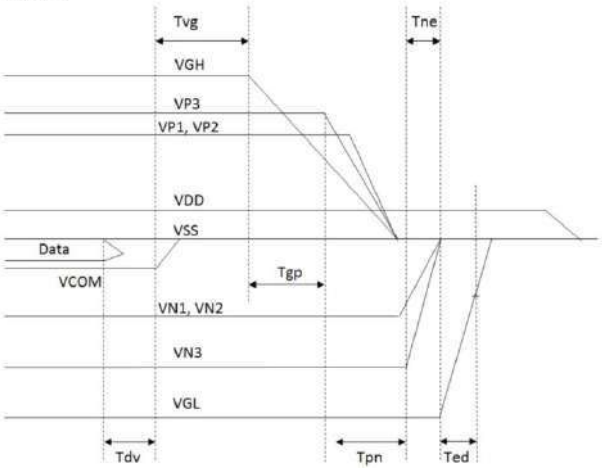
1. VSS →VDD →VN3 →VN1(VN2) →VP1(VP2) →VP3 →VCOM
2. VSS →VDD →VGL →VGH (Gate driver)

POWER ON



	Min	Max	Remark
Tsd	30us	-	
Tde	100us	-	
Tep	1000us	-	
Tpv	100us	-	
Tvd	100us	-	
Ten	0us	-	
Tng	1000us	-	
Tgv	100us	-	

POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

8. Optical Characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	40	-	%	Note 8-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	12	-		

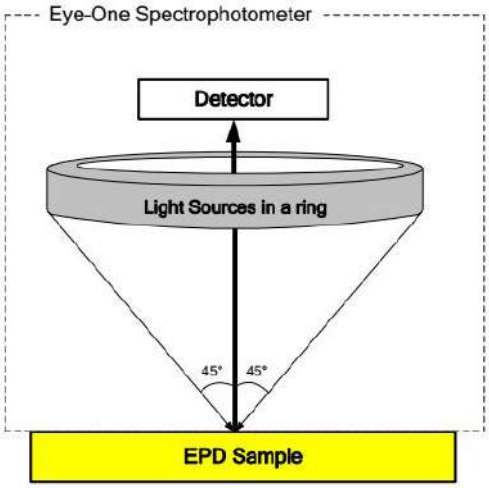
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS

m:4、8、16 when 2、3、4 bits mode

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl/Rd.



8-3) Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factorwhite board x (Lcenter / Lwhite board)

Lcenter is the luminance measured at center in a white area (R=G=B=1). Lwhite board is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirement

WARNING
The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause's circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.
Data sheet status
Product specification
This data sheet contains Preliminary product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition These are stress ratings only and operation of the device at these or at any other condition to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification

10. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +65°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = -15°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
7	Solar radiation test	765 W/m2,168hrs,40℃	IEC60 068-2-5Sa	
8	Package Vibration	Random Wave (1.5Grms) Frequency: 10~200Hz Direction: X,Y,Z Duration: 30mins each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 15.2 cm on concrete surface. Drop sequence: 6 flats	Full packed for shipment	
10	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	
11	Electrostatic Effect (non-operating)	(ESD gun) Air 15k, Contact 8k	IEC 62179, IEC 62180	

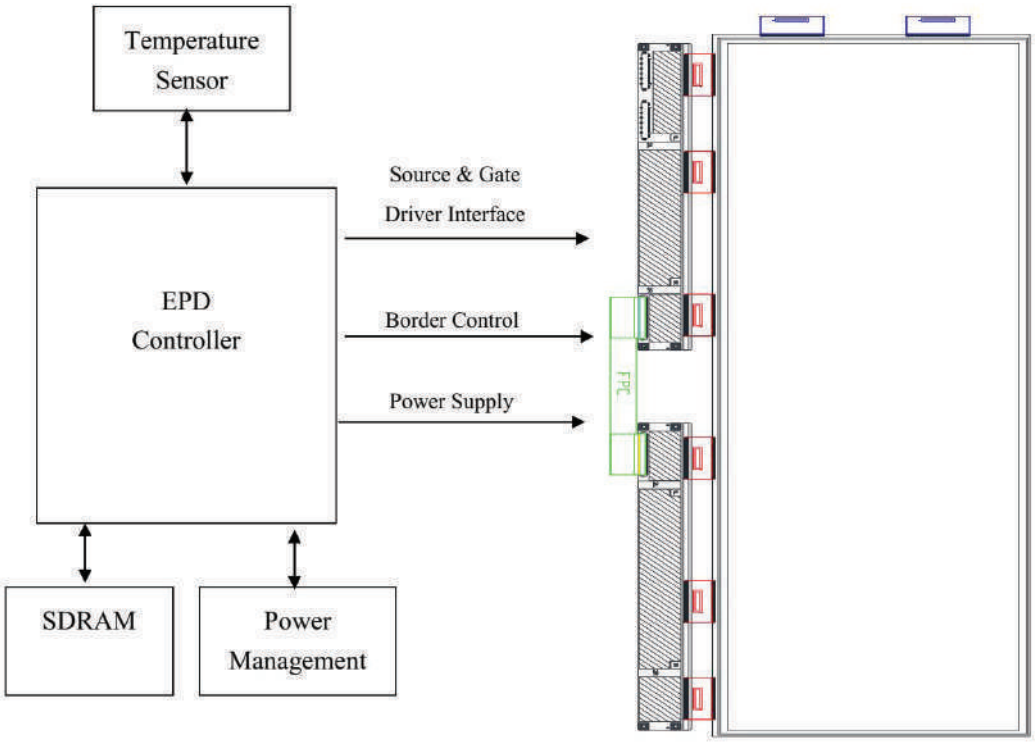
Actual EMC level to be measured on customer application

Note: The protective film must be removed before temperature test.

< Criteria >

In the standard conditions, there is not display function NG issue occurred. (Including: line defect, no image). All the cosmetic specification is judged before the reliability stress.

11. Block Diagram



12. Bar Code definition

TBA

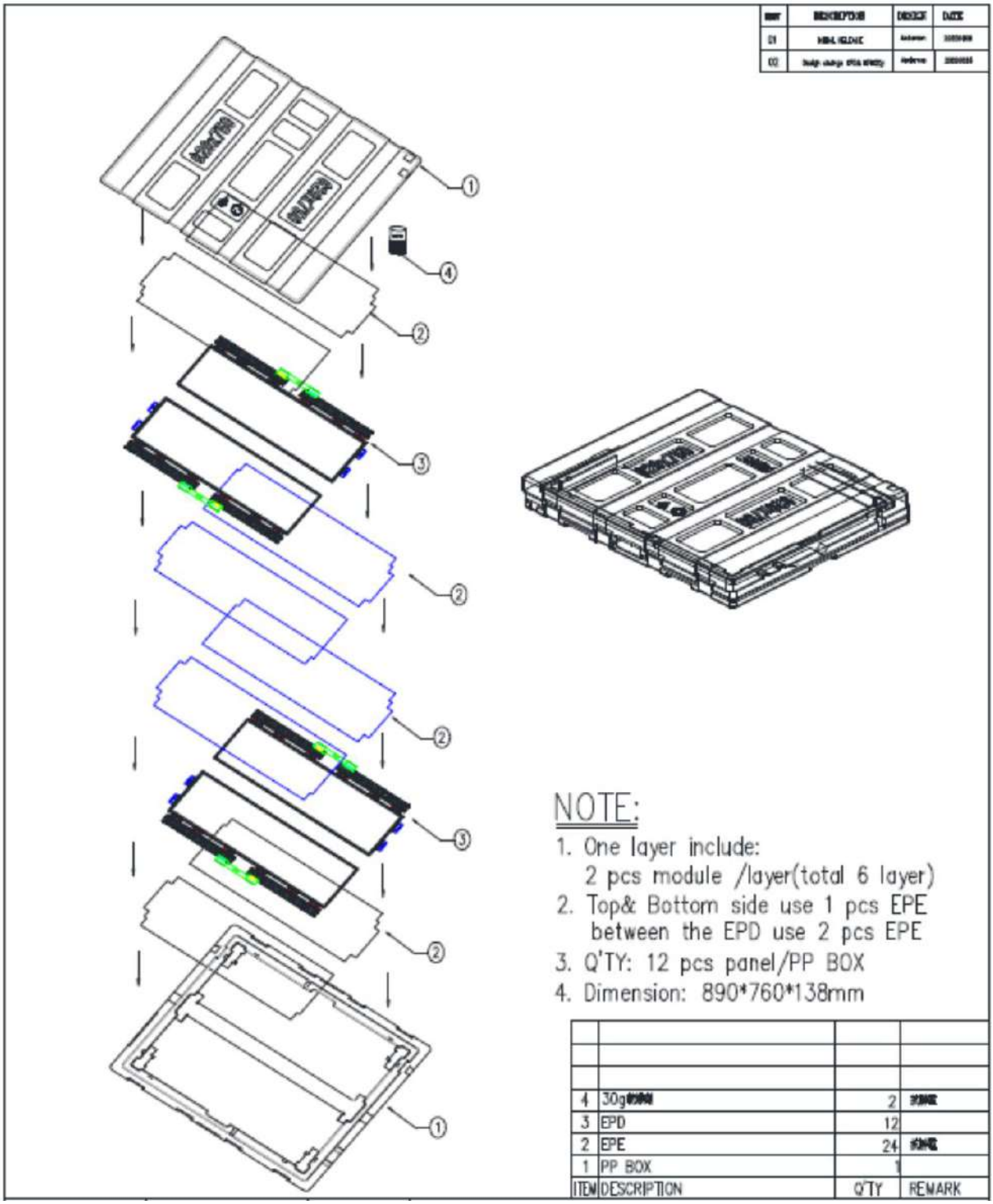
13. Appendix

For outdoor product please refer to details by followed documentations:

1. Outdoor Signage Design Recommendation
2. Signage Wide Temp. Support Requirement.

14.Packing

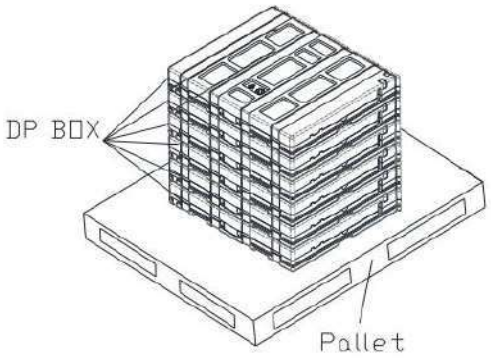
14-1) packing drawing

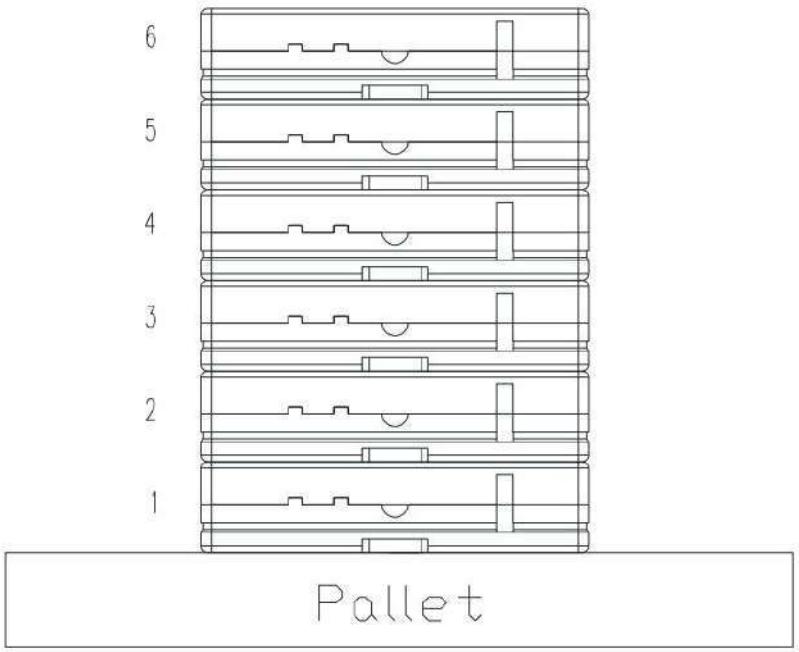


14-2) Pallet Stacking

Note: Stacking layer limitation: 6 layers.

REV.	DESCRIPTION	DESIGN	DATE
1	INITIAL RELEASE	Anderson	20200602



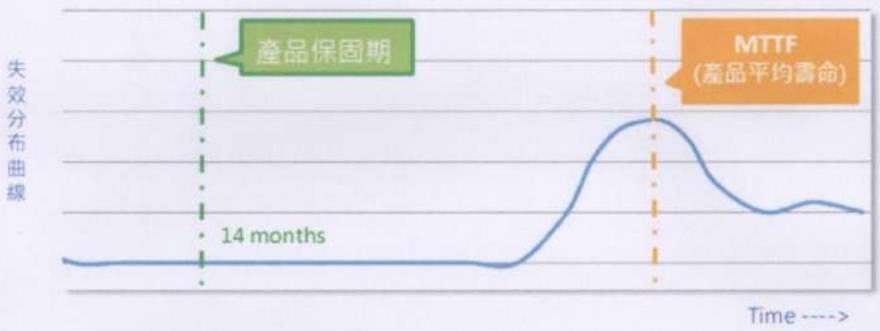


NOTE:
1.Pallet Dimension:1150*950*114 mm
2.6Boxes/Pallet
3.PP Box Dimension : 890*760*138mm

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
2		PP BOX	6	
1		Pallet	1	

15.MTTF & MCTF

產品保固期 & 產品平均壽命



- 規格書一般會提供產品保固期。
- 產品平均壽命(MTTF)通常因為產品使用的環境以及消費者的使用習慣產生變化。

MTTF and MCTF

- Mean Time To Failure~產品平均壽命(時間)
  產品平均失效發生時間，即機率理論所定義之產品失效發生時間的期望值

- Mean Cycle To Failure ~產品平均壽命(次數)
  產品平均失效發生作業次數，即機率理論所定義之產品失效發生作業次數的期望值

MTTF for storage test (一般適用於標籤類產品)

- The predicting MTTF is shown on below. Here the **MTTF > 5 years** are marked by **green**.

MTTF (years)		Humidity (%)						
		50	55	60	65	70	75	80
Temp. (C)	0	328.6	121.2	67.7	39.0	23.7	15.4	11.0
	5	201.7	74.4	41.6	24.0	14.5	9.5	6.8
	10	126.0	46.4	26.0	15.0	9.1	5.9	4.2
	15	80.0	29.5	16.5	9.5	5.8	3.8	2.7
	20	51.6	19.0	10.6	6.1	3.7	2.4	1.7
	25	33.7	12.4	6.9	4.0	2.4	1.6	1.1
	30	22.4	8.3	4.6	2.7	1.6	1.1	0.7
	35	15.1	5.5	3.1	1.8	1.1	0.7	0.5
	40	10.3	3.8	2.1	1.2	0.7	0.5	0.3
	45	7.1	2.6	1.5	0.8	0.5	0.3	0.2
	50	5.0	1.8	1.0	0.6	0.4	0.2	0.2

MCTF for operation test (一般適用於CE產品)

- **Test Condition:**
  1. Accelerated Stress Condition：50℃80% , operation with 5sec update.
  2. Input RA Q'ty：11 PCS

$$MTTF = \left(\frac{2T}{\chi^2_{\alpha,2r+2}} \right) \qquad T = AFx[\delta+(n-\gamma)xt]$$

Peck' s Combination model

$$AF_\eta = \frac{\eta_n}{\eta_a} = [\frac{H_a}{H_n}]^m \times e^{\frac{E_a(\frac{1}{T_n}-\frac{1}{T_a})}{k}}$$

- **Based on the formula calculation:**

(Ea = 0.39, Confidence Level: 90%)

-The MTTF of 25℃50% , operation with 5sec update would be 13301 hrs

-The MCTF of 25℃50% , operation would be 9,576,720 times.