Specification for E-Paper

AEZ25601440A00-31.2ENRS

Revision 1.3

A	Orient Display
EZ	E-Paper
25601440	Resolution 2560 x 1440
A00	Revision A00
31.2	Diagonal: 31.2’’, Module: 697.2(H)×402.8(V)×0.805(D)mm
E	EPD - Electrophoretic Display (Active Matrix)
N	Top: -15°C ~ +65°C; Tstr: -25°C ~ +70°C
R	Reflective Polarizer
S	3-/4-wire SPI Interface
/	Controller
/	ZIF FPC
/	Ultra Wide Viewing Angle
/	Ultra Low Power Consumption

REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	NOV.25.2019	New Creation	ALL	
1.1	APR.12.2022	Update Mechanical Drawing of EPD module	P5	
1.2	JUL.25.2022	Update Packing	P23	
1.3	SEP.09.2022	Update Features Update Mechanical Drawing of EPD module Update the pin assignment Update Electrical Characteristics Update Optical characteristics	P4 P5 P6-9 P10 P19	

LIST

1. General Description----------(4)

2. Features----------(4)

3. Mechanical Specifications----------(4)

4. Mechanical Drawing of EPD module----------(5)

5. Input /Output Terminals----------(6-10)

6. Electrical Characteristics----------(10-16)

7. Power on Sequence----------(17-18)

8. Optical Characteristics----------(19)

9. Handling, Safety and Environment Requirements and Remark----------(20-21)

10. Reliability test----------(21)

11. Block Diagram ----------(22)

12. Bar Code Definition----------(22)

13. Packing----------(23)

1. General Description

AEZ25601440A00-31.2ENRS is a reflective electrophoretic technology display module based on active matrix TFT substrate. It has 31.2” active area with 2560 x 1440 pixels and 16:9 aspect ratios. The display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

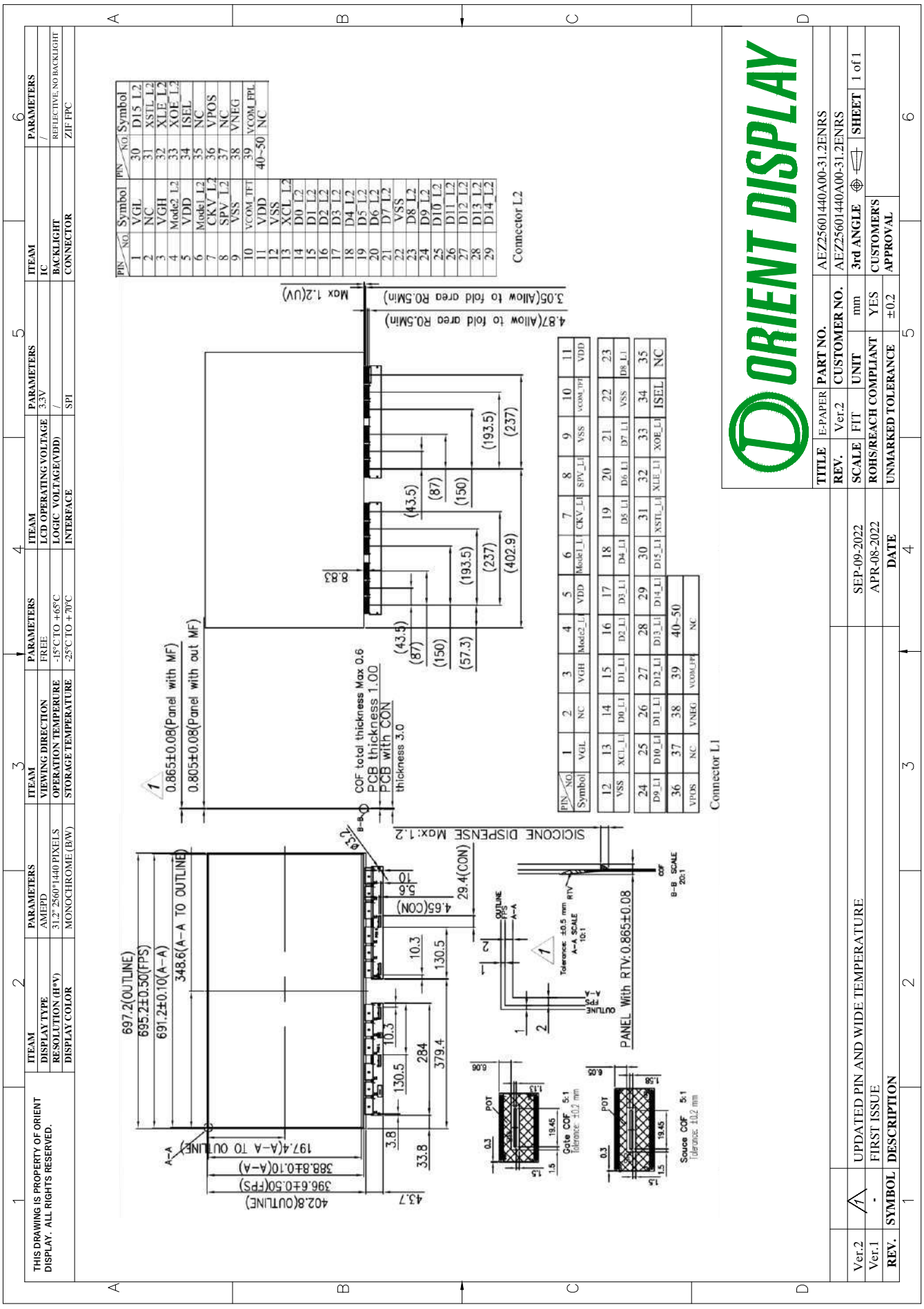
2. Features

- High contrast electrophoretic imaging film
- 2560 x 1440 display
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Wide temperature operating range from -15℃ to 0℃ and from 50℃ to 65℃ with 1-bit WF; otherwise, from 0℃ to 50℃ with 4-bit WF

3. Mechanical Specifications

Parameter	**Specifications**	**Unit**	**Remark**
Screen Size	31.2	Inch	
Display Resolution	2560 (H) × 1440 (V)	Pixel	16:9
Active Area	691.2 (H) × 388.8 (V)	mm	94dpi
Outline Dimension	697.2(H) × 402.8(V) × 0.805(D)	mm	
Pixel Pitch	0.27	mm	
Pixel Configuration	Square		
Module Weight	494	g	
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		
Glass Substrate	0.5	mm	
Surface Treatment	Hard Coating		

4. Mechanical Drawing of EPD module



5. Input / Output Terminals

5.1 Connector type：Hirose FH52-50S-0.5SH compatible

5.2 Pin Assignment

Connector L2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_L2	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_L2	Output enable gate driver
7	CKV_L2	Clock gate driver
8	SPV_L2	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_L2	Clock source driver
14	D0_L2	Data signal source driver
15	D1_L2	Data signal source driver
16	D2_L2	Data signal source driver
17	D3_L2	Data signal source driver
18	D4_L2	Data signal source driver
19	D5_L2	Data signal source driver
20	D6_L2	Data signal source driver
21	D7_L2	Data signal source driver
22	VSS	Ground
23	D8_L2	Data signal source driver
24	D9_L2	Data signal source driver
25	D10_L2	Data signal source driver
26	D11_L2	Data signal source driver
27	D12_L2	Data signal source driver
28	D13_L2	Data signal source driver
29	D14_L2	Data signal source driver
30	D15_L2	Data signal source driver
31	XSTL_L2	Start pulse source driver
32	XLE_L2	Latch enable source driver
33	XOE_L2	Outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”.
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic “L” levels or let them open. H: input data bus width is 16-bit.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

Connector L1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_L1	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_L1	Output enable gate driver
7	CKV_L1	Clock gate driver
8	SPV_L1	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_L1	Clock source driver
14	D0_L1	Data signal source driver
15	D1_L1	Data signal source driver
16	D2_L1	Data signal source driver
17	D3_L1	Data signal source driver
18	D4_L1	Data signal source driver
19	D5_L1	Data signal source driver
20	D6_L1	Data signal source driver
21	D7_L1	Data signal source driver
22	VSS	Ground
23	D8_L1	Data signal source driver
24	D9_L1	Data signal source driver
25	D10_L1	Data signal source driver
26	D11_L1	Data signal source driver
27	D12_L1	Data signal source driver
28	D13_L1	Data signal source driver
29	D14_L1	Data signal source driver
30	D15_L1	Data signal source driver
31	XSTL_L1	Start pulse source driver
32	XLE_L1	Latch enable source driver
33	XOE_L1	Outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”.
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic “L” levels or let them open. H: input data bus width is 16-bit.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

Connector R1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_R1	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_R1	Output enable gate driver
7	CKV_R1	Clock gate driver
8	SPV_R1	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_R1	Clock source driver
14	D0_R1	Data signal source driver
15	D1_R1	Data signal source driver
16	D2_R1	Data signal source driver
17	D3_R1	Data signal source driver
18	D4_R1	Data signal source driver
19	D5_R1	Data signal source driver
20	D6_R1	Data signal source driver
21	D7_R1	Data signal source driver
22	VSS	Ground
23	D8_R1	Data signal source driver
24	D9_R1	Data signal source driver
25	D10_R1	Data signal source driver
26	D11_R1	Data signal source driver
27	D12_R1	Data signal source driver
28	D13_R1	Data signal source driver
29	D14_R1	Data signal source driver
30	D15_R1	Data signal source driver
31	XSTL_R1	Start pulse source driver
32	XLE_R1	Latch enable source driver
33	XOE_R1	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

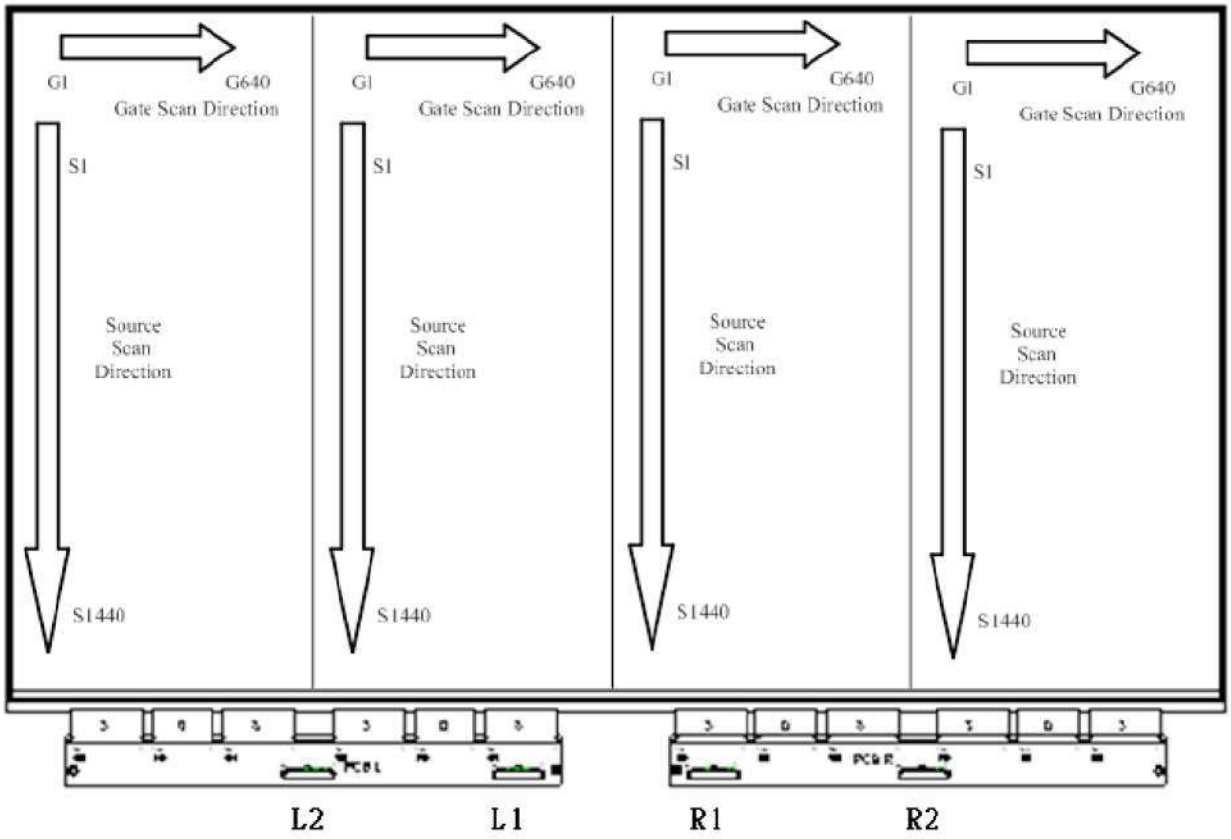
Connector R2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_R2	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_R2	Output enable gate driver
7	CKV_R2	Clock gate driver
8	SPV_R2	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_R2	Clock source driver
14	D0_R2	Data signal source driver
15	D1_R2	Data signal source driver
16	D2_R2	Data signal source driver
17	D3_R2	Data signal source driver
18	D4_R2	Data signal source driver
19	D5_R2	Data signal source driver
20	D6_R2	Data signal source driver
21	D7_R2	Data signal source driver
22	VSS	Ground
23	D8_R2	Data signal source driver
24	D9_R2	Data signal source driver
25	D10_R2	Data signal source driver
26	D11_R2	Data signal source driver
27	D12_R2	Data signal source driver
28	D13_R2	Data signal source driver
29	D14_R2	Data signal source driver
30	D15_R2	Data signal source driver
31	XSTL_R2	Start pulse source driver
32	XLE_R2	Latch enable source driver
33	XOE_R2	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

NOTE1: Detection function pin is for checking IC & Panel status.

5-3 Panel Scan direction

When panel replace the image, the each sub panel need active at same time



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +7	V	--
Positive Supply Voltage	V_{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V	--
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V	--
Supply Voltage	VGH	-0.3 to +55	V	--
Supply Voltage	VGL	-32 to +0.3	V	--
Supply Range	VGH-VGL	-0.3 to +55	V	--
Operating Temp. Range	TOTR	-15 to +65	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

6.2 Display Module DC Characteristics

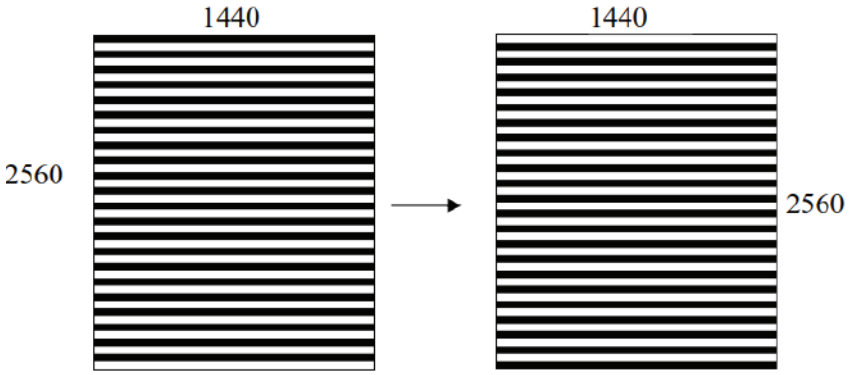
this is the total current for 4 sub panel

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		2.7	3.3	3.6	V
	I_{VDD}	V_{DD}= 3.3V	-	3	7	mA
Gate Negative supply	V_{GL}		-21	-20	-19	V
	I_{GL}	V_{GL} = -20V	-	4	9	mA
Gate Positive supply	V_{GH}		21	22	23	V
	I_{GH}	V_{GH} = 22V	-	3	6	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V	-	7	415	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V
	I_{POS}	V_{POS} = 15V	-	7	445	mA
Asymmetry source	V_{Asym}	V_{POS}+V_{NEG}	-800	-	+800	mV
Common voltage	V_{COM}		-2.96	Adjusted	-2.04	V
	I_{COM}		-	1.2	-	mA
Panel power	P		-	370	13300	mW
Standby power panel	P_{STBY}		-	-	1.32	mW
Rush current	I_{DD}	VDD=3.3V	-260		260	mA
	I_{GL}	VGL=-20V	-2700		2700	mA
	I_{GH}	VGH=22V	-230		230	mA
	I_{NEG}	V_{NEG}=-15V	-2000			mA
	I_{POS}	V_{POS}=15V			2000	mA
	Icom		-800		800	mA

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines.(Note 6-1)
- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by ODNA.
- Vcom is recommended to be set in the range of assigned value ±0.1V.
- The maximum I_{COM} inrush current is about 2 mA.
- The rushcurrent is for reference only.

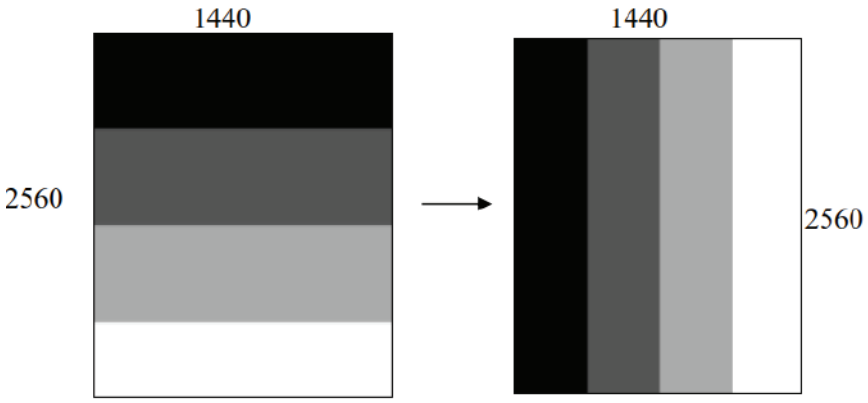
Note 6-1

The maximum power consumption



Note6-2

The Typical power consumption



6.3 Refresh Rate

The module AEZ25601440A00-31.2ENRS is applied at a maximum screen refresh rate of 50Hz

	Min	Max
Refresh Rate	-	50Hz

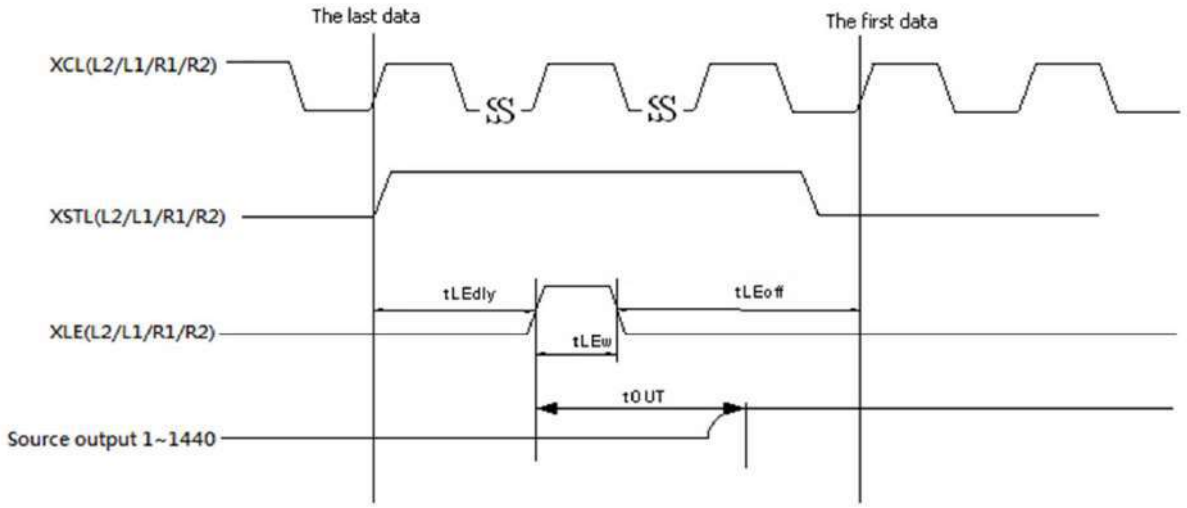
6.4 Panel AC characteristics

VDD=2.7 V to 3.6V, unless otherwise specified.

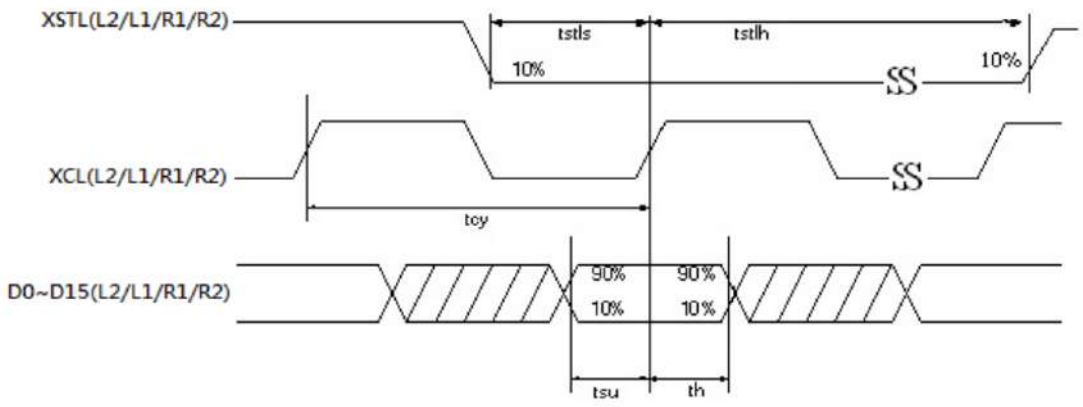
For 1/4 panel (the timing parameter for each sub panel)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum "L" clock pulse width	twL	0.5	-	-	us
Minimum "H" clock pulse width	twH	0.5	-	-	us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20	-	ns
D0 .. D15 setup time	tsu	8	-	-	ns
D0 .. D15 hold time	th	8	-	-	ns
XSTL setup time	tstls	8	-	-	ns
XSTL hold time	tstlh	8	-	-	ns
XLE on delay time	tLEdly	40	-	-	ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	12	us

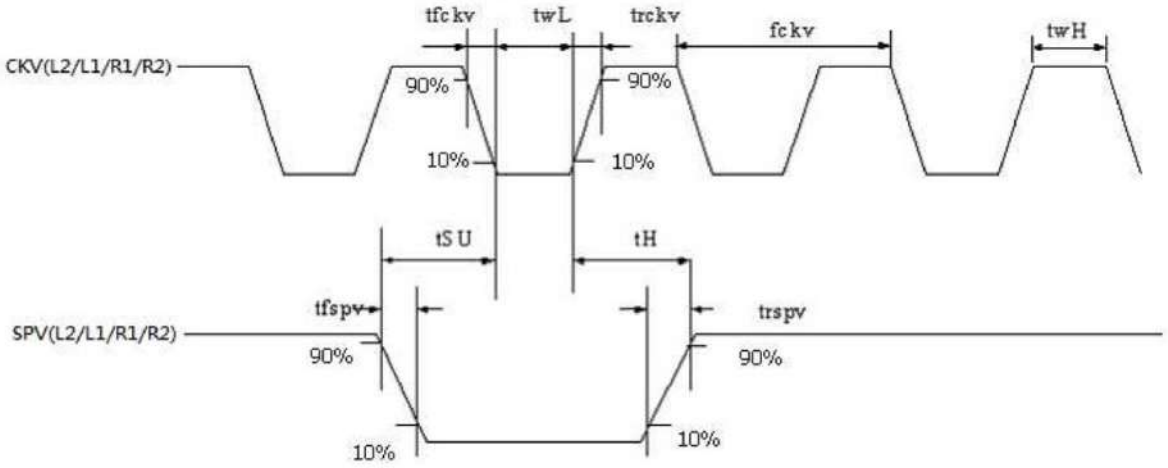
OUTPUT LATCH CONTROL SIGNALS



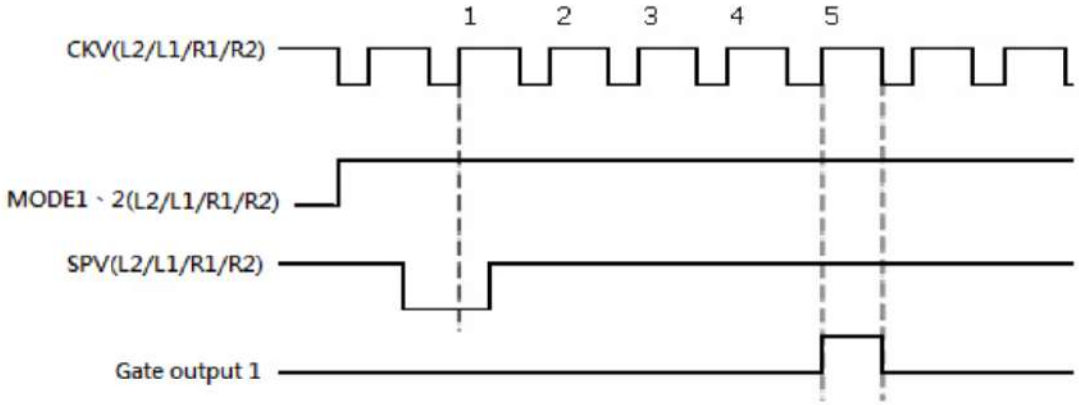
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note：First gate line on timing

After 5CKV, Gate output 1 is on.

6.5 Controllers Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE)[3] and Gate Driver Clock (GDCK)[3]. Note, that in this mode LGON follows GDCK timing.

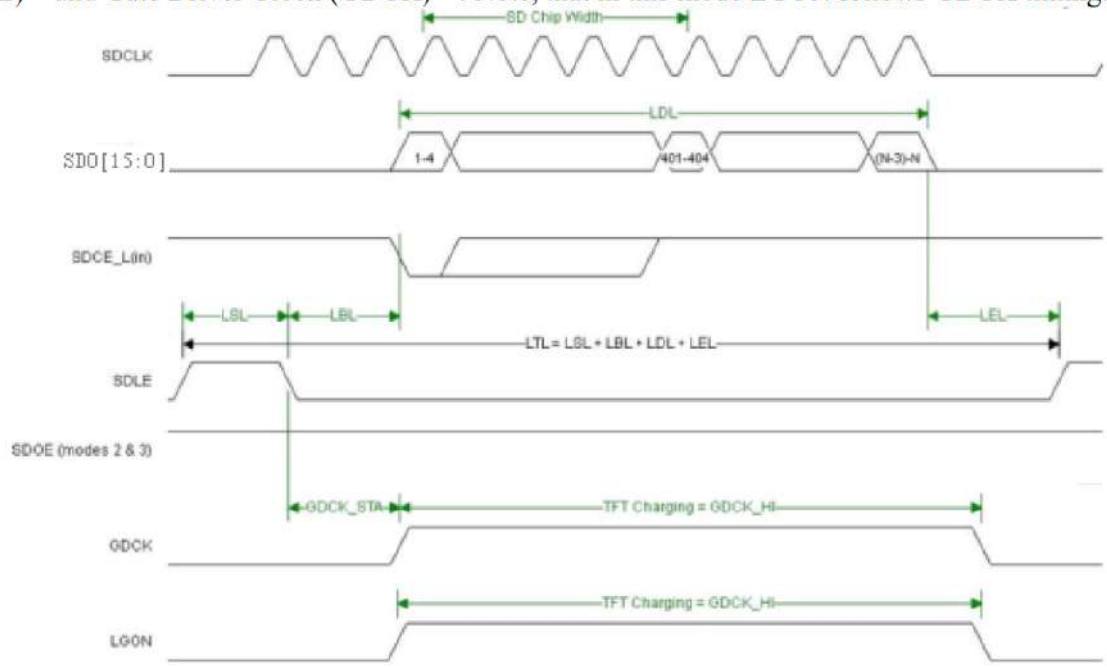


Figure 1 Line Timing in Mode 3

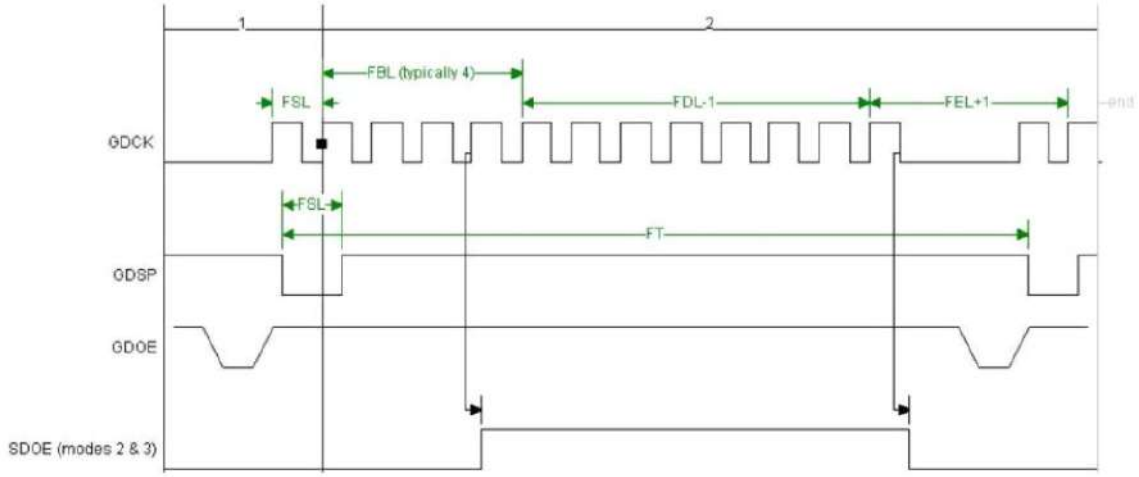


Figure 2 Frame Timing in Mode 3

Table Timing Parameters Table

For 1/4 panel

Mode	3	Resolution 1440x640				
SDCLK [MHz]	10.00					
Pixels per SDCLK	8					
Line Parameters	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
[SDCLK]	11	11	180	101	11	280
Line Parameters	-	-	-	-	-	-
[us]	1.10	1.10	18.00	10.10	1.10	28.00
Frame Parameters	FSL	FBL	FDL	FEL	-	FR[Hz]
[Lines]	1	4	640	14	-	50.08
Frame	-	-	-	-	-	-
Parameters[us]	30.30	121.20	19392.00	424.20	-	-

Note 1: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL.

Note 2:

SDCLK = XCL(L2/L1/R1/R2)

SDD[15:0] = D0~D15(L2/L1/R1/R2)

SDCE_L(in) = XSTL(L2/L1/R1/R2)

GDCK = CKV(L2/L1/R1/R2)

GDSP = SPV(L2/L1/R1/R2)

GDOE = Mode1、2(L2/L1/R1/R2)

SDOE = XOE(L2/L1/R1/R2)

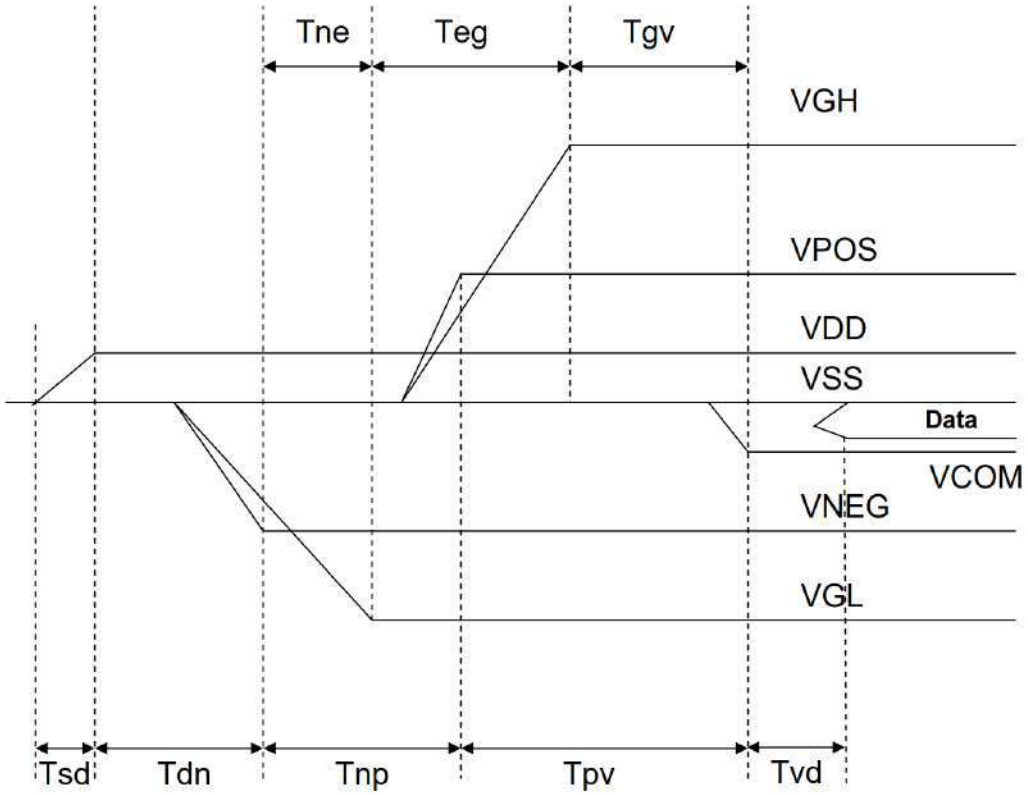
7. Power Sequence

Power Rails must be sequenced in the following order:
1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

Note:

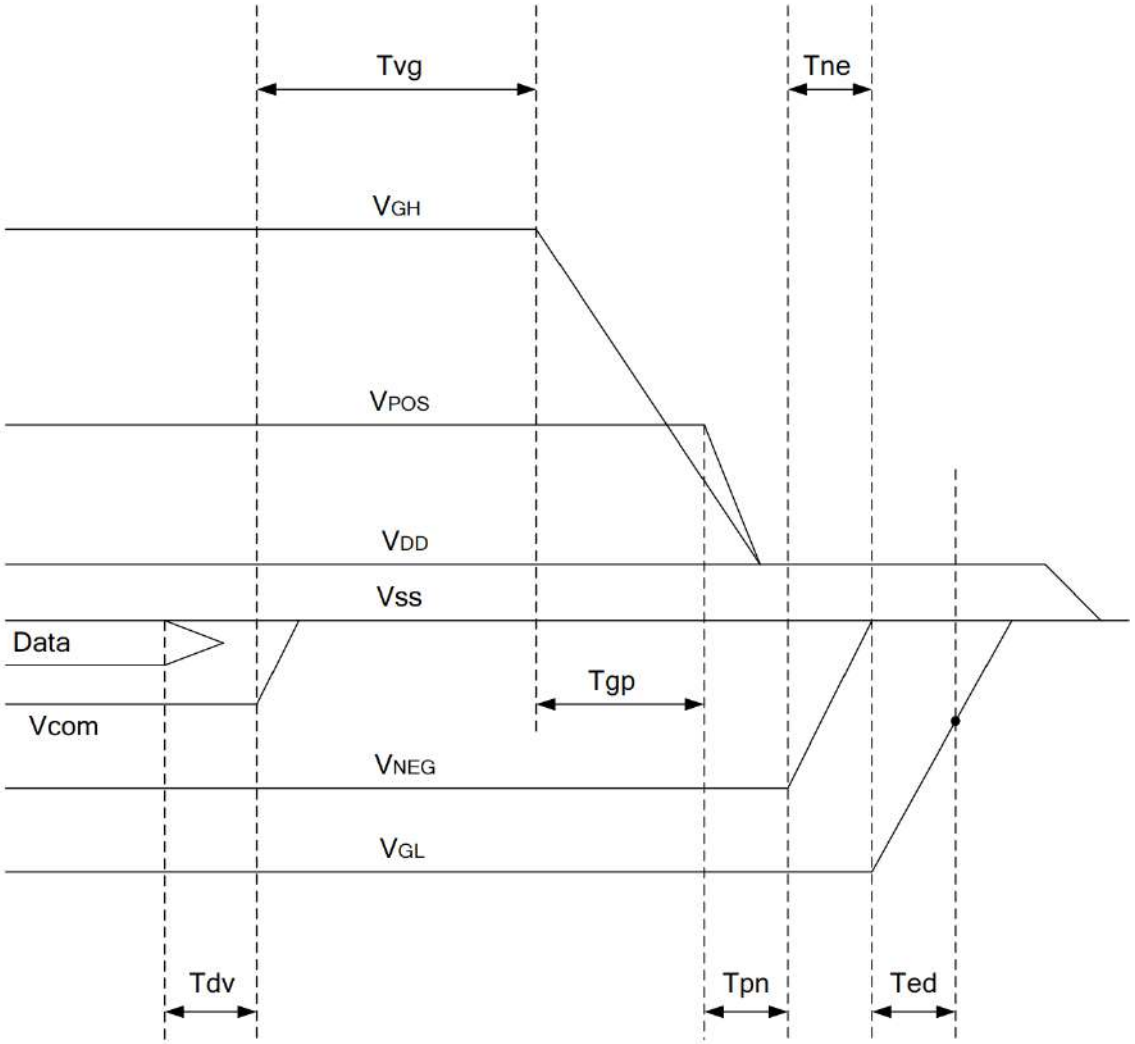
- VGL should be turned off after VNEG and VPOS have been turned off and returned to the ground state.
- VGL should be turned off after the Vcom has been turned off and returned to the ground state.
- All of Vcom/VNEG/VPOS/VGN/VGL MUST turn off right after data transfer completes.

Power on



	Min	Max
Tsd	30us	-
Tdn	100us	-
Tnp	1000us	-
Tpv	100us	-
Tvd	100us	-
Tne	0us	-
Teg	1000us	-
Tgv	100us	-

Power off



	Min	Max	
Tdv	100 μs	-	
Tvg	0 μs	-	
Tgp	0 μs	-	
Tpn	0 μs	-	
Tne	0 μs	-	
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note1 ： Supply voltages decay through pull-down resistors.

8. Optical characteristics

8.1 Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	40	-	%	Note 8-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	12	-		

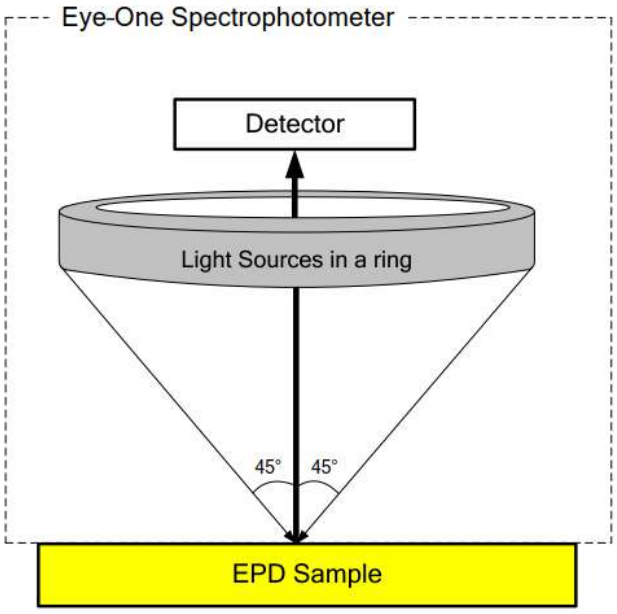
WS: White state, DS: Dark state, Gray state from Dark to White: DS、G1、G2…、Gn…、Gm-2、WS

m: 4、8、16 when 2、3、4 bits mode.

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer.

8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl/Rd



8.3 Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirement

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter cause circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status
Product specification
This data sheet contains Preliminary product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Where application information is given, it is advisory and does not form part of the specification.

Remark
All the specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any post-assembly operation.

10. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +65°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = -15°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 168 hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
8	Solar radiation test	765 W/m^2 for 168hrs, 40℃ Test in white pattern	IEC60 068-2-5Sa	
9	Package Vibration	Random wave(1.5Grms 10~200Hz) Direction: X,Y,Z 30mins per axes	Full packed for shipment	
10	Package Drop Impact	Height: 15.2 cm. 6 faces	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	

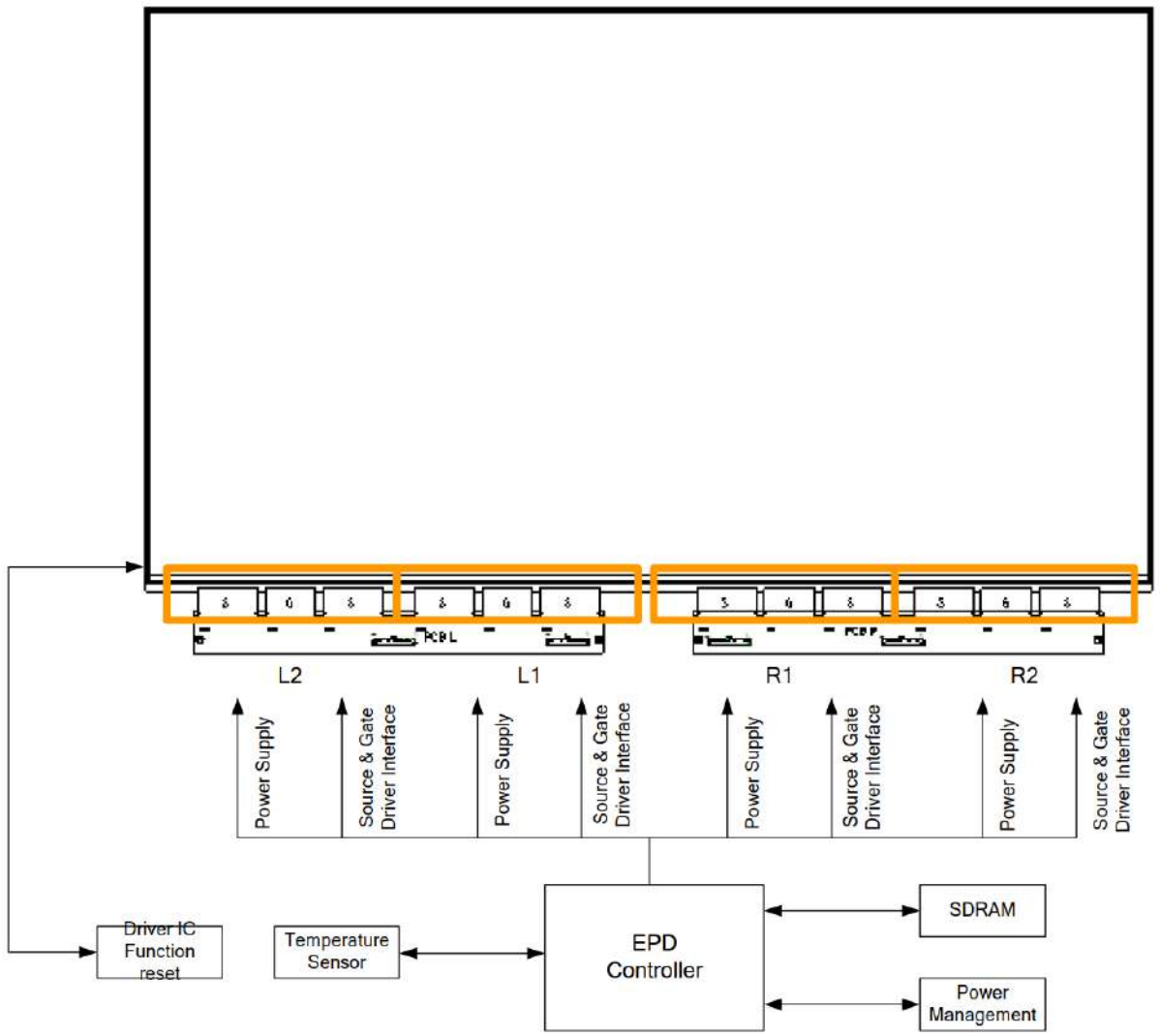
Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

< Criteria >

In the standard conditions, there is not display function NG issue occurred. (Line defect, no image).

All the cosmetic specification is judged before the reliability stress.

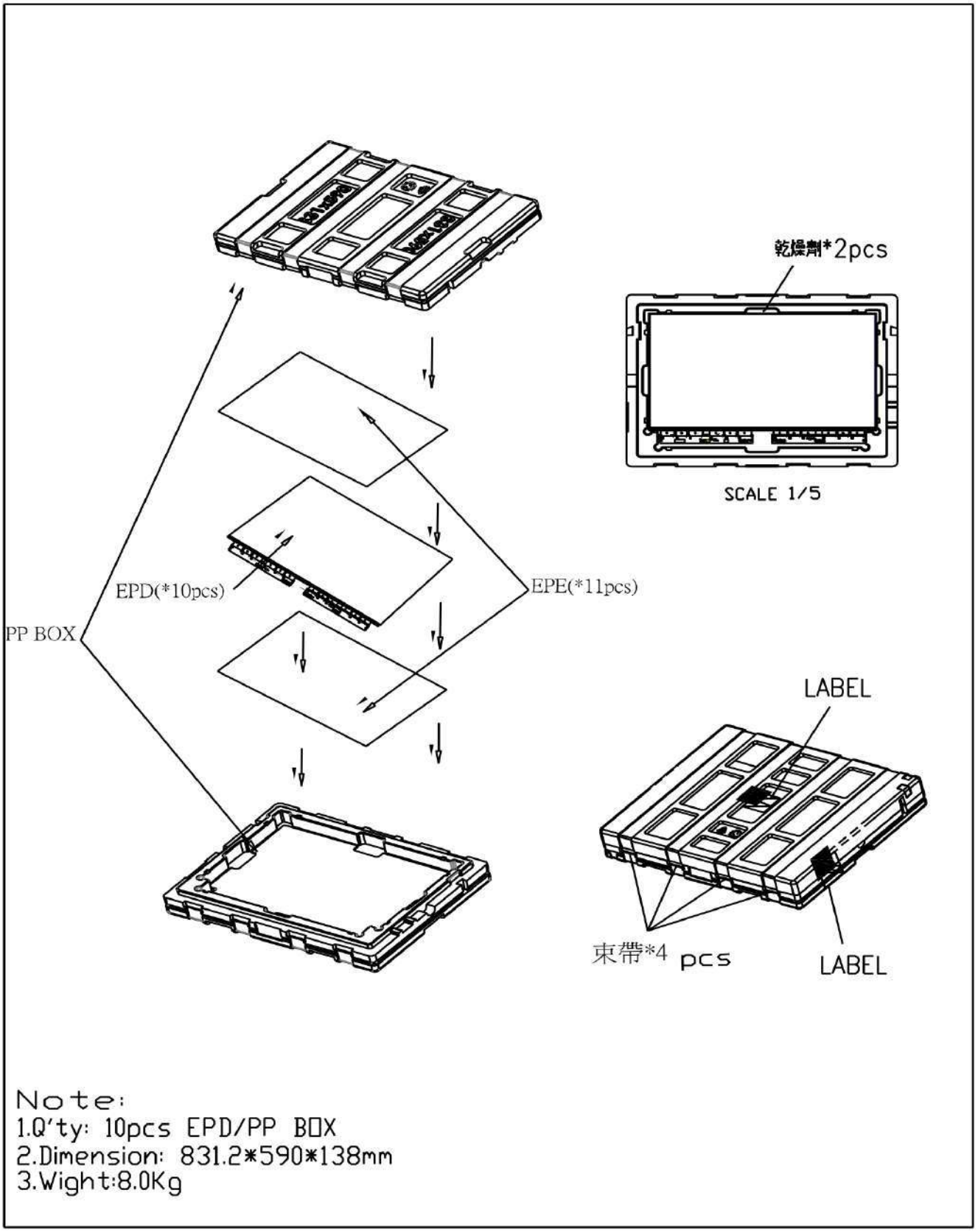
11.Block Diagram



12. Bar Code definition

TBD

13.Packing


乾燥劑*2pcs
SCALE 1/5
EPD(*10pcs)
EPE(*11pcs)
PP BOX
LABEL
束帶*4 pcs
LABEL
Note:
1.Q'ty: 10pcs EPD/PP BOX
2.Dimension: 831.2*590*138mm
3.Wight:8.0Kg