Specification for E-Paper

AEZ21602880A00-42.0ENRS

Revision 3.0

A	Orient Display
EZ	E-Paper
21602880	Resolution 2160 x 2880
A00	Revision A00
42.0	Diagonal: 42.0’’, Module: 650(H)x872.5(V)x0.805(D) mm
E	EPD - Electrophoretic Display (Active Matrix)
N	Top: -15°C ~ +65°C; Tstr: -25°C ~ +70°C
R	Reflective Polarizer
S	3-/4-wire SPI Interface
/	Controller
/	ZIF FPC
/	Ultra Wide Viewing Angle
/	Ultra Low Power Consumption

REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	NOV.25.2019	New Creation	ALL	
2.0	JAN.22.2024	New Creation	ALL	
3.0	JAN.22.2024	New Creation	ALL	

LIST

1. General Description

AEZ21602880A00-42.0ENRS is a reflective electrophoretic technology display module based on active matrix TFT substrate. It has 42” active area with 2160 x 2880 pixels and 3:4 aspect ratios. The display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

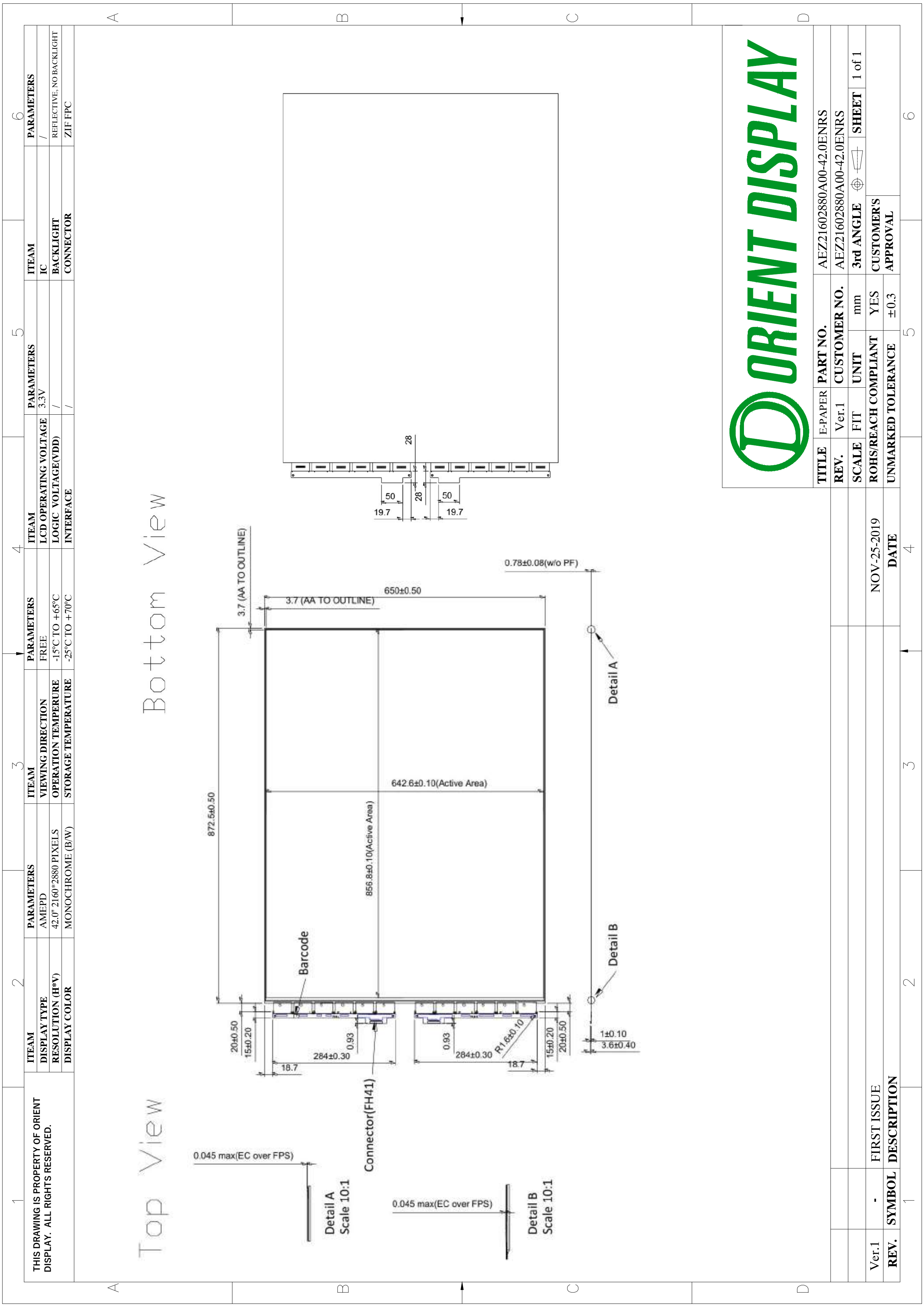
2.Features

- High contrast electrophoretic imaging film
- 2160 x 2880 display
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range: 0℃ ~50℃
- Landscape, portrait mode

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	42	Inch	
Display Resolution	2160(H) x 2880(V)	Pixel	3:4
Active Area	642.6(H) x 856.8 (V)	mm	85dpi
Outline Dimension	650(H) x 872.5 (V) x 0.805(D)	mm	
Pixel Pitch	0.2975	mm	
Pixel Configuration	Square		
Module Weight	1100	g	
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		
Glass Substrate	0.5	mm	
Surface Treatment	Hard Coat		

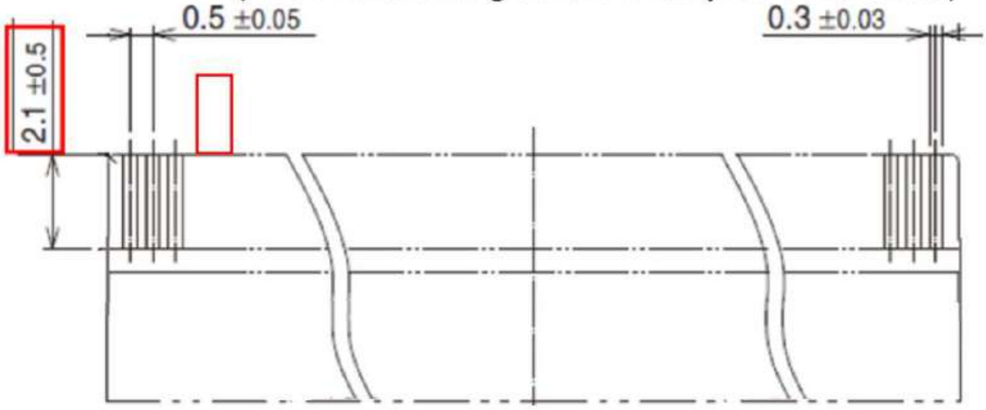
4. Mechanical Drawing of EPD module



5. Input / Output Terminals

5.1 Connector type：FH41-50S-0.5SH compatible.

- **Note 5-1**: Recommended the lead length of the FFC is 2.1mm.
  (The FFC drawing below is only for reference.)



5.2 Pin Assignment

1) PCB_L

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_L	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_L	Output enable gate driver
7	CKV_L	Clock gate driver
8	SPV_L	Start pulse gate driver
9	VSS	Ground
10	VCOM TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_L	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver

26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	NC	Please keep the pin floating
32	XLE_L	Latch enable source driver
33	XOE_L	Outputs enabled when OE is logic “H”,
34	ISEL	Input data bus width selection.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM FPL	Common voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	XSTL_L	Start pulse source driver

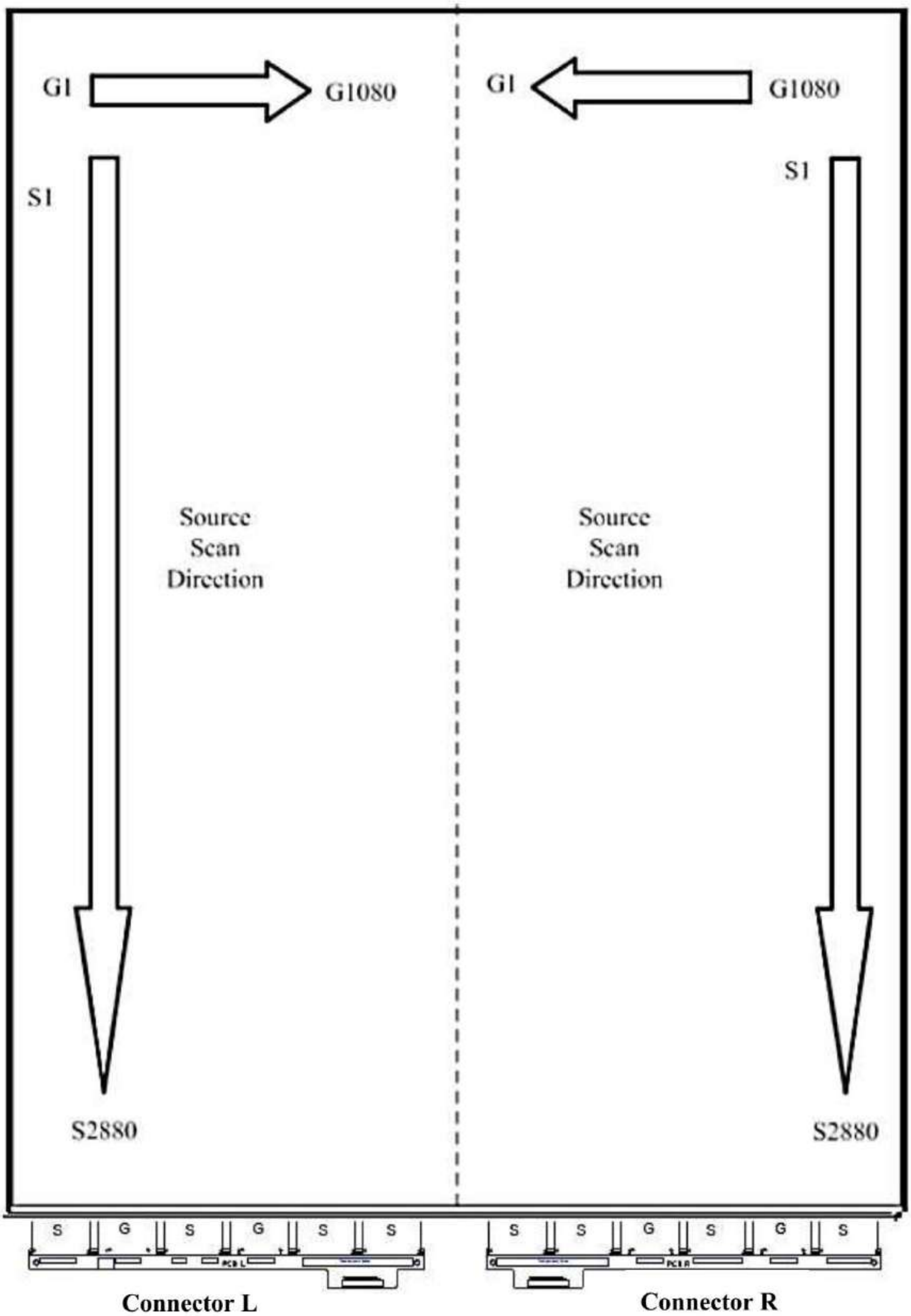
2) PCB_R

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_R	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1_R	Output mode selection gate driver
7	CKV_R	Clock gate driver
8	NC	Please keep the pin floating
9	VSS	Ground
10	VCOM TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground

13	XCL_R	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL_R	Start pulse source driver
32	XLE_R	Latch enable source driver
33	XOE_R	Outputs enabled when OE is logic "H"
34	ISEL	Input data bus width selection.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM FPL	Common voltage
40	NC	Please keep the pin floating
41	SPV_R	Start pulse gate driver
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

5-2 Panel Scan direction

When panel replace the image, each sub panel need to be active at the same time.



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1 Absolution maxing rating: The conditions in the table should not be exceeded; otherwise, the panel may be damaged.

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +7	V	--
Positive Supply Voltage	V_{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V	--
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V	--
Supply Voltage	VGH	-0.3 to +55	V	--
Supply Voltage	VGL	-32 to +0.3	V	--
Supply Range	VGH-VGL	-0.3 to +55	V	--
Operating Temp. Range	TOTR	0 to +50	°C	--
Storage Temperature	TSTG	-25 to +70	°C	--

6.2 Display Module DC Characteristics

Table 6-2 Panel DC characteristics: Please follow the table for the normal operation of the panel; otherwise, it may influence the panel's optical performance.

The standby power (P_{STBY}) is the consumed power when the panel controller is in standby mode. This value is only for reference since it depends on the performance of the panel controller.

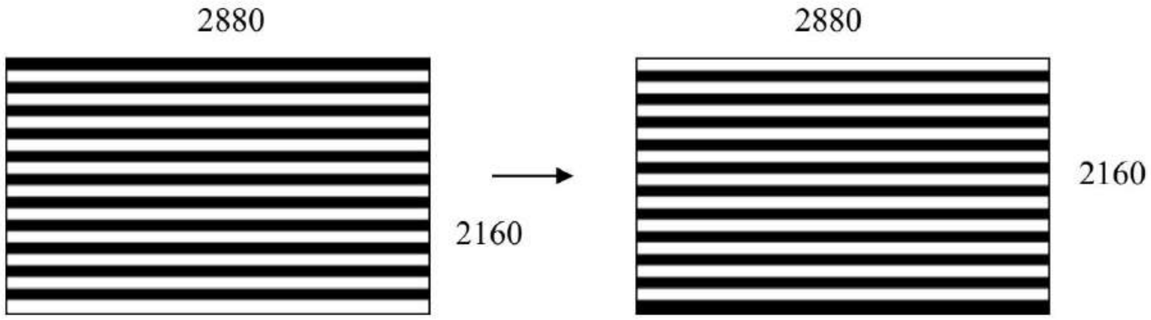
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		2.7	3.3	3.6	V
	I_{VDD}	VDD=3.3V	-	78	84	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{GL}	VGL = -20V		6	6	mA
Gate Positive supply	VGH		26	27	28	V
	I_{GH}	VGH = (27V)		6	6	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V		16	778	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V
	I_{POS}	VPOS = 15V	-	18	780	mA
Asymmetry source	V_{Asym}	VPOS+VNEG	-800	-	+800	mV
Common voltage	V_{COM}		-2	Adjusted	-1	V
	I_{COM}		-	2	-	mA
Panel Power	P		-	1024	23894	mW
Standby Power Panel	P_{STBY}		-	-	112	mW

Rush Current	IDD	VDD=3.3V	-620		620	mA
	IGL	VGL=-20V	-1640		1640	mA
	IGH	VGH=27V	-480		480	mA
	INEG	VNEG=-15V	-1000			mA
	IPOS	VPOS=15V			1000	mA
	ICOM		-870		870	mA

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standby mode which here VDD is ON while other power supplies are OFF.
- The listed electrical/optical characteristics are only guaranteed under the panel controller & waveform provided by ODNA.
- Vcom is recommended to be set in the range of assigned value ±0.1V.
- The rush current is for reference only since it depends on the driving capacity of the panel controller.

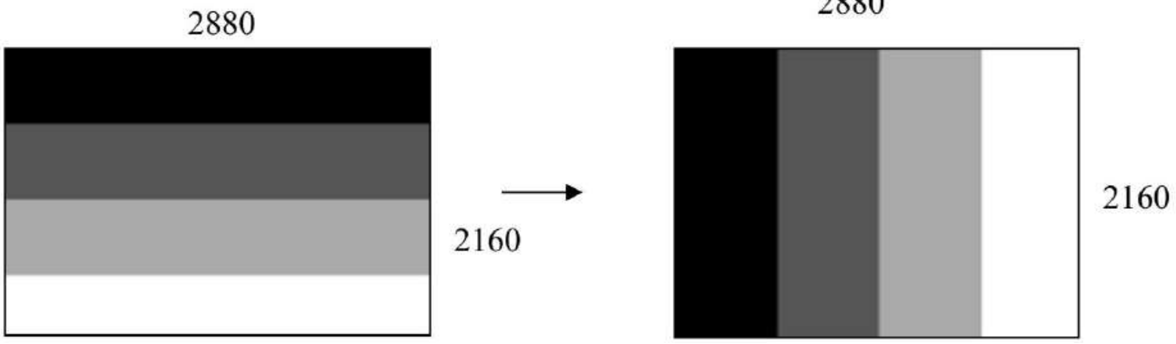
Note 6-1

The maximum power consumption



Note 6-2

The Typical power consumption



6.3 Refresh Rate

The module Polaris is applied at a maximum screen refresh rate of 50Hz.

	Min	Max
Refresh Rate	-	50Hz

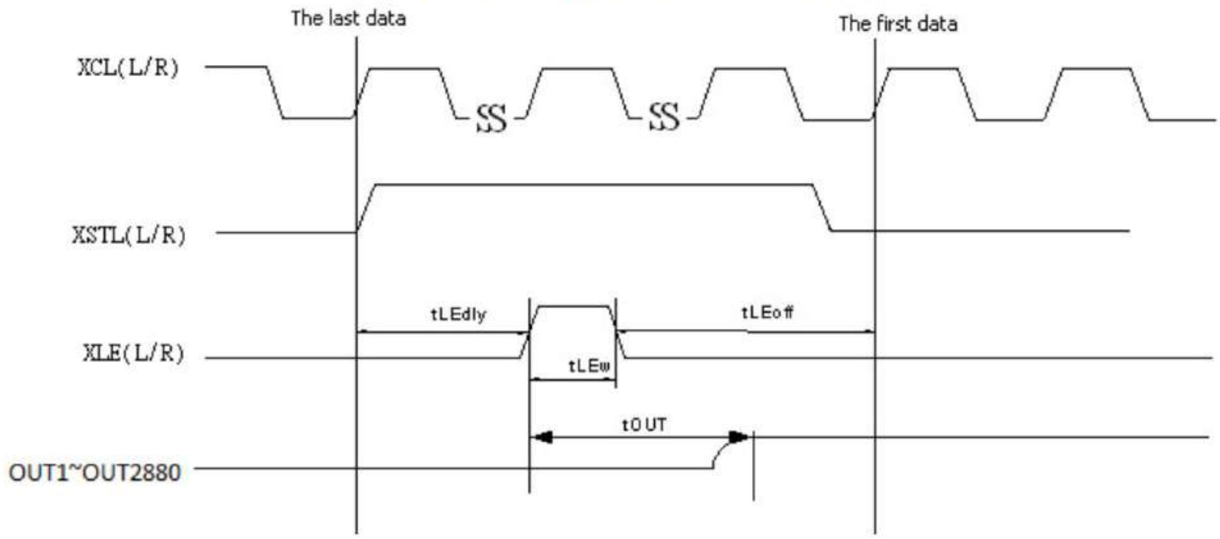
6.4 Panel AC characteristics

VDD=2.7V to 3.6V, unless otherwise specified.

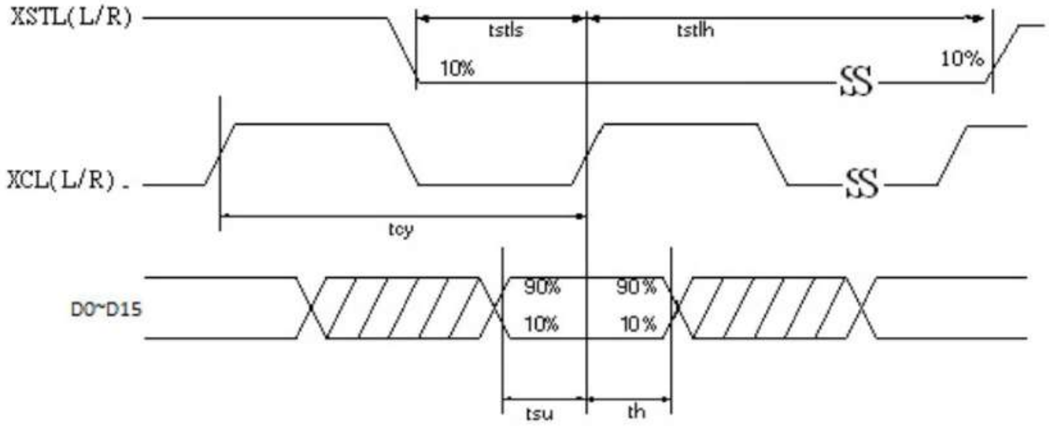
The timing parameter for each sub panel

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv			200	kHz
Minimum "L" clock pulse width	twL	0.5			us
Minimum "H" clock pulse width	twH	0.5			us
Clock rise time	trckv			100	ns
Clock fall time	tfckv			100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20		ns
D0 .. D15 setup time	tsu	8			ns
D0 .. D15 hold time	th	8			ns
XSTL setup time	tstls	8			ns
XSTL hold time	tstlh	8			ns
XLE on delay time	tLEdly	40			ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40			ns
XLE off delay time	tLEoff	200			ns

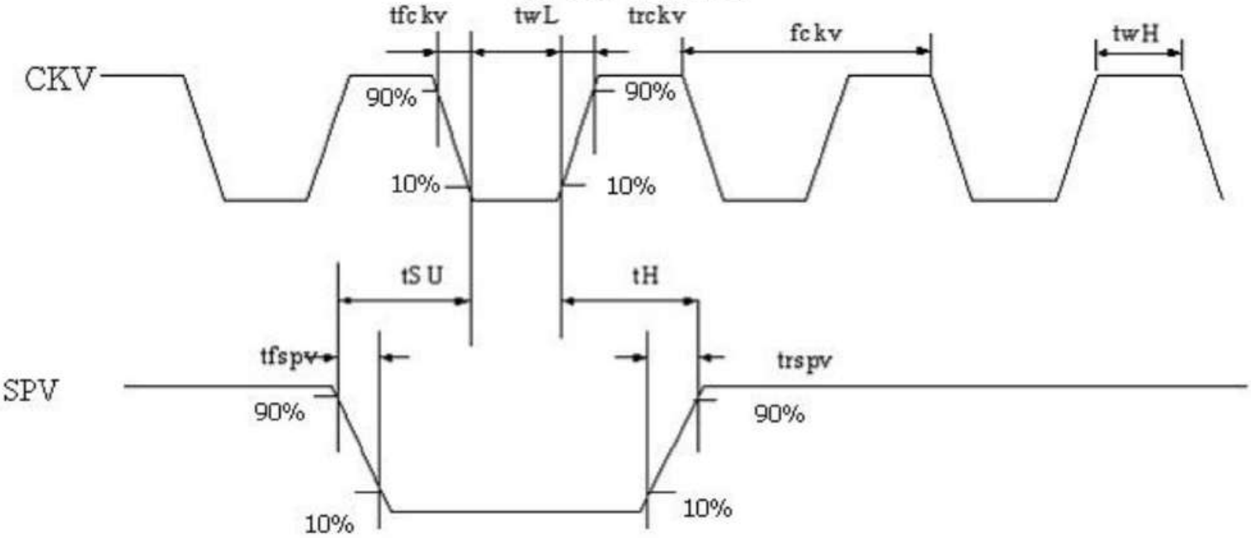
OUTPUT LATCH CONTROL SIGNALS



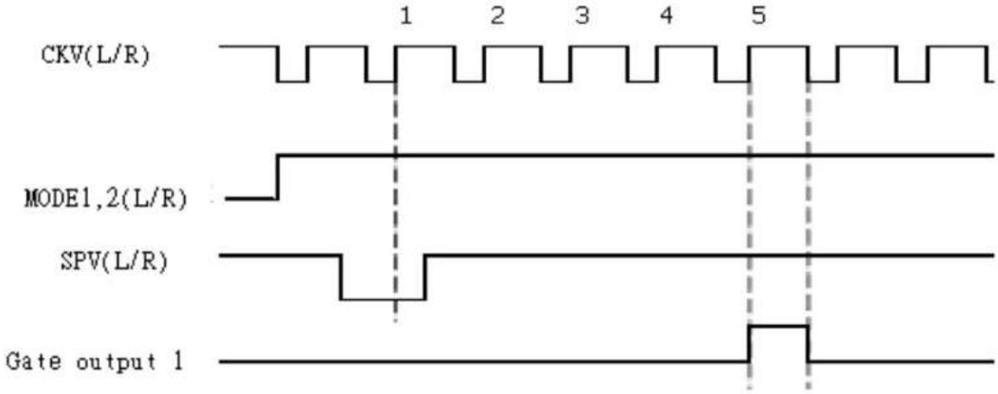
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note 6-3: First gate line on timing

After 5CKV, Gate output 1 is on.

6.5 Controllers Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE)(3) and Gate Driver Clock (GDCK)(3). Note, that in this mode LGON follows GDCK timing.

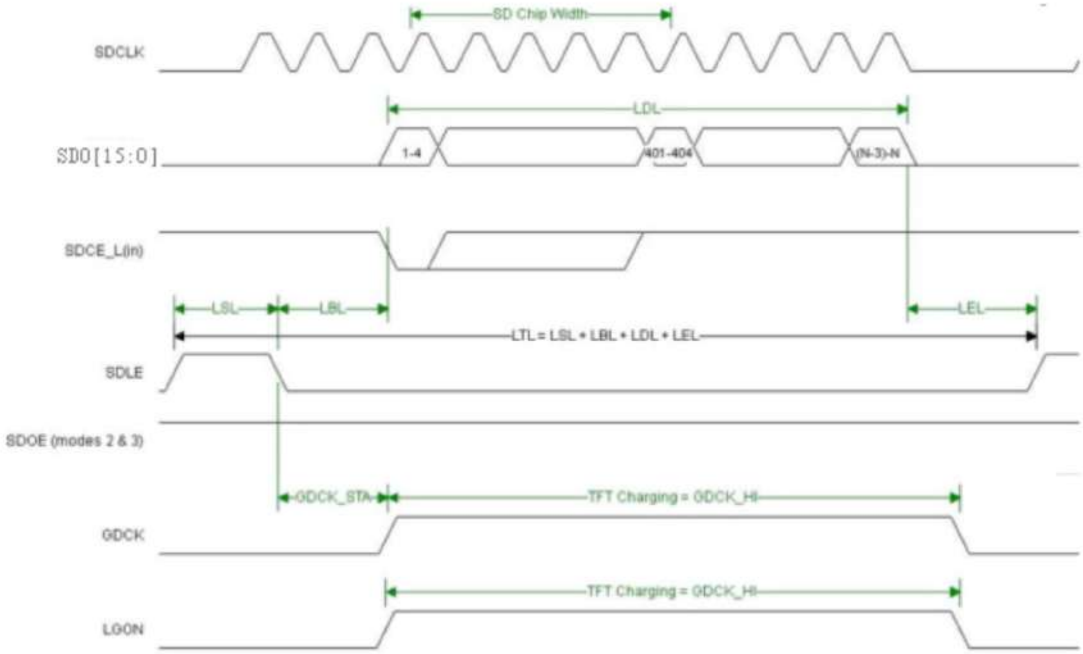


Figure 1 Line Timing in Mode 3

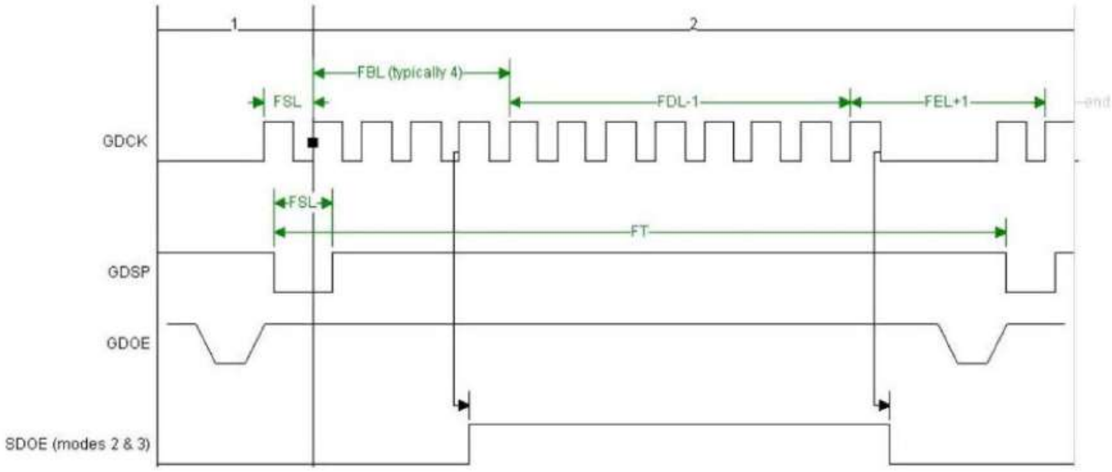


Figure 2 Frame Timing in Mode 3

6.6 Table Timing Parameters Table

Table Timing Parameters Table (For 1 panel)

Mode	3	Timing				
SDCLK[MHz]	42.00	Resolution				5760x1080
Pixels per SDCLK	8					
Line Parameters [SDCLK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	1	5	720	40	37	630
Line Parameters [us]	0.02	0.12	17.14	0.95	0.88	15.04
Frame Parameters [Lines]	FSL	FBL	FDL	FEL	-	FR[Hz]
	1	4	1080	15	-	49.84
Frame Parameters[us]	18.23	72.95	19697	273.57	-	-

Note 1: For parameters definition, see Section 7. Active Matrix Electronic Paper Display Timings.

Note 2: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

Note 3:

- SDCLK = XCL(L /R)
- SDD [15:0] = D0~D15(L/R)
- SDCE_L(in) = XSTL(L /R)
- GDCK = CKV(L /R)
- GDSP = SPV(L /R)
- GDOE = Mode1、2(L /R)
- SDOE = XOE(L/R)

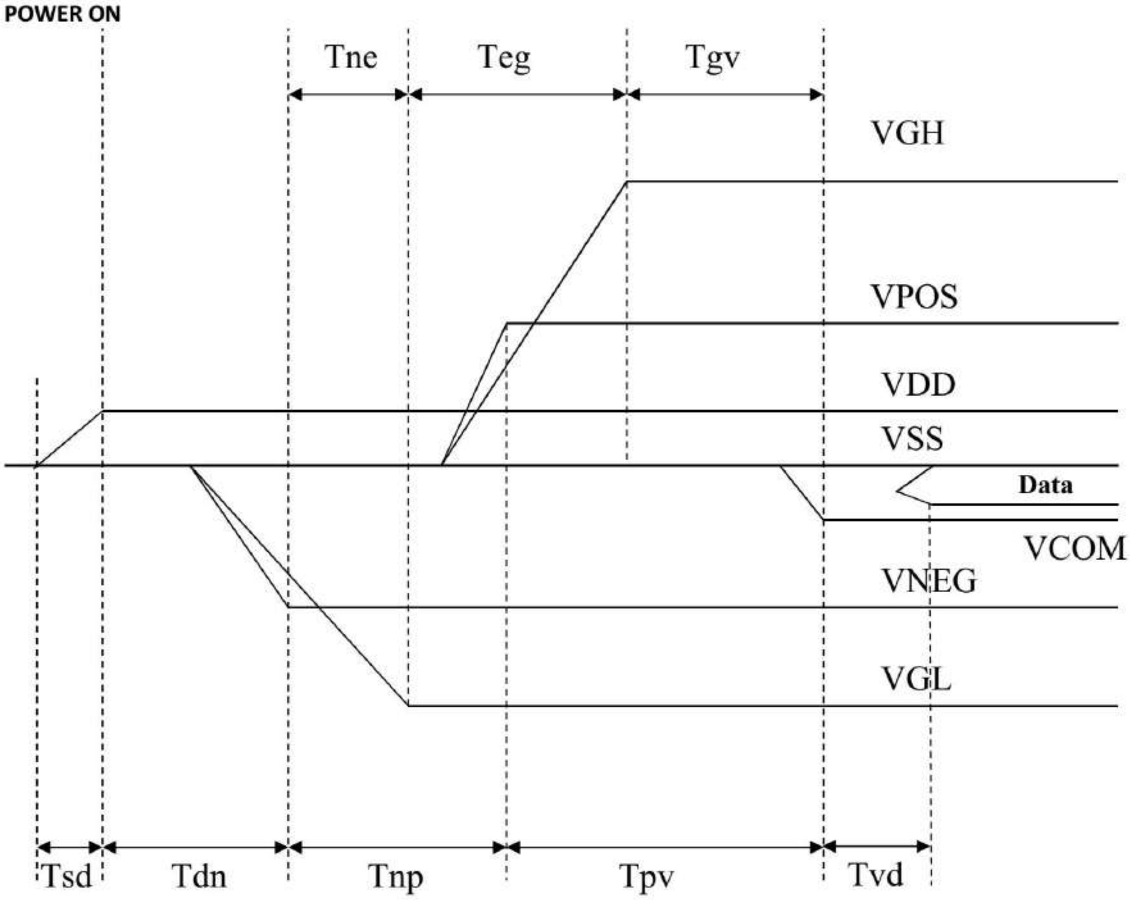
7. Power Sequence

Power Rails must be sequenced in the following order：

1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

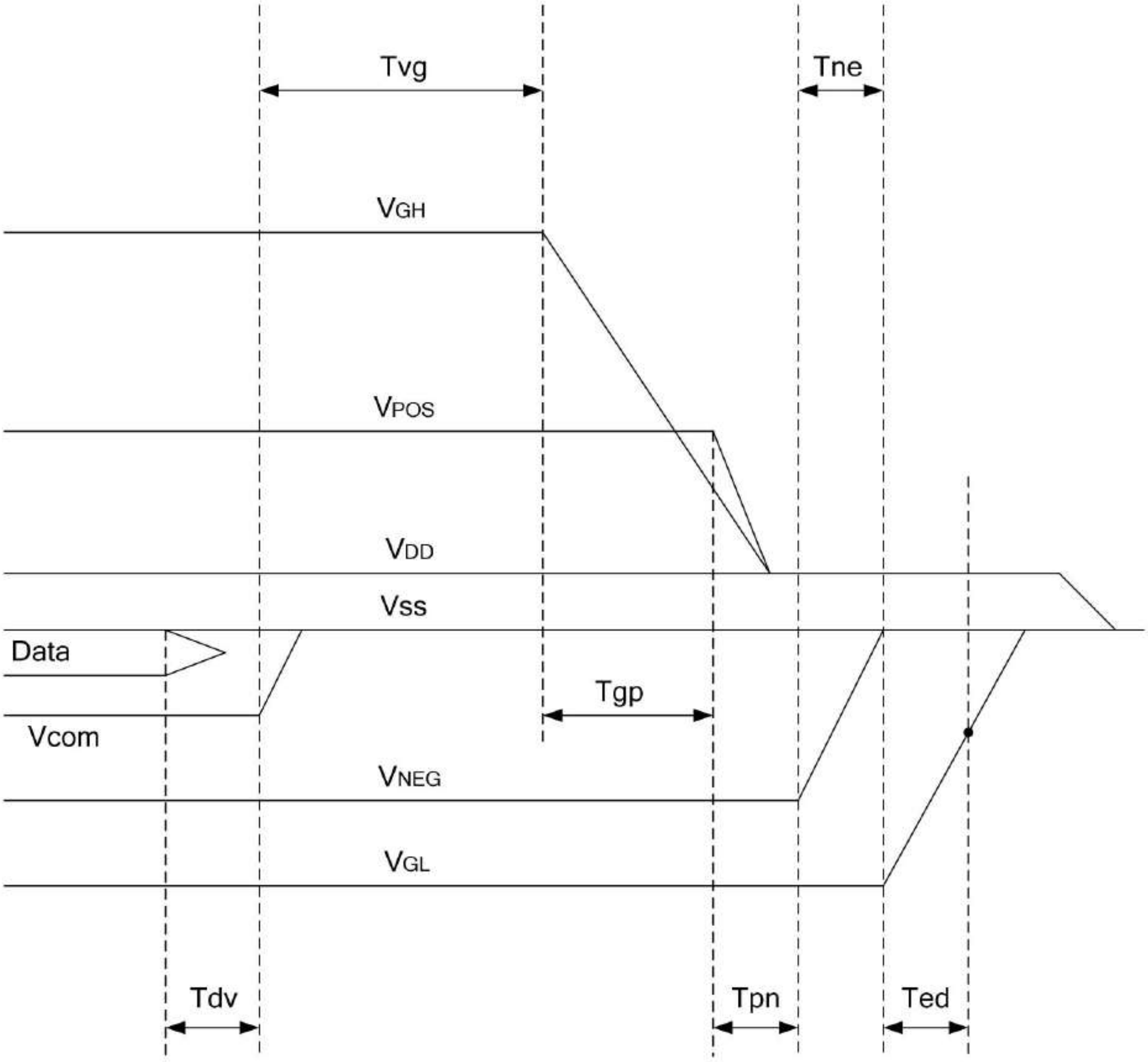
Note7-1:

- VGL should be turned off after VNEG and VPOS have been turned off and returned to the ground state.
- VGL should be turned off after the Vcom has been turned off and returned to the ground state.
- All of Vcom/VNEG/VPOS/VGN/VGL MUST turn off right after data transfer completes.



	Min	Max
Tsd	30us	-
Tdn	100us	-
Tnp	1000us	-
Tpv	100us	-
Tvd	100us	-
Tne	0us	-
Teg	1000us	-
Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note7-2: Supply voltages decay through pull-down resistors.

8. Optical characteristics

8.1 Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	40	-	%	**Note 8-1**
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	12	-		

WS: White state

DS: Dark state

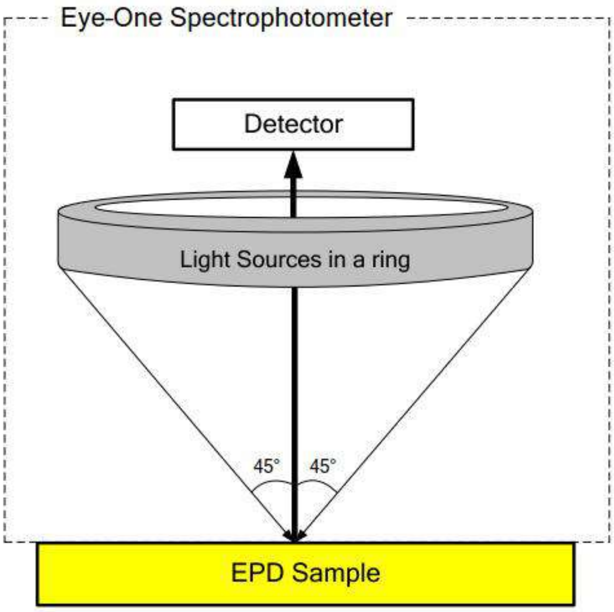
Gray state from Dark to White: DS、G1、G2...、Gn...、Gm-2、WS

m: 4、8、16 when 2、3、4 bits mode

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer

8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl/Rd



8.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor$_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements

WARNING
The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause's circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition these are stress ratings only and operation of the device at these or at any other condition to limiting values for extended periods may affect device reliability.

Application information
Where application information is given, it is advisory and does not form part of the specification

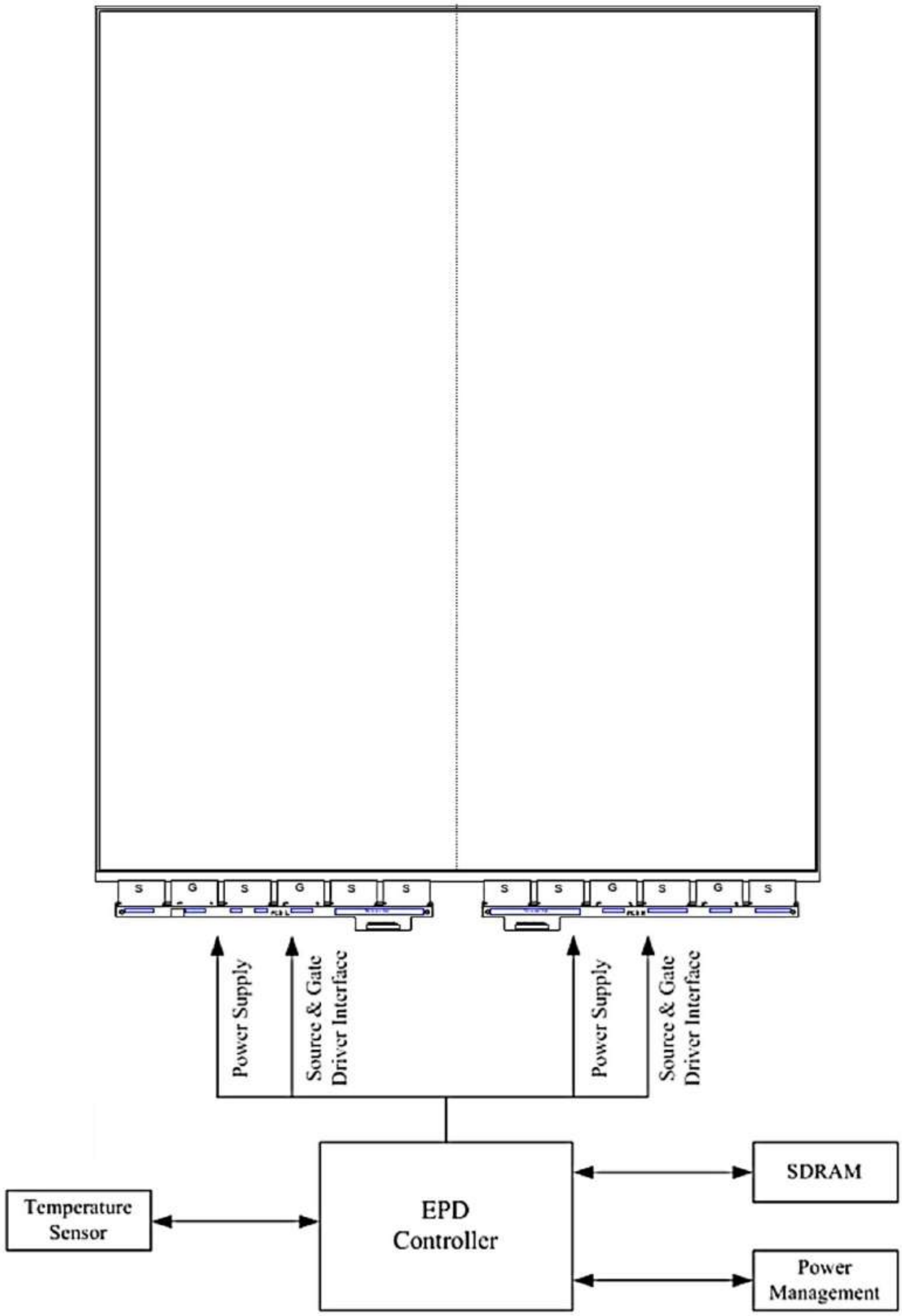
10. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-1Ab	
3	High-Temperature Storage	T = +70°C, RH=40% for 240 hrs Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-78	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 240 hrs Test in white pattern	IEC 60 068-2-78	
7	Temperature Cycle	-25℃ → +70℃, 100 Cycles (30min) (30min) Test in white pattern	IEC 68-2-14Nb	
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ Test in white pattern	IEC60 068-2-5Sa	
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
10	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3 edges, 6 faces One drop for each.	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62180	

Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

< Criteria >
In the standard conditions, there is not display function NG issue occurred. (Including: line defect, no image). All the cosmetic specification is judged before the reliability stress.

11.Block Diagram



12. Bar Code definition

TBD

13.Packing

TBD