Specification for E-Paper

AEZ122250A00-2.13ENRWS

Revision 1.0

A	Orient Display
EZ	E-Paper
122250	Resolution 122 x 250
A00	Revision A00
2.13	Diagonal: 2.13’’, Module: 29.2(H)×59.2 (V) ×1.65(D)mm
E	EPD - Electrophoretic Display (Active Matrix)
N	Top: 0°C ~ +50°C; Tstr: -25°C ~ +70°C
R	Reflective Polarizer
W	White Front Light
S	3-/4-wire SPI Interface
/	Controller SSD1680 Or Compatible
/	ZIF FPC
/	Ultra Wide Viewing Angle
/	Ultra Low Power Consumption

REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	MAR.14.2025	New Creation	ALL	

LIST

1. Over View

AEZ122250A00-2.13ENRWS is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black full display capabilities. The 2.13 inch active area contains 122×250 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

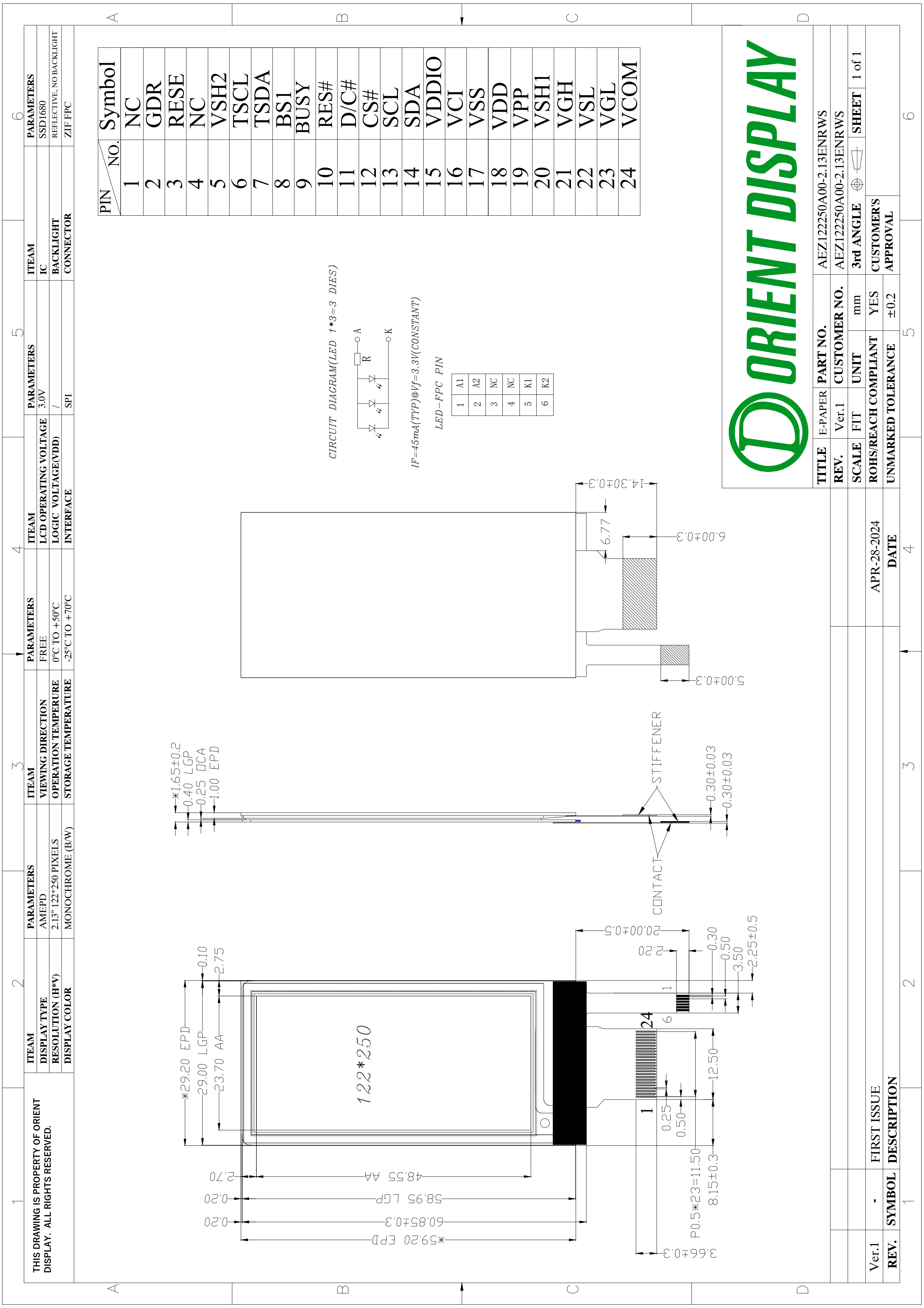
2.Features

- 122×250 pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read external temperature sensor
- Built-in temperature sensor

3. Mechanical Specifications

Parameter	**Specifications**	**Unit**	**Remark**
Screen Size	2.13	Inch	
Display Resolution	122(H)×250(V)	Pixel	Dpi:130
Active Area	23.7×48.55	mm	
Pixel Pitch	0.1943×0.1942	mm	
Pixel Configuration	Square		
Outline Dimension	29.2(H)×59.2 (V) ×1.65(D)	mm	
Weight	TBD	g	

4. Mechanical Drawing of EPD module



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ITEAM	PARAMETERS	ITEAM	PARAMETERS	ITEAM	PARAMETERS	ITEAM	PARAMETERS
DISPLAY TYPE	AMEPD	VIEWING DIRECTION	FREE	LCD OPERATING VOLTAGE	3.0V	IC	SSD1680
RESOLUTION (H*V)	2.13" 122*250 PIXELS	OPERATION TEMPERURE	0°C TO +50°C	LOGIC VOLTAGE(VDD)	/	BACKLIGHT	REFLECTIVE, NO BACKLIGHT
DISPLAY COLOR	MONOCHROME (B/W)	STORAGE TEMPERATURE	-25°C TO +70°C	INTERFACE	SPI	CONNECTOR	ZIF FPC

PIN NO.	Symbol
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TSDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM

LED-FPC PIN

1	A1
2	A2
3	NC
4	NC
5	K1
6	K2

ORIENT DISPLAY

TITLE	E-PAPER	PART NO.	AEZ122250A00-2.13ENRWS
REV.	Ver.1	CUSTOMER NO.	AEZ122250A00-2.13ENRWS
SCALE	FIT	UNIT	mm
ROHS/REACH COMPLIANT		YES	CUSTOMER'S APPROVAL
UNMARKED TOLERANCE		±0.2	

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REV.	SYMBOL	DESCRIPTION	DATE
Ver.1	-	FIRST ISSUE	APR-28-2024

5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	This pin is I^2C Interface to digital temperature sensor Clock pin. External pull up resistor is required when connecting to I^2C slave. When not in use:VSS	
7	TSDA	I/O	This pin is I^2C Interface to digital temperature sensor Data pin. External pull up resistor is required when connecting to I^2C slave. When not in use: VSS	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	

23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when –Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	**MCU Interface**
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	**Symbol**	**Rating**	**Unit**
Logic supply voltage	VCI	-0.5 to +6.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	°C
Storage Temp range	TSTG	-25 to+70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

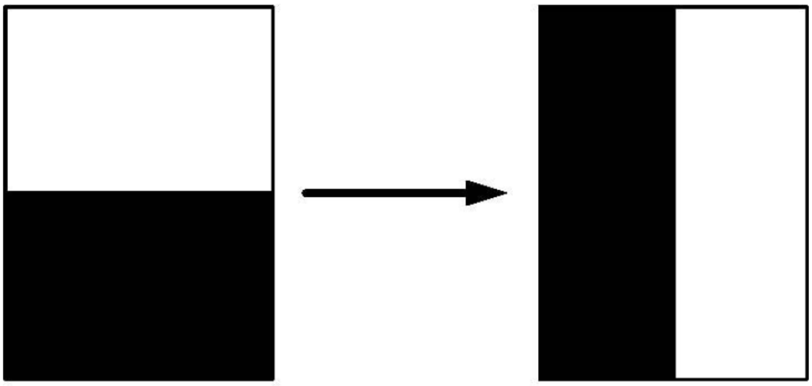
Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.7	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 VCI	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	10.5	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI} =3.0V	-	-	3.5	-	mA
Image update time	-	25 ºC	-	-	3	-	sec
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by ODNA.

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	**Data/Command Interface**		**Control Signal**		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.3.2 MCU Serial Interface (4-wire SPI)

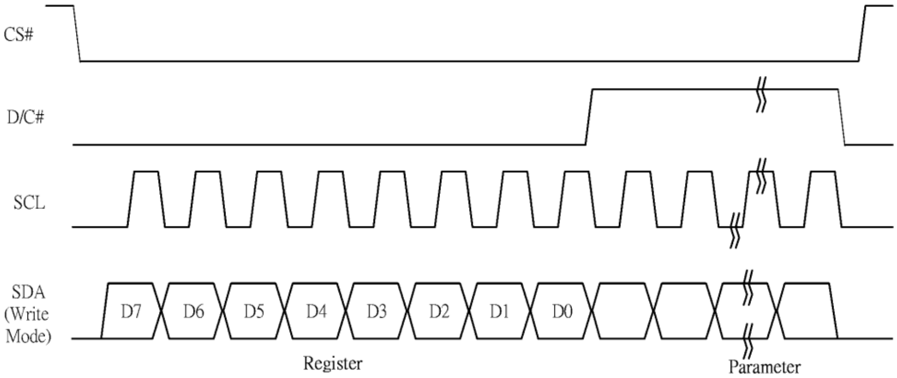
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	**CS#**	**D/C#**	**SCL**
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

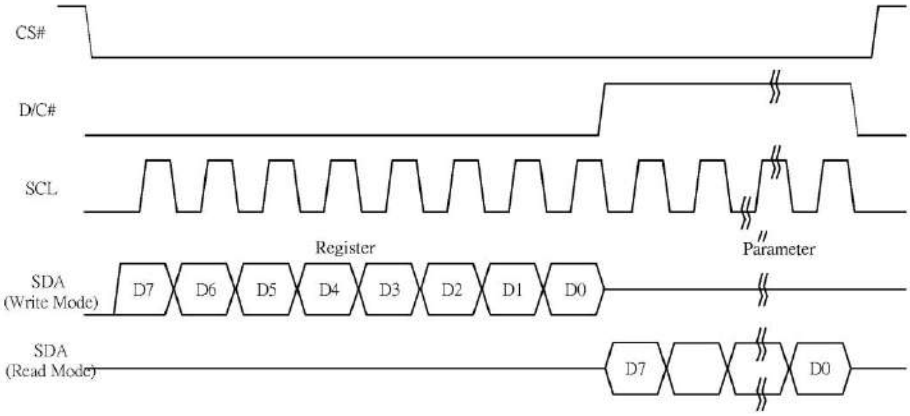
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode



6.3.3 MCU Serial Interface (3-wire SPI)

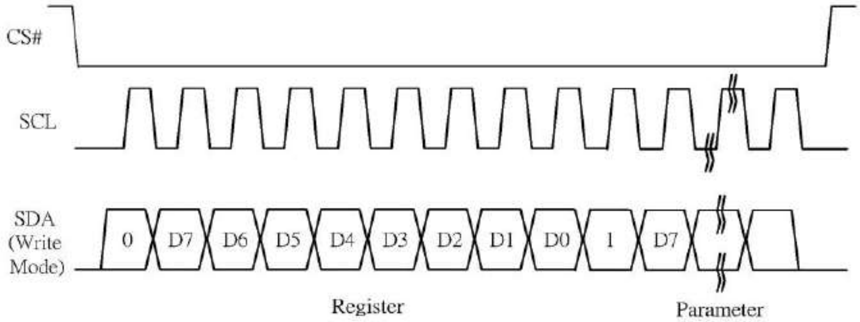
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note： ↑ stands for rising edge of signal

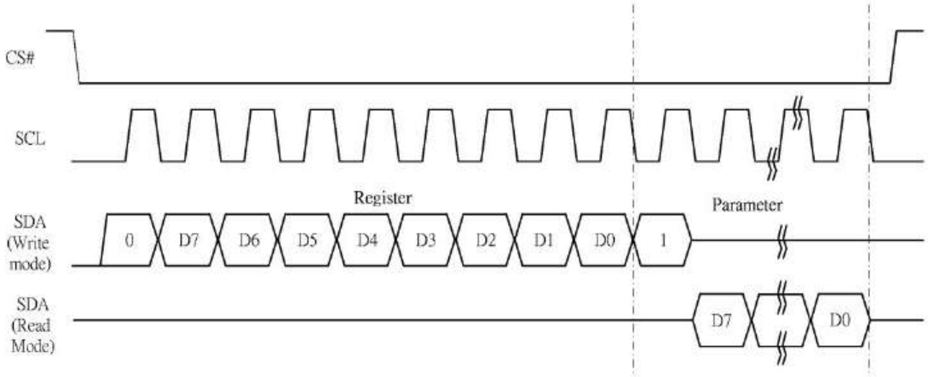
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

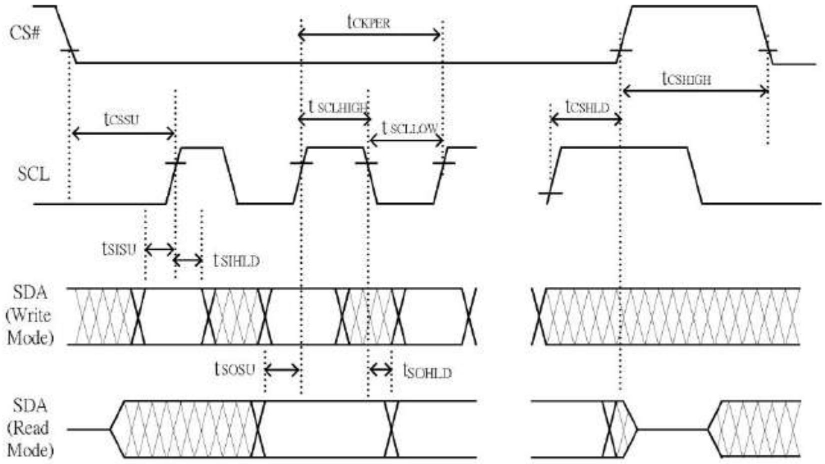
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.



Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

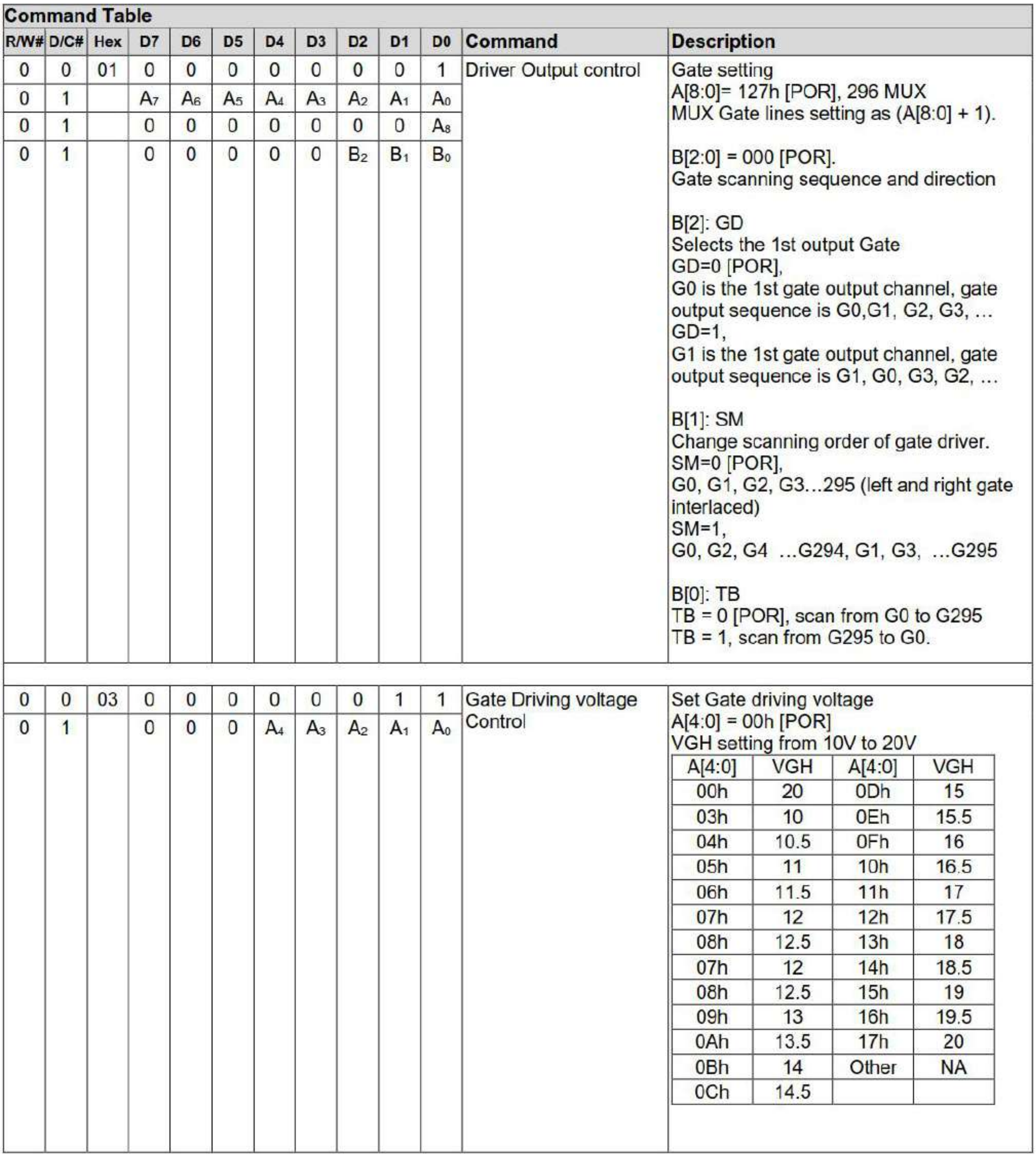
Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)			20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)			2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

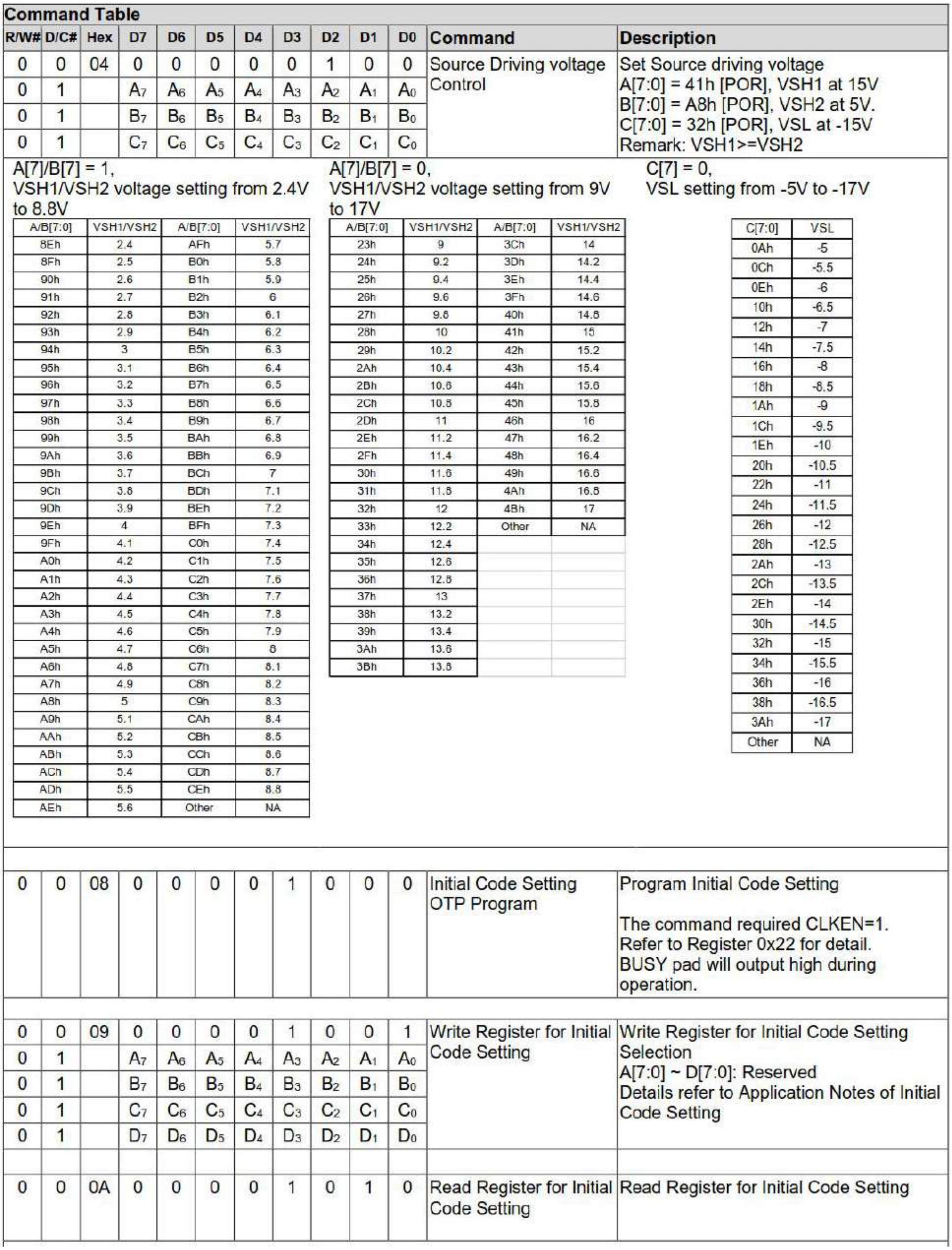
7. Command Table



Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 127h [POR], 296 MUX MUX Gate lines setting as (A[8:0] + 1). B[2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…295 (left and right gate interlaced) SM=1, G0, G2, G4 …G294, G1, G3, …G295 B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	VGH	A[4:0]	VGH
00h	20	0Dh	15
03h	10	0Eh	15.5
04h	10.5	0Fh	16
05h	11	10h	16.5
06h	11.5	11h	17
07h	12	12h	17.5
08h	12.5	13h	18
07h	12	14h	18.5
08h	12.5	15h	19
09h	13	16h	19.5
0Ah	13.5	17h	20
0Bh	14	Other	NA
0Ch	14.5		



Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -5V to -17V

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR]
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		

Bit Description of each byte:
A[6:0] / B[6:0] / C[6:0]:

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control:
0	1		0	0	0	0	0	0	A_1	A_0		

A[1:0] :	Description
00	Normal Mode [POR]
01	Enter Deep Sleep Mode 1
11	Enter Deep Sleep Mode 2

After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.
Remark:
To Exit Deep Sleep mode, User required to send HWRESET to the driver

0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A_6	A_5	A_4	0	A_2	A_1	A_0		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.

<table>
<tr><td>0</td><td>0</td><td>15</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">VCI Detection</td><td rowspan="2">VCI Detection
A[2:0] = 100 [POR] , Detect level at 2.3V
A[2:0] : VCI level Detect<table><tr><th>A[2:0]</th><th>VCI level</th></tr><tr><td>011</td><td>2.2V</td></tr><tr><td>100</td><td>2.3V</td></tr><tr><td>101</td><td>2.4V</td></tr><tr><td>110</td><td>2.5V</td></tr><tr><td>111</td><td>2.6V</td></tr><tr><td>Other</td><td>NA</td></tr></table>
The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.

After this command initiated, VCI detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperatrure sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[11:0] = 7FFh [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_{11}</td><td>A_{10}</td><td>A_9</td><td>A_8</td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1B</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="3">Temperature Sensor Control (Read from temperature register)</td><td rowspan="3">Read from temperature register.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_{11}</td><td>A_{10}</td><td>A_9</td><td>A_8</td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1C</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Temperature Sensor Control (Write Command to External temperature sensor)</td><td rowspan="4">Write Command to External temperature sensor.
A[7:0] = 00h [POR],
B[7:0] = 00h [POR],
C[7:0] = 00h [POR],

A[7:6]<table><tr><th>A[7:6]</th><th>Select no of byte to be sent</th></tr><tr><td>00</td><td>Address + pointer</td></tr><tr><td>01</td><td>Address + pointer + 1st parameter</td></tr><tr><td>10</td><td>Address + pointer + 1st parameter + 2nd pointer</td></tr><tr><td>11</td><td>Address</td></tr></table>A[5:0] – Pointer Setting
B[7:0] – 1st parameter
C[7:0] – 2nd parameter
The command required CLKEN=1.
Refer to Register 0x22 for detail.

After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence

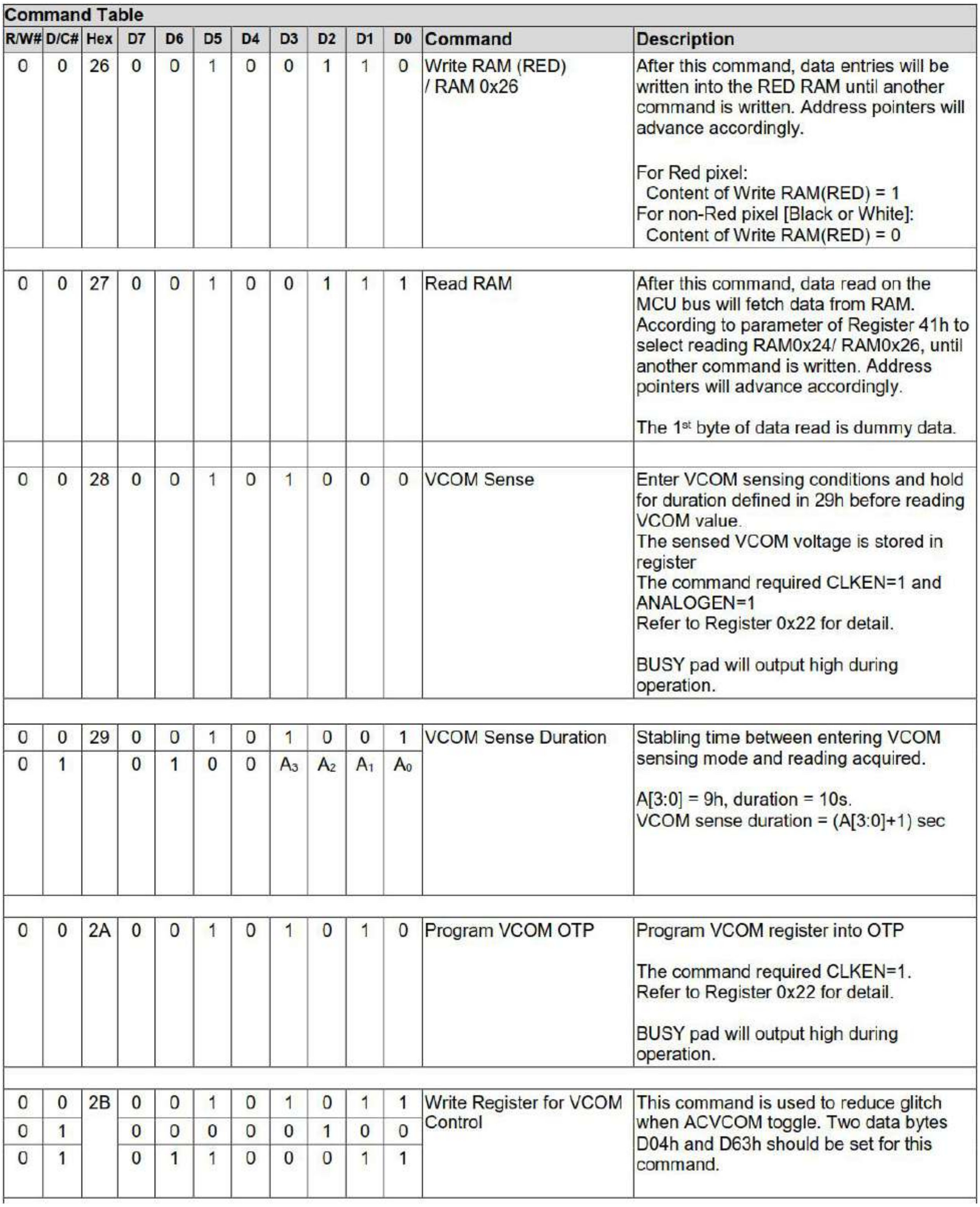
The Display Update Sequence Option is located at R22h.

BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.</td></tr>
</table>

<table>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">Display Update Control 1</td><td rowspan="3">RAM content option for Display Update
A[7:0] = 00h [POR]
B[7:0] = 00h [POR]

A[7:4] Red RAM option<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table>
A[3:0] BW RAM option<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table>
B[7] Source Output Mode<table><tr><td>0</td><td>Available Source from S0 to S175</td></tr><tr><td>1</td><td>Available Source from S8 to S167</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
A[7:0]= FFh (POR)<table>
<tr><th>Operating sequence</th><th>Parameter (in Hex)</th></tr>
<tr><td>Enable clock signal</td><td>80</td></tr>
<tr><td>Disable clock signal</td><td>01</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Enable clock signal
→ Enable Analog</td><td>C0</td></tr>
<tr><td>Disable Analog
→ Disable clock signal</td><td>03</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Enable clock signal
→ Load LUT with DISPLAY Mode 1
→ Disable clock signal</td><td>91</td></tr>
<tr><td>Enable clock signal
→ Load LUT with DISPLAY Mode 2
→ Disable clock signal</td><td>99</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Enable clock signal
→ Load temperature value
→ Load LUT with DISPLAY Mode 1
→ Disable clock signal</td><td>B1</td></tr>
<tr><td>Enable clock signal
→ Load temperature value
→ Load LUT with DISPLAY Mode 2
→ Disable clock signal</td><td>B9</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Enable clock signal
→ Enable Analog
→ Display with DISPLAY Mode 1
→ Disable Analog
→ Disable OSC</td><td>C7</td></tr>
<tr><td>Enable clock signal
→ Enable Analog
→ Display with DISPLAY Mode 2
→ Disable Analog
→Disable OSC</td><td>CF</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Enable clock signal
→Enable Analog
→ Load temperature value
→ DISPLAY with DISPLAY Mode 1
→ Disable Analog
→ Disable OSC</td><td>F7</td></tr>
<tr><td>Enable clock signal
→Enable Analog
→ Load temperature value
→ DISPLAY with DISPLAY Mode 2
→ Disable Analog
→ Disable OSC</td><td>FF</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM (Black White) / RAM 0x24</td><td>After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly

For Write pixel:
Content of Write RAM(BW) = 1
For Black pixel:
Content of Write RAM(BW) = 0</td></tr>
</table>



Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Ch	-0.3	48h	-1.8
10h	-0.4	4Ch	-1.9
14h	-0.5	50h	-2
18h	-0.6	54h	-2.1
1Ch	-0.7	58h	-2.2
20h	-0.8	5Ch	-2.3
24h	-0.9	60h	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
30h	-1.2	6Ch	-2.7
34h	-1.3	70h	-2.8
38h	-1.4	74h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
1	1		K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0		
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A_5	A_4	0	0	A_1	A_0		

0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1680 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0 Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1
0	1		A_7	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	0	0	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		

0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		

0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A_1	A_0		

0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[7:6]	Select VBD as
00	GS Transition, Defined in A[2] and A[1:0]
01	Fix Level, Defined in A[5:4]
10	VCOM
11[POR]	HiZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00	VSS
01	VSH1
10	VSL
11	VSH2

A[2] GS Transition control

A[2]	GS Transition control
0	Follow LUT (Output VCOM @ RED)
1	Follow LUT

A [1:0] GS Transition setting for VBD

A[1:0]	VBD Transition
00	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end A[7:0]= 02h [POR] 22h Normal. 07h Source output level keep previous output before power off
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A_0		

0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		

<table>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Set Ram Y- address Start / End position</td><td rowspan="5">Specify the start/end positions of the window address in the Y direction by an address unit for RAM

A[8:0]: YSA[8:0], YStart, POR = 000h
B[8:0]: YEA[8:0], YEnd, POR = 127h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_8</td></tr>
<tr><td>0</td><td>0</td><td>46</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td rowspan="2">Auto Write RED RAM for Regular Pattern</td><td rowspan="2">Auto Write RED RAM for Regular Pattern
A[7:0] = 00h [POR]

A[7]: The 1st step value, POR = 0
A[6:4]: Step Height, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>296</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>176</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>NA</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>47</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]

A[7]: The 1st step value, POR = 0
A[6:4]: Step Height, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>296</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>176</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>NA</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
During operation, BUSY pad will output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="2">Set RAM X address counter</td><td rowspan="2">Make initial settings for the RAM X address in the address counter (AC)
A[5:0]: 00h [POR].</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td rowspan="3">Set RAM Y address counter</td><td rowspan="3">Make initial settings for the RAM Y address in the address counter (AC)
A[8:0]: 000h [POR].</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>0</td><td>7F</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>NOP</td><td>This command is an empty command; it does not have any effect on the display module.
However it can be used to terminate Frame Memory Write or Read Commands.</td></tr>
</table>

8.Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
T update	Image update time	at 25 °C		3	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

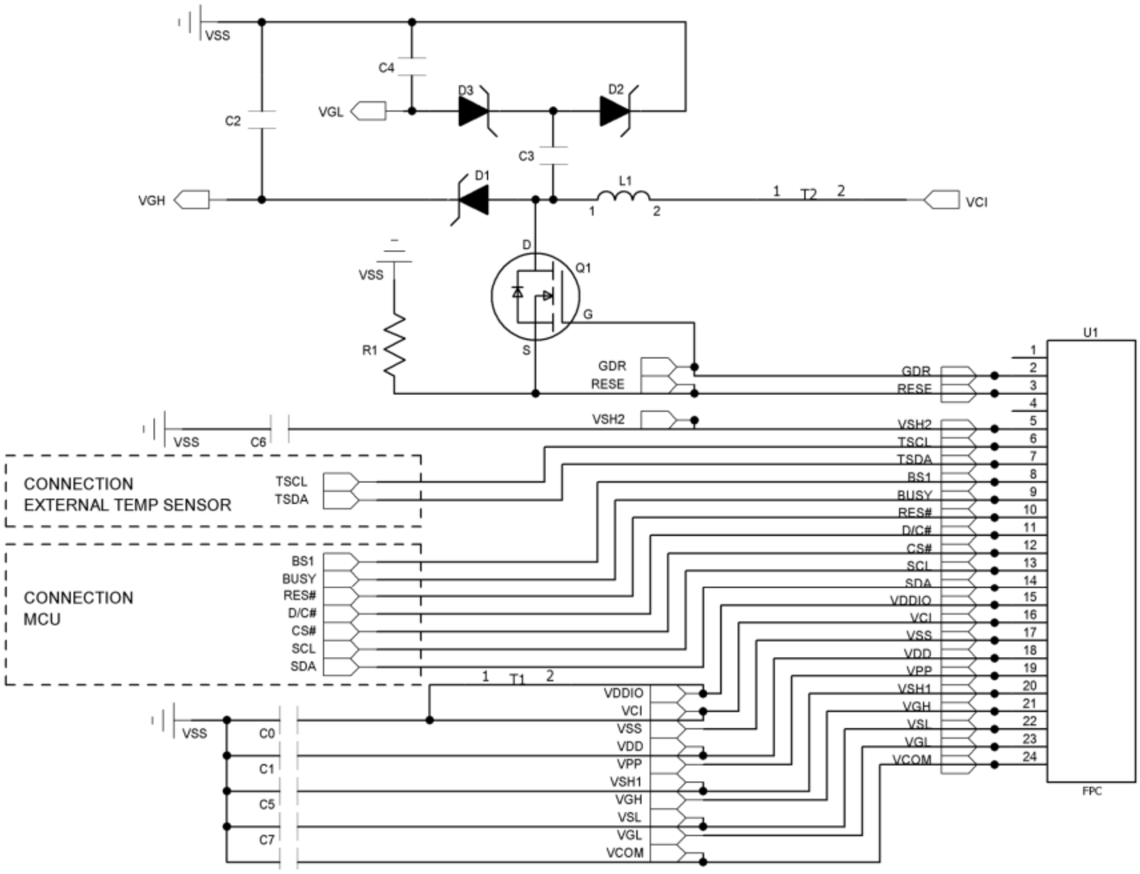
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10.Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40° C，RH=35%，240h
4	Low-Temperature Operation	T=0° C，240h
5	High-Temperature, High-Humidity Operation	T=40° C，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50° C，RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25° C 30min]→[+60° C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

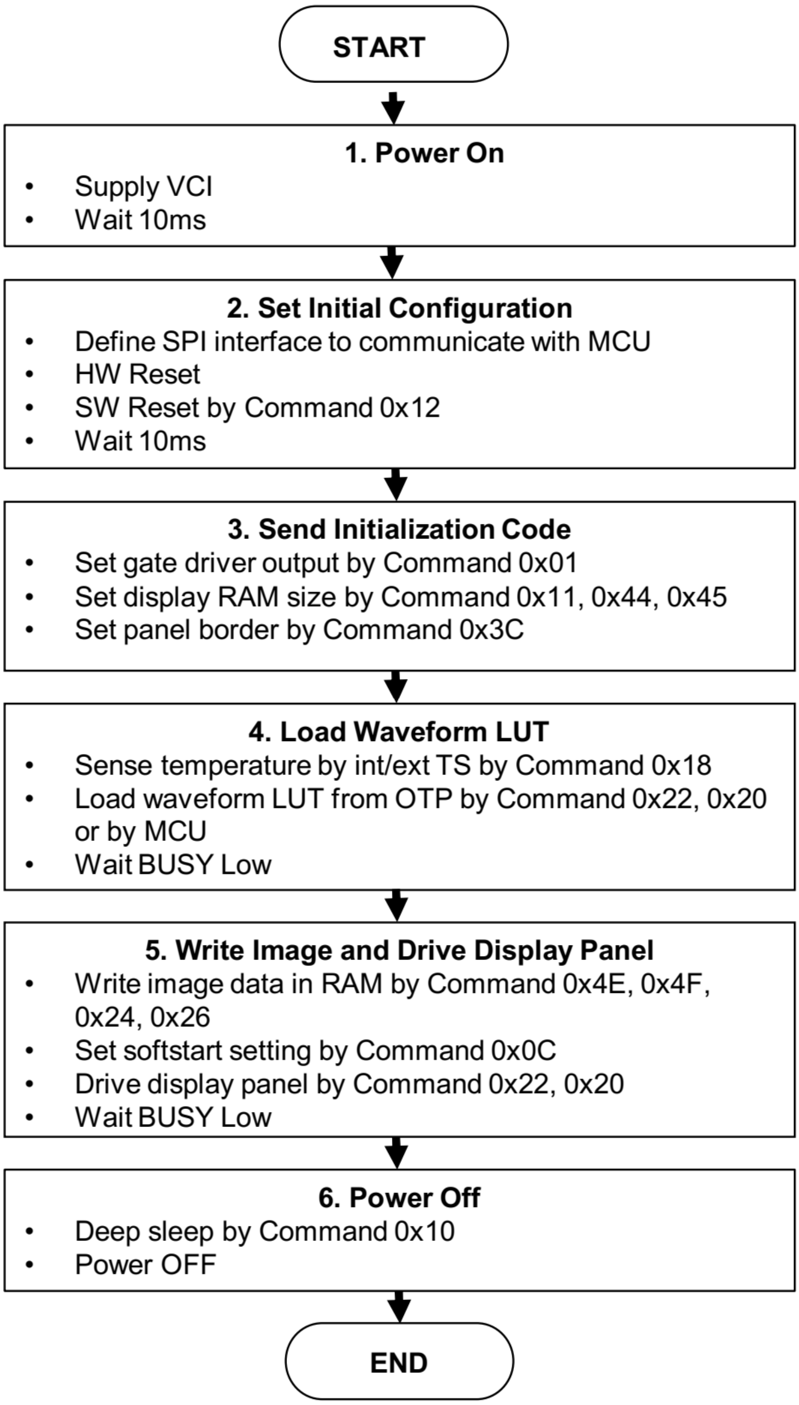
11. Typical Application Circuit with SPI Interface



Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	0.47uF, 1uF	0603/0805; X7R; Voltage Rating : 25V Note: Effective capacitance > 0.25uF @ 18V DC bias
R1	2.2 ohm	0402, 0603, 0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

12. Typical Operating Sequence

12.1 Normal Operation Flow



1. Power On

- Supply VCI
- Wait 10ms

2. Set Initial Configuration

- Define SPI interface to communicate with MCU
- HW Reset
- SW Reset by Command 0x12
- Wait 10ms

3. Send Initialization Code

- Set gate driver output by Command 0x01
- Set display RAM size by Command 0x11, 0x44, 0x45
- Set panel border by Command 0x3C

4. Load Waveform LUT

- Sense temperature by int/ext TS by Command 0x18
- Load waveform LUT from OTP by Command 0x22, 0x20 or by MCU
- Wait BUSY Low

5. Write Image and Drive Display Panel

- Write image data in RAM by Command 0x4E, 0x4F, 0x24, 0x26
- Set softstart setting by Command 0x0C
- Drive display panel by Command 0x22, 0x20
- Wait BUSY Low

6. Power Off

- Deep sleep by Command 0x10
- Power OFF

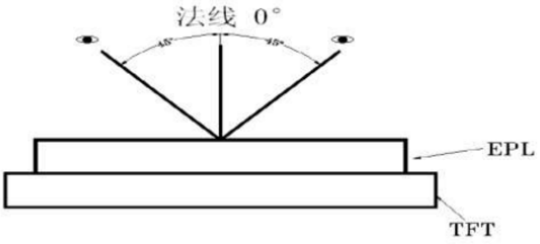
13. Part Number Definition

TBD

14. Inspection method and condition

14. 1 Inspection condition

Item	Condition
Illuminance	800~1500 lux
Temperature	22℃±3℃
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes

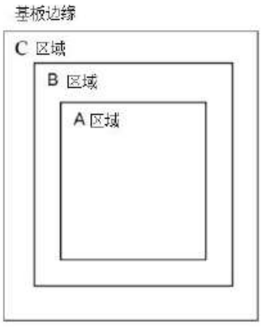


14. 2 Zone definition

A Zone： Active area

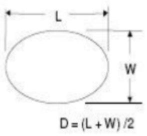
B Zone： Border zone

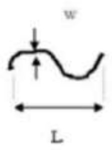
C Zone： From B zone edge to panel edge

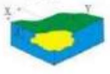
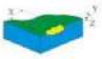
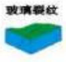
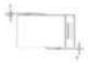
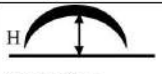


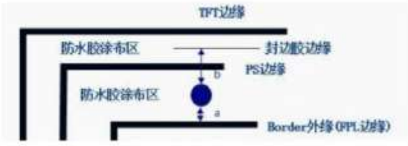
14. 3 General inspection standards for products

14.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter D=(L+W)/2 (L-length、W-width) Measuring method shown in the figure below 	The distance between the two spots should not be less than 10mm	7.5"-13.3"Module（Not include 7.5"）： D＞1mm N=0 0.5＜D≤0.8 N≤4 D≤0.5 Ignore 0.8＜D≤1 N≤2 4.2"-7.5"Module（Not include 4.2"）： D＞0.5 N=0 0.4＜D≤0.5 N≤2 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 Module below 4.2”： D＞0.5 N=0 0.4＜D≤0.5 N≤1 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 0.1mm＜D≤0.25 N≤3/cm²	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length，W-Width，(W/L)＜1/4 Judged by line， (W/L)≥1/4 Judged by dot 	The distance between the two lines should not be less than 5mm	7.5"-13.3"Module（Not include 7.5"）： L＞10mm,N=0 W＞0.8mm，N=0 5mm≤L≤10mm，0.5mm≤W≤0.8mm N≤2 L≤5mm，W≤0.5mm Ignore 4.2"-7.5"Module（Not include 4.2"）： L＞8mm,N=0 W＞0.2mm，N=0 2mm≤L≤8mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore Module below 4.2"： L＞5mm,N=0 W＞0.2mm，N=0 2mm≤L≤5mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel  	Chipping at the edge： Module over 7.5”（Include 7.5”）： X≤ 6mm,Y≤1mm Z≤T N=3 Allowed Module below 7.5”(Not include 7.5”)： X≤ 3mm,Y≤1mm Z≤T N=3 Allowed Chipping on the corner： IC sideX≤2mm Y≤2mm, Non-IC sideX≤1mm Y≤1mm . Allowed Note： Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes、 Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes、 Film gauge	MIN
	Burr edge		No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel	 Curl height	Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film	 	1 .Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed		
			Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm , allowed No exposure of wiring, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
EC defect	Adhesive effect	 	1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、Single silver dot dispensing amount ≥1mm, allowed 2、One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring	 	FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
	FPC golden finger		The height of burr edge of TCP punching surface ≧ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm，W≤0.5mm，N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

Front lighting	Evenly under visual inspection	Check by eyes	MIN
Structure, specification	The structure meets the corresponding design requirements; Product size, thickness and components installing position meet the requirements of the drawing.		

15. Packaging

TBD