



Specification for TFT

AFR480480A0R-2.76INTM-C-I

Revision V1.0



A	Orient Display
FR	TFT Type
480480	Resolution 480 x 480
A0R	Serial A0, Round
2.76	2.76", Module Dimension 87.73*89.73*3.39 mm
I	IPS Display
N	Top: -20~+70°C; Tstr: -30~+80°C
T	Transmissive
M	Medium Brightness, 500cd/m2
C	Capacitive Touch Panel
I	MIPI interface
/	ST7701S OR COMPATIBLE



Revision History

[illegible]

Contents

1. Basic Specifications	5
1.1 TFT Features	5
1.2 CTP Features	5
1.3 Mechanical Information	6
2. Block Diagram	6
3. Outline dimension	7
4. Input terminal Pin Assignment	8
4.1 TFT PIN Define	8
4.2 CTP PIN Define	9
5. LCD Optical Characteristics	10
5.1 Optical specification	10
6. Electrical Characteristics	13
6.1 Absolute Maximum Rating	13
6.2 DC Electrical Characteristics	13
6.3 MIPI DC Electrical Characteristics	14
6.4 LED Backlight Characteristics	15
7. AC Characteristics	17
7.1 MIPI Interface Characteristics:	17
7.1.1 High Speed Mode	17
7.1.2 Low Power Mode	18
7.1.3 Bursts Mode	19
7.2 Reset timing	21
8. CTP Specification	22
8.1 Electrical Characteristics	22
8.1.1 Absolute Maximum Rating	22
8.1.2 DC Electrical Characteristics (Ta=25°C)	22
8.2 AC Electrical Characteristics	23
8.3 SYSTEM MANAGEMENT	24
8.3.1 Power Down	24
8.3.2 Reset	24
8.3.3 Power On/Off Sequence	24
9. LCD Module Out-Going Quality Level	25
9.1 VISUAL & FUNCTION INSPECTION STANDARD	25
9.1.1 Inspection conditions	25
9.1.2 Definition	25
9.1.3 Sampling Plan	26
9.1.4 Criteria (Visual)	27
10. Reliability Test Result	33

11. Cautions and Handling Precautions.....33
 11.1 Handling and Operating the Module33
 11.2 Storage and Transportation.....34
12. Packing34

1.Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses a amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, capacitance touch panel, back-light unit. The resolution of a 2.76" TFT-LCD contains 480 x 480 pixels, and can display up to 16.7M colors.

1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	70.13(H)*70.13(V) (2.76 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	16.7M	colors	
Number of pixels	480(RGB)*480	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.1461(H)*0.1461(V)	mm	
Viewing angle	ALL	o'clock	
Controller IC	ST7701S	-	
LCM Interface	2-lane MIPI	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	
Touch and LCM Bonding techn	Optical bonding	-	

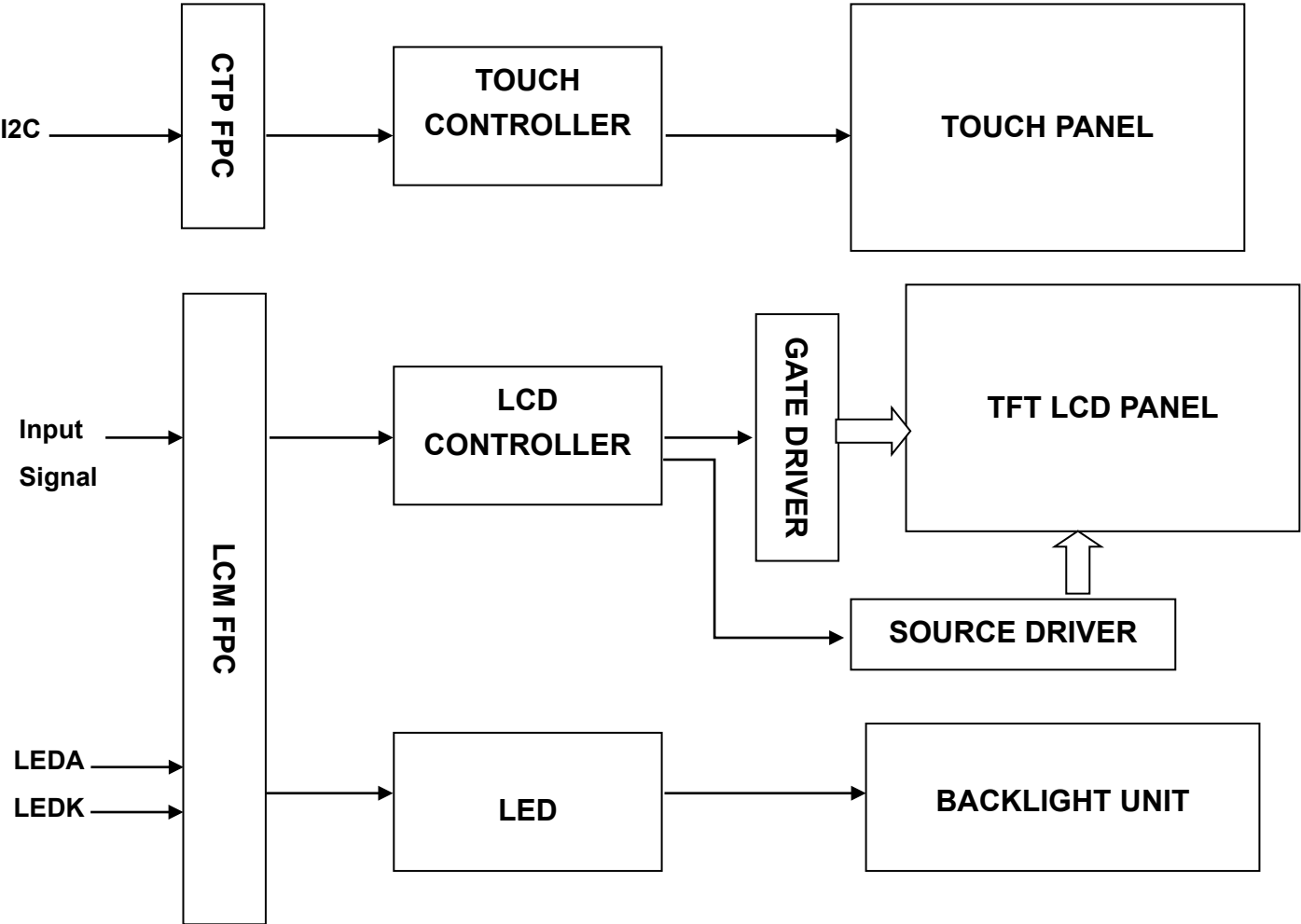
1.2 CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	480(H)*480(V)	-	
Structure	G+F+F	-	
Controller IC	ST1633i	-	
Interface	I2C	-	
Slave Address	0x70	-	
Touch mode	Multi-Touch	-	
Logic level	3.3		

1.3 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	87.73	-	mm	
	Vertical(V)	-	89.73	-	mm	
	Depth(D)	-	3.39	-	mm	
Weight		-	34	-	g	

2. Block Diagram



[illegible]

4. Input terminal Pin Assignment

4.1 TFT PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	--	--
2	LEDK	Cathode pin of backlight.	P
3	NC	--	--
4	LEDA	Anode pin of backlight.	P
5	NC	--	--
6	VDD/VCI	Supply Voltage (3.3V).	P
7	IOVCC	I/O power supply voltage.	P
8	TE	-Tearing effect output Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground.	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
12	MIPI_D1N		I/O
13	GND	Ground.	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-).	I
15	MIPI_CLN		I
16	GND	Ground.	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
18	MIPI_D0N		I/O
19	GND	Ground.	P
20	GND	Ground.	P

4.2 CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	NC	No Connection	
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

5. LCD Optical Characteristics

5.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	700	1000	--		*(1)(2))
Response time	Rising	T_{R+T_F}		--	35	40	msec	*(1)(3))
	Falling							
Color Gamut		S(%)		55	59	--	%	*
Color Filter Chromaticity	White	W_X		0.237	0.277	0.317		CA-310 Test
		W_Y		0.238	0.278	0.318		
	Red	R_X		0.572	0.612	0.652		
		R_Y		0.291	0.331	0.371		
	Green	G_X		0.266	0.306	0.346		
		G_Y		0.511	0.551	0.591		
	Blue	B_X	0.109	0.149	0.189			
		B_Y	0.015	0.055	0.095			
Viewing angle	Hor.	Θ_L	CR>10	80	85	--		*(1)(4))
		Θ_R		80	85	--		
	Ver.	Θ_U		80	85	--		
		Θ_D		80	85	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

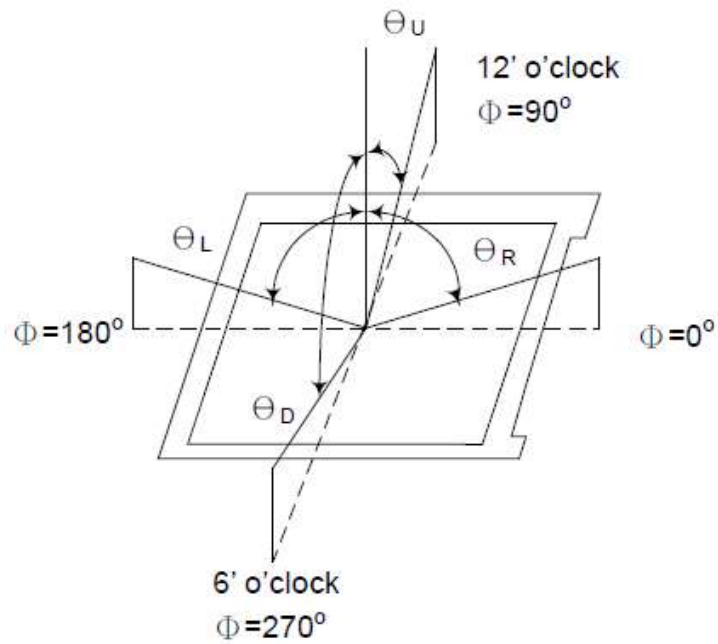
Ambient temperature : $25 \pm 2^\circ\text{C}$

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

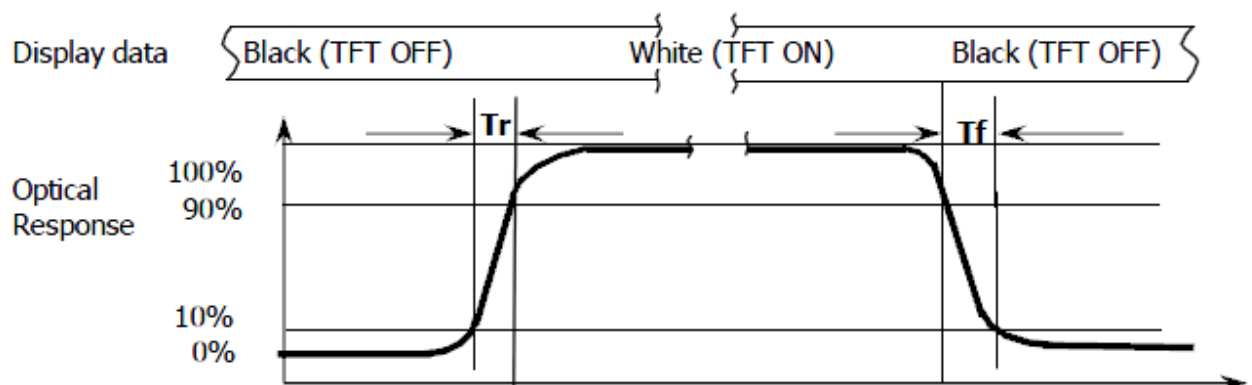
Note (1): Definition of Viewing Angle :



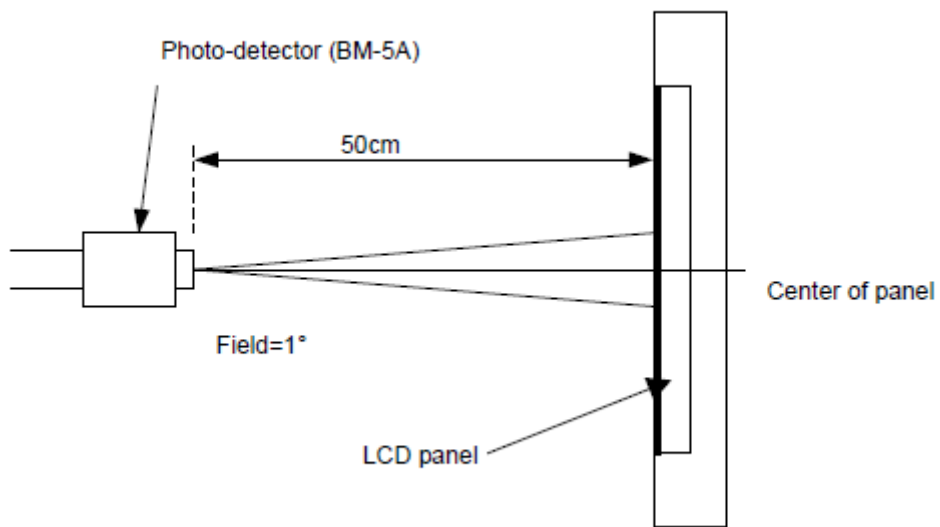
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



6. Electrical Characteristics

6.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.6	V	Note1
Digital Interface Supply	IOVCC	-0.3	4.6	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily,

the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values

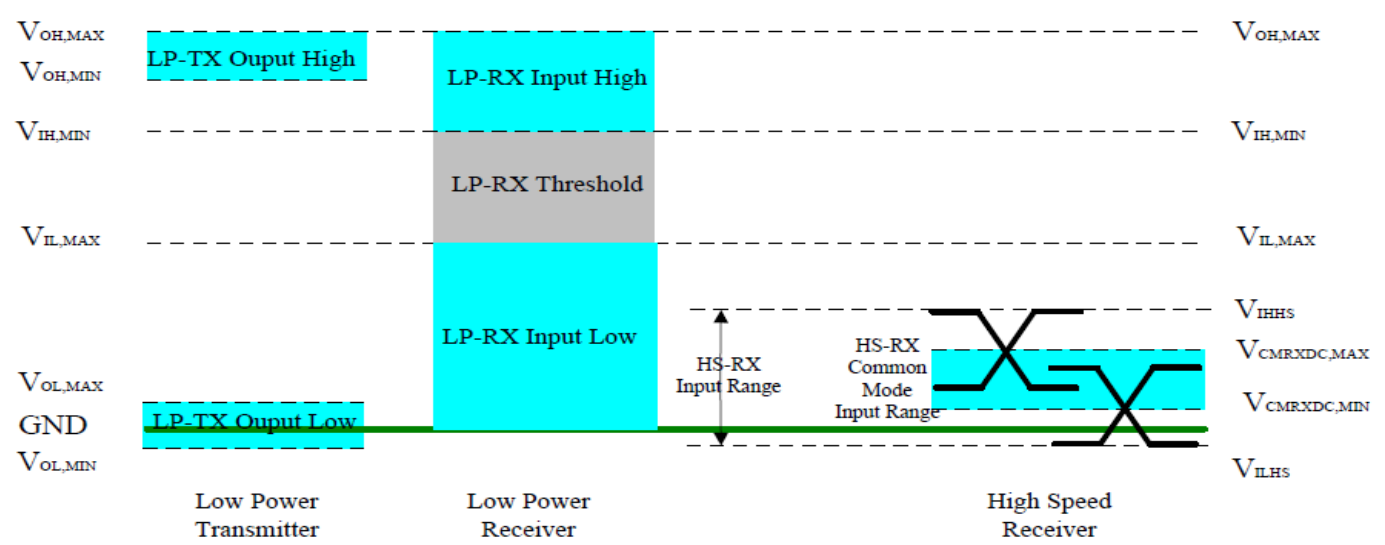
exceeding which the product may be physically damaged. Be sure to use the product within the range

of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital interface supply	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	ICC	--	16	32	mA	
Differential Input High Threshold Voltage	VIT+	--	0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-	-50	0	--	mV	
Single-ended Receiver Input Operation Voltage Range	VIR	0.5	--	1.2	V	

6.3 MIPI DC Electrical Characteristics



Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V _{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V _{ILHS}	-40	-	-	mV
Single-ended input high voltage	V _{IHHS}	-	-	460	mV
Common-mode voltage	V _{CMRXDC}	70	-	330	mV
Differential input impedance	Z _{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V _I	-50	-	1350	mV
Logic 0 input threshold	V _{IL}	0-	-	550	mV
Logic 1 input threshold	V _{IH}	880	-	1350	mV
Output low level	V _{OL}	-50	-	50	mV
Output high level	V _{OH}	1.1	1.2	1.3	V

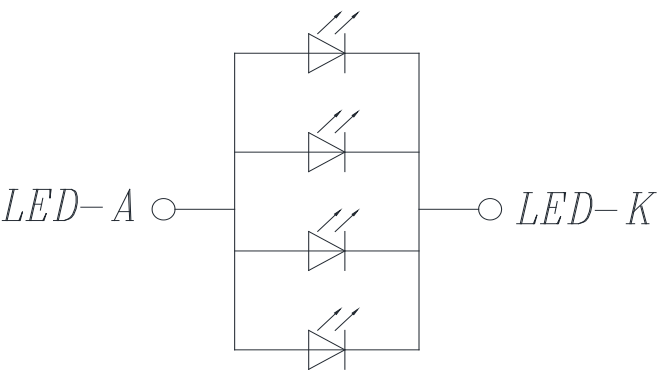
6.4 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	80	--	mA	
Forward Voltage	V_F	5.4	--	6.6	V	
LCM Luminance	LV	450	500	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

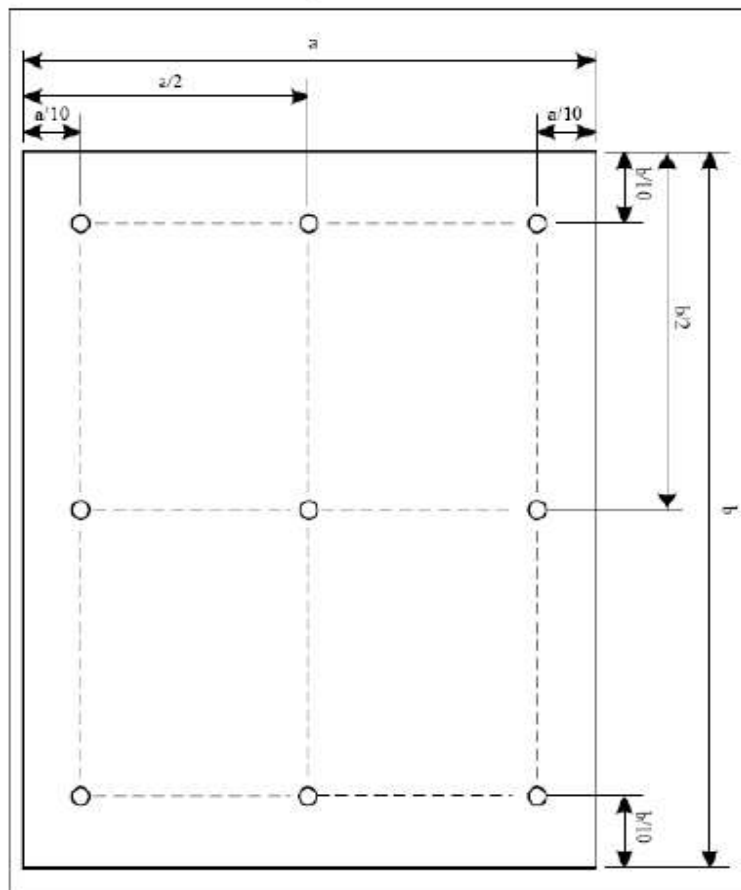
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:
Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. AC Characteristics

7.1 MIPI Interface Characteristics:

7.1.1 High Speed Mode

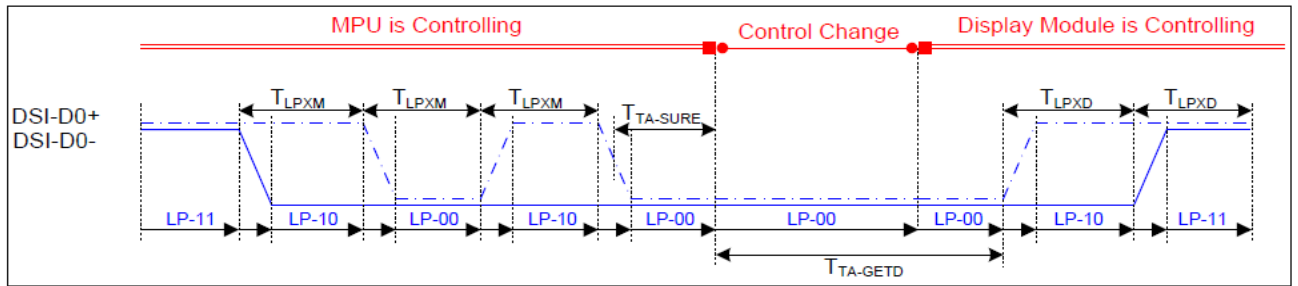


*DSI clock channel timing

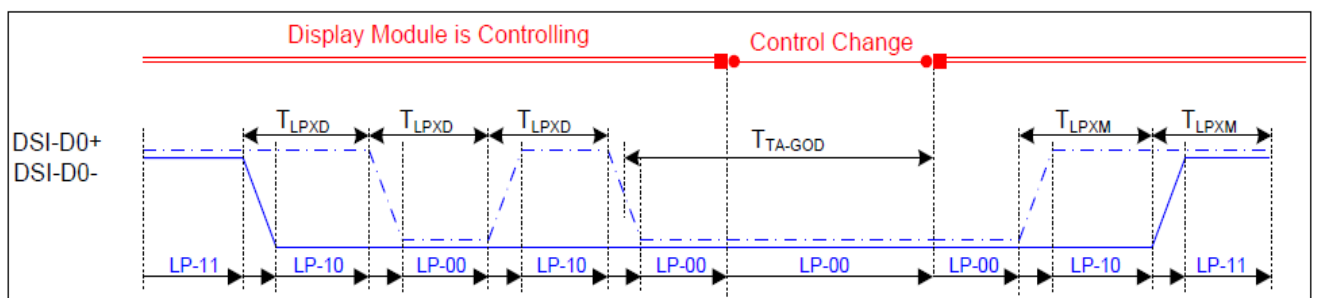
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	UI	

* Mipi Interface-High SpeedMode Timing Characteristics

7.1.2 Low Power Mode



* Bus Turnaround (BTA) from display module to MPU Timing

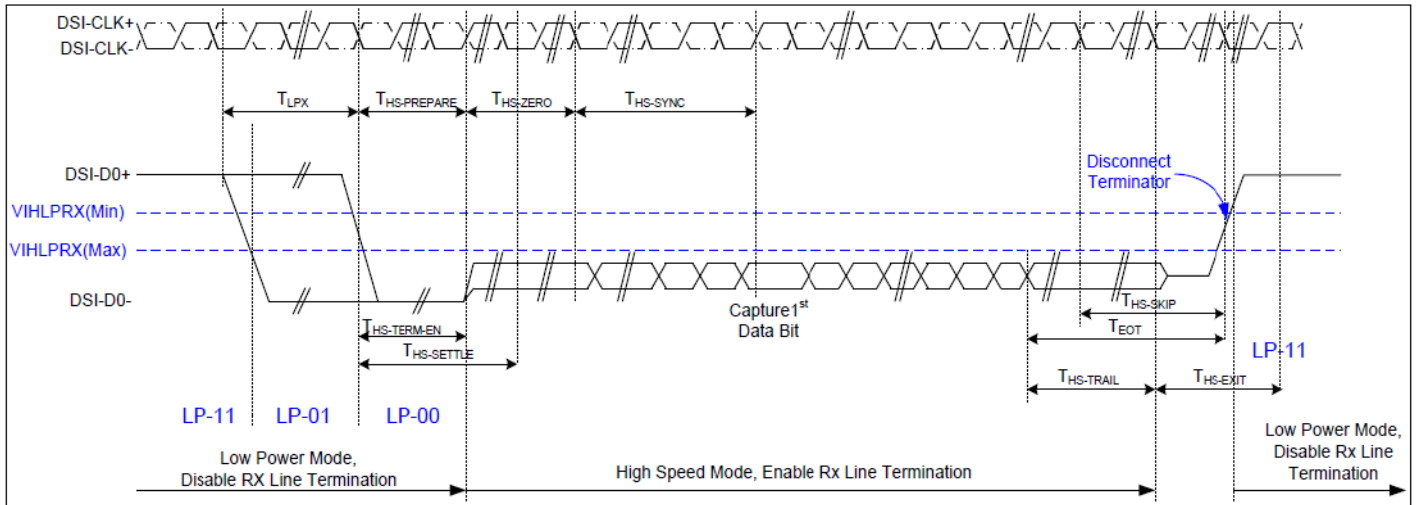


*Bus Turnaround (BTA) from MPU to display module Timing

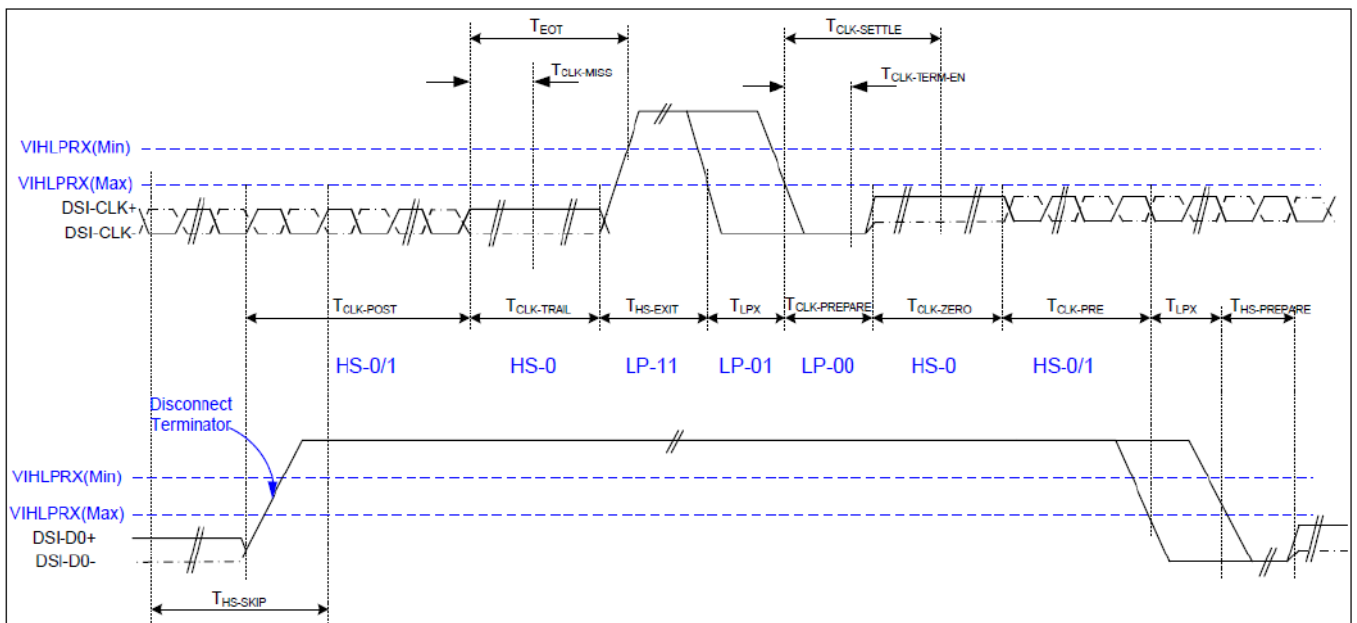
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

*Mipi Interface Low Power Mode Timing Characteristics

7.1.3 Bursts Mode



***Data lanes-Low Power Mode to/from High Speed Mode Timing**



***Clock lanes- High Speed Mode to/from Low Power Mode Timing**

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+8 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

7.2 Reset timing

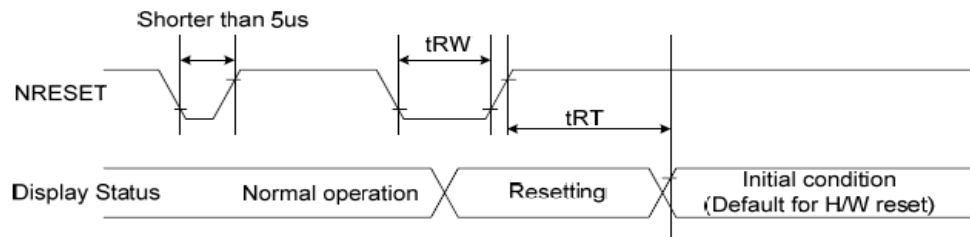


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5) 120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

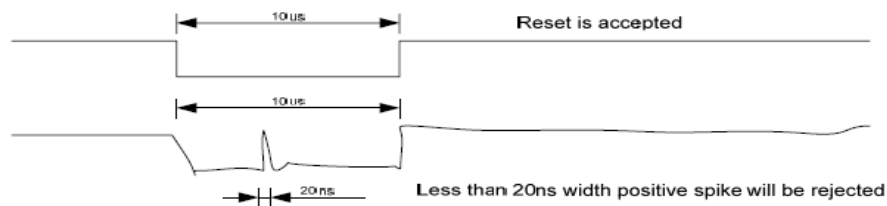


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	6	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the

device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended.

Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

8.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, VDD=3.3V, VDDIO=1.8V or VDDIO=VDD)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VDD	2.7	3.3	3.6	V	
Normal mode operating current	--	16.1	24	mA	
Green mode operating current	--	8.1	12.2	mA	
Power Down Current	--	--	20	uA	
Digital Input low voltage/VIL	--	--	0.15*VDD	V	
Digital Input high voltage/VIH	0.85*VDD	--	--	V	

8.2 AC Electrical Characteristics

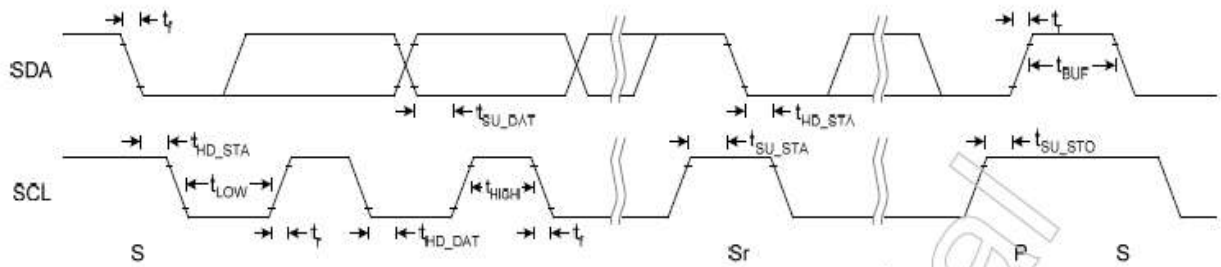


Figure 5-1 I2C Fast Mode Timing

Table 5-3 I2C Fast Mode Timing Characteristic

Conditions: VDD = 3.3V, GND = 0V, T_A = 25°C

Symbol	Parameter	Rating			Unit
		Min.	Typ	Max.	
f _{SCL}	SCL clock frequency	0	-	400	kHz
t _{LOW}	Low period of the SCL clock	1.3	-	-	μs
t _{HIGH}	High period of the SCL clock	0.6	-	-	μs
t _f	Signal falling time	-	-	300	ns
t _r	Signal rising time	-	-	300	ns
t _{SU_STA}	Set up time for a repeated START condition	0.6	-	-	μs
t _{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	μs
t _{SU_DAT}	Data set up time	100	-	-	ns
t _{HD_DAT}	Data hold time	0	-	0.9	μs
t _{SU_STO}	Set up time for STOP condition	0.6	-	-	μs
t _{BUF}	Bus free time between a STOP and START condition	1.3	-	-	μs
C _b	Capacitive load for each bus line	-	-	400	pF

8.3 SYSTEM MANAGEMENT

8.3.1 Power Down

In power down mode, all of the clocks of ST1633i are stopped. The way to exit power down mode is by a hardware reset or I2C.

8.3.2 Reset

Master can reset ST1633i through RESET pin. RESET pin is low active and needs hold low for 1us to take effect.

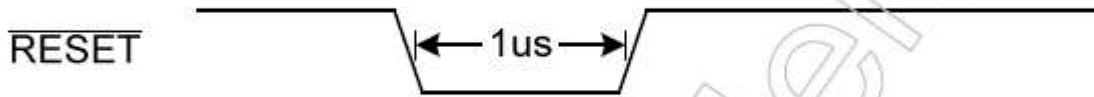


Figure 3-1 $\overline{\text{RESET}}$ Pin Low Pulse Width

8.3.3 Power On/Off Sequence

RESET pin should be held low before power on and power off. During power on, after both VDD and IOVDD reach normal voltage, RESET pin needs to be held low for 5ms to ensure internal block stable. Note: IOVDD and VDD had connected together.

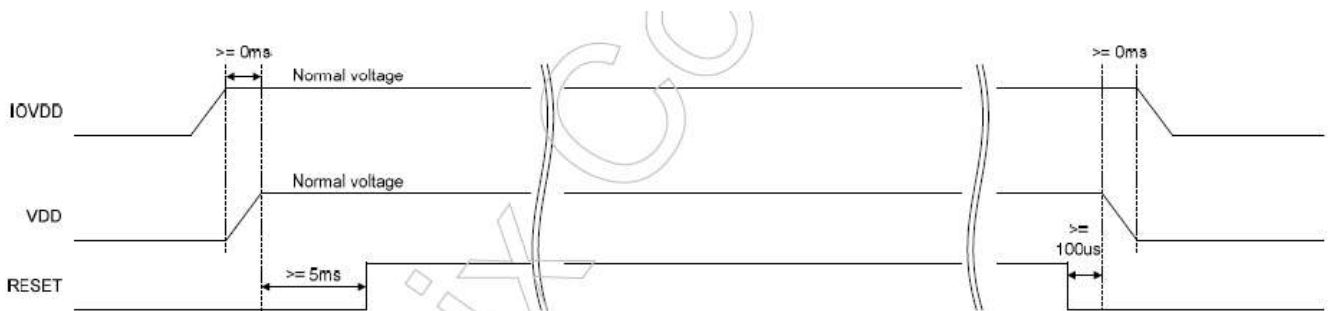


Figure 3-2 Power On/Off Sequence

9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

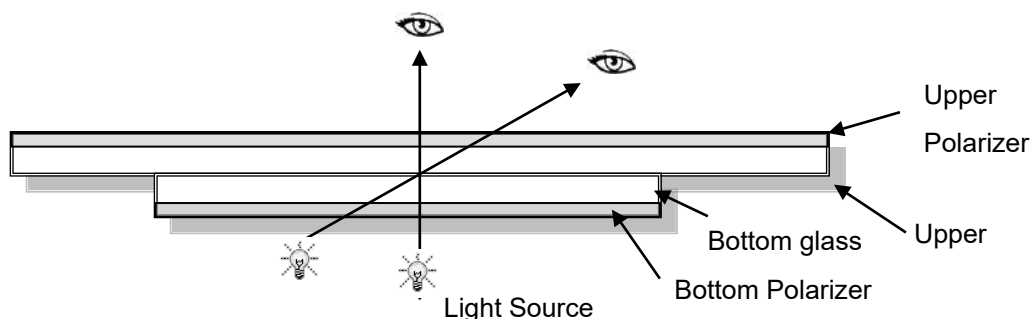
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

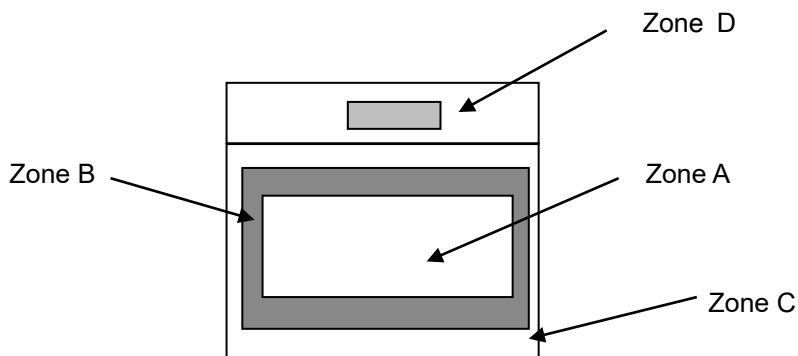
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



9.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

9.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

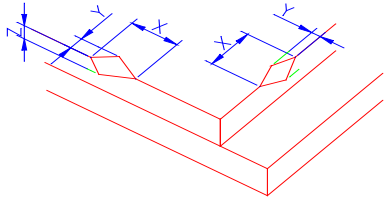
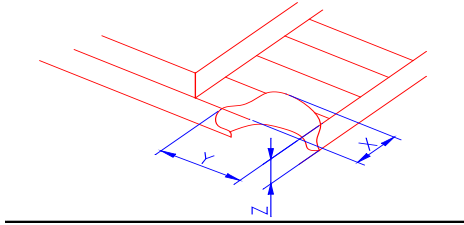
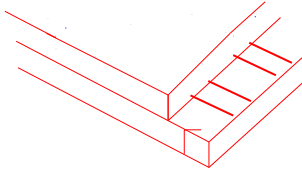
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

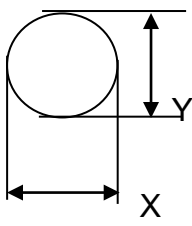
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

9.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

2.0

Spot defect



$\Phi=(X+Y)/2$

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 6\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 6\text{mm}$)		
$\Phi > 0.4$	0		

② Dim spot (light leakage、dent、dark spot, etc)

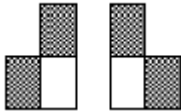
Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 6\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 6\text{mm}$)		
$\Phi > 0.4$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.5$	2(distance $\geq 6\text{mm}$)		
$\Phi > 0.5$	0		

④ Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.4$	3(distance $\geq 6\text{mm}$)		
$\Phi > 0.4$	0		

3.0	LCD Pixel defect	<table> <tr> <th>Item</th><th>Zone A</th><th>Acceptable Qty</th></tr> <tr> <td rowspan="3">Bright dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td rowspan="3">Dark dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>Distance</td><td> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td>5mm</td></tr> <tr> <td colspan="2">Total bright and dark dot</td><td>$N \leq 4$</td></tr> </table> Note: A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture:   2 dot adjacent 2 dot adjacent   2 dot adjacent (vertical) 2 dot adjacent (slant)	Item	Zone A	Acceptable Qty	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qty																							
Bright dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Dark dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	Width(mm)	Length(m m)	Acceptable Qty			
				A	B	C	
		$\Phi \leq 0.03$	Ignore	Ignore			Ignore
		$0.03 < W \leq 0.04$	$L \leq 3.0$	$N \leq 2$			
		$0.04 < W \leq 0.05$	$L \leq 2.0$	$N \leq 1$			
		$W > 0.05$	Define as spot defect				
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite					
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.					
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.					

8.0	CTP Related	CTP Cover sensor accidented black/white spot	Size Φ (mm)	Acceptable Qty			
				A	B	C	
			$\Phi \leq 0.1$	Ignore		Ignore	
			$0.1 < \Phi \leq 0.2$	3 (distance ≥ 6 mm)			
			$0.20 < \Phi \leq 0.25$	2 (distance ≥ 6 mm)			
			$\Phi > 0.25$	0			
		CTP Cover scratch					
			Width(mm)	Ignore(mm)	Acceptable Qty		
					A	B	C
			$\Phi \leq 0.03$	Ignore	Ignore		
	$0.03 < W \leq 0.04$		$L \leq 3.0$	$N \leq 2$			
$0.04 < W \leq 0.05$	$L \leq 2.0$		$N \leq 1$				
$0.05 < W$	Define as spot defect						

		CTP Cover Pinhole/ Lack of ink <table><tr><th> Zone Size (mm) </th><th>Acceptable Qty</th></tr><tr><td></td><th>C</th></tr><tr><td>$\Phi \leq 0.1$</td><td>Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.25$</td><td>3(distance $\geq 6\text{mm}$)</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td>2(distance $\geq 6\text{mm}$)</td></tr><tr><td>$\Phi > 0.3$</td><td>0</td></tr></table>	Zone Size (mm)	Acceptable Qty		C	$\Phi \leq 0.1$	Ignore	$0.1 < \Phi \leq 0.25$	3(distance $\geq 6\text{mm}$)	$0.25 < \Phi \leq 0.3$	2(distance $\geq 6\text{mm}$)	$\Phi > 0.3$	0					
Zone Size (mm)	Acceptable Qty																		
	C																		
$\Phi \leq 0.1$	Ignore																		
$0.1 < \Phi \leq 0.25$	3(distance $\geq 6\text{mm}$)																		
$0.25 < \Phi \leq 0.3$	2(distance $\geq 6\text{mm}$)																		
$\Phi > 0.3$	0																		
	CTP Bonding bubble/ accident spot <table><tr><th>Size $\Phi(\text{mm})$</th><th colspan="2">Acceptable Qty</th></tr><tr><td></td><th>A</th><th>B</th></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td colspan="2">3(distance $\geq 6\text{mm}$)</td></tr><tr><td>$0.2 < \Phi \leq 0.25$</td><td colspan="2">2(distance $\geq 6\text{mm}$)</td></tr><tr><td>$\Phi > 0.25$</td><td colspan="2">0</td></tr></table>	Size $\Phi(\text{mm})$	Acceptable Qty			A	B	$\Phi \leq 0.1$	Ignore		$0.1 < \Phi \leq 0.2$	3(distance $\geq 6\text{mm}$)		$0.2 < \Phi \leq 0.25$	2(distance $\geq 6\text{mm}$)		$\Phi > 0.25$	0	
Size $\Phi(\text{mm})$	Acceptable Qty																		
	A	B																	
$\Phi \leq 0.1$	Ignore																		
$0.1 < \Phi \leq 0.2$	3(distance $\geq 6\text{mm}$)																		
$0.2 < \Phi \leq 0.25$	2(distance $\geq 6\text{mm}$)																		
$\Phi > 0.25$	0																		
	Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																	
	CTP cover broken X : length Y : width Z : height <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.5\text{mm}$</td><td>$Y \leq 0.5\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$												
X	Y	Z																	
$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																	
	CTP cover broken X : length Y : width Z : height <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.3\text{mm}$</td><td>$Y \leq 0.3\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$												
X	Y	Z																	
$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$																	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

10. Reliability Test Result

Remark:

Item	Condition	Inspection after test
High Temperature Operating	70°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10°C,30 min ↔ +60°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (ESD test: 150C, 250C, 300V, 300V)	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X Y Z (6 hours for total) (Package	
Box Drop Test	1 Corner 3 Edges 6 faces,80 _{cm} (MEDIUM BOX)	

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper

operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

11.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

12. Packing

----TBD-----