HIGH-VOLTAGE MIXED-SIGNAL IC

UC1697u

130 x 130RGB C-STN LCD Controller-Driver
w/ 16-bit per RGB On-Chip SRAM
Optimized for VSTN (Video-CSTN)

Preliminary Specifications
Revision 0.1

March 21, 2006

ULTRACHIP

The Coolest LCD Drive, Ever!!

TABLE OF CONTENT

UC1697u

Single-Chip, Ultra-Low Power
130COM x130RGB Matrix
Passive Color LCD Controller-Driver
with VSTN Support

INTRODUCTION

UC1697u is an advanced high-voltage mixed-signal CMOS IC, specially designed for the display needs of low power hand-held devices.

In addition to low power COM and SEG drivers, UC1697u contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation, and graphics data memory.

UC1697u employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and LRM (Line Rate Modulation) gray-shade modulation scheme to achieve well balanced shading, vivid colors, and natural-looking images while supporting very fast Liquid Crystal material for video applications.

With UC1697u, LCD makers can now achieve TFT-like image quality, support video applications while maintaining the same STN advantages in power consumption, unit cost, ease of customization and production flexibility.

MAIN APPLICATIONS

- Cellular Phones and other battery operated hand held devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 130x130 matrix C-STN LCD with comprehensive support for input format and color depth:
  12-bit RGB: 4K-color
  16-bit RGB: 64K-color
- Support video rate CSTN applications.
- Real time overlay function and window-write, window-skip functions to support flexible video applications such as OSD, dynamic service provider screen saver for cell phone and others.
- One ID pin (ID0) plus two programmable ID flags, totally 3 software-readable ID bits to support configurable vender identification.
- ID pin (ID1)-switched input data sets (D[0:7] or D[0,2,4,6,8,10,12,14]) for 8-bit mode.
- ID pin (ID2) switch-able 128x128 / 130x130 resolution selection. (However, the descriptions in this datasheet are based on 130 x 130)
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 3/4-wire, 4-wire serial bus (S8, S8uc) and 16-bit/8-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Low power consumption under all display patterns.
- No power consumption or image quality penalty when used with video rate CSTN
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable temperature compensation coefficients.
- Software programmable, self-configuring 10x charge pump.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Pad layouts support COG applications.
- V_{DD} (digital) range: 1.8V ~ 3.3V (Typ.)
  V_{DD} (analog) range: 2.6V ~ 3.3V (Typ.)
  LCD V_{OP} range: 6.4V ~ 16.5V
- Available MTP trimming supports precise LCD contrast matching.
- Available in gold bump dies:
- COM/SEG bump information
  Bump pitch: 31 μM
  Bump gap: 14 μM
  Bump surface: 2006 μM^2

ORDERING INFORMATION

GOLD BUMPED DIE

Part Number	MTP	Description
UC1697uGAB	Yes	Gold bumped die, with MTP function.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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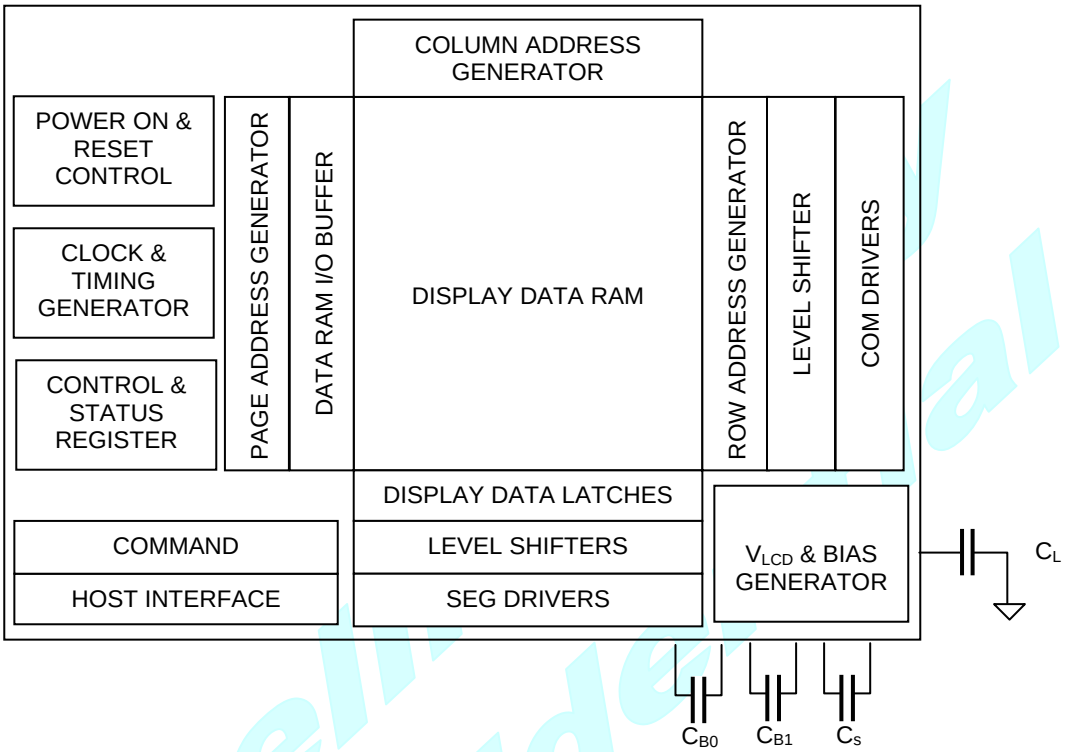
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	# of Pads	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	9 9 2	V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	12 12	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{S+} , V_{S-} V_{B1+} , V_{B1-} V_{B0+} , V_{B0-}	PWR	3, 3 6, 6 6, 6	LCD SEG driving voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. Connect a 150 ~ 220nF/25V capacitor between V_{S+} and V_{S-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCD-IN} $V_{LCD-OUT}$	PWR	2 2	High voltage LCD Power Supply. Connect these pins together. Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance under 30 Ω.

NOTE

- Recommended capacitor values:
  C_B: 2.2μF/2V or 300x LCD load capacitance, whichever is higher.
  C_L: 330nF(25V) is appropriate for most applications.
  C_S: 150 ~ 220nF / 5V.

<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and {DB15, DB13} by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>{DB15, DB13}</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/16-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/16-bit</td></tr>
<tr><td>01</td><td>0x</td><td>6800/8-bit</td></tr>
<tr><td>00</td><td>0x</td><td>8080/8-bit</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr>
</table></td></tr>
<tr><td>CS0
CS1</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[15:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1697u has built-in Power-ON reset and software reset commands, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID0</td><td>I</td><td>1</td><td>Used for production control.
Connect ID0 to V_{DD} for “H” or V_{SS} for “L”.
The wiring status of ID0 is available with PID[2:0] of <code>Get Status</code> command.</td></tr>
<tr><td>ID1</td><td>I</td><td>1</td><td>Select input data set for 8-bit mode.
ID1=0 : 8-bit input data are D[0,2,4,6,8,10,12,14]
ID1=1 : 8-bit input data are D[0:7]
The wiring status of ID1 is available with PID[2:0] of <code>Get Status</code> command.</td></tr>
<tr><td>ID2</td><td>I</td><td>1</td><td>Dimension option.
ID2 = 0 : 128 x 128
ID2 = 1 : 130 x 130
The wiring status of ID2 is available with PID[2:0] of <code>Get Status</code> command.
For clearness, all the descriptions in this datasheet are based on 130 x 130.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">DATA BUS</td></tr>
<tr><td>D0~D15</td><td>I/O</td><td>16</td><td>Bi-directional bus for parallel host interfaces.
In serial modes, connect DB[0] to SCK, DB[8] to SDA.
<table>
<tr><th></th><th>BM=1x
(16-bit)</th><th>BM=0x
(8-bit)
ID1=0</th><th>BM=0x
(8-bit)
ID1=1</th><th>BM=00
(S8/S8uc)
DB15=1</th></tr>
<tr><td>DB0</td><td>D0</td><td>D0/D8</td><td>D0/D8</td><td>SCK</td></tr>
<tr><td>DB1</td><td>D1</td><td>–</td><td>D1/D9</td><td>–</td></tr>
<tr><td>DB2</td><td>D2</td><td>D1/D9</td><td>D2/D10</td><td>–</td></tr>
<tr><td>DB3</td><td>D3</td><td>–</td><td>D3/D11</td><td>–</td></tr>
<tr><td>DB4</td><td>D4</td><td>D2/D10</td><td>D4/D12</td><td>–</td></tr>
<tr><td>DB5</td><td>D5</td><td>–</td><td>D5/D13</td><td>–</td></tr>
<tr><td>DB6</td><td>D6</td><td>D3/D11</td><td>D6/D14</td><td>–</td></tr>
<tr><td>DB7</td><td>D7</td><td>–</td><td>D7/D15</td><td>–</td></tr>
<tr><td>DB8</td><td>D8</td><td>D4/D12</td><td>–</td><td>SDA</td></tr>
<tr><td>DB9</td><td>D9</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB10</td><td>D10</td><td>D5/D13</td><td>–</td><td>–</td></tr>
<tr><td>DB11</td><td>D11</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB12</td><td>D12</td><td>D6/D14</td><td>–</td><td>–</td></tr>
<tr><td>DB13</td><td>D13</td><td>–</td><td>–</td><td>0:S8 / 1:S8uc</td></tr>
<tr><td>DB14</td><td>D14</td><td>D7/D15</td><td>–</td><td>–</td></tr>
<tr><td>DB15</td><td>D15</td><td>0</td><td>0</td><td>1</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
</table>

Name	Type	# of Pads	Description
			HIGH VOLTAGE LCD DRIVER OUTPUT
SEG1 ~ SEG390	HV	390	SEG (column) driver outputs. Support up to 130xRGB pixels. Leave unused SEG drivers open-circuit.
COM1 ~ COM130	HV	130	COM (row) driver outputs. Support up to 130 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 130, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 130] open-circuit.
			MISC. PINS
V_{DDX}	O	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus within the IC. These pads are provided to facilitate chip configurations in COG application. These pins should *NOT* be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV	2	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.
TST1 TST2	O	1 1	Test I/O pins. Leave these pins open during normal use.

NOTE:

Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~129 for COM and 0~389 for SEG.

RECOMMENDED COG LAYOUT

Note for V_{DD} and V_{SS} with COG:

The operation condition V_{DD}=1.8V (typical) must be satisfied under all operating conditions. With its video capability, UC1697u peak current (I_{DD}) can be up to ~15mA range during high speed data write to UC1697u's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD}, V_{SS} ITO trances in COG glass modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1697u contains registers which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, starting with a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (129– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The top FLTx2 and bottom FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	8	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	8	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	3	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 000b: 6 001b: 10 010b: 11 **011b: 12** 100b: 9
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.00%** 01b: -0.10% 10b: -0.15% 11b: -0.20%
PM	8	5CH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	7	00H	PM offset. PMO[6]=1: The effective PM value, PMV = PM - PMO[5:0] PMO[6]=0: The effective PM value, PMV = PM + PMO[5:0]
PC	4	EH	Power Control. PC[1:0]: 0xb: LCD: ⩽ 13nF **1xb: LCD:13~22nF** PC[3:2]: 00b: External V_{LCD} **11b:** Internal V_{LCD} (10x charge pump)
AC	4	1H	Address Control: AC[0]: WA: Automatic column/row Wrap Around (Default **1 : ON**) AC[1]: Auto-Increment order **0 : Column (CA) first** 1 : Row (RA) first AC[2]: RID: RA (row address) auto increment direction (**L : +1** H : -1) AC[3]: Window Program Mode **0 : Inside Mode:** Write to SRAM within the window defined by (WPC0,WPP0), (WPC1,WPP1) 1 : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0), (WPC1,WPP1)

Name	Bits	Default	Description
DC	5	18 H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray-shade Modulation mode. 0 : On/Off mode **1 : 32-shade Mode** DC[4]: Green Enhance Mode. *Only valid in 4K-color mode.* 0 : Enable. Allows an extra display bit for green color. **1 : Disable**
LC	10	090H	LCD Control: LC[0]: Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default **OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 20.4 Klps 01b: 24.8 Klps **10b: 30.0 Klps** 11b: 36.4 Klps Line Rate (for 8-color On/Off mode) 00b: 5.5 Klps 01b: 6.7 Klps **10b: 8.1 Klps** 11b: 9.0 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 64K color mode**. 5R-6G-5B (16-bit/RGB) when DC[4]=0: 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 64K color mode. 5R-6G-5B (16-bit/RGB) LC[9:8] : Partial Display Control **0xb: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 10b: Enabled Mux-Rate = CEN+1 11b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	5	1CH	N-Line Inversion: NIV[2:0]: 000b: 7 lines 001b: 9 lines 010b: 11 lines 011b: 15 lines **100b: 17 lines** 101b: 23 lines 110b: 29 lines 111b: 37 lines NIV[3]: 0b: no-XOR **1b: XOR** NIV[4]: 0b: Disable NIV **1b: Enable NIV**
CSF	3	0H	COM Scan Function CSF[0]: **0b: LRM sequence: AEBCD-AEBCD** 1b: LRM sequence: AEBCD-EBCDA CSF[1]: **0b:FRC Disable** 1b: FRC Enable CSF[2]: Shade-1 / Shade-30 option **0 : Dither directly on input data (SRAM Change)** 1 : PWM on SEG output stage

Name	Bits	Default	Description
CEN DST DEN	8 8 8	81H 00H 81H	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	8	00H	Window program starting column address. Value range: 0 ~129.
WPP0	8	00H	Window program starting row address. Value range: 0~129.
WPC1	8	81H	Window program ending column address. Value range: 0~129.
WPP1	8	81H	Window program ending row address. Value range: 0~129.
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : **Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	7	--	Multiple-Time Programming. For V_{LCD} fine tune.
MTPID	2	--	Multiple-Time Programming. For LCM manufacturer's configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC	2	N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

COMMAND TABLE

The following is a list of host commands supported by UC1697u

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A Product Code (5h)
				Ver	PMO[6:0]								
				Product Code			PID[2:0]			MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1xb
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1, or 2	N/A
	(Double-byte command)	0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
11	Set PMO	0	0	1 -	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set PMO[6:0]	0
12	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	5CH
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
13	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0xH
14	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
15	Set Fixed Lines	0 0	0 0	1 #	0 #	0 #	1 #	0 #	0 #	0 #	0 #	Set {FLT, FLB}	0
16	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
17	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
18	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
19	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
20	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
21	Set N-Line Inversion	0	0	1 -	1 -	0 -	0 #	1 #	0 #	0 #	0 #	Set NIV[4:0]	1CH
22	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
23	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
24	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
25	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
26	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
27	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(Double-byte command)	0	0	#	#	#	#	#	#	#	#		
28	Set LCD Bias Ratio	0	0	1	1	1	0	1	#	#	#	Set BR[2:0]	011b: 12
29	Set COM End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[7:0]	129
30	Set Partial Display Start	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[7:0]	0
31	Set Partial Display End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[7:0]	129
32	Set Window Program Starting Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with MTP Commands: Set WPC0	0
33	Set Window Program Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #	Set WPP0	0
34	Set Window Program Ending Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	0 #	Set WPC1	129
35	Set Window Program Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #	Set WPP1	129
36	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside
37	Set MTP Operation control	0 0	0 0	1 -	0 -	1 -	1 #	1 #	0 #	0 #	0 #	Set MTPC[4:0]	10H

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
38	Set MTP Write Mask	0 0 0	0 0 0	1 - -	0 # -	1 # -	1 # -	1 # -	0 # -	0 # #	1 # #	Set MTPM[6:0] MTPM1[1:0]		0
39	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
40	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
41	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
42	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A

NOTE:

- Other than commands listed above, all other bit patterns may result in undefined behavior.
- Command `Set PMO` is only available for non-MTP version UC1697u. This command has no meaning for the MTP version of UC1697u.
- The interpretation of commands (38)~(42) depends on the setting of register MTPC[3].
  - Commands (39)~(42) are shared with commands (32)~(35). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
  - MTPM and PMO are actually the same register and it can be modified by either command (38) or command (11). Only one of these two commands is valid at any time, as determined by MTPC[3].
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.
- Under 16-bit bus mode and CD=0, D[15:8] is ignored and only D[7:0] is used. As a result, the bus cycles for commands under 16-bit bus and 8-bit bus are the same, and double-byte commands still need two bus cycles under 16-bit bus mode.

  Example:

  8-bit bus mode:

  Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

  Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

  2nd D[7:0] = 1000 1011

  16-bit bus mode:

  Set PL[1:0] = 2'b11: D[15:0] = 0000 0000 0010 1011

  Set PM[7:0] = 8'h8b: 1st D[15:0] = 0000 0000 1000 0001

  2nd D[15:0] = 0000 0000 1000 1011

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

UC1697u will convert input RAM data to 16-bit of RGB data. Please refer to command *Set Color Mode* for detail of data-write sequence.

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Each RGB triplet is stored as 16-bit in the display RAM. Each 16-bit of RGB data takes 1 / 2 RAM read cycles for 16 / 8 – bit bus mode, respectively. The read out RGB data is *after-extension* for 64K color mode.

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
1st 8-bit Read								2nd 8-bit Read							

Write/Read Data Byte (commands (1) and (2)) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing commands `Set Row Address` and `Set Column Address`. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 129), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS & PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS
	0	1	Ver	PMO[6:0]						
	0	1	Product Code			PID[2:0]			MID[1:0]	

Status1 definitions:
- *GE*: Green Enhancing enable flag. Green Enhance Mode is disabled when GE = 1.
- *MX*: Status of register LC[1], mirror X.
- *MY*: Status of register LC[2], mirror Y.
- *WA:* Status of register AC[0]. Automatic column/row wrap around.
- *DE*: Display enable flag. DE=1 when display is enabled
- *WS*: MTP Operation succeeded
- *MD*: MTP Option (1 for MTP version, 0 for non-MTP version)
- *MS*: MTP action status

Status2 definitions:
- *Ver:* Version Code. 0 or 1.
- *PMO[6:0]:* PM offset value.

Status3 definitions:
- *Product Code*: 101b (5h)
- *PID[2:0]:* Provide access to ID pins connection status.
- *MID[1:0] :* LCM manufacturer's configuration.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~129**

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b = -0.00%/°C 01b = -0.10%/°C 10b = -0.15%/°C 11b = -0.20%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition:

0xb: LCD: ≤ 13nF **1xb: LCD: 13~22nF**

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages. Always make sure the IC is in a RESET state before changing PC[3:2] value. Avoid changing PC[3:2] setting when the display is enabled.

Pump control definition:

00b = External V_{LCD} **11b = Internal V_{LCD} (x10)**

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[2:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(Double-byte command)	0	0	APC register parameter							

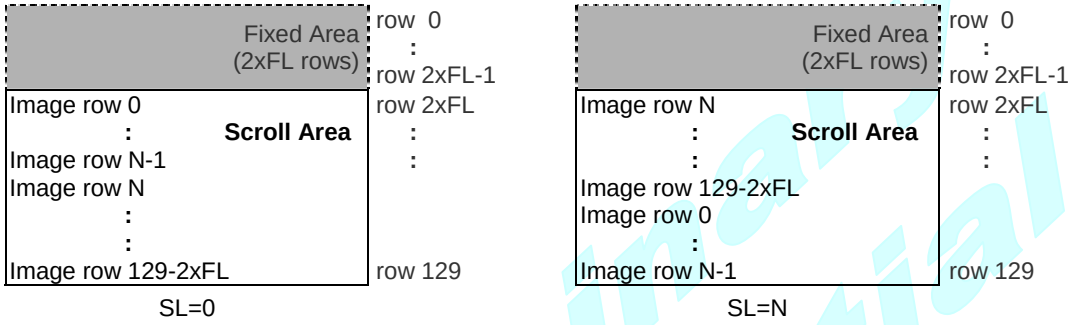
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	**0**	**1**	**0**	**1**	SL7	SL6	SL5	SL4

Set the number of lines for scroll area.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 129-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the `Set Fixed Lines` command.



(10) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address MSB RA [7:4]	0	0	**0**	**1**	**1**	**1**	RA7	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0~129**

(11) SET PMO CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set PMO[6:0] (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	-	*PMO[6:0]*						

This command is used to set the PMO register value for non-MTP version of UC1697u. For the related setting values, please refer to the `Set MTP Write Mask` command.

A typical application of this register is when a cell phone user is provided with a manual adjustment of LCD contrast, instead of calculating PM value manually. System programmers may use this register to fine tune V_{LCD} value directly.

(12) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD Voltage Setting* for more detail.

Effective range: **0 ~ 255**

(13) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to enable partial display function.

LC[9:8] : **0X**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
10b: Enable Partial Display, Mux-Rate = CEN+1
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(14) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

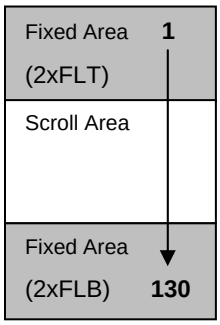
AC[2]: RID, row address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. For Window Program enabling (AC[3]=ON), see section *Command Description* (34) ~ (37) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[3] is.

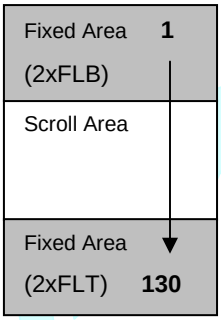
(15) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT, FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0



MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(16) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 87, 65, 44 and 33.

The following are line rates at Mux Rate = 88 ~ 130.

00b: 20.4 Klps 01b: 24.8 Klps **10b: 30.0 Klps** 11b: 36.4 Klps

In On/Off Mode

00b: 5.5 Klps 01b: 6.7 Klps **10b: 8.1 Klps** 11b: 9.0 Klps

(Klps: Kilo-Line-per-second)

(17) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(18) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

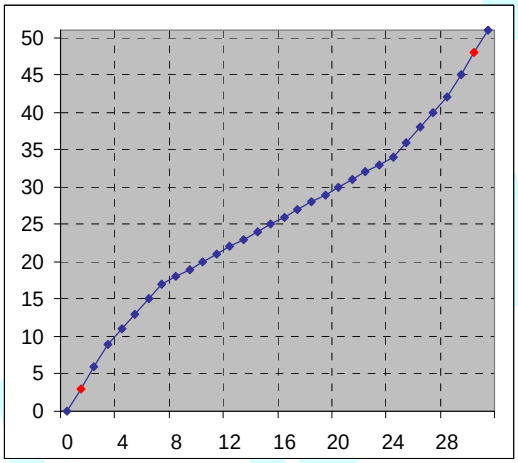
(19) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1697u will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1697u has two gray shade modulation modes: an On/Off mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] Green Enhance Mode. Refer to command `Set Color Mode` for more information.

0b: Green Enhancing Mode enabled **1b: Green Enhancing Mode disabled**

NOTE:

1. For red and blue colors, shades mapped to data 1 and 30 (shown as red points above) are achieved by special dithering. This will be solved when the PWM function is enabled.
2. Green shades are created by combining FRC and special dithering. Six of the shades (1, 2, 3, 59, 60, and 61) are created by special dithering. This will be solved when the PWM function is enabled. Data 62 and 63 are mapped to the same shade.
3. When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1697u for 5~10mS after setting DC[2] to 1.

(20) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] to control COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by the MY action. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 129-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

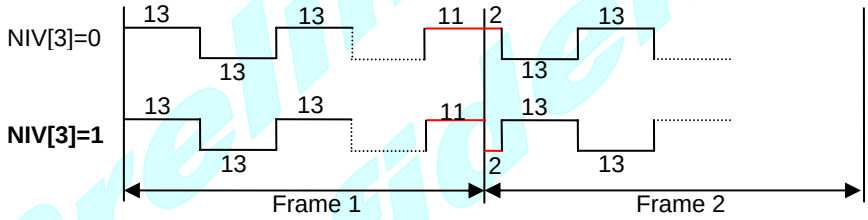
LC[0] controls whether soft icon sections (2xFLT, 2xFLB) are displayed during partial display mode.

(21) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line Inversion, NIV[4:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(Double-byte command)	0	0	-	-	-	NIV4	NIV3	NIV2	NIV1	NIV0

N-Line Inversion:

NIV[2:0]: 000b: 7 lines 001b: 9 lines 010b: 11 lines 011b: 15 lines
100b: 17 lines 101b: 23 lines 110b: 29 lines 111b: 37 lines
NIV[3]: 0b: non-XOR **1b: XOR**
NIV[4]: 0b: Disable NIV **1b: Enable NIV**



(22) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	LC5

UC1697u supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG388	SEG389	SEG390
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *`Set Color Mode`* below.

(23) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Note: *For serial bus modes, please refer to 8-bit tables below.*

Green Enhance Mode disabled (DC[4] = **1**):

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K-color)

12 bits of input RGB data are stored to 16 RAM bits. No dither is performed. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R3 R2 R1 R0 G3 G2 G1 G0
2nd Write Data Cycle	B3 B2 B1 B0 R3 R2 R1 R0
3rd Write Data Cycle	G3 G2 G1 G0 B3 B2 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G3 G2 G1 G0 B3 B2 B1 B0
2nd Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G3 G2 G1 G0 B3 B2 B1 B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 64K-color)

16 bits of input data are stored to 16 RAM bits directly.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R4 R3 R2 R1 R0 G5 G4 G3
2nd Write Data Cycle	G2 G1 G0 B4 B3 B2 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B4 B3 B2 B1 B0

Green Enhance Mode enabled (DC[4]=0):

LC[7:6] = 01b (RRRR-GGGG-BBB, 4K-color)

12 bits of input data are extended and stored to 16 RAM bits. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R3 R2 R1 R0 G4 G3 G2 G1
2nd Write Data Cycle	G0 B2 B1 B0 R3 R2 R1 R0
3rd Write Data Cycle	G4 G3 G2 G1 G0 B2 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G4 G3 G2 G1 G0 B2 B1 B0
2nd Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G4 G3 G2 G1 G0 B2 B1 B0

LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color)

The behaviors of 8-bit input mode and 16-bit input mode do not change with DC[4] setting. Refer to previous section for more information on these two input modes.

(24) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[2:0]	0	0	**1**	**1**	**0**	**1**	**1**	CSF2	CSF1	CSF0

COM scan function

CSF[0]: LRM sequence option
- **0b: LRM sequence: AEBCD-AEBCD**
- 1b : LRM sequence: AEBC-EBCDA

CSF[1]: FRC option
- **0b: FRC Disable**
- 1b: FRC Enable

CSF[2]: Shade-1, Shade-30 option
- **0 : Dither directly on input data(SRAM Change)**
- 1 : PWM on SEG output stage

(25) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(26) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(27) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	TT	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Do *NOT* use.

(28) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [2:0]	0	0	**1**	**1**	**1**	**0**	**1**	BR2	BR1	BR0

Bias ratio definition:

000b = 6 001b = 10 010b = 11 **011b = 12**

100b = 9

***(29)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	*CEN* register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 130 pixel rows, the LCM designer should set CEN to N-1 (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes.

***(30)* SET PARTIAL DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	*DST* register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

***(31)* SET PARTIAL DISPLAY END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	*DEN* register parameter							

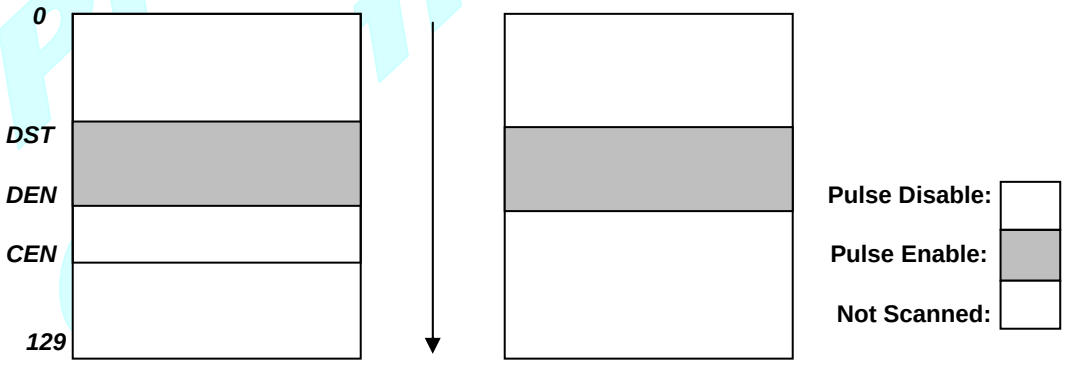
This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1b, the Mux-Rate is narrowed down to DST-DEN+1+(FLT+FLB)xLC[0]x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[8]=1b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use on/off mode, set PC[1:0]=00b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 32, it is recommended to set BR=6 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(32) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	*WPC0[7:0]* register parameter							

This command is to program the starting column address of RAM program window.

(33) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	*WPP0[7:0]* register parameter							

This command is to program the starting row address of RAM program window.

(34) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	*WPC1[7:0]* register parameter							

This command is to program the ending column address of RAM program window.

(35) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	*WPP1[7:0]* register parameter							

This command is to program the ending row address of RAM program window.

(36) SET WINDOW PROGRAM MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command controls the Window Program function.

AC[3]=0: Inside Mode

When Window Programming is under “Inside” mode , the CA and RA increment and wrap-around will be performed automatically around the boundaries as defined by registers WPC0, WPC1, WPP0, and WPP1, so that the CA/RA address will stay ***within*** the defined window of SRAM address, and therefore allow effective data update within the window.

AC[3]=1: Outside Mode

When Window Programming is under “Outside” mode, the CA and RA increment and wrap-around boundary will cover the entire UC1697u SRAM map (CA: 0~129, RA:0~129). However, when CA/RA points to a memory location within the window defined by registers WPC0, WPC1, WPP0, and WPP1, the SRAM data update operation will be suspended, the existing data will be retained and the input data will be ignored.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting.

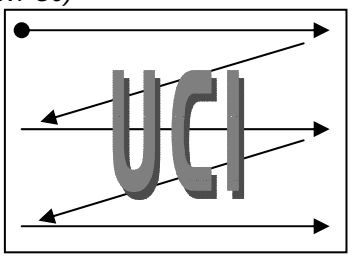
- WA decides whether the program RAM address advances to next row/column after reaching the specified window column / row boundary.
- RID controls the RAM address incrementing from WPP0 toward WPP1 (RID=0) or reverse the direction (RID=1).
- Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0).
- MX results the RAM column address incrementing from 129-WPC0 to 129-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the “window”, effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

Auto-increment order = 0 MX=0 RID = 0

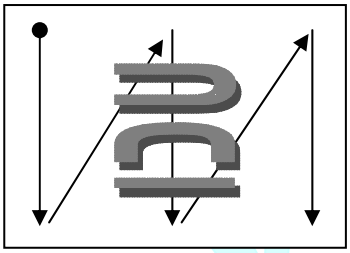
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 0

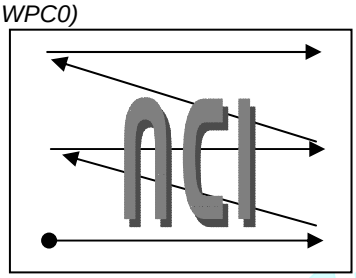
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=0 RID = 1

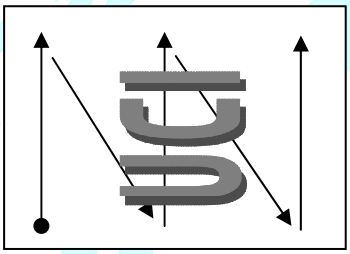
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 1

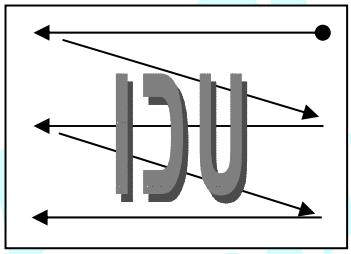
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=1 RID = 0

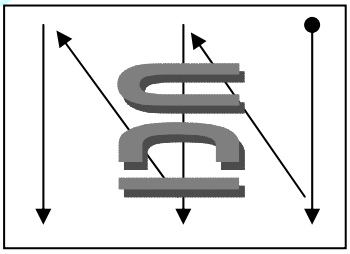
(WPP0,129-WPC0)



(WPP1,129-WPC1)

Auto-increment order = 1 MX=1 RID = 0

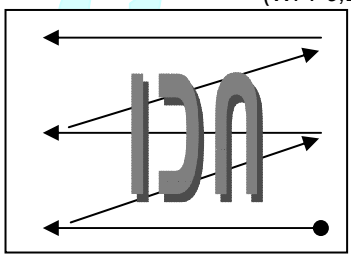
(WPP0,129-WPC0)



(WPP1,129-WPC1)

Auto-increment order = 0 MX=1 RID = 1

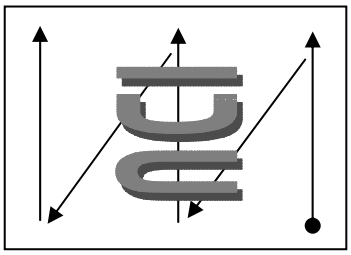
(WPP0,129-WPC0)



(WPP1,129-WPC1)

Auto-increment order = 1 MX=1 RID = 1

(WPP0,129-WPC0)



(WPP1,129-WPC1)

(37) SET MTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	**-**	*MTPC [4:0]* register parameter				

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Sleep
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

The following commands, (38) ~ (42), are used as MTP commands only when MTPC[3]=1.

(38) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (Triple-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	MTPM[6:0] register parameter						
	0	0	**-**	**-**	**-**	**-**	**-**	**-**	MTPM1[1:0]	

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to “1”. MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of “programming current” increases with the number of 1’s in MTPM. If the “programming current” appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1’s evenly into these cycles.

MTPM[6:0] : Set PMO value
MTPM1[1:0]: Set MID value

This command is only valid when MTPC[3]=1.

(39) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{OPT1} setting (use with BR=000) and is only valid when MTPC[3]=1.

(40) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (use with BR=001) and is only valid when MTPC[3]=1.

(41) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(42) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1697u via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[9:8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 6, UC1697u can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=130), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1697u supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3	4
Bias Ratio	6	10	11	12	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	-0.00	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\,\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} AND CONTRAST FINE TUNING

Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. It is very difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to precisely match the actual V_{OP} of each LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH FOR COG

The power supply circuit of UC1697u is designed to handle LCD panels with loading up to ~16nF using 7-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.7V$. For larger LCD panels, use lower resistance ITO glass.

Due to crosstalk consideration, ~16nF is also the recommended maximum LCD panel loading for COG applications. Using 4.5-Ω/Sq low resistance ITO glass for the IC bonding substrate can help improve image quality and operation tolerance.

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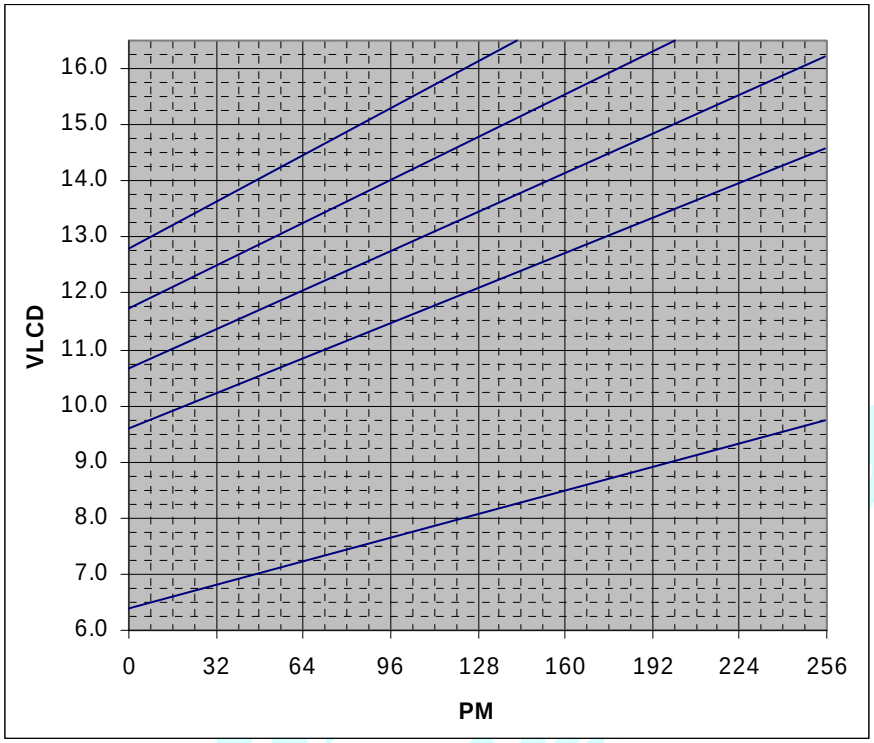
V_{LCD} QUICK REFERENCE



BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
6	6.402	13.03	0	6.40
			255	9.72
10	10.670	21.71	0	10.67
			255	16.21
11	11.737	23.88	0	11.74
			200	16.51
12	12.804	26.06	0	12.80
			142	16.50
9	9.603	19.54	0	9.60
			255	14.59

V_{LCD}-PM-BR relationship at 25°C

NOTE:

1. For good product reliability, please keep V_{LCD} under **16.5V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

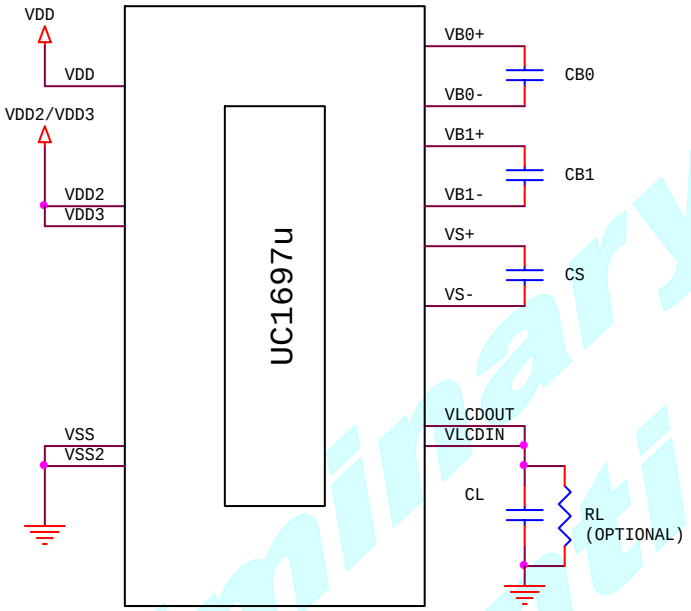


FIGURE 1: Sample circuit using internal Hi-V generator circuit

NOTE:
Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

$C_{B0\sim1}$: 2.2 μF/2V or 300 x LCD load capacitance, whichever is higher.

C_L : 330 nF (25V) is appropriate for most applications.

C_S : 150 ~ 220nF/5V

R_L : 3.3~10 MΩ to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1697u contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 88, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 87, 65, 44 and 33, line rate will be scaled down automatically by 1.5, 2, 3 and 4 times to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate 239Hz or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to On/Off mode, line rate will be scaled down automatically by ~30% to reduce power.

Under most situations, flicker behavior is similar between these two modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming convention is COM(*X*), where *X* =1~130, referring to the COM driver for the *X*-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1697u will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1697u will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1697u provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

GRAY-SHADE MODULATION MODE

UC1697u has two gray-shade modulation modes: 32-shade and On/Off mode.

The On/Off mode will consume roughly 40~45% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 32-shade mode.

INPUT COLOR FORMATS

UC1697u supports the following two different input color formats.

4KC (12-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 5R-6G-5B format before they are stored to display RAM.

64KC (16-bit/RGB): This is the native color mode. Data will be stored directly to on-chip SRAM in 5R-6G-5B (16-bit) format. This is the default input format mode.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can mix several color modes together and switch among them in real time.

For example, the menu portion can be painted in 4K-color mode for fast update speed, and then switch to 64K-color mode, together with window programming function to effectively produce smooth graphics images.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1697u can be as short as 15µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 0.9\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 0.22\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.25\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast and color saturation will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/130	1/12	8.95%	7.2%	6.4%
1/130	1/11	8.85%	7.1%	6.4%

VIDEO CSTN & COG

UC1697u can support very fast CSTN for video rate applications. For LCM with t_r+t_f = 180 ~ 200 mS or smaller, it is recommended to set the line rate higher such that the frame rate is 250Hz or higher. For such applications, special attentions are necessary for COG design to minimize crosstalk and to ensure plenty of power is available to drive the LCM at such high speed.

- At this fast scan rate, the SEG/COM trace RC decay minimization will be very critical in minimizing crosstalk.
- MPU will perform frequent high speed update to the on-chip video RAM for video applications. Make sure the ITO does not cause on-chip V_{DD}-V_{SS} to fall below 1.65V, and V_{SS} bounce is under 7% x V_{DD}.

For VSTN (video CSTN) applications, it is recommended to use low resistance ITO glass to help reducing SEG signal RC decay, minimizing V_{DD}, V_{SS} noise, and ensuring sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

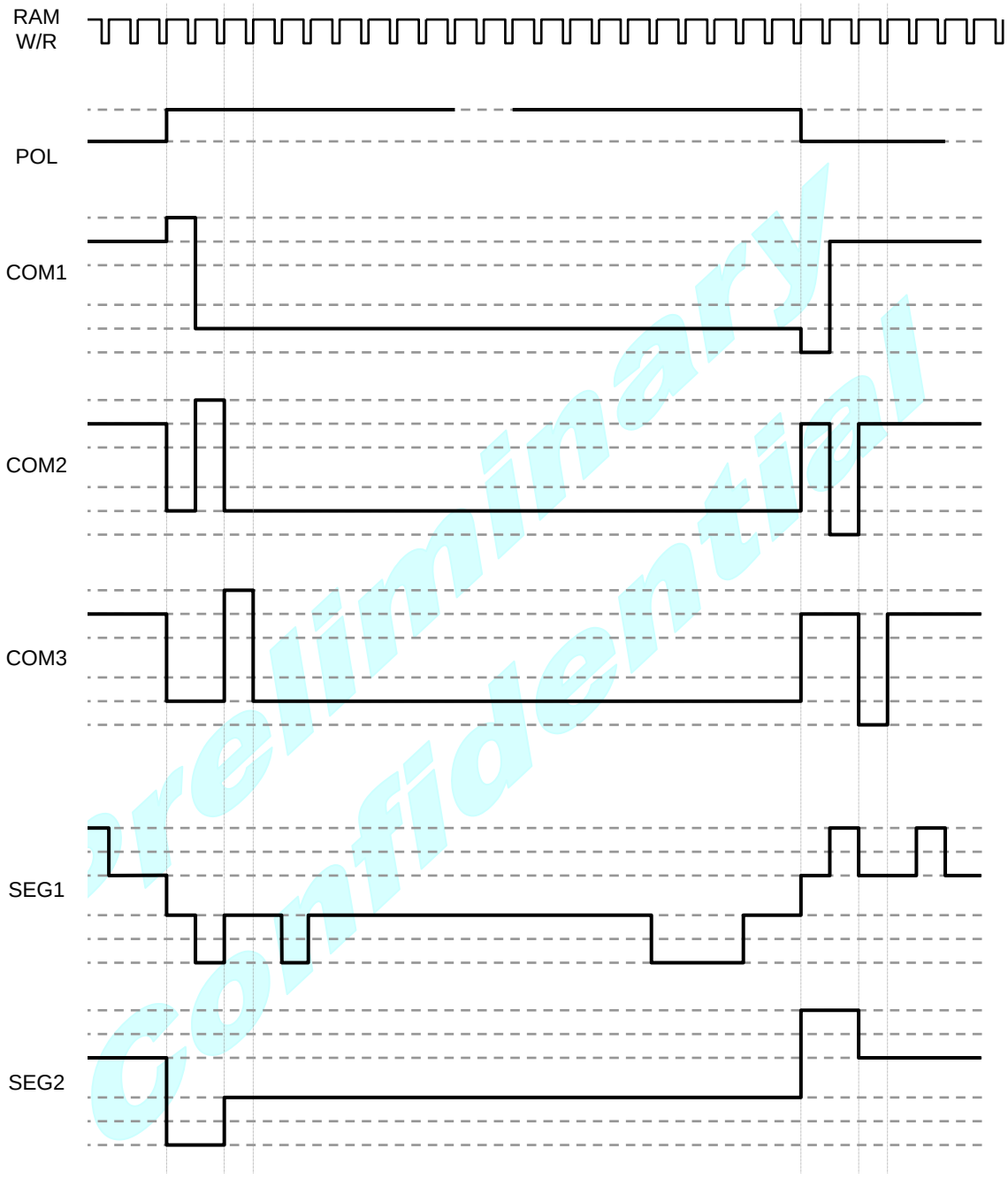


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1697u supports two parallel bus protocols, in either 8-bit or 16-bit bus width, and three serial bus protocols.

Designers can either use parallel buses to achieve high data transfer rate, or use serial buses to create compact LCD modules.

		Bus Type					
		8080		6800		S8 (4wr)	S8uc (3/4wr)
Width		16-bit	8-bit	16-bit	8-bit	Serial	
Access		Read/Write				Write Only	
Control & Data Pins	BM[1:0]	10	00	11	01	00	00
	{DB[15], DB[13]}	Data	0x	Data	0x	10	11
	CS[1:0]	Chip Select					
	CD	Control / Data					
	WR0	$\overline{WR}$		R/$\overline{W}$		0	
	WR1	$\overline{RD}$		EN		0	
	DB[1,3,5,7,9,11]	Data	–	Data	–	–	
	DB[0,2,4,6,8,10,12,14]	Data	Data	Data	Data	DB[8]=SDA, DB[0]=SCK	

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Interface	CS Init bus state	CD 1⇔0 Init bus state	CD 1⇨0 Init color mapping	RESET Init bus state	RESET Init color mapping
16-bit	✓	–	–	✓	✓	✓
8-bit	✓	–	–	✓	✓	✓
S8	✓	✓	–	✓	✓	✓
S8uc	✓	–	✓	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS Sync / RESET can be used to initialize bus state machine (like 8-bit / S8).
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1697u internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 16-bit mode, by either *Set CA,* or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

16-BIT & 8-BIT BUS OPERATION

UC1697u supports both 8-bit and 16-bit bus width. The bus width is determined by pin BM[1].

8-bit bus operation exactly doubles the clock cycles of 16-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 8-bit mode is reset each time CD pin changes state (when CS is active).

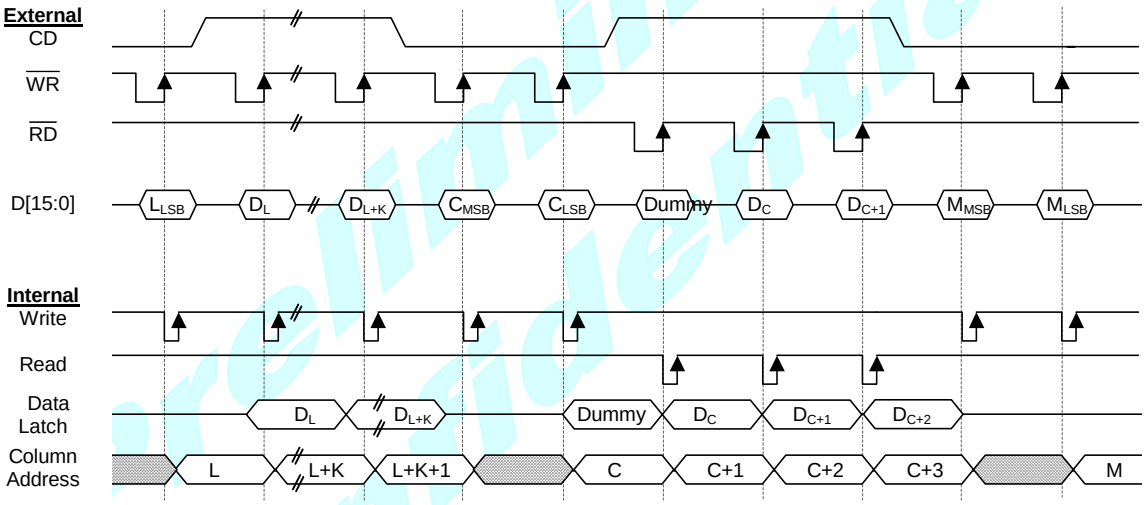


FIGURE 3: 16-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1697u supports two serial modes, one 4-wire SPI mode (S8), and one compact 3/4-wire mode (S8uc). Bus interface mode is determined by the wiring of the BM[1:0], DB[15] and DB[13]. See table on last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

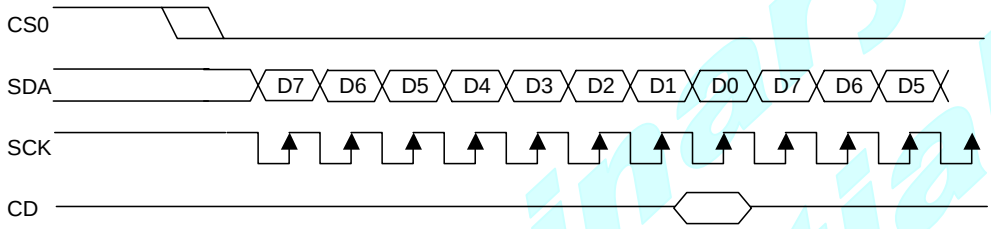


FIGURE 4.a: 4-wire Serial Interface (S8)

S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. However, in addition to CS pins, CD pin transitions will also reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

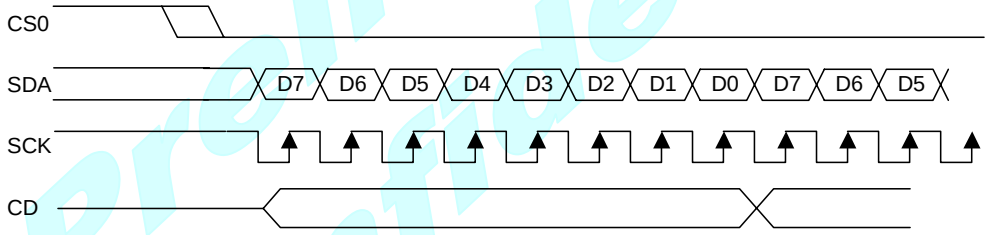


FIGURE 4.b: 3/4-wire Serial Interface (S8uc)

HOST INTERFACE REFERENCE CIRCUIT

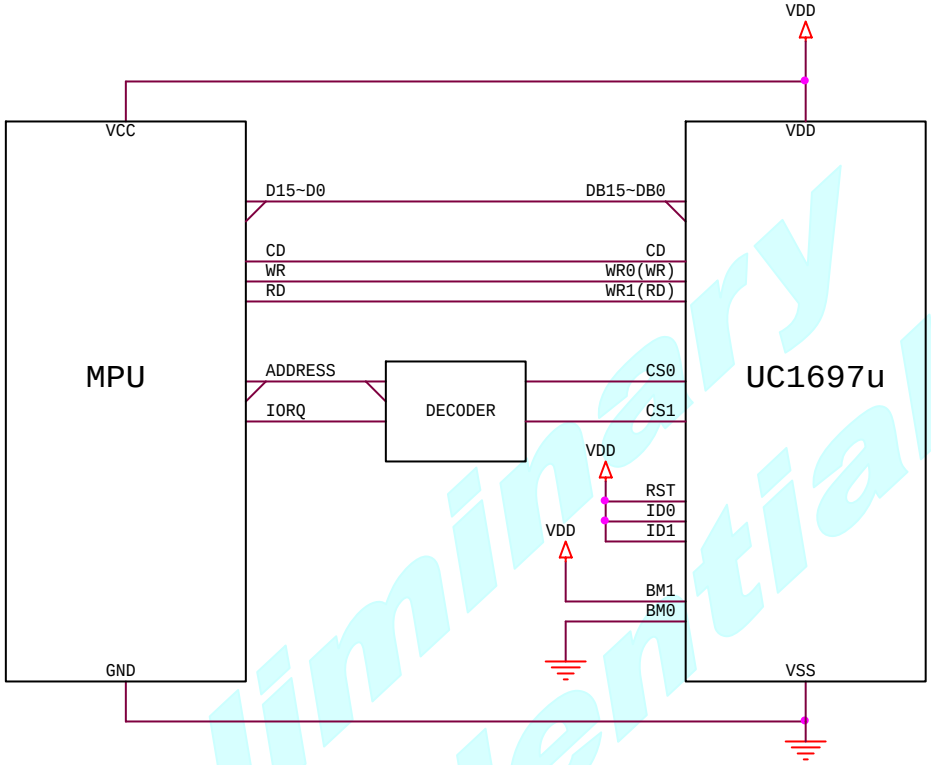


FIGURE 5: 8080/16-bit parallel mode example

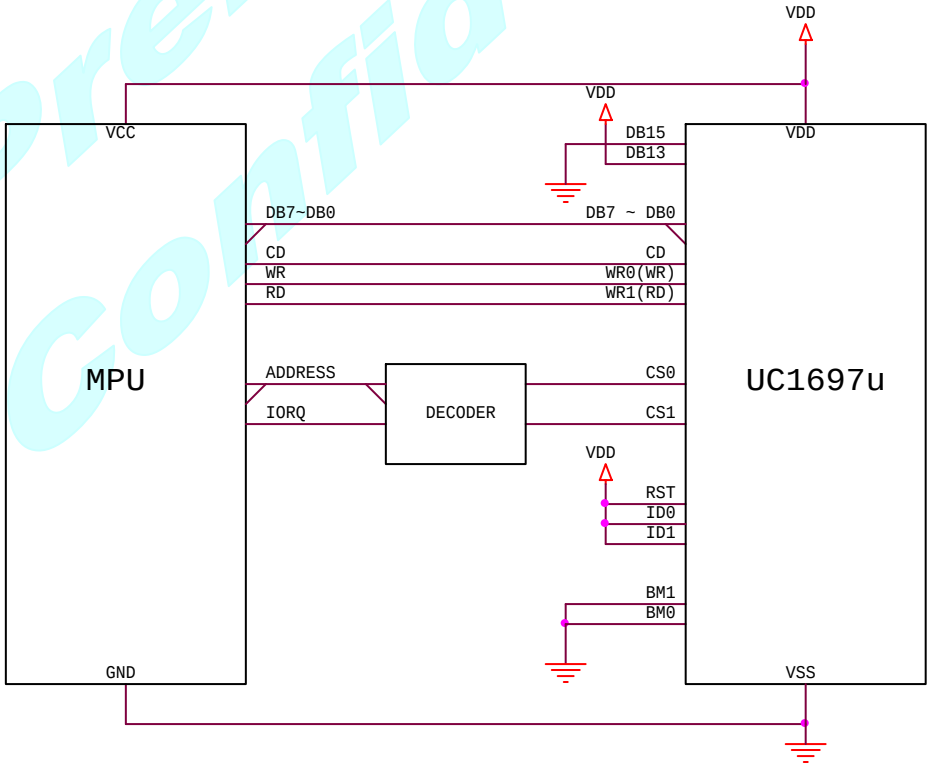


FIGURE 6: 8080/8-bit parallel mode example

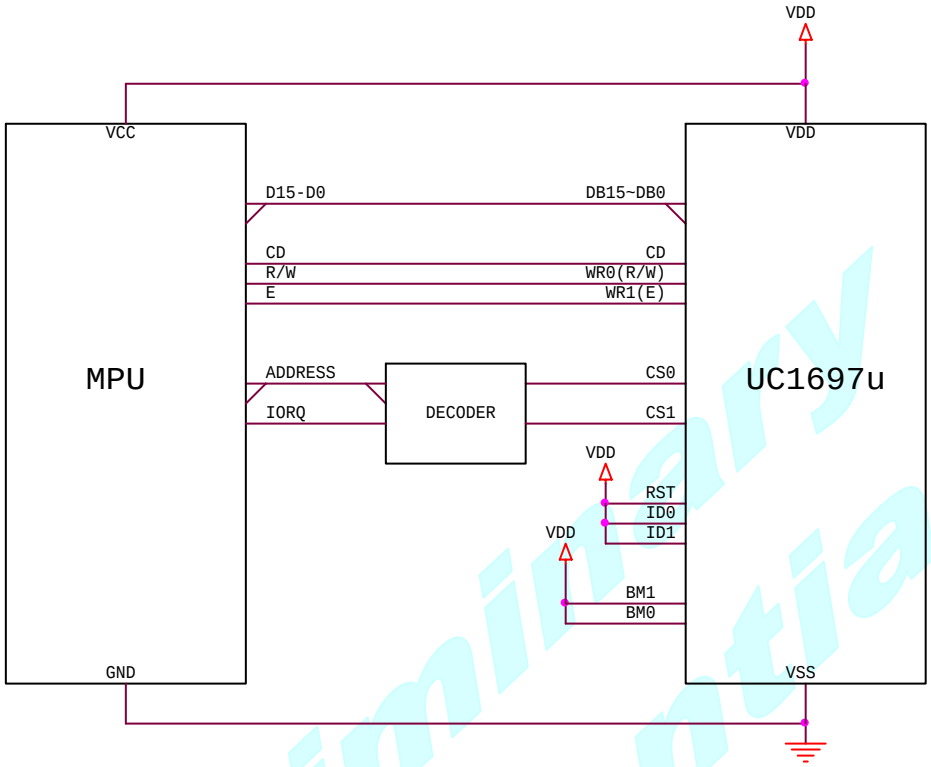


FIGURE 7: 6800/16-bit parallel mode example

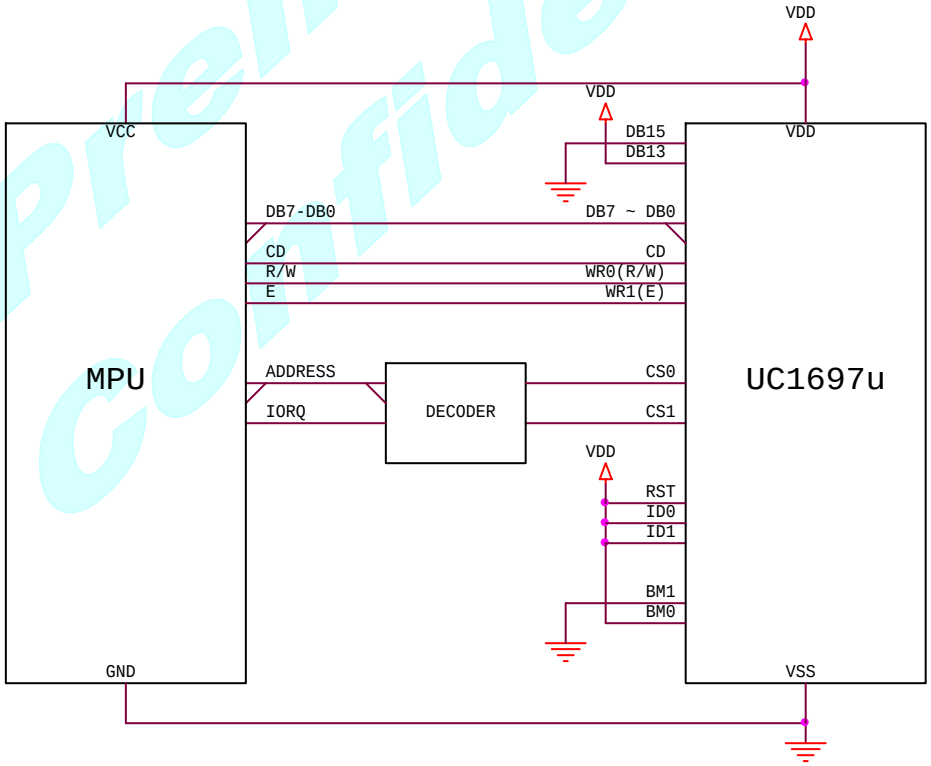


FIGURE 8: 6800/8-bit parallel mode example

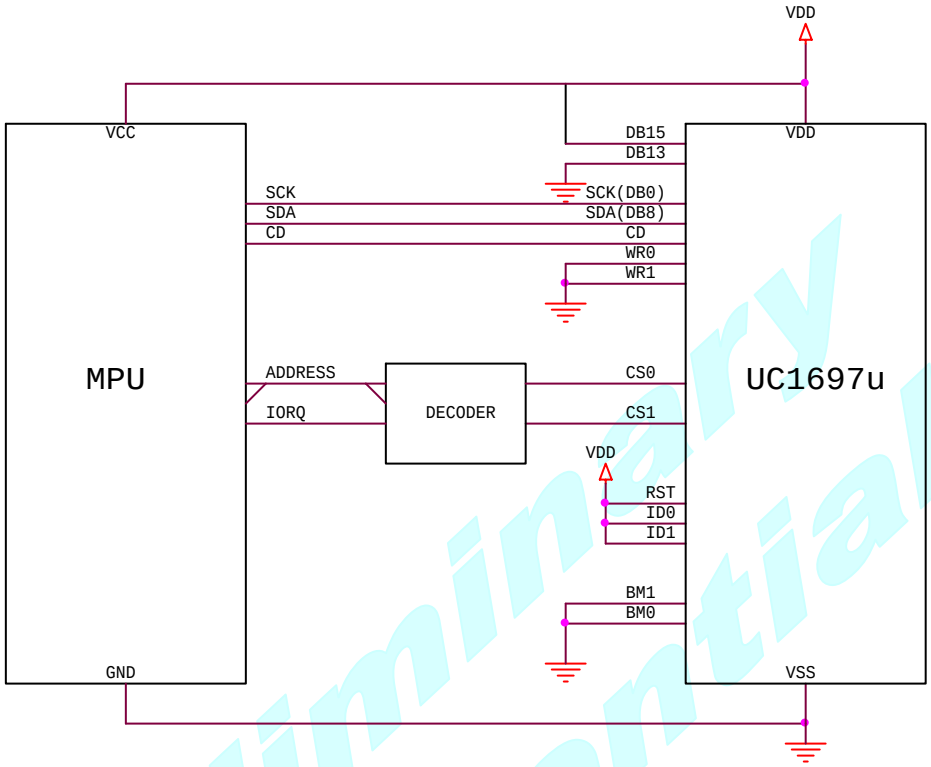


FIGURE 9: 4-Wires SPI (S8) serial mode example

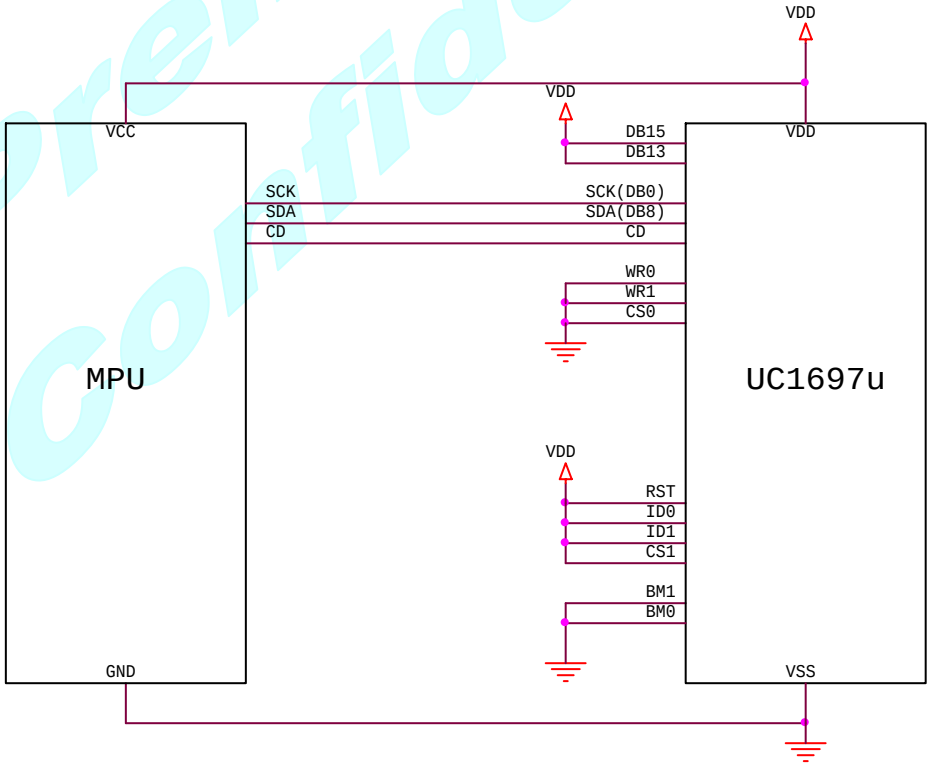


FIGURE 10: 3/4-Wires SPI (S8uc) serial mode example

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 130x130x16.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing `Set Row Address` and `Set Column Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (129), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 129), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (129–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Scroll Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 130)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 130. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, 130)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1*, 130)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

WINDOW PROGRAM

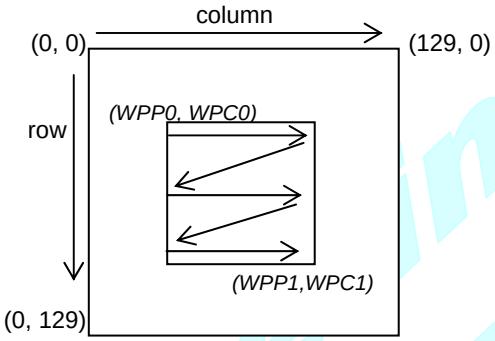
Window program is designed for data-write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and AC[3] setting for inside/outside window mode. When AC[3] is set to '0' (default value), data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). When AC[3] is set to '1', data will be written to whole SRAM excluding the specified window area.

The data-write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data-write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

Specify the starting point of data-write by issuing commands `Set Window Program Starting Column Address`, and `Set Window Program Starting Row Address`.

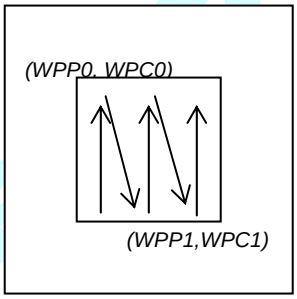
Example1 (AC[2:0] = 001) **:**

AC[3]=0 MX=0



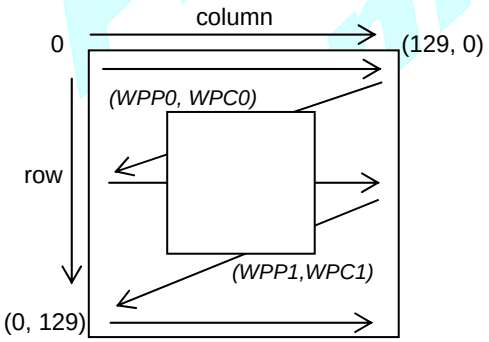
Example 2 (AC[2:0] = 111) **:**

AC[3] = 0 MX = 0



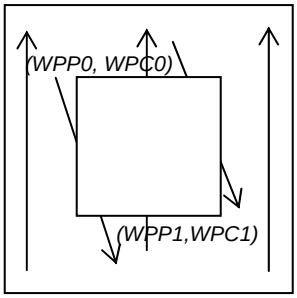
Example1-1 :

AC[3]=1 MX=0



Example 2-1 :

AC[3] = 1 MX = 0



Row Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H		COM1	COM17	COM130	COM16
01H		COM2	COM18	COM129	COM15
02H		COM3	COM19	COM128	COM14
03H		COM4	COM20	COM127	COM13
04H		COM5	COM21	COM126	COM12
05H		COM6	COM22	COM125	COM11
06H		COM7	COM23	COM124	COM10
07H		COM8	COM24	COM123	COM9
08H		COM9	COM25	COM122	COM8
09H		COM10	COM26	COM121	COM7
0AH		COM11	COM27	COM120	COM6
0BH		COM12	COM28	COM119	COM5
0CH		COM13	COM29	COM118	COM4
0DH		COM14	COM30	COM117	COM3
0EH		COM15	COM31	COM116	COM2
0FH		COM16	COM32	COM115	COM1
10H		COM17	COM33	COM114	COM130
11H		COM18	COM34	COM113	COM129
12H		COM19	COM35	COM112	COM128
13H		COM20	COM36	COM111	COM127
14H		COM21	COM37	COM110	COM126
15H		COM22	COM38	COM109	COM125
16H		COM23	COM39	COM108	COM124
17H		COM24	COM40	COM107	COM123
18H		COM25	COM41	COM106	COM122
19H		COM26	COM42	COM105	COM121
1AH		COM27	COM43	COM104	COM120
1BH		COM28	COM44	COM103	COM119
1CH		COM29	COM45	COM102	COM118
6AH		COM107	COM123	COM24	COM40
6BH		COM108	COM124	COM23	COM39
6CH		COM109	COM125	COM22	COM38
6DH		COM110	COM126	COM21	COM37
6EH		COM111	COM127	COM20	COM36
6FH		COM112	COM128	COM19	COM35
70H		COM113	COM129	COM18	COM34
71H		COM114	COM130	COM17	COM33
72H		COM115	COM1	COM16	COM32
73H		COM116	COM2	COM15	COM31
74H		COM117	COM3	COM14	COM30
75H		COM118	COM4	COM13	COM29
76H		COM119	COM5	COM12	COM28
77H		COM120	COM6	COM11	COM27
78H		COM121	COM7	COM10	COM26
79H		COM122	COM8	COM9	COM25
7AH		COM123	COM9	COM8	COM24
7BH		COM124	COM10	COM7	COM23
7CH		COM125	COM11	COM6	COM22
7DH		COM126	COM12	COM5	COM21
7EH		COM127	COM13	COM4	COM20
7FH		COM128	COM14	COM3	COM19
80H		COM129	COM15	COM2	COM18
81H		COM130	COM16	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG386	SEG387	SEG388	SEG389	SEG390
0	SEG1	SEG2	SEG3	SEG4	SEG5			SEG386	SEG387	SEG388	SEG389	SEG390
1	SEG388	SEG389	SEG390	SEG385	SEG386			SEG5	SEG6	SEG1	SEG2	SEG3

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st byte of Write data: 11111111b

⇒ 2nd byte of Write data: 11111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1697u has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 150mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1697u enters RESET sequence:

- Operation mode will be “Reset”.
- All control registers are reset to default values. Refer to section *Control Registers* for details of their default values.

OPERATION MODES

UC1697u has three operating modes (OM): Reset, Sleep, Normal.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by `Set Display Enable`, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1697u internal clock. To ensure consistent system states, wait at least 10μS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
Reset command RST_ pin pulled “L” Power ON reset	Reset	00
Set Driver Enable to “0”	Sleep	10
Set Driver Enable to “1”	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1697u consumes very little energy in Sleep mode (typically under 2μA).

EXITING SLEEP MODE

UC1697u contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1697u internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1697u power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 150 ms before the CPU starting to issue commands to UC1697u. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD}, $V_{DD2/3}$ should be started not later than V_{DD}.

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 14.

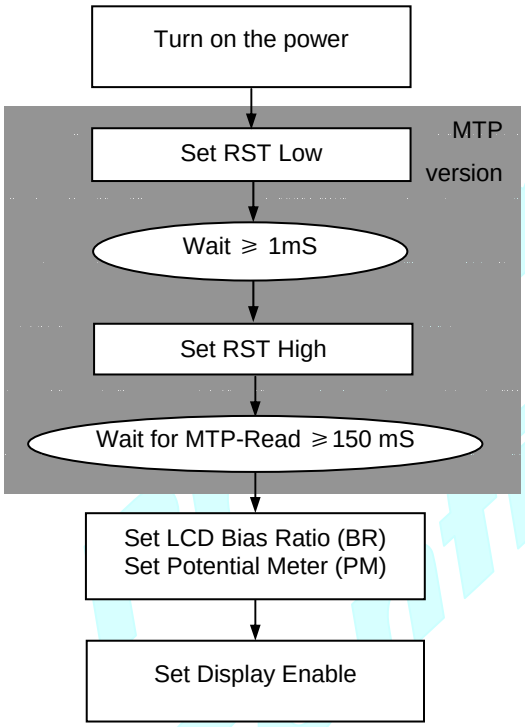


Figure 12: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 10 KΩ for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 0.1 uF, then the draining time required for V_{LCD} is ~3 mS.

When internal V_{LCD} is not used, UC1697u will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

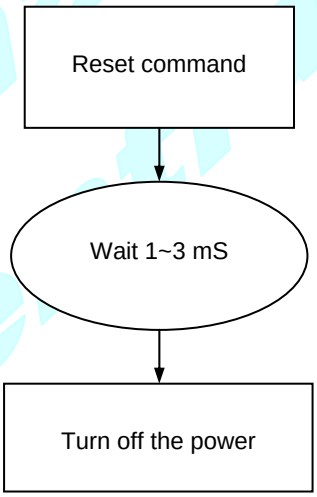


Figure 13: Reference Power-Down Sequence

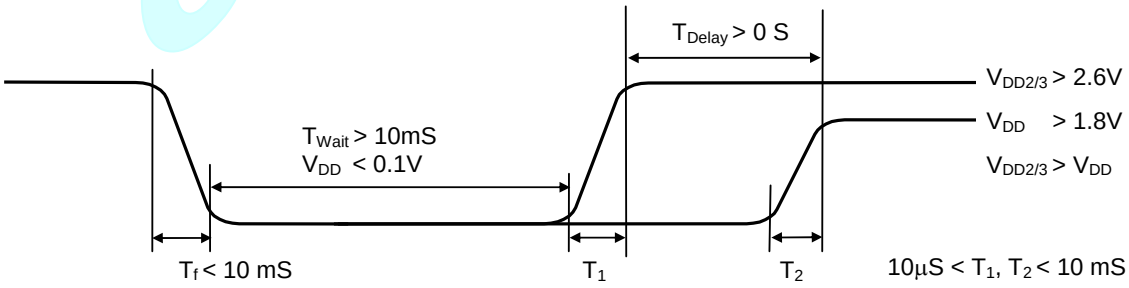


Figure 14: Delay allowance and Power Off-On Sequence

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1697u such that LCM makers can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1697u:

MTP-Erase, MTP-Program, MTP-Read.

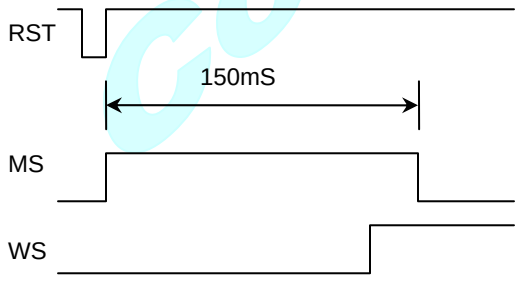
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1697u, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1697u, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

During the MTP-READ process, it is actually safe to issue commands or perform data write to the LCM. The only thing that is blocked is the LSB of the *Set Display Enable* command, which results in the DC[2] being effectively locked at "0" during this auto-MTP-READ process.

Although user can use *Read Status* command in a polling loop to make sure {MS, WS}={0, 1} before proceeding with the normal operations, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 7~9V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operations, TST4 should be open, or connected to V_{DD3}.

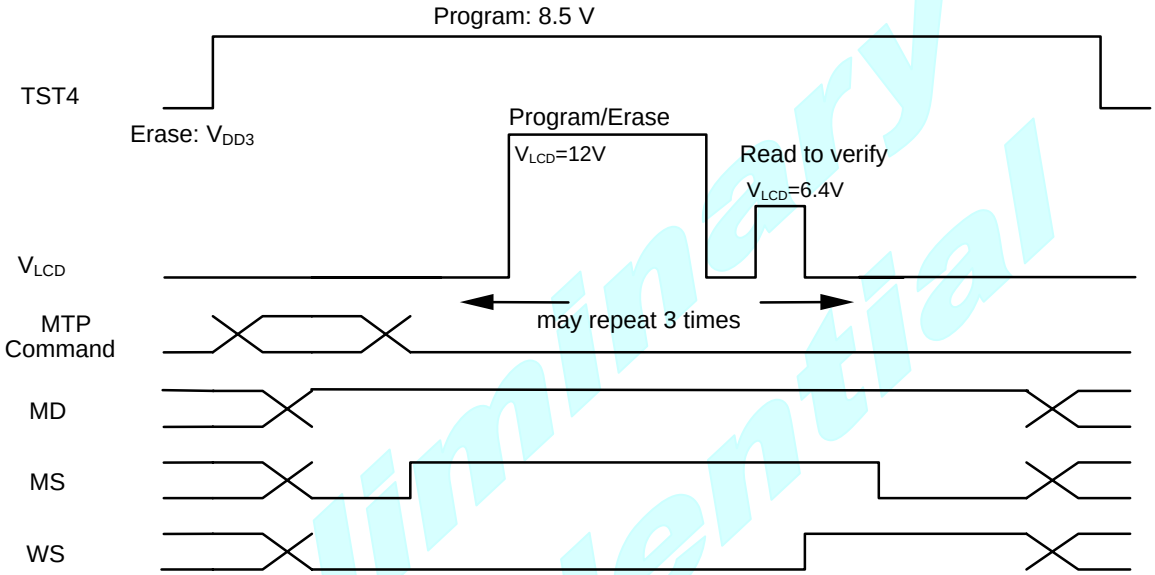
	V_{LCD}	**TST4 (external input)**
Program	MTP3 : 3Eh (12V)	8.5V (1mA per bit)
Erase	MTP3 : 3Eh (12V)	Floating or V_{DD3}
Read	MTP2 : 00h (6.4V)	Floating or V_{DD3}

Note:

1. Do Erase before Program and program one bit at a time.
2. It's recommended to use $V_{DD2/3}$ > 3.0V when MTP Program or Erase.

3. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 9 MTP cell bits. They are divided into two groups for different purpose.

MTP[6:0] : V_{LCD} Trim
When PMO[6]=1: PM with trim = PM - PMO[5:0]
When PMO[6]=0: PM with trim = PM + PMO[5:0]

MTPID[1:0]: For LCM manufacturer's configuration.

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	0	0	1	0	1	0	0	0	1	1	(16) Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	(39)Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	(40)Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	1	1	0		MTP3: 3Eh(12V)
R	0	0	1	1	1	1	0	1	1	0	(41)Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP4: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	(42)Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP5: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	(38)Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	MTPM MTPM1	Ex: To program MTPM[0] to be 1, set the value to 00000001b *
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 8.5V
R	0	0	1	0	1	1	1	0	0	0	(37) Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	(3)Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	(16) Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	(39) Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	(40) Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	1	1	0		MTP3: 3Eh(12V)
R	0	0	1	1	1	1	0	1	1	0	(41) Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP4: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	(42) Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP5: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	(38) Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0 0	0 0	0 0	0 0	1 0	1 0	1 0	1 0	MTPM MTPM1	Ex: To erase MTPM[3:0], set the value to 00001111b
R	0	0	1	0	1	1	1	0	0	0	(37) Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	WS	-	MS	(3) Get Status & PM	Check MTP Status until MS=0 WS=1
R											V_{DD}=0V	Power OFF

Note: It is recommended that users clear all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS
C	0	0	0	0	1	0	0	1	#	#	(5) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(16) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	(23) Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	(28) Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(12) Set V_{BIAS} Potentiometer	LCD specific operating voltage setting
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(25) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(19) Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	(19) Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1697u require special "ESD Sensitivity" consideration in particular:

Test Mode		MM V_{DD}	MM V_{SS}	HBM V_{DD}	HBM V_{SS}
LCD Driver		(TBD)			
LCM Interface					
LCM HV pin/ Test pin	TST1/2/4				
	CB pins				
	VLCDIN				
	VLCDOUT				
PWR / GND					

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, Note 1 and 2

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Driving voltage	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

NOTE:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.5		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ = 2.8V, 25^{O}C		15.2	16.5	V
V_D	LCD data voltage	$V_{DD2/3}$ = 2.8V, 25^{O}C	0.93		1.76	V
V_{IL}	Input logic LOW				0.2V_{DD}	V
V_{IH}	Input logic HIGH		0.8V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD}	V
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current				1.5	µA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 15.8V		820	1100	Ω
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 15.8V		820	1100	Ω
$R_{ONs(COM)}$	Downward COM output impedance	V_{LCD} = 15.8V		1650	2200	Ω
f_{LINE}	Average line rate	LC[4:3] = 10b, 25^{O}C	-10%	31.1	+10%	Klps

Note : Voltages exceeding the Max. value may still keep the IC operating properly, yet might shorten its lifetime.

POWER CONSUMPTION

V_{DD} = (TBD) V,
V_{LCD} = (TBD) V,
Mux Rate = (TBD),
C_B = (TBD) µF,
N-line inversion = (TBD) lines
Bias Ratio = (TBD),
Line Rate = (TBD),
Bus mode = (TBD),
Temperature = 25^{O}C,
Color Mode = (TBD) mode,
PM = (TBD),
Panel Loading (PC[1:0]) = (TBD),
C_L = (TBD) nF,
MTP=(TBD) H,
All HV outputs are open circuit.

Display Pattern	Conditions	Typ. (µA)	Max. (µA)
All-Pixel-OFF	Bus = idle	(TBD)	(TBD)
2-pixel checker	Bus = idle	(TBD)	(TBD)
None	Reset (stand-by current)	<1	5

AC CHARACTERISTICS

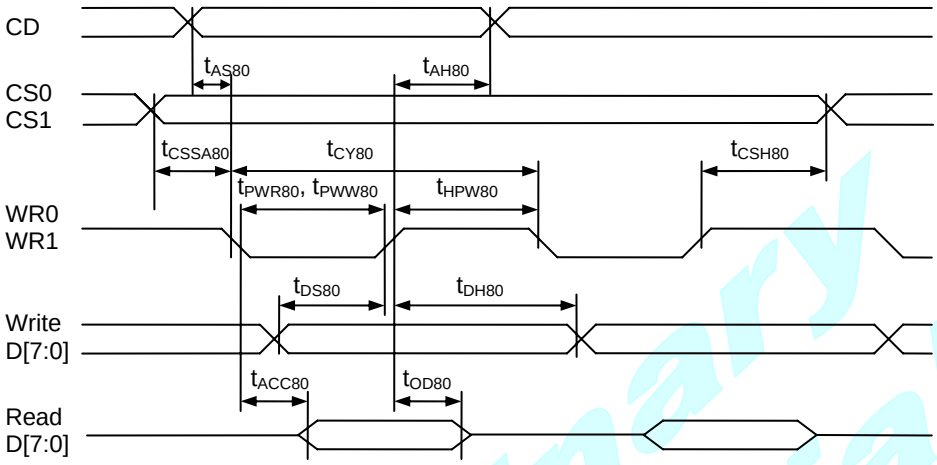


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

Normal Mode : (8 bits bus timing is only for 5-6-5 color input mode)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 170 130 100 80	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit		65 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 85 65 50 40	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 320 270 180 145	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit (read)		160 90	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit (write)		135 72	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bits bus (read) (write)		 160 135 90 72	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		60 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 30	120 60	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0		nS

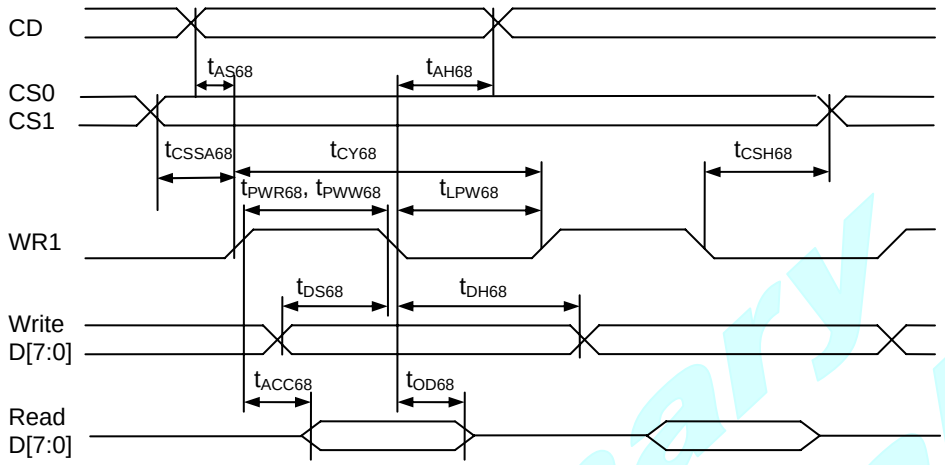


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

Normal Mode : (8-bit bus timing is valid only for 5-6-5 color input mode)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 170 130 100 80	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit		65 40	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 85 65 50 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 320 270 180 145	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit (read)		160 90	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit (write)		135 72	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 160 135 90 72	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 30	120 60	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0		nS

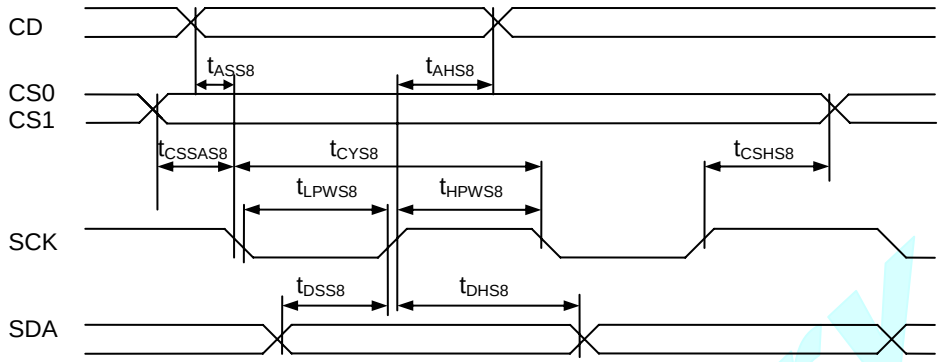


FIGURE 17: Serial Bus Timing Characteristics (for S8/S8uc)

Normal Mode :

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		75	–	nS
t_{LPWS8}		Low pulse width		37	–	nS
t_{HPWS8}		High pulse width		37	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10		nS

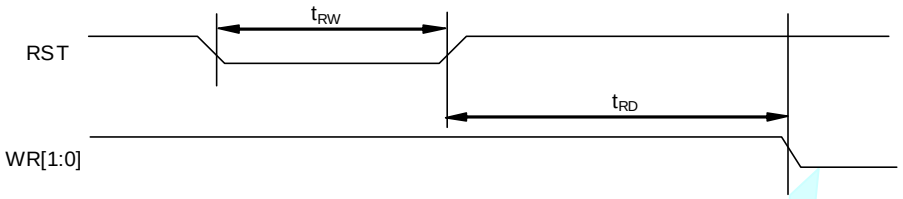


FIGURE 19: Reset Characteristics

(1.65V ⩽ V_{DD} < 3.3V, Ta= –30 to +85^{o}C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
13505 x 1542 μM^2 ± 50 μM

DIE THICKNESS:
0.4 mm ± 0.02 mm

BUMP HEIGHT:
15 μM
(H_{MAX}-H_{MIN}) within die ≤ 2μM

COM/SEG SIZE:
118 x 17 μM^2 (Typ.)

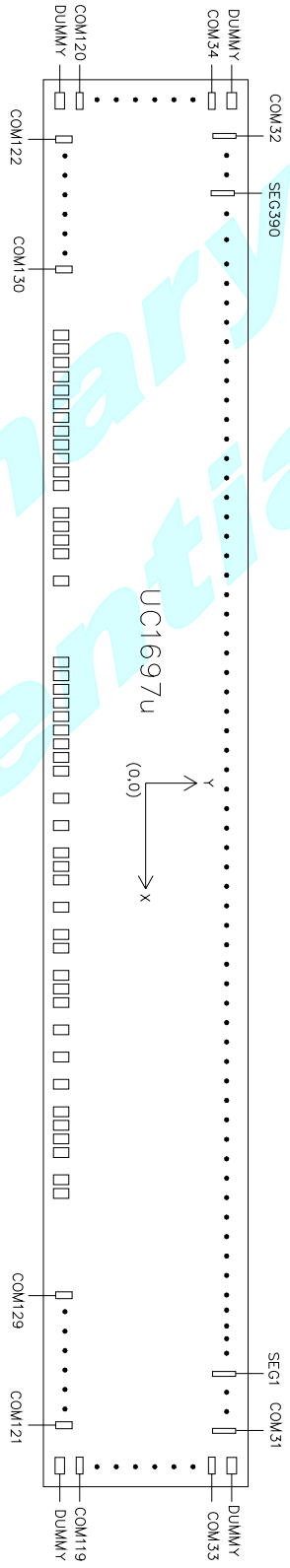
BUMP PITCH:
SEG: 31 μM (Typ.)
COM: 31 μM (Typ.)

BUMP GAP:
SEG/COM: 14 μM (Typ.)
12 μM (Min.)

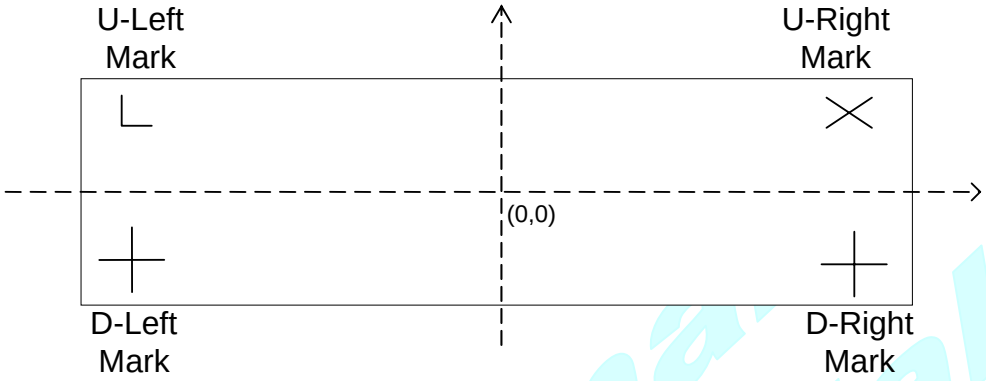
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

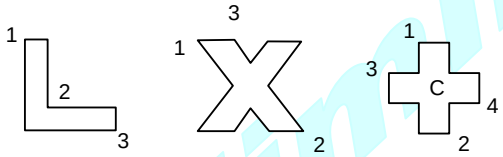
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

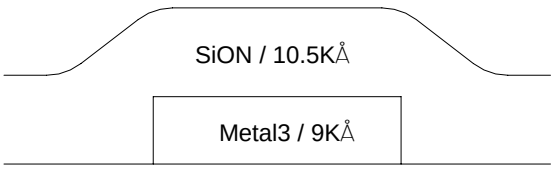
COORDINATES:

	U-Left Mark (L)		U-Right Mark (X)	
	X	Y	X	Y
1	-6519.9	512.6	6479.9	512.6
2	-6504.3	488.1	6519.9	472.6
3	-6479.9	472.6	6489.9	512.6

	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	6304.2	-619.2	-6324.2	-619.2
2	6324.2	-714.2	-6304.2	-714.2
3	6272.7	-656.7	-6355.7	-656.7
4	6355.7	-676.7	-6272.7	-676.7
C	6314.2	-666.7	-6314.2	-666.7

Note: The values of x-coordinate and y-coordinate in the tables are after-rounded.

TOP METAL AND PASSIVATION:



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-6646.5	702.5	118	36
2	COM34	-6646.5	662	118	17
3	COM36	-6646.5	631	118	17
4	COM38	-6646.5	600	118	17
5	COM40	-6646.5	569	118	17
6	COM42	-6646.5	538	118	17
7	COM44	-6646.5	507	118	17
8	COM46	-6646.5	476	118	17
9	COM48	-6646.5	445	118	17
10	COM50	-6646.5	414	118	17
11	COM52	-6646.5	383	118	17
12	COM54	-6646.5	352	118	17
13	COM56	-6646.5	321	118	17
14	COM58	-6646.5	290	118	17
15	COM60	-6646.5	259	118	17
16	COM62	-6646.5	228	118	17
17	COM64	-6646.5	197	118	17
18	COM66	-6646.5	166	118	17
19	COM68	-6646.5	135	118	17
20	COM70	-6646.5	104	118	17
21	COM72	-6646.5	73	118	17
22	COM74	-6646.5	42	118	17
23	COM76	-6646.5	11	118	17
24	COM78	-6646.5	-20	118	17
25	COM80	-6646.5	-51	118	17
26	COM82	-6646.5	-82	118	17
27	COM84	-6646.5	-113	118	17
28	COM86	-6646.5	-144	118	17
29	COM88	-6646.5	-175	118	17
30	COM90	-6646.5	-206	118	17
31	COM92	-6646.5	-237	118	17
32	COM94	-6646.5	-268	118	17
33	COM96	-6646.5	-299	118	17
34	COM98	-6646.5	-330	118	17
35	COM100	-6646.5	-361	118	17
36	COM102	-6646.5	-392	118	17
37	COM104	-6646.5	-423	118	17
38	COM106	-6646.5	-454	118	17
39	COM108	-6646.5	-485	118	17
40	COM110	-6646.5	-516	118	17
41	COM112	-6646.5	-547	118	17
42	COM114	-6646.5	-578	118	17
43	COM116	-6646.5	-609	118	17
44	COM118	-6646.5	-640	118	17
45	COM120	-6646.5	-671	118	17
46	DUMMY	-6646.5	-707	118	27
47	COM122	-6528.8	-662	17	118
48	COM124	-6497.8	-662	17	118
49	COM126	-6466.8	-662	17	118
50	COM128	-6435.8	-662	17	118
51	COM130	-6404.8	-662	17	118
52	D15	-6131.4	-678	45	84
53	VDDX	-6071.4	-678	45	84
54	D14	-6011.4	-678	45	84

#	Pad	X	Y	W	H
55	D13	-5765.4	-678	45	84
56	D12	-5705.4	-678	45	84
57	D11	-5459.4	-678	45	84
58	D10	-5399.4	-678	45	84
59	D9	-5153.4	-678	45	84
60	D8	-5093.4	-678	45	84
61	D7	-4847.4	-678	45	84
62	D6	-4787.4	-678	45	84
63	D5	-4541.4	-678	45	84
64	D4	-4481.4	-678	45	84
65	D3	-4235.4	-678	45	84
66	D2	-4175.4	-678	45	84
67	D1	-3929.4	-678	45	84
68	D0	-3869.4	-678	45	84
69	RST	-3707.4	-678	45	84
70	WR0	-3461.4	-678	45	84
71	VDDX	-3401.4	-678	45	84
72	WR1	-3341.4	-678	45	84
73	CD	-3179.4	-678	45	84
74	CS0	-2933.4	-678	45	84
75	VDDX	-2873.4	-678	45	84
76	CS1	-2813.4	-678	45	84
77	BM0	-2567.4	-678	45	84
78	VDDX	-2507.4	-678	45	84
79	BM1	-2447.4	-678	45	84
80	TST4	-2285.4	-678	45	84
81	TST4	-2225.4	-678	45	84
82	TST1	-1814.6	-678	45	84
83	TST2	-1754.6	-678	45	84
84	ID0	-1497.9	-678	45	84
85	VDDX	-1437.9	-678	45	84
86	ID1	-1377.9	-678	45	84
87	ID2	-1131.9	-678	45	84
88	VSS	-1057.4	-678	45	84
89	VSS	-997.4	-678	45	84
90	VSS	-937.4	-678	45	84
91	VSS	-877.4	-678	45	84
92	VSS	-817.4	-678	45	84
93	VSS	-757.4	-678	45	84
94	VSS	-697.4	-678	45	84
95	VSS	-637.4	-678	45	84
96	VSS	-577.4	-678	45	84
97	VSS	-517.4	-678	45	84
98	VSS	-457.4	-678	45	84
99	VSS	-397.4	-678	45	84
100	VSS2	-224.4	-678	45	84
101	VSS2	-164.4	-678	45	84
102	VSS2	-104.4	-678	45	84
103	VSS2	-44.4	-678	45	84
104	VSS2	15.6	-678	45	84
105	VSS2	75.6	-678	45	84
106	VSS2	135.6	-678	45	84
107	VSS2	195.6	-678	45	84
108	VSS2	255.6	-678	45	84

#	Pad	X	Y	W	H
109	VSS2	315.6	-678	45	84
110	VSS2	375.6	-678	45	84
111	VSS2	435.6	-678	45	84
112	VDD	495.6	-678	45	84
113	VDD	555.6	-678	45	84
114	VDD	615.6	-678	45	84
115	VDD	675.6	-678	45	84
116	VDD	735.6	-678	45	84
117	VDD	795.6	-678	45	84
118	VDD	855.6	-678	45	84
119	VDD	915.6	-678	45	84
120	VDD	975.6	-678	45	84
121	VDD2	1525.8	-678	45	84
122	VDD2	1585.8	-678	45	84
123	VDD2	1645.8	-678	45	84
124	VDD2	1705.8	-678	45	84
125	VDD2	1765.8	-678	45	84
126	VDD2	1825.8	-678	45	84
127	VDD2	1885.8	-678	45	84
128	VDD2	1945.8	-678	45	84
129	VDD2	2005.8	-678	45	84
130	VDD3	2270.7	-678	45	84
131	VDD3	2330.7	-678	45	84
132	VB0+	2405.2	-678	45	84
133	VB0+	2465.2	-678	45	84
134	VB0+	2525.2	-678	45	84
135	VB0+	2585.2	-678	45	84
136	VB0+	2645.2	-678	45	84
137	VB0+	2705.2	-678	45	84
138	VB1+	3045.2	-678	45	84
139	VB1+	3105.2	-678	45	84
140	VB1+	3165.2	-678	45	84
141	VB1+	3225.2	-678	45	84
142	VB1+	3285.2	-678	45	84
143	VB1+	3345.2	-678	45	84
144	VB1-	3405.2	-678	45	84
145	VB1-	3465.2	-678	45	84
146	VB1-	3525.2	-678	45	84
147	VB1-	3585.2	-678	45	84
148	VB1-	3645.2	-678	45	84
149	VB1-	3705.2	-678	45	84
150	VB0-	4045.2	-678	45	84
151	VB0-	4105.2	-678	45	84
152	VB0-	4165.2	-678	45	84
153	VB0-	4225.2	-678	45	84
154	VB0-	4285.2	-678	45	84
155	VB0-	4345.2	-678	45	84
156	VS-	4419.7	-678	45	84
157	VS-	4635.8	-678	45	84
158	VS-	4852.0	-678	45	84
159	VS+	5068.1	-678	45	84
160	VS+	5284.3	-678	45	84
161	VS+	5500.4	-678	45	84
162	VLCDIN	5840.4	-678	45	84
163	VLCDIN	5900.4	-678	45	84

#	Pad	X	Y	W	H
164	VLCDOUT	5960.4	-678	45	84
165	VLCDOUT	6020.4	-678	45	84
166	COM129	6404.8	-662	17	118
167	COM127	6435.8	-662	17	118
168	COM125	6466.8	-662	17	118
169	COM123	6497.8	-662	17	118
170	COM121	6528.8	-662	17	118
171	DUMMY	6646.5	-707	118	27
172	COM119	6646.5	-671	118	17
173	COM117	6646.5	-640	118	17
174	COM115	6646.5	-609	118	17
175	COM113	6646.5	-578	118	17
176	COM111	6646.5	-547	118	17
177	COM109	6646.5	-516	118	17
178	COM107	6646.5	-485	118	17
179	COM105	6646.5	-454	118	17
180	COM103	6646.5	-423	118	17
181	COM101	6646.5	-392	118	17
182	COM99	6646.5	-361	118	17
183	COM97	6646.5	-330	118	17
184	COM95	6646.5	-299	118	17
185	COM93	6646.5	-268	118	17
186	COM91	6646.5	-237	118	17
187	COM89	6646.5	-206	118	17
188	COM87	6646.5	-175	118	17
189	COM85	6646.5	-144	118	17
190	COM83	6646.5	-113	118	17
191	COM81	6646.5	-82	118	17
192	COM79	6646.5	-51	118	17
193	COM77	6646.5	-20	118	17
194	COM75	6646.5	11	118	17
195	COM73	6646.5	42	118	17
196	COM71	6646.5	73	118	17
197	COM69	6646.5	104	118	17
198	COM67	6646.5	135	118	17
199	COM65	6646.5	166	118	17
200	COM63	6646.5	197	118	17
201	COM61	6646.5	228	118	17
202	COM59	6646.5	259	118	17
203	COM57	6646.5	290	118	17
204	COM55	6646.5	321	118	17
205	COM53	6646.5	352	118	17
206	COM51	6646.5	383	118	17
207	COM49	6646.5	414	118	17
208	COM47	6646.5	445	118	17
209	COM45	6646.5	476	118	17
210	COM43	6646.5	507	118	17
211	COM41	6646.5	538	118	17
212	COM39	6646.5	569	118	17
213	COM37	6646.5	600	118	17
214	COM35	6646.5	631	118	17
215	COM33	6646.5	662	118	17
216	DUMMY	6646.5	702.5	118	36
217	COM31	6525.5	665	17	118
218	COM29	6494.5	665	17	118

#	Pad	X	Y	W	H
219	COM27	6463.5	665	17	118
220	COM25	6432.5	665	17	118
221	COM23	6401.5	665	17	118
222	COM21	6370.5	665	17	118
223	COM19	6339.5	665	17	118
224	COM17	6308.5	665	17	118
225	COM15	6277.5	665	17	118
226	COM13	6246.5	665	17	118
227	COM11	6215.5	665	17	118
228	COM9	6184.5	665	17	118
229	COM7	6153.5	665	17	118
230	COM5	6122.5	665	17	118
231	COM3	6091.5	665	17	118
232	COM1	6060.5	665	17	118
233	SEG1	6029.5	665	17	118
234	SEG2	5998.5	665	17	118
235	SEG3	5967.5	665	17	118
236	SEG4	5936.5	665	17	118
237	SEG5	5905.5	665	17	118
238	SEG6	5874.5	665	17	118
239	SEG7	5843.5	665	17	118
240	SEG8	5812.5	665	17	118
241	SEG9	5781.5	665	17	118
242	SEG10	5750.5	665	17	118
243	SEG11	5719.5	665	17	118
244	SEG12	5688.5	665	17	118
245	SEG13	5657.5	665	17	118
246	SEG14	5626.5	665	17	118
247	SEG15	5595.5	665	17	118
248	SEG16	5564.5	665	17	118
249	SEG17	5533.5	665	17	118
250	SEG18	5502.5	665	17	118
251	SEG19	5471.5	665	17	118
252	SEG20	5440.5	665	17	118
253	SEG21	5409.5	665	17	118
254	SEG22	5378.5	665	17	118
255	SEG23	5347.5	665	17	118
256	SEG24	5316.5	665	17	118
257	SEG25	5285.5	665	17	118
258	SEG26	5254.5	665	17	118
259	SEG27	5223.5	665	17	118
260	SEG28	5192.5	665	17	118
261	SEG29	5161.5	665	17	118
262	SEG30	5130.5	665	17	118
263	SEG31	5099.5	665	17	118
264	SEG32	5068.5	665	17	118
265	SEG33	5037.5	665	17	118
266	SEG34	5006.5	665	17	118
267	SEG35	4975.5	665	17	118
268	SEG36	4944.5	665	17	118
269	SEG37	4913.5	665	17	118
270	SEG38	4882.5	665	17	118
271	SEG39	4851.5	665	17	118
272	SEG40	4820.5	665	17	118
273	SEG41	4789.5	665	17	118

#	Pad	X	Y	W	H
274	SEG42	4758.5	665	17	118
275	SEG43	4727.5	665	17	118
276	SEG44	4696.5	665	17	118
277	SEG45	4665.5	665	17	118
278	SEG46	4634.5	665	17	118
279	SEG47	4603.5	665	17	118
280	SEG48	4572.5	665	17	118
281	SEG49	4541.5	665	17	118
282	SEG50	4510.5	665	17	118
283	SEG51	4479.5	665	17	118
284	SEG52	4448.5	665	17	118
285	SEG53	4417.5	665	17	118
286	SEG54	4386.5	665	17	118
287	SEG55	4355.5	665	17	118
288	SEG56	4324.5	665	17	118
289	SEG57	4293.5	665	17	118
290	SEG58	4262.5	665	17	118
291	SEG59	4231.5	665	17	118
292	SEG60	4200.5	665	17	118
293	SEG61	4169.5	665	17	118
294	SEG62	4138.5	665	17	118
295	SEG63	4107.5	665	17	118
296	SEG64	4076.5	665	17	118
297	SEG65	4045.5	665	17	118
298	SEG66	4014.5	665	17	118
299	SEG67	3983.5	665	17	118
300	SEG68	3952.5	665	17	118
301	SEG69	3921.5	665	17	118
302	SEG70	3890.5	665	17	118
303	SEG71	3859.5	665	17	118
304	SEG72	3828.5	665	17	118
305	SEG73	3797.5	665	17	118
306	SEG74	3766.5	665	17	118
307	SEG75	3735.5	665	17	118
308	SEG76	3704.5	665	17	118
309	SEG77	3673.5	665	17	118
310	SEG78	3642.5	665	17	118
311	SEG79	3611.5	665	17	118
312	SEG80	3580.5	665	17	118
313	SEG81	3549.5	665	17	118
314	SEG82	3518.5	665	17	118
315	SEG83	3487.5	665	17	118
316	SEG84	3456.5	665	17	118
317	SEG85	3425.5	665	17	118
318	SEG86	3394.5	665	17	118
319	SEG87	3363.5	665	17	118
320	SEG88	3332.5	665	17	118
321	SEG89	3301.5	665	17	118
322	SEG90	3270.5	665	17	118
323	SEG91	3239.5	665	17	118
324	SEG92	3208.5	665	17	118
325	SEG93	3177.5	665	17	118
326	SEG94	3146.5	665	17	118
327	SEG95	3115.5	665	17	118
328	SEG96	3084.5	665	17	118

#	Pad	X	Y	W	H
329	SEG97	3053.5	665	17	118
330	SEG98	3022.5	665	17	118
331	SEG99	2991.5	665	17	118
332	SEG100	2960.5	665	17	118
333	SEG101	2929.5	665	17	118
334	SEG102	2898.5	665	17	118
335	SEG103	2867.5	665	17	118
336	SEG104	2836.5	665	17	118
337	SEG105	2805.5	665	17	118
338	SEG106	2774.5	665	17	118
339	SEG107	2743.5	665	17	118
340	SEG108	2712.5	665	17	118
341	SEG109	2681.5	665	17	118
342	SEG110	2650.5	665	17	118
343	SEG111	2619.5	665	17	118
344	SEG112	2588.5	665	17	118
345	SEG113	2557.5	665	17	118
346	SEG114	2526.5	665	17	118
347	SEG115	2495.5	665	17	118
348	SEG116	2464.5	665	17	118
349	SEG117	2433.5	665	17	118
350	SEG118	2402.5	665	17	118
351	SEG119	2371.5	665	17	118
352	SEG120	2340.5	665	17	118
353	SEG121	2309.5	665	17	118
354	SEG122	2278.5	665	17	118
355	SEG123	2247.5	665	17	118
356	SEG124	2216.5	665	17	118
357	SEG125	2185.5	665	17	118
358	SEG126	2154.5	665	17	118
359	SEG127	2123.5	665	17	118
360	SEG128	2092.5	665	17	118
361	SEG129	2061.5	665	17	118
362	SEG130	2030.5	665	17	118
363	SEG131	1999.5	665	17	118
364	SEG132	1968.5	665	17	118
365	SEG133	1937.5	665	17	118
366	SEG134	1906.5	665	17	118
367	SEG135	1875.5	665	17	118
368	SEG136	1844.5	665	17	118
369	SEG137	1813.5	665	17	118
370	SEG138	1782.5	665	17	118
371	SEG139	1751.5	665	17	118
372	SEG140	1720.5	665	17	118
373	SEG141	1689.5	665	17	118
374	SEG142	1658.5	665	17	118
375	SEG143	1627.5	665	17	118
376	SEG144	1596.5	665	17	118
377	SEG145	1565.5	665	17	118
378	SEG146	1534.5	665	17	118
379	SEG147	1503.5	665	17	118
380	SEG148	1472.5	665	17	118
381	SEG149	1441.5	665	17	118
382	SEG150	1410.5	665	17	118
383	SEG151	1379.5	665	17	118

#	Pad	X	Y	W	H
384	SEG152	1348.5	665	17	118
385	SEG153	1317.5	665	17	118
386	SEG154	1286.5	665	17	118
387	SEG155	1255.5	665	17	118
388	SEG156	1224.5	665	17	118
389	SEG157	1193.5	665	17	118
390	SEG158	1162.5	665	17	118
391	SEG159	1131.5	665	17	118
392	SEG160	1100.5	665	17	118
393	SEG161	1069.5	665	17	118
394	SEG162	1038.5	665	17	118
395	SEG163	1007.5	665	17	118
396	SEG164	976.5	665	17	118
397	SEG165	945.5	665	17	118
398	SEG166	914.5	665	17	118
399	SEG167	883.5	665	17	118
400	SEG168	852.5	665	17	118
401	SEG169	821.5	665	17	118
402	SEG170	790.5	665	17	118
403	SEG171	759.5	665	17	118
404	SEG172	728.5	665	17	118
405	SEG173	697.5	665	17	118
406	SEG174	666.5	665	17	118
407	SEG175	635.5	665	17	118
408	SEG176	604.5	665	17	118
409	SEG177	573.5	665	17	118
410	SEG178	542.5	665	17	118
411	SEG179	511.5	665	17	118
412	SEG180	480.5	665	17	118
413	SEG181	449.5	665	17	118
414	SEG182	418.5	665	17	118
415	SEG183	387.5	665	17	118
416	SEG184	356.5	665	17	118
417	SEG185	325.5	665	17	118
418	SEG186	294.5	665	17	118
419	SEG187	263.5	665	17	118
420	SEG188	232.5	665	17	118
421	SEG189	201.5	665	17	118
422	SEG190	170.5	665	17	118
423	SEG191	139.5	665	17	118
424	SEG192	108.5	665	17	118
425	SEG193	77.5	665	17	118
426	SEG194	46.5	665	17	118
427	SEG195	15.5	665	17	118
428	SEG196	-15.5	665	17	118
429	SEG197	-46.5	665	17	118
430	SEG198	-77.5	665	17	118
431	SEG199	-108.5	665	17	118
432	SEG200	-139.5	665	17	118
433	SEG201	-170.5	665	17	118
434	SEG202	-201.5	665	17	118
435	SEG203	-232.5	665	17	118
436	SEG204	-263.5	665	17	118
437	SEG205	-294.5	665	17	118
438	SEG206	-325.5	665	17	118

#	Pad	X	Y	W	H
439	SEG207	-356.5	665	17	118
440	SEG208	-387.5	665	17	118
441	SEG209	-418.5	665	17	118
442	SEG210	-449.5	665	17	118
443	SEG211	-480.5	665	17	118
444	SEG212	-511.5	665	17	118
445	SEG213	-542.5	665	17	118
446	SEG214	-573.5	665	17	118
447	SEG215	-604.5	665	17	118
448	SEG216	-635.5	665	17	118
449	SEG217	-666.5	665	17	118
450	SEG218	-697.5	665	17	118
451	SEG219	-728.5	665	17	118
452	SEG220	-759.5	665	17	118
453	SEG221	-790.5	665	17	118
454	SEG222	-821.5	665	17	118
455	SEG223	-852.5	665	17	118
456	SEG224	-883.5	665	17	118
457	SEG225	-914.5	665	17	118
458	SEG226	-945.5	665	17	118
459	SEG227	-976.5	665	17	118
460	SEG228	-1007.5	665	17	118
461	SEG229	-1038.5	665	17	118
462	SEG230	-1069.5	665	17	118
463	SEG231	-1100.5	665	17	118
464	SEG232	-1131.5	665	17	118
465	SEG233	-1162.5	665	17	118
466	SEG234	-1193.5	665	17	118
467	SEG235	-1224.5	665	17	118
468	SEG236	-1255.5	665	17	118
469	SEG237	-1286.5	665	17	118
470	SEG238	-1317.5	665	17	118
471	SEG239	-1348.5	665	17	118
472	SEG240	-1379.5	665	17	118
473	SEG241	-1410.5	665	17	118
474	SEG242	-1441.5	665	17	118
475	SEG243	-1472.5	665	17	118
476	SEG244	-1503.5	665	17	118
477	SEG245	-1534.5	665	17	118
478	SEG246	-1565.5	665	17	118
479	SEG247	-1596.5	665	17	118
480	SEG248	-1627.5	665	17	118
481	SEG249	-1658.5	665	17	118
482	SEG250	-1689.5	665	17	118
483	SEG251	-1720.5	665	17	118
484	SEG252	-1751.5	665	17	118
485	SEG253	-1782.5	665	17	118
486	SEG254	-1813.5	665	17	118
487	SEG255	-1844.5	665	17	118
488	SEG256	-1875.5	665	17	118
489	SEG257	-1906.5	665	17	118
490	SEG258	-1937.5	665	17	118
491	SEG259	-1968.5	665	17	118
492	SEG260	-1999.5	665	17	118
493	SEG261	-2030.5	665	17	118

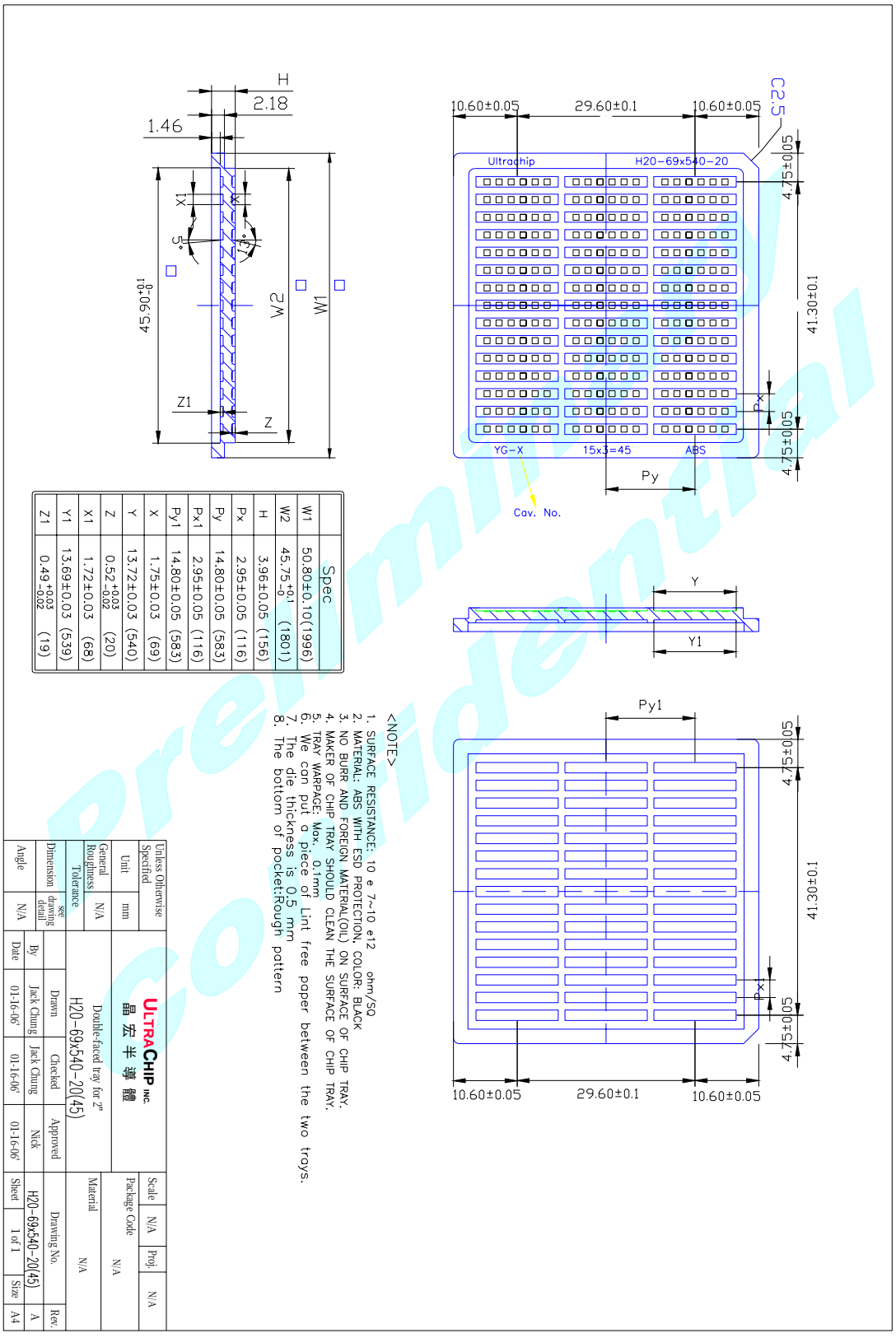
#	Pad	X	Y	W	H
494	SEG262	-2061.5	665	17	118
495	SEG263	-2092.5	665	17	118
496	SEG264	-2123.5	665	17	118
497	SEG265	-2154.5	665	17	118
498	SEG266	-2185.5	665	17	118
499	SEG267	-2216.5	665	17	118
500	SEG268	-2247.5	665	17	118
501	SEG269	-2278.5	665	17	118
502	SEG270	-2309.5	665	17	118
503	SEG271	-2340.5	665	17	118
504	SEG272	-2371.5	665	17	118
505	SEG273	-2402.5	665	17	118
506	SEG274	-2433.5	665	17	118
507	SEG275	-2464.5	665	17	118
508	SEG276	-2495.5	665	17	118
509	SEG277	-2526.5	665	17	118
510	SEG278	-2557.5	665	17	118
511	SEG279	-2588.5	665	17	118
512	SEG280	-2619.5	665	17	118
513	SEG281	-2650.5	665	17	118
514	SEG282	-2681.5	665	17	118
515	SEG283	-2712.5	665	17	118
516	SEG284	-2743.5	665	17	118
517	SEG285	-2774.5	665	17	118
518	SEG286	-2805.5	665	17	118
519	SEG287	-2836.5	665	17	118
520	SEG288	-2867.5	665	17	118
521	SEG289	-2898.5	665	17	118
522	SEG290	-2929.5	665	17	118
523	SEG291	-2960.5	665	17	118
524	SEG292	-2991.5	665	17	118
525	SEG293	-3022.5	665	17	118
526	SEG294	-3053.5	665	17	118
527	SEG295	-3084.5	665	17	118
528	SEG296	-3115.5	665	17	118
529	SEG297	-3146.5	665	17	118
530	SEG298	-3177.5	665	17	118
531	SEG299	-3208.5	665	17	118
532	SEG300	-3239.5	665	17	118
533	SEG301	-3270.5	665	17	118
534	SEG302	-3301.5	665	17	118
535	SEG303	-3332.5	665	17	118
536	SEG304	-3363.5	665	17	118
537	SEG305	-3394.5	665	17	118
538	SEG306	-3425.5	665	17	118
539	SEG307	-3456.5	665	17	118
540	SEG308	-3487.5	665	17	118
541	SEG309	-3518.5	665	17	118
542	SEG310	-3549.5	665	17	118
543	SEG311	-3580.5	665	17	118
544	SEG312	-3611.5	665	17	118
545	SEG313	-3642.5	665	17	118
546	SEG314	-3673.5	665	17	118
547	SEG315	-3704.5	665	17	118
548	SEG316	-3735.5	665	17	118

#	Pad	X	Y	W	H
549	SEG317	-3766.5	665	17	118
550	SEG318	-3797.5	665	17	118
551	SEG319	-3828.5	665	17	118
552	SEG320	-3859.5	665	17	118
553	SEG321	-3890.5	665	17	118
554	SEG322	-3921.5	665	17	118
555	SEG323	-3952.5	665	17	118
556	SEG324	-3983.5	665	17	118
557	SEG325	-4014.5	665	17	118
558	SEG326	-4045.5	665	17	118
559	SEG327	-4076.5	665	17	118
560	SEG328	-4107.5	665	17	118
561	SEG329	-4138.5	665	17	118
562	SEG330	-4169.5	665	17	118
563	SEG331	-4200.5	665	17	118
564	SEG332	-4231.5	665	17	118
565	SEG333	-4262.5	665	17	118
566	SEG334	-4293.5	665	17	118
567	SEG335	-4324.5	665	17	118
568	SEG336	-4355.5	665	17	118
569	SEG337	-4386.5	665	17	118
570	SEG338	-4417.5	665	17	118
571	SEG339	-4448.5	665	17	118
572	SEG340	-4479.5	665	17	118
573	SEG341	-4510.5	665	17	118
574	SEG342	-4541.5	665	17	118
575	SEG343	-4572.5	665	17	118
576	SEG344	-4603.5	665	17	118
577	SEG345	-4634.5	665	17	118
578	SEG346	-4665.5	665	17	118
579	SEG347	-4696.5	665	17	118
580	SEG348	-4727.5	665	17	118
581	SEG349	-4758.5	665	17	118
582	SEG350	-4789.5	665	17	118
583	SEG351	-4820.5	665	17	118
584	SEG352	-4851.5	665	17	118
585	SEG353	-4882.5	665	17	118
586	SEG354	-4913.5	665	17	118
587	SEG355	-4944.5	665	17	118
588	SEG356	-4975.5	665	17	118
589	SEG357	-5006.5	665	17	118
590	SEG358	-5037.5	665	17	118
591	SEG359	-5068.5	665	17	118
592	SEG360	-5099.5	665	17	118
593	SEG361	-5130.5	665	17	118
594	SEG362	-5161.5	665	17	118
595	SEG363	-5192.5	665	17	118
596	SEG364	-5223.5	665	17	118
597	SEG365	-5254.5	665	17	118
598	SEG366	-5285.5	665	17	118
599	SEG367	-5316.5	665	17	118
600	SEG368	-5347.5	665	17	118
601	SEG369	-5378.5	665	17	118
602	SEG370	-5409.5	665	17	118
603	SEG371	-5440.5	665	17	118

#	Pad	X	Y	W	H
604	SEG372	-5471.5	665	17	118
605	SEG373	-5502.5	665	17	118
606	SEG374	-5533.5	665	17	118
607	SEG375	-5564.5	665	17	118
608	SEG376	-5595.5	665	17	118
609	SEG377	-5626.5	665	17	118
610	SEG378	-5657.5	665	17	118
611	SEG379	-5688.5	665	17	118
612	SEG380	-5719.5	665	17	118
613	SEG381	-5750.5	665	17	118
614	SEG382	-5781.5	665	17	118
615	SEG383	-5812.5	665	17	118
616	SEG384	-5843.5	665	17	118
617	SEG385	-5874.5	665	17	118
618	SEG386	-5905.5	665	17	118
619	SEG387	-5936.5	665	17	118
620	SEG388	-5967.5	665	17	118
621	SEG389	-5998.5	665	17	118
622	SEG390	-6029.5	665	17	118
623	COM2	-6060.5	665	17	118
624	COM4	-6091.5	665	17	118
625	COM6	-6122.5	665	17	118
626	COM8	-6153.5	665	17	118
627	COM10	-6184.5	665	17	118
628	COM12	-6215.5	665	17	118
629	COM14	-6246.5	665	17	118
630	COM16	-6277.5	665	17	118
631	COM18	-6308.5	665	17	118
632	COM20	-6339.5	665	17	118
633	COM22	-6370.5	665	17	118
634	COM24	-6401.5	665	17	118
635	COM26	-6432.5	665	17	118
636	COM28	-6463.5	665	17	118
637	COM30	-6494.5	665	17	118
638	COM32	-6525.5	665	17	118

(The values of the x-coordinate and the y-coordinate in the table are after-rounded.)

TRAY INFORMATION



	Spec
W1	50.80±0.10(1996)
W2	45.75 +0.1 -0 (1801)
H	3.96±0.05 (156)
Px	2.95±0.05 (116)
Py	14.80±0.05 (583)
Px1	2.95±0.05 (116)
Py1	14.80±0.05 (583)
X	1.75±0.03 (69)
Y	13.72±0.03 (540)
Z	0.52 +0.03 -0.02 (20)
X1	1.72±0.03 (68)
Y1	13.69±0.03 (539)
Z1	0.49 +0.03 -0.02 (19)

Unless Otherwise Specified		ULTRACHIP INC. 晶宏半導體						Scale	N/A
Unit	mm	Double-faced tray for 2" H20-69x540-20(45)					Package Code	Proj	
General Roughness	N/A						N/A	N/A	
Tolerance									
Dimension	see drawing detail						Material	Drawing No.	Rev.
Angle	N/A						N/A	H20-69x540-20(45)	A
	By	Date	Drawn	Checked	Approved			Sheet	Size
		01-16-06'	Jack Chung	Jack Chung	Nick			1 of 1	A4