HIGH-VOLTAGE MIXED-SIGNAL IC

UC1697a

128 x 128RGB C-STN LCD Controller-Driver
w/ 8-bit per RGB On-Chip SRAM

MP Specifications
Revision 1.0

August 24, 2009

ULTRACHIP

The Coolest LCD Drive, Ever!!

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UC1697a

Single-Chip, Ultra-Low Power
128COM x 128RGB Matrix
Passive Color LCD Controller-Driver

INTRODUCTION

UC1697a is an advanced high-voltage mixed-signal CMOS IC, specially designed for the display needs of low power hand-held devices.

In addition to low power COM and SEG drivers, UC1697a contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation, and graphics data memory.

UC1697a employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and LRM (Line Rate Modulation) gray-shade modulation scheme to achieve well balanced shading, vivid colors, and natural-looking images.

With UC1697a, LCD makers can now achieve TFT-like image quality, while maintaining the same STN advantages in power consumption, unit cost, ease of customization and production flexibility.

MAIN APPLICATIONS

- Cellular Phones and other battery operated hand held devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 128x128 matrix C-STN LCD with comprehensive support for input format and color depth:
  - 8-bit RGB: 256-color
  - 12-bit RGB: 4K-color
  - 16-bit RGB: 64K-color
- A software-readable ID bit (ID0) to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 4-wire, 3-wire serial bus (S8, S9) and 8-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable temperature compensation coefficients.
- Software programmable, self-configuring 11x charge pump.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Pad layouts support COG applications.
- V_{DD} (digital) range (Typ.) : 1.8V ~ 3.3V
  V_{DD} (analog) range (Typ.) : 2.6V ~ 3.3V
  LCD V_{OP} range: 6.1V ~ 16.5V
- Available MTP trimming supports precise LCD contrast matching.
- Available in gold bump dies.

  COM/SEG bump information
  - Bump pitch: 23 μM
  - Bump gap: 11 μM
  - Bump surface: 1800 μM^2

ORDERING INFORMATION

GOLD BUMPED DIE

Part Number	MTP	I^2C	Description
UC1697aGAA-U2P	Yes	No	Gold bumped die, with MTP function.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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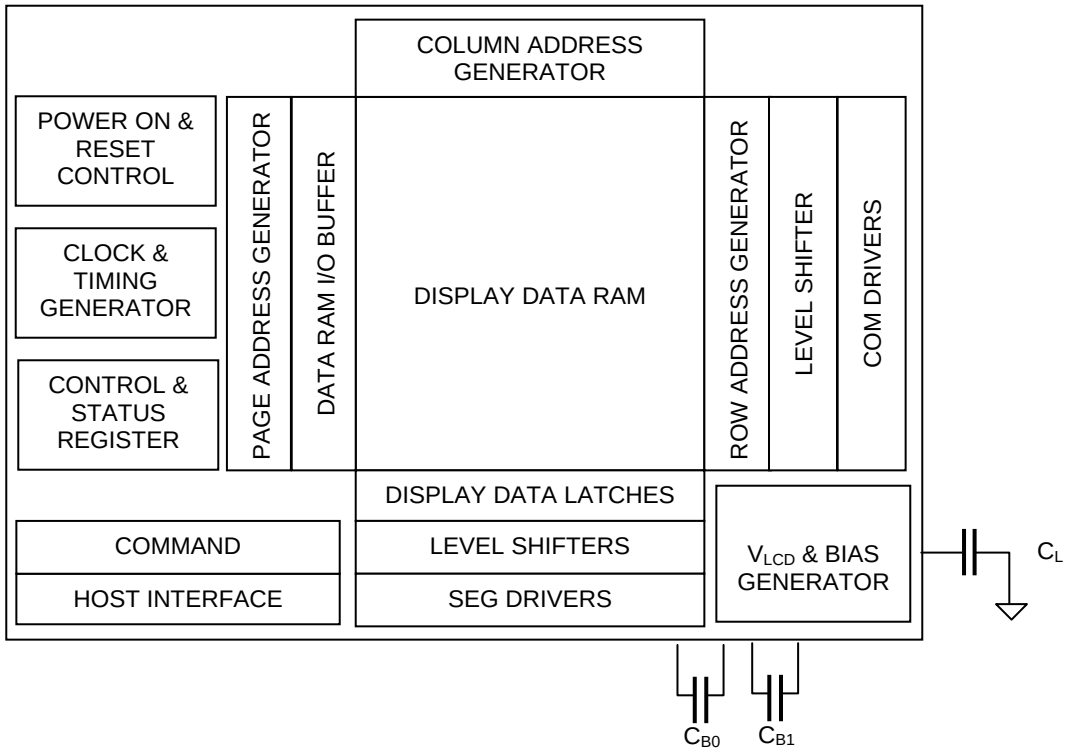
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	# of Pads	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	10 9 3	V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	13 13	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} , V_{B1-} V_{B0+} , V_{B0-}	PWR	3, 3 3, 3	LCD SEG driving voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect a capacitor, C_{BX}, between V_{BX+} and V_{BX-} . The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCD-IN} $V_{LCD-OUT}$	PWR	1 1	High voltage LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open. Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance under 30 Ω.

NOTE

- Recommended capacitor values:
  C_{Bx} : 2.2µF/5V or 100~250 x LCD load capacitance.
  C_L : 330nF (25V) is appropriate for most applications.

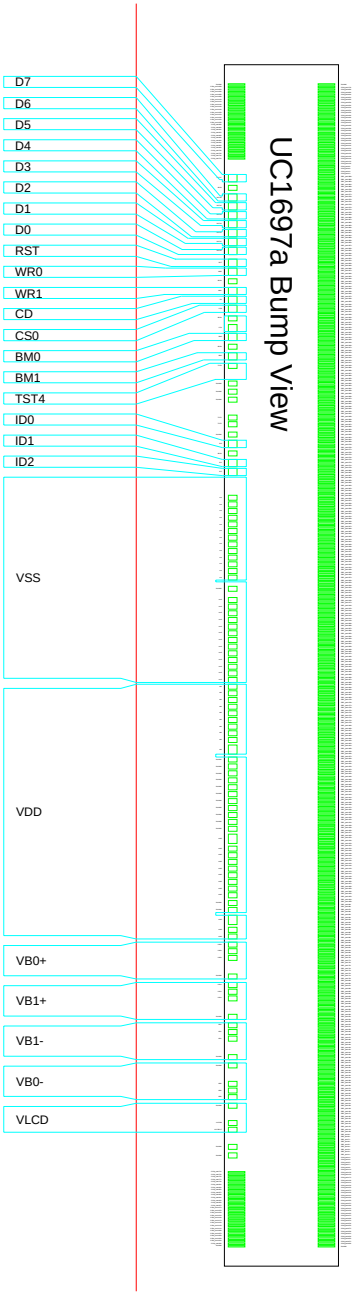
<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] with the following relationship:
<table>
<tr><th>BM[1:0]</th><th>Mode</th></tr>
<tr><td>00</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>3-wire SPI w/ 9-bit token
(S9: conventional)</td></tr>
<tr><td>11</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
</table></td></tr>
<tr><td>CS0
CS1</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. In S9, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID0
ID1</td><td>I</td><td>1
1</td><td>Used for production control.
Connect ID0 to V_{DD} for “H” or V_{SS} for “L”.
The wiring status of ID1/ID0 is available with PID[1:0] of the <code>Get Status</code> command.</td></tr>
<tr><td>ID2</td><td>I</td><td>1</td><td>Used for Power-On Reset control.
Connect ID2 to V_{DD} for “H” or V_{SS} for “L”.
”L” : Power-On Reset Enabled ”H”: Power-On Reset Disabled
The wiring status of ID2 is available with PID[2] of the <code>Get Status</code> command.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td colspan="4">DATA BUS</td></tr>
<tr><td>D7~D0</td><td>I/O</td><td>8</td><td>Bi-directional bus for parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA.
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>BM=0x (8-bit)</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td></tr>
<tr><td>BM=10 (S9)</td><td>–</td><td>–</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
<tr><td>BM=11 (S8)</td><td>–</td><td>–</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
</table>

Name	Type	# of Pads	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG384	HV	384	SEG (column) driver outputs. Support up to 128xRGB pixels. Leave unused SEG drivers open-circuit.
COM1 ~ COM128	HV	128	COM (row) driver outputs. Support up to 128 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 128, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 128] open-circuit.
MISC. PINS			
V_{DDX}	O	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus within the IC. These pads are provided to facilitate chip configurations in COG application. These pins should *NOT* be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I	1	TST4 is used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.
TST1 TST2	O	1 1	Test I/O pins. Leave these pins open during normal use.
Dummy		29	Dummy pins are *NOT* connected inside the IC.

NOTE:

Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~127 for COM and 0~383 for SEG.

RECOMMENDED COG LAYOUT



Note for V_{DD} and V_{SS} with COG:

The operation condition V_{DD}=1.8V (typical) must be satisfied under all operating conditions. With its high speed data-write condition, UC1697a's peak current (I_{DD}) can be up to ~15mA range during high speed data write to UC1697a's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD}, V_{SS} ITO trances in COG glass modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1697a contains registers which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, starting with a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (127 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The top FLTx2 and bottom FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	7	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	3	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 000b : 6 001b : 10 010b : 11 **011b : 12** 100b : 9
TC	2	0H	Temperature Compensation (per ^{o}C) **00b : -0.00%** 01b : -0.10% 10b : -0.15% 11b : -0.05%
PM	8	5CH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	6	00H	PM offset. PMO[5]=1: The effective PM value, PMV = PM - PMO[4:0] PMO[5]=0: The effective PM value, PMV = PM + PMO[4:0]
PC	4	EH	Power Control. PC[1:0] : 0xb: LCD: ⩽ 13nF **1xb: 13 < LCD < 22nF** PC[3:2] : 00b: External V_{LCD} **11b: Internal V_{LCD} (11x charge pump)**
AC	4	1H	Address Control: AC[0] : WA: Automatic column/row Wrap Around (**1 : ON**) AC[1] : Auto-Increment order **0 : Column (CA) first** 1 : Row (RA) first AC[2] : RID: RA (row address) auto increment direction (**0 : +1** 1 : -1) AC[3] : Window Program Mode **0 : Inside Mode:** Write to SRAM within the window defined by (WPC0, WPP0), (WPC1, WPP1) 1 : Outside Mode: Write to SRAM but skip the window defined by (WPC0, WPP0), (WPC1, WPP1)

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>DC</td><td>5</td><td>18H</td><td>Display Control:
DC[0] : PXV: Pixels Inverse. Bit-wise data inversion. (Default 0: OFF)
DC[1] : APO: All Pixels ON (Default 0: OFF)
DC[2] : Display ON/OFF (Default 0: OFF)
When DC[2] is set to 0, the IC will enter Sleep mode.
DC[3] : Gray-shade Modulation mode.
0 : On/Off mode
1 : 32-shade Mode
DC[4] : Green Enhance Mode. Only valid in 4K-color mode.
0 : Enable. Allows an extra display bit for green color.
1 : Disable</td></tr>
<tr><td>LGS</td><td>2</td><td>0H</td><td>LGS[0] : 4/8 Gray-shade ON/OFF. (Default 0: OFF)
LGS[1] : Gray-shade Modulation mode.
0 : 4-shade Mode 1 : 8-shade Mode</td></tr>
<tr><td>LC</td><td>10</td><td>090H</td><td>LCD Control:
LC[0] : Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default 0: OFF).
LC[1] : MX, Mirror X. SEG/Column sequence inversion (Default: 0: OFF)
LC[2] : MY, Mirror Y. COM/Row sequence inversion (Default: 0: OFF)
LC[4:3] : Line Rate
<table>
<tr><th>LC[4:3]</th><th>32-shade</th><th>8-shade</th><th>4-shade</th><th>On/Off mode</th></tr>
<tr><td>00b</td><td>20.1Klps</td><td>12.7</td><td>17.2</td><td>5.5</td></tr>
<tr><td>01b</td><td>24.4</td><td>15.4</td><td>20.9</td><td>6.6</td></tr>
<tr><td>10b</td><td>29.6</td><td>18.6</td><td>25.3</td><td>8.0</td></tr>
<tr><td>11b</td><td>35.8</td><td>22.6</td><td>30.7</td><td>9.7</td></tr>
</table>
(Klps : Kilo-Line-per-second)
LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3)
0 : BGR-BGR 1 : RGB-RGB
LC[7:6] : Color and input mode
when DC[4]=1:
00b : 256 color mode 3R-3G-2B (8-bit/RGB)
01b : 4K color mode 4R-4G-4B (12-bit/RGB)
10b : 64K color mode 5R-6G-5B (16-bit/RGB)
when DC[4]=0:
00b : 256 color mode 3R-3G-2B (8-bit/RGB)
01b : 4K color mode 4R-5G-3B (12-bit/RGB)
10b : 64K color mode 5R-6G-5B (16-bit/RGB)
LC[9:8] : Partial Display Control
0xb: Disable Mux-Rate = CEN+1 (DST, DEN not used)
10b: Enabled Mux-Rate = CEN+1
11b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2</td></tr>
<tr><td>NIV</td><td>7</td><td>51H</td><td>N-Line Inversion:
NIV[5:0] :
000000b: Disable
000001b ~ 111111b: 2~ 64 lines (Default: 10001b: 18 lines)
NIV[6] : 0b: no-XOR 1b: XOR</td></tr>
<tr><td>CSF</td><td>2</td><td>0H</td><td>COM Scan Function
CSF[0] : 0b : LRM sequence: AEBCD-AEBCD
1b : LRM sequence: AEBCD-EBCDA
CSF[1] : 0b :FRC Disable
1b : FRC Enable</td></tr>
</table>

Name	Bits	Default	Description
CEN DST DEN	7 7 7	7FH 00H 7FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	7	00H	Window program starting row address. Value range: 0~127.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	7	7FH	Window program ending row address. Value range: 0~127.
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : **Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	6	--	Multiple-Time Programming. For V_{LCD} fine tune.
MTPM	6	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC	2	N/A	Advanced Program Control. (APC1, APC3) For UltraChip only. Please do not use.
LRM	1	1	LRM (Line Rate Modulation) scheme switch 0 : LRM disabled **1 : LRM enabled**
CSC	1	0	COM Scan control **0 : COM Progressive Scan (line by line)** 1 : COM Interlace Scan (every other line)
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
PID	3	PIN	Access the connected status of ID pins.

COMMAND TABLE

The following is a list of host commands supported by UC1697a

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Prod_Code, PID, EF}	Ver: 0 Prod_Code: 5H
		0	1	Ver		PMO[5:0]							
		0	1	Prod_Code				PID[1:0]		PID2	EF		
3.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
4.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
5.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1xb
6.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
7.	Set Adv. Program Ctrl (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 1or 3	N/A
		0	0	#	#	#	#	#	#	#	#		
8.	Set LRM Enable (double-byte command)	0	0	0	0	1	1	0	0	0	0	Set LRM	1b
		0	0	#	1	0	1	1	1	1	1		
9.	Set COM Scan Control (double-byte command)	0	0	0	0	1	1	0	0	1	0	Set CSC	0b
		0	0	#	1	0	1	1	0	0	0		
10.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	0	#	#	#	Set SL[6:4]	0
11.	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	0	#	#	#	Set RA[6:4]	0
12.	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	5CH
		0	0	#	#	#	#	#	#	#	#		
13.	Set LCD Gray Shade (double-byte command)	0	0	1	0	0	0	0	0	1	1	Set LGS[1:0]	0H
		0	0	0	0	1	0	0	1	#	#		
14.	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0xH
15.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
16.	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	00H
		0	0	#	#	#	#	#	#	#	#		
17.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
18.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
19.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
20.	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
21.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
22.	Set Lookup Table	0	0	1	0	1	1	0	0	0	#	Set DC[5]	0b
23.	Set Shade Lookup Table	0	0	1	0	1	1	0	0	1	0	See Appendix Set Shade[S][5:0]	See Appendix
				0	0	S - Shade number							
				-	-	#	#	#	#	#	#		
24.	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	51H
				-	#	#	#	#	#	#	#		
25.	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
26.	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
27.	Set COM Scan Function	0	0	1	1	0	1	1	-	#	#	Set CSF[1:0]	00b
28.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
29.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
30.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
31.	Set LCD Bias Ratio	0	0	1	1	1	0	1	#	#	#	Set BR[2:0]	011b: 12
32.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
33.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
34.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
35.	Set Window Program Starting Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with MTP Commands	Set WPC0	0
36.	Set Window Program Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
37.	Set Window Program Ending Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set WPC1	127
38.	Set Window Program Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
39.	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Inside
40.	Set MTP Operation control	0 0	0 0	1 -	0 -	1 -	1 #	1 #	0 #	0 #	0 #	Set MTPC[4:0]		10H
41.	Set MTP Write Mask	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[5:0]		00H
42.	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
43.	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
44.	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
45.	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A
Serial Read Command (Enabled only in S8/S9 mode)														
46.	Get Status	0	0	1	1	1	1	1	1	1	0	Get status till chip disabled		Ver=0 Prod_Code= 5H
		0	1	GE	MX	MY	WA	DE	WS	MD	MS			
		0	1	Ver		PMO[5:0]								
		0	1	Prod_code				PID[1:0]		PID2	EF			

NOTE:

- All bit patterns other than commands listed above, may result in undefined behavior.
- The interpretation of commands (41)~(45) depends on the setting of register MTPC[3].
  - Commands (42)~(45) are shared with commands (35)~(38). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

UC1697a will convert input RAM data to 16-bit of RGB data. Please refer to command `Set Color Mode` for detail of data-write sequence.

Write Data Byte accesses Display Data RAM based on Page Address (PA) register and Column Address (CA) register. PA and CA can also be programmed directly by issuing `Set Row Address` and `Set Column Address` commands.

(2) GET STATUS & PMO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status & PMO	0	1	GE	MX	MY	WA	DE	WS	MD	MS
	0	1	Ver		PMO[5:0]					
	0	1	Prod_Code[3:0]				PID[1:0]		PID2	EF

Status1 definitions:

GE: Green Enhancing enable flag. Green Enhance Mode is disabled when GE = 1.
MX: Status of register LC[1], mirror X.
MY: Status of register LC[2], mirror Y.
WA: Status of register AC[0]. Automatic column/row wrap around.
DE: Display enable flag. DE=1 when display is enabled
WS: MTP Operation succeeded
MD: MTP Option (1 for MTP version, 0 for non-MTP version)
MS: MTP action status

Status2 definitions:

Ve[1:0]: Version Code. 00 ~ 11b.
PMO[5:0]: PM offset value.

Status3 definitions:

Prod_Code: 0101b (5h)
PID[2:0]: Provide external connection status of ID pins.
EF: ESD Flag. EF=1 when ESD strikes. **Default : 0**

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(3) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	**0**	**0**	**0**	**1**	**0**	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~127**

(4) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b = -0.00%/°C 01b = -0.10%/°C 10b = -0.15%/°C 11b = -0.05%/°C

(5) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition:
0xb: LCD: ≤ 13nF **1xb: LCD: 13~22nF**

(6) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages. Always make sure the IC is in a RESET state before changing PC[3:2] value. Avoid changing PC[3:2] setting when the display is enabled.

Pump control definition:
00b = External V_{LCD} **11b = Internal V_{LCD} (x11)**

(7) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(Double-byte command)	0	0	APC register parameter							

Set APC1[7:0] or APC3[7:0]. ({RR}=01b or 11b). For UltraChip only. Please do NOT use.

(8) SET LRM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LRM	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	LRM	**1**	**0**	**1**	**1**	**1**	**1**	**1**

LRM : Line Rate Modulation scheme switch.

0: LRM disabled **1: LRM enabled**

(9) SET COM SCAN CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CSC	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	CSC	**1**	**0**	**1**	**1**	**0**	**0**	**0**

Set COM Scan Method.

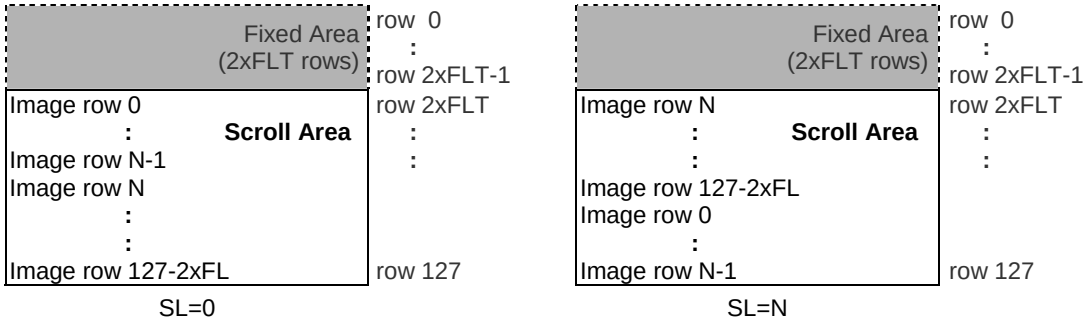
0: COM Progressive Scan (line by line) 1: COM Interlace Scan (every other line)

(10) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	**0**	SL6	SL5	SL4

Set the number of lines for scroll area.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 127-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the `Set Fixed Lines` command.



(11) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address MSB RA [6:4]	0	0	**0**	**1**	**1**	**1**	**0**	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0~127**

(12) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD Voltage Setting* for more detail.

Effective range: **0 ~ 255**

(13) SET LCD GRAY SHADE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	0	0	**0**	**0**	**1**	**0**	**0**	**1**	LGS[1:0]	

This command is used for set the 4/8 Gray-shade select control.

LGS[0] : 4/8 Gray-shade ON/OFF. (Default **0: OFF**)

LGS[1] : Gray-shade Modulation mode.

0 : 4-shade Mode 1 : 8-shade Mode

(14) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to enable partial display function.

LC[9:8] : **0x**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
10b: Enable Partial Display, Mux-Rate = CEN+1
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(15) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

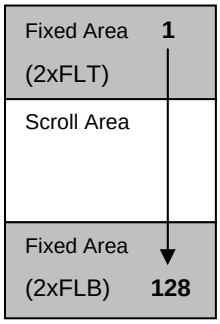
AC[2]: RID, row address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. For Window Program enabling (AC[3]=ON), see section *Command Description* (36) ~ (39) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[3] is.

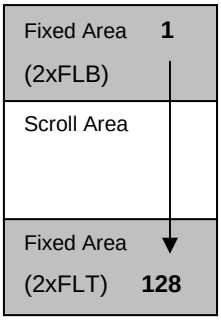
(16) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT, FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0



MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(17) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 87, 65, 44 and 33.

LC[4:3]	32-shade	8-shade	4-shade	On/Off mode
00b	20.1Klps	12.7	17.2	5.5
01b	24.4	15.4	20.9	6.6
10b	**29.6**	**18.6**	**25.3**	**8.0**
11b	35.8	22.6	30.7	9.7

(Klps: Kilo-Line-per-second)

(18) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(19) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

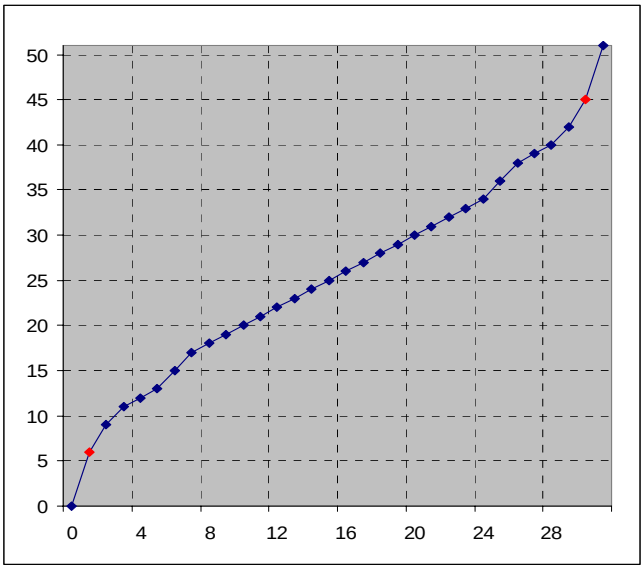
(20) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1697a will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1697a has two gray shade modulation modes: an On/Off mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] Green Enhance Mode. Refer to command `Set Color Mode` for more information.

0b: Green Enhancing Mode enabled **1b: Green Enhancing Mode disabled**

NOTE:

1. For red and blue colors, shades mapped to data 1 and 30 (shown as red points above) are achieved by special dithering. This will be solved when the PWM function is enabled.
2. Green shades are created by combining FRC and special dithering. Six of the shades (1, 2, 3, 59, 60, and 61) are created by special dithering. This will be solved when the PWM function is enabled. Data 62 and 63 are mapped to the same shade.
3. When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1697a for 5~10mS after setting DC[2] to 1.

(21) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] to control COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by the MY action. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether soft icon sections (2xFLT, 2xFLB) are displayed during partial display mode.

(22) SET LOOKUP TABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Lookup Table Enable DC [5]	0	0	**1**	**0**	**1**	**1**	**0**	**0**	**0**	DC5

Lookup Table Control:

DC[5] : **0: Lookup Table disable** 1: Lookup Table enable

(23) SET SHADE LOOKUP TABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Shade Lookup Table Shade[S][5:0] S=0~63	0	0	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**0**
	0	0	**0**	**0**	S					
	0	0	**-**	**-**	Shade[S][5:0]					

S : Shade number. Range : 0~63.

For the setting of Shade0~Shade63, see Appendix.

(24) SET N-LINE INVERSION

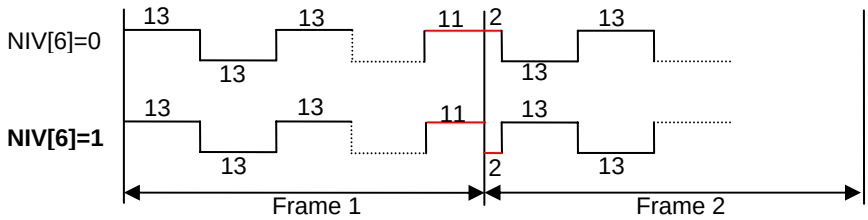
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line Inversion, NIV[6:0] (Double-byte command)	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
	0	0	**-**	NIV6	NIV5	NIV4	NIV3	NIV2	NIV1	NIV0

N-Line Inversion:

NIV[5:0]: 000000b: Disable

000001b ~ 111111b: 2~64 lines (**Default 010001: 18 lines**)

NIV[6]: 0b: non-XOR **1b: XOR**



(25) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	LC5

UC1697a supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG388	SEG389	SEG390
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *Set Color Mode* below.

(26) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Note: *For serial bus modes, please refer to 8-bit tables below.*

Green Enhance Mode disabled (**DC[4] = 1**):

LC[7:6] = 00b (3R-3G-2B, 256-color)
Every 1 byte of RAM is used to store a set of 8-bit input RGB data. No dither is performed.

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R2	R1	R0	G2	G1	G0	B1	B0

LC[7:6] = 01b (4R-4G-4B, 4K-color)
Every 3 bytes of RAM are used to store 2 sets of 12-bit input RGB data. No dither is performed.

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R3	R2	R1	R0	G3	G2	G1	G0
2nd Write Data Cycle	B3	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G3	G2	G1	G0	B3	B2	B1	B0

LC[7:6] = **10b** (5R-6G-5B, 64K-color)
Every 2 bytes of RAM are used to store 1 set of 16-bit input RGB data.

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R4	R3	R2	R1	R0	G5	G4	G3
2nd Write Data Cycle	G2	G1	G0	B4	B3	B2	B1	B0

Green Enhance Mode enabled (DC[4]=0):

LC[7:6] = 00b (3R-3G-2B, 256-color)
The behavior does not change with DC[4] setting.

LC[7:6] = 01b (4R-5G-3B, 4K-color)

Data Write Sequence (8-bit)	***D[7:0]***							
1st Write Data Cycle	R3	R2	R1	R0	G4	G3	G2	G1
2nd Write Data Cycle	G0	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G4	G3	G2	G1	G0	B2	B1	B0

LC[7:6] = 10b (5R-6G-5B, 64K-color)
The behavior does not change with DC[4] setting.

(27) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[2:0]	0	0	**1**	**1**	**0**	**1**	**1**	**-**	CSF1	CSF0

COM scan function

CSF[0]: LRM sequence option

0b: LRM sequence: AEBCD-AEBCD 1b : LRM sequence: AEBCD-EBCDA

CSF[1]: FRC option

0b: FRC Disable 1b: FRC Enable

(28) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(29) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(30) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	TT	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Do *NOT* use.

(31) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [2:0]	0	0	**1**	**1**	**1**	**0**	**1**	BR2	BR1	BR0

Bias ratio definition:

000b = 6 001b = 10 010b = 11 **011b = 12**

100b = 9

***(32)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	**-**	*CEN* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 128 pixel rows, the LCM designer should set CEN to *N-1* (where *N* is the number of pixel rows) and use COM1 through COM-*N* as COM driver electrodes.

***(33)* SET PARTIAL DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	**-**	*DST* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

(34) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	**-**	*DEN* register parameter						

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based indexes of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

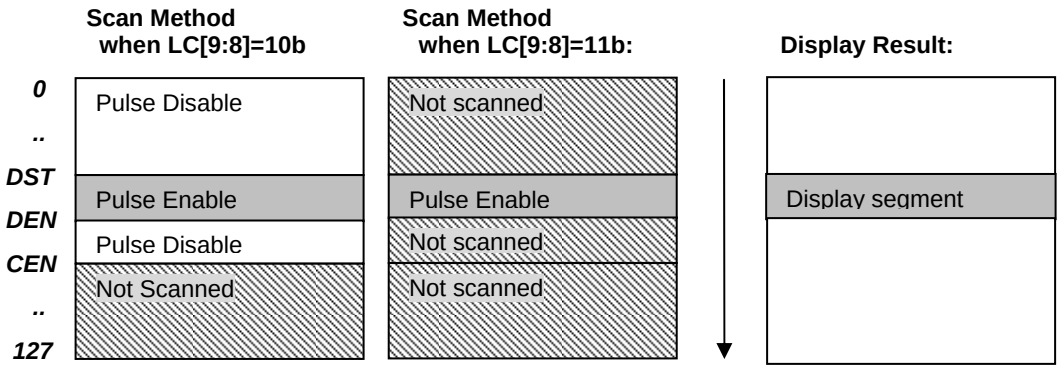
When LC[9]=1, two partial display modes are possible with UC1697a:
LC[8]=1: ON-OFF only, ultra-low-power mode (if Mux-Rate ⩽ 33, set BR=6).
LC[8]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[9:8]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots, for COM electrodes that is outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power can be reduced significantly.

When LC[9:8]=11b, the Mux-Rate is narrowed down DEN-DST +1 + 2x(FLT+FLB)xLC[0]. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be readjusted. When Mux-Rate is under 33, it is recommend to set BR=6.

For minimum power consumption, set LC[9:8]=11b, set (DST, DEN, FL, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On-Off mode, set PC[1:0]=00b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(35) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	**-**	*WPC0* register parameter						

This command is to program the starting column address of RAM program window.

(36) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	**-**	*WPP0* register parameter						

This command is to program the starting row address of RAM program window.

(37) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	**-**	*WPC1* register parameter						

This command is to program the ending column address of RAM program window.

(38) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	**-**	*WPP1* register parameter						

This command is to program the ending row address of RAM program window.

(39) SET WINDOW PROGRAM MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command controls the Window Program function.

AC[3]=0: Inside Mode

When Window Programming is under “Inside” mode , the CA and RA increment and wrap-around will be performed automatically around the boundaries as defined by registers WPC0, WPC1, WPP0, and WPP1, so that the CA/RA address will stay *within* the defined window of SRAM address, and therefore allow effective data update within the window.

AC[3]=1: Outside Mode

When Window Programming is under “Outside” mode, the CA and RA increment and wrap-around boundary will cover the entire UC1697a SRAM map (CA: 0~127, RA:0~127). However, when CA/RA points to a memory location within the window defined by registers WPC0, WPC1, WPP0, and WPP1, the SRAM data update operation will be suspended, the existing data will be retained and the input data will be ignored.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting.

- WA decides whether the program RAM address advances to next row/column after reaching the specified window column / row boundary.
- RID controls the RAM address incrementing from WPP0 toward WPP1 (RID=0) or reverse the direction (RID=1).
- Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0).
- MX results the RAM column address incrementing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the “window”, effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

(40) SET MTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC [4:0] (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	**-**	*MTPC* register parameter				

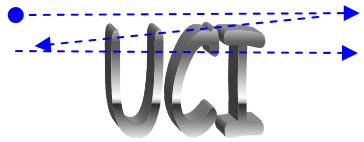
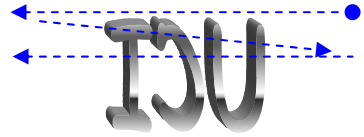
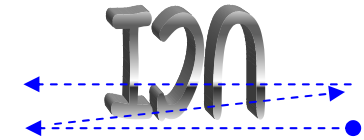
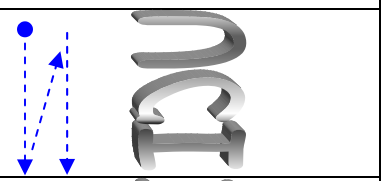
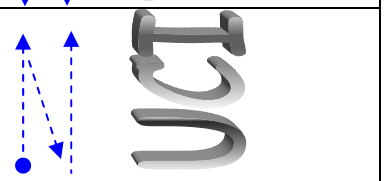
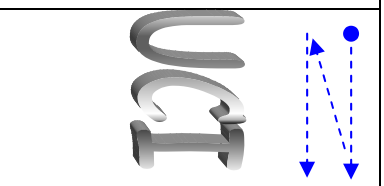
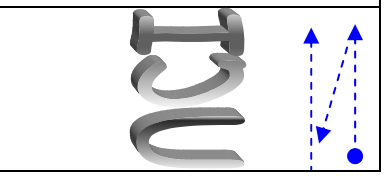
This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Sleep
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

Display Data Direction	Function Setting			Image in Display Data Ram (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]	
Normal	0	0	0	
Y-mirror	0	0	1	
X-mirror	0	1	0	
X-mirror Y-mirror	0	1	1	
X-Y Exchange	1	0	0	
X-Y Exchange Y-mirror	1	0	1	
X-Y Exchange X-mirror	1	1	0	
X-Y Exchange X-mirror Y-mirror	1	1	1	

The following commands, (41) ~ (45), are used as MTP commands only when MTPC[3]=1.

(41) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM [5:0] (Triple-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	**-**	MTPM register parameter					

This command enables Write to each of the individual MTP bits. When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[5:0] : Set PMO value

(42) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{OPT1} setting (with BR=000).

(43) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (with BR=001).

(44) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(45) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

Serial Read Command (Enable only in S8/S9 mode):

(46) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status & PMO	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
	0	1	GE	MX	MY	WA	DE	WS	MD	MS
	0	1	Ver		PMO[5:0]					
	0	1	Prod_Code[3:0]				PID[1:0]		PID2	EF

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1697a via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[9:8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 6, UC1697a can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1697a supports five *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3	4
Bias Ratio	6	10	11	12	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	-0.00	-0.10	-0.15	-0.05

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} AND CONTRAST FINE TUNING

Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. It is very difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to precisely match the actual V_{OP} of each LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH FOR COG

The power supply circuit of UC1697a is designed to handle LCD panels with loading up to ~16nF using 7-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.8V$. For larger LCD panels, use lower resistance ITO glass.

Due to crosstalk consideration, ~16nF is also the recommended maximum LCD panel loading for COG applications. Using 4.5-Ω/Sq low resistance ITO glass for the IC bonding substrate can help improve image quality and operation tolerance.

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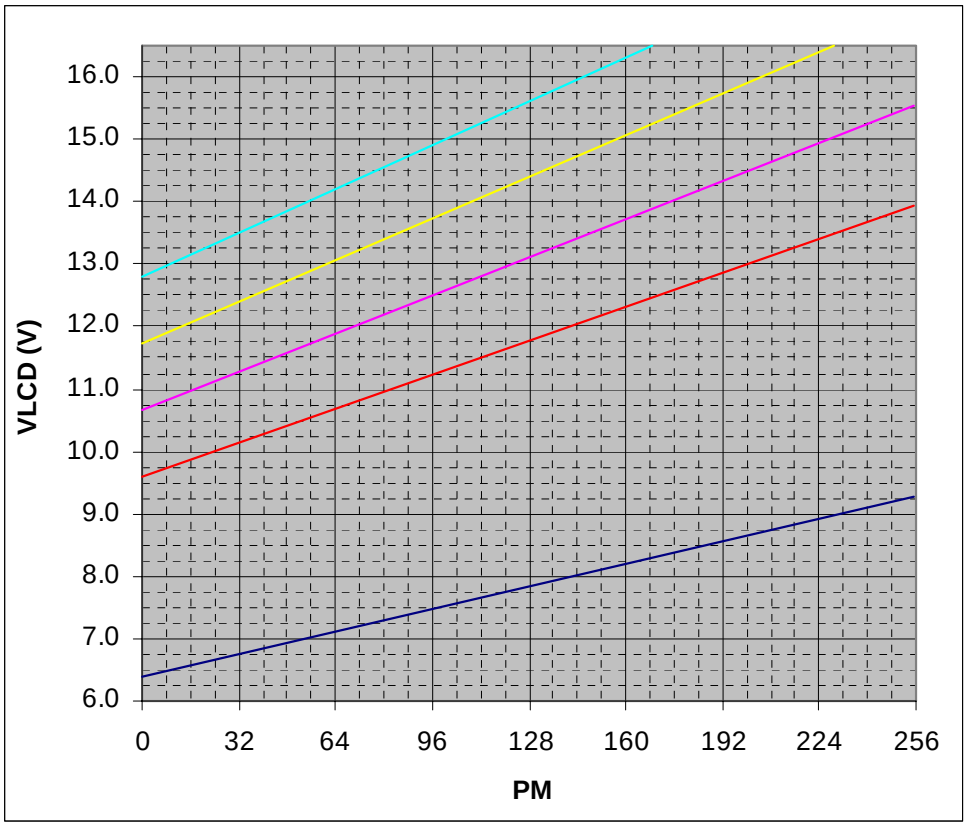
V_{LCD} QUICK REFERENCE



BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
6	6.089	12.49	0	6.09
			255	9.27
10	10.201	20.92	0	10.20
			255	15.54
11	11.232	23.05	0	11.23
			229	16.51
12	12.262	25.16	0	12.26
			169	16.51
9	9.153	18.77	0	9.15
			255	13.94

V_{LCD}-PM-BR relationship at 25°C

NOTE:

1. For good product reliability, please keep V_{LCD} under **16.5V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

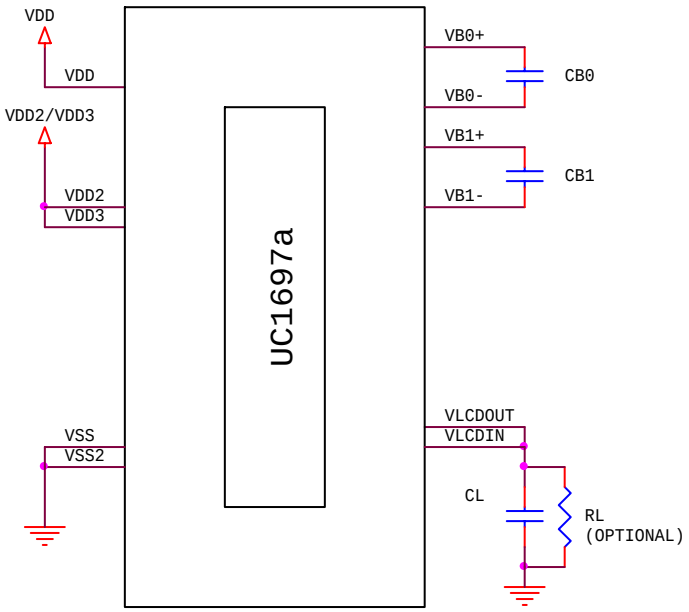


FIGURE 1: Sample circuit using internal Hi-V generator circuit

NOTE:
Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

$C_{B0\sim1}$: 2.2 µF/5V or 100~250 x LCD load capacitance.

C_L : 330 nF (25V) is appropriate for most applications.

R_L : 3.3M ~10 MΩ to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1697a contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 88, frame rate is calculated as:

Line-Rate = Frame Rate x Mux-Rate.

When Mux-Rate is lowered to 87, 65, 44 and 33, line rate will be scaled down automatically by 1.5, 2, 3 and 4 times to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Line rate 30 Klps or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to On/Off mode, line rate will be scaled down automatically by ~30% to reduce power.

Under most situations, flicker behavior is similar between these two modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming convention is COM(*X*), where *X* =1~128, referring to the COM driver for the *X*-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1697a will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1697a will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1697a provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

GRAY-SHADE MODULATION MODE

UC1697a has 4 gray-shade modulation modes: 32-shade, 8-shade, 4-shade, and On/Off mode.

The On/Off mode will consume roughly 40~45% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 32-shade mode.

INPUT COLOR FORMATS

UC1697a supports the following two different input color formats.

256C (8-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 3R-3G-2B format before they are stored to display RAM.

4KC (12-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 5R-6G-5B format before they are stored to display RAM.

64KC (16-bit/RGB): This is the native color mode. Data will be stored directly to on-chip SRAM in 5R-6G-5B (16-bit) format (except shade1 and shade30, which are achieved by special dithering. See command `Set Display Enable` for more details). This is the default input format mode.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can mix several color modes together and switch among them in real time.

For example, the menu portion can be painted in 4K-color mode for fast update speed, and then switch to 64K-color mode, together with window programming function to effectively produce smooth graphics images.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1697a can be as short as 15µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 0.9\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 0.22\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.25\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast and color saturation will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/128	1/12	8.95%	7.2%	6.4%
1/128	1/11	8.85%	7.1%	6.4%

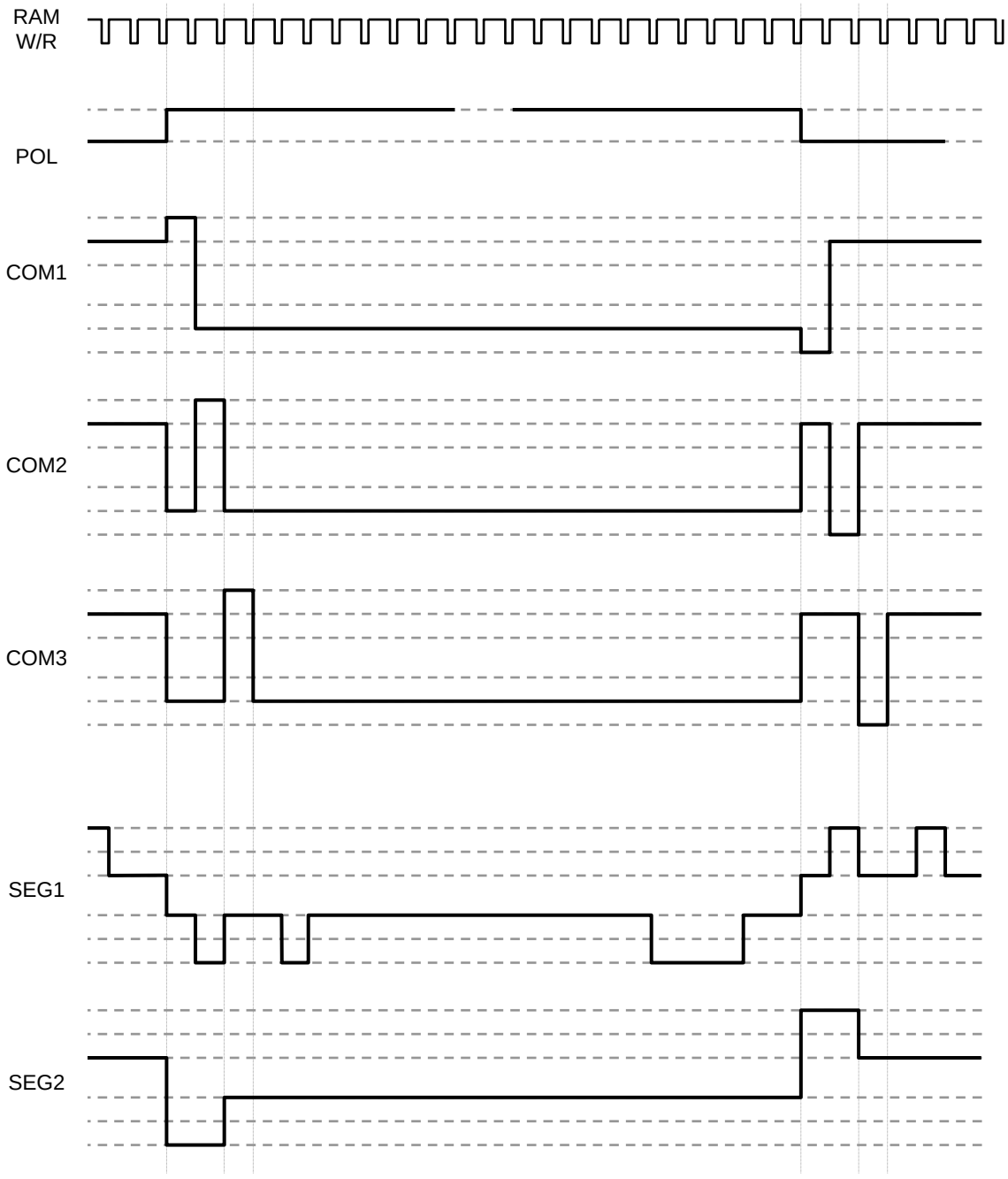


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1697a supports 2 parallel bus protocols (8080 & 6800) in 8-bit bus width, and 2 serial bus protocols (S8 and S9).

Designers can either use parallel buses to achieve high data transfer rate, or use serial buses to create compact LCD modules.

		Bus Type			
		Parallel		Serial	
		8080	6800	S8	S9
Width		8-bit		(4-wire)	(3-wire)
Access		Read / Write			
Control & Data Pins	BM[1:0]	00	01	11	10
	CS[1:0]	Chip Select			
	CD	Control / Data			0
	WR0	$\overline{WR}$	R/$\overline{W}$	0	
	WR1	$\overline{RD}$	EN	0	
	D[7:4, 2:1]	Data	Data	-- (Note)	
	D[3, 0]	Data	Data	D[3]=SDA, D[0]=SCK	

Note: Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Interface	CS Init bus state	CD 1⇔0 Init bus state	CD 1⇨0 Init color mapping	RESET Init bus state	RESET Init color mapping
8-bit	✓	–	–	✓	✓	✓
S8 or S9	✓	✓	–	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS Sync / RESET can be used to initialize bus state machine.
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1697a internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires a dummy read cycle to be performed before the actual data can propagate through the pipe-line and be read from data port D, every time memory address is modified by either *Set CA*, or *Set RA* command.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT BUS OPERATION

UC1697a supports 8-bit bus width.

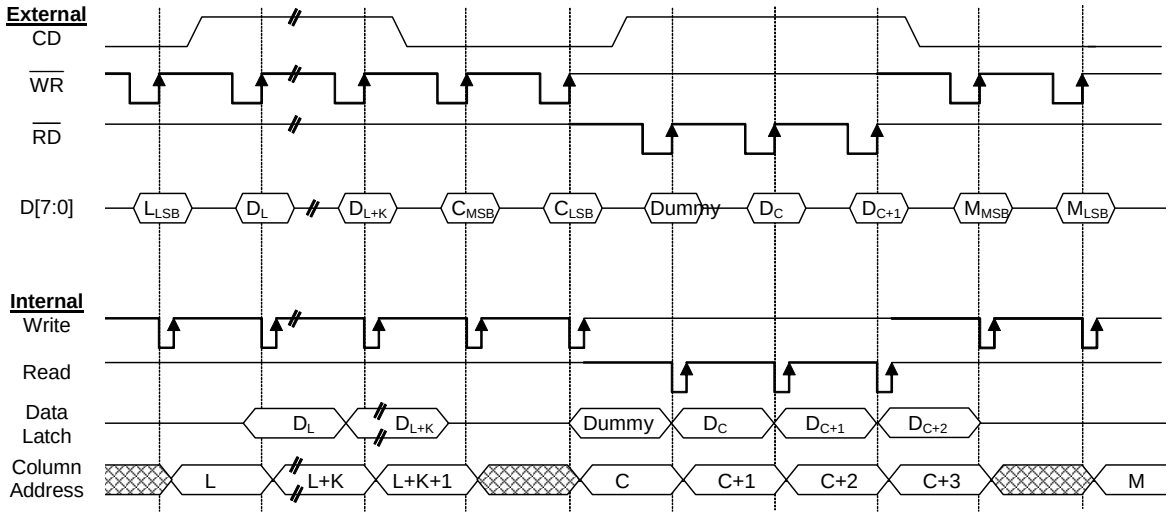


FIGURE 3: 8-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1697a supports 2 serial modes, a 4-wire SPI mode (S8) and a 3-wire mode (S9). Bus interface mode is determined by the wiring of the BM[1:0].

S8 (4-WIRE) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

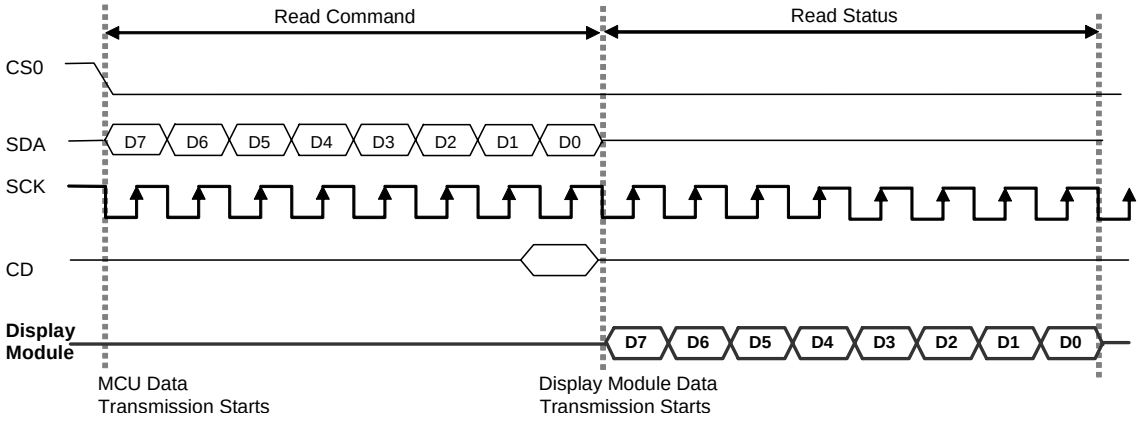


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

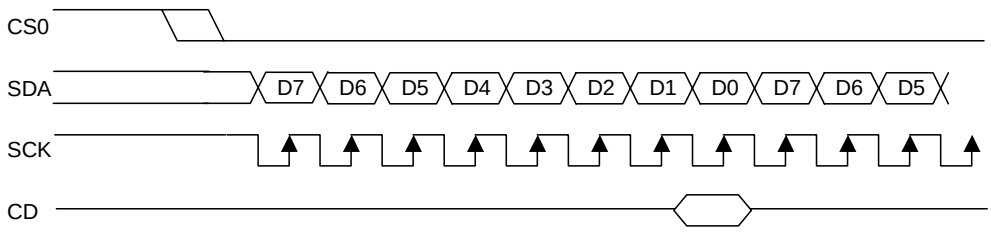


FIGURE 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIRE) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

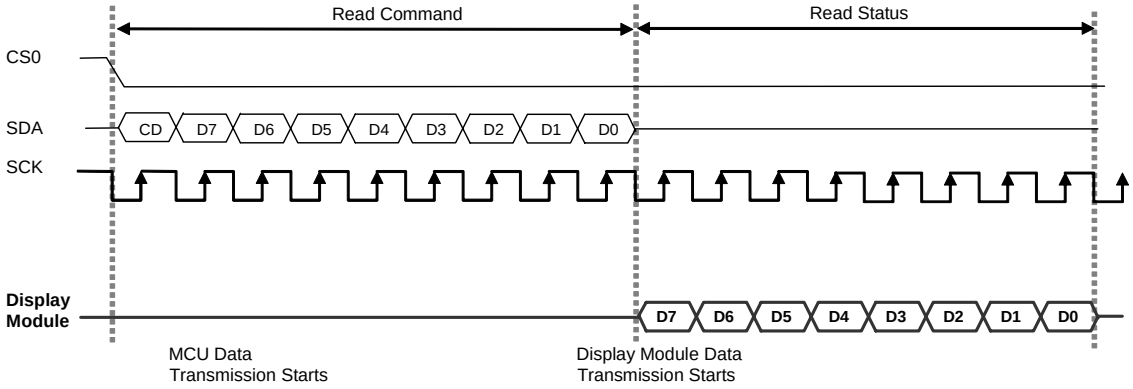


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

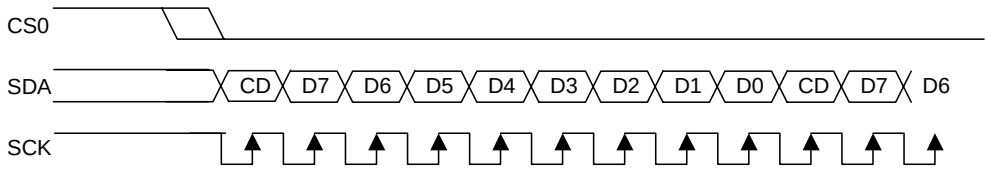


FIGURE 5.b: 3-wire Serial Interface (S9) – Write

HOST INTERFACE REFERENCE CIRCUIT

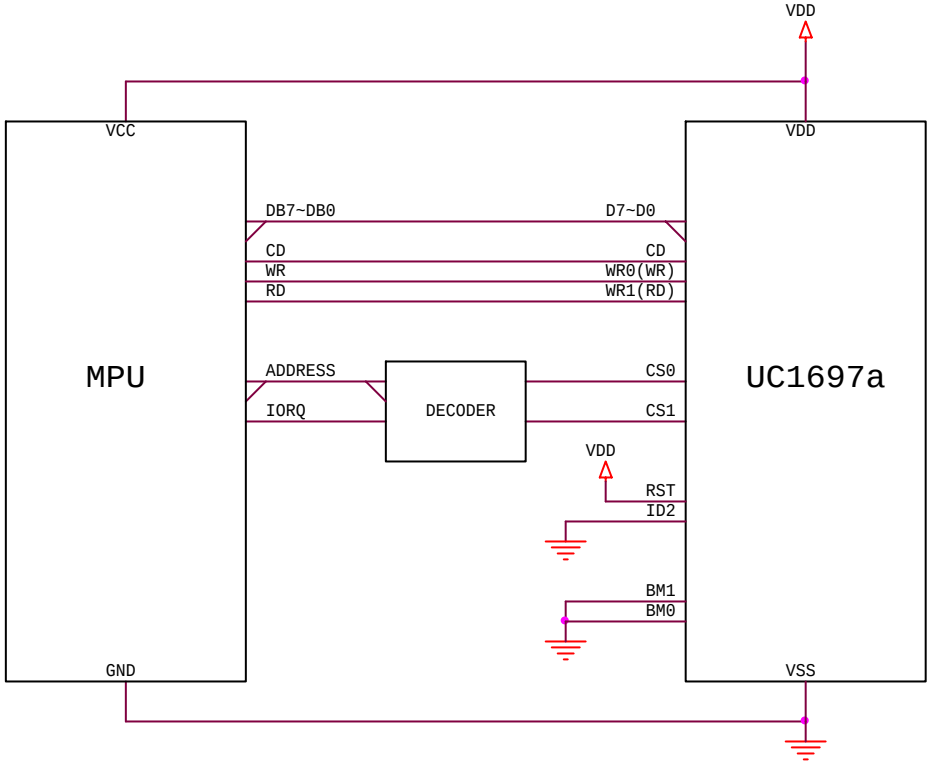


FIGURE 6: 8080/8-bit parallel mode example

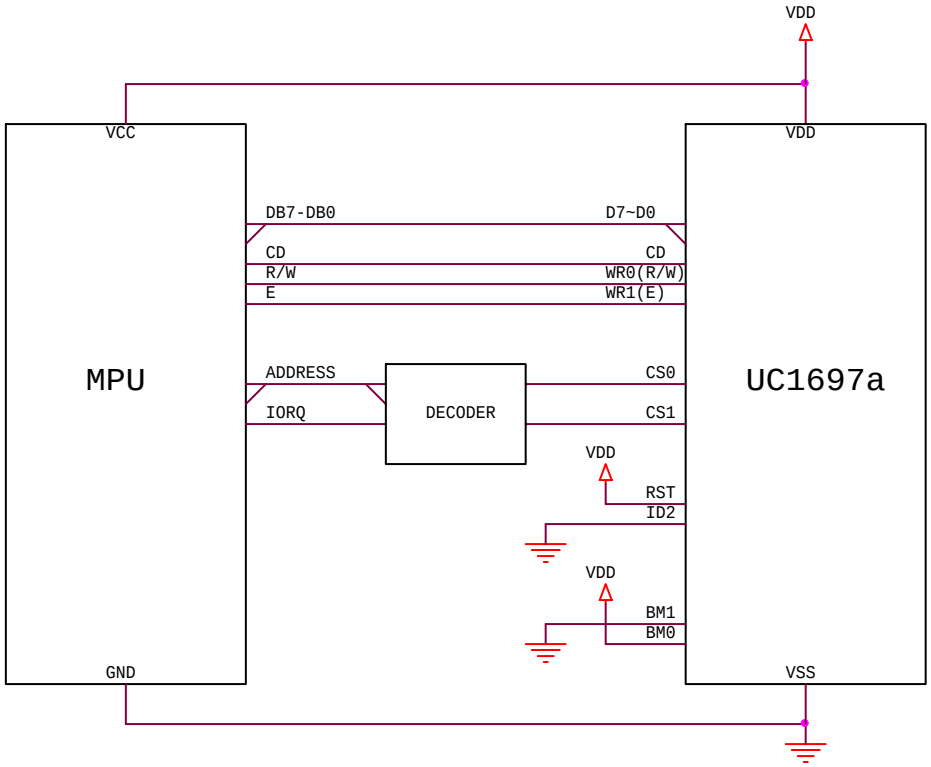


FIGURE 7: 6800/8-bit parallel mode example

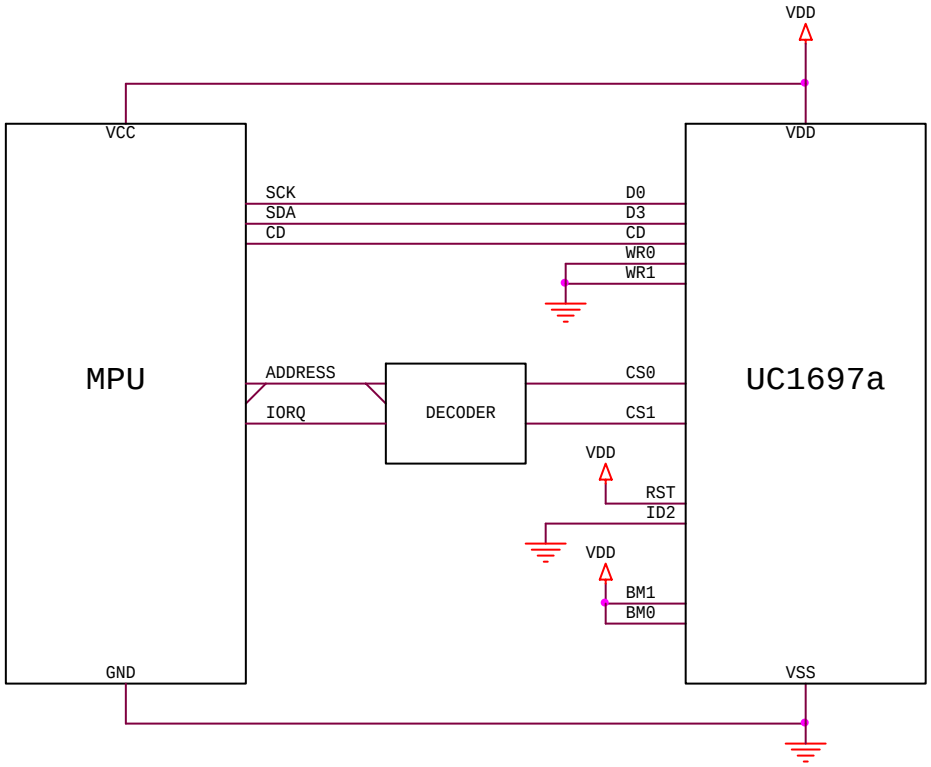


FIGURE 8: 4-Wires SPI (S8) serial mode example

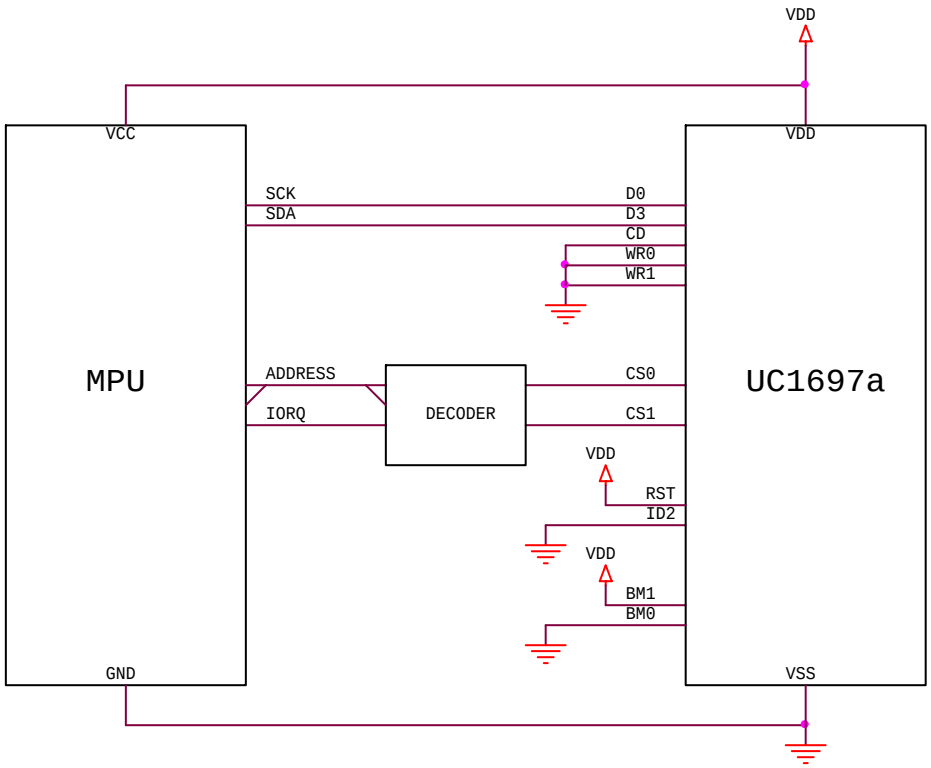


FIGURE 9: 3-Wires SPI (S9) serial mode example

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x128x16.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing `Set Row Address` and `Set Column Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (127), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Scroll Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 128)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches 128. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, 128)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1*, 128)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

WINDOW PROGRAM

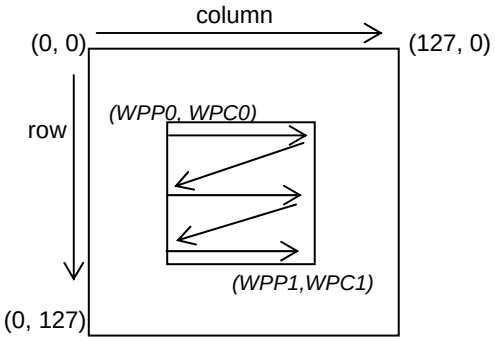
Window program is designed for data-write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and AC[3] setting for inside/outside window mode. When AC[3] is set to '0' (default value), data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). When AC[3] is set to '1', data will be written to whole SRAM excluding the specified window area.

The data-write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data-write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

Specify the starting point of data-write by issuing commands `Set Window Program Starting Column Address`, and `Set Window Program Starting Row Address`.

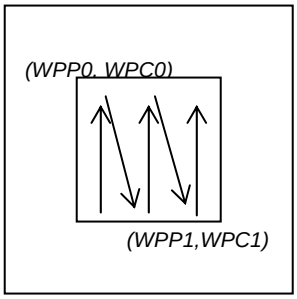
Example1 (AC[2:0] = 001) **:**

AC[3]=0 MX=0



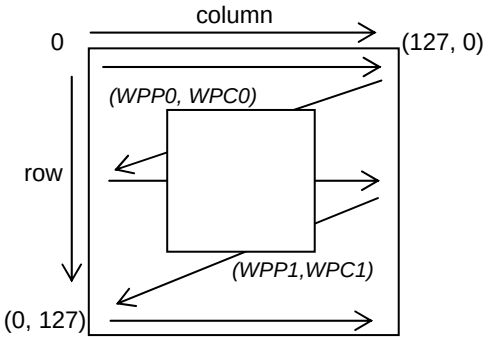
Example 2 (AC[2:0] = 111) **:**

AC[3] = 0 MX = 0



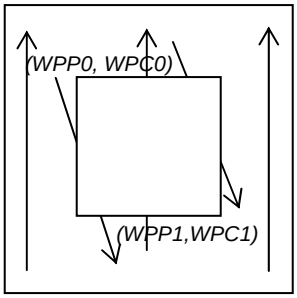
Example1-1 :

AC[3]=1 MX=0



Example 2-1 :

AC[3] = 1 MX = 0



Row Adderss	RAM											
00H	11111	111111	11111									
01H												
02H												
03H												
04H												
05H												
06H												
07H												
08H												
09H												
0AH												
0BH												
0CH												
0DH												
0EH												
0FH												
10H												
11H												
12H												
13H												
14H												
15H												
16H												
17H												
18H												
19H												
1AH												
1BH												
1CH												
:	:	:	:	:	:	:	:	:	:	:	:	:
68H						...	...					
69H						...	...					
6AH												
6BH												
6CH												
6DH												
6EH												
6FH												
70H												
71H												
72H												
73H												
74H												
75H												
76H												
77H												
78H												
79H												
7AH												
7BH												
7CH												
7DH												
7EH												
7FH												

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	..	..	SEG380	SEG381	SEG382	SEG383	SEG384
MX=1	SEG382	SEG383	SEG384	SEG379	SEG380	..	..	SEG5	SEG6	SEG1	SEG2	SEG3

Panel Location	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
COM1	COM1	COM17	COM128	COM16
COM2	COM2	COM18	COM127	COM15
COM3	COM3	COM19	COM126	COM14
COM4	COM4	COM20	COM125	COM13
COM5	COM5	COM21	COM124	COM12
COM6	COM6	COM22	COM123	COM11
COM7	COM7	COM23	COM122	COM10
COM8	COM8	COM24	COM121	COM9
COM9	COM9	COM25	COM120	COM8
COM10	COM10	COM26	COM119	COM7
COM11	COM11	COM27	COM118	COM6
COM12	COM12	COM28	COM117	COM5
COM13	COM13	COM29	COM116	COM4
COM14	COM14	COM30	COM115	COM3
COM15	COM15	COM31	COM114	COM2
COM16	COM16	COM32	COM113	COM1
COM17	COM17	COM33	COM112	COM128
COM18	COM18	COM34	COM111	COM127
COM19	COM19	COM35	COM110	COM126
COM20	COM20	COM36	COM109	COM125
COM21	COM21	COM37	COM108	COM124
COM22	COM22	COM38	COM107	COM123
COM23	COM23	COM39	COM106	COM122
COM24	COM24	COM40	COM105	COM121
COM25	COM25	COM41	COM104	COM120
COM26	COM26	COM42	COM103	COM119
COM27	COM27	COM43	COM102	COM118
COM28	COM28	COM44	COM101	COM117
COM29	COM29	COM45	COM100	COM116
:	:	:	:	:
COM105	COM105	COM121	COM24	COM40
COM106	COM106	COM122	COM23	COM39
COM107	COM107	COM123	COM22	COM38
COM108	COM108	COM124	COM21	COM37
COM109	COM109	COM125	COM20	COM36
COM110	COM110	COM126	COM19	COM35
COM111	COM111	COM127	COM18	COM34
COM112	COM112	COM128	COM17	COM33
COM113	COM113	COM1	COM16	COM32
COM114	COM114	COM2	COM15	COM31
COM115	COM115	COM3	COM14	COM30
COM116	COM116	COM4	COM13	COM29
COM117	COM117	COM5	COM12	COM28
COM118	COM118	COM6	COM11	COM27
COM119	COM119	COM7	COM10	COM26
COM120	COM120	COM8	COM9	COM25
COM121	COM121	COM9	COM8	COM24
COM122	COM122	COM10	COM7	COM23
COM123	COM123	COM11	COM6	COM22
COM124	COM124	COM12	COM5	COM21
COM125	COM125	COM13	COM4	COM20
COM126	COM126	COM14	COM3	COM19
COM127	COM127	COM15	COM2	COM18
COM128	COM128	COM16	COM1	COM17

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 5-6-5, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st byte of Write data: 11111111b

⇒ 2nd byte of Write data: 11111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1697a has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 150mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1697a enters RESET sequence:

- Operation mode will be "Reset".
- All control registers are reset to default values. Refer to section *Control Registers* for details of their default values.

OPERATION MODES

UC1697a has three operating modes (OM): Reset, Sleep, Normal.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by `Set Display Enable`, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1697a internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1697a consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1697a contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1697a internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1697a power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1697a. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first. (See Figure 11)

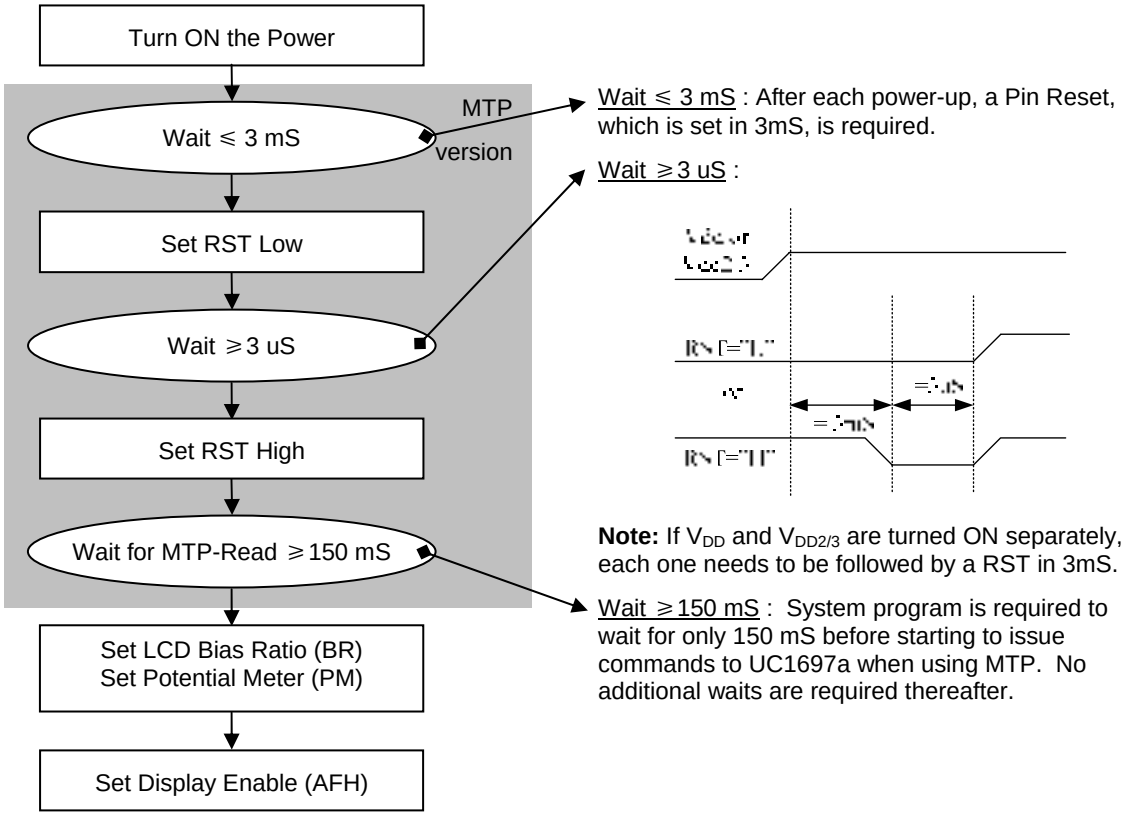


Figure 10: Reference Power-Up Sequence

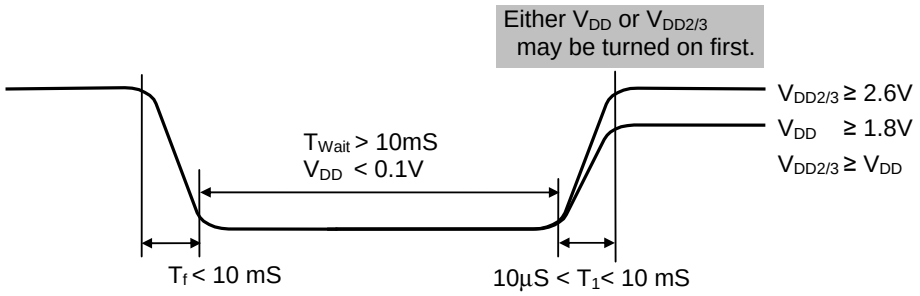


Figure 11: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1697a enters Sleep mode from Display mode by issuing Set Display OFF command. To exit Sleep mode, Set Display ON.

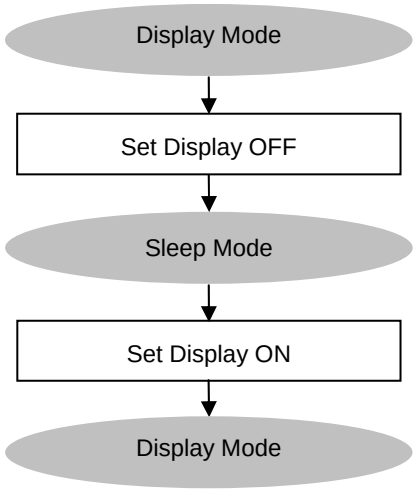


Figure 12 : Enter/Exit Sleep Mode Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge the external capacitor.

When internal V_{LCD} is not used, UC1697a will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

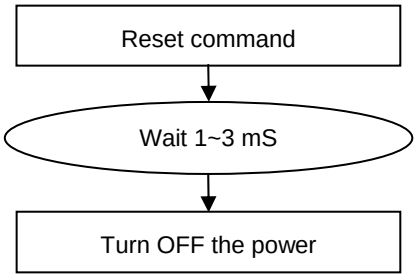


Figure 13: Reference Power-Down Sequence

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1697a such that LCM makers can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1697a:

MTP-Erase, MTP-Program, MTP-Read.

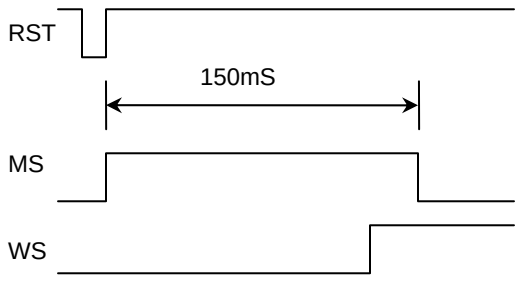
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1697a, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1697a, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use *Read Status* command in a polling loop to make sure {MS, WS}={0, 1} before proceeding with the normal operations, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above “Periodical re-initializing” approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP1 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operations, TST4 should be open, or connected to V_{DD3}.

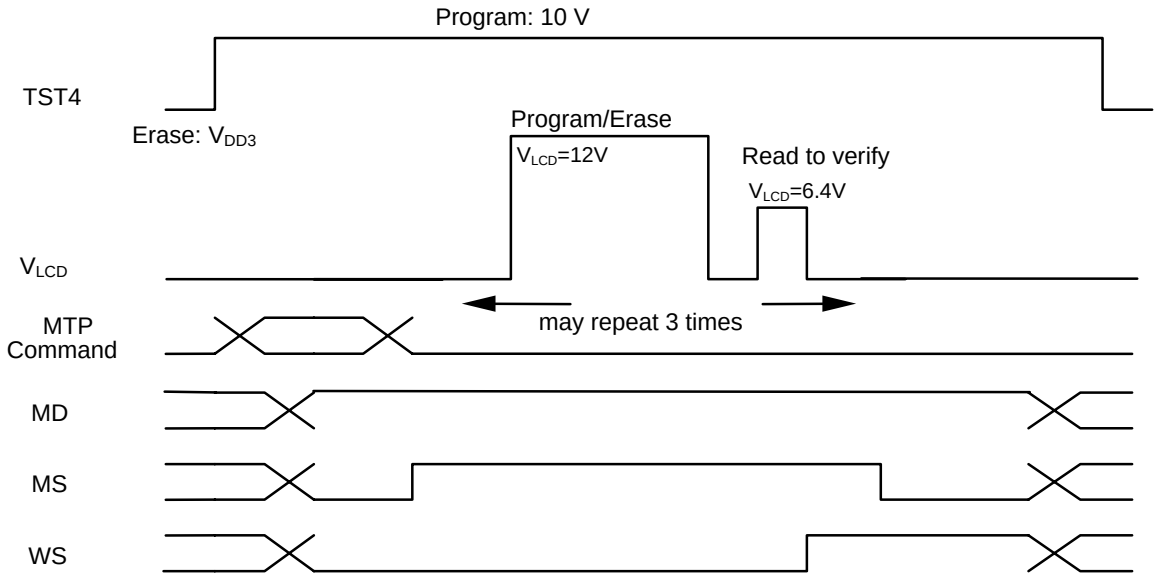
	V_{LCD}	**TST4 (external input)**
Program	MTP2 : 3Dh (12V)	10V (1mA per bit)
Erase	MTP2 : 3Dh (12V)	Floating or V_{DD3}
Read	MTP1 : 00h (6.4V)	Floating or V_{DD3}

Note:

1. Do Erase before Program and program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqslant 3.0V$.

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 6 MTP cell bits. They are divided into two groups for different purpose.

MTP[5:0] : V_{LCD} Trim
When PMO[5]=1: PM with trim = PM - PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP1: 00h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP2: 3Dh(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP3: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP4: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	0	0	0	1	MTPM	Ex: To program MTPM[0] to be 1, set the value to 00000001b *
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP1: 00h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP2: 3Dh(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP3: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP4: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	1	1	1	1	MTPM1	Ex: To erase MTPM[3:0], set the value to 00001111b
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0 WS=1
R											V_{DD}=0V	Power OFF

Note: It is recommended that users clear first all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	LCD specific operating voltage setting
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1697a require special "ESD Sensitivity" consideration in particular:

Test Mode		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		200V	200V	2.5KV	2.5KV
LCM Interface		300V	300V	3.0KV	3.0KV
LCM HV pin/ Test pin	TST1/2/4	250V	250V	3.0KV	3.0KV
	CB pins	300V	300V	3.0KV	3.0KV
	V_{LCDIN}	300V	300V	3.0KV	3.0KV
	V_{LCDOUT}	300V	300V	3.0KV	3.0KV
PWR / GND		--	300V	--	3.0KV

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ESD RECOVERY FUNCTION

There are 2 ways of ESD Recovery supported by UC1697a:

(1) ESD-detection circuits method

Place two detection circuits at each corner of a chip, totally 8 registers. When the data of these registers are different from their default values, it means ESD probably strikes and EF will be set to 1. See command `Get Status & PM0` for EF.

(2) Working Status Monitor Function method

The chip is considered in working state when Display Enable is ON, hi-pump, and low-pump. When any of these 3 situation does not apply, ESD probably strikes, DE=0. See command `Get Status & PM0` for DE.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, Note 1 and 2

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Driving voltage	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

NOTE:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65	1.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.5	2.6~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ = 2.5V, 25^{O}C		14.58	16.5	V
V_D	LCD data voltage	$V_{DD2/3}$ = 2.5V, 25^{O}C	1.07		1.63	V
V_{IL}	Input logic LOW				0.2V_{DD}	V
V_{IH}	Input logic HIGH		0.85V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD}	V
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85^{o}C			50	µA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 16.5V		1000	1500	Ω
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 16.5V		1000	1500	Ω
f_{LINE}	Average line rate	LC[4:3] = 10b, 25^{O}C	-10%	29.6	+10%	Klps

Note : Voltages exceeding the Max. value may still keep the IC operating properly, yet might shorten its lifetime.

POWER CONSUMPTION

V_{DD} = 2.8 V,
V_{LCD} = 14.58 V,
Mux Rate = 128,
C_B = 2.2 µF,
N-line inversion = 18 lines

Bias Ratio = 12,
Line Rate = 10 b,
Bus mode = 6800,
Temperature = 25 ^{o}C,
Color Mode = 64 K color mode,

PM = 92,
Panel Loading (PC[1:0]) = 1x b,
C_L = 330 nF,
MTP= 00 H,
All HV outputs are open circuit.

Display Pattern	Conditions	Typ. (µA)	Max. (µA)
All-Pixel-OFF	Bus = idle	1208	1812
2-pixel checker	Bus = idle	1773	2660
None	Reset (stand-by current)	< 1	5

AC CHARACTERISTICS

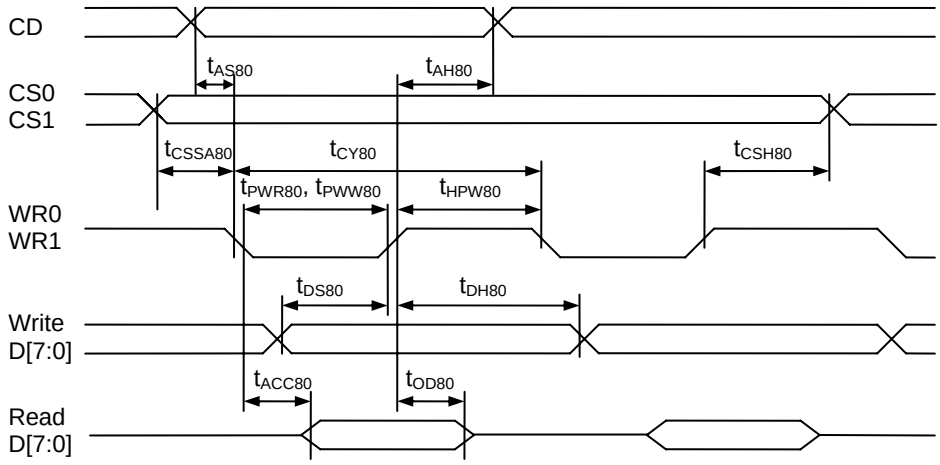


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Units
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80}	CD	Address setup time		0	–	nS
t_{AH80}		Address hold time		0		
t_{CSSA80}	CS1/CS0	Chip select setup time		0	–	nS
t_{CSH80}				0		
t_{CY80}	WR0, WR1	System cycle time		160 / 110	–	nS
t_{PWR80}, t_{PWW80}		Low Pulse width		65 / 40		
t_{HPW80}		High pulse width		65 / 40		
t_{DS80}	D7~D0	Data setup time		--- / 30	–	nS
t_{DH80}	(Write)	Data hold time		--- / 0		
t_{ACC80}	D7~D0	Read access time	C_L = 100pF	– / ---	70	nS
t_{OD80}	(Read)	Output disable time		15 / ---	30	
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80}	CD	Address setup time		0	–	nS
t_{AH80}		Address hold time		0		
t_{CSSA80}	CS1/CS0	Chip select setup time		0	–	nS
t_{CSH80}				0		
t_{CY80}	WR0, WR1	System cycle time		280 / 185	–	nS
t_{PWR80}, t_{PWW80}		Low Pulse width		125 / 77		
t_{HPW80}		High pulse width		125 / 77		
t_{DS80}	D7~D0	Data setup time		60	–	nS
t_{DH80}	(Write)	Data hold time		0		
t_{ACC80}	D7~D0	Read access time	C_L = 100pF	–	140	nS
t_{OD80}	(Read)	Output disable time		30	60	

Note: tr (rising time), tf (falling time) : ≤ 15nS

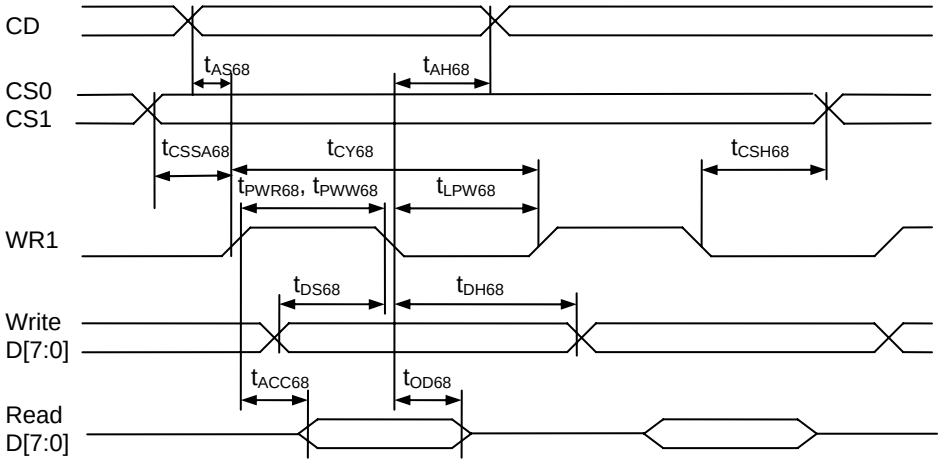


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Units
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0	–	nS
t_{CY68}	WR1	System cycle time		160 / 110	–	nS
t_{PWR68}, t_{PWW68}		High Pulse width		65 / 40		
t_{LPW68}		Low pulse width		65 / 40		
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		--- / 30 --- / 0	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / --- 15 / ---	70 30	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0	–	nS
t_{CY68}	WR1	System cycle time		280 / 185	–	nS
t_{PWR68}, t_{PWW68}		High Pulse width		125 / 77		
t_{LPW68}		Low pulse width		125 / 77		
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		--- / 60 --- / 0	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / --- 30 / ---	140 60	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

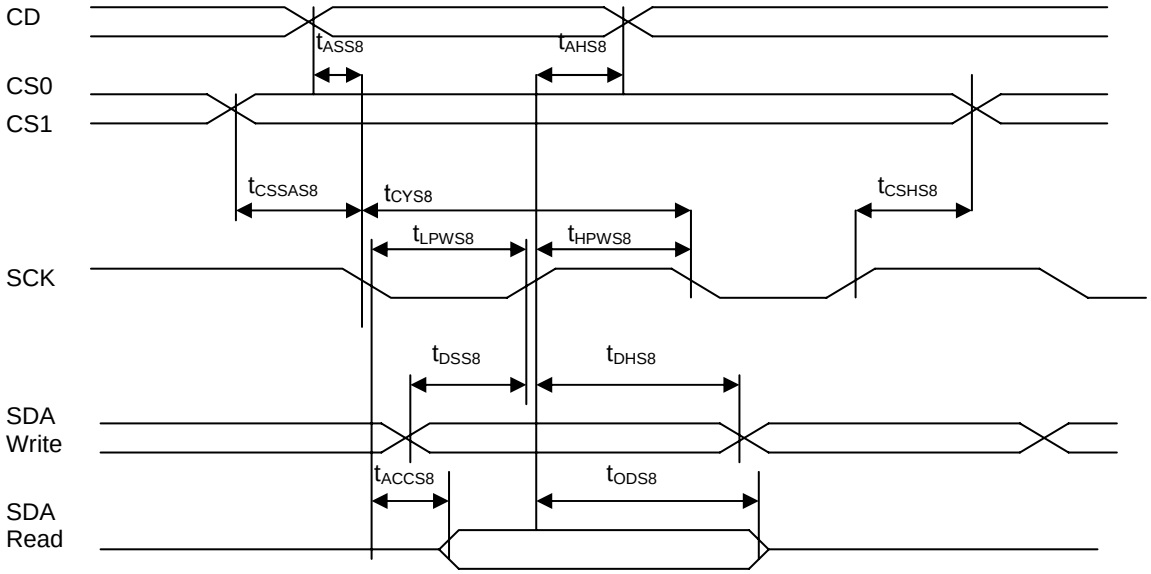


FIGURE 15: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Units
(2.5V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 / 5 5 / 5	–	nS
t_{CYS8}	SCK	System cycle time		130 / 70	–	nS
t_{LPWS8}		Low pulse width		50 / 20		
t_{HPWS8}		High pulse width		50 / 20		
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		--- / 15 --- / 5	–	nS
t_{ACCS8} t_{ODS8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / --- 30 / ---	50 –	nS
(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		15 / 15 15 / 15	–	nS
t_{CYS8}	SCK	System cycle time		210 / 105	–	nS
t_{LPWS8}		Low pulse width		90 / 37		
t_{HPWS8}		High pulse width		90 / 37		
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		--- / 30 --- / 10	–	nS
t_{ACCS8} t_{ODS8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / --- 60 / ---	95 –	nS

Note: tr (rising time), tf (falling time) : ⩽ 15nS

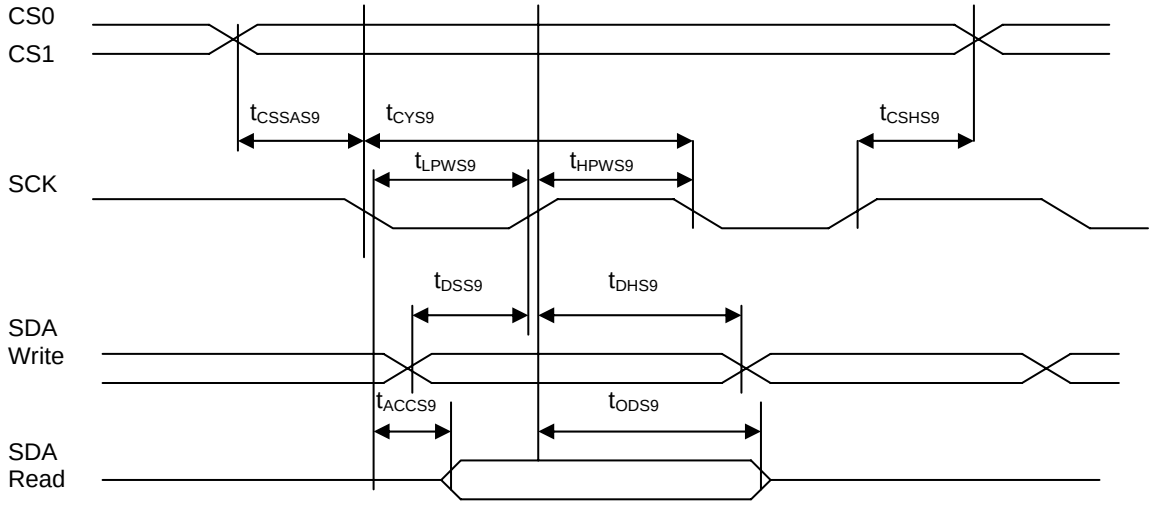


FIGURE 16: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Units
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 / 5 5 / 5	–	nS
t_{CYS9}	SCK	System cycle time		130 / 70	–	nS
t_{LPWS9}		Low pulse width		50 / 20		
t_{HPWS9}		High pulse width		50 / 20		
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		--- / 15 --- / 5	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / --- 30 / ---	50 –	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 / 10 10 / 10	–	nS
t_{CYS9}	SCK	System cycle time		210 / 105	–	nS
t_{LPWS9}		Low pulse width		90 / 37		
t_{HPWS9}		High pulse width		90 / 37		
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		--- / 30 --- / 10	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / --- 60 / ---	95 –	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

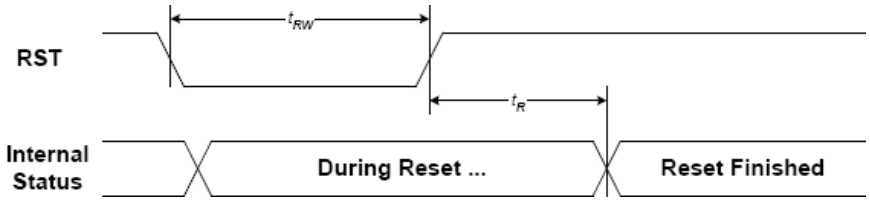
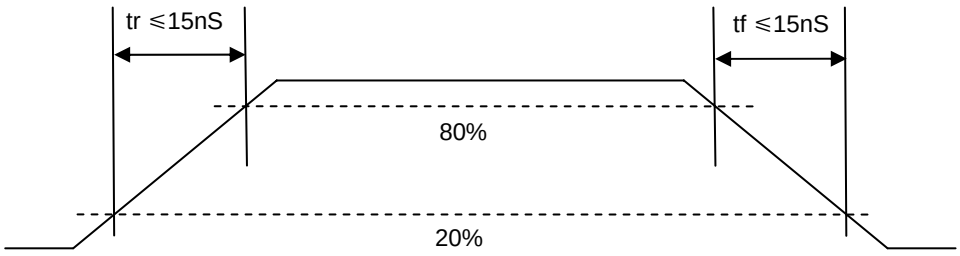


FIGURE 17: Reset Characteristics

(1.65V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		6	–	mS

Note: For each mode, the rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.



PHYSICAL DIMENSIONS

PAD INFORMATION

DIE SIZE:
10821 µM x 1033 µM ± 40 µM

DIE THICKNESS:
400 µM ± 20 µM
(H_{MAX}-H_{MIN}) within die ≤ 2 µM

BUMP HEIGHT:
15 µM ± 3 µM
(H_{MAX}-H_{MIN}) within die ≤ 2 µM

HARDNESS:
90 Hv

BUMP SIZE:
SEG/COM: 12 x 150 μM^2 ± 2.5 µM

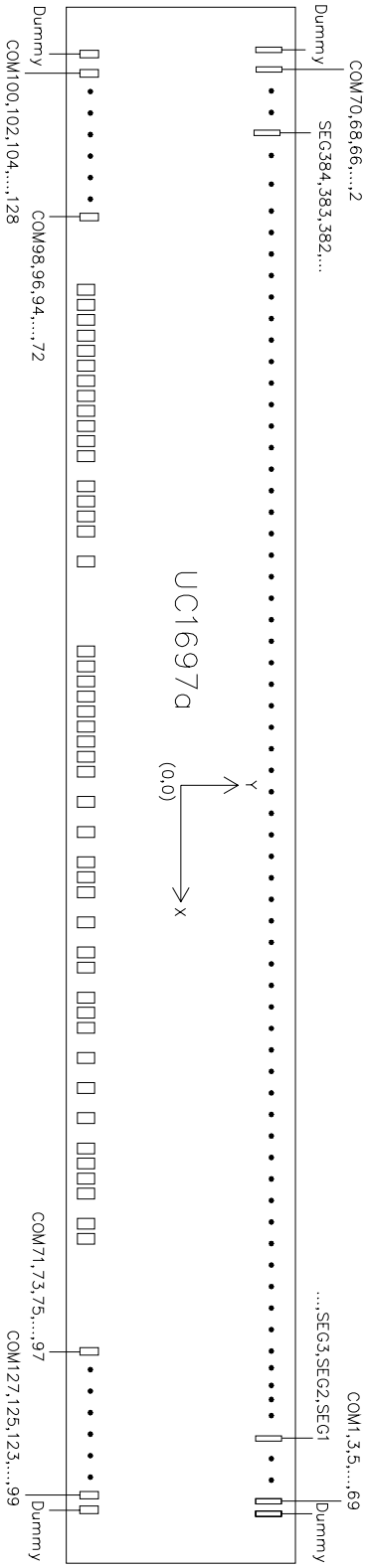
BUMP PITCH:
23 µM

BUMP GAP:
11 µM

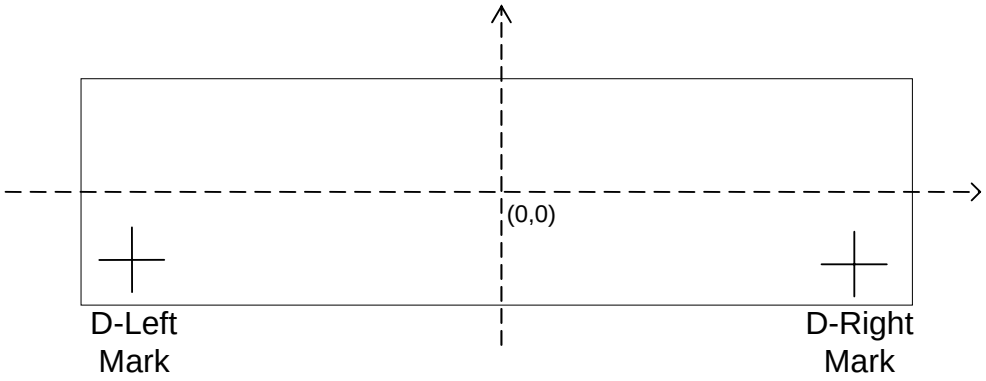
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

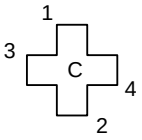
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

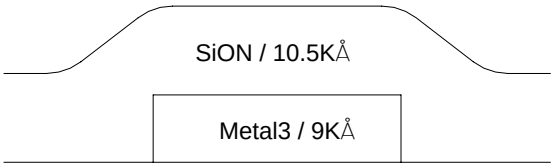
Alignment marks are on Metal3 under Passivation.

The "+" mark is symmetric both horizontally and vertically.

COORDINATES:

	Down-Left Mark (+)		Down-Right Mark (+)	
	X	Y	X	Y
1	-4502.96	-411	4484.36	-411
2	-4482.96	-471	4504.36	-471
3	-4522.96	-431	4464.36	-431
4	-4462.96	-451	4524.36	-451
C	-4492.96	-441	4494.36	-441

TOP METAL AND PASSIVATION:



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-5232.5	-407	12	150
2	COM100	-5209.5	-407	12	150
3	COM102	-5186.5	-407	12	150
4	COM104	-5163.5	-407	12	150
5	COM106	-5140.5	-407	12	150
6	COM108	-5117.5	-407	12	150
7	COM110	-5094.5	-407	12	150
8	COM112	-5071.5	-407	12	150
9	COM114	-5048.5	-407	12	150
10	COM116	-5025.5	-407	12	150
11	COM118	-5002.5	-407	12	150
12	COM120	-4979.5	-407	12	150
13	COM122	-4956.5	-407	12	150
14	COM124	-4933.5	-407	12	150
15	COM126	-4910.5	-407	12	150
16	COM128	-4887.5	-407	12	150
17	COM98	-4864.5	-407	12	150
18	COM96	-4841.5	-407	12	150
19	COM94	-4818.5	-407	12	150
20	COM92	-4795.5	-407	12	150
21	COM90	-4772.5	-407	12	150
22	COM88	-4749.5	-407	12	150
23	COM86	-4726.5	-407	12	150
24	COM84	-4703.5	-407	12	150
25	COM82	-4680.5	-407	12	150
26	COM80	-4657.5	-407	12	150
27	COM78	-4634.5	-407	12	150
28	COM76	-4611.5	-407	12	150
29	COM74	-4588.5	-407	12	150
30	COM72	-4565.5	-407	12	150
31	D7	-4387.99	-442.215	65	77.57
32	VDDX	-4301.32	-442.215	45	77.57
33	D6	-4214.65	-442.215	65	77.57
34	D5	-4134.31	-442.215	65	77.57
35	D4	-4053.97	-442.215	65	77.57
36	D3	-3973.63	-442.215	65	77.57
37	D2	-3893.29	-442.215	65	77.57
38	D1	-3812.95	-442.215	65	77.57
39	D0	-3732.61	-442.215	65	77.57
40	RST	-3626.07	-442.215	65	77.57
41	WR0	-3545.73	-442.215	65	77.57
42	VDDX	-3459.06	-442.215	45	77.57
43	WR1	-3372.39	-442.215	65	77.57
44	CD	-3292.05	-442.215	65	77.57
45	CS0	-3211.71	-442.215	65	77.57
46	VDDX	-3125.04	-442.215	45	77.57
47	CS1	-3038.37	-442.215	65	77.57
48	BM0	-2958.03	-442.215	65	77.57
49	VDDX	-2870.36	-442.215	45	77.57
50	BM1	-2783.69	-442.215	65	77.57
51	TST4	-2697.52	-442.215	45	77.57
52	DUMMY	-2538.16	-442.215	45	77.57
53	DUMMY	-2465.66	-442.215	45	77.57
54	DUMMY	-2393.16	-442.215	45	77.57
55	TST1	-2232.36	-442.215	45	77.57
56	TST2	-2172.36	-442.215	45	77.57
57	DUMMY	-2079.04	-442.215	45	77.57
58	ID0	-1994.67	-442.215	65	77.57
59	VDDX	-1908.5	-442.215	45	77.57
60	ID1	-1822.33	-442.215	65	77.57

#	Pad	X	Y	W	H
61	ID2	-1741.99	-442.215	65	77.57
62	vss	-1509.95	-442.215	45	77.57
63	vss	-1449.95	-442.215	45	77.57
64	vss	-1389.95	-442.215	45	77.57
65	vss	-1329.95	-442.215	45	77.57
66	vss	-1269.95	-442.215	45	77.57
67	vss	-1209.95	-442.215	45	77.57
68	vss	-1149.95	-442.215	45	77.57
69	vss	-1089.95	-442.215	45	77.57
70	vss	-1029.95	-442.215	45	77.57
71	vss	-969.95	-442.215	45	77.57
72	vss	-909.95	-442.215	45	77.57
73	vss	-849.95	-442.215	45	77.57
74	vss	-789.95	-442.215	45	77.57
75	DUMMY	-689.29	-442.215	45	77.57
76	vss2	-588.63	-442.215	45	77.57
77	vss2	-528.63	-442.215	45	77.57
78	vss2	-468.63	-442.215	45	77.57
79	vss2	-408.63	-442.215	45	77.57
80	vss2	-348.63	-442.215	45	77.57
81	vss2	-288.63	-442.215	45	77.57
82	vss2	-228.63	-442.215	45	77.57
83	vss2	-168.63	-442.215	45	77.57
84	vss2	-108.63	-442.215	45	77.57
85	vss2	-48.63	-442.215	45	77.57
86	vss2	11.37	-442.215	45	77.57
87	vss2	71.37	-442.215	45	77.57
88	vss2	131.37	-442.215	45	77.57
89	vdd	191.37	-442.215	45	77.57
90	vdd	251.37	-442.215	45	77.57
91	vdd	311.37	-442.215	45	77.57
92	vdd	371.37	-442.215	45	77.57
93	vdd	431.37	-442.215	45	77.57
94	vdd	491.37	-442.215	45	77.57
95	vdd	551.37	-442.215	45	77.57
96	vdd	611.37	-442.215	45	77.57
97	vdd	671.37	-442.215	45	77.57
98	vdd	758.99	-442.215	83.24	77.57
99	DUMMY	848.29	-442.215	45	77.57
100	DUMMY	910.65	-442.215	45	77.57
101	DUMMY	973.01	-442.215	45	77.57
102	DUMMY	1035.37	-442.215	45	77.57
103	DUMMY	1097.73	-442.215	45	77.57
104	DUMMY	1160.09	-442.215	45	77.57
105	DUMMY	1222.45	-442.215	45	77.57
106	DUMMY	1284.81	-442.215	45	77.57
107	DUMMY	1347.17	-442.215	45	77.57
108	DUMMY	1409.53	-442.215	45	77.57
109	DUMMY	1471.89	-442.215	45	77.57
110	vdd2	1561.19	-442.215	83.24	77.57
111	vdd2	1650.83	-442.215	45	77.57
112	vdd2	1710.83	-442.215	45	77.57
113	vdd2	1770.83	-442.215	45	77.57
114	vdd2	1830.83	-442.215	45	77.57
115	vdd2	1890.83	-442.215	45	77.57
116	vdd2	1950.83	-442.215	45	77.57
117	vdd2	2010.83	-442.215	45	77.57
118	vdd2	2070.83	-442.215	45	77.57
119	DUMMY	2140.31	-442.215	45	77.57
120	DUMMY	2202.67	-442.215	45	77.57

#	Pad	X	Y	W	H
121	vdd3	2291.97	-442.215	83.24	77.57
122	vdd3	2382.09	-442.215	45	77.57
123	vdd3	2442.09	-442.215	45	77.57
124	VB0+	2515.09	-442.215	45	77.57
125	VB0+	2575.09	-442.215	45	77.57
126	VB0+	2635.09	-442.215	45	77.57
127	DUMMY	2801.53	-442.215	45	77.57
128	VB1+	2879.41	-442.215	45	77.57
129	VB1+	2939.41	-442.215	45	77.57
130	VB1+	2999.41	-442.215	45	77.57
131	DUMMY	3165.85	-442.215	45	77.57
132	VB1-	3241.59	-442.215	45	77.57
133	VB1-	3301.59	-442.215	45	77.57
134	VB1-	3361.59	-442.215	45	77.57
135	DUMMY	3528.03	-442.215	45	77.57
136	DUMMY	3602.91	-442.215	45	77.57
137	VB0-	3769.35	-442.215	45	77.57
138	VB0-	3829.36	-442.215	45	77.57
139	VB0-	3889.36	-442.215	45	77.57
140	DUMMY	3965.44	-442.215	45	77.57
141	VLCDIN	4121.8	-442.215	45	77.57
142	VLCDOUT	4181.8	-442.215	45	77.57
143	DUMMY	4336.72	-442.215	45	77.57
144	DUMMY	4413.66	-442.215	45	77.57
145	COM71	4565.5	-407	12	150
146	COM73	4588.5	-407	12	150
147	COM75	4611.5	-407	12	150
148	COM77	4634.5	-407	12	150
149	COM79	4657.5	-407	12	150
150	COM81	4680.5	-407	12	150
151	COM83	4703.5	-407	12	150
152	COM85	4726.5	-407	12	150
153	COM87	4749.5	-407	12	150
154	COM89	4772.5	-407	12	150
155	COM91	4795.5	-407	12	150
156	COM93	4818.5	-407	12	150
157	COM95	4841.5	-407	12	150
158	COM97	4864.5	-407	12	150
159	COM127	4887.5	-407	12	150
160	COM125	4910.5	-407	12	150
161	COM123	4933.5	-407	12	150
162	COM121	4956.5	-407	12	150
163	COM119	4979.5	-407	12	150
164	COM117	5002.5	-407	12	150
165	COM115	5025.5	-407	12	150
166	COM113	5048.5	-407	12	150
167	COM111	5071.5	-407	12	150
168	COM109	5094.5	-407	12	150
169	COM107	5117.5	-407	12	150
170	COM105	5140.5	-407	12	150
171	COM103	5163.5	-407	12	150
172	COM101	5186.5	-407	12	150
173	COM99	5209.5	-407	12	150
174	DUMMY	5232.5	-407	12	150
175	DUMMY	5232.5	407	12	150
176	COM69	5209.5	407	12	150
177	COM67	5186.5	407	12	150
178	COM65	5163.5	407	12	150
179	COM63	5140.5	407	12	150
180	COM61	5117.5	407	12	150
181	COM59	5094.5	407	12	150
182	COM57	5071.5	407	12	150

#	Pad	X	Y	W	H
183	COM55	5048.5	407	12	150
184	COM53	5025.5	407	12	150
185	COM51	5002.5	407	12	150
186	COM49	4979.5	407	12	150
187	COM47	4956.5	407	12	150
188	COM45	4933.5	407	12	150
189	COM43	4910.5	407	12	150
190	COM41	4887.5	407	12	150
191	COM39	4864.5	407	12	150
192	COM37	4841.5	407	12	150
193	COM35	4818.5	407	12	150
194	COM33	4795.5	407	12	150
195	COM31	4772.5	407	12	150
196	COM29	4749.5	407	12	150
197	COM27	4726.5	407	12	150
198	COM25	4703.5	407	12	150
199	COM23	4680.5	407	12	150
200	COM21	4657.5	407	12	150
201	COM19	4634.5	407	12	150
202	COM17	4611.5	407	12	150
203	COM15	4588.5	407	12	150
204	COM13	4565.5	407	12	150
205	COM11	4542.5	407	12	150
206	COM9	4519.5	407	12	150
207	COM7	4496.5	407	12	150
208	COM5	4473.5	407	12	150
209	COM3	4450.5	407	12	150
210	COM1	4427.5	407	12	150
211	SEG1	4404.5	407	12	150
212	SEG2	4381.5	407	12	150
213	SEG3	4358.5	407	12	150
214	SEG4	4335.5	407	12	150
215	SEG5	4312.5	407	12	150
216	SEG6	4289.5	407	12	150
217	SEG7	4266.5	407	12	150
218	SEG8	4243.5	407	12	150
219	SEG9	4220.5	407	12	150
220	SEG10	4197.5	407	12	150
221	SEG11	4174.5	407	12	150
222	SEG12	4151.5	407	12	150
223	SEG13	4128.5	407	12	150
224	SEG14	4105.5	407	12	150
225	SEG15	4082.5	407	12	150
226	SEG16	4059.5	407	12	150
227	SEG17	4036.5	407	12	150
228	SEG18	4013.5	407	12	150
229	SEG19	3990.5	407	12	150
230	SEG20	3967.5	407	12	150
231	SEG21	3944.5	407	12	150
232	SEG22	3921.5	407	12	150
233	SEG23	3898.5	407	12	150
234	SEG24	3875.5	407	12	150
235	SEG25	3852.5	407	12	150
236	SEG26	3829.5	407	12	150
237	SEG27	3806.5	407	12	150
238	SEG28	3783.5	407	12	150
239	SEG29	3760.5	407	12	150
240	SEG30	3737.5	407	12	150
241	SEG31	3714.5	407	12	150
242	SEG32	3691.5	407	12	150
243	SEG33	3668.5	407	12	150
244	SEG34	3645.5	407	12	150

#	Pad	X	Y	W	H
245	SEG35	3622.5	407	12	150
246	SEG36	3599.5	407	12	150
247	SEG37	3576.5	407	12	150
248	SEG38	3553.5	407	12	150
249	SEG39	3530.5	407	12	150
250	SEG40	3507.5	407	12	150
251	SEG41	3484.5	407	12	150
252	SEG42	3461.5	407	12	150
253	SEG43	3438.5	407	12	150
254	SEG44	3415.5	407	12	150
255	SEG45	3392.5	407	12	150
256	SEG46	3369.5	407	12	150
257	SEG47	3346.5	407	12	150
258	SEG48	3323.5	407	12	150
259	SEG49	3300.5	407	12	150
260	SEG50	3277.5	407	12	150
261	SEG51	3254.5	407	12	150
262	SEG52	3231.5	407	12	150
263	SEG53	3208.5	407	12	150
264	SEG54	3185.5	407	12	150
265	SEG55	3162.5	407	12	150
266	SEG56	3139.5	407	12	150
267	SEG57	3116.5	407	12	150
268	SEG58	3093.5	407	12	150
269	SEG59	3070.5	407	12	150
270	SEG60	3047.5	407	12	150
271	SEG61	3024.5	407	12	150
272	SEG62	3001.5	407	12	150
273	SEG63	2978.5	407	12	150
274	SEG64	2955.5	407	12	150
275	SEG65	2932.5	407	12	150
276	SEG66	2909.5	407	12	150
277	SEG67	2886.5	407	12	150
278	SEG68	2863.5	407	12	150
279	SEG69	2840.5	407	12	150
280	SEG70	2817.5	407	12	150
281	SEG71	2794.5	407	12	150
282	SEG72	2771.5	407	12	150
283	SEG73	2748.5	407	12	150
284	SEG74	2725.5	407	12	150
285	SEG75	2702.5	407	12	150
286	SEG76	2679.5	407	12	150
287	SEG77	2656.5	407	12	150
288	SEG78	2633.5	407	12	150
289	SEG79	2610.5	407	12	150
290	SEG80	2587.5	407	12	150
291	SEG81	2564.5	407	12	150
292	SEG82	2541.5	407	12	150
293	SEG83	2518.5	407	12	150
294	SEG84	2495.5	407	12	150
295	SEG85	2472.5	407	12	150
296	SEG86	2449.5	407	12	150
297	SEG87	2426.5	407	12	150
298	SEG88	2403.5	407	12	150
299	SEG89	2380.5	407	12	150
300	SEG90	2357.5	407	12	150
301	SEG91	2334.5	407	12	150
302	SEG92	2311.5	407	12	150
303	SEG93	2288.5	407	12	150
304	SEG94	2265.5	407	12	150
305	SEG95	2242.5	407	12	150
306	SEG96	2219.5	407	12	150

#	Pad	X	Y	W	H
307	SEG97	2196.5	407	12	150
308	SEG98	2173.5	407	12	150
309	SEG99	2150.5	407	12	150
310	SEG100	2127.5	407	12	150
311	SEG101	2104.5	407	12	150
312	SEG102	2081.5	407	12	150
313	SEG103	2058.5	407	12	150
314	SEG104	2035.5	407	12	150
315	SEG105	2012.5	407	12	150
316	SEG106	1989.5	407	12	150
317	SEG107	1966.5	407	12	150
318	SEG108	1943.5	407	12	150
319	SEG109	1920.5	407	12	150
320	SEG110	1897.5	407	12	150
321	SEG111	1874.5	407	12	150
322	SEG112	1851.5	407	12	150
323	SEG113	1828.5	407	12	150
324	SEG114	1805.5	407	12	150
325	SEG115	1782.5	407	12	150
326	SEG116	1759.5	407	12	150
327	SEG117	1736.5	407	12	150
328	SEG118	1713.5	407	12	150
329	SEG119	1690.5	407	12	150
330	SEG120	1667.5	407	12	150
331	SEG121	1644.5	407	12	150
332	SEG122	1621.5	407	12	150
333	SEG123	1598.5	407	12	150
334	SEG124	1575.5	407	12	150
335	SEG125	1552.5	407	12	150
336	SEG126	1529.5	407	12	150
337	SEG127	1506.5	407	12	150
338	SEG128	1483.5	407	12	150
339	SEG129	1460.5	407	12	150
340	SEG130	1437.5	407	12	150
341	SEG131	1414.5	407	12	150
342	SEG132	1391.5	407	12	150
343	SEG133	1368.5	407	12	150
344	SEG134	1345.5	407	12	150
345	SEG135	1322.5	407	12	150
346	SEG136	1299.5	407	12	150
347	SEG137	1276.5	407	12	150
348	SEG138	1253.5	407	12	150
349	SEG139	1230.5	407	12	150
350	SEG140	1207.5	407	12	150
351	SEG141	1184.5	407	12	150
352	SEG142	1161.5	407	12	150
353	SEG143	1138.5	407	12	150
354	SEG144	1115.5	407	12	150
355	SEG145	1092.5	407	12	150
356	SEG146	1069.5	407	12	150
357	SEG147	1046.5	407	12	150
358	SEG148	1023.5	407	12	150
359	SEG149	1000.5	407	12	150
360	SEG150	977.5	407	12	150
361	SEG151	954.5	407	12	150
362	SEG152	931.5	407	12	150
363	SEG153	908.5	407	12	150
364	SEG154	885.5	407	12	150
365	SEG155	862.5	407	12	150
366	SEG156	839.5	407	12	150
367	SEG157	816.5	407	12	150
368	SEG158	793.5	407	12	150

#	Pad	X	Y	W	H
369	SEG159	770.5	407	12	150
370	SEG160	747.5	407	12	150
371	SEG161	724.5	407	12	150
372	SEG162	701.5	407	12	150
373	SEG163	678.5	407	12	150
374	SEG164	655.5	407	12	150
375	SEG165	632.5	407	12	150
376	SEG166	609.5	407	12	150
377	SEG167	586.5	407	12	150
378	SEG168	563.5	407	12	150
379	SEG169	540.5	407	12	150
380	SEG170	517.5	407	12	150
381	SEG171	494.5	407	12	150
382	SEG172	471.5	407	12	150
383	SEG173	448.5	407	12	150
384	SEG174	425.5	407	12	150
385	SEG175	402.5	407	12	150
386	SEG176	379.5	407	12	150
387	SEG177	356.5	407	12	150
388	SEG178	333.5	407	12	150
389	SEG179	310.5	407	12	150
390	SEG180	287.5	407	12	150
391	SEG181	264.5	407	12	150
392	SEG182	241.5	407	12	150
393	SEG183	218.5	407	12	150
394	SEG184	195.5	407	12	150
395	SEG185	172.5	407	12	150
396	SEG186	149.5	407	12	150
397	SEG187	126.5	407	12	150
398	SEG188	103.5	407	12	150
399	SEG189	80.5	407	12	150
400	SEG190	57.5	407	12	150
401	SEG191	34.5	407	12	150
402	SEG192	11.5	407	12	150
403	SEG193	-11.5	407	12	150
404	SEG194	-34.5	407	12	150
405	SEG195	-57.5	407	12	150
406	SEG196	-80.5	407	12	150
407	SEG197	-103.5	407	12	150
408	SEG198	-126.5	407	12	150
409	SEG199	-149.5	407	12	150
410	SEG200	-172.5	407	12	150
411	SEG201	-195.5	407	12	150
412	SEG202	-218.5	407	12	150
413	SEG203	-241.5	407	12	150
414	SEG204	-264.5	407	12	150
415	SEG205	-287.5	407	12	150
416	SEG206	-310.5	407	12	150
417	SEG207	-333.5	407	12	150
418	SEG208	-356.5	407	12	150
419	SEG209	-379.5	407	12	150
420	SEG210	-402.5	407	12	150
421	SEG211	-425.5	407	12	150
422	SEG212	-448.5	407	12	150
423	SEG213	-471.5	407	12	150
424	SEG214	-494.5	407	12	150
425	SEG215	-517.5	407	12	150
426	SEG216	-540.5	407	12	150
427	SEG217	-563.5	407	12	150
428	SEG218	-586.5	407	12	150
429	SEG219	-609.5	407	12	150
430	SEG220	-632.5	407	12	150

#	Pad	X	Y	W	H
431	SEG221	-655.5	407	12	150
432	SEG222	-678.5	407	12	150
433	SEG223	-701.5	407	12	150
434	SEG224	-724.5	407	12	150
435	SEG225	-747.5	407	12	150
436	SEG226	-770.5	407	12	150
437	SEG227	-793.5	407	12	150
438	SEG228	-816.5	407	12	150
439	SEG229	-839.5	407	12	150
440	SEG230	-862.5	407	12	150
441	SEG231	-885.5	407	12	150
442	SEG232	-908.5	407	12	150
443	SEG233	-931.5	407	12	150
444	SEG234	-954.5	407	12	150
445	SEG235	-977.5	407	12	150
446	SEG236	-1000.5	407	12	150
447	SEG237	-1023.5	407	12	150
448	SEG238	-1046.5	407	12	150
449	SEG239	-1069.5	407	12	150
450	SEG240	-1092.5	407	12	150
451	SEG241	-1115.5	407	12	150
452	SEG242	-1138.5	407	12	150
453	SEG243	-1161.5	407	12	150
454	SEG244	-1184.5	407	12	150
455	SEG245	-1207.5	407	12	150
456	SEG246	-1230.5	407	12	150
457	SEG247	-1253.5	407	12	150
458	SEG248	-1276.5	407	12	150
459	SEG249	-1299.5	407	12	150
460	SEG250	-1322.5	407	12	150
461	SEG251	-1345.5	407	12	150
462	SEG252	-1368.5	407	12	150
463	SEG253	-1391.5	407	12	150
464	SEG254	-1414.5	407	12	150
465	SEG255	-1437.5	407	12	150
466	SEG256	-1460.5	407	12	150
467	SEG257	-1483.5	407	12	150
468	SEG258	-1506.5	407	12	150
469	SEG259	-1529.5	407	12	150
470	SEG260	-1552.5	407	12	150
471	SEG261	-1575.5	407	12	150
472	SEG262	-1598.5	407	12	150
473	SEG263	-1621.5	407	12	150
474	SEG264	-1644.5	407	12	150
475	SEG265	-1667.5	407	12	150
476	SEG266	-1690.5	407	12	150
477	SEG267	-1713.5	407	12	150
478	SEG268	-1736.5	407	12	150
479	SEG269	-1759.5	407	12	150
480	SEG270	-1782.5	407	12	150
481	SEG271	-1805.5	407	12	150
482	SEG272	-1828.5	407	12	150
483	SEG273	-1851.5	407	12	150
484	SEG274	-1874.5	407	12	150
485	SEG275	-1897.5	407	12	150
486	SEG276	-1920.5	407	12	150
487	SEG277	-1943.5	407	12	150
488	SEG278	-1966.5	407	12	150
489	SEG279	-1989.5	407	12	150
490	SEG280	-2012.5	407	12	150
491	SEG281	-2035.5	407	12	150
492	SEG282	-2058.5	407	12	150

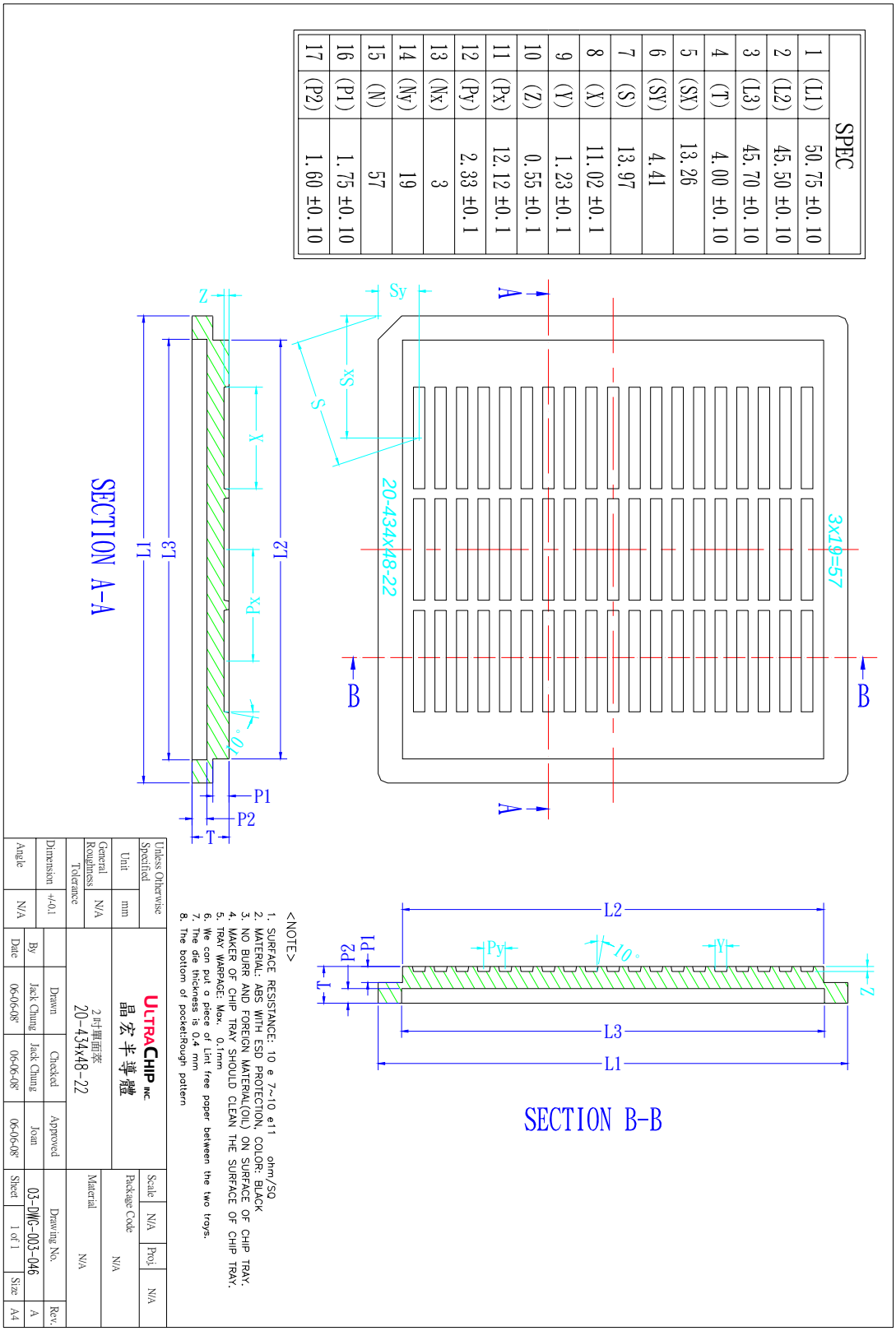
#	Pad	X	Y	W	H
493	SEG283	-2081.5	407	12	150
494	SEG284	-2104.5	407	12	150
495	SEG285	-2127.5	407	12	150
496	SEG286	-2150.5	407	12	150
497	SEG287	-2173.5	407	12	150
498	SEG288	-2196.5	407	12	150
499	SEG289	-2219.5	407	12	150
500	SEG290	-2242.5	407	12	150
501	SEG291	-2265.5	407	12	150
502	SEG292	-2288.5	407	12	150
503	SEG293	-2311.5	407	12	150
504	SEG294	-2334.5	407	12	150
505	SEG295	-2357.5	407	12	150
506	SEG296	-2380.5	407	12	150
507	SEG297	-2403.5	407	12	150
508	SEG298	-2426.5	407	12	150
509	SEG299	-2449.5	407	12	150
510	SEG300	-2472.5	407	12	150
511	SEG301	-2495.5	407	12	150
512	SEG302	-2518.5	407	12	150
513	SEG303	-2541.5	407	12	150
514	SEG304	-2564.5	407	12	150
515	SEG305	-2587.5	407	12	150
516	SEG306	-2610.5	407	12	150
517	SEG307	-2633.5	407	12	150
518	SEG308	-2656.5	407	12	150
519	SEG309	-2679.5	407	12	150
520	SEG310	-2702.5	407	12	150
521	SEG311	-2725.5	407	12	150
522	SEG312	-2748.5	407	12	150
523	SEG313	-2771.5	407	12	150
524	SEG314	-2794.5	407	12	150
525	SEG315	-2817.5	407	12	150
526	SEG316	-2840.5	407	12	150
527	SEG317	-2863.5	407	12	150
528	SEG318	-2886.5	407	12	150
529	SEG319	-2909.5	407	12	150
530	SEG320	-2932.5	407	12	150
531	SEG321	-2955.5	407	12	150
532	SEG322	-2978.5	407	12	150
533	SEG323	-3001.5	407	12	150
534	SEG324	-3024.5	407	12	150
535	SEG325	-3047.5	407	12	150
536	SEG326	-3070.5	407	12	150
537	SEG327	-3093.5	407	12	150
538	SEG328	-3116.5	407	12	150
539	SEG329	-3139.5	407	12	150
540	SEG330	-3162.5	407	12	150
541	SEG331	-3185.5	407	12	150
542	SEG332	-3208.5	407	12	150
543	SEG333	-3231.5	407	12	150
544	SEG334	-3254.5	407	12	150
545	SEG335	-3277.5	407	12	150
546	SEG336	-3300.5	407	12	150
547	SEG337	-3323.5	407	12	150
548	SEG338	-3346.5	407	12	150
549	SEG339	-3369.5	407	12	150
550	SEG340	-3392.5	407	12	150
551	SEG341	-3415.5	407	12	150
552	SEG342	-3438.5	407	12	150
553	SEG343	-3461.5	407	12	150
554	SEG344	-3484.5	407	12	150

#	Pad	X	Y	W	H
555	SEG345	-3507.5	407	12	150
556	SEG346	-3530.5	407	12	150
557	SEG347	-3553.5	407	12	150
558	SEG348	-3576.5	407	12	150
559	SEG349	-3599.5	407	12	150
560	SEG350	-3622.5	407	12	150
561	SEG351	-3645.5	407	12	150
562	SEG352	-3668.5	407	12	150
563	SEG353	-3691.5	407	12	150
564	SEG354	-3714.5	407	12	150
565	SEG355	-3737.5	407	12	150
566	SEG356	-3760.5	407	12	150
567	SEG357	-3783.5	407	12	150
568	SEG358	-3806.5	407	12	150
569	SEG359	-3829.5	407	12	150
570	SEG360	-3852.5	407	12	150
571	SEG361	-3875.5	407	12	150
572	SEG362	-3898.5	407	12	150
573	SEG363	-3921.5	407	12	150
574	SEG364	-3944.5	407	12	150
575	SEG365	-3967.5	407	12	150
576	SEG366	-3990.5	407	12	150
577	SEG367	-4013.5	407	12	150
578	SEG368	-4036.5	407	12	150
579	SEG369	-4059.5	407	12	150
580	SEG370	-4082.5	407	12	150
581	SEG371	-4105.5	407	12	150
582	SEG372	-4128.5	407	12	150
583	SEG373	-4151.5	407	12	150
584	SEG374	-4174.5	407	12	150
585	SEG375	-4197.5	407	12	150
586	SEG376	-4220.5	407	12	150
587	SEG377	-4243.5	407	12	150
588	SEG378	-4266.5	407	12	150
589	SEG379	-4289.5	407	12	150
590	SEG380	-4312.5	407	12	150
591	SEG381	-4335.5	407	12	150
592	SEG382	-4358.5	407	12	150
593	SEG383	-4381.5	407	12	150
594	SEG384	-4404.5	407	12	150
595	COM2	-4427.5	407	12	150
596	COM4	-4450.5	407	12	150
597	COM6	-4473.5	407	12	150
598	COM8	-4496.5	407	12	150
599	COM10	-4519.5	407	12	150
600	COM12	-4542.5	407	12	150
601	COM14	-4565.5	407	12	150
602	COM16	-4588.5	407	12	150
603	COM18	-4611.5	407	12	150
604	COM20	-4634.5	407	12	150
605	COM22	-4657.5	407	12	150
606	COM24	-4680.5	407	12	150
607	COM26	-4703.5	407	12	150
608	COM28	-4726.5	407	12	150
609	COM30	-4749.5	407	12	150
610	COM32	-4772.5	407	12	150
611	COM34	-4795.5	407	12	150
612	COM36	-4818.5	407	12	150
613	COM38	-4841.5	407	12	150
614	COM40	-4864.5	407	12	150
615	COM42	-4887.5	407	12	150
616	COM44	-4910.5	407	12	150

#	Pad	X	Y	W	H
617	COM46	-4933.5	407	12	150
618	COM48	-4956.5	407	12	150
619	COM50	-4979.5	407	12	150
620	COM52	-5002.5	407	12	150
621	COM54	-5025.5	407	12	150
622	COM56	-5048.5	407	12	150
623	COM58	-5071.5	407	12	150
624	COM60	-5094.5	407	12	150
625	COM62	-5117.5	407	12	150
626	COM64	-5140.5	407	12	150
627	COM66	-5163.5	407	12	150
628	COM68	-5186.5	407	12	150
629	COM70	-5209.5	407	12	150
630	DUMMY	-5232.5	407	12	150

TRAY INFORMATION

	SPEC
1 (L1)	50.75 ±0.10
2 (L2)	45.50 ±0.10
3 (L3)	45.70 ±0.10
4 (T)	4.00 ±0.10
5 (SX)	13.26
6 (SY)	4.41
7 (S)	13.97
8 (X)	11.02 ±0.1
9 (Y)	1.23 ±0.1
10 (Z)	0.55 ±0.1
11 (Px)	12.12 ±0.1
12 (Py)	2.33 ±0.1
13 (Nx)	3
14 (Ny)	19
15 (N)	57
16 (P1)	1.75 ±0.10
17 (P2)	1.60 ±0.10



<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e11 ohm/SQ
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: Max. 0.1mm
6. We can put a piece of Lint free paper between the two trays.
7. The die thickness is 0.4 mm
8. The bottom of pocket:Rough pattern

Unless Otherwise Specified		ULTRACHIP INC 晶宏半導體				Scale	N/A
Unit	mm	2吋單面盒 20-434x48-22				Proj.	N/A
General Roughness Tolerance	N/A					Package Code	N/A
Dimension	+/-0.1		Drawn	Checked	Approved	Material	N/A
Angle	N/A	By	Jack Chung	Jack Chung	Joan	Drawing No.	03-DWG-003-046
		Date	06-06-08	06-06-08	06-06-08	Sheet	1 of 1
						Size	A4
						Rev.	A

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	First Release	Oct. 15, 2008
0.7	(1) V_{DD} (Typical) is adjusted: 1.8V ~ 3.3V → 2.8V ~ 3.3V (Section "Feature Highlights", page 3; "Specifications" – DC Characteristics, page 54; "AC Characteristics", Pp 55~62)	Jan. 20, 2009
	(2) $V_{DD2/3}$ (Minimum) is adjusted: 2.5V → 2.7V $V_{DD2/3}$ (Typical) is adjusted: 2.4V ~ 3.3V → 2.8V ~ 3.3V (Section "Feature Highlights", page 3; "Specifications" – DC Characteristics, page 54)	
	(3) Some MTP names are corrected: MTP3 → MTP2, MTP2 → MTP1 MTP4 → MTP3, MTP5 → MTP4 (Section "MTP OPERATION FOR LCM MAKERS", Pp 47, 49~50)	
0.71	(1) Commands "Set LRM Enable" and "Set COM Scan Control" are added. (Section "Control Register" – LRM, CSC, page 12; "Command Table" – (8) (9), page 13; "Command Description" – (8) (9), page 16)	Apr. 27, 2009
0.72	(1) Bump Size Tolerance is adjusted: 2 uM → 2.5 uM (Section "Physical Dimensions", page 65)	May 12, 2009
0.73	(1) V_{DD} (Typical range) : 2.8V~3.3V → 1.8V~3.3V $V_{DD2/3}$ (Typical range) : 2.8V~3.3V → 2.6V~3.3V $V_{DD2/3}$ (Minimum) : 2.7V → 2.5V	Jul. 21, 2009
	(2) AC timing tables are updated accordingly. (pages 3, 55~60)	
	(3) Part Number : UC1697aGAA → UC1697aGAA_U2P (page 4)	
0.8	(1) V_{IH} (Minimum) : $0.8xV_{DD}$ → $0.85xV_{DD}$ (2) $R_{ON(SEG)}$ (Maximum) : 1300Ω → 1500Ω (3) $R_{ON(COM)}$ (Maximum) : 1300Ω → 1500Ω (4) $R_{ONS(COM)}$ is removed. (page 55)	Jul. 29, 2009
	(5) Power consumption data present : All-pixel-off (Maximum) : 1812 uA 2-pixel checker (Maximum) : 2660 uA (page 55)	
	(6) Some AC timings are updated. (Pp 56~59)	
0.81	(1) The "_" in part number for ordering is revised as "-". (page 4)	Jul. 31, 2009
1.0	(1) The DDRAM table is improved. (page 44)	Aug. 24, 2009
	(2) The Power-Up Sequence sub-section is updated. (page 47)	
	(3) A sub-section "Enter/Exit Sleep Mode Sequence" is added. (page 48)	
	(4) The RST timing page is updated. (page 62)	

APPENDIX : SHADE LOOKUP TABLE

Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default (Decimal)	Range
Set Shade0	0	0	1	0	1	1	0	0	1	0	Set Shade0[4:0]	0	0 ~ 31
			0	0	0	0	0	0	0	0			
			-	-	-	#	#	#	#	#			
Set Shade1	0	0	1	0	1	1	0	0	1	0	Set Shade1[4:0]	1	0 ~ 31
			0	0	0	0	0	0	0	1			
			-	-	-	#	#	#	#	#			
Set Shade2	0	0	1	0	1	1	0	0	1	0	Set Shade2[4:0]	2	0 ~ 31
			0	0	0	0	0	0	1	0			
			-	-	-	#	#	#	#	#			
Set Shade3	0	0	1	0	1	1	0	0	1	0	Set Shade3[4:0]	3	0 ~ 31
			0	0	0	0	0	0	1	1			
			-	-	-	#	#	#	#	#			
Set Shade4	0	0	1	0	1	1	0	0	1	0	Set Shade4[4:0]	4	0 ~ 31
			0	0	0	0	0	1	0	0			
			-	-	-	#	#	#	#	#			
Set Shade5	0	0	1	0	1	1	0	0	1	0	Set Shade5[4:0]	5	0 ~ 31
			0	0	0	0	0	1	0	1			
			-	-	-	#	#	#	#	#			
Set Shade6	0	0	1	0	1	1	0	0	1	0	Set Shade6[4:0]	6	0 ~ 31
			0	0	0	0	0	1	1	0			
			-	-	-	#	#	#	#	#			
Set Shade7	0	0	1	0	1	1	0	0	1	0	Set Shade7[4:0]	7	0 ~ 31
			0	0	0	0	0	1	1	1			
			-	-	-	#	#	#	#	#			
Set Shade8	0	0	1	0	1	1	0	0	1	0	Set Shade8[4:0]	8	0 ~ 31
			0	0	0	0	1	0	0	0			
			-	-	-	#	#	#	#	#			
Set Shade9	0	0	1	0	1	1	0	0	1	0	Set Shade9[4:0]	9	0 ~ 31
			0	0	0	0	1	0	0	1			
			-	-	-	#	#	#	#	#			
Set Shade10	0	0	1	0	1	1	0	0	1	0	Set Shade10[4:0]	10	0 ~ 31
			0	0	0	0	1	0	1	0			
			-	-	-	#	#	#	#	#			
Set Shade11	0	0	1	0	1	1	0	0	1	0	Set Shade11[4:0]	11	0 ~ 31
			0	0	0	0	1	0	1	1			
			-	-	-	#	#	#	#	#			
Set Shade12	0	0	1	0	1	1	0	0	1	0	Set Shade12[4:0]	12	0 ~ 31
			0	0	0	0	1	1	0	0			
			-	-	-	#	#	#	#	#			
Set Shade13	0	0	1	0	1	1	0	0	1	0	Set Shade13[4:0]	13	0 ~ 31
			0	0	0	0	1	1	0	1			
			-	-	-	#	#	#	#	#			
Set Shade14	0	0	1	0	1	1	0	0	1	0	Set Shade14[4:0]	14	0 ~ 31
			0	0	0	0	1	1	1	0			
			-	-	-	#	#	#	#	#			
Set Shade15	0	0	1	0	1	1	0	0	1	0	Set Shade15[4:0]	15	0 ~ 31
			0	0	0	0	1	1	1	1			
			-	-	-	#	#	#	#	#			
Set Shade16	0	0	1	0	1	1	0	0	1	0	Set Shade16[4:0]	16	0 ~ 31
			0	0	0	1	0	0	0	0			
			-	-	-	#	#	#	#	#			

Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default (Decimal)	Range
Set Shade17	0	0	1	0	1	1	0	0	1	0	Set Shade17[4:0]	17	0 ~ 31
			0	0	0	1	0	0	0	1			
			-	-	-	#	#	#	#	#			
Set Shade18	0	0	1	0	1	1	0	0	1	0	Set Shade18[4:0]	18	0 ~ 31
			0	0	0	1	0	0	1	0			
			-	-	-	#	#	#	#	#			
Set Shade19	0	0	1	0	1	1	0	0	1	0	Set Shade19[4:0]	19	0 ~ 31
			0	0	0	1	0	0	1	1			
			-	-	-	#	#	#	#	#			
Set Shade20	0	0	1	0	1	1	0	0	1	0	Set Shade20[4:0]	20	0 ~ 31
			0	0	0	1	0	1	0	0			
			-	-	-	#	#	#	#	#			
Set Shade21	0	0	1	0	1	1	0	0	1	0	Set Shade21[4:0]	21	0 ~ 31
			0	0	0	1	0	1	0	1			
			-	-	-	#	#	#	#	#			
Set Shade22	0	0	1	0	1	1	0	0	1	0	Set Shade22[4:0]	22	0 ~ 31
			0	0	0	1	0	1	1	0			
			-	-	-	#	#	#	#	#			
Set Shade23	0	0	1	0	1	1	0	0	1	0	Set Shade23[4:0]	23	0 ~ 31
			0	0	0	1	0	1	1	1			
			-	-	-	#	#	#	#	#			
Set Shade24	0	0	1	0	1	1	0	0	1	0	Set Shade24[4:0]	24	0 ~ 31
			0	0	0	1	1	0	0	0			
			-	-	-	#	#	#	#	#			
Set Shade25	0	0	1	0	1	1	0	0	1	0	Set Shade25[4:0]	25	0 ~ 31
			0	0	0	1	1	0	0	1			
			-	-	-	#	#	#	#	#			
Set Shade26	0	0	1	0	1	1	0	0	1	0	Set Shade26[4:0]	26	0 ~ 31
			0	0	0	1	1	0	1	0			
			-	-	-	#	#	#	#	#			
Set Shade27	0	0	1	0	1	1	0	0	1	0	Set Shade27[4:0]	27	0 ~ 31
			0	0	0	1	1	0	1	1			
			-	-	-	#	#	#	#	#			
Set Shade28	0	0	1	0	1	1	0	0	1	0	Set Shade28[4:0]	28	0 ~ 31
			0	0	0	1	1	1	0	0			
			-	-	-	#	#	#	#	#			
Set Shade29	0	0	1	0	1	1	0	0	1	0	Set Shade29[4:0]	29	0 ~ 31
			0	0	0	1	1	1	0	1			
			-	-	-	#	#	#	#	#			
Set Shade30	0	0	1	0	1	1	0	0	1	0	Set Shade30[4:0]	30	0 ~ 31
			0	0	0	1	1	1	1	0			
			-	-	-	#	#	#	#	#			
Set Shade31	0	0	1	0	1	1	0	0	1	0	Set Shade31[4:0]	31	0 ~ 31
			0	0	0	1	1	1	1	1			
			-	-	-	#	#	#	#	#			

Shade	Value	Default	Range
G Shade0	Shade0 + Shade0	0	0~62
G Shade1	Shade0 + Shade1	1	0~62
G Shade2	Shade1 + Shade1	2	0~62
G Shade3	Shade1 + Shade2	3	0~62
G Shade4	Shade2 + Shade2	4	0~62
G Shade5	Shade2 + Shade3	5	0~62
G Shade6	Shade3 + Shade3	6	0~62
G Shade7	Shade3 + Shade4	7	0~62
G Shade8	Shade4 + Shade4	8	0~62
G Shade9	Shade4 + Shade5	9	0~62
G Shade10	Shade5 + Shade5	10	0~62
G Shade11	Shade5 + Shade6	11	0~62
G Shade12	Shade6 + Shade6	12	0~62
G Shade13	Shade6 + Shade7	13	0~62
G Shade14	Shade7 + Shade7	14	0~62
G Shade15	Shade7 + Shade8	15	0~62
G Shade16	Shade8 + Shade8	16	0~62
G Shade17	Shade8 + Shade9	17	0~62
G Shade18	Shade9 + Shade9	18	0~62
G Shade19	Shade9 + Shade10	19	0~62
G Shade20	Shade10 + Shade10	20	0~62
G Shade21	Shade10 + Shade11	21	0~62
G Shade22	Shade11 + Shade11	22	0~62
G Shade23	Shade11 + Shade12	23	0~62
G Shade24	Shade12 + Shade12	24	0~62
G Shade25	Shade12 + Shade13	25	0~62
G Shade26	Shade13 + Shade13	26	0~62
G Shade27	Shade13 + Shade14	27	0~62
G Shade28	Shade14 + Shade14	28	0~62
G Shade29	Shade14 + Shade15	29	0~62
G Shade30	Shade15 + Shade15	30	0~62
G Shade31	Shade15 + Shade16	31	0~62
G Shade32	Shade16 + Shade16	32	0~62
G Shade33	Shade16 + Shade17	33	0~62
G Shade34	Shade17 + Shade17	34	0~62
G Shade35	Shade17 + Shade18	35	0~62
G Shade36	Shade18 + Shade18	36	0~62
G Shade37	Shade18 + Shade19	37	0~62
G Shade38	Shade19 + Shade19	38	0~62
G Shade39	Shade19 + Shade20	39	0~62
G Shade40	Shade20 + Shade20	40	0~62
G Shade41	Shade20 + Shade21	41	0~62
G Shade42	Shade21 + Shade21	42	0~62
G Shade43	Shade21 + Shade22	43	0~62
G Shade44	Shade22 + Shade22	44	0~62
G Shade45	Shade22 + Shade23	45	0~62
G Shade46	Shade23 + Shade23	46	0~62
G Shade47	Shade23 + Shade24	47	0~62
G Shade48	Shade24 + Shade24	48	0~62
G Shade49	Shade24 + Shade25	49	0~62
G Shade50	Shade25 + Shade25	50	0~62
G Shade51	Shade25 + Shade26	51	0~62
G Shade52	Shade26 + Shade26	52	0~62
G Shade53	Shade26 + Shade27	53	0~62
G Shade54	Shade27 + Shade27	54	0~62
G Shade55	Shade27 + Shade28	55	0~62
G Shade56	Shade28 + Shade28	56	0~62
G Shade57	Shade28 + Shade29	57	0~62
G Shade58	Shade29 + Shade29	58	0~62
G Shade59	Shade29 + Shade30	59	0~62
G Shade60	Shade30 + Shade30	60	0~62
G Shade61	Shade30 + Shade31	61	0~62
G Shade62	2*Shade31	62	0~62
G Shade63	2*Shade31 + 1	63	1~63

Shade	Value	Default	Range
R/B Shade0	Shade0	0	0~31
R/B Shade1	Shade1	1	0~31
R/B Shade2	Shade2	2	0~31
R/B Shade3	Shade3	3	0~31
R/B Shade4	Shade4	4	0~31
R/B Shade5	Shade5	5	0~31
R/B Shade6	Shade6	6	0~31
R/B Shade7	Shade7	7	0~31
R/B Shade8	Shade8	8	0~31
R/B Shade9	Shade9	9	0~31
R/B Shade10	Shade10	10	0~31
R/B Shade11	Shade11	11	0~31
R/B Shade12	Shade12	12	0~31
R/B Shade13	Shade13	13	0~31
R/B Shade14	Shade14	14	0~31
R/B Shade15	Shade15	15	0~31
R/B Shade16	Shade16	16	0~31
R/B Shade17	Shade17	17	0~31
R/B Shade18	Shade18	18	0~31
R/B Shade19	Shade19	19	0~31
R/B Shade20	Shade20	20	0~31
R/B Shade21	Shade21	21	0~31
R/B Shade22	Shade22	22	0~31
R/B Shade23	Shade23	23	0~31
R/B Shade24	Shade24	24	0~31
R/B Shade25	Shade25	25	0~31
R/B Shade26	Shade26	26	0~31
R/B Shade27	Shade27	27	0~31
R/B Shade28	Shade28	28	0~31
R/B Shade29	Shade29	29	0~31
R/B Shade30	Shade30	30	0~31
R/B Shade31	Shade31	31	0~31