SSD1623

Product Preview

96 Segments with Common
3-Level Generic Display Driver
CMOS

CONTENTS

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FIGURES

1 GENERAL DESCRIPTION

SSD1623 is a CMOS generic display driver with controller. It has 95 segments, 1 background segment and 1 common output. Each segment / common is capable of 3-voltage levels output.

SSD1623 is designed for SPI interface with hardware address map setting pin, allowing two SSD1623 connected to same SPI bus, increasing the available number of segments.

SSD1623 embeds with flexible and power saving DC/DC to general high voltage for panel driving. VCI regulator is embedded to accept direct power supply from Lithium battery. Battery voltage and IC temperature sensor are built.

2 FEATURES

- 3-level output generic driver: V0, V1 and VSS. Each pin level can be individually programmed to V0, V1, VSS or Hi-Z.
- Power supply
  - VDD: 2.0 to 3.6V (Logic operation)
  - VDDIO: 2.0 to VDD (MCU interface)
  - V0: 10 to 40V (High voltage panel driving)
  - VCI: 2.4 to 3.6V (Charge pump and analog power supply)
  - VBAT: 2.8 to 4.5V (Li battery supply)
- VBAT can be supplied directly from Li – battery when option VCI regulator is used.
- Lower power DC/DC with maximum output voltage 38V
- Circuit selectable DC/DC multiplier ratio (16x, 12x, 8x, 6x, 4x)
- Adjustable DC/DC output voltage in step of 1V
- V0 can be supplied from internal DC/DC or external power supply
- Output channel
  - 95 segments (SEG[95:1]) for normal segment/icon driving
  - 1 background segment (SEG[0]) Background segment (4 times driving power)
  - 1 common segment (COM) Common signal
- 32-bit SPI interface with address map setting pin
- Dual frame display memory 96 x 2 bits, (Previous and Current)
- Built in oscillator or external clock inputs
- Built in programmable frequency divider to divide external clock signal (4Mhz to 32 kHz) for IC operations
- Programmable waveform
- Temperature sensing function,
- Battery voltage sensing
- Design for wire bond package, 69um pad pitch minimum

3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD1623V	Bare die, 200um, on waffle pack
SSD1623Z	Au bumped die

4 BLOCK DIAGRAM

Figure 4-1: SSD1623 Block Diagram

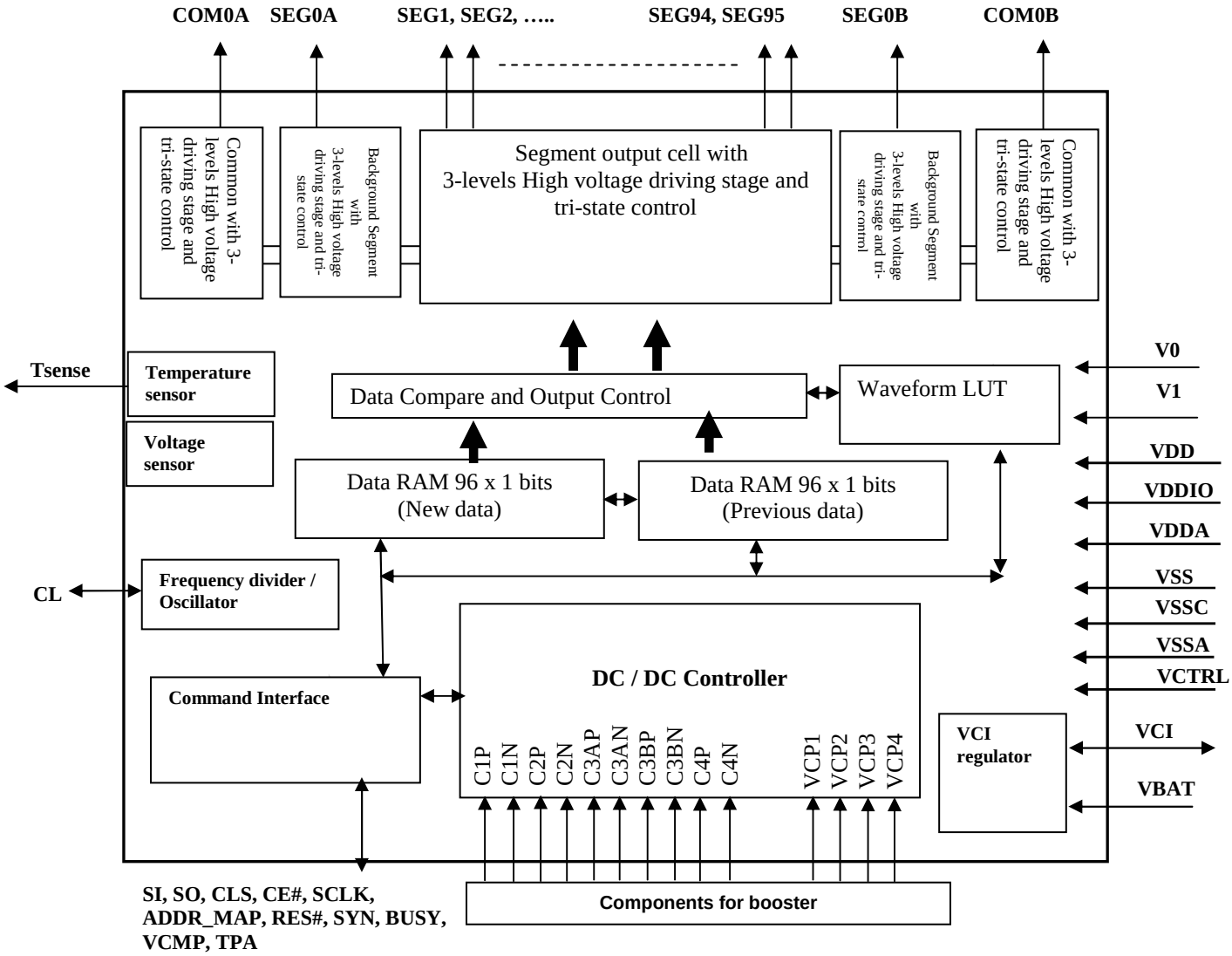
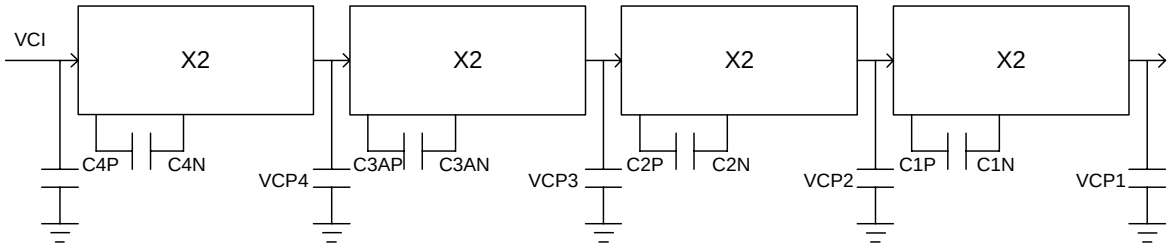
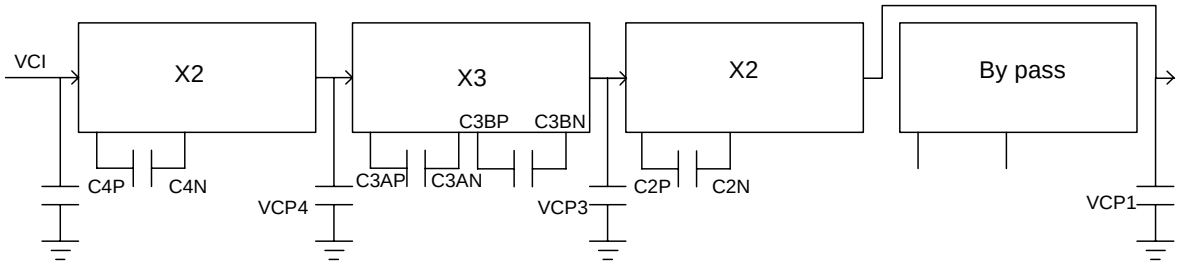


Figure 4-2: SSD1623 DC/DC Block Diagram

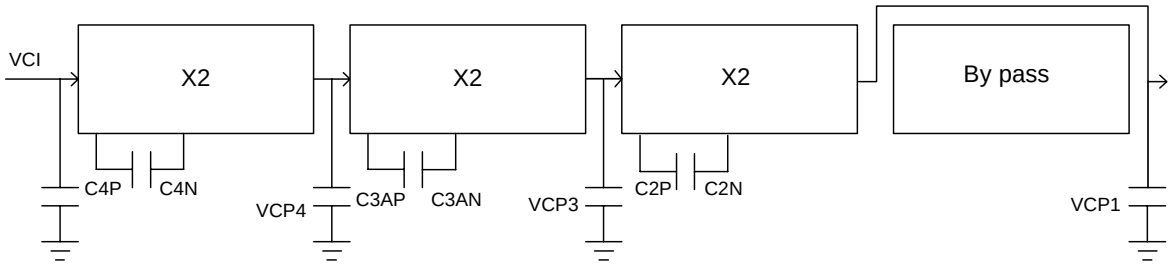
16x Configurations



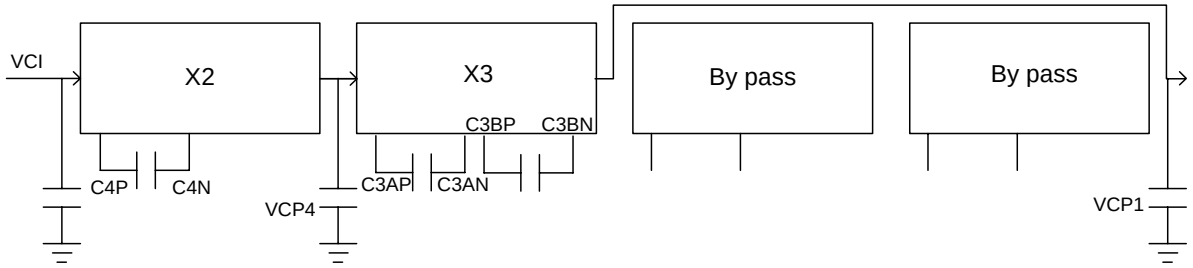
12x Configurations



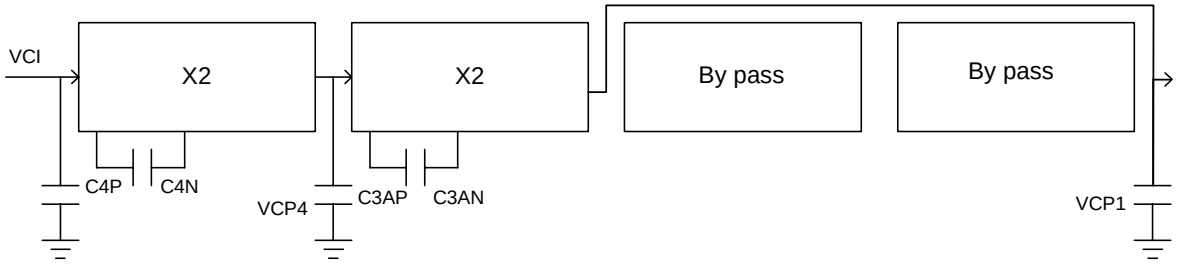
8x Configurations



6x Configurations



4x Configurations



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1623 layout diagram (Pad face up)

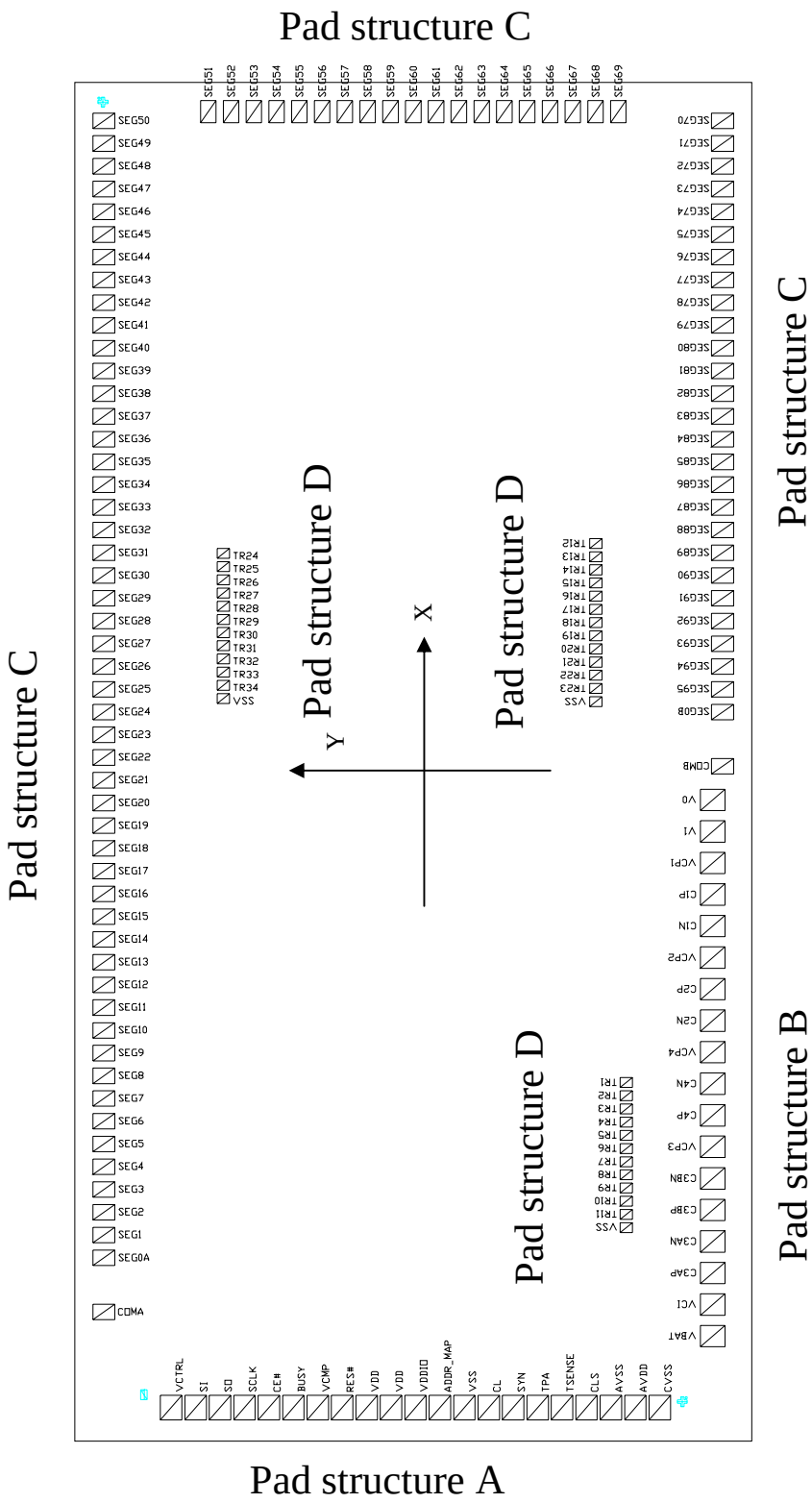


Figure 5-2 : SSD1623V- Bare chip pad layout

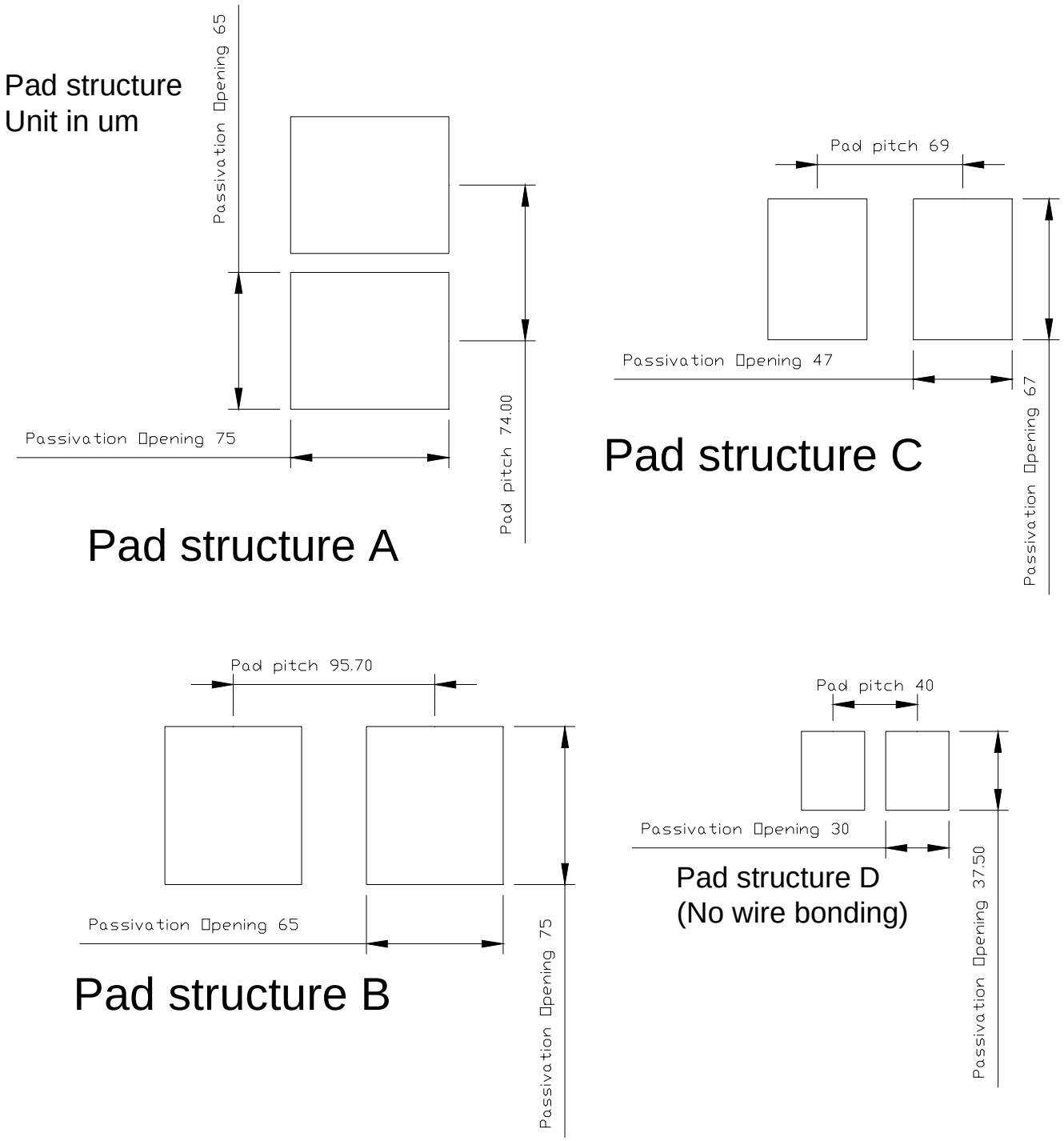


Figure 5-3 : SSD1623Z – Gold bumped chip pad layout

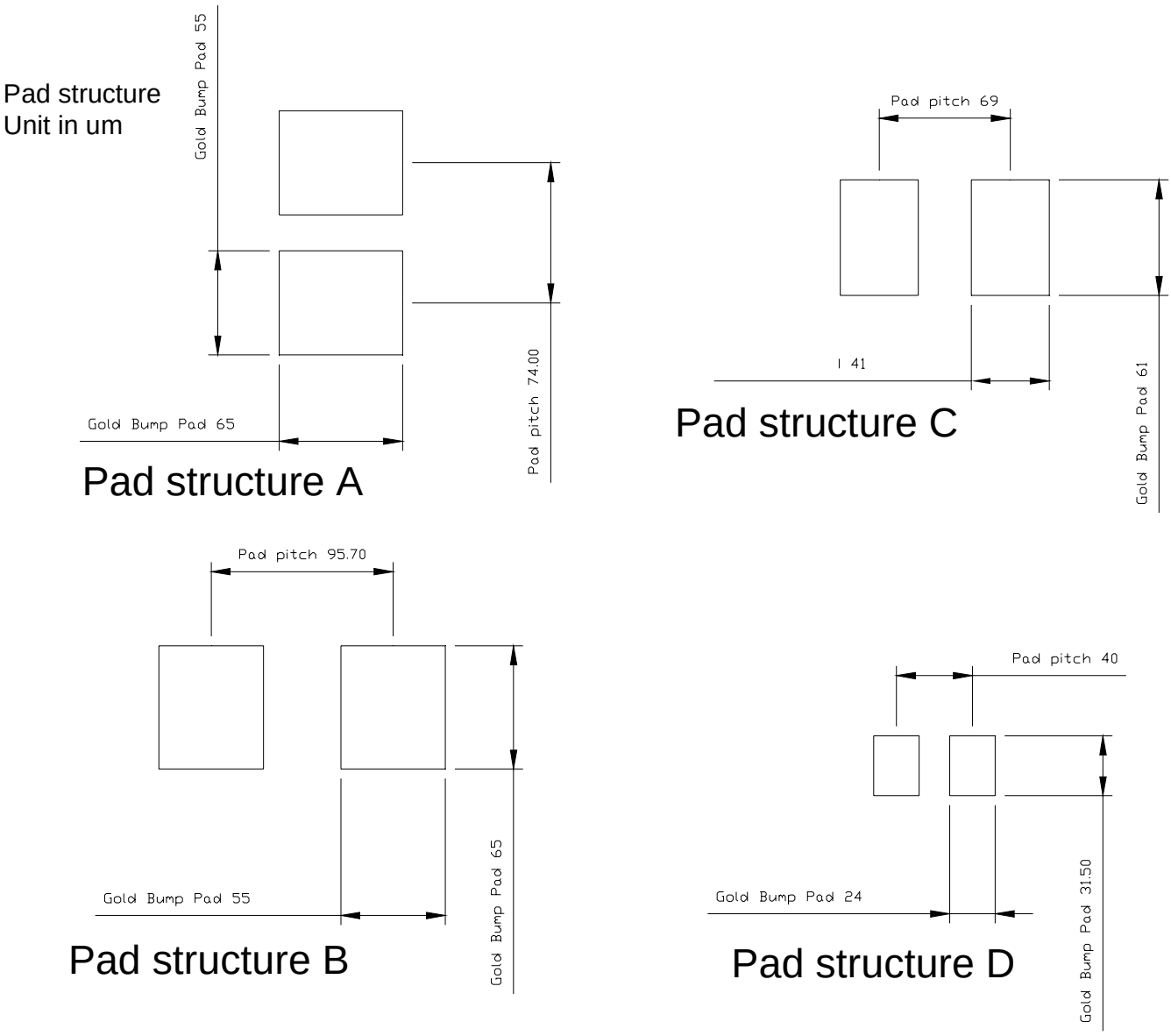


Figure 5-4 : SSD1623 alignment mark

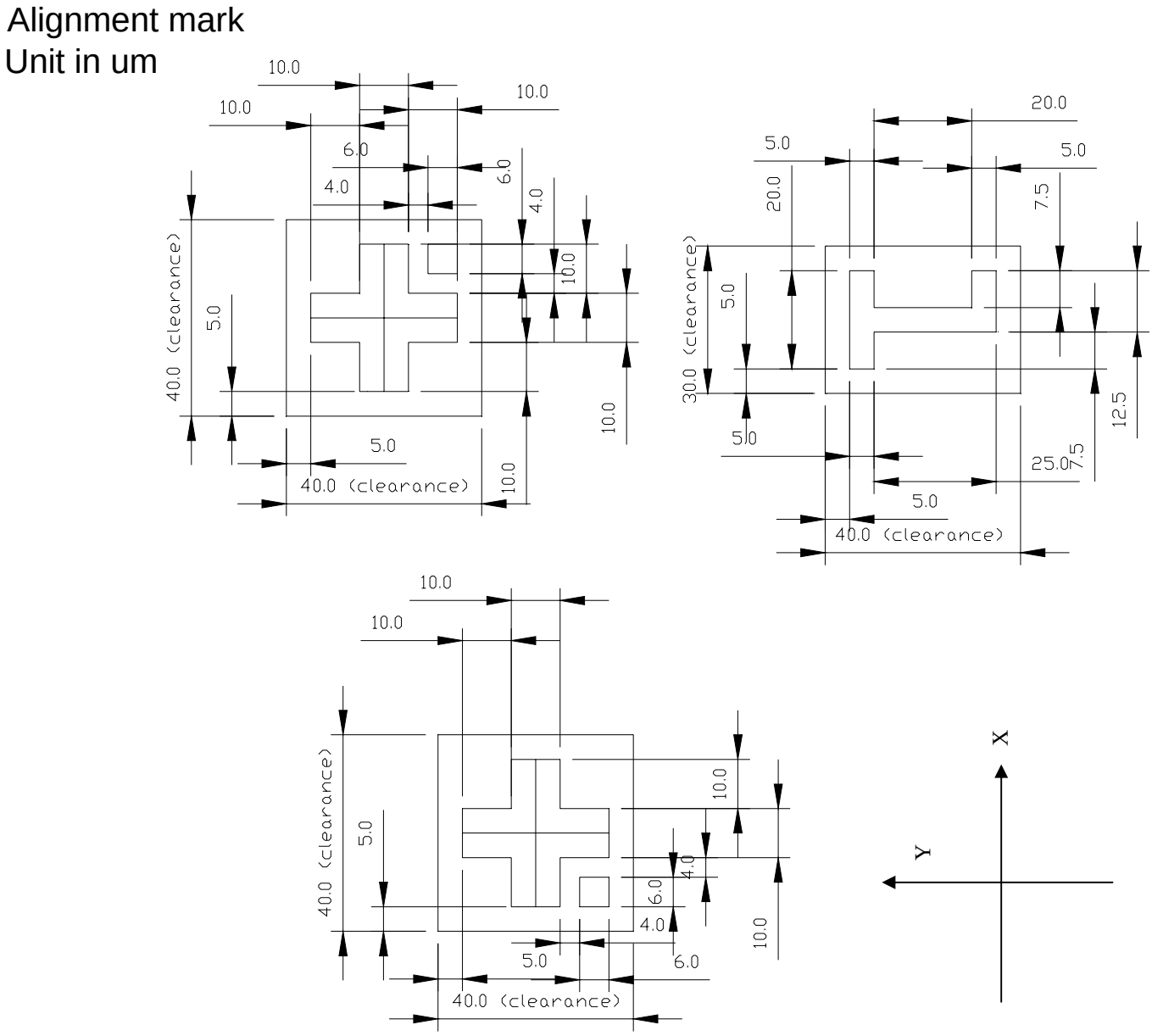
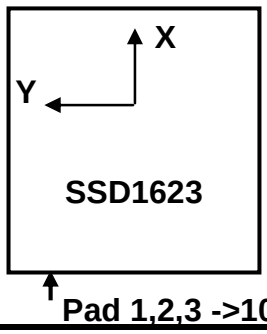


Table 5-1: SSD1623 pad coordinates

Pad No	Pin Name	X	Y
1	VCTRL	-1959.8	733.3
2	SI	-1959.8	659.3
3	SO	-1959.8	585.3
4	SCLK	-1959.8	511.3
5	CE#	-1959.8	437.3
6	BUSY	-1959.8	363.3
7	VCMP	-1959.8	289.3
8	RES#	-1959.8	215.3
9	VDD	-1959.8	141.3
10	VDD	-1959.8	67.3
11	VDDIO	-1959.8	-6.7
12	ADDR_MAP	-1959.8	-80.7
13	VSS	-1959.8	-154.7
14	CL	-1959.8	-228.7
15	SYN	-1959.8	-302.7
16	TPA	-1959.8	-376.7
17	TSENSE	-1959.8	-450.7
18	CLS	-1959.8	-524.7
19	VSSA	-1959.8	-598.7
20	VDDA	-1959.8	-672.7
21	VSSC	-1959.8	-746.7
22	VBAT	-1742.8	-907.0
23	VCI	-1647.1	-907.0
24	C3AP	-1551.4	-907.0
25	C3AN	-1455.7	-907.0
26	C3BP	-1360.0	-907.0
27	C3BN	-1264.3	-907.0
28	VCP3	-1168.6	-907.0
29	C4P	-1072.9	-907.0
30	C4N	-977.2	-907.0
31	VCP4	-881.5	-907.0
32	C2N	-785.8	-907.0
33	C2P	-690.1	-907.0
34	VCP2	-594.4	-907.0
35	C1N	-498.7	-907.0
36	C1P	-403.0	-907.0
37	VCP1	-307.3	-907.0
38	V1	-211.6	-907.0
39	V0	-115.9	-907.0
40	COMB	-13.6	-937.0
41	SEG0B	150.9	-937.0
42	SEG95	219.9	-937.0
43	SEG94	288.9	-937.0
44	SEG93	357.9	-937.0
45	SEG92	426.9	-937.0
46	SEG91	495.9	-937.0
47	SEG90	564.9	-937.0
48	SEG89	633.9	-937.0
49	SEG88	702.9	-937.0
50	SEG87	771.9	-937.0
51	SEG86	840.9	-937.0
52	SEG85	909.9	-937.0
53	SEG84	978.9	-937.0
54	SEG83	1047.9	-937.0
55	SEG82	1116.9	-937.0
56	SEG81	1185.9	-937.0
57	SEG80	1254.9	-937.0
58	SEG79	1323.9	-937.0
59	SEG78	1392.9	-937.0
60	SEG77	1461.9	-937.0
61	SEG76	1530.9	-937.0
62	SEG75	1599.9	-937.0
63	SEG74	1668.9	-937.0
64	SEG73	1737.9	-937.0
65	SEG72	1806.9	-937.0
66	SEG71	1875.9	-937.0
67	SEG70	1944.9	-937.0

Pad No	Pin Name	X	Y
68	SEG69	1973.0	-621.0
69	SEG68	1973.0	-552.0
70	SEG67	1973.0	-483.0
71	SEG66	1973.0	-414.0
72	SEG65	1973.0	-345.0
73	SEG64	1973.0	-276.0
74	SEG63	1973.0	-207.0
75	SEG62	1973.0	-138.0
76	SEG61	1973.0	-69.0
77	SEG60	1973.0	0.0
78	SEG59	1973.0	69.0
79	SEG58	1973.0	138.0
80	SEG57	1973.0	207.0
81	SEG56	1973.0	276.0
82	SEG55	1973.0	345.0
83	SEG54	1973.0	414.0
84	SEG53	1973.0	483.0
85	SEG52	1973.0	552.0
86	SEG51	1973.0	621.0

Pad No	Pin Name	X	Y
87	SEG50	1944.9	937.0
88	SEG49	1875.9	937.0
89	SEG48	1806.9	937.0
90	SEG47	1737.9	937.0
91	SEG46	1668.9	937.0
92	SEG45	1599.9	937.0
93	SEG44	1530.9	937.0
94	SEG43	1461.9	937.0
95	SEG42	1392.9	937.0
96	SEG41	1323.9	937.0
97	SEG40	1254.9	937.0
98	SEG39	1185.9	937.0
99	SEG38	1116.9	937.0
100	SEG37	1047.9	937.0
101	SEG36	978.9	937.0
102	SEG35	909.9	937.0
103	SEG34	840.9	937.0
104	SEG33	771.9	937.0
105	SEG32	702.9	937.0
106	SEG31	633.9	937.0
107	SEG30	564.9	937.0
108	SEG29	495.9	937.0
109	SEG28	426.9	937.0
110	SEG27	357.9	937.0
111	SEG26	288.9	937.0
112	SEG25	219.9	937.0
113	SEG24	150.9	937.0
114	SEG23	81.9	937.0
115	SEG22	12.9	937.0
116	SEG21	-56.1	937.0
117	SEG20	-125.1	937.0
118	SEG19	-194.1	937.0
119	SEG18	-263.1	937.0
120	SEG17	-332.1	937.0
121	SEG16	-401.1	937.0
122	SEG15	-470.1	937.0
123	SEG14	-539.1	937.0
124	SEG13	-608.1	937.0
125	SEG12	-677.1	937.0
126	SEG11	-746.1	937.0
127	SEG10	-815.1	937.0
128	SEG9	-884.1	937.0
129	SEG8	-953.1	937.0
130	SEG7	-1022.1	937.0
131	SEG6	-1091.1	937.0
132	SEG5	-1160.1	937.0
133	SEG4	-1229.1	937.0
134	SEG3	-1298.1	937.0
135	SEG2	-1367.1	937.0
136	SEG1	-1436.1	937.0
137	SEG0A	-1505.1	937.0
138	COMA	-1669.6	937.0



Die size	4.2mm x 2.1mm
Bump height (SSD1623Z)	15um
IC thickness	200um

SSD1623V Pad size:

Pad number	Pad size
1 -21	75um x 65um
22-39	65um x 75um
40-67, 87-138	47um x67um
68-86	67um x 47um

SSD1623Z Pad size:

Pad number	Pad size
1 -21	65um x 55um
22-39	55um x 65um
40-67, 87-138	41um x61um
68-86	61um x 41um

Alignment Mark:

Type	Size	Coordinate (Centre of marks)
+ shape	30um x 30um	2001.8, 939.8
+ shape	30um x 30um	-1942.0, -815.1
pin1	30um x 20um	-1920.8, 816.3

6 Pin Description

Pin name	Type	Description
VDD	Power	Power supply for IC digital circuit. It should be connected to VDDA
VDDIO	Power	Power supply for MCU interface block.
VDDA	Power	Power supply for IC analog circuit. It should be connected to VDD
VCI	Power	Analog power supply, also act as VCI regulator output pin
VBAT	Power	Battery power input. Connect to power supply when using VCI regulator
VSS	Power	Ground pin of IC. VSS should connected with VSSC and VSSA
VSSC	Power	Ground pin of charge pump circuit. VSSC should connected with VSS and VSSA
VSSA	Power	Ground pin of analog circuit. VSSA should connected with VSSC and VSS
SI	Digital	Data input to IC for SPI interface
SO	Digital	Data output from IC for SPI interface
CE#	Digital	Chip Enable for SPI interface
SCLK	Digital	Clock signal for SPI interface
ADDR_MAP	Digital	Address mapping pin to choose different addressing (upper address or lower address) of SPI interface. Connect to VDDIO when normal operation. *Internal clock can not be enabled when ADDR_MAP=VSS
RES#	Digital	Hardware Reset Pin
CLS	Digital	Internal Clock enable pin. Internal clock is enabled when this pin and ADDR_MAP are pulled high. External clock is selected when this pin is pulled low. Connect both CLS pins of master and slave ICs for cascading mode
CL	Digital	System Clock input pin. Connect both CL pins of master and slave ICs for cascading mode
SYN	Digital	Connect both SYN pins of master and slave ICs for cascading mode
TPA	Digital	Testing reserved. Keep NC during normal operation
VCTRL	Digital	VDD and VDDA power cut off pin. VDD and VDDA are cut off when this pin is pulled low. VDD and VDDA are connected to IC when this pin is pulled high. * Memory will be lost when VDD and VDDA cut off.
TSENSE	Analog	Testing reserved
C1P	Analog	Charge pump pin for flying capacitor
C1N	Analog	Charge pump pin for flying capacitor
C2P	Analog	Charge pump pin for flying capacitor
C2N	Analog	Charge pump pin for flying capacitor
C3AP	Analog	Charge pump pin for flying capacitor
C3AN	Analog	Charge pump pin for flying capacitor
C3BP	Analog	Charge pump pin for flying capacitor
C3BN	Analog	Charge pump pin for flying capacitor
C4P	Analog	Charge pump pin for flying capacitor
C4N	Analog	Charge pump pin for flying capacitor
VCP1	Analog	Charge pump pin for storage capacitor
VCP2	Analog	Charge pump pin for storage capacitor
VCP3	Analog	Charge pump pin for storage capacitor
VCP4	Analog	Charge pump pin for storage capacitor
V0	Power	Voltage power pin for segment and common driving
V1	Power	Voltage power pin for segment and common driving
SEG[95:1]	Output	Segment output
SEG0A SEG0B	Output	Background segment output
COM0A COM0B	Output	Common output pins

Pin name	Type	Description
TR[34:0]	Digital	Testing reserved
BUSY	Digital	Busy status output pin
VCMP	Digital	Testing reserved.

7 FUNCTIONAL BLOCK DESCRIPTION

7.1 MCU Serial Interface

The IC has a slave SPI interface, which is comprised of 4 signals, plus one configuration pin:

SI — Data input to display driver IC.
SO — Data output from display driver IC.
SCLK — SPI Clock. Input to display driver.
CE# — Chip enable. Input to display driver.
ADDR_MAP — Indicates whether the IC use upper address (*ADDR_MAP*=1) or lower address (*ADDR_MAP*=0) in address space

SPI transactions are 32 bits in length. These 32 bits are organized into several fields.

The first field is a single bit (the first bit of the transaction) that indicates whether the transfer is a read or a write action (high for a write).

The next field is the address field. This field is comprised of 6 bits (A0-A5—the 2nd through the 7th bits of the SPI transaction). The address indicates the data register that is to be accessed (read from and possibly written to).

Addresses 0x00, 0x03, 0x08 and 0x14 to 0x1B are special "command" registers, which contain a set of command bits that control the operation of the IC. The command register is accessed any time and are written to —regardless of the state of the ADDR_MAP pin (whether ADDR_MAP is high or low).

The ADDR_MAP pin indicates whether the IC is mapped to the low memory locations (addresses b000000-b011111) or the high memory locations (b100000-b111111). If the ADDR_MAP pin is low, the IC should only decode addresses where the Address5 bit is low. If the ADDR_MAP pin is high, then the IC should decode addresses where Address5 is high.

The next field in the SPI transaction (the 7th bit) is a special bit called the "dead" bit. It is essentially a placeholder and does not contain any data. This placeholder allows a full clock period for the address to be decoded by the logic before receiving the data portion of the transaction.

The final field is comprised of 24 bits of data (D0-D23). This is the data that is written to (in a write transaction) and read from whatever address register is encoded in A0-A6. If an address is decoded for a register which is not physically realized in the IC, then logic zeros will be output on the SO pin for the remainder of the transaction.

Field	# of bits	Content
1	1	Read / Write
2	6	Address (IC and register)
3	1	Dead bit
4	24	Data / Command
Total	**32**	

Figure 7-1: Sample SPI Transfer

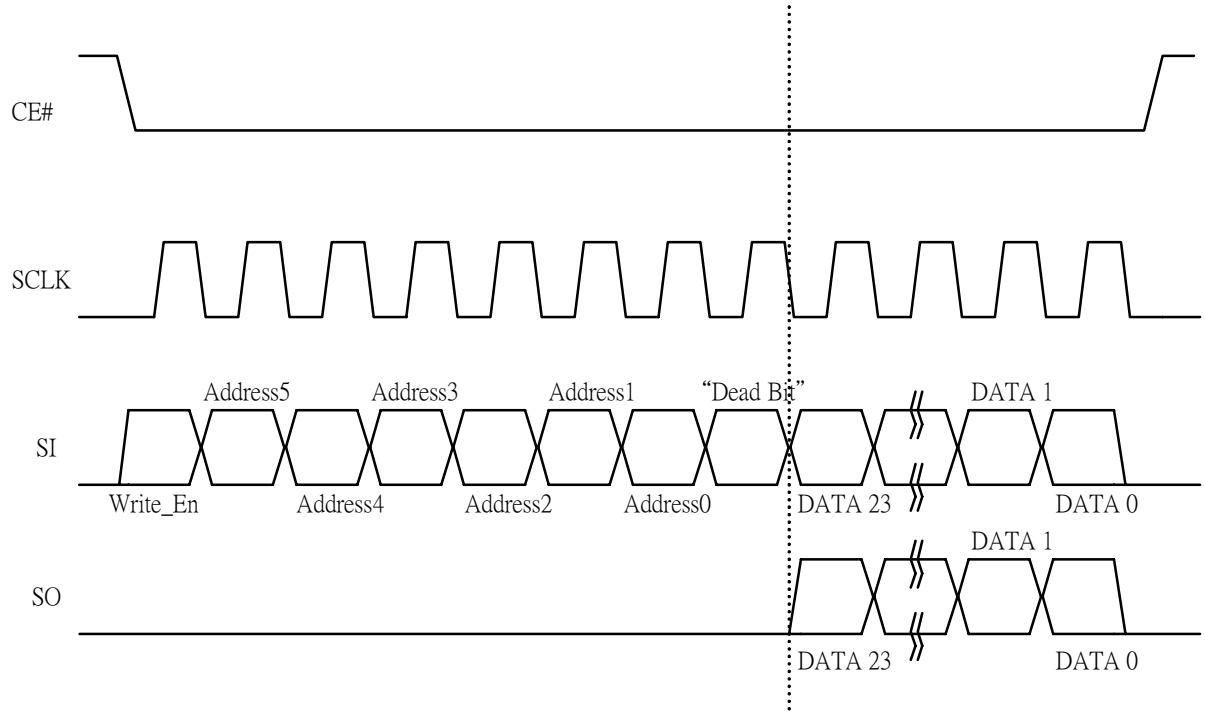
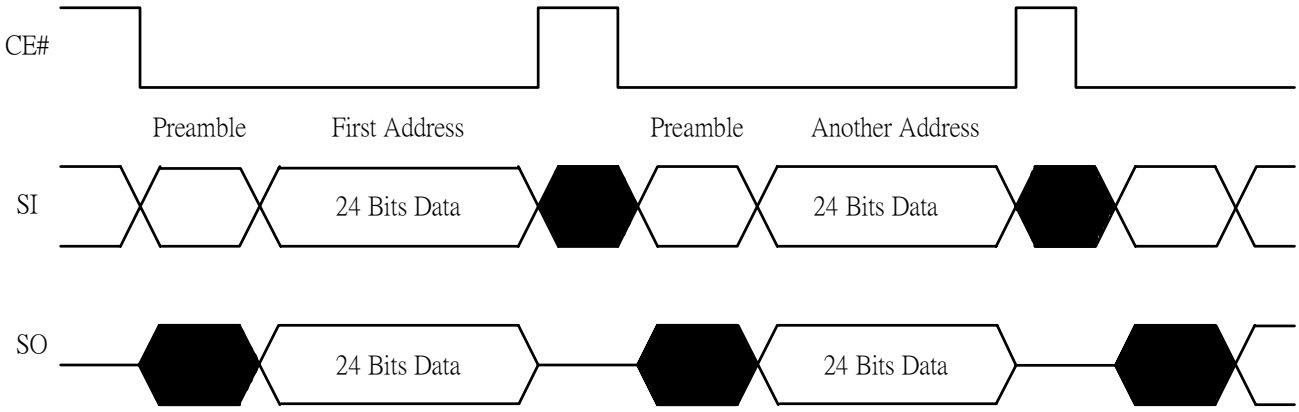


Figure 7-2: Consecutive SPI Transfers



8 Register Table.

Table 8-1: Register Table

Register Address	Register Name	Description	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	Update	Display update		Update	Output off	Polarity	Inverse	test_update[3]	test_update[2]	test_update[1]	test_update[0]											Phase1_en	Phase2_en	Phase3_en	Phase4_en	Phase5_en
01																										
02																										
03	Clock	Overall timing scaling					Osc_En	E_CLK_DIV[2]	E_CLK_DIV[1]	E_CLK_DIV[0]	CLK_Base[3]	CLK_Base[2]	CLK_Base[1]	CLK_Base[0]												
04																										
05																										
06																										
07																										
08	Reset	Reset	SW_Reset[1]	SW_Reset[0]	lock1	lock0																				
09	DC/DC 2	Booster voltage	DC_Volt[4]	DC_Volt[3]	DC_Volt[2]	DC_Volt[1]	DC_Volt[0]			DOFF_out[1]	DOFF_out[0]	VTH[2]	VTH[1]	VTH[0]												
0A	DC/DC 1	Analog Control	VCI_En	DCDC_En	DCDis_En	Bias_En	HVBuff_En	TSEN_out	TADC_En[1]	TADC_En[0]	DCDis[1]	DCDis[0]	VSEN_En	st2en	st3en	st4en	st2bypass	st3bypass	st4bypass	st2x3	Reg_en					
0B	Status	Read Status	TSEN[6]	TSEN[5]	TSEN[4]	TSEN[3]	TSEN[2]	TSEN[1]	TSEN[0]			BUSY		VSEN[2]	VSEN[1]	VSEN[0]										
0C	HiZ register 0	SEG[23:0]	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
0D	HiZ register 1	SEG[47:24]	S47	S46	S45	S44	S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32	S31	S30	S29	S28	S27	S26	S25	S24
0E	HiZ register 2	SEG[71:48]	S71	S70	S69	S68	S67	S66	S65	S64	S63	S62	S61	S60	S59	S58	S57	S56	S55	S54	S53	S52	S51	S50	S49	S48
0F	HiZ register 3	SEG[95:72]	S95	S94	S93	S92	S91	S90	S89	S88	S87	S86	S85	S84	S83	S82	S81	S80	S79	S78	S77	S76	S75	S74	S73	S72
10	Data register 0	SEG[23:0]	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
11	Data register 1	SEG[47:24]	S47	S46	S45	S44	S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32	S31	S30	S29	S28	S27	S26	S25	S24
12	Data register 2	SEG[71:48]	S71	S70	S69	S68	S67	S66	S65	S64	S63	S62	S61	S60	S59	S58	S57	S56	S55	S54	S53	S52	S51	S50	S49	S48
13	Data register 3	SEG[95:72]	S95	S94	S93	S92	S91	S90	S89	S88	S87	S86	S85	S84	S83	S82	S81	S80	S79	S78	S77	S76	S75	S74	S73	S72
14	Waveform LUT1	Waveform LUT1	DLH_V1[1]	DLH_V1[0]	DHH_V1[1]	DHH_V1[0]	DHL_V1[1]	DHL_V1[0]	DLL_V1[1]	DLL_V1[0]	C_V1[1]	C_V1[0]	DLH_V2[1]	DLH_V2[0]	DHH_V2[1]	DHH_V2[0]	DHL_V2[1]	DHL_V2[0]	DLL_V2[1]	DLL_V2[0]	C_V2[1]	C_V2[0]	RPT1[3]	RPT1[2]	RPT1[1]	RPT1[0]
15	Waveform LUT2	Waveform LUT2	DLH_V3[1]	DLH_V3[0]	DHH_V3[1]	DHH_V3[0]	DHL_V3[1]	DHL_V3[0]	DLL_V3[1]	DLL_V3[0]	C_V3[1]	C_V3[0]	DLH_V4[1]	DLH_V4[0]	DHH_V4[1]	DHH_V4[0]	DHL_V4[1]	DHL_V4[0]	DLL_V4[1]	DLL_V4[0]	C_V4[1]	C_V4[0]	RPT2[3]	RPT2[2]	RPT2[1]	RPT2[0]
16	Waveform LUT3	Waveform LUT3	DLH_V5[1]	DLH_V5[0]	DHH_V5[1]	DHH_V5[0]	DHL_V5[1]	DHL_V5[0]	DLL_V5[1]	DLL_V5[0]	C_V5[1]	C_V5[0]	DLH_V6[1]	DLH_V6[0]	DHH_V6[1]	DHH_V6[0]	DHL_V6[1]	DHL_V6[0]	DLL_V6[1]	DLL_V6[0]	C_V6[1]	C_V6[0]	RPT3[3]	RPT3[2]	RPT3[1]	RPT3[0]
17	Waveform LUT4	Waveform LUT4	DLH_V7[1]	DLH_V7[0]	DHH_V7[1]	DHH_V7[0]	DHL_V7[1]	DHL_V7[0]	DLL_V7[1]	DLL_V7[0]	C_V7[1]	C_V7[0]	DLH_V8[1]	DLH_V8[0]	DHH_V8[1]	DHH_V8[0]	DHL_V8[1]	DHL_V8[0]	DLL_V8[1]	DLL_V8[0]	C_V8[1]	C_V8[0]	RPT4[3]	RPT4[2]	RPT4[1]	RPT4[0]
18	Waveform LUT5	Waveform LUT5	DLH_V9[1]	DLH_V9[0]	DHH_V9[1]	DHH_V9[0]	DHL_V9[1]	DHL_V9[0]	DLL_V9[1]	DLL_V9[0]	C_V9[1]	C_V9[0]	DLH_V10[1]	DLH_V10[0]	DHH_V10[1]	DHH_V10[0]	DHL_V10[1]	DHL_V10[0]	DLL_V10[1]	DLL_V10[0]	C_V10[1]	C_V10[0]	RPT5[3]	RPT5[2]	RPT5[1]	RPT5[0]
19	Waveform LUT6	Timing1	T1[5]	T1[4]	T1[3]	T1[2]	T1[1]	T1[0]	T2[5]	T2[4]	T2[3]	T2[2]	T2[1]	T2[0]	T3[5]	T3[4]	T3[3]	T3[2]	T3[1]	T3[0]	T4[5]	T4[4]	T4[3]	T4[2]	T4[1]	T4[0]
1A	Waveform LUT7	Timing2	T5[5]	T5[4]	T5[3]	T5[2]	T5[1]	T5[0]	T6[5]	T6[4]	T6[3]	T6[2]	T6[1]	T6[0]	T7[5]	T7[4]	T7[3]	T7[2]	T7[1]	T7[0]	T8[5]	T8[4]	T8[3]	T8[2]	T8[1]	T8[0]
1B	Waveform LUT8	Timing3	T9[5]	T9[4]	T9[3]	T9[2]	T9[1]	T9[0]	T10[5]	T10[4]	T10[3]	T10[2]	T10[1]	T10[0]												
1C	Reserved																									
1D	Reserved																									
1E	Reserved																									
1F	Reserved																									

9 COMMAND DESCRIPTIONS

R00h Display update

Update - When this bit is set to 1, update begin. This bit will be reset to 0 after update is started. Default is 0.

Output off - 1: All output segments and commons will set to VSS level instantly. Segment pins that in Hi-Z state (register 0Ch to 0Fh) are not affected.
0: Normal Operation (Default)

Polarity - Change the polarity setting. Default is 0

LUT setting	Polarity = 0	Polarity = 1
00	Hi-Z	Hi-Z
01	VSS	V0
10	V1	V1
11	V0	VSS

Inverse- 1: Data 1 and 0 mapping is reversed.
0: Normal application (Default)

test_update[3:0] - Waveform update for test pattern
* Segment pins set to Hi-Z state in register 0Ch to 0Fh are not affected

test_update[3:0]	Waveform update
0000	Follow ram data (Default)
0001	All common and segment output pins output a data low to high waveform
0010	All common and segment output pins output a data high to high waveform
0011	All common and segment output pins output a data high to low waveform
0100	All common and segment output pins output a data low to low waveform
0101	All common and segment output pins output VSS level
0110	All common and segment output pins output V1 level
0111	All common and segment output pins output V0 level
1000	All common and segment output pins become HiZ state
Others	Follow ram data

Phase1_Skip	1	Disable phase 1 output during update. i.e. skipping phase 1
	0	Enable phase 1 output during update.
Phase2_Skip	1	Disable phase 2 output during update. i.e. skipping phase 2
	0	Enable phase 2 output during update.
Phase3_Skip	1	Disable phase 3 output during update. i.e. skipping phase 3
	0	Enable phase 3 output during update.
Phase4_Skip	1	Disable phase 4 output during update. i.e. skipping phase 4
	0	Enable phase 4 output during update.
Phase5_Skip	1	Disable phase 5 output during update. i.e. skipping phase 5
	0	Enable phase 5 output during update.

* Any phase in Phase 1 to 5 can be skipped but must be output in sequence.
* If all phases are skipped, the IC will output phase 1 waveform only.

R03h Timing scaling

Osc_En -
1: Internal oscillator enables.
0: Internal oscillator disables. (Default)

E_CLK_Div[3:0] - Divider for external clock

E_CLK_Div[3:0]	Divider for external clock to 32kHz
000	No divide (Default)
001	Divide by 2
010	Divide by 4
011	Divide by 8
100	Divide by 16
101	Divide by 32
110	Divide by 64
111	Divide by 128

CLK_Base[3:0] - Base unit of waveform build up

CLK_Base[3:0]	ms
0000	0.0625
0001	0.125
0010	0.25
0011	0.5
0100	1
0101	2 (Default)
0110	5
0111	10
1000	20
1001	40
1010	80
1011	160
1100	320
1101	Invalid
1110	Invalid
1111	Invalid

R08h Software reset

SW_Reset[1:0] - reset

00	No action (Default)
01	No action
10	No action
11	Software reset. RAM content remains

Lock[1:0] - lock register

00	Normal operations (Default)
01	Normal operations
10	Normal operations
11	Lock stage. Once these lock bits are set, only unlock bit can be set. No other register settings are accepted.

R09h Booster voltage

DC_Volt[4:0] Set DC/DC output

DC_Volt[4:0]	Output voltage	DC_Volt[4:0]	Output voltage	DC_Volt[4:0]	Output voltage	DC_Volt[4:0]	Output voltage
00000	9	01000	17	10000	25	11000	33
00001	10	01001	18	10001	26	11001	34
00010	11	01010	19	10010	27	11010	35
00011	12	01011	20	10011	28	11011	36
00100	13	01100	21	10100	29	11100	37
00101	14	01101	22	10101	30 (Default)	11101	38
00110	15	01110	23	10110	31	11110	Reserved
00111	16	01111	24	10111	32	11111	Reserved

DOFF_out[1:0] - All output segments and commons will be ended at certain level

LUT setting	Output end level
00	Hi-Z
01	VSS (Default)
10	V1
11	V0

VTH[2:0]: Set Threshold for battery voltage

VTH[2:0]	V
000	2.1 (Default)
001	2.3
010	2.5
011	2.7
100	2.9
101	3.1
110	3.3
111	3.5

R0Ah Analog control

VCI_En
1: Enable VCI regulator. When VCI_En enabled, VCI will regulate from VBAT, power input should supply to VBAT pin and no connection to VCI.
0: Disable VCI regulator. When VCI_En disabled, VCI become the power pin, VBAT power can be disconnected. (Default)

DC/DC_En
1: Enable DC/DC.
0: Disable DC/DC. (Default)

DCDis_En
1: Fast discharge option of DC/DC.
0: Disable discharge option of DC/DC. (Default)

Bias_En
1: Bias circuit enables. Bias circuit should be enabled when DCDC enable.
0: Disable Bias circuit. (Default)

HVBuff_En
1: High voltage buffer output enables. It is for stabilize the segment and common driving voltage
0: Disable High voltage buffer output. (Default)

TSEN_out
1: For testing only
0: For normal operation (Default)

TADC_En [1:0]
11: Temperature sensor enables, allow digital output of temperature sensing block.
other: Temperature sensor disables. (Default)

DCDis[1:0]
DC/DC Discharge timing setting
00: 4ms (Default)
01: 2ms
10: 8ms
11: 16ms

VSEN_En
1: VBAT voltage sensor enables.
0: VBAT voltage sensor disables. (Default)

DCDC Multiplier ratio	Stage2_En	Stage3_En	Stage4_En	Stage2_bypass	Stage3_bypass	Stage4_bypass	Stage2_level	Remark
4X	0	1	1	0	1	1	0	Refer to application circuit Figure 16-5
6X	0	1	1	0	1	1	1	Refer to application circuit Figure 16-4
8X	0	0	1	0	0	1	0	Refer to application circuit Figure 16-3
12X	0	0	1	0	0	1	1	Refer to application circuit Figure 16-2
16X	0	0	0	0	0	0	0	Refer to application circuit Figure 16-1

Stage2_En
1: Charge pump stage 2 disables. (Default)
0: Charge pump stage 2 enables.

Stage3_En
1: Charge pump stage 3 disables. (Default)
0: Charge pump stage 3 enables.

Stage4_En
1: Charge pump stage 4 disables. (Default)
0: Charge pump stage 4 enables.

Stage2_bypass
1: Bypass the stage 2 of charge pump circuit.
0: Normal operation. (Default)

Stage3_bypass
1: Bypass the stage 3 of charge pump circuit.
0: Normal operation. (Default)

Stage4_bypass
1: Bypass the stage 4 of charge pump circuit.
0: Normal operation. (Default)

Stage2_level
1: Multiple level of the stage 2 of charge pump circuit is x3.
0: Multiple level of the stage 2 of charge pump circuit is x2. (Default)

Reg_En
It is for DC/DC output regulator, it prevent the DC/DC output voltage over 40V
1: Disable voltage regulation on VCP1. (Default)
0: Enable voltage regulation on VCP1.

Remark:
1) Default booster mode setting is 16X.
2) DCDC multiplier ratio setting required a matching of hardware connections and software setting. Please refer to Section 16 for the corresponding application circuit.

R0Bh Status read

This is the status read register

TSEN[6:0]
Digital Temperature sensor reading

Temperature	ADC value [6:0] (typical value)
-40	0x18
-30	0x24
-20	0x2C
-10	0x32
0	0x3A
10	0x43
20	0x49
25	0x4E
30	0x51
40	0x59
50	0x60
60	0x69
70	0x6F
80	0x77
85	0x7B

BUSY:
1: Indicates the chip is running waveform update. Please don't send data and update the chip when the chip is running.

0: Indicates no waveform update is on-going. Update is allowed when the chip is idle.

VSEN[2:0]
Voltage sensor reading

VSEN[2:0]	V
000	2.1
001	2.3
010	2.5
011	2.7
100	2.9
101	3.1
110	3.3
111	3.5

R0Ch to R0Fh Hi-Z register

Allow individual pin Hi-Z setting.
1: Hi-Z
0: output follow ram data (Default)

R10h to R13F Data register (Current data)

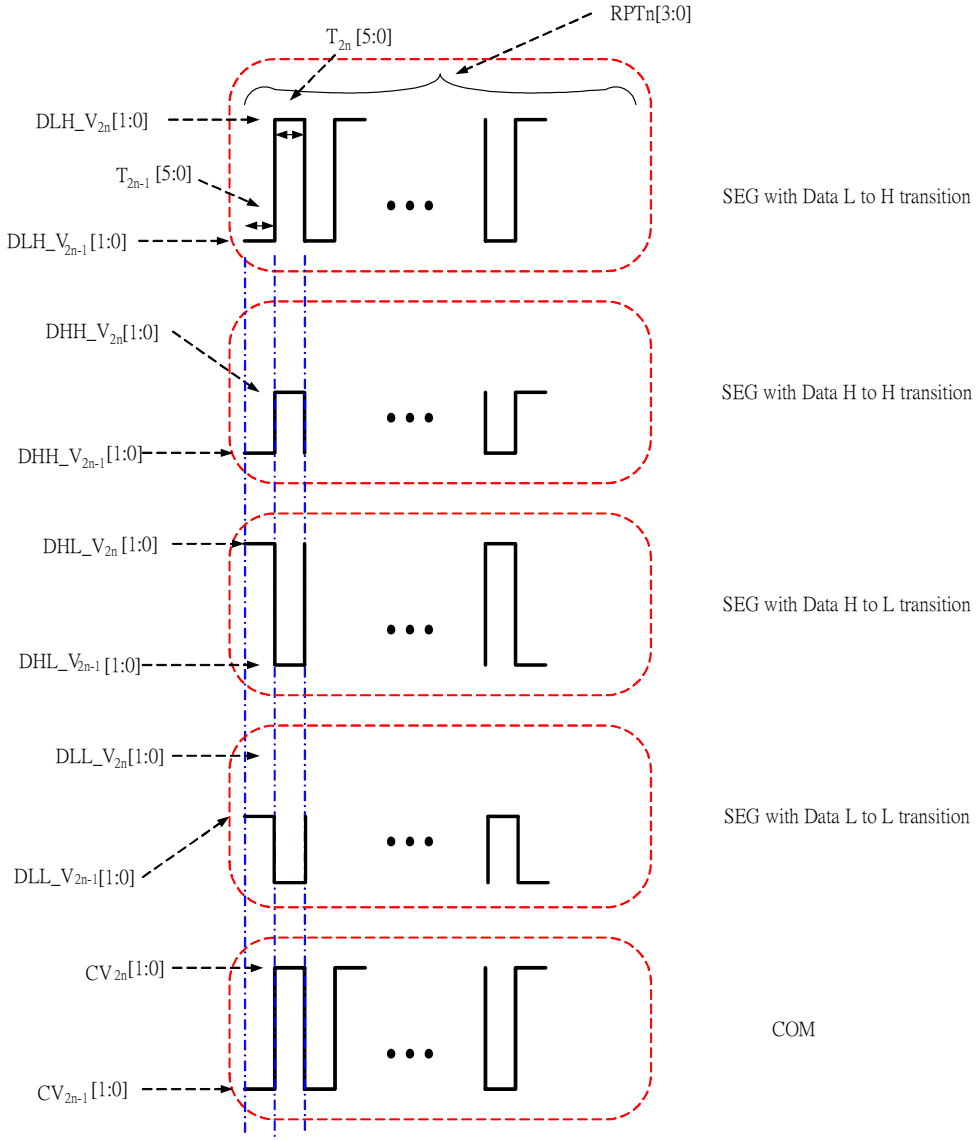
Data register of Current data
*Data register of previous data is not accessible

R14h to R1Bh Waveform LUT

DLH_V_y [1:0] / DHH_V_y [1:0] / DHL_V_y [1:0] / DLL_V_y [1:0] / C_V_y[1:0]	Output status
00	Hi-Z
01	VSS
10	V1
11	V0

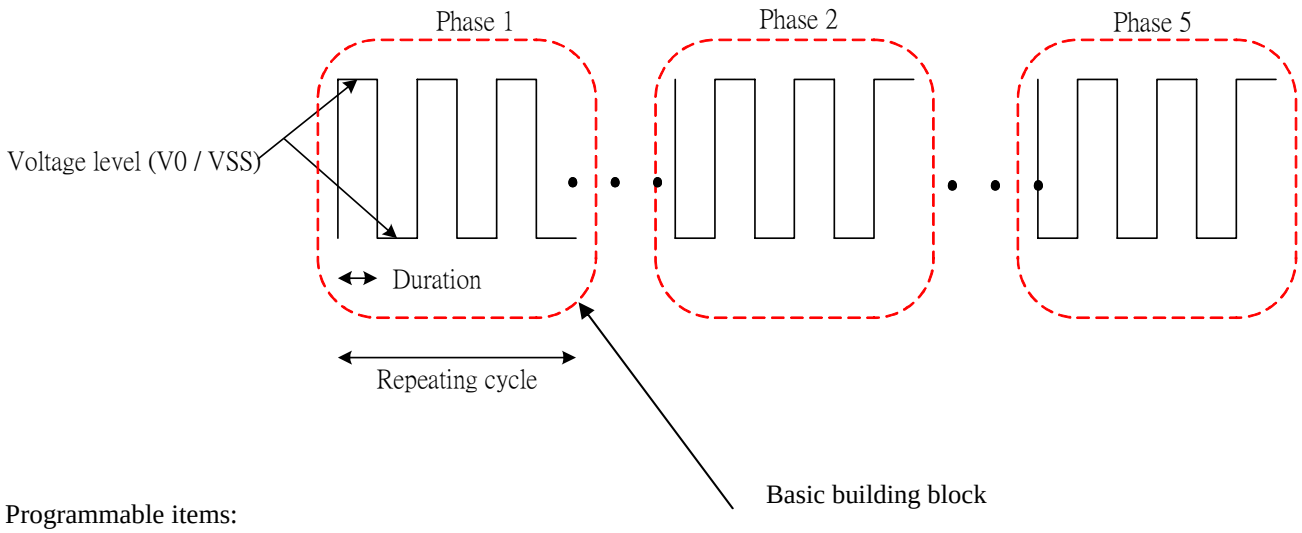
Tn[5:0] Output waveform duration
000000 - Skip
000001 – 111111 Waveform duration = Base unit times x Tn[5:0]

Figure 9-1: Illustration of output waveform under different phase behavior setting



10 OUTPUT WAVEFORM

The number of output waveform phase is programmable. And the maximum number of phase can be selected is 5. After waveform complete, both COM and SEG go to VSS.



Programmable items:

- Voltage level of each phase
- Repeating cycle of each phase
- Duration of each phase
- A maximum of 5 different phases can be set.
- Five separate settings for
  - COM
  - SEG, L to H transition
  - SEG, H to H transition
  - SEG, H to L transition
  - SEG, L to L transition

- Individual phase can be disabled during update. E.g.
  - Ph1 > Ph2 > Ph3 > Ph4, disable Ph5
  - Ph1 > Ph2 > Ph 4, disable Ph3 and Ph5
  - Ph3 > Ph5, disable Ph1, Ph2 and Ph4

11 ABSOLUTE MAXIMUM RATINGS

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Logic supply voltage	-0.5 to +4.0	V
V_{DDIO}	I/O supply voltage	-0.5 to +4.0	V
V_{CI}	DC/DC circuit supply voltage	-0.5 to +4.0	V
V_{BAT}	Battery supply power	-0.5 to +4.8	V
V_0	Panel driving voltage	-0.5 to +42	V
V_{IN}	Logic Input voltage	-0.5 to +4.0	V
V_{OUT}	Logic Output voltage	-0.5 to +4.0	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to 150	°C

12 OPERATING RATINGS

Table 12-1: DC Operating Rating

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.0		3.6	V
V_{DDIO}	I/O supply voltage		2.0		V_{DD}	V
V_{BAT}	VCI regulator supply voltage		2.8		4.5	V
V_{CI}	Charge pump power supply		2.4		3.6	V
V_0	Driver supply voltage		10		40	V
V_1	Driver supply voltage			$V_0/2$		V

13 DC Electrical Characteristics

The following specifications apply for: Vss=0V, V_{DD}=+2.8V, V_{DDIO} = +2.8V, V_{CI}= +2.8V, V_{BAT}= +3.5V, temperature = 25 °C

Table 13-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{DD}	V_{DD} operation voltage		V_{DD}	2.0		3.6	V
V_{DDIO}	V_{DDIO} voltage		V_{DDIO}	2.0		V_{DD}	V
V_0	V_0 operation voltage		V_0	10		40	V
V_{BAT}	V_{BAT} operating voltage		V_{BAT}	2.8		4.5	V
V_{CI}	DC/DC input voltage		V_{CI}	2.4		3.6	V
V_{CI}	VCI regulator output voltage	VDDIO = VDD =2.8V VBAT=3.5V	V_{CI}		3		V
VIH	High level input voltage			$0.8V_{DDIO}$			V
VIL	Low level input voltage					$0.2\ V_{DDIO}$	V
VOH	High level output voltage			$0.9V_{DD}$			V
VOL	Low level output voltage					$0.1V_{DD}$	V
Ron_SEG	Segment ON resistance	V_0=36V, dV=0.5V	SEG[95:1]		10k		Ohm
Ron_SEG0	Background segment ON resistance	V_0=36V, dV=0.5V	SEG0		1k		Ohm
Ron_COM	Common ON resistance	V_0=36V, dV=0.5V	COM		1k		Ohm
VCP0	DC/DC output voltage	VCI=3.0V, Output set to 36V 16X setting No loading	V0	35.2	36	36.8	V
VCP0	DC/DC output voltage	VCI=2.5V, Output set to 36V No loading	V0	36 x 0.95	36	36 x 1.05	V
VCP0	DC/DC output voltage	VCI=2.6V, Output set to 38V No loading	V0	38 x 0.95	38	38 x 1.05	V
V1	V1 output voltage	V0=30V, Loading at V1 = 5nF, 1MΩ	V1	V0/2 x 0.98	V0/2	V0/2 x 1.02	V
DIslp_vdd	Deep Sleep mode current	VDDIO = VDD =2.8V DC/DC off No clock No output load	VDD		0.5	2	uA

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
DIslp_vddio	Deep Sleep mode current	VDDIO = VDD =2.8V DC/DC off No clock No output load	VDDIO		0.5	2	uA
DIslp_vci	Deep Sleep mode current	VDDIO = VDD =2.8V VCI=2.8V DC/DC off No clock No output load	VCI		1	3	uA
DIslp_all	Deep Sleep mode current	VDDIO = VDD =2.8V VCI=2.8V DC/DC off No clock No output load	VDD + VDDIO + VCI		2	7	uA
DIslp_vbat	Deep Sleep mode current	VDDIO = VDD =2.8V VBAT=3.5V VCI regulator off DC/DC off No clock No output load	VBAT		0.5	2	uA
DIslp_v0	Deep Sleep mode current	VDDIO = VDD =2.8V VCI=2.8V DC/DC off No clock No output load	V0		0.5	2	uA
Iop_vdd	Operating current	VDDIO = VDD =2.8V VCI=2.8V DC/DC on V0=36V Osc on with 32kHz No output load	VDD		80	100	uA
Iop_vci	Operating current	VDDIO = VDD =2.8V VCI=2.8V DC/DC on V0=36V Osc on with 32kHz VCOM / VSEG all tie to V1	VCI		250	350	uA

Table 13-2: Temperature sensor characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
	Temperature senor operating range			-40		85	°C
RES_{TS}	Resolution of temperature sensor	-0 to 50 °C			1.3		°C
Acc_{TS}	Accuracy of temperature sensor reading	-0 to 50 °C			TBD		°C

14 AC CHARACTERISTICS

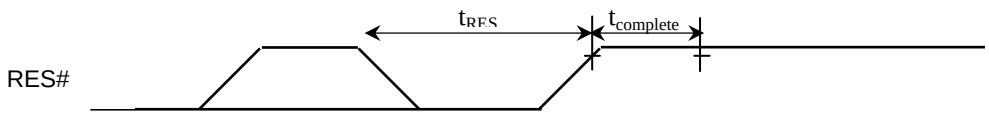
14.1 Reset timing

Table 14-1: Reset Timing Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.8V, V_{DDIO}=2.8V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{RES}	Reset pulse width	20			us
$t_{Complete}$	Reset completion time	20			us

Figure 14-1: Reset timing diagram



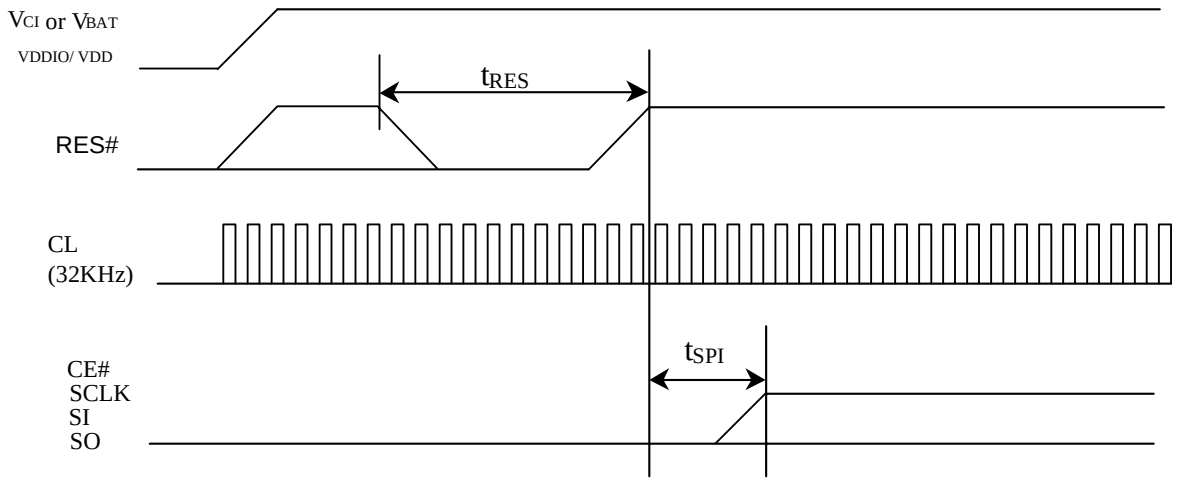
14.2 Power Up Sequence

Table 14-2: Power up timing characteristics

Symbol	Characteristic	Min.	Typ.	Max	Units
t_{RES}	Reset Pulse Width	20			us
t_{SPI}	SPI Stable Time	31.25			us

Note: In all cases, VDDIO and VCI (or VBAT) power up sequence should not have any impact on the driver/ display functionalities/ performance.

Figure 14-2: Power up timing diagram



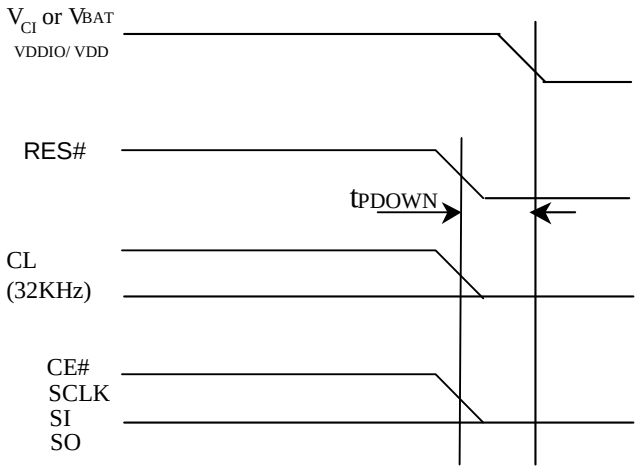
14.3 Power down Sequence

Table 14-3: Power down timing characteristics

Symbol	Characteristic	Min.	Typ.	Max	Units
t_{PDOWN}	Power Hold Time	100			ns

Note: The IC performs DC/DC discharge on all high voltages during abnormal power supply removal to avoid any functional corruption upon next power up.

Figure 14-3: Power down timing diagram



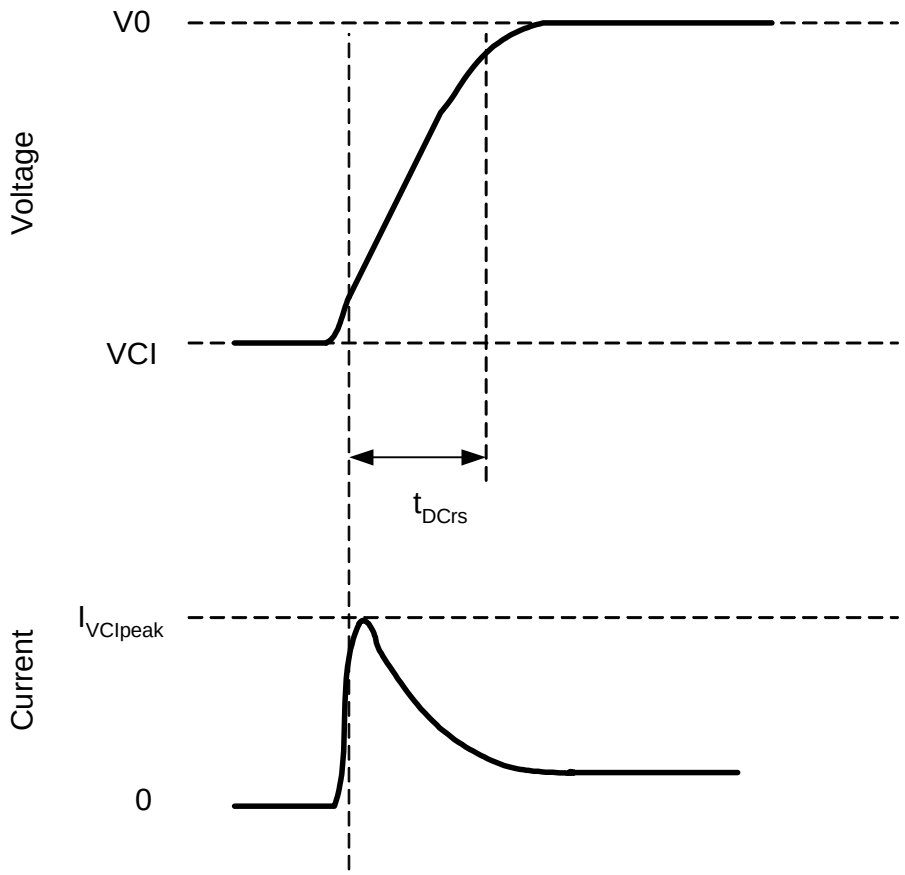
14.4 DC/DC start up

Table 14-4: DC/DC start up characteristics

Conditions: Panel Loading = 5nF

Symbol	Characteristic	Min.	Typ.	Max	Units
$I_{VCIpeak}$	DC/DC Start up transient current peak			TBD	mA
t_{DCrs}	Start up settling time 90% of 36V DC/DC		80	200	ms

Figure 14-4: Typical DC/DC start up profile



15 MCU interface Timing

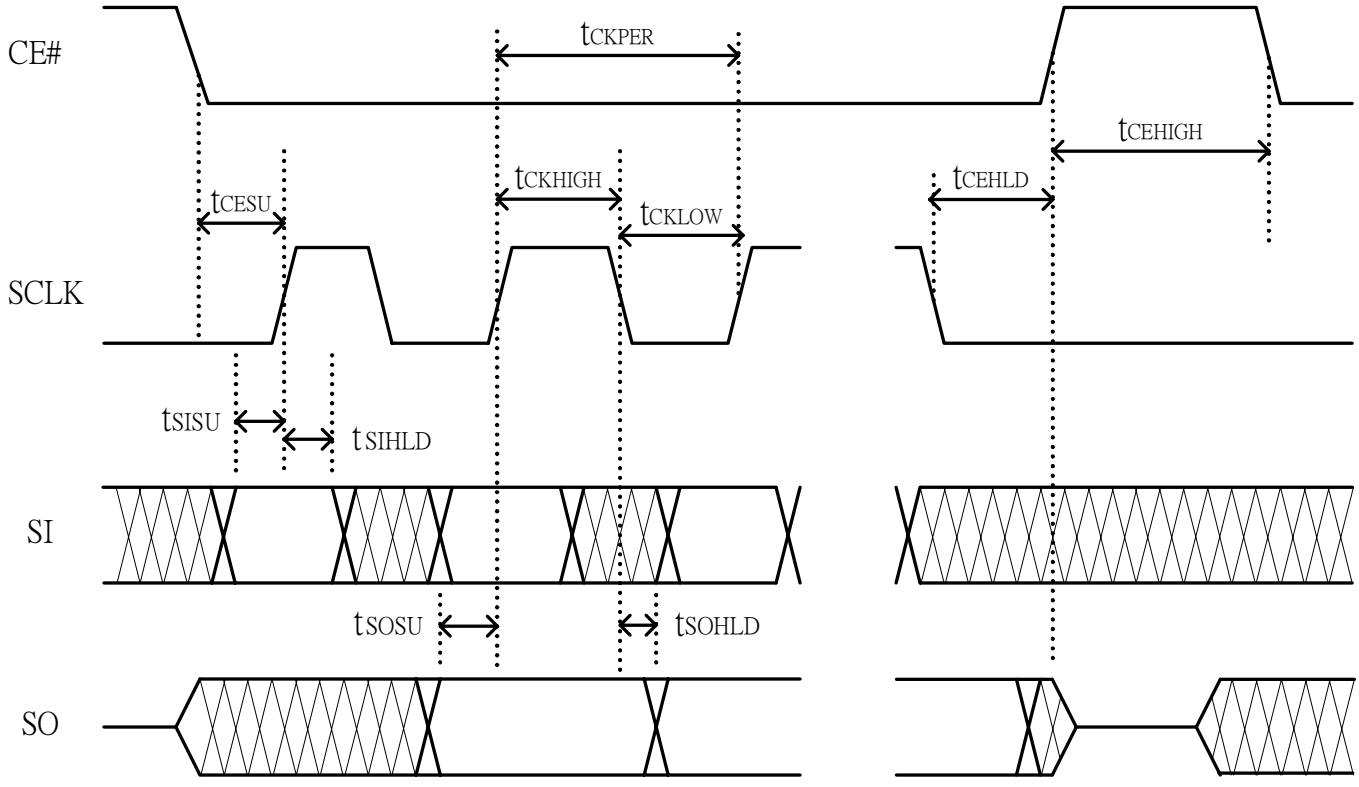
Table 15-1: SPI Timing Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.8V, V_{DDIO}=2.8V, T_A = -30 to 85 ^oC)

Symbol	Parameter	Time min (ns)
t_{CESU}	Time CE has to be low before the first rising edge of SCLK	20
t_{CEHLD}	Time CE has to remain low after the last falling edge of SCLK	20
t_{CEHIGH}	Time CE has to remain high between two transfers	20
t_{CKPER}	Clock period of SCLK (1)	38.46
t_{CKHIGH}	Part of the clock period where SCLK has to remain high	15
t_{CLKLOW}	Part of the clock period where SCLK has to remain low	15
t_{SISU}	Time SI has to be stable before the next rising edge of SCLK	5
t_{SIGHLD}	Time SI has to remain stable after the rising edge of SCLK	5
t_{SOSU}	Time SO will be stable before the next rising edge of SCLK	5
t_{SOHLD}	Time SO will remain stable after the falling edge of SCLK	5

(1) Equivalent to a maximum clock frequency of 26MHz.

Figure 15-1: SPI Timing Diagram



16 APPLICATION CIRCUIT

Figure 16-1: Typical application diagram for 16x DCDC

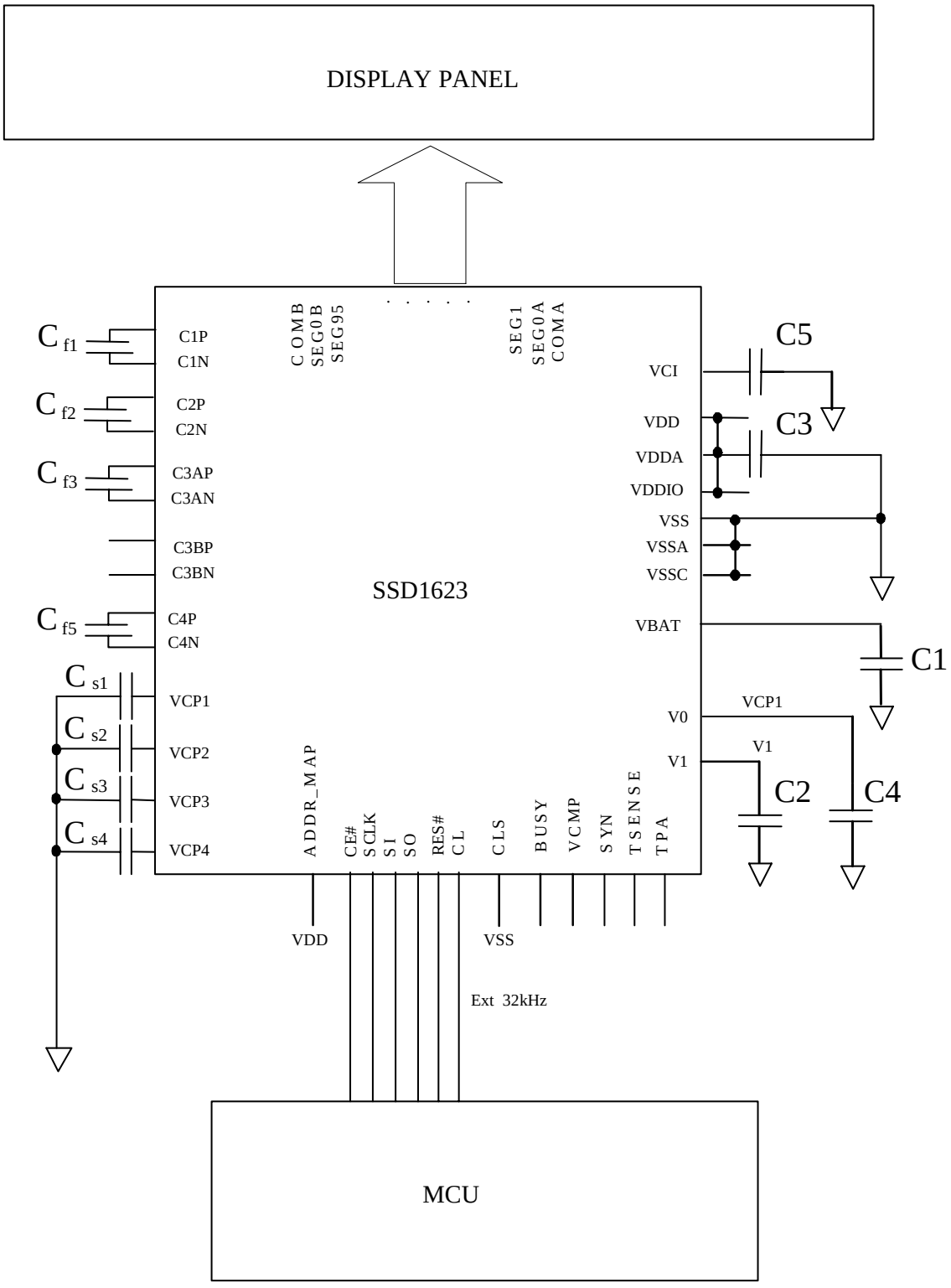


Figure 16-2: Typical application diagram for 12x DCDC

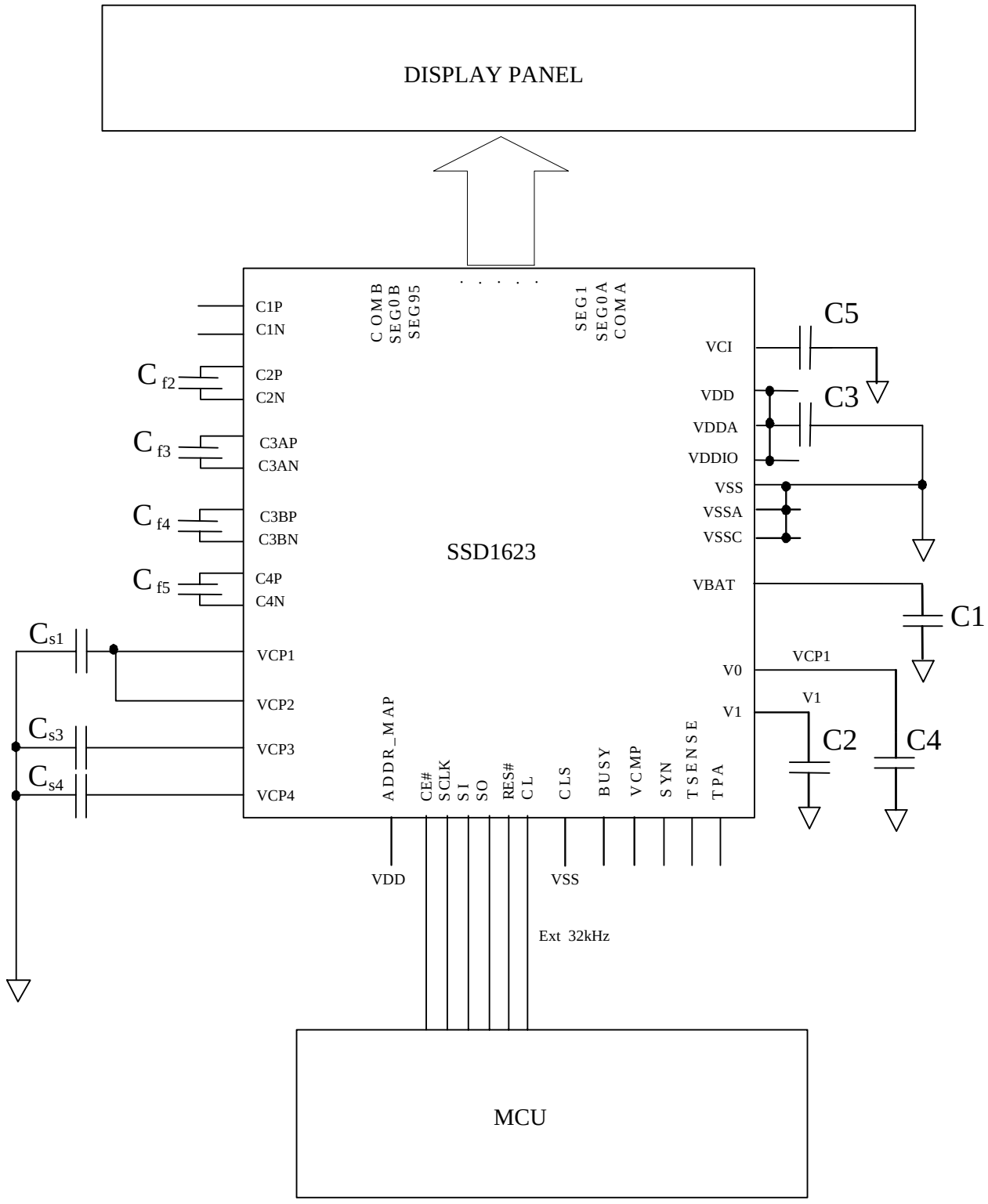


Figure 16-3: Typical application diagram for 8x DCDC

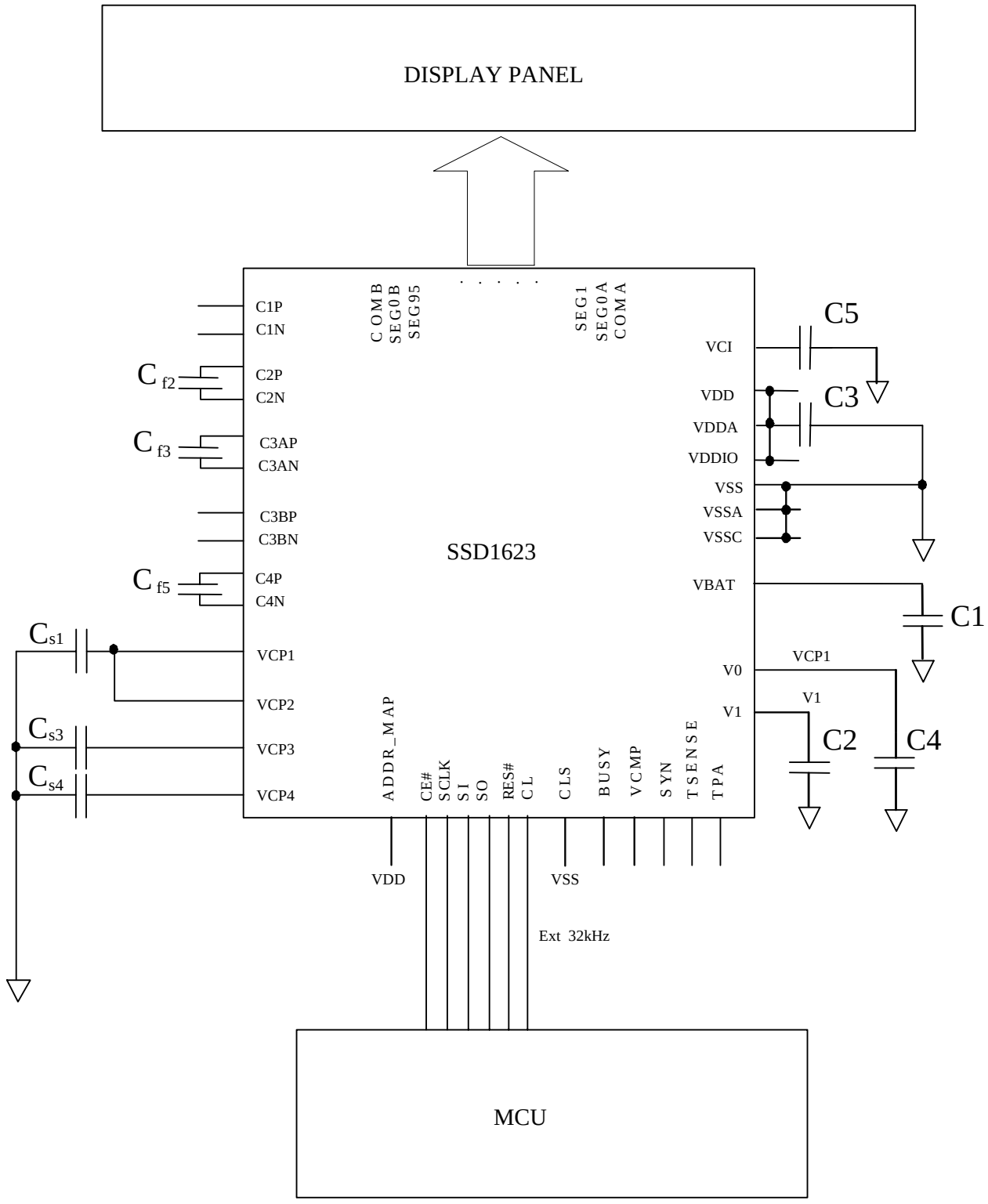


Figure 16-4: Typical application diagram for 6x DCDC

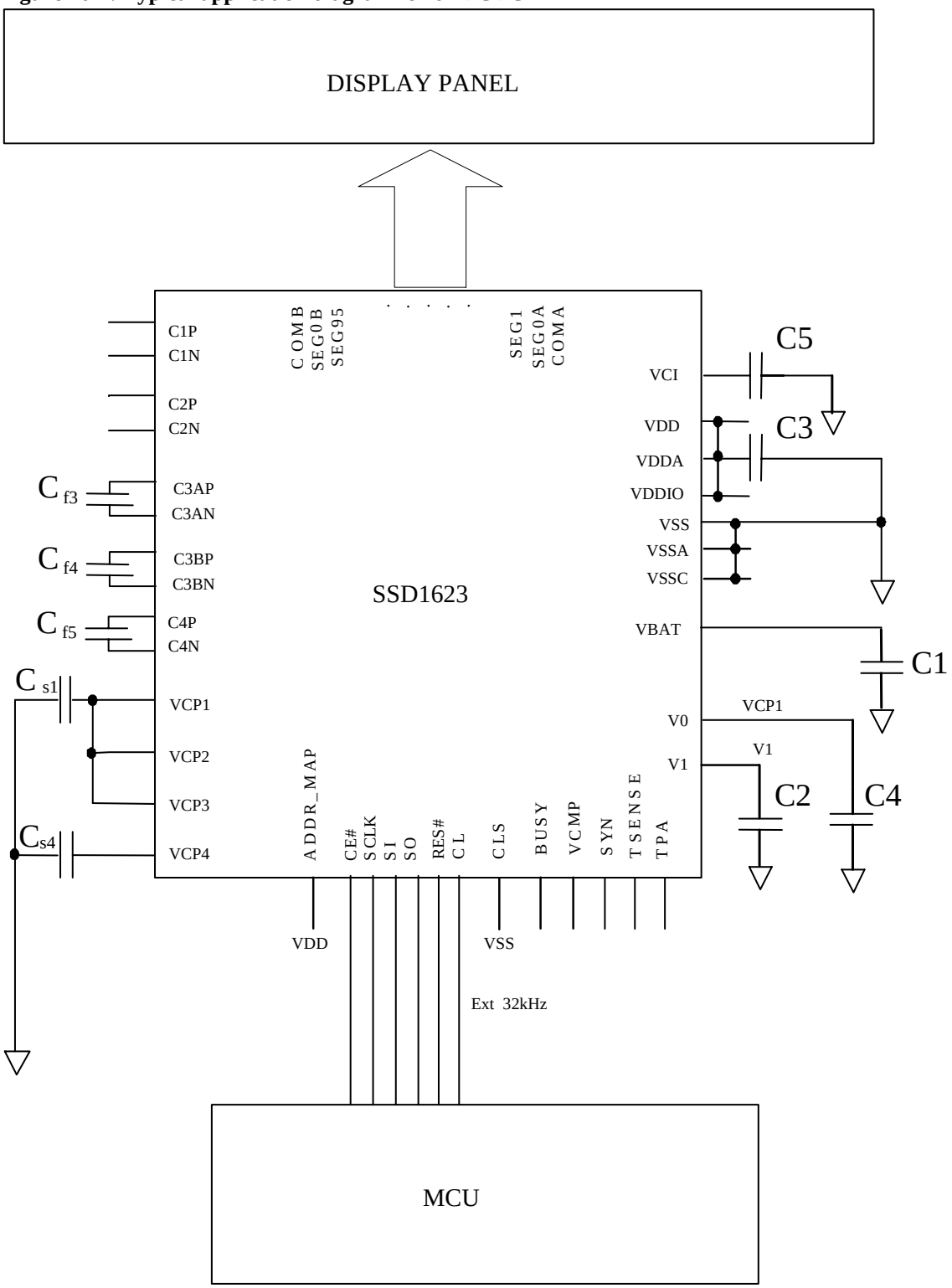


Figure 16-5: Typical application diagram for 4x DCDC

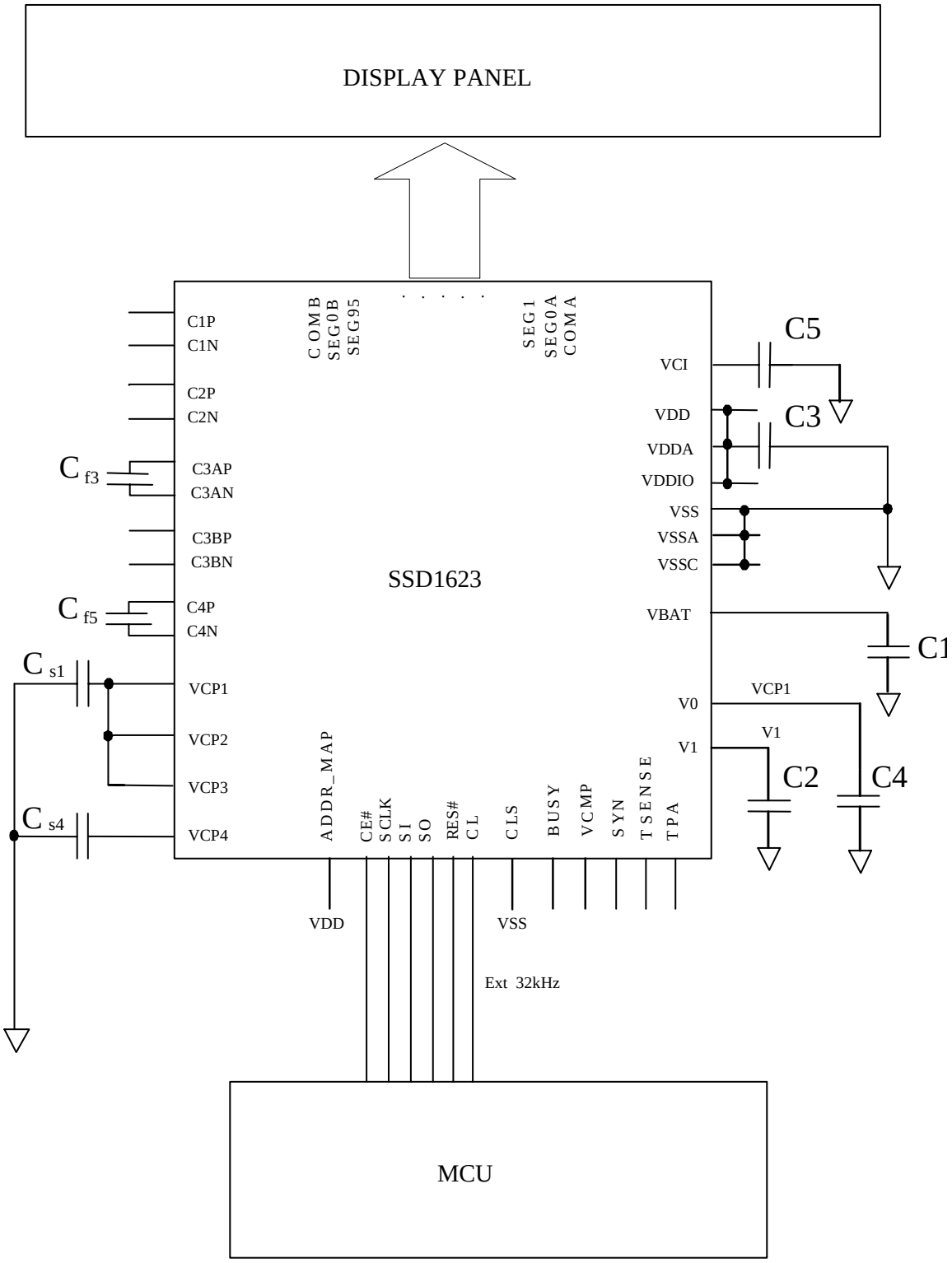


Table 16-1: Reference Capacitor Value

Part reference	Value (uF)	Min Rating
Cf1	0.22	50V
Cf2	0.22	25V
Cf3	0.22	25V
Cf4	0.22	10V
Cf5	0.22	10V
Cs1	0.22	50V
Cs2	0.22	25V
Cs3	0.22	10V
Cs4	0.22	10V
C1	1.0	10V
C2	1.0	50V
C3	1.0	10V
C4	1.0	25V
C5	0.22	10V

- Capacitor values requirement depends on panel loading and voltage setting.

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol  . Hazardous Substances test report is available upon requested.

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