

SED1530 Series

DOT MATRIX LCD DRIVER-CONTROLLER

DESCRIPTION

The SED1530 Series are intelligent CMOS LCD controller-drivers with the ability to drive alphanumeric and graphic displays. The LSI communicates with a high-speed microprocessor, such as the Intel 80xx and 68xx family, through either a serial or 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (65 × 132 bits) and generates an LCD drive signal.

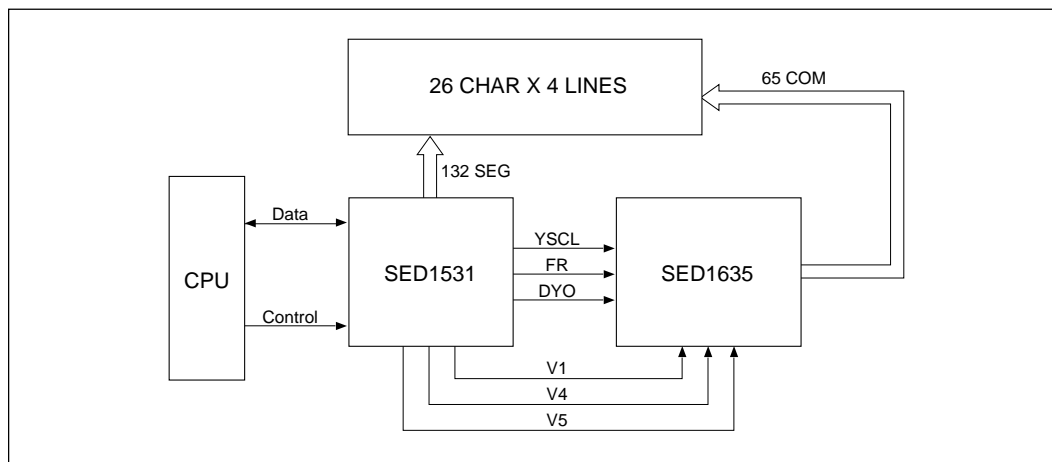
FEATURES

- Low-power CMOS technology
- Direct interface to both 80xx and 68xx MPU
- Support 8-bit parallel and serial interface
- On-chip display data RAM 132 × 65 bits
- On-chip DC/DC converter for LCD voltage
- On-chip CR oscillator circuit
- Supports master/slave mode
- Voltage regulator, low-power voltage follower
- $-0.17\%/^{\circ}\text{C}$ temperature gradient
- 32-level contrast adjustment by software
- 2.4V to 6.0V supply voltage
- -4.5V to -16V LCD voltage
- Operating temperature -40 to 85°C
- Low power consumption $80\mu\text{A}$
- Package
 - TAB T**
 - Al pad Die D*A
 - Au bump Die D*B

AVAILABLE MODELS

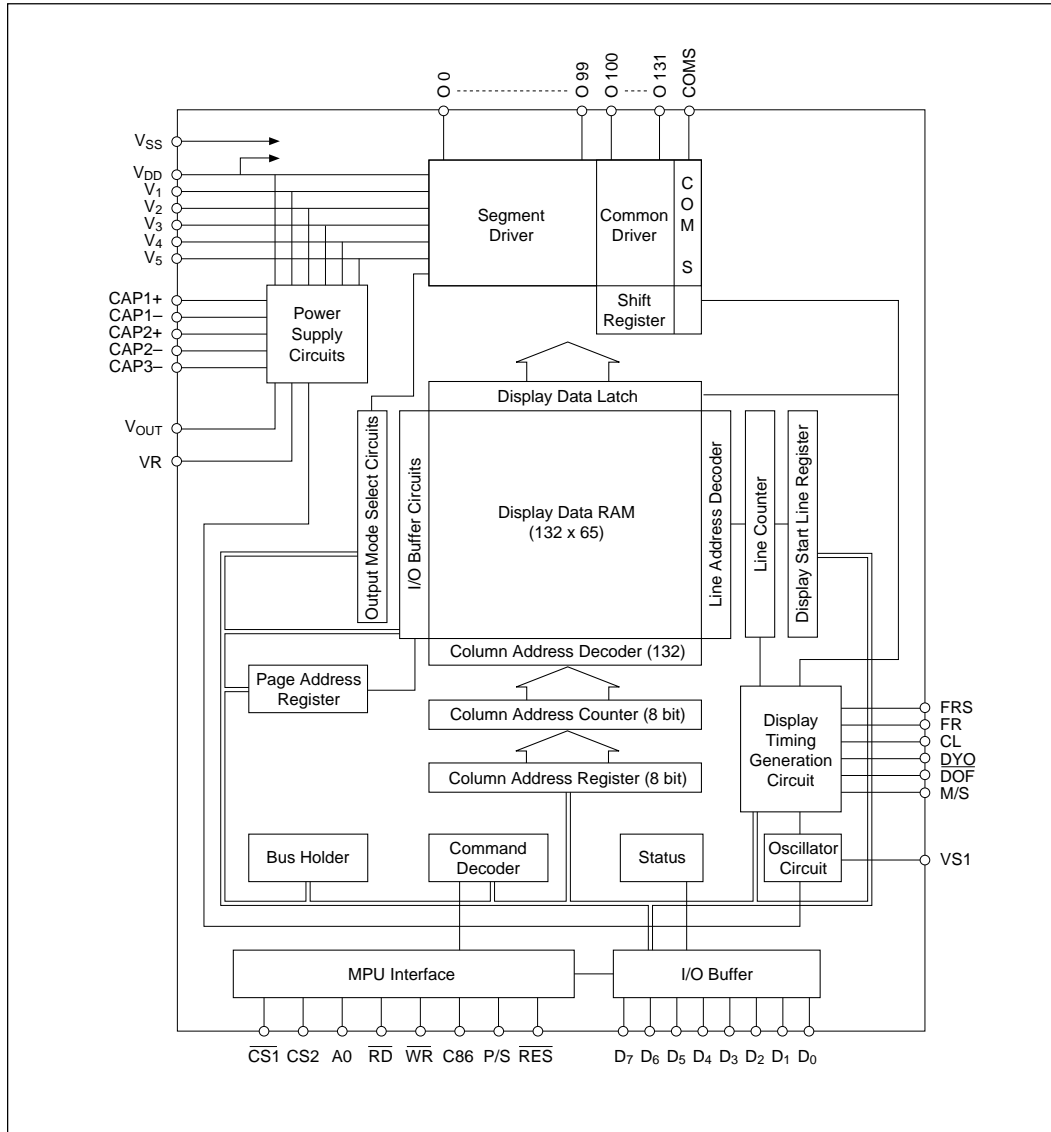
Name	Duty	LCD Bias	SEG Driver	COM Driver	Display Area	Remarks
SED1530D0*	1/33	1/5, 1/6	100	33	33 × 100	COM single-side assignment
SED1530DA*	1/33	1/5, 1/6	100	33	33 × 100	COM dual-side assignment
SED1531D0*	1/65	1/6, 1/8	132	0	65 × 132	SED1635 is used for COM
SED1532D0*	1/65	1/6, 1/8	100	33	65 × 200	COM single-side right assignment
SED1532DB*	1/65	1/6, 1/8	100	33	65 × 200	COM single-side left assignment

SYSTEM BLOCK DIAGRAM

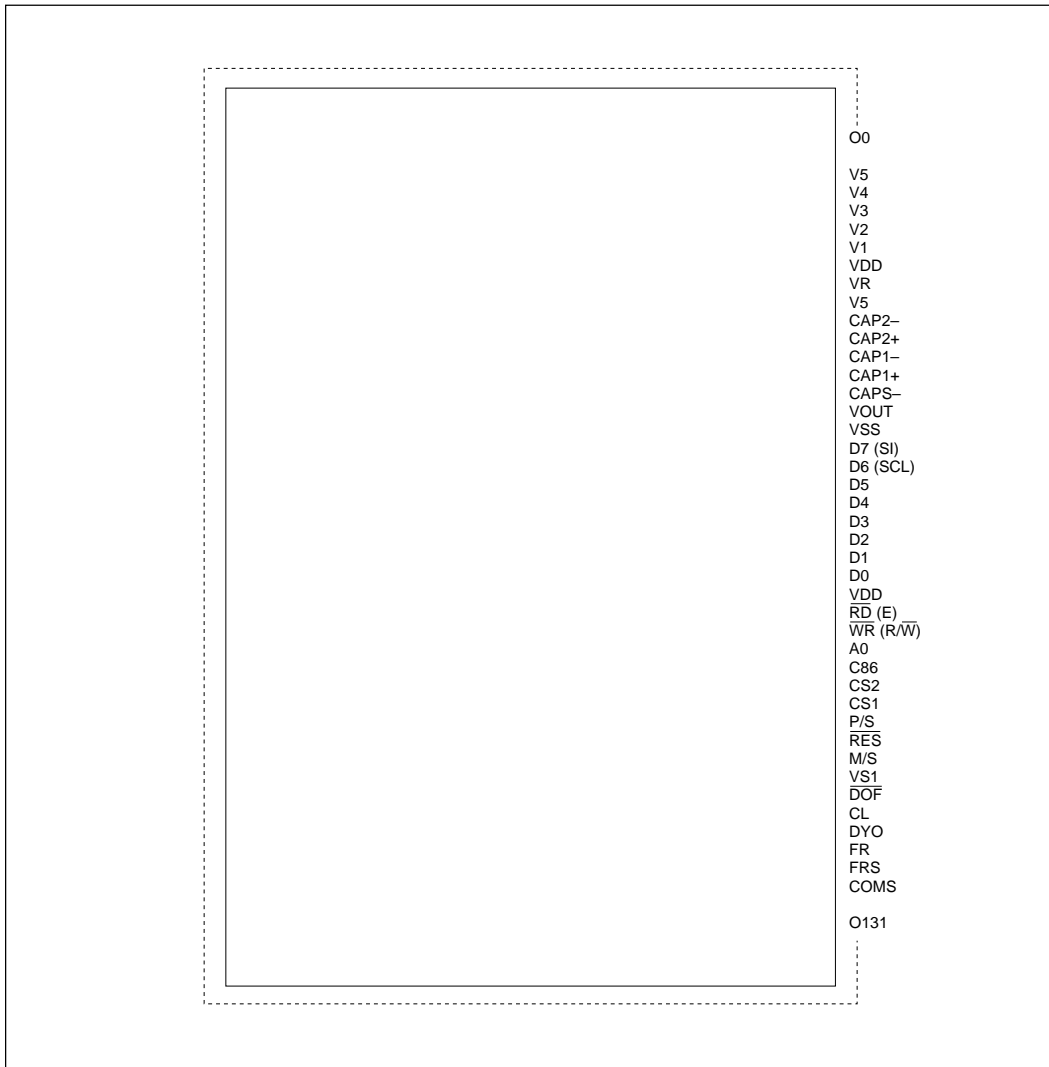


SED1530 Series

■ BLOCK DIAGRAM



■ PINOUT



■ PINOUT TABLE

Model	Output	O ₀ to O ₁₅	O ₁₅ to O ₃₁	O ₃₂ ----- O ₉₉	O ₁₀₀ to O ₁₁₅	O ₁₁₆ to O ₁₃₁
SED1530*0*	0 1	SEG0 ----- SEG99			COM0 ----- 31	COM31 ----- 0
SED1530*A*	0 1	COM15 -- 0 COM16 31	SEG0 ----- SEG99			COM16 31 COM15 -- 0
SED1531*0*		SEG0 ----- SEG131				
SED1532*0*	0 1	SEG99 ----- SEG0			COM31 -- 0	COM0 -- 31
SED1532*B*	0 1	COM0 -- 31 COM31 -- 0	SEG0 ----- SEG99			

Note: * "0" and "1" indicate the mode of the D3 output mode select register.

SED1530 Series

■ PIN DESCRIPTION

● Power Signals

Pin	I/O	Function	Number of Pins															
V _{DD}	Power	Connected to +5V power. Connected with MPU power supply V _{CC} pin.	2															
V _{SS}	Power	0V, connected to system GND.	1															
V1 ~ V5	Power	<p>Multi-level power for LC driver. Transforms impedance using resistive voltage divider or op amps in order to apply the voltage determined for each LC cell. The voltage levels are based on V_{DD}, and must conform to the relationship below:</p> $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ <p>When the master operation power supply is ON, the internal power supply circuitry supplies the V1 ~ V4 voltages shown below. The voltage levels are selected using the LCD bias set command.</p> <table border="1"> <thead> <tr> <th></th> <th>SED1530D0*</th> <th>SED1530DA*, SED1531D0*, SED1532D**</th> </tr> </thead> <tbody> <tr> <td>V1</td> <td>1/5 × V5 1/6 × V5</td> <td>1/5 × V5 1/6 × V5</td> </tr> <tr> <td>V2</td> <td>2/5 × V5 2/6 × V5</td> <td>2/5 × V5 2/6 × V5</td> </tr> <tr> <td>V3</td> <td>3/5 × V5 4/6 × V5</td> <td>3/5 × V5 4/6 × V5</td> </tr> <tr> <td>V4</td> <td>4/5 × V5 5/6 × V5</td> <td>4/5 × V5 5/6 × V5</td> </tr> </tbody> </table>		SED1530D0*	SED1530DA*, SED1531D0*, SED1532D**	V1	1/5 × V5 1/6 × V5	1/5 × V5 1/6 × V5	V2	2/5 × V5 2/6 × V5	2/5 × V5 2/6 × V5	V3	3/5 × V5 4/6 × V5	3/5 × V5 4/6 × V5	V4	4/5 × V5 5/6 × V5	4/5 × V5 5/6 × V5	6
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V3	3/5 × V5 4/6 × V5	3/5 × V5 4/6 × V5																
V4	4/5 × V5 5/6 × V5	4/5 × V5 5/6 × V5																

● LCD Power Circuit Pins

Pin	I/O	Function	Number of Pins
CAP1+	O	Voltage step-up capacitor, positive side connection pin. Connect the capacitor between this pin and CAP1-.	1
CAP1-	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP1+.	1
CAP2+	O	Voltage step-up capacitor, positive side connection pin. Connect the capacitor between this pin and CAP2-.	1
CAP2-	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP2+.	1
CAP3-	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP1+.	1
V _{OUT}	O	Voltage step-up output pin. Connect the capacitor between this terminal and V _{SS} .	1
V _R	I	Voltage regulator pin. Use a resistive voltage divider to provide voltage between V _{DD} and V5.	1

● System Bus Interface Signals

Pin	I/O	Function	Number of Pins																		
D7 ~ D0 (SI) (SCL)	I/O	8-bit bi-directional data bus, normally connected to a standard 8-bit or 16-bit MPU data bus. When serial interface is selected: D7: Serial Data Input Pin (SI) D6: Serial Clock Input Pin (SCL)	8																		
A0	I	Normally the LSB of the MPU address bus is connected to this pin to provide data/command selection: 0: D0 ~ D7 indicate display control data 1: D0 ~ D7 indicate display data	1																		
RES	I	Reset to initial settings by setting RES to "L". The reset operation is performed according to the RES signal level.	1																		
CS1 CS2	I	Chip Select input pins. Data I/O is enabled by the combination below: <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>Pin Name</th> <th>CS1</th> <th>CS2</th> </tr> </thead> <tbody> <tr> <td>State</td> <td>"L"</td> <td>"H"</td> </tr> </tbody> </table>	Pin Name	CS1	CS2	State	"L"	"H"	2												
Pin Name	CS1	CS2																			
State	"L"	"H"																			
RD (E)	I	* When connected to an 80-series MPU: Active "L" This pin is connected to the RD signal from the MPU. When this signal is "L" the SED1530 Series data bus is in output mode. * When connected to a 68-series MPU: Active "H" This is the 68-series MPU enable clock input pin.	1																		
WR (R/W)	I	* When connected to an 80-series MPU: Active "L" This pin is connected to the WR signal from the MPU. The data bus signals are retrieved at the rising edge of the WR signal. * When connected to a 68-series MPU: This is the read/write control signal input pin. R/W = "H": Read R/W = "L": Write	1																		
C86	I	MPU interface select pin: C86 = "H": the 68-series MPU interface C86 = "L": the 80-series MPU interface	1																		
P/S	I	Serial data input/parallel data input selection pin: <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>P/S</th> <th>Chip Select</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>CS1/CS2</td> <td>A0</td> <td>D0 ~ D7</td> <td>RD/WR</td> <td>—</td> </tr> <tr> <td>"L"</td> <td>CS1/CS2</td> <td>A0</td> <td>SI (D7)</td> <td>Write only</td> <td>SCL (D6)</td> </tr> </tbody> </table> Note: RAM data read cannot be performed by serial data input. When P/S = L, fix D0 ~ D5 to HZ RD, and fix WR to either "H" or "L".	P/S	Chip Select	Data/Command	Data	Read/Write	Serial Clock	"H"	CS1/CS2	A0	D0 ~ D7	RD/WR	—	"L"	CS1/CS2	A0	SI (D7)	Write only	SCL (D6)	1
P/S	Chip Select	Data/Command	Data	Read/Write	Serial Clock																
"H"	CS1/CS2	A0	D0 ~ D7	RD/WR	—																
"L"	CS1/CS2	A0	SI (D7)	Write only	SCL (D6)																



SED1530 Series

● LCD Drive Circuit Signals

Pin	I/O	Function	Number of Pins
M/S	I	This pin selects the master/slave operation of the SED1530 series chips. The master operation outputs the signals necessary for the LCD display. The slave operations input the signals necessary to synchronize the LCD display.	1
CL	I/O	This is the display clock I/O terminal. When using the SED1530 Series chips in master/slave, the CL pins of the chips must be connected. When using in combination with a dedicated common driver, the common driver YSCL pin must be connected to this pin. M/S = "H": Output M/S = "L": Input	1
FR	I/O	This is the LCD alternating current signal I/O pin. When using the SED1530 Series chips in master/slave, the FR pins of the chips must be connected. When using an SED1530 Series chip in master mode, this pin must be connected to the FR pin of the dedicated common driver. M/S = "H": Output M/S = "L": Input	1
DYO	O	This is the common activation output pin. This pin is used only when the SED1530 Series chip is in master mode. This pin must be connected to the common driver DIO pin. This pin is HZ in slave mode.	1
VS1	O	This pin is used to monitor the voltage of the internal power supply.	1
$\overline{\text{DOF}}$	I/O	This is the LCD display blanking control pin. When using the SED1530 Series chips in master/slave, the $\overline{\text{DOF}}$ pins of the chips must be connected. When using in combination with a dedicated common driver (SED1635), the common driver $\overline{\text{DOFF}}$ pin must be connected to this pin. M/S = "H": Output M/S = "L": Input	1
FRS	O	Static drive output pin. This is effective only when in master mode, and is used with the FR pin. This pin is HZ in slave mode.	1

(continued)

● LCD Drive Circuit Signals (continued)

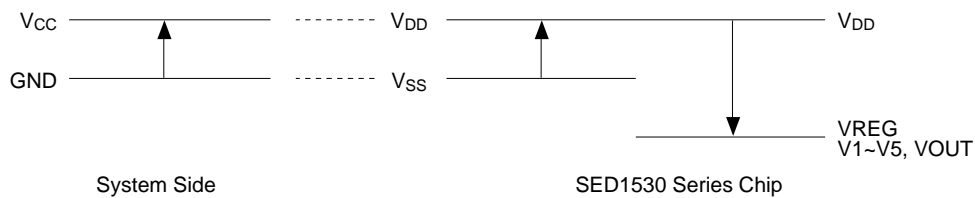
Pin	I/O	Function	Number of Pins																																																										
<i>On</i> (SEG <i>n</i>) (COM <i>n</i>)	O	<p>LC driver output</p> <p>This output depends on the model type, as shown below:</p> <table border="1"> <thead> <tr> <th></th> <th>Segment</th> <th>Column</th> </tr> </thead> <tbody> <tr> <td>SED1530*0*</td> <td>O0 ~ O99</td> <td>O100 ~ O131</td> </tr> <tr> <td>SED1530*A*</td> <td>O16 ~ O115</td> <td>O0 ~ O15, O116 ~ O131</td> </tr> <tr> <td>SED1531*0*</td> <td>O0 ~ O131</td> <td>\</td> </tr> <tr> <td>SED1530*0*</td> <td>O0 ~ O99</td> <td>O100 ~ O131</td> </tr> <tr> <td>SED1532*B*</td> <td>O32 ~ O131</td> <td>O0 ~ O31</td> </tr> </tbody> </table> <p>Segment Output Terminal</p> <p>This is the output for driving the LC segments. Through combining the contents of the display RAM with the FR signal, a single level can be selected from V_{DD}, V2, V3, and V5:</p> <table border="1"> <thead> <tr> <th rowspan="2">RAM Data</th> <th rowspan="2">FR</th> <th colspan="2">On Output Voltage</th> </tr> <tr> <th>Positive Display</th> <th>Negative Display</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V_{DD}</td> <td>V2</td> </tr> <tr> <td>L</td> <td>V5</td> <td>V3</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V2</td> <td>V_{DD}</td> </tr> <tr> <td>L</td> <td>V3</td> <td>V5</td> </tr> <tr> <td>Power Save</td> <td>—</td> <td colspan="2">V_{DD}</td> </tr> </tbody> </table> <p>Common Output Terminal</p> <p>This is the output for driving the LC commons. Through combining the scan data with the FR signal, a single level can be selected from V_{DD}, V1, V4, and V5:</p> <table border="1"> <thead> <tr> <th>Scan Data</th> <th>FR</th> <th>On Output Voltage</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V5</td> </tr> <tr> <td>L</td> <td>V_{DD}</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V1</td> </tr> <tr> <td>L</td> <td>V4</td> </tr> <tr> <td>Power Save</td> <td>—</td> <td>V_{DD}</td> </tr> </tbody> </table>		Segment	Column	SED1530*0*	O0 ~ O99	O100 ~ O131	SED1530*A*	O16 ~ O115	O0 ~ O15, O116 ~ O131	SED1531*0*	O0 ~ O131	\	SED1530*0*	O0 ~ O99	O100 ~ O131	SED1532*B*	O32 ~ O131	O0 ~ O31	RAM Data	FR	On Output Voltage		Positive Display	Negative Display	H	H	V _{DD}	V2	L	V5	V3	L	H	V2	V _{DD}	L	V3	V5	Power Save	—	V _{DD}		Scan Data	FR	On Output Voltage	H	H	V5	L	V _{DD}	L	H	V1	L	V4	Power Save	—	V _{DD}	133
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Power Save	—	V _{DD}																																																											
COMS	O	<p>This is a common output pin dedicated for the indicator.</p> <p>Leave open if not used. This pin is functional only for the SED1530 and SED1532. It is HZ for the SED1531.</p>	1																																																										

SED1530 Series

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		V _{DD}	-0.3 to +7.0	V
	(at 3× step-up)		-0.3 to +6.0	V
	(at 4× step-up)		-0.3 to +4.5	V
Power supply voltage (2)	(V _{DD} reference)	V5	-18.0 to +0.3	V
Power supply voltage (3)	(V _{DD} reference)	V1, V2, V3, V4	V5 to +0.3	V
Input voltage		V _{IN}	-0.3 to V _{DD} + 0.3	V
Output voltage		V _O	-0.3 to V _{DD} + 0.3	V
Operating temperature		T _{opr}	-30 to +85	°C
Storage temperature	TCP	T _{STR}	-55 to +100	°C
	Bare chip		-55 to +125	°C



Notes:

- V1 ~ V5, V_{OUT}, and the V5 voltage are all values based on V_{DD} = 0V.
- The voltages of V1, V2, V3 and V4 must always fulfill the relationship V_{DD} ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5.
- Permanent damage to the LSI may result if the absolute maximum ratings are exceeded during use. Under normal operation, use should be within the range of the electrical characteristics listed. Violations of these conditions may cause the LSI to malfunction or may cause loss of reliability in the LSI.

● DC Characteristics

V_{SS} = 0V, V_{DD} = 5V ±10%, T_a = -40 to 85°C

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Pin	
Power supply voltage (1)	Recommended operation	V _{DD}		4.5	5.0	5.5	V	V _{SS} *1	
	Possible operation	V _{DD}		2.4	—	6.0			
Operating voltage (2)	Possible operation	V5	V _{DD} reference (V _{DD} = 0V)	-16.0	—	-4.0	V	V5 *2	
	Possible operation	V1, V2	V _{DD} reference (V _{DD} = 0V)	0.4 × V5	—	V _{DD}	V	V1, V2	
	Possible operation	V3, V4	V _{DD} reference (V _{DD} = 0V)	V5	—	0.6 × V5	V	V3, V4	
CMOS	High-level input voltage	V _{IHC}		0.7 × V _{DD}	—	V _{DD}	V	*3	
			V _{DD} = 2.7V	0.8 × V _{DD}	—	V _{DD}			
	Low-level input voltage	V _{ILC}		V _{SS}	—	0.3 × V _{DD}	V	*3	
			V _{DD} = 2.7V	V _{SS}	—	0.2 × V _{DD}			
High-level output voltage	V _{OHC}	I _{OH} = 1mA	0.8 × V _{DD}	—	V _{DD}	V	*5		
		V _{DD} = 2.7V I _{OH} = -0.5mA	0.8 × V _{DD}	—	V _{DD}				
Low-level output voltage	V _{OLC}	I _{OL} = 1mA	V _{SS}	—	0.2 × V _{DD}	V	*5		
		V _{DD} = 2.7V I _{OL} = 0.5mA	V _{SS}	—	0.2 × V _{DD}				
Schmitt	High-level input voltage	V _{IHS}		0.85 × V _{DD}	—	V _{DD}	V	*4	
			V _{DD} = 2.7V	0.8 × V _{DD}	—	V _{DD}			
	Low-level input voltage	V _{ILS}		V _{SS}	—	0.15 × V _{DD}	V	*4	
V _{DD} = 2.7V			V _{SS}	—	0.2 × V _{DD}				
Input leak current	I _{LI}	V _{IN} = V _{DD} or V _{SS}		-1.0	—	1.0	μA	*6	
Output leak current	I _{LO}			-3.0	—	3.0	μA	*7	
LC driver ON resistance	R _{ON}	T _a = 25°C V _{DD} ref.	V5 = -14.0V	—	2.0	3.0	kΩ	SEG _n	
			V5 = -8.0V	—	3.0	4.5	kΩ	COM _n	
Static consumption current	I _{SSQ}	V _{IN} = V _{DD} or V _{SS}		—	0.01	5.0	μA	V _{SS}	
	I _{SQ}	V5 = -18.0V V _{DD} ref.		—	0.01	15.0	μA	V5	
Input terminal capacitance	C _{IN}	T _a = 25°C f = 1MHz		—	5.0	8.0	pF	*3, *4	
Oscillator frequency	f _{OSC}	T _a = 25°C	V _{DD} = 5.0V	19	22	25	kHz		
			V _{DD} = 2.7V	19	22	25			
Internal Power Supply Circuit	Input voltage	V _{DD}	When 3x step-up	2.4	—	6.0	V		
			When 4x step-up	2.4	—	4.5			
	Booster output voltage	V _{OUT}	When 3x V _{DD} Ref. set-up	-18.0	—	—	V	V _{OUT}	
	Voltage regulator circuit operating voltage	V _{OUT}	V _{DD} Ref.	-18.0	—	-6.0	V	V _{OUT}	
	Voltage follower operating voltage	V5 (1)	When applied to the SED1530	V _{DD} Ref.	-16.0	—	-6.0	V	
				V _{DD} Ref.	-16.0	—	-4.6	V	
Reference voltage	V _{REG}	T _a = 25°C	V _{DD} Ref.	-2.65	-2.5	-2.35	V		

SED1530 Series

- Dynamic consumption current value (1) in display, internal power supply ON

Unless otherwise specified, $T_a = -40$ to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
SED1530	I _{DD} (1)	V _{DD} = 5.0V, V5 - V _{DD} = -8.0V, 2× Step-up	—	41	70	μA	
		V _{DD} = 3.0V, V5 - V _{DD} = -8.0V, 3× Step-up	—	48	80	μA	
SED1531		V _{DD} = 5.0V, V5 - V _{DD} = -11.0V, 3× Step-up	—	96	160	μA	
		V _{DD} = 3.0V, V5 - V _{DD} = -11.0V, 4× Step-up	—	118	190	μA	
SED1532		V _{DD} = 5.0V, V5 - V _{DD} = -11.0V, 3× Step-up	—	96	160	μA	
		V _{DD} = 3.0V, V5 - V _{DD} = -11.0V, 4× Step-up	—	114	190	μA	

- Current consumption in power save mode

(V_{SS} = 0V, V_{DD} = 2.7 to 5.5V, T_a = 25°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Standby	I _{DD} S1	SED1530, SED1531, SED1532	—	0.01	1.0	μA
	I _{DD} S2	SED1530, SED1531, SED1532	—	1.0	2.0	μA

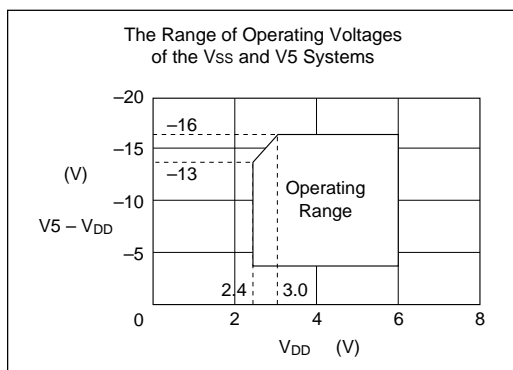
Typical current consumption characteristics:

Dynamic current consumption (1)

LCD display status using an external power supply

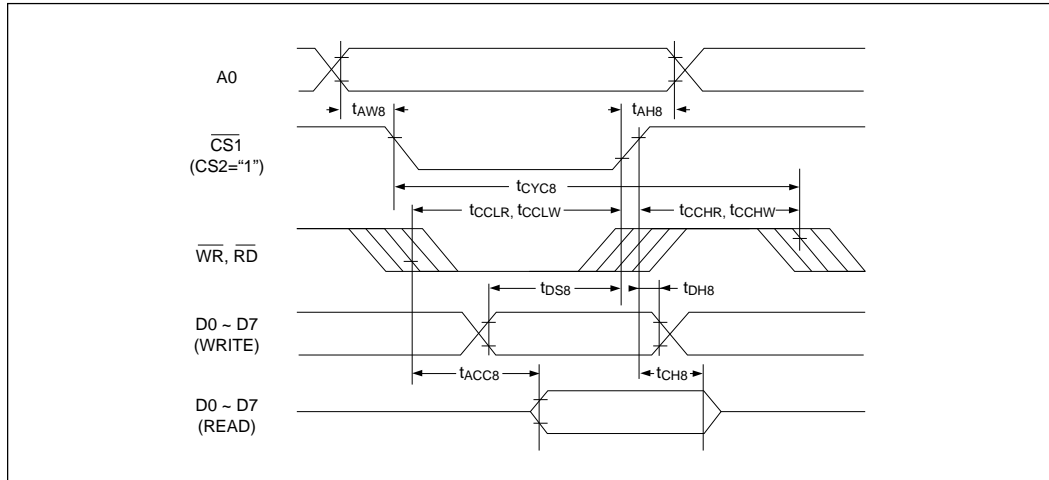
Notes

- *1. Although a broad operating voltage range is guaranteed, this does not guarantee against sudden voltage changes during MPU access.
- *2. The range of operating voltages of the V_{DD} system and V5 system. See the figure below. The range of operating voltages applies when the external power supply is used.
- *3. The A0, D0 to D5, D6, D7 (SI), $\overline{\text{RD}}$ (E), $\overline{\text{WR}}$ (R/W), $\overline{\text{CS}}$ 1, CS2, FR, M/S, C86, P/S and DOF pins.
- *4. The CL, SCL (D6) and $\overline{\text{RES}}$ pins.
- *5. The D0 to D5, D6, D7 (SI), FR, FRS, DY0, $\overline{\text{DOF}}$ and CL pins.
- *6. The A0, $\overline{\text{RD}}$, (E), $\overline{\text{WR}}$ (R/W), $\overline{\text{CS}}$ 1, CS2, M/S, $\overline{\text{RES}}$, C86 and P/S pins.
- *7. Applicable when the D0 to D7, FR, CL, DY0 and DOF pins are in a high impedance state.



SED1530 Series

- Timing Characteristics
 - System Bus: Read/Write Characteristics I (80-Series MPU)



$V_{DD} = 5.0V \pm 10\%$, $T_a = -40$ to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	tAH8		10	—	ns
Address setup time	A0	tAW8		10	—	ns
System cycle time		tCYC8		200	—	ns
Control L pulse width (WR)	$\overline{\text{WR}}$	tcCLW		22	—	ns
Control L pulse width (RD)	$\overline{\text{RD}}$	tcCLR		77	—	ns
Control H pulse width (WR)	$\overline{\text{WR}}$	tcCHW		172	—	ns
Control H pulse width (RD)	$\overline{\text{RD}}$	tcCHR		117	—	ns
Data setup time	D0 ~ D7	tDS8		20	—	ns
Data hold time	D0 ~ D7	tDH8		10	—	ns
RD access time		tACC8	CL = 100pF	—	70	ns
Output disable time		tCH8		10	50	ns

$V_{DD} = 2.7$ to $4.5V$, $T_a = -40$ to 85°C

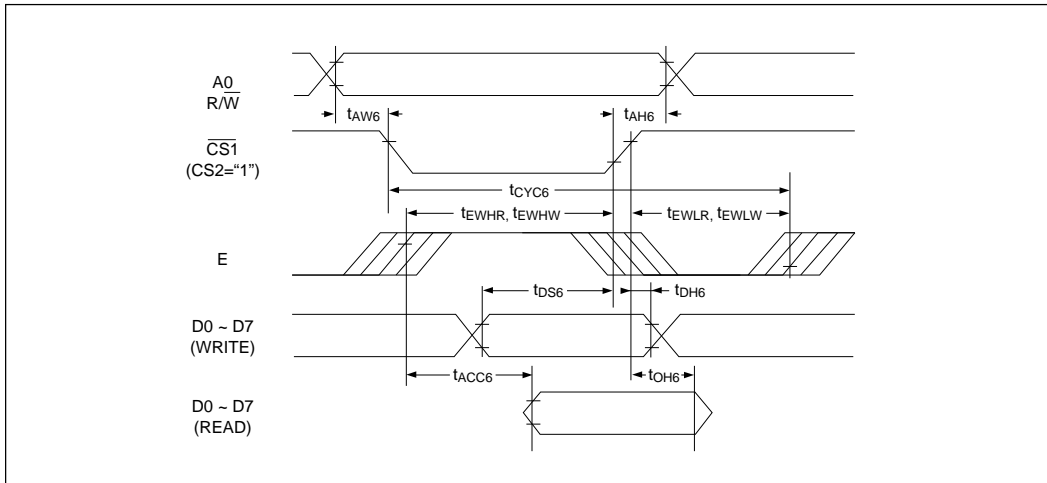
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	tAH8		25	—	ns
Address setup time	A0	tAW8		25	—	ns
System cycle time		tCYC8		450	—	ns
Control L pulse width (WR)	$\overline{\text{WR}}$	tcCLW		44	—	ns
Control L pulse width (RD)	$\overline{\text{RD}}$	tcCLR		194	—	ns
Control H pulse width (WR)	$\overline{\text{WR}}$	tcCHW		394	—	ns
Control H pulse width (RD)	$\overline{\text{RD}}$	tcCHR		244	—	ns
Data setup time	D0 ~ D7	tDS8		40	—	ns
Data hold time	D0 ~ D7	tDH8		20	—	ns
RD access time		tACC8	CL = 100pF	—	140	ns
Output disable time		tCH8		10	100	ns

*1. The input signal rise time and fall time (t_r , t_f) are specified at 15ns or less. When the cycle time is used at high speed, the specification is $t_r + t_f \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CLR} - t_{CHR})$.

*2. All timings are specified based on 20% and 80% of V_{DD} .

*3. tcCLW and tcCLR are specified by the overlap period of $\text{CS1} = "0"$ ($\text{CS2} = "1"$) and $\overline{\text{WR}}, \overline{\text{RD}} = "0"$ level.

○ System Bus: Read/Write Characteristics I (68-Series MPU)



$V_{DD} = 5.0V \pm 10\%$, $T_a = -40$ to $85^\circ C$

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		tCYC6		200	—	ns
Address setup time	A0	tAW6		10	—	ns
Address hold time	R/W	tAH6		10	—	ns
Data setup time	D0 ~ D7	tDS6		20	—	ns
Data hold time		tDH6		10	—	ns
Output disable time		tOH6	CL = 100pF	10	50	ns
Access time		tACC6		—	70	ns
Enable H pulse width	Read	E	tEWHR	77	—	ns
	Write		tEWHW	22	—	ns
Enable L pulse width	Read	E	tEWLR	117	—	ns
	Write		tEWLW	172	—	ns

$V_{DD} = 2.7$ to $4.5V$, $T_a = -40$ to $85^\circ C$

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		tCYC6		450	—	ns
Address setup time	A0	tAW6		25	—	ns
Address hold time	R/W	tAH6		25	—	ns
Data setup time	D0 ~ D7	tDS6		40	—	ns
Data hold time		tDH6		20	—	ns
Output disable time		tOH6	CL = 100pF	20	50	ns
Access time		tACC6		—	70	ns
Enable H pulse width	Read	E	tEWHR	194	—	ns
	Write		tEWHW	44	—	ns
Enable L pulse width	Read	E	tEWLR	244	—	ns
	Write		tEWLW	394	—	ns

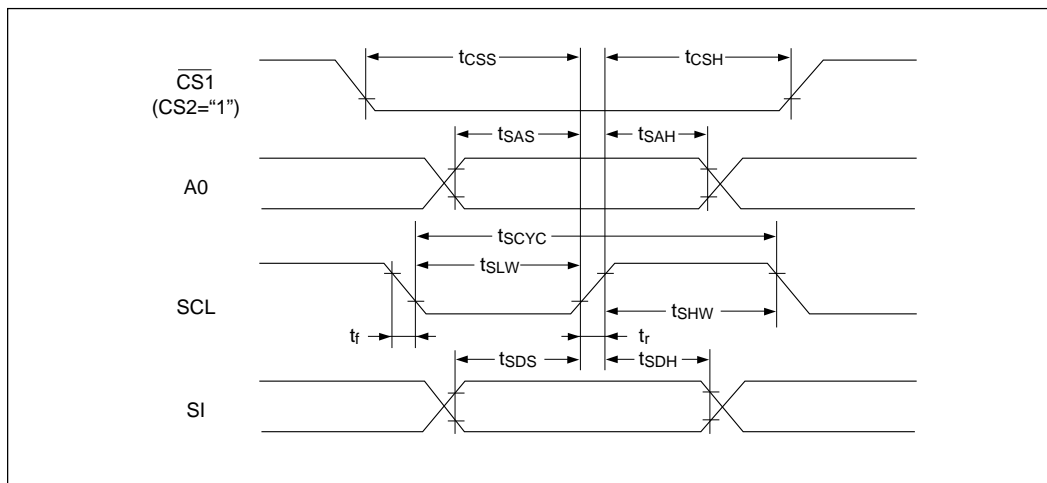
*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less. When the cycle time is used at high speed, the specification is $tr + tf \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $tr + tf \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.

*2. All timings are specified based on 20% and 80% of V_{DD} .

*3. tEWHR and tEWHW are specified by the overlap period of $\overline{CS1} = "0"$ ($CS2 = "1"$) and $E = "1"$ level.

SED1530 Series

Serial Interface



$V_{DD} = 5.0V \pm 10\%$, $T_a = -40$ to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock period	SCL	tSCYC		500	—	ns
SCL "H" pulse width		tSHW		150	—	ns
SCL "L" pulse width		tsLW		150	—	ns
Address setup time	A0	tsAS		120	—	ns
Address hold time		tsAH		200	—	ns
Data setup time	SI	tsDS		120	—	ns
Data hold time		tsDH		50	—	ns
CS-SCL time	CS	tcSS		30	—	ns
		tcSH		400	—	ns

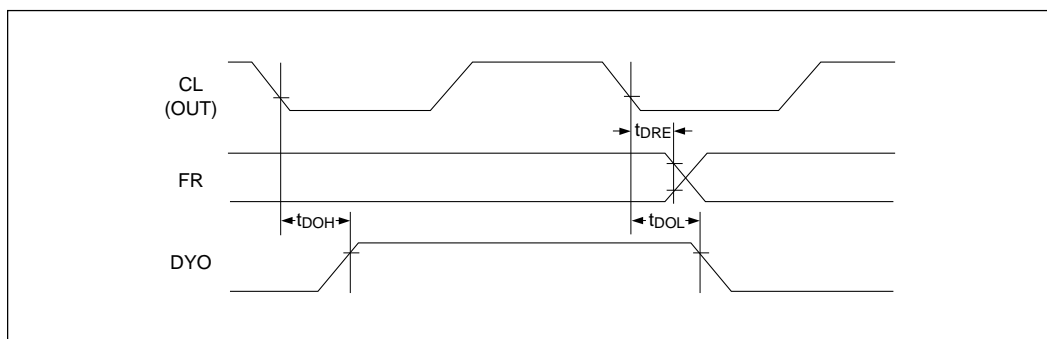
$V_{DD} = 2.7$ to $4.5V$, $T_a = -40$ to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock period	SCL	tSCYC		1000	—	ns
SCL "H" pulse width		tSHW		300	—	ns
SCL "L" pulse width		tsLW		300	—	ns
Address setup time	A0	tsAS		250	—	ns
Address hold time		tsAH		400	—	ns
Data setup time	SI	tsDS		250	—	ns
Data hold time		tsDH		100	—	ns
CS-SCL time	CS	tcSS		60	—	ns
		tcSH		400	—	ns

*1. The input signal rise time and fall time (t_r , t_f) are specified at 15ns or less.

*2. All timings are specified based on 20% and 80% of V_{DD} .

○ Display Control Timing



$V_{DD} = 5.0V \pm 10\%$, $T_a = -40$ to $85^\circ C$

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	tDFR	CL = 50pF	—	80	150	ns
DYO "H" delay time	DYO	tDOH		—	70	160	ns
DYO "L" delay time		tDOL		—	70	160	ns

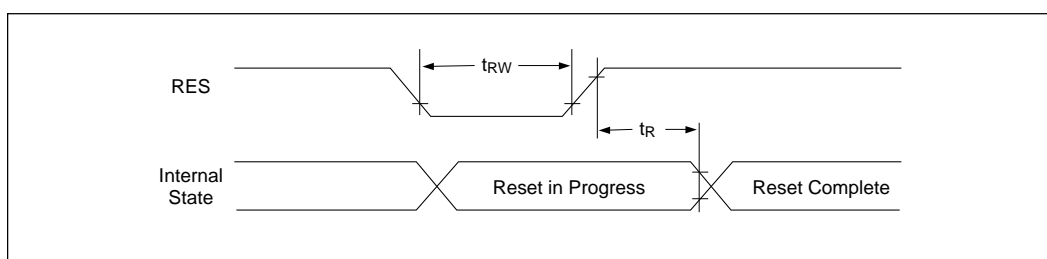
$V_{DD} = 2.7$ to $4.5V \pm 10\%$, $T_a = -40$ to $85^\circ C$

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	tDFR	CL = 50pF	—	120	240	ns
DYO "H" delay time	DYO	tDOH		—	140	250	ns
DYO "L" delay time		tDOL		—	140	250	ns

*1. Effective only when operating in master mode.

*2. All timings are specified based on 20% or 80% of V_{DD} .

○ Reset Timing



$V_{DD} = 5.0V \pm 10\%$, $T_a = -40$ to $85^\circ C$

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t _R		1.0	—	—	ms
Reset "L" pulse width	RES	t _{RW}		1.0	—	—	ms

$V_{DD} = 2.7$ to $4.5V$, $T_a = -40$ to $85^\circ C$

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t _R		3.0	—	—	ms
Reset "L" pulse width	RES	t _{RW}		3.0	—	—	ms

*1. All timings are specified based on 10% and 90% of V_{DD} .

SED1530 Series

● Table of Commands for the SED1530 Series

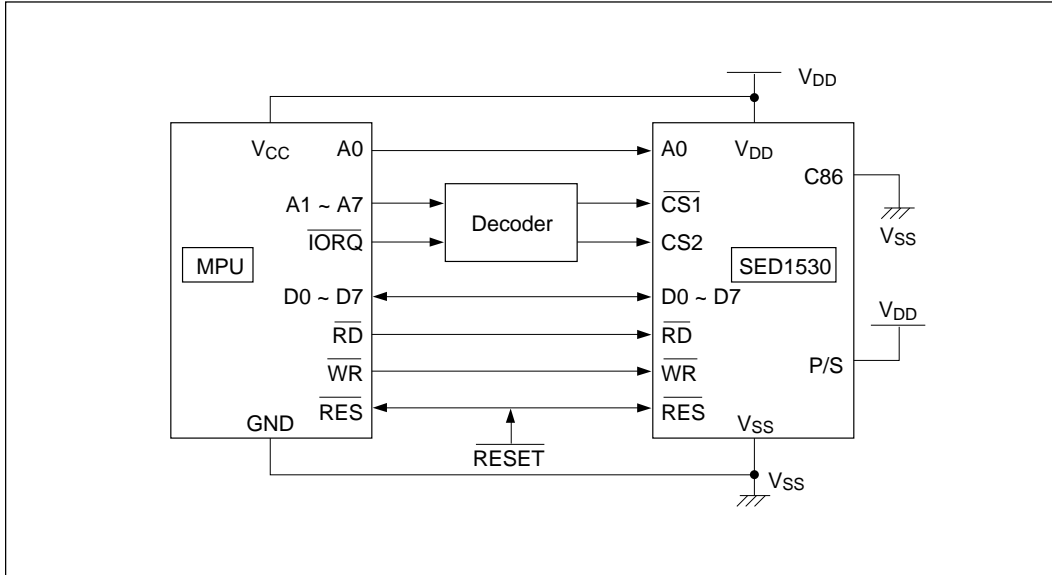
Command		Code											Function		
		A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0			
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	1	0	1	Turns the LCD display on and off. 0: OFF 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address					Determines the RAM display line displayed to COM0.			
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page to the page address register.		
(4)	Column address set, first 4 bits	0	1	0	0	0	0	1	Most significant column address bits			Sets the 4 most significant bits of the display RAM column address to the register.			
(4)	Column address set, last 4 bits	0	1	0	0	0	0	0	Least significant column address bits			Sets the 4 least significant bits of the display RAM column address to the register.			
(5)	Status read	0	0	1	Status				0	0	0	0	Read status data.		
(6)	Write display data	1	1	0	Write data								Writes to the display RAM.		
(7)	Reads display data	1	0	1	Read data								Reads from the display RAM.		
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0	0	1	Sets the relationship between the display RAM address and the SEG output 0: Normal 1: Reverse
(9)	Display: Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0	1	0	Sets the LCD display to normal/reverse. 0: Normal 1: Reverse
(10)	Display: All Pixel Lit: ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	0	Display: All Pixels Lit 0: Normal display 1: All pixels lit
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0	0	0	Sets the LCD drive voltage ratio.
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	0	0	Increments the column address counter by 1 when write, zero when read.
(13)	End	0	1	0	1	1	1	0	1	1	1	0	0	0	Gets out of read/modify/write mode.
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	0	0	Internal reset.
(15)	Output mode register set	0	1	0	1	1	0	0	0	*	*	*	*	*	Selects the direction of the COM output scan. * = disabled
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode		Selects the power supply circuit operating mode.			
(17)	Electronic volume register set	0	1	0	1	0	0	Electronic volume level				Sets the V5 output voltage to the electronic volume register.			
(18)	Standby set	0	1	0	1	0	1	0	1	1	0	0	1	0	Selects the standby mode. 0: OFF 1: ON
(19)	Power save														A composite command with display: OFF and Display: All Pixels On.

Note: Do not use any other command, or a system malfunction may result.

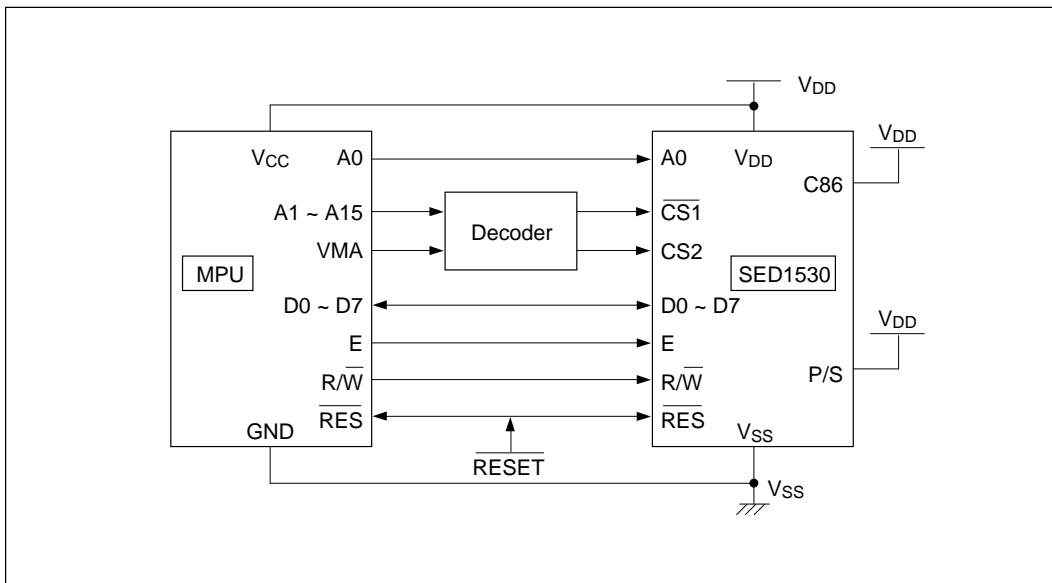
■ MPU INTERFACE (REFERENCE EXAMPLE)

The SED1530 Series chips can be connected to 80-series and 68-series MPUs. Moreover, by utilizing the serial interface, the connections can be made with fewer signal lines. When multiple SED1530 chips are used, each can be connected to the MPU and the chips can be selected using the chip select.

● 80-Series MPU

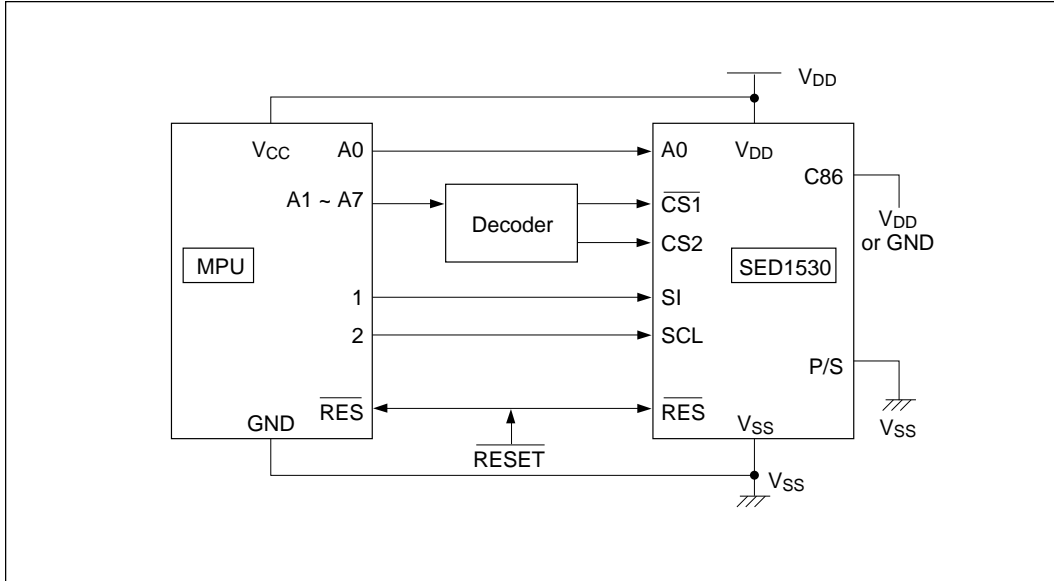


● 68-Series MPU

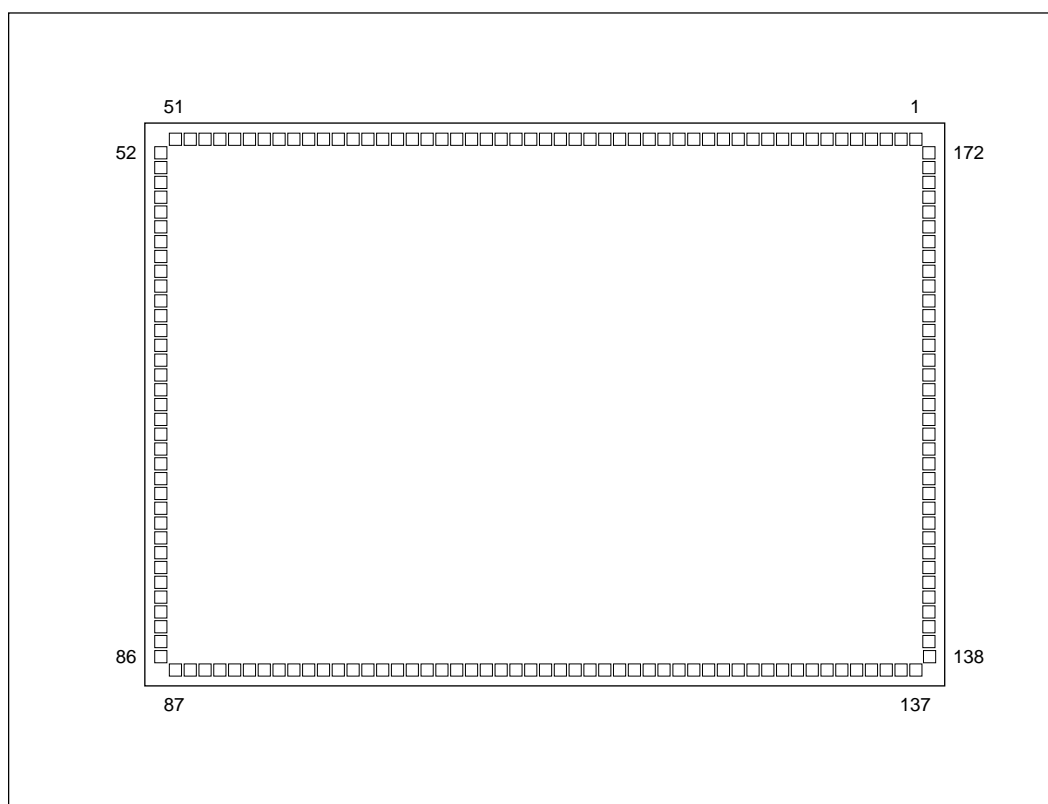


SED1530 Series

- Serial Interface



■ PIN LAYOUT



Chip Size:	6.65 X 4.57 mm
Pad Pitch:	118 μ m (Min.)
SED153*D_A	(Aluminum Pad Model)
Pad Center Size:	90 X 90 μ m
Chip Thickness:	300 μ m
SED153*D_B	(Gold Bump Model)
Bump Size:	76 X 76 μ m
Bump Height:	17 to 28 μ m (Typ)
Chip Thickness:	625 μ m

SED1530 Series

■ PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.	No.	Pin Name	X Coord.	Y Coord.	No.	Pin Name	X Coord.	Y Coord.	No.	Pin Name	X Coord.	Y Coord.
1	O127	2988	2142	46	O0	-2366	2142	91	O45	-2490	-2142	136	O90	2862	-2142
2	O128	2860	2142	47	O1	-2490	2142	92	O46	-2386	-2142	137	O91	2986	-2142
3	O129	2738	2142	48	O2	-2614	2142	93	O47	-2242	-2142	138	O92	3178	-2006
4	O130	2614	2142	49	O3	-2738	2142	94	O48	-2124	-2142	139	O93	3178	-1888
5	O131	2490	2142	50	O4	-2862	2142	95	O49	-2006	-2142	140	O94	3178	-1770
6	COM3	2386	2142	51	O5	-2986	2142	96	O50	-1888	-2142	141	O95	3178	-1652
7	FR5	2242	2142	52	O6	-3178	2006	97	O51	-1770	-2142	142	O96	3178	-1534
8	FR	2124	2142	53	O7	-3178	1888	98	O52	-1652	-2142	143	O97	3178	-1416
9	DYO	2006	2142	54	O8	-3178	1770	99	O53	-1534	-2142	144	O98	3178	-1298
10	CL	1000	2142	55	O9	-3178	1652	100	O54	-1416	-2142	145	O99	3178	-1180
11	DOF	1770	2142	56	O10	-3178	1534	101	O55	-1298	-2142	146	O100	3178	-1062
12	VSI	1652	2142	57	O11	-3178	1416	102	O56	-1180	-2142	147	O101	3178	-944
13	M/S	1534	2142	58	O12	-3178	1286	103	O57	-1062	-2142	148	O102	3178	-826
14	REG	1416	2142	59	O13	-3178	1150	104	O58	-944	-2142	149	O103	3178	-708
15	P/S	1298	2142	60	O14	-3178	1062	105	O59	-826	-2142	150	O104	3178	-590
16	CS1	1180	2142	61	O15	-3178	944	106	O60	-708	-2142	151	O105	3178	-472
17	CS2	1062	2142	62	O16	-3178	826	107	O61	-590	-2142	152	O106	3178	-354
18	C86	944	2142	63	O17	-3178	708	108	O62	-472	-2142	153	O107	3178	-236
19	A0	826	2142	64	O18	-3178	690	109	O63	-354	-2142	154	O108	3178	-118
20	WR (W/R)	708	2142	65	O19	-3178	472	110	O64	-236	-2142	155	O109	3178	0
21	RD (E)	590	2142	66	O20	-3178	364	111	O65	-118	-2142	156	O110	3178	118
22	V _{DD}	354	2142	67	O21	-3178	238	112	O66	0	-2142	157	O111	3178	236
23	D0	236	2142	68	O22	-3178	118	113	O67	118	-2142	158	O112	3178	354
24	D1	236	2142	69	O23	-3178	0	114	O68	236	-2142	159	O113	3178	472
25	D2	118	2142	70	O24	-3178	-118	115	O69	354	-2142	160	O114	3178	590
26	D3	0	2142	71	O25	-3178	-236	116	O70	472	-2142	161	O115	3178	708
27	D4	-118	2142	72	O26	-3178	-354	117	O71	590	-2142	162	O116	3178	826
28	D5	-236	2142	73	O27	-3178	-472	118	O72	708	-2142	163	O117	3178	944
29	D6 (SCL)	-354	2142	74	O28	-3178	-590	119	O73	826	-2142	164	O118	3178	1062
30	D7 (31)	-472	2142	75	O29	-3178	-708	120	O74	944	-2142	165	O119	3178	1180
31	V _{SS}	-590	2142	76	O30	-3178	-826	121	O75	1062	-2142	166	O120	3178	1298
32	V _{OUT}	-708	2142	77	O31	-3178	-944	122	O76	1180	-2142	167	O121	3178	1416
33	CAP3-	-826	2142	78	O32	-3178	-1062	123	O77	1298	-2142	168	O122	3178	1534
34	CAP1+	-944	2142	79	O33	-3178	-1180	124	O78	1416	-2142	169	O123	3178	1652
35	CAP1-	-1062	2142	80	O34	-3178	-1298	125	O79	1534	-2142	170	O124	3178	1770
36	CAP2+	-1180	2142	81	O35	-3178	-1418	126	O80	1652	-2142	171	O125	3178	1888
37	CAP2-	-1298	2142	82	O36	-3178	-1534	127	O81	1770	-2142	172	O126	3178	2006
38	V5	-1416	2142	83	O37	-3178	-1652	128	O82	1888	-2142				
39	VR	-1534	2142	84	O38	-3178	-1770	129	O83	2006	-2142				
40	V _{DD}	-1652	2142	85	O39	-3178	-1888	130	O84	2124	-2142				
41	V1	-1770	2142	86	O40	-3178	-2006	131	O85	2242	-2142				
42	V2	-1888	2142	87	O41	-2986	-2142	132	O86	2366	-2142				
43	V3	-2006	2142	88	O42	-2862	-2142	133	O87	2490	-2142				
44	V4	-2124	2142	89	O43	-2738	-2142	134	O88	2614	-2142				
45	V5	-2242	2142	90	O44	-2614	-2142	135	O89	2738	-2142				

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