

# S6B0717

## 55 COM / 100 SEG DRIVER & CONTROLLER FOR STN LCD

January.2000

Ver. 1.2

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### **Precautions for Light**

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

<b>S6B0717 Specification Revision History</b>		
<b>Version</b>	<b>Content</b>	<b>Date</b>
0.0		Apr.1999
1.0	Change VDD Range : 2.4V to 5.5V → 2.4V to 3.6V	Jan.2000
1.1	Added detail information for several items	Mar.2001
1.2	Change VDD Range : 2.4V to 3.6V → 2.4V to 5.5V	Mar.2002

# CONTENTS

<b>INTRODUCTION .....</b>	<b>1</b>
<b>FEATURES .....</b>	<b>1</b>
<b>BLOCK DIAGRAM .....</b>	<b>3</b>
<b>PAD CONFIGURATION .....</b>	<b>4</b>
<b>PAD CENTER COORDINATES .....</b>	<b>5</b>
<b>PIN DESCRIPTION .....</b>	<b>7</b>
POWER SUPPLY .....	7
LCD DRIVER SUPPLY .....	7
SYSTEM CONTROL.....	8
MICROPROCESSOR INTERFACE .....	10
LCD DRIVER OUTPUTS .....	12
<b>FUNCTIONAL DESCRIPTION .....</b>	<b>13</b>
MICROPROCESSOR INTERFACE .....	13
DISPLAY DATA RAM (DDRAM) .....	17
LCD DISPLAY CIRCUITS .....	20
LCD DRIVER CIRCUIT .....	22
POWER SUPPLY CIRCUITS .....	23
REFERECE CIRCUIT EXAMPLES .....	30
RESET CIRCUIT .....	32
<b>INSTRUCTION DESCRIPTION .....</b>	<b>33</b>
<b>SPECIFICATIONS .....</b>	<b>47</b>
ABSOLUTE MAXIMUM RATINGS .....	47
DC CHARACTERISTICS .....	48
REFERENCE DATA .....	51
AC CHARACTERISTICS .....	53
<b>REFERENCE APPLICATIONS .....</b>	<b>59</b>
MICROPROCESSOR INTERFACE .....	59
CONNECTIONS BETWEEN S6B0717 AND LCD PANEL .....	60



## INTRODUCTION

The S6B0717 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 55 common and 100 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 65 x 100 bits. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

## FEATURES

### Driver Output Circuits

- 55 common outputs / 100 segment outputs

### On-chip Display Data RAM

- Capacity: 65 x 100 = 6,500 bits
- Bit data "1": a dot of display is illuminated.
- Bit data "0": a dot of display is not illuminated.

### Multi-chip Operation (Master, Slave) Available

### Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/55	1/8 or 1/6	55 × 100
1/34	1/6 or 1/5	34 × 100

### Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- Serial interface (only write operation) available

### On-Chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x2, x3, x4, x5)
- Voltage regulator (temperature coefficient: -0.05%/°C or external input)
- Voltage follower (LCD bias: 1/5, 1/6 or 1/8)
- Electronic contrast control function (64 steps)

### Operating Voltage Range

- Supply voltage (VDD): 2.4 to 3.3 V
- Supply voltage (VDD): 2.4 to 5.5 V (Select by product code)
- LCD driving voltage (VLCD = V0 - VSS): 4.0 to 15.0 V

### Wide Operating Temperature Range

- Ta = -40°C to 85 °C

### Low Power Consumption

- 100 µA Max. (VDD = 3V, x4 boosting, V0 = 11V, internal power supply ON)
- 10 µA Max. (during power save [standby] mode)

### Package Type

- Gold bumped chip or TCP

## Series Specifications

Product code	Temp. coefficient	Package	Chip thickness	VDD Range
S6B0717X01-B0CZ	-0.05% / °C	COG	670 μm	2.4~3.6[V]
S6B0717X01-B0CY			470 μm	
S6B0717X01-xxX0		TCP	670 μm	
S6B0717X01-xxXN			470 μm	
S6B0717X05-B0CZ	-0.05% / °C	COG	670 μm	2.4~5.5[V]
S6B0717X05-B0CY			470 μm	
S6B0717X05-xxX0		TCP	670 μm	
S6B0717X05-xxXN			470 μm	

\* xx: TCP ordering number

**BLOCK DIAGRAM**

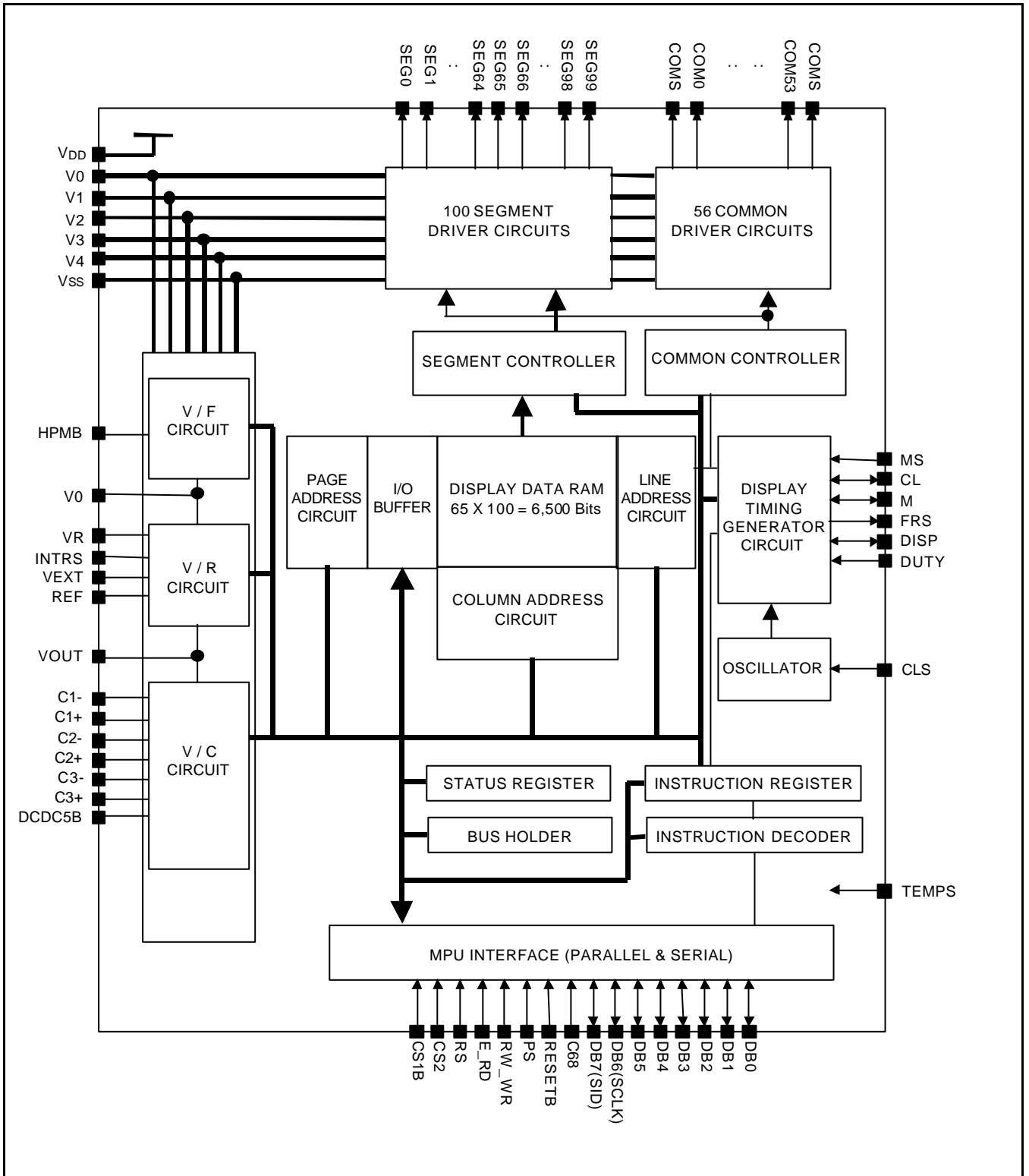


Figure 1. Block Diagram

### PAD CONFIGURATION

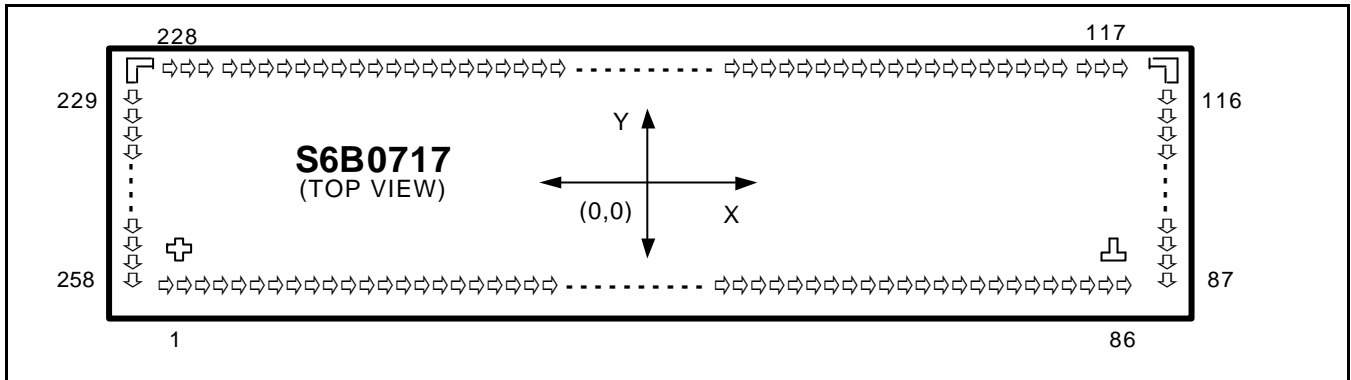


Figure 2. S6B0717 Chip Configuration

Table 1. S6B0717 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	9000	2350	μm
Pad pitch	1 to 86	90		
	87 to 258	70		
Bumped pad size	1 to 86	56	114	
	87 to 116	108	50	
	117 to 228	50	108	
	229 to 258	108	50	
Bumped pad height	1 to 258	17 (Typ.)		

Figure 3. COG Align Key Coordinate

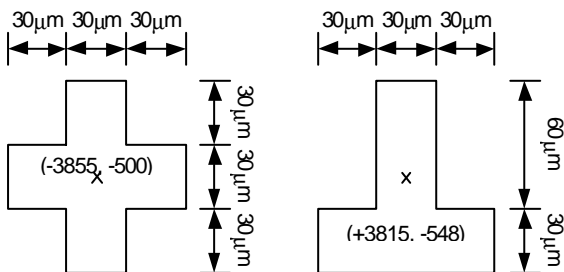
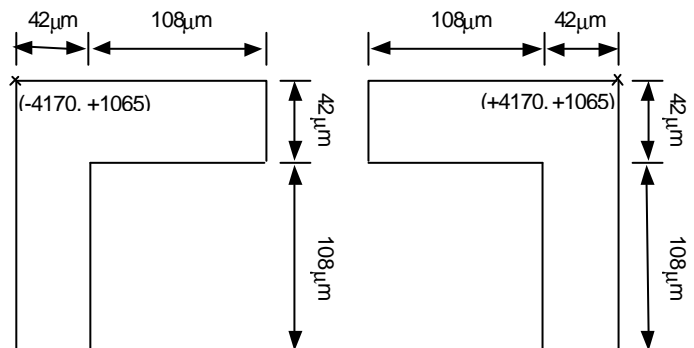


Figure 4. ILB Align Key Coordinate (with Gold Bump \*)



\* When designing electrode pattern must be prohibited on this area (ILB Align Key). If electrode pattern is used for routing over this area, it can be happened pattern-short through gold bump pattern on ILB Align Key.



## PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit:  $\mu\text{m}$ ]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-3825	-1051	51	C3-	675	-1051	101	COM13	4341	-35
2	FRS	-3735	-1051	52	C1-	765	-1051	102	COM12	4341	35
3	M	-3645	-1051	53	C1-	855	-1051	103	COM11	4341	105
4	CI	-3555	-1051	54	C1+	945	-1051	104	COM10	4341	175
5	DISP	-3465	-1051	55	C1+	1035	-1051	105	COM9	4341	245
6	VSS	-3375	-1051	56	C1+	1125	-1051	106	COM8	4341	315
7	CS1B	-3285	-1051	57	C2+	1215	-1051	107	COM7	4341	385
8	CS2	-3195	-1051	58	C2+	1305	-1051	108	COM6	4341	455
9	VDD	-3105	-1051	59	C2-	1395	-1051	109	COM5	4341	525
10	E_RD	-3015	-1051	60	C2-	1485	-1051	110	COM4	4341	595
11	RESETB	-2925	-1051	61	C2-	1575	-1051	111	COM3	4341	665
12	VSS	-2835	-1051	62	VDD	1665	-1051	112	COM2	4341	735
13	RS	-2745	-1051	63	VEXT	1755	-1051	113	COM1	4341	805
14	RW_WR	-2655	-1051	64	REF	1845	-1051	114	COM0	4341	875
15	DB0	-2565	-1051	65	VSS	1935	-1051	115	COMS	4341	945
16	DB1	-2475	-1051	66	V1	2025	-1051	116	DUMMY	4341	1015
17	DB2	-2385	-1051	67	V1	2115	-1051	117	DUMMY	3885	1016
18	DB3	-2295	-1051	68	V2	2205	-1051	118	DUMMY	3815	1016
19	DB4	-2205	-1051	69	V2	2295	-1051	119	DUMMY	3745	1016
20	DB5	-2115	-1051	70	V3	2385	-1051	120	DUMMY	3675	1016
21	DB6	-2025	-1051	71	V3	2475	-1051	121	DUMMY	3605	1016
22	DB7	-1935	-1051	72	V4	2565	-1051	122	DUMMY	3535	1016
23	VSS	-1845	-1051	73	V4	2655	-1051	123	SEG0	3465	1016
24	MS	-1755	-1051	74	V0	2745	-1051	124	SEG1	3395	1016
25	CLS	-1665	-1051	75	V0	2835	-1051	125	SEG2	3325	1016
26	VDD	-1575	-1051	76	VR	2925	-1051	126	SEG3	3255	1016
27	DCDC5B	-1485	-1051	77	VR	3015	-1051	127	SEG4	3185	1016
28	O68	-1395	-1051	78	VSS	3105	-1051	128	SEG5	3115	1016
29	VSS	-1305	-1051	79	VSS	3195	-1051	129	SEG6	3045	1016
30	VSS	-1215	-1051	80	PS	3285	-1051	130	SEG7	2975	1016
31	VSS	-1125	-1051	81	HPMB	3375	-1051	131	SEG8	2905	1016
32	VSS	-1035	-1051	82	VDD	3465	-1051	132	SEG9	2835	1016
33	VSS	-945	-1051	83	INTRS	3555	-1051	133	SEG10	2765	1016
34	VSS	-855	-1051	84	TEMPS	3645	-1051	134	SEG11	2695	1016
35	VSS	-765	-1051	85	VSS	3735	-1051	135	SEG12	2625	1016
36	DUTY	-675	-1051	86	DUMMY	3825	-1051	136	SEG13	2555	1016
37	VDD	-585	-1051	87	DUMMY	4341	-1015	137	SEG14	2485	1016
38	VDD	-495	-1051	88	COM26	4341	-945	138	SEG15	2415	1016
39	VDD	-405	-1051	89	COM25	4341	-875	139	SEG16	2345	1016
40	VDD	-315	-1051	90	COM24	4341	-805	140	SEG17	2275	1016
41	VDD	-225	-1051	91	COM23	4341	-735	141	SEG18	2205	1016
42	VDD	-135	-1051	92	COM22	4341	-665	142	SEG19	2135	1016
43	VDD	-45	-1051	93	COM21	4341	-595	143	SEG20	2065	1016
44	VOUT	45	-1051	94	COM20	4341	-525	144	SEG21	1995	1016
45	VOUT	135	-1051	95	COM19	4341	-455	145	SEG22	1925	1016
46	VOUT	225	-1051	96	COM18	4341	-385	146	SEG23	1855	1016
47	C3+	315	-1051	97	COM17	4341	-315	147	SEG24	1785	1016
48	C3+	405	-1051	98	COM16	4341	-245	148	SEG25	1715	1016
49	C3-	495	-1051	99	COM15	4341	-175	149	SEG26	1645	1016
50	C3-	585	-1051	100	COM14	4341	-105	150	SEG27	1575	1016

Table 2. Pad Center Coordinates (Continued)

[Unit:  $\mu\text{m}$ ]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
151	SEG28	1505	1016	201	SEG78	-1995	1016	251	COM48	-4341	-525
152	SEG29	1435	1016	202	SEG79	-2065	1016	252	COM49	-4341	-595
153	SEG30	1365	1016	203	SEG80	-2135	1016	253	COM50	-4341	-665
154	SEG31	1295	1016	204	SEG81	-2205	1016	254	COM51	-4341	-735
155	SEG32	1225	1016	205	SEG82	-2275	1016	255	COM52	-4341	-805
156	SEG33	1155	1016	206	SEG83	-2345	1016	256	COM53	-4341	-875
157	SEG34	1085	1016	207	SEG84	-2415	1016	257	COM5	-4341	-945
158	SEG35	1015	1016	208	SEG85	-2485	1016	258	DUMMY	-4341	-1015
159	SEG36	945	1016	209	SEG86	-2555	1016				
160	SEG37	875	1016	210	SEG87	-2625	1016				
161	SEG38	805	1016	211	SEG88	-2695	1016				
162	SEG39	735	1016	212	SEG89	-2765	1016				
163	SEG40	665	1016	213	SEG90	-2835	1016				
164	SEG41	595	1016	214	SEG91	-2905	1016				
165	SEG42	525	1016	215	SEG92	-2975	1016				
166	SEG43	455	1016	216	SEG93	-3045	1016				
167	SEG44	385	1016	217	SEG94	-3115	1016				
168	SEG45	315	1016	218	SEG95	-3185	1016				
169	SEG46	245	1016	219	SEG96	-3255	1016				
170	SEG47	175	1016	220	SEG97	-3325	1016				
171	SEG48	105	1016	221	SEG98	-3395	1016				
172	SEG49	35	1016	222	SEG99	-3465	1016				
173	SEG50	-35	1016	223	DUMMY	-3535	1016				
174	SEG51	-105	1016	224	DUMMY	-3605	1016				
175	SEG52	-175	1016	225	DUMMY	-3675	1016				
176	SEG53	-245	1016	226	DUMMY	-3745	1016				
177	SEG54	-315	1016	227	DUMMY	-3815	1016				
178	SEG55	-385	1016	228	DUMMY	-3885	1016				
179	SEG56	-455	1016	229	DUMMY	-4341	1015				
180	SEG57	-525	1016	230	COM27	-4341	945				
181	SEG58	-595	1016	231	COM28	-4341	875				
182	SEG59	-665	1016	232	COM29	-4341	805				
183	SEG60	-735	1016	233	COM30	-4341	735				
184	SEG61	-805	1016	234	COM31	-4341	665				
185	SEG62	-875	1016	235	COM32	-4341	595				
186	SEG63	-945	1016	236	COM33	-4341	525				
187	SEG64	-1015	1016	237	COM34	-4341	455				
188	SEG65	-1085	1016	238	COM35	-4341	385				
189	SEG66	-1155	1016	239	COM36	-4341	315				
190	SEG67	-1225	1016	240	COM37	-4341	245				
191	SEG68	-1295	1016	241	COM38	-4341	175				
192	SEG69	-1365	1016	242	COM39	-4341	105				
193	SEG70	-1435	1016	243	COM40	-4341	35				
194	SEG71	-1505	1016	244	COM41	-4341	-35				
195	SEG72	-1575	1016	245	COM42	-4341	-105				
196	SEG73	-1645	1016	246	COM43	-4341	-175				
197	SEG74	-1715	1016	247	COM44	-4341	-245				
198	SEG75	-1785	1016	248	COM45	-4341	-315				
199	SEG76	-1855	1016	249	COM46	-4341	-385				
200	SEG77	-1925	1016	250	COM47	-4341	-455				

## PIN DESCRIPTION

### POWER SUPPLY

**Table 3. Power Supply Pins Description**

Name	I/O	Description																				
VDD	Supply	Power supply																				
VSS	Supply	Ground																				
V0 V1 V2 V3 V4	I/O	<p>LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship; <math>V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS</math> When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</p> <table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/8 bias</td> <td><math>(7/8) \times V0</math></td> <td><math>(6/8) \times V0</math></td> <td><math>(2/8) \times V0</math></td> <td><math>(1/8) \times V0</math></td> </tr> <tr> <td>1/6 bias</td> <td><math>(5/6) \times V0</math></td> <td><math>(4/6) \times V0</math></td> <td><math>(2/6) \times V0</math></td> <td><math>(1/6) \times V0</math></td> </tr> <tr> <td>1/5 bias</td> <td><math>(4/5) \times V0</math></td> <td><math>(3/5) \times V0</math></td> <td><math>(2/5) \times V0</math></td> <td><math>(1/5) \times V0</math></td> </tr> </tbody> </table>	LCD bias	V1	V2	V3	V4	1/8 bias	$(7/8) \times V0$	$(6/8) \times V0$	$(2/8) \times V0$	$(1/8) \times V0$	1/6 bias	$(5/6) \times V0$	$(4/6) \times V0$	$(2/6) \times V0$	$(1/6) \times V0$	1/5 bias	$(4/5) \times V0$	$(3/5) \times V0$	$(2/5) \times V0$	$(1/5) \times V0$
LCD bias	V1	V2	V3	V4																		
1/8 bias	$(7/8) \times V0$	$(6/8) \times V0$	$(2/8) \times V0$	$(1/8) \times V0$																		
1/6 bias	$(5/6) \times V0$	$(4/6) \times V0$	$(2/6) \times V0$	$(1/6) \times V0$																		
1/5 bias	$(4/5) \times V0$	$(3/5) \times V0$	$(2/5) \times V0$	$(1/5) \times V0$																		

### LCD DRIVER SUPPLY

**Table 4. LCD Driver Supply Pins Description**

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3-	O	Capacitor 3 negative connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin
DCDC5B	I	5 times boosting circuit enable input pin. When this pin is low in 4 times boosting circuit, the 5 times boosting voltage appears at VOOUT
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L")
VEXT	I	External VREF input pin for the LCD power supply voltage regulator
REF	I	Selects the external VREF voltage via the VEXT pin – REF = "H": using the internal VREF – REF = "L": using the external VREF

## SYSTEM CONTROL

Table 5. System Control Pins Description

Name	I/O	Description							
MS	I	Master / Slave operation select pin – MS = "H": master operation – MS = "L": slave operation The following table depends on the MS status.							
		MS	CLS	OSC circuit	Power supply circuit	CL	M	FRS	DISP
		H	H	Enabled	Enabled	Output	Output	Output	Output
			L	Disabled	Enabled	Input	Output	Output	Output
L	-	Disabled	Disabled	Input	Input	Output	Input		
CLS	I	Built-in oscillator circuit enable / disable select pin – CLS = "H": enable – CLS = "L": disable (external display clock input to CL pin)							
CL	I/O	Display clock input / output pin When the S6B0717 is used in master / slave mode (multi-chip), the CL pins must be connected each other.							
M	I/O	LCD AC signal input / output pin When the S6B0717 is used in master/slave mode (multi-chip), the M pins must be connected each other. – MS = "H": output – MS = "L": input							
FRS	O	Static driver segment output pin This pin is used together with the M pin.							
DISP	I/O	LCD display blanking control input/output When S6B0717 is used in master/slave mode (multi-chip), the DISP pins must be connected each other. – MS = "H": output – MS = "L": input							
INTRS	I	Internal resistor select pin This pin selects the resistors for adjusting V <sub>0</sub> voltage level. – INTRS = "H": use the internal resistors – INTRS = "L": use the external resistors V <sub>0</sub> voltage is controlled by VR pin and external resistive divider.							
HPMB	I	Power control pin of the power supply circuit for LCD driver – HPMB = "L": high power mode – HPMB = "H": normal mode This pin is valid in master mode							
TEMPS	I	Test pin This pin is fixed to High or Low.							

**Table 6. System Control Pins Description (Continued)**

Name	I/O	Description
DUTY	I	The LCD driver duty ratio select pin – DUTY = "L": 1/34 – DUTY = "H": 1/55

NOTE: DUMMY – These pins should be open (floated).

## MICROPROCESSOR INTERFACE

Table 7. Microprocessor Interface Pins Description

Name	I/O	Description						
RESETB	I	Reset input pin When RESETB is "L", initialization is executed.						
PS	I	Parallel / Serial data input select input						
		PS	Interface mode	Chip select	Data / instruction	Data	Read / Write	Serial clock
		H	Parallel	CS1B, CS2	RS	DB0 to DB7	E_RD RW_WR	-
		L	Serial	CS1B, CS2	RS	SID (DB7)	Write only	SCLK (DB6)
*NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L".								
C68	I	Microprocessor interface select input pin – C68 = "H": 6800-series MPU interface – C68 = "L": 8080-series MPU interface						
CS1B CS2	I	Chip select input pins Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB7 may be high impedance.						
RS	I	Register select input pin – RS = "H": DB0 to DB7 are display data – RS = "L": DB0 to DB7 are control data						
RW_WR	I	Read / Write execution control pin						
		C68	MPU type	RW_WR	Description			
		H	6800-series	RW	Read/Write control input pin – RW = "H": read – RW = "L": write			
		L	8080-series	/WR	Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WR signal.			

Table 8. Microprocessor Interface Pins Description (Continued)

Name	I/O	Description			
E_RD	I	Read / Write execution control pin			
		C68	MPU type	E_RD	Description
		H	6800-series	E	Read/Write control input pin – RW = "H": When E is "H", DB0 to DB7 are in an output status. – RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.
		L	8080-series	/RD	Read enable clock input pin When /RD is "L", DB0 to DB7 are in an output status.
DB0 to DB7	I/O	8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L"); – DB0 to DB5: high impedance – DB6: serial input clock (SCLK) – DB7: serial input data (SID) When chip select is not active, DB0 to DB7 may be high impedance.			

## LCD DRIVER OUTPUTS

Table 9. LCD Driver Outputs Pins Description

Name	I/O	Description			
SEG0 to SEG99	O	LCD segment driver outputs The display data and the M signal control the output voltage of segment driver.			
		Display data	M	Segment driver output voltage	
				Normal display	Reverse display
		H	H	V0	V2
		H	L	VSS	V3
		L	H	V2	V0
		L	L	V3	VSS
		Power save mode		VSS	VSS
COM0 to COM53	O	LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver.			
		Scan data	M	Common driver output voltage	
		H	H	VSS	
		H	L	V0	
		L	H	V1	
		L	L	V4	
		Power save mode		VSS	
COMS	O	Common output for the icons The output signals of two pins are same. When not used, these pins should be left open. In multi-chip (master / slave) mode, all COMS pins on both master and slave units are the same signal.			



## FUNCTIONAL DESCRIPTION

### MICROPROCESSOR INTERFACE

#### Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0717 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E\_RD, and RW\_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

#### Parallel / Serial Interface

S6B0717 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 10.

**Table 10. Parallel / Serial Interface Mode**

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*x	Serial-mode

\*x: Don't care

#### Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in Parallel Interface and the type of MPU is selected by C68 as shown in table 11. The type of data transfer is determined by signals at RS, E\_RD and RW\_WR as shown in table 12.

**Table 11. Microprocessor Selection for Parallel Interface**

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

**Table 12. Parallel Data Transfer**

Common	6800-series		8080-series		Description
	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
RS					
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

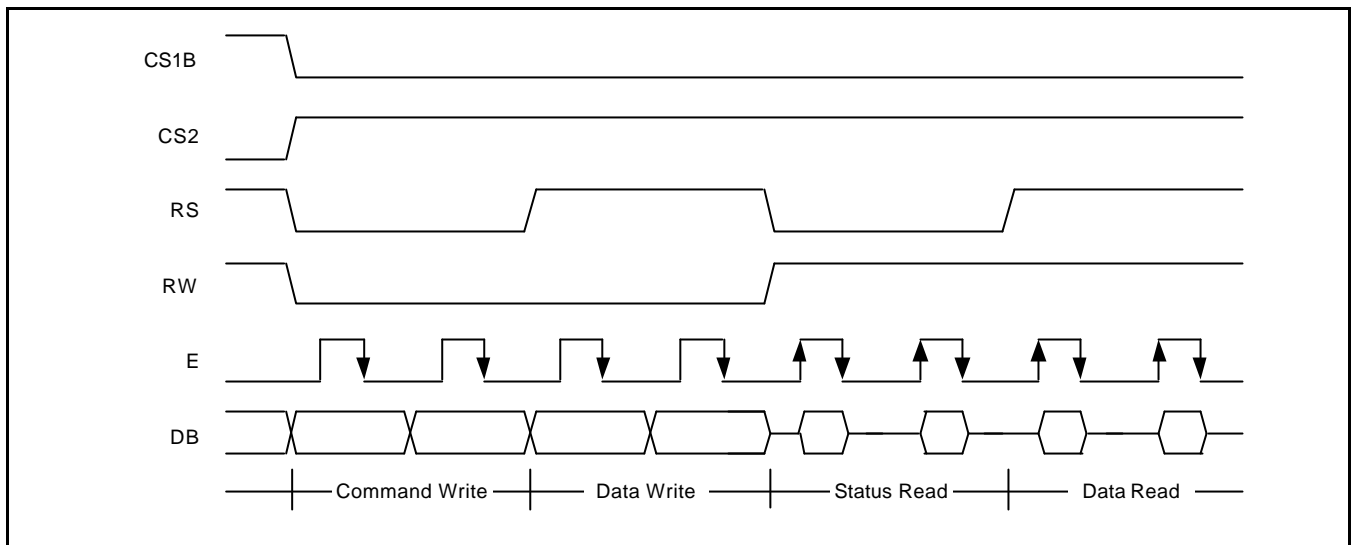


Figure 5. 6800-Series MPU Interface protocol (PS="H", MI="H")

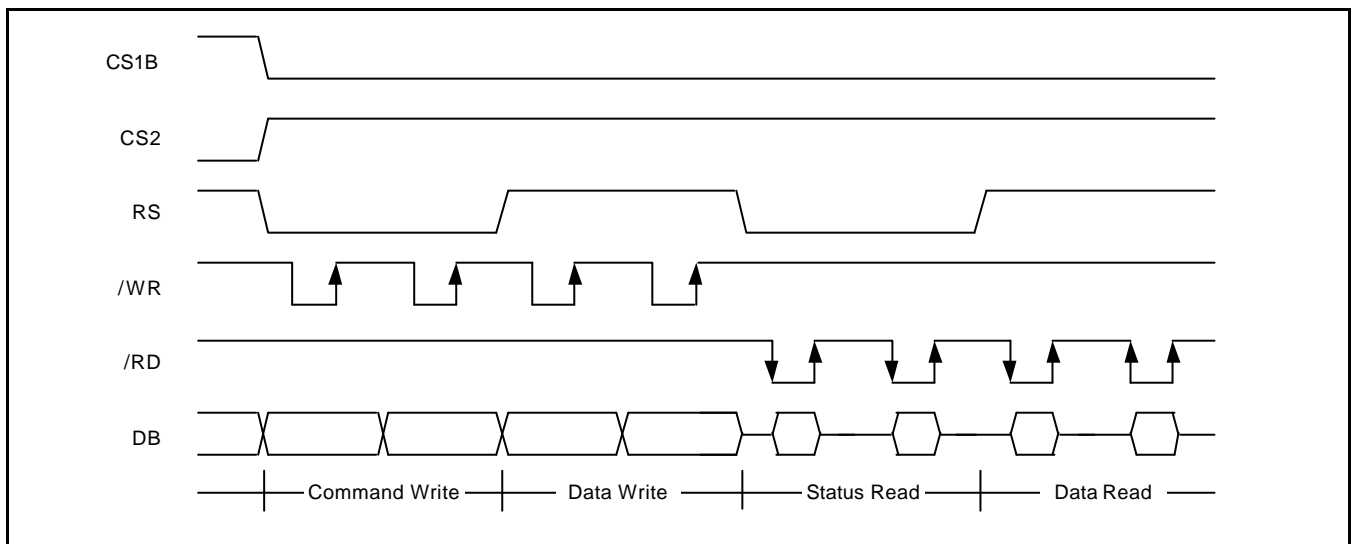


Figure 6. 8080-Series MPU Interface Protocol (PS="H", MI="L")

**Serial Interface (PS = "L")**

When the S6B0717 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

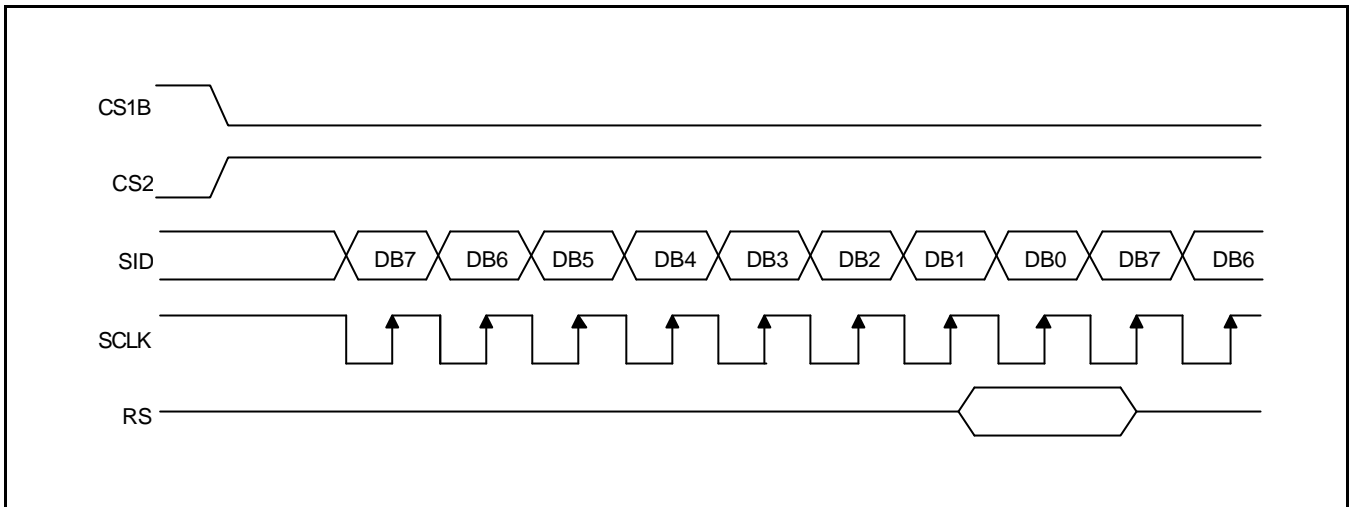


Figure 7. Serial Interface Timing

**Busy Flag**

The Busy Flag indicates whether the S6B0717 is operating or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

**Data Transfer**

The S6B0717 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

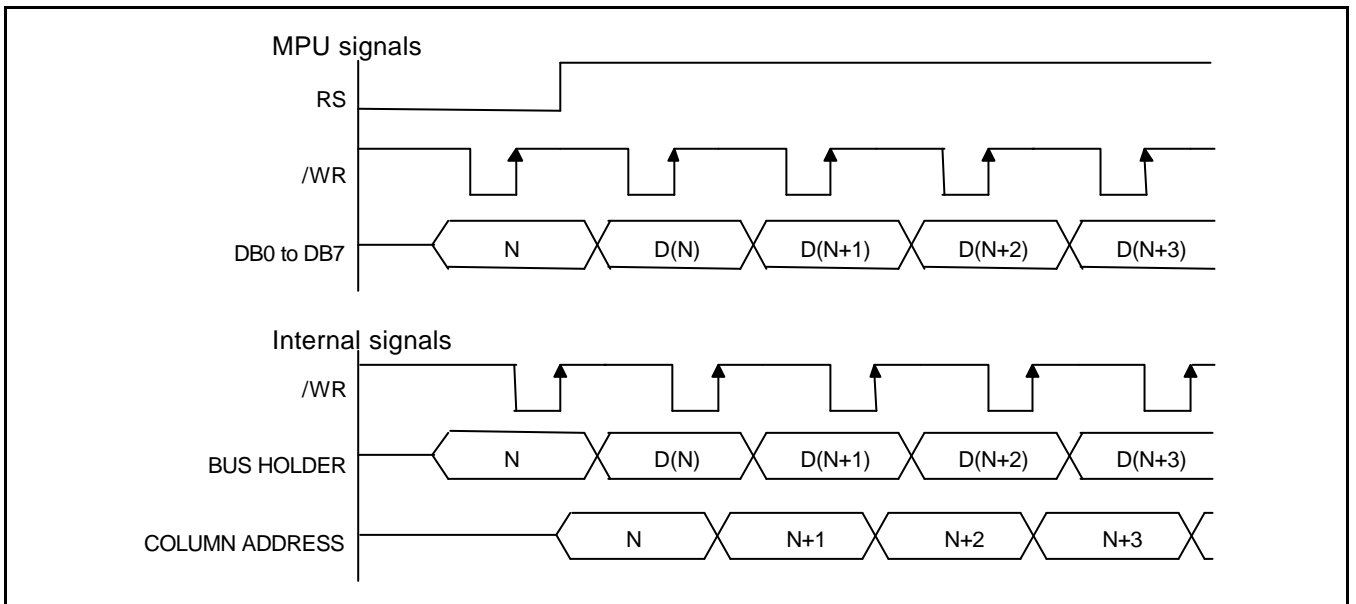


Figure 8. Write Timing



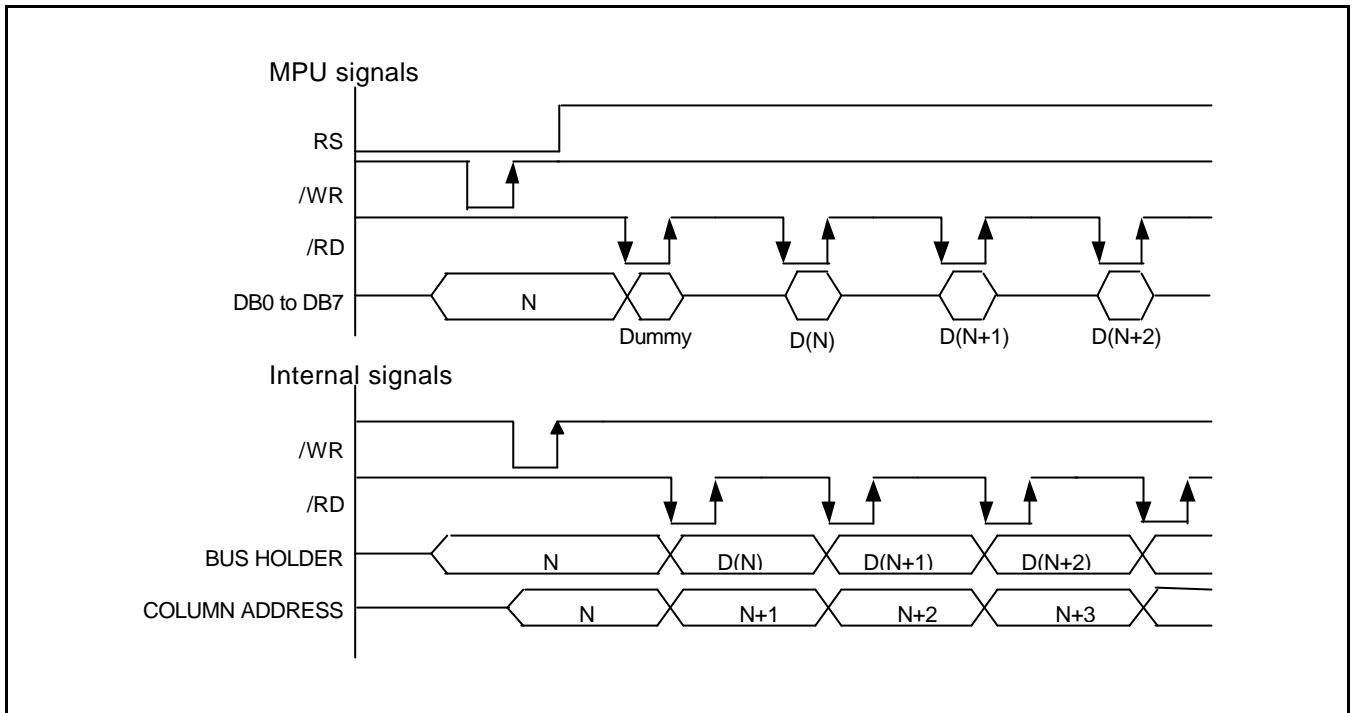


Figure 9. Read Timing

## DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 100-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 10. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

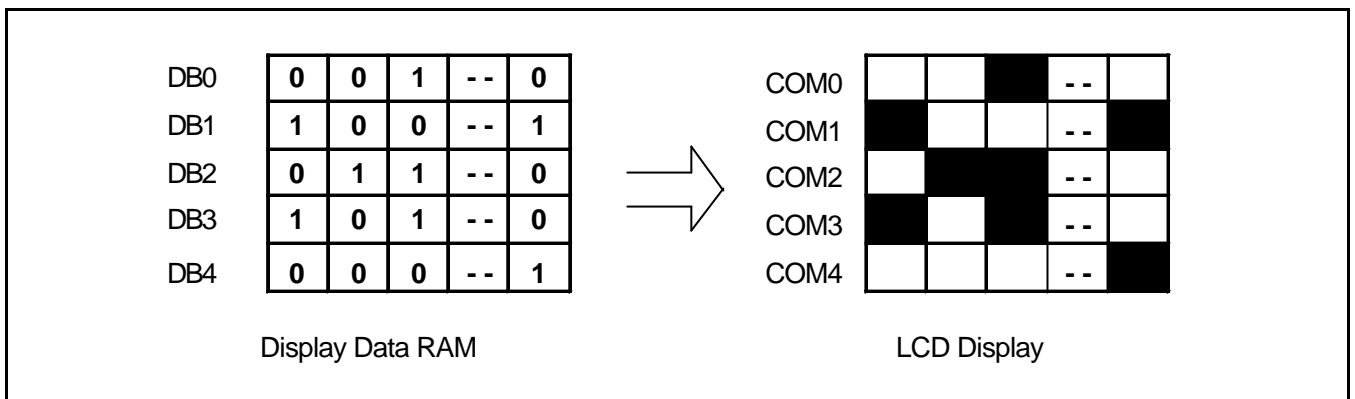


Figure 10. RAM-to-LCD Data Transfer

### Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 12. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

### Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 12. It incorporates 6-bit Line Address register changed by only the Initial Display Line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 100-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

### Column Address Circuit

Column Address circuit has a 7-bit preset counter that provides column address to the Display Data RAM as shown in figure 12. When set Column Address MSB / LSB instruction is issued, 7-bit [Y6:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 63H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 11.

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	... ..	SEG 96	SEG 97	SEG 98	SEG 99
Column address [Y6:Y0]	00H	01H	02H	03H	... ..	60H	61H	62H	63H
Display data	1	0	1	0		1	1	0	0
LCD panel display ( ADC = 0 )					... ..				
LCD panel display ( ADC = 1 )					... ..				

Figure 11. The Relationship between the Column Address and the Segment Outputs

### Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

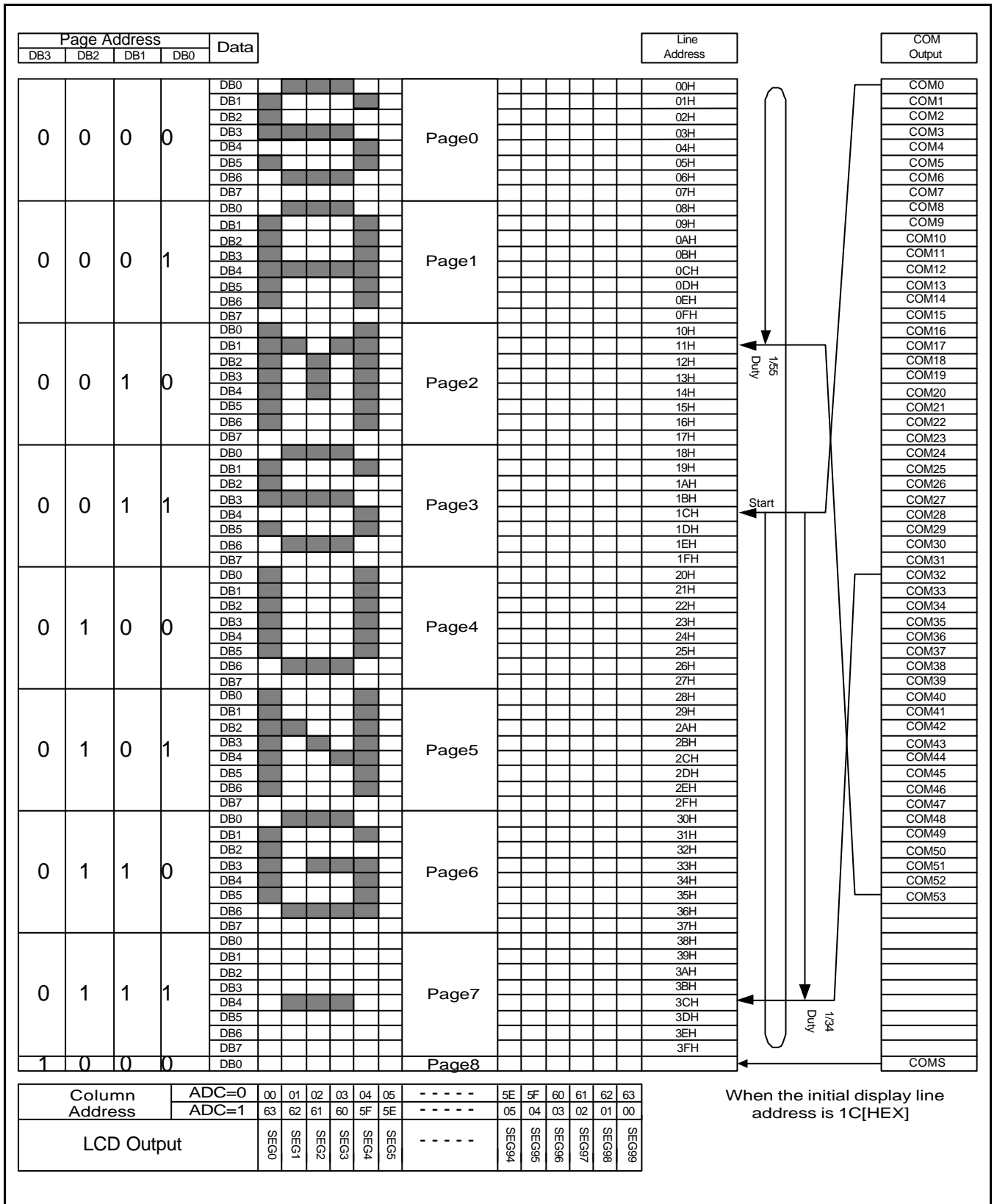


Figure 12. Display Data RAM Map

## LCD DISPLAY CIRCUITS

### Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of VDD. This oscillator signal is used in the voltage converter and display timing generation circuit.

\* Test Condition: Temperature (25°C & 85°C)

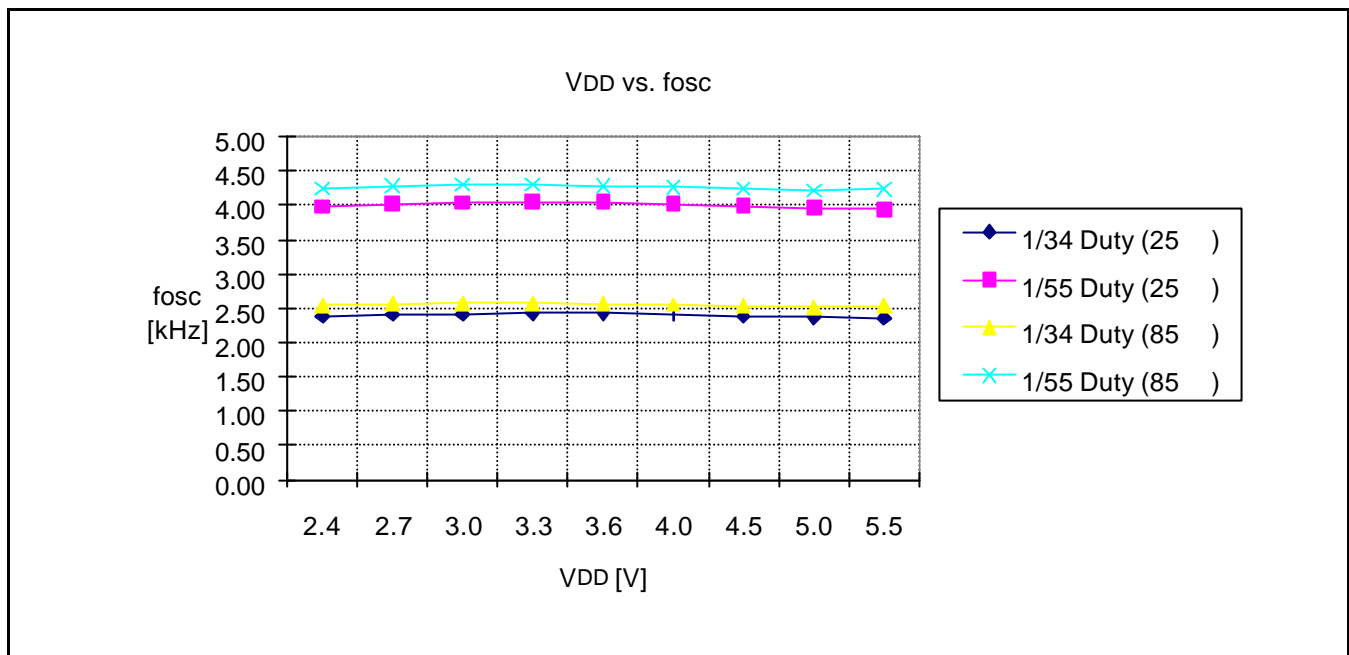


Figure 13. VDD vs. fosc

### Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 14.

In a multiple chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 13 shows the M, CL, and DISP status.

Table 13. Master and Slave Timing Signal Status

Operation mode	Oscillator	M	CL	DISP
Master (MS = 1)	ON (CLS = 1, internal clock used)	Output	Output	Output
	OFF (CLS = 0, external clock used)	Output	Input	Output
Slave (MS = 0)	-	Input	Input	Input



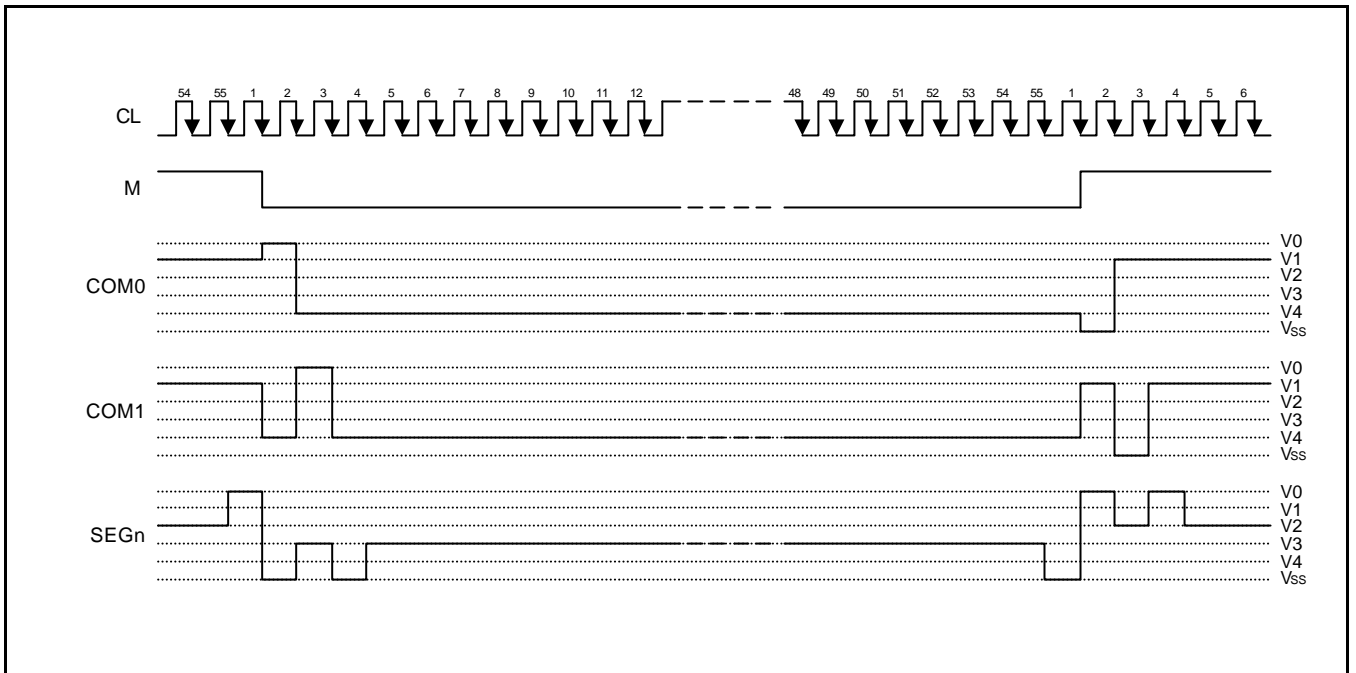


Figure 14. 2-frame AC Driving Waveform (Duty Ratio = 1/55)

**Common Output Control Circuit**

This circuit controls the relationship between the number of common output and specified duty ratio. SHL select Instruction specifies the scanning direction of the common output pins.

Table 14. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins			
		COM[0:16]	COM[17:37]	COM[38:53]	COMS
1/34	0	COM[0:16]	*NC	COM[17:32]	COMS
	1	COM[32:16]	*NC	COM[15:0]	
1/55	0	COM[0:53]			COMS
	1	COM[53:0]			

\*NC: No Connection

### LCD DRIVER CIRCUIT

This driver circuit is configured by 56-channel (including 2 COMS channel) common driver and 100-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

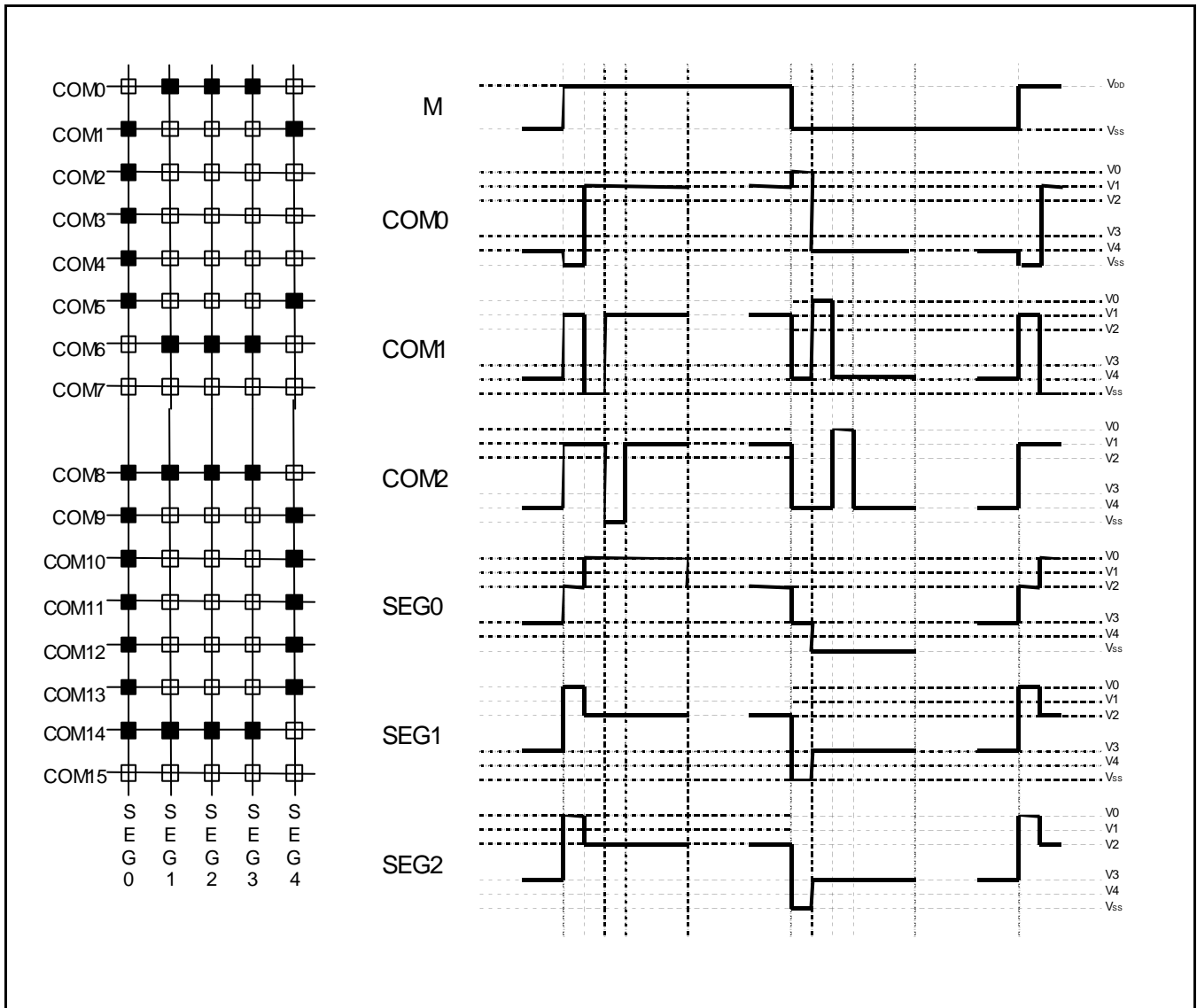


Figure 15. Segment and Common Timing

## POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 13 shows the referenced combinations in using Power Supply circuits.

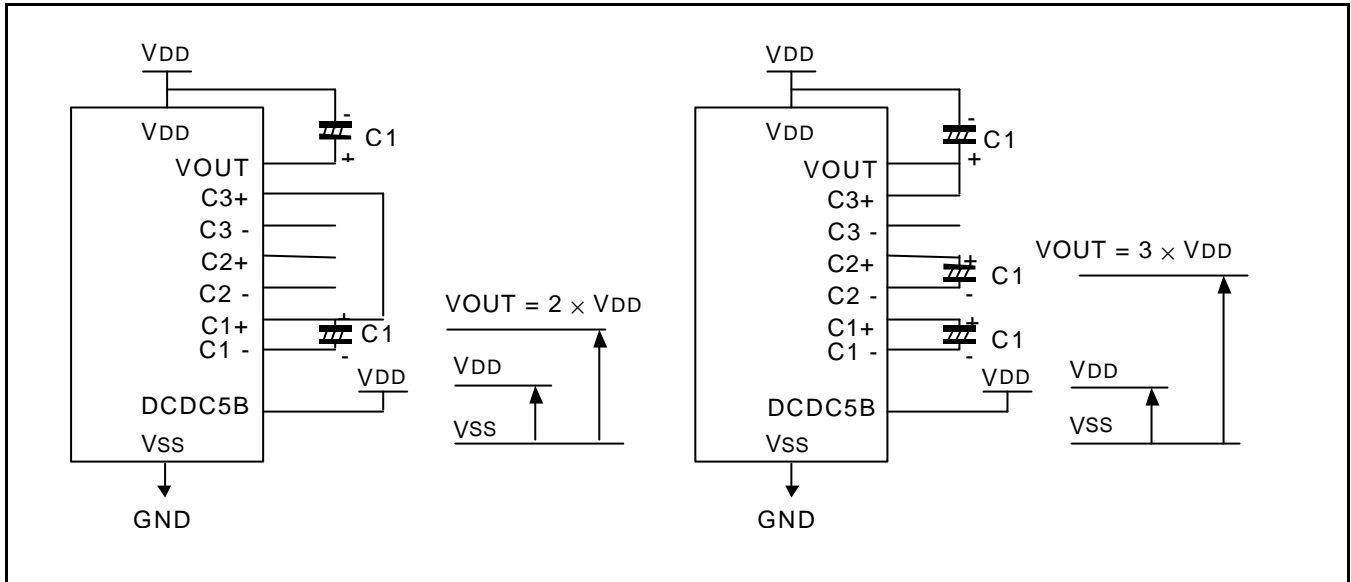
**Table 13. Recommended Power Supply Combinations**

User Setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

**Voltage Converter Circuits**

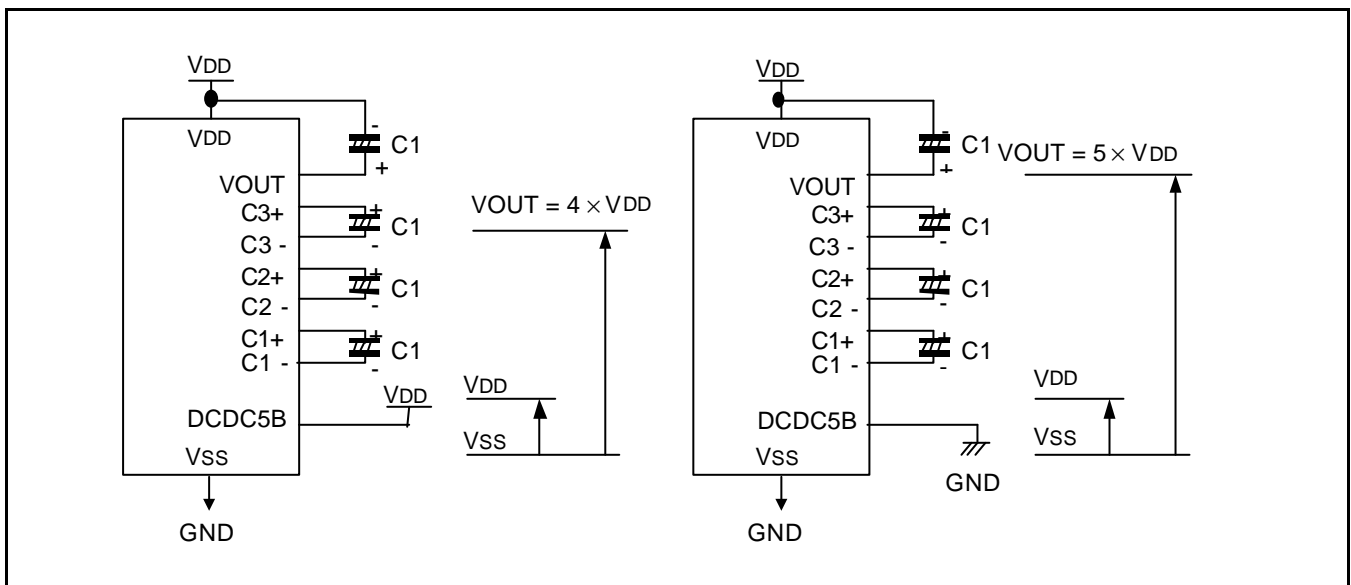
These circuits boost up the electric potential between VDD and VSS to 2, 3, 4 or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7  $\mu$ f]



**Figure 16. Two Times Boosting Circuit**

**Figure 17. Three Times Boosting Circuit**



**Figure 18. Four Times Boosting Circuit**

**Figure 19. Five Times Boosting Circuit**

**Voltage Regulator Circuits**

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 20, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta = 25°C is shown in table 14-1.

$$V0 = \left( 1 + \frac{Rb}{Ra} \right) \times VEV \text{ [V] ----- (Eq. 1)}$$

$$VEV = \left( 1 - \frac{(63 - \alpha)}{162} \right) \times VREF \text{ [V] ----- (Eq. 2)}$$

**Table 14-1. VREF voltage at Ta = 25°C**

REF	VREF [V]
H (internal)	2.1
L (external)	VEXT

**Table 14-2. Reference Voltage Parameter (a)**

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

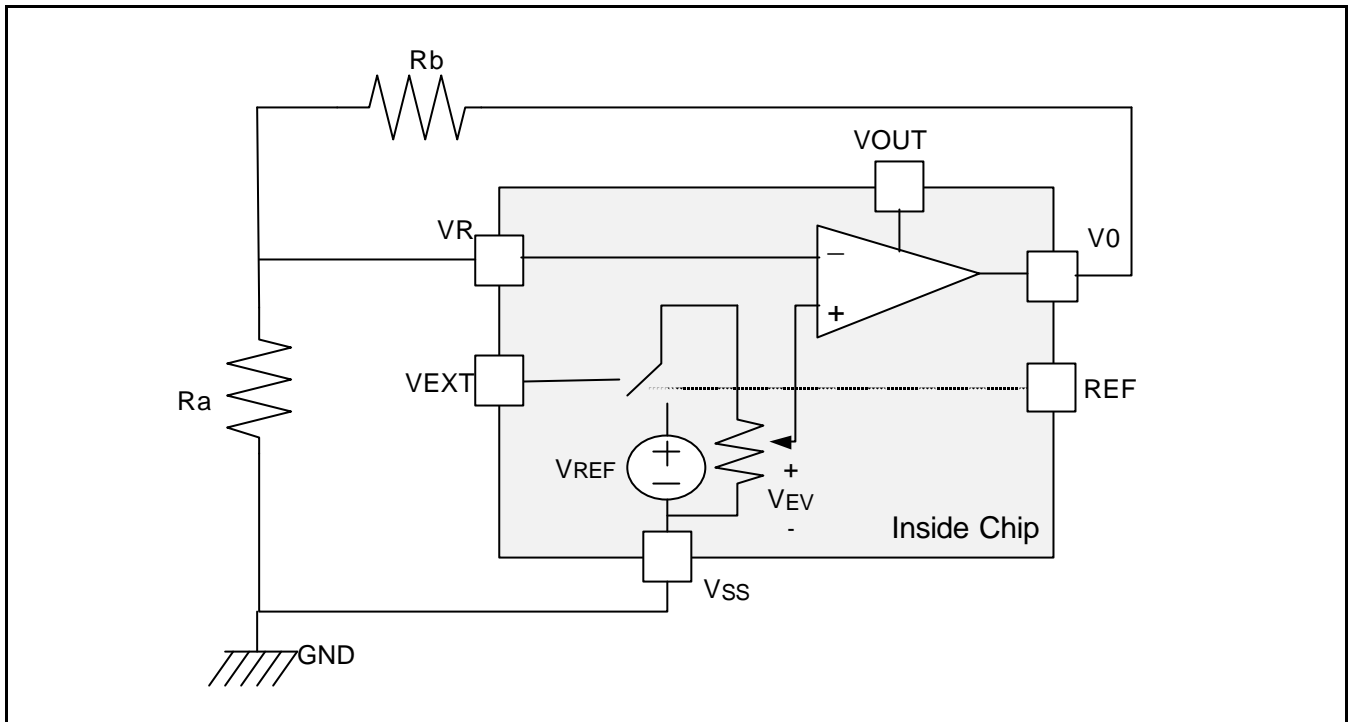


Figure 20. Internal Voltage Regulator Circuit

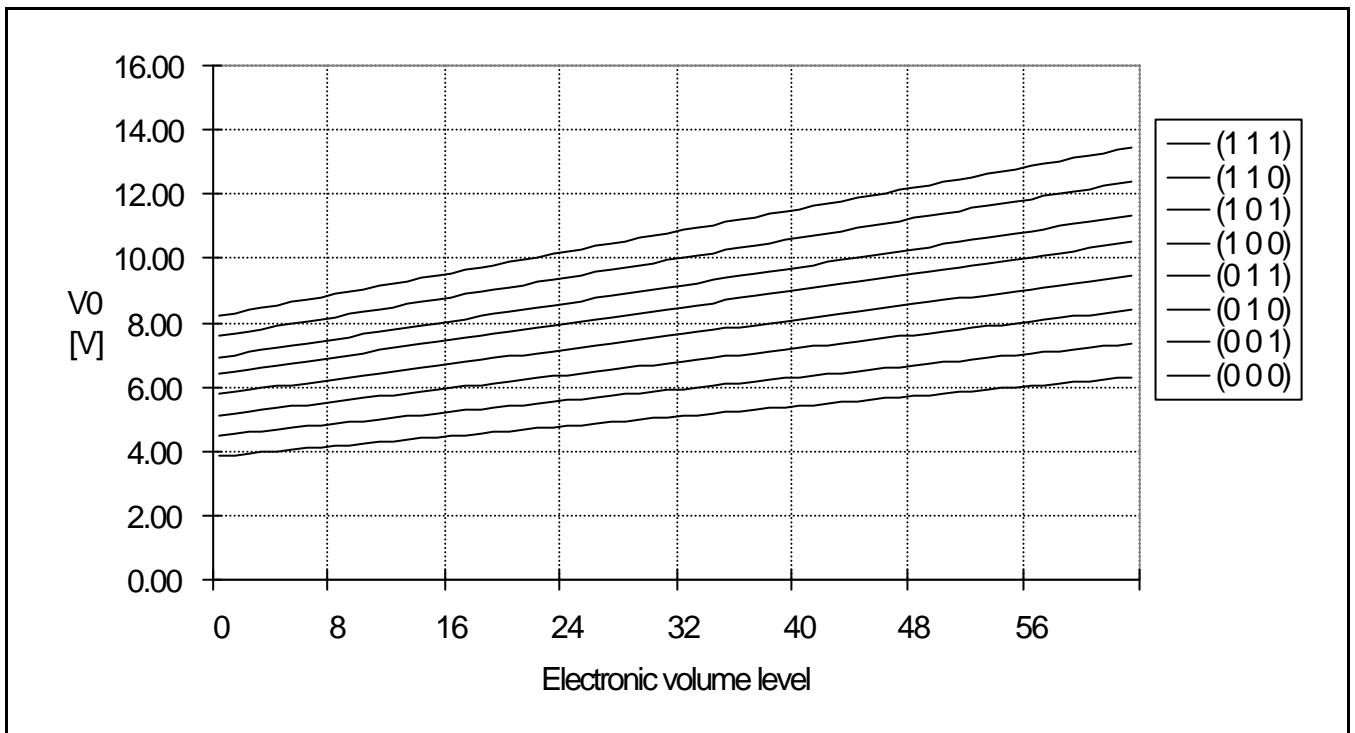
**In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")**

When INTRS pin is "H", resistor Ra is connected internally between VR pin and V<sub>SS</sub>, and Rb is connected between V<sub>0</sub> and VR. We determine V<sub>0</sub> by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

**Table 15. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)**

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb / Ra)	3.0	3.5	4.0	4.5	5.0	5.4	5.9	6.4

The following figure shows V<sub>0</sub> voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.



**Figure 21. Electronic Volume Level**

**In Case of Using External Resistors, Ra and Rb (INTRS = "L")**

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and Vss, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage,  $V_0 = 10V$
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra,  $R_b = 1 \mu A$

From Eq. 1

$$10 = \left( 1 + \frac{R_b}{R_a} \right) \times V_{EV} \quad [V] \quad \text{----- (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left( 1 - \frac{(63 - 32)}{162} \right) \times 2.1 = 1.698 \quad [V] \quad \text{----- (Eq. 4)}$$

From requirement 3.

$$\frac{10}{R_a + R_b} = 1 \quad [\mu A] \quad \text{----- (Eq. 5)}$$

From equations Eq. 3, 4 and 5

$$R_a = 1.69 \quad [M\Omega]$$

$$R_b = 8.31 \quad [M\Omega]$$

The following table shows the range of  $V_0$  depending on the above requirements.

**Table 16.  $V_0$  depending on Electronic Volume Level**

	Electronic volume level				
	0	.....	32	.....	63
$V_0$	7.59	.....	10.00	.....	12.43



### Voltage Follower Circuits

VLCD voltage ( $V_0$ ) is resistively divided into four voltage levels ( $V_1, V_2, V_3, V_4$ ), and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between  $V_1$  to  $V_4$  level and each duty ratio.

**Table 17. The Relationship between  $V_1$  to  $V_4$  level and Duty Ratio**

Duty ratio	Duty	LCD bias	$V_1$	$V_2$	$V_3$	$V_4$
1/55	H	1/8	$(7/8) \times V_0$	$(6/8) \times V_0$	$(2/8) \times V_0$	$(1/8) \times V_0$
		1/6	$(5/6) \times V_0$	$(4/6) \times V_0$	$(2/6) \times V_0$	$(1/6) \times V_0$
1/34	L	1/6	$(5/6) \times V_0$	$(4/6) \times V_0$	$(2/6) \times V_0$	$(1/6) \times V_0$
		1/5	$(4/5) \times V_0$	$(3/5) \times V_0$	$(2/5) \times V_0$	$(1/5) \times V_0$

REFERECE CIRCUIT EXAMPLES

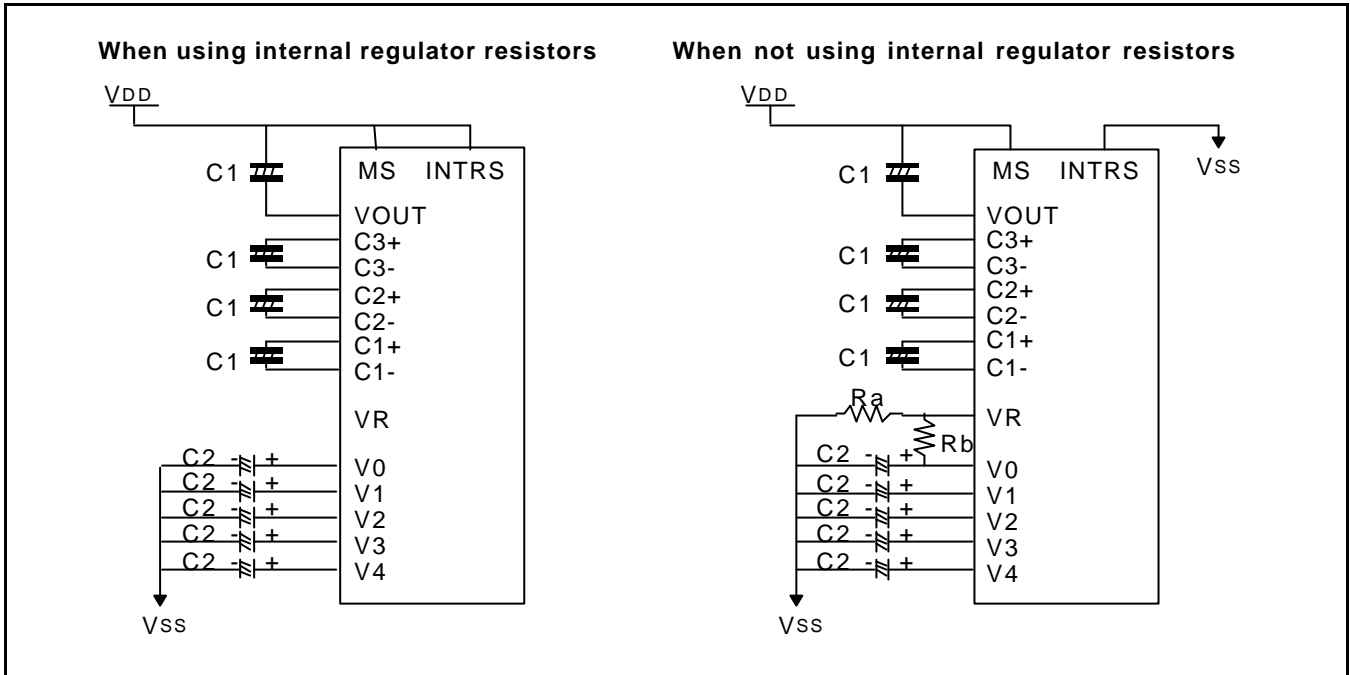


Figure 22. When Using all LCD Power Circuits (4-time V/C: ON, V/R: ON, V/F: ON)

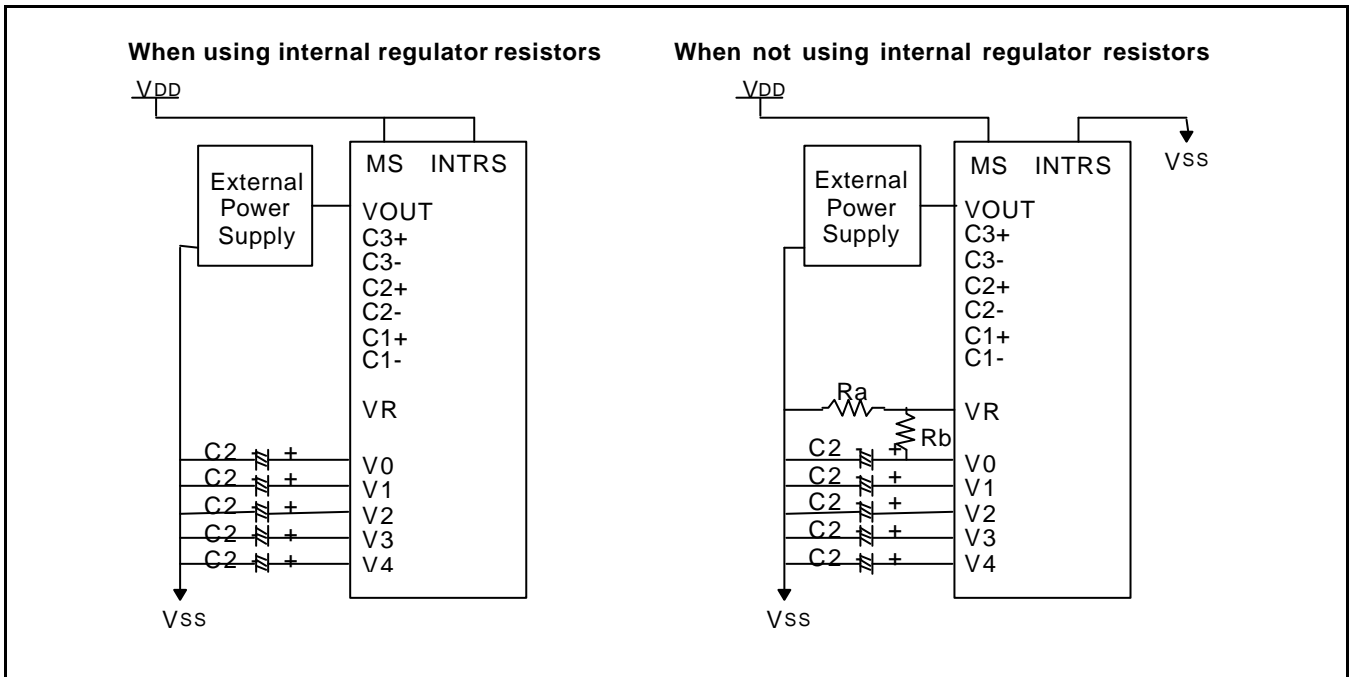


Figure 23. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

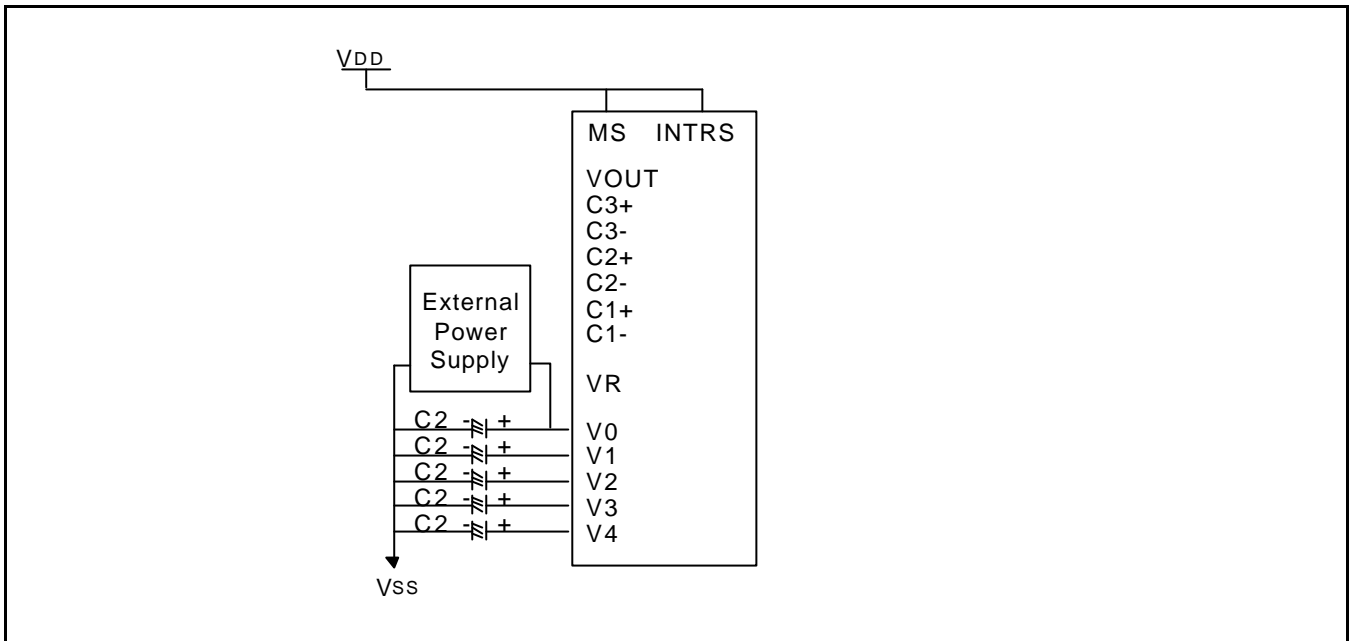


Figure 24. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

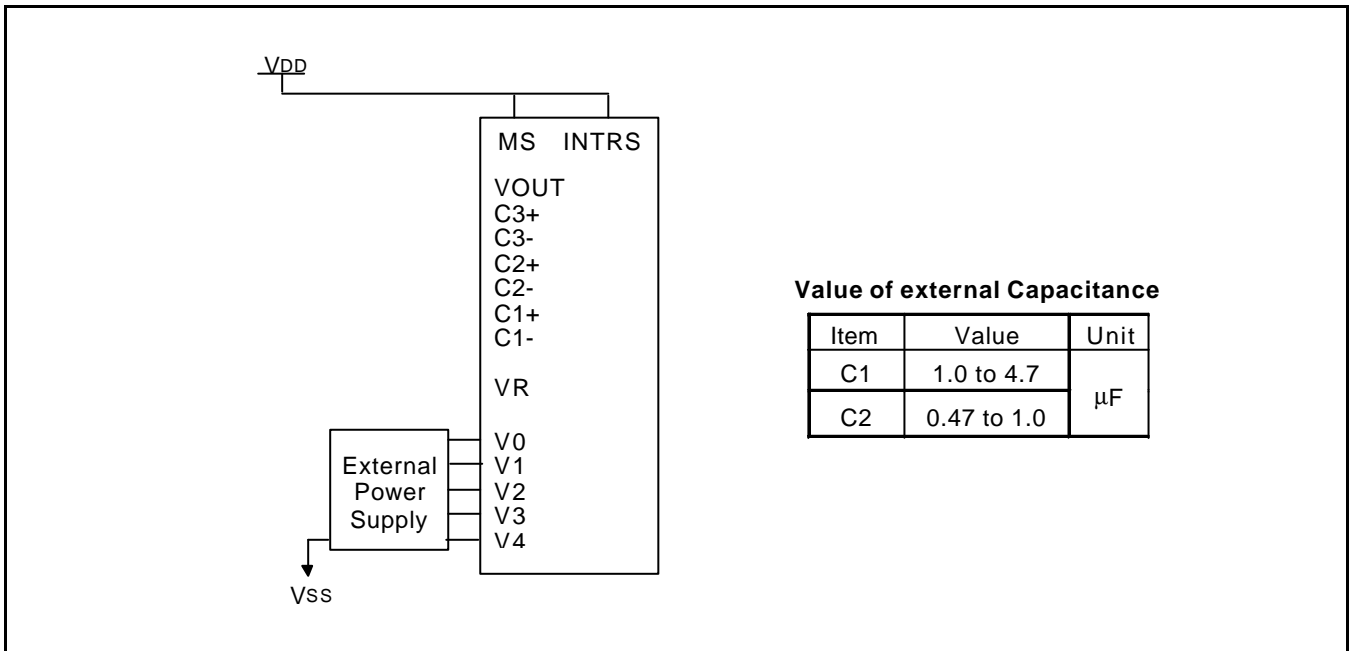


Figure 25. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

## RESET CIRCUIT

Setting RESETB to "L" or Re set instruction can initialize internal function.  
When RESETB becomes "L", following procedure is occurred.

Display ON / OFF: OFF  
Entire display ON / OFF: OFF (normal)  
ADC select: OFF (normal)  
Reverse display ON / OFF: OFF (normal)  
Power control register (VC, VR, VF) = (0, 0, 0)  
LCD bias ratio: 1/8(1/55 duty), 1/6(1/34 duty)  
Read-modify-write: OFF  
SHL select: OFF (normal)  
Static indicator mode: OFF  
Static indicator register: (S1, S0) = (0, 0)  
Display start line: 0 (first)  
Column address: 0  
Page address: 0  
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)  
Reference voltage set: OFF  
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF  
Static indicator mode: OFF  
Static indicator register: (S1, S0) = (0, 0)  
SHL select: 0  
Display start line: 0 (first)  
Column address: 0  
Page address: 0  
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)  
Reference voltage set: OFF  
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

While RESETB is "L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

## INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG0→SEG99) When ADC = 1: reverse direction (SEG99→SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM0→COM53) When SHL = 1: reverse direction (COM53→COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON
Test instruction	0	0	1	1	1	1	×	×	×	×	<b><u>Don't use this instruction.</u></b>

**Read Display Data**

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

**Write Display Data**

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

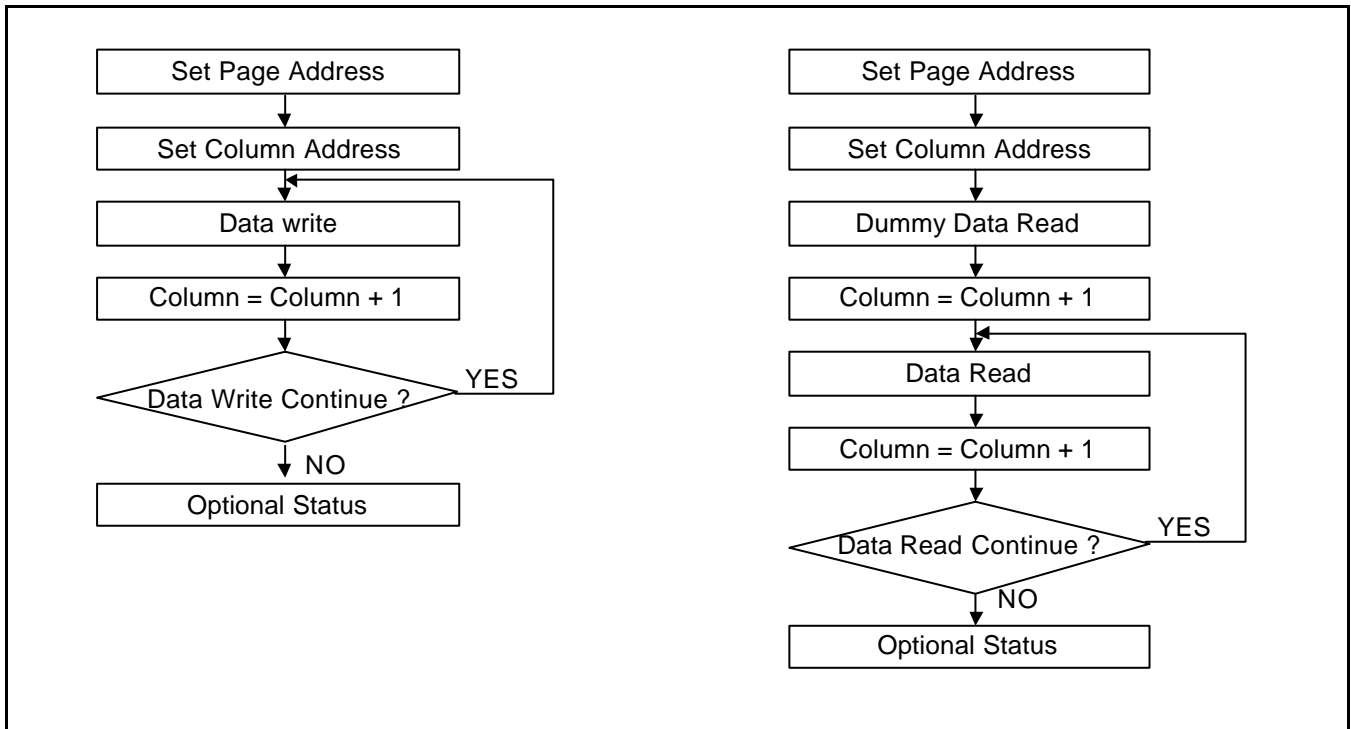


Figure 26. Sequence for Writing Display Data

Figure 27. Sequence for Reading Display Data

**Read Status**

Indicates the internal status of the S6B0717

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON / OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG99 → SEG0), 1: normal direction (SEG0 → SEG99)
ON / OFF	Indicates display ON / OFF status 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal 0: chip is active, 1: chip is being reset

**Display ON / OFF**

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

**Initial Display Line**

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM0) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

### Reference Voltage Select

Consists of 2-byte instruction

The 1<sup>st</sup> instruction sets reference voltage mode, the 2<sup>nd</sup> one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

#### The 1<sup>st</sup> Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

#### The 2<sup>nd</sup> Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

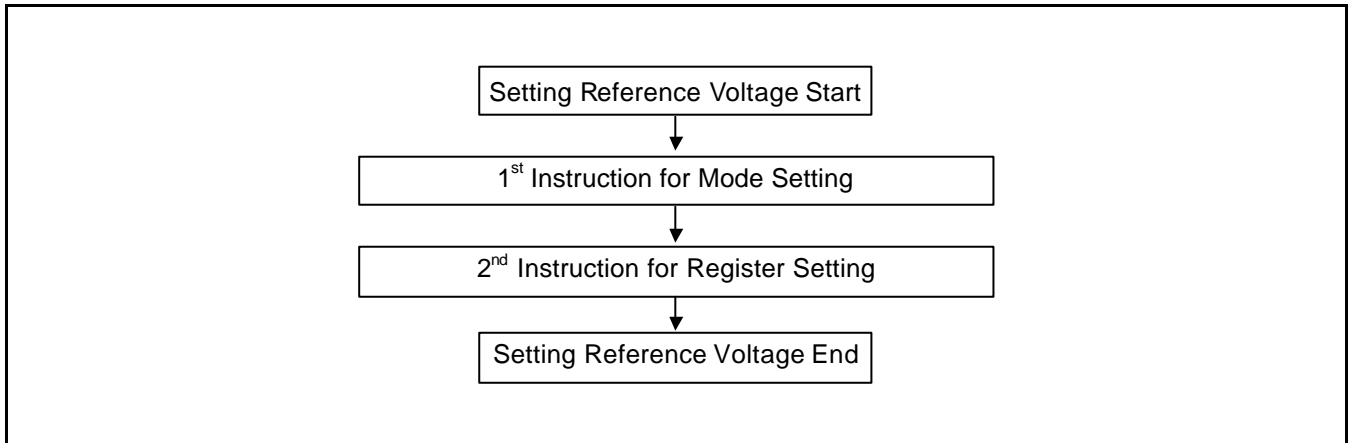


Figure 28. Sequence for Setting the Reference Voltage



**Set Page Address**

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

**Set Column Address**

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased.

**Set Column Address MSB**

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y6	Y5	Y4

**Set Column Address LSB**

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99

**ADC Select**

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG99)

ADC = 1: reverse direction (SEG99 → SEG0)

**Reverse Display ON / OFF**

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

**Entire Display ON / OFF**

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display

EON = 1: entire display ON

**Select LCD Bias**

Selects LCD bias ratio of the voltage required for driving the LCD

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY	LCD bias	
		Bias = 0	Bias = 1
1/55	1	1/8	1/6
1/34	0	1/6	1/5

**Set Modify-Read**

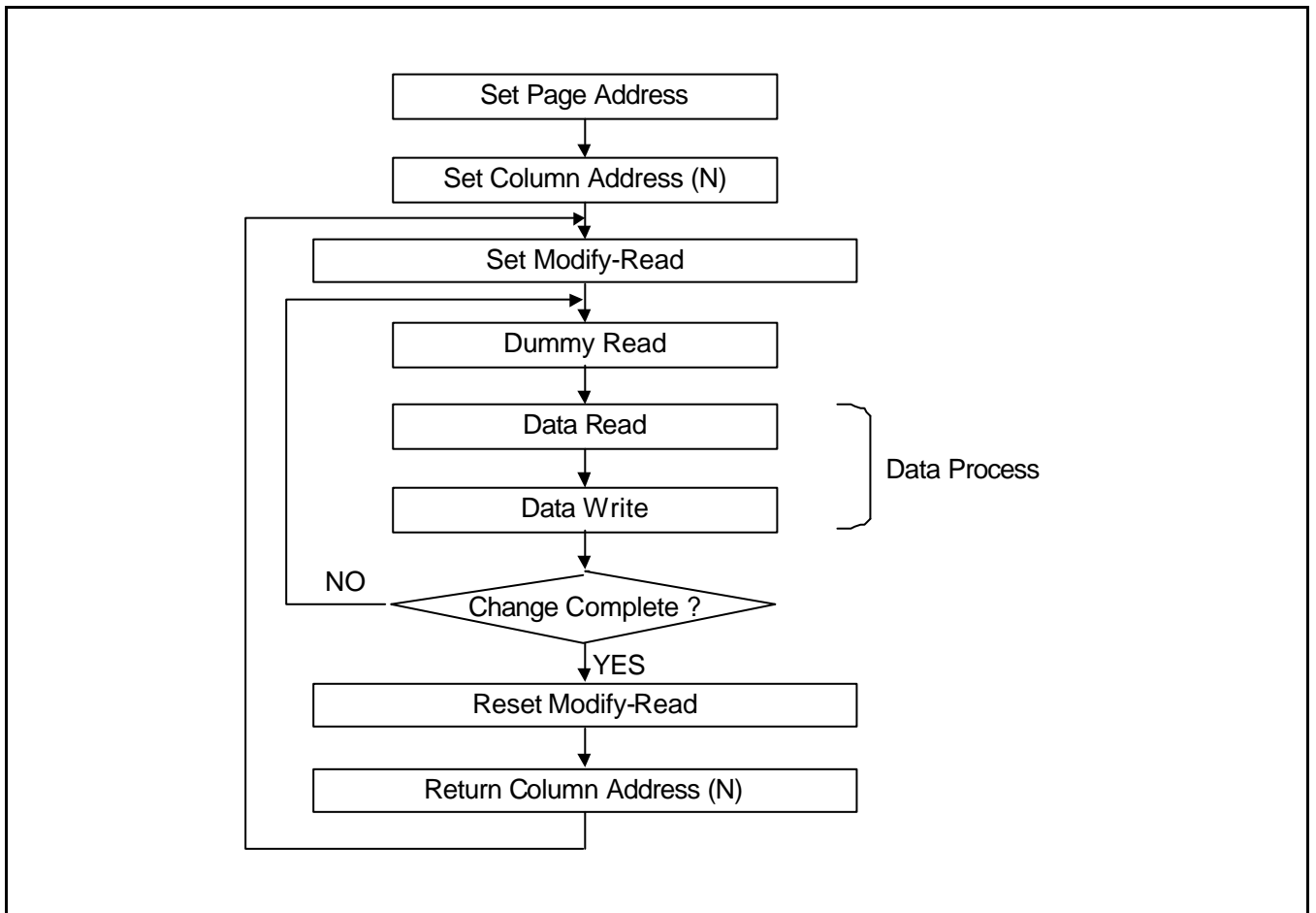
This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

**Reset Modify-Read**

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the Set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0



**Figure 29. Sequence for Cursor Display**

**Reset**

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

**SHL Select**

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don't care

SHL = 0: normal direction (COM0 → COM53)

SHL = 1: reverse direction (COM53 → COM0)

**Power Control**

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

### Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	$1 + (R_b / R_a)$
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.4
1	1	0	5.9
1	1	1	6.4

### Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator Mode) enables the second byte instruction (set Static Indicator Register) to be valid. The first byte sets the Static Indicator ON / OFF. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

#### The 1<sup>st</sup> Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF

SM = 1: static indicator ON

#### The 2<sup>nd</sup> Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking )
1	1	ON (always ON)

### Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B0717 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, Power Save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the display ON & entire display OFF instruction.

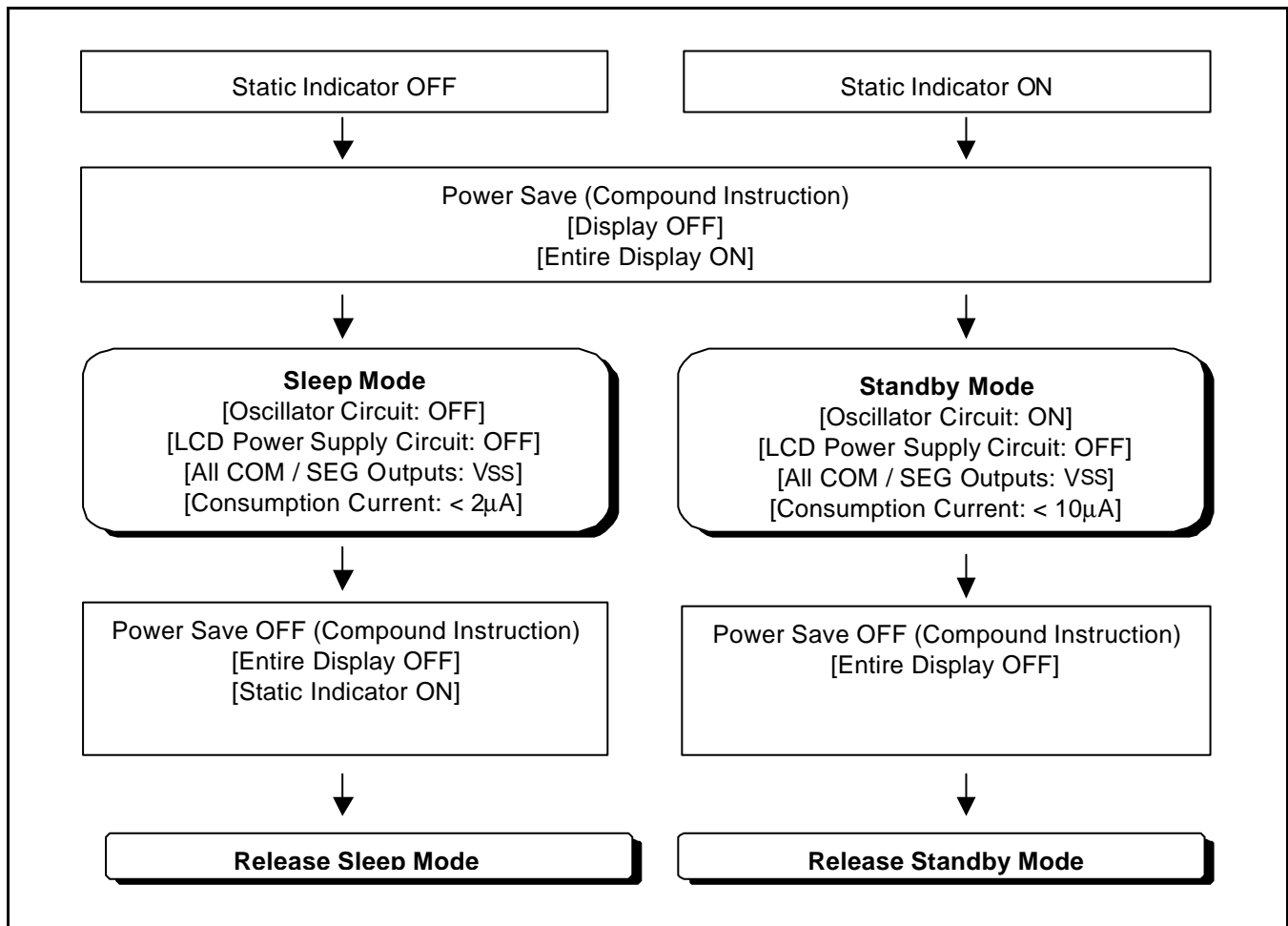


Figure 30. Power Save Routine

## Referential Instruction Setup Flow (1)

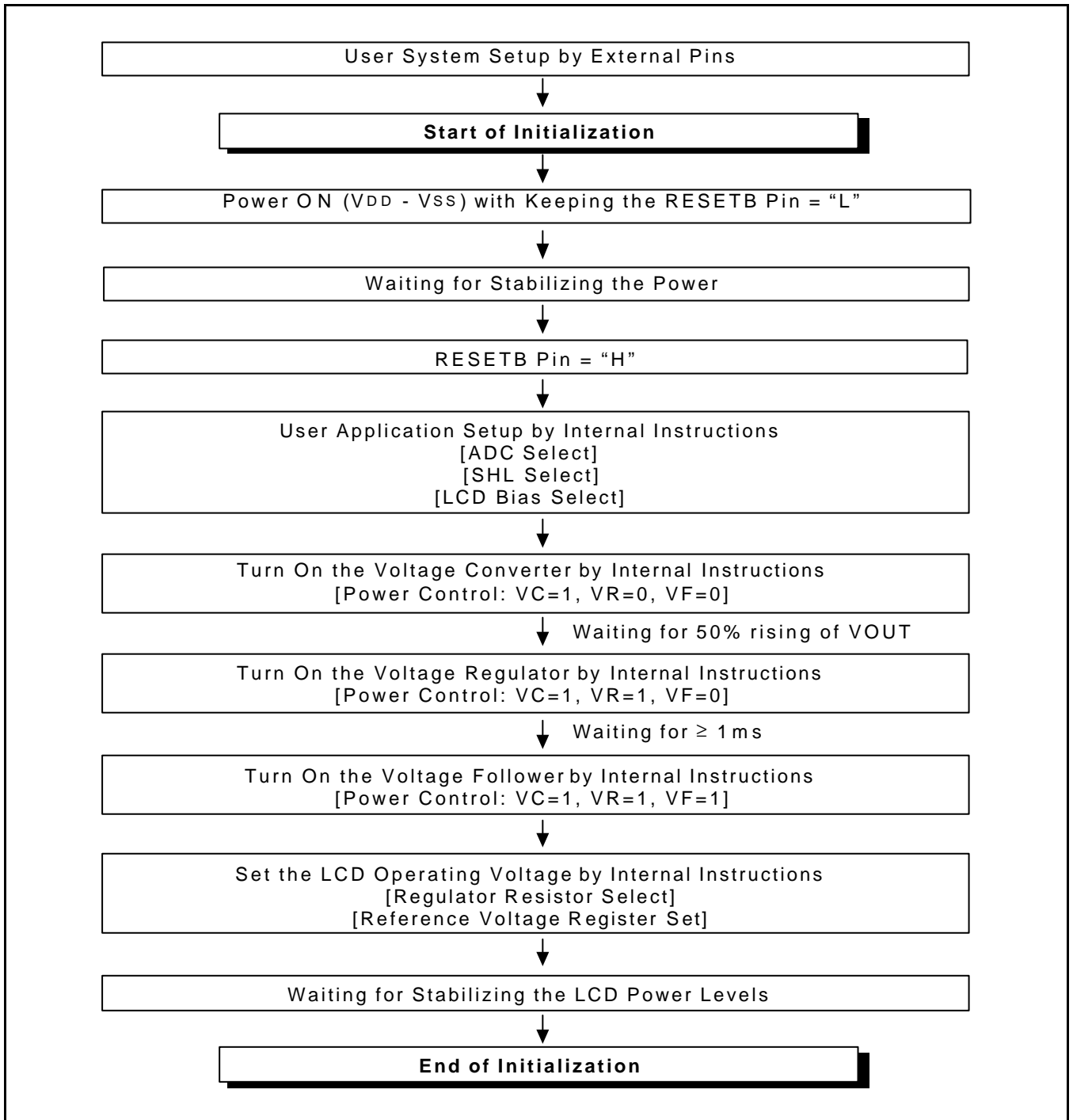


Figure 31. Initializing with the Built-in Power Supply Circuits

## Referential Instruction Setup Flow (2)

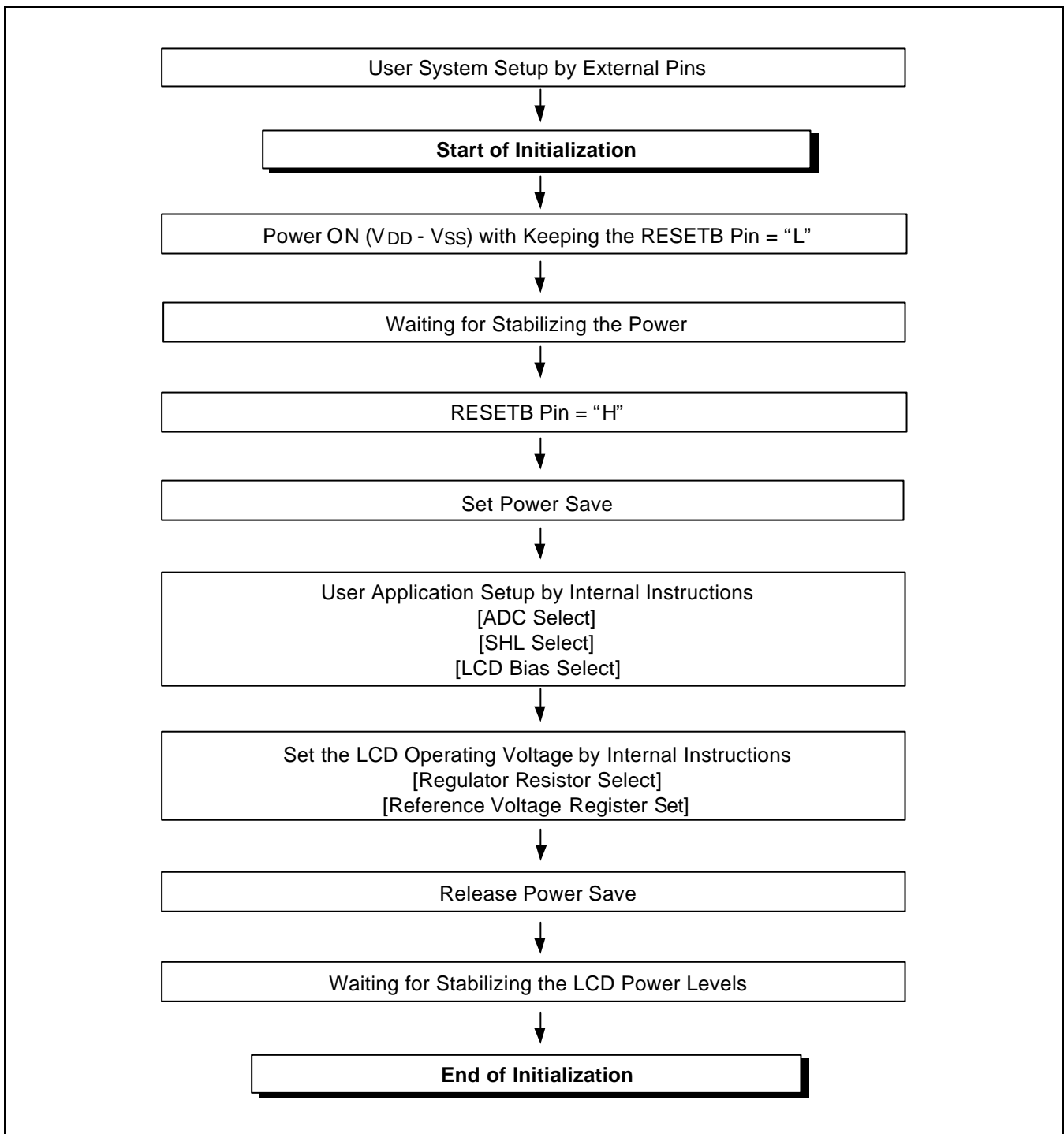


Figure 32. Initializing without the Built-in Power Supply Circuits



## Referential Instruction Setup Flow (3)

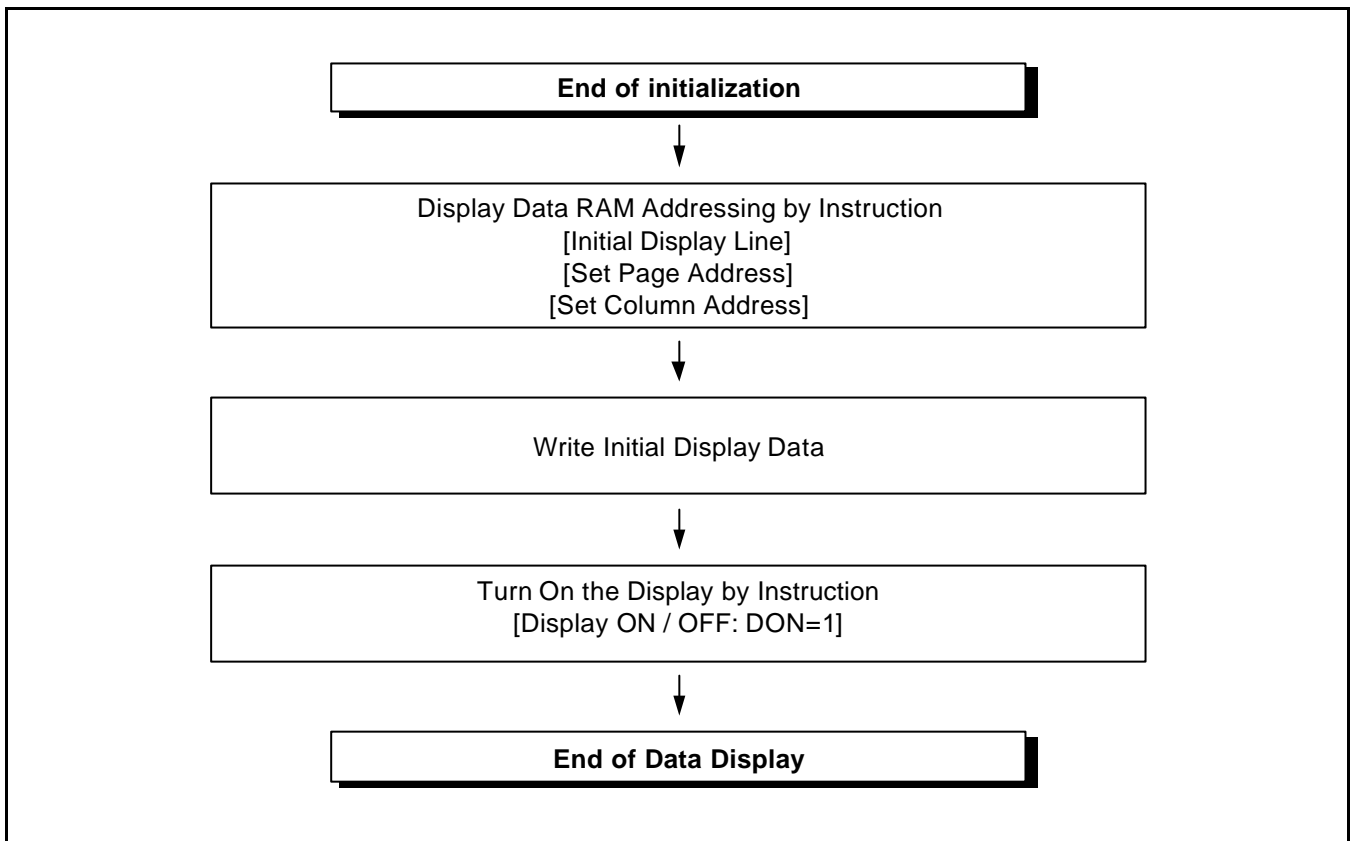


Figure 33. Data Displaying

## Referential Instruction Setup Flow (4)

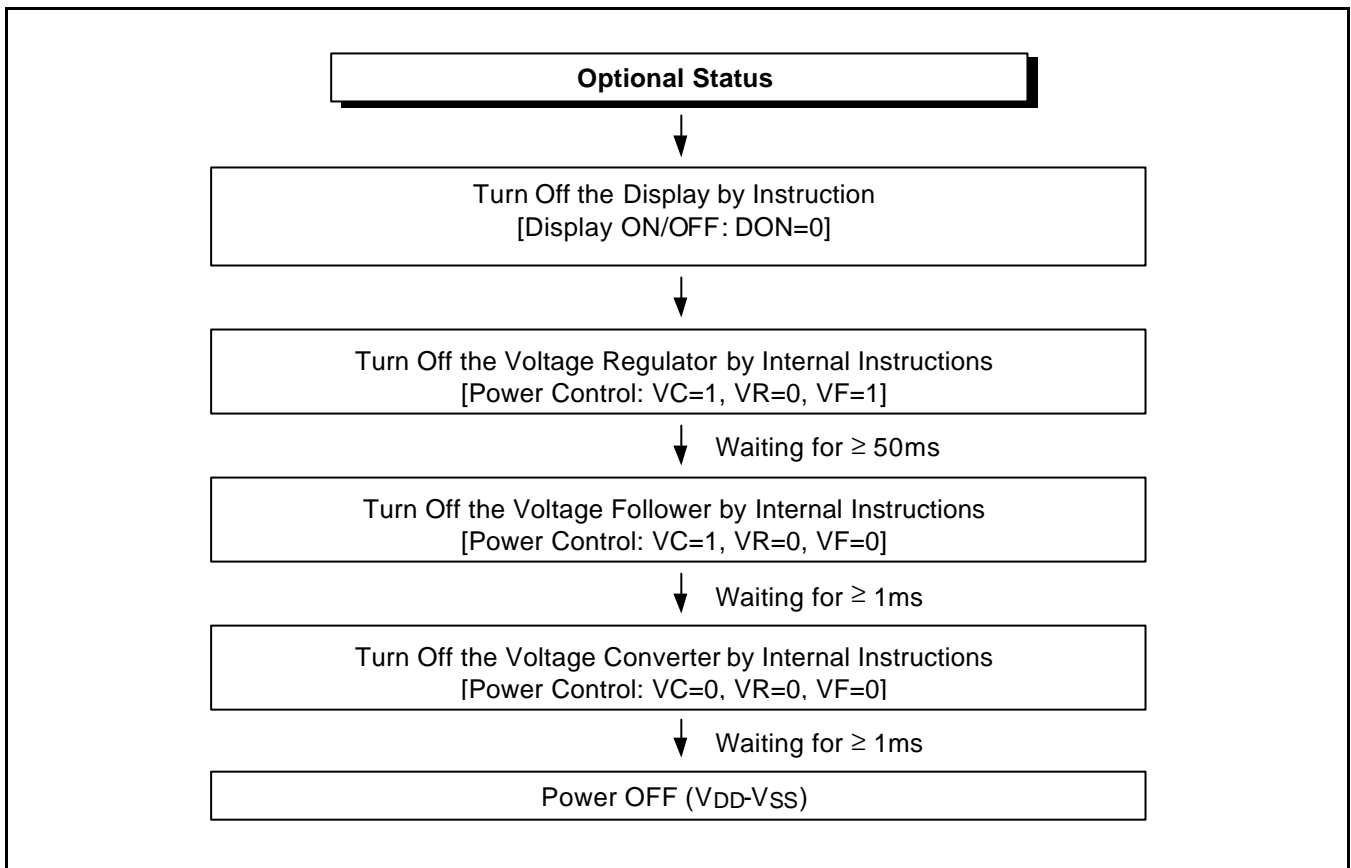


Figure 34. Power OFF

## SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD	-0.3 to +7.0	V
	VLCD	-0.3 to +17.0	V
Input voltage range	VIN	-0.3 to VDD +0.3	V
Operating temperature range	TOPR	-40 to +85	°C
Storage temperature range	TSTR	-55 to +125	°C

NOTES:

- VDD and VLCD are based on VSS = 0V.
- Voltages  $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$  must always be satisfied. (VLCD = V0 – VSS)
- If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.  
It is desirable to use this LSI under electrical characteristic conditions during general operation.  
Otherwise, this LSI may malfunction or reduced LSI reliability may result.

## DC CHARACTERISTICS

Table 20. DC Characteristics

(VSS = 0V, VDD = 2.4 to 5.5V, Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used	
Operating voltage (1)	VDD	Select by product code	2.4	-	3.6	V	VDD *1	
			2.4	-	5.5	V		
Operating voltage (2)	V0		4.0	-	15.0	V	V0, *2	
Input voltage	High	VIH	0.8VDD	-	VDD	V	*3	
	Low	VIL	VSS	-	0.2VDD			
Output voltage	High	VOH	IOH = -0.5mA	0.8VDD	-	VDD	V	*4
	Low	VOL	IOL = 0.5mA	VSS	-	0.2VDD		
Input leakage current	IIL	VDD = 3.0V VIN = VDD or VSS	- 1.0	-	+ 1.0	μA	*5	
Output leakage current	IOZ	VIN = VDD or VSS	- 3.0	-	+ 3.0	μA	*6	
LCD driver ON resistance	RON	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEgN COMn *7	
Oscillator frequency (1)	Internal	fOSC	VDD = 3.0V Ta = 25°C Duty ratio = 1/55	11.5	14	16.5	kHz	CL *8
	External	fCL		3.83	4.67	5.50		
Oscillator frequency (2)	Internal	fOSC	VDD = 3.0V Ta = 25°C Duty ratio = 1/34	11.5	14	16.5	kHz	CL *8
	External	fCL		2.30	2.80	3.30		
Voltage converter Input voltage	VDD	× 2	2.4	-	5.5	V	VDD	
		× 3	2.4	-	5.0			
		× 4	2.4	-	3.75			
		× 5	2.4	-	3.0			
Voltage converter output voltage	VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load )	95	99	-	%	VOUT	
Voltage regulator operating voltage	VOUT		4.0	-	15.0	V	VOUT	
Voltage follower operating voltage	V0		4.0	-	15.0	V	V0 *9	
Reference voltage	VREF	VDD = 3.0V Ta = 25°C	2.04	2.10	2.16	V	*10	

**Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)**

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	IDD1	VDD = 3.0V V0 – VSS = 11.0V 1/55 duty ratio Display pattern OFF	-	-	50	μA	*11

**Dynamic Current Consumption (2) when the Built-in Power Circuit is ON (At Operate Mode)**

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	IDD2	VDD = 3.0V, quad boosting, V0 – VSS = 11.0V, 1/55 duty ratio, Display pattern OFF, Normal power mode	-	-	100	μA	*12
		VDD = 3.0V, quad boosting, V0 – VSS = 11.0V, 1/55 duty ratio, Display pattern checker, Normal power mode	-	-	160	μA	*12

**Current Consumption during Power Save mode**

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	IDDS1	VDD = 3.0V During sleep	-	-	2.0	μA	
Standby mode current	IDDS2	VDD = 3.0V During standby	-	-	10.0	μA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	fCL	fM
1/55	On-chip oscillator circuit is used	$\frac{f_{OSC}}{3}$	$\frac{f_{OSC}}{6 \times 55}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{f_{CL}}{2 \times 55}$
1/34	On-chip oscillator circuit is used	$\frac{f_{OSC}}{5}$	$\frac{f_{OSC}}{10 \times 34}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{f_{CL}}{2 \times 34}$

(fOSC: oscillation frequency, fCL: display clock frequency, fM: LCD AC signal frequency)

## [\* Remark Solves]

- \*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
- \*2. In case of external power supply is applied.
- \*3. CS1B, CS2, RS, DB0 to DB7, E\_RD, RW\_WR, RESETB, MS, C68, PS, INTRs, HPMB, REF, DCDC5B, CLS, CL, M, DISP pins.
- \*4. DB0 to DB7, M, FRS, DISP, CL pins.
- \*5. CS1B, CS2, RS, DB[7:0], E\_RD, RW\_WR, RESETB, MS, C68, PS, INTRs, HPMB, REF, DCDC5B, CLS, CL, M, DISP pins.
- \*6. Applies when the DB[7:0], M, DISP, and CL pins are in high impedance.
- \*7. Resistance value when  $\pm 0.1$ [mA] is applied during the On status of the output pin SEGn or COMn.  
 $R_{ON} = \Delta V / 0.1$  [k $\Omega$ ] ( $\Delta V$ : voltage change when  $\pm 0.1$ [mA] is applied in the ON status.)
- \*8. See table 21 for the relationship between oscillation frequency and frame frequency.
- \*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
- \*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
- \*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.  
 The current consumption, when the built-in power supply circuit is on or off.  
 The current flowing through voltage regulation resistors (Ra and Rb) is not included.  
 It does not include the current of the LCD panel capacity, wiring capacity, etc

### REFERENCE DATA

#### IDD1 vs. VDD

\* Test Condition: Temperature (25°C & 85°C), V0 = 11V (External), TEMPS = 'L', 1/55 Duty, Normal Power Mode

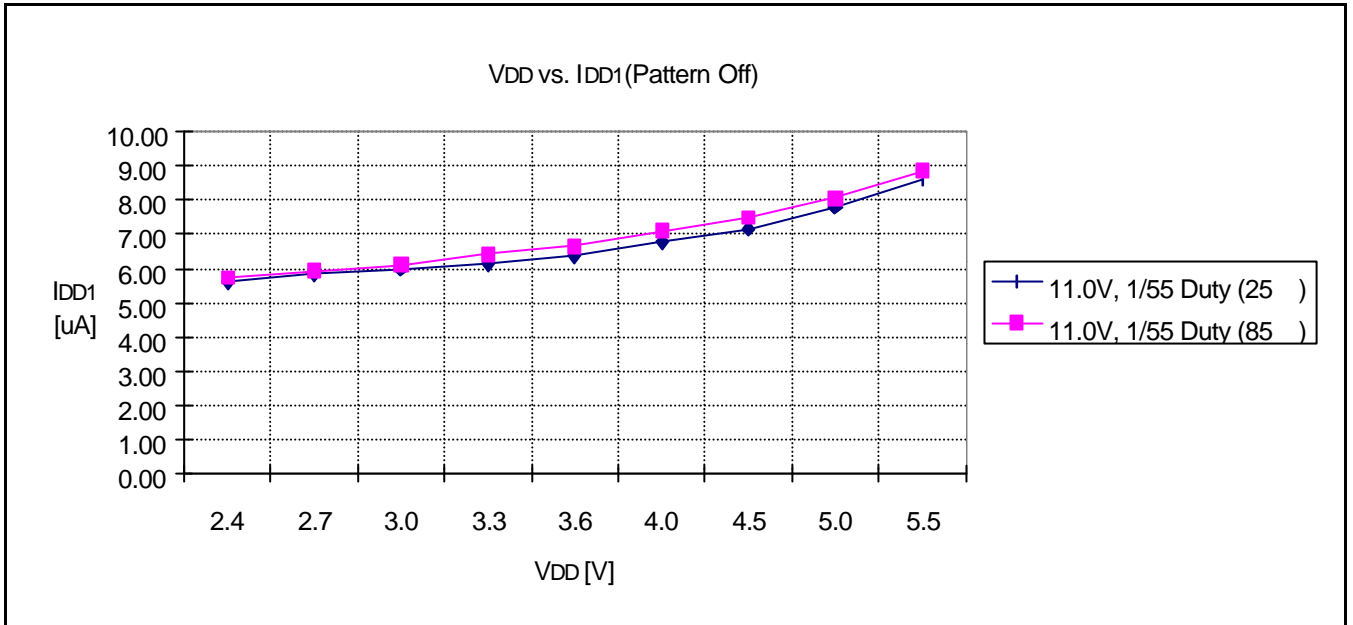
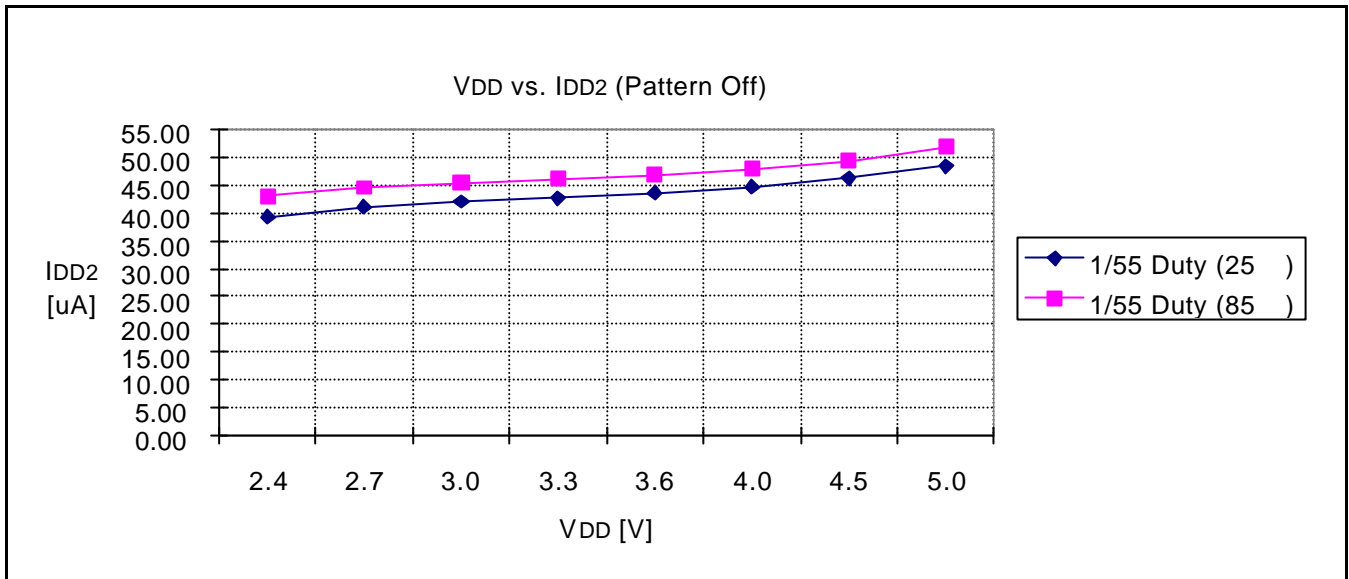


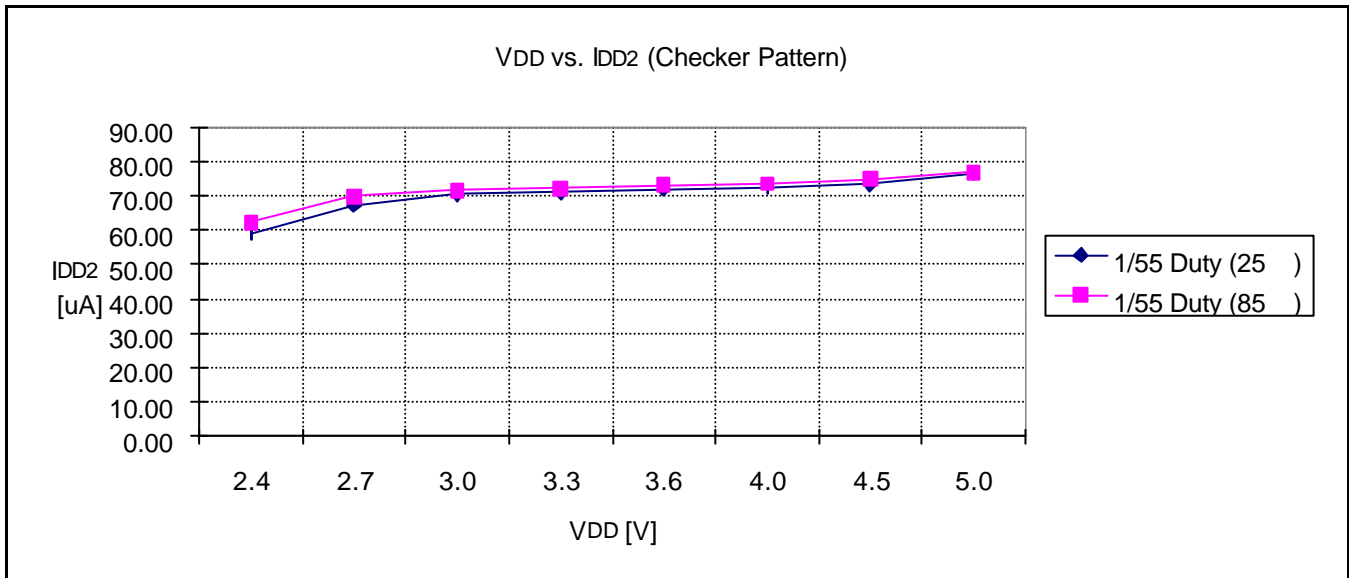
Figure 35. Display Pattern is OFF

**IDD2 vs. VDD**

\* Test Condition: Temperature (25°C & 85°C), Quad Boosting, RR = 6, EV = 32, TEMPS = 'L', 1/55 Duty



**Figure 36. Display Pattern is OFF**



**Figure 37. Display Pattern is Checker**



### AC CHARACTERISTICS

#### Read / Write Characteristics (8080-series MPU)

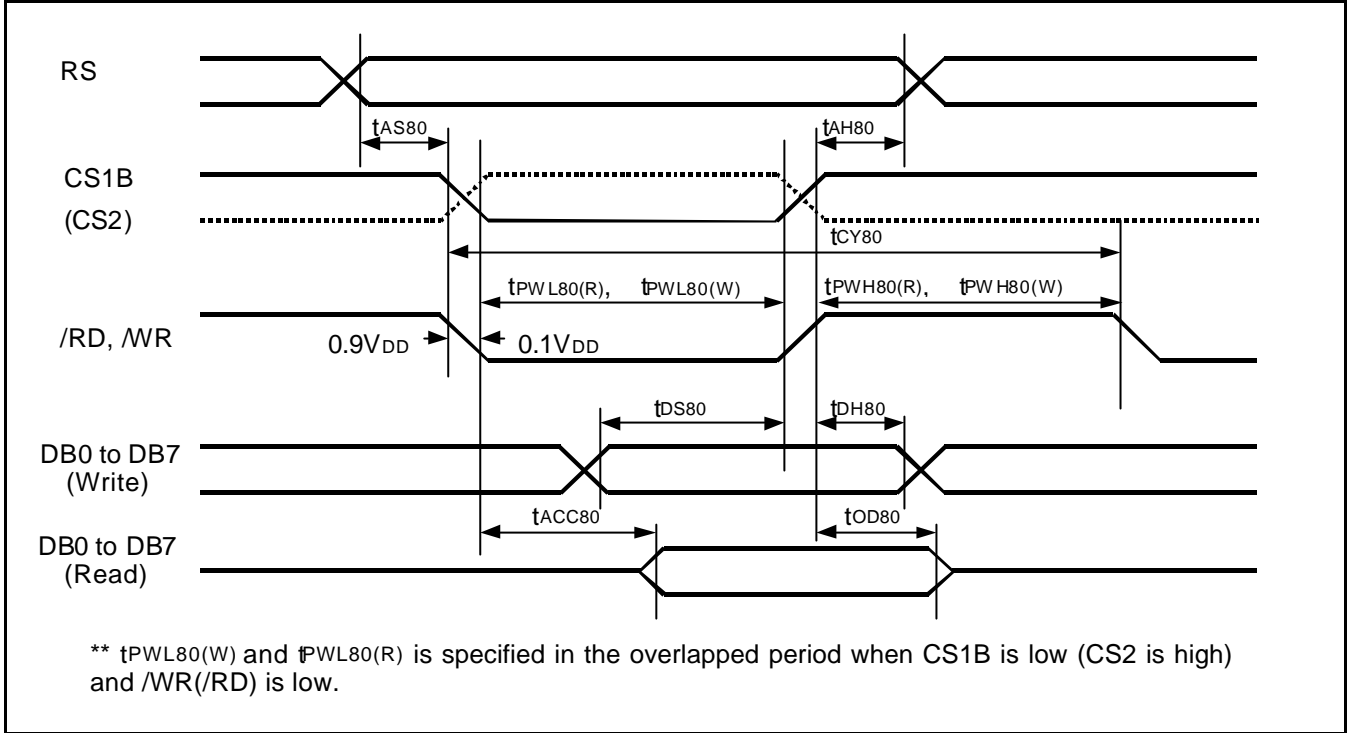


Figure 38. Read / Write Characteristics (8080-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	tAS80 tAH80	13 17	-	-	ns	
System cycle time	/WR, /RD	tCY80	400	-	-	ns	
Enable Pulse Low width	Read	/WR, /RD	tPWL80 (R)	125	-	-	ns
	Write		tPWL80 (W)	55	-	-	ns
Enable Pulse High width	Read	/WR, /RD	tPWH80 (R)	245	-	-	ns
	Write		tPWH80 (W)	315	-	-	ns
Data setup time Data hold time	DB7 To DB0	tDS80 tDH80	35 13	-	-	ns	
Read access time Output disable time		tACC80 tOD80	- 10	-	125 90	ns	CL = 100 pF

(VDD = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	tAS80 tAH80	10 10	-	-	ns	
System cycle time	/WR, /RD	tCY80	150	-	-	ns	
Enable Pulse Low width	Read	/WR, /RD	tPWL80 (R)	65	-	-	ns
	Write		tPWL80 (W)	25	-	-	ns
Enable Pulse High width	Read	/WR, /RD	tPWH80 (R)		-	-	ns
	Write		tPWH80 (W)		-	-	ns
Data setup time Data hold time	DB7 To DB0	tDS80 tDH80	18 10	-	-	ns	
Read access time Output disable time		tACC80 tOD80	- 10	-	65 45	ns	CL = 100 pF

Note: The input signal rising time and falling time (tr, tf) is specified at 15ns or less.

Or (tr + tf) < (tCY80 – tPWL80 (W) – tPWH80 (W)) for write, (tr + tf) < (tCY80 – tPWL80 (R) – tPWH80 (R)) for read.

Read / Write Characteristics (6800-series Microprocessor)

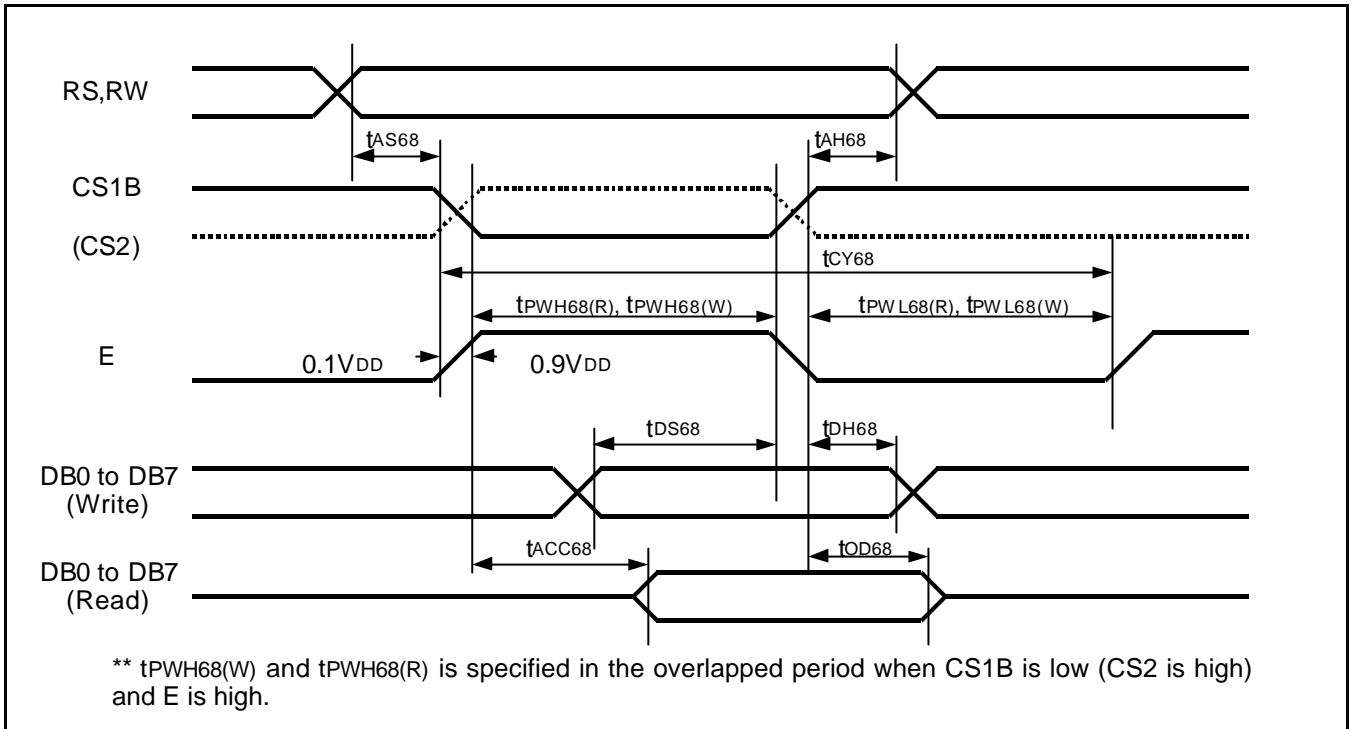


Figure 39. Read / Write Characteristics (6800-series Microprocessor)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS,RW	tAS68 tAH68	13 17	-	-	ns	
System cycle time	E	tCY68	400	-	-	ns	
Enable Pulse Low Width	Read	tPWL68 (R)	125			ns	
	Write	tPWL68 (W)	55				
Enable Pulse High Width	Read	tPWH68 (R)	245			ns	
	Write	tPWH68 (W)	315				
Data setup time Data hold time	DB7 To DB0	tDS68 tDH68	35 13	-	-	ns	
Access time Output disable time		tACC68 tOD68	- 10	-	125 90	ns	CL = 100 pF

(VDD = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS,RW	tAS68 tAH68	10 10	-	-	ns	
System cycle time	E	tCY68	150	-	-	ns	
Enable Pulse Low Width	Read	tPWL68 (R)	65			ns	
	Write	tPWL68 (W)	25				
Enable Pulse High Width	Read	tPWH68 (R)				ns	
	Write	tPWH68 (W)					
Data setup time Data hold time	DB7 To DB0	tDS68 tDH68	18 10	-	-	ns	
Access time Output disable time		tACC68 tOD68	- 10	-	65 45	ns	CL = 100 pF

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less.

Or (tr + tf) &lt; (tCY68 – tPWL68 (W) – tPWH68 (W)) for write, (tr + tf) &lt; (tCY68 – tPWL68 (R) – tPWH68 (R)) for read.

Serial Interface Characteristics

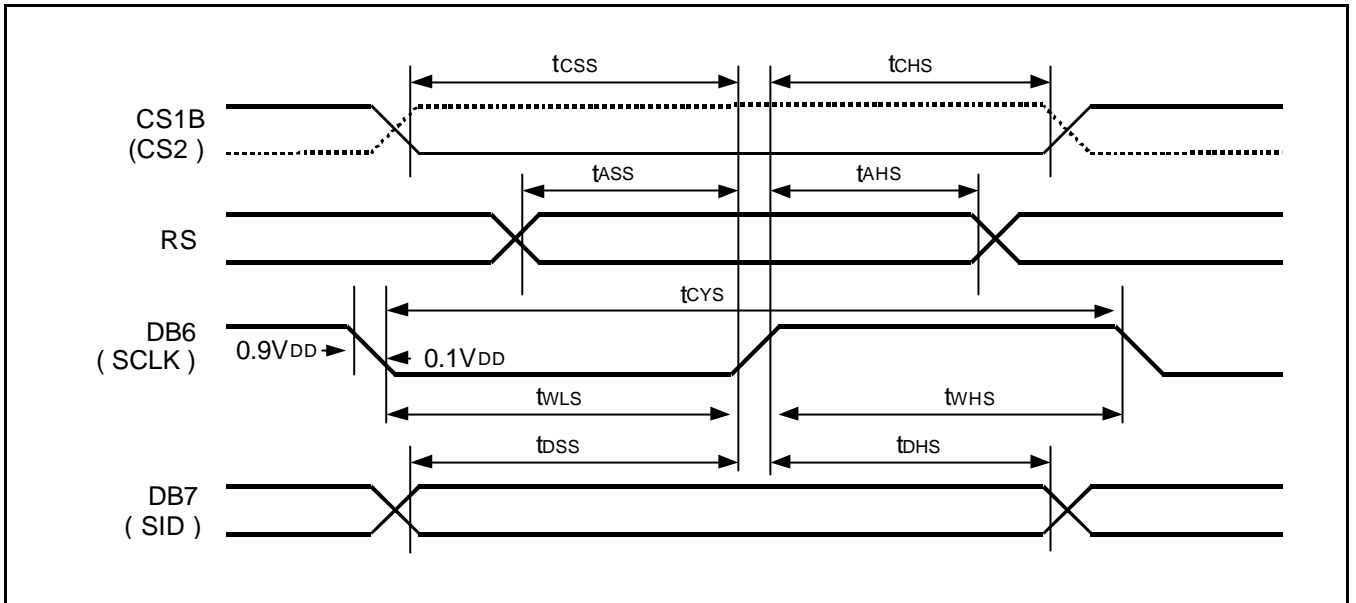


Figure 40. Serial Interface Characteristics

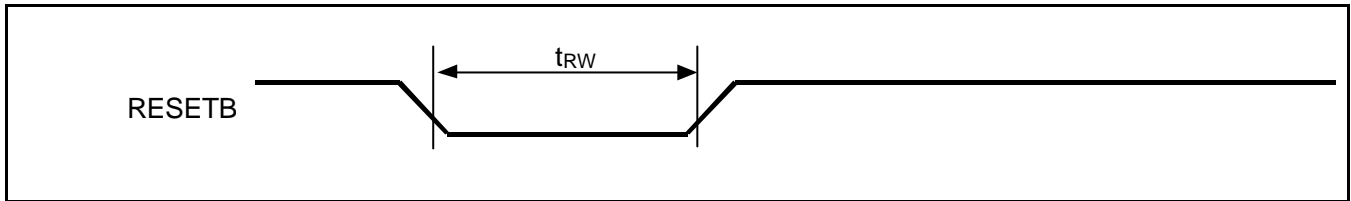
(V<sub>DD</sub> = 2.4 to 3.6V, T<sub>a</sub> = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	DB6 (SCLK)	tCYS	450	-	-	ns	
SCLK high pulse width		tWHS	180	-	-		
SCLK low pulse width		tWLS	135	-	-		
Address setup time	RS	tASS	90	-	-	ns	
Address hold time		tAHS	360	-	-		
Data setup time	DB7 (SID)	tDSS	90	-	-	ns	
Data hold time		tDHS	90	-	-		
CS1B setup time	CS1B	tCSS	55	-	-	ns	
CS1B hold time		tCHS	180	-	-		

(V<sub>DD</sub> = 4.5 to 5.5V, T<sub>a</sub> = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	DB6 (SCLK)	tCYS	225	-	-	ns	
SCLK high pulse width		tWHS	90	-	-		
SCLK low pulse width		tWLS	70	-	-		
Address setup time	RS	tASS	45	-	-	ns	
Address hold time		tAHS	180	-	-		
Data setup time	DB7 (SID)	tDSS	45	-	-	ns	
Data hold time		tDHS	45	-	-		
CS1B setup time	CS1B	tCSS	25	-	-	ns	
CS1B hold time		tCHS	90	-	-		

**Reset Input Timing**



**Figure 41. Reset Input Timing**

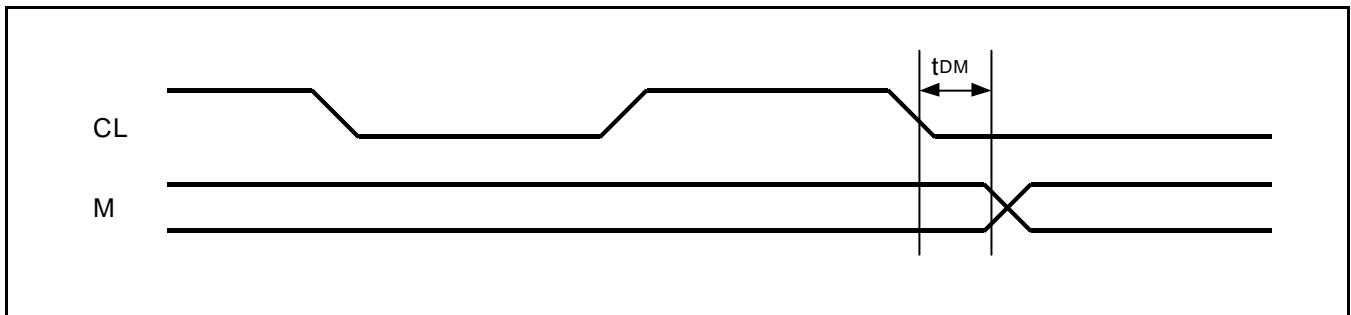
(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	tRW	900	-	-	ns	

(VDD = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	tRW	450	-	-	ns	

**Display Control Output Timing**



**Figure 42. Display Control Output Timing**

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	tDM	-	13	70	ns	

(VDD = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	tDM	-	10	35	ns	

## REFERENCE APPLICATIONS

### MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", C68 = "H")

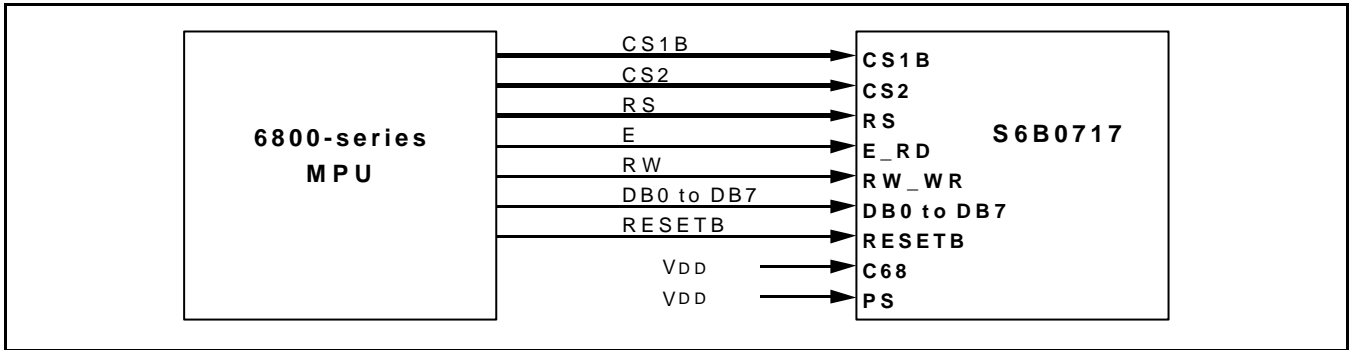


Figure 43. In Case of Interfacing with 6800-series (PS = "H", C68 = "H")

In Case of Interfacing with 8080-series (PS = "H", C68 = "L")

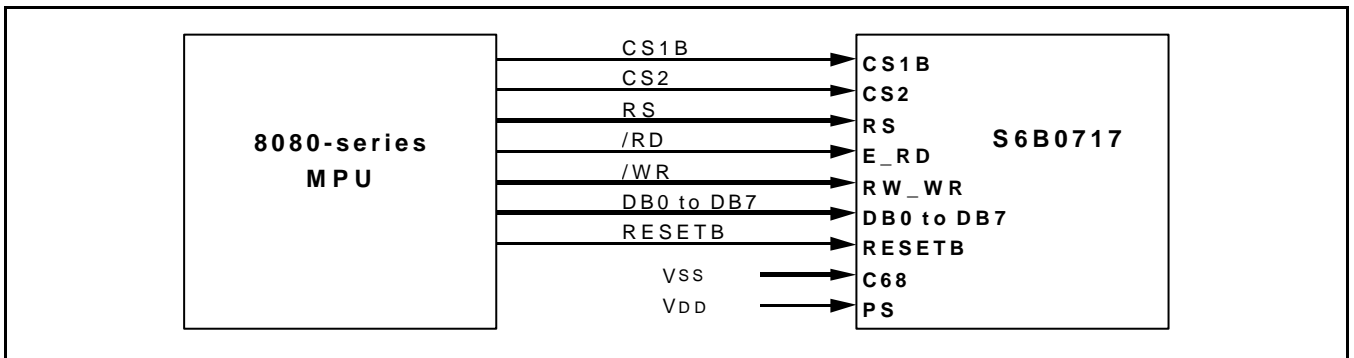


Figure 44. In Case of Interfacing with 8080-series (PS = "H", C68 = "L")

In Case of Serial Interface (PS = "L", C68 = "H/L")

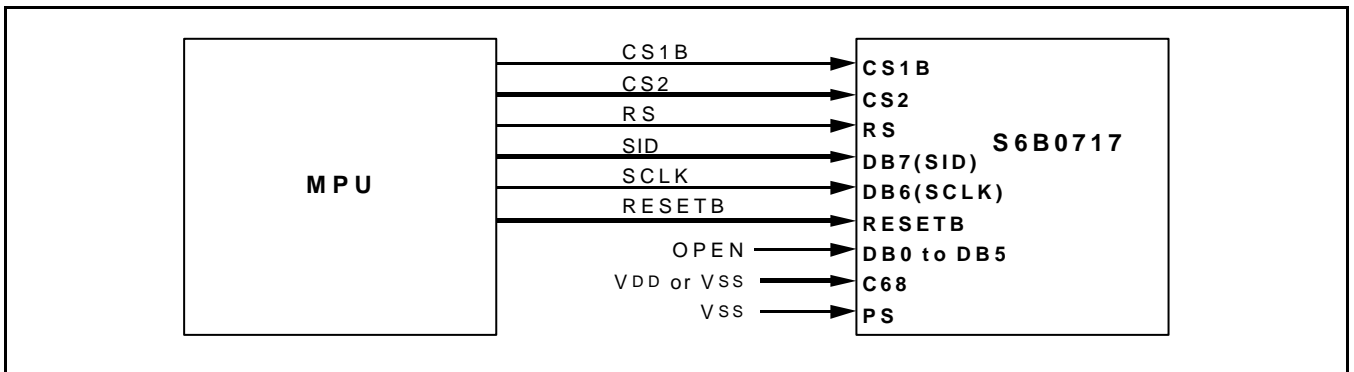


Figure 45. In Case of Serial Interface (PS = "L", C68 = "H/L")

## CONNECTIONS BETWEEN S6B0717 AND LCD PANEL

### Single Chip Configuration (1/55 Duty Configurations)

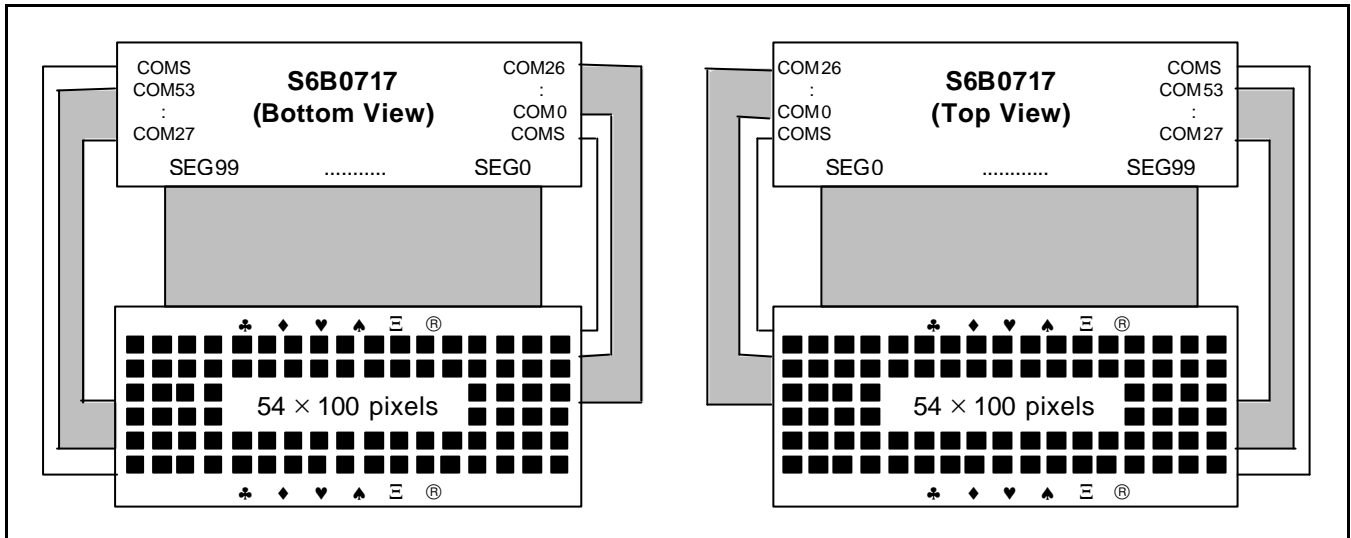


Figure 46. SHL = 0, ADC = 1

Figure 47. SHL = 0, ADC = 0

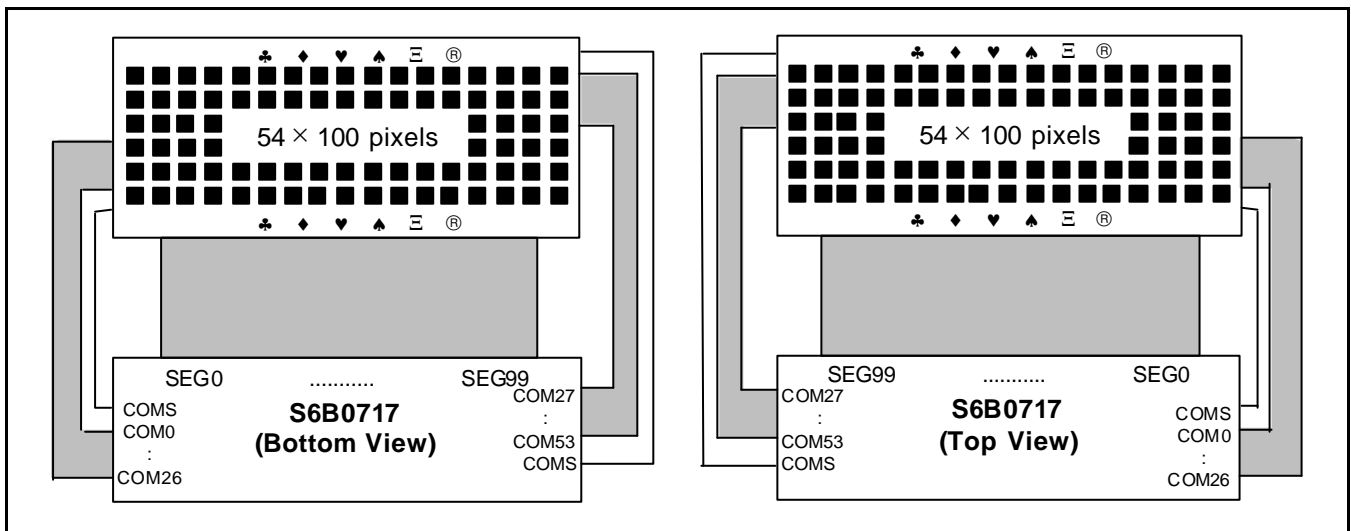


Figure 48. SHL = 1, ADC = 0

Figure 49. SHL = 1, ADC = 1



Single Chip Configuration (1/34 Duty Configurations)

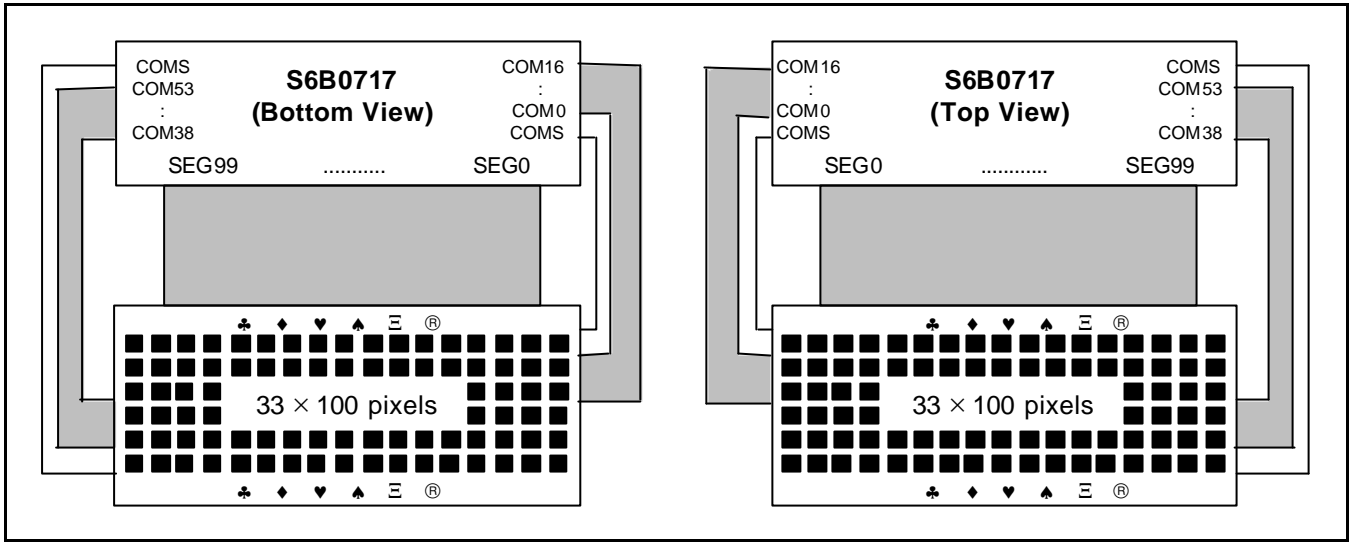


Figure 50. SHL = 0, ADC = 1

Figure 51. SHL = 0, ADC = 0

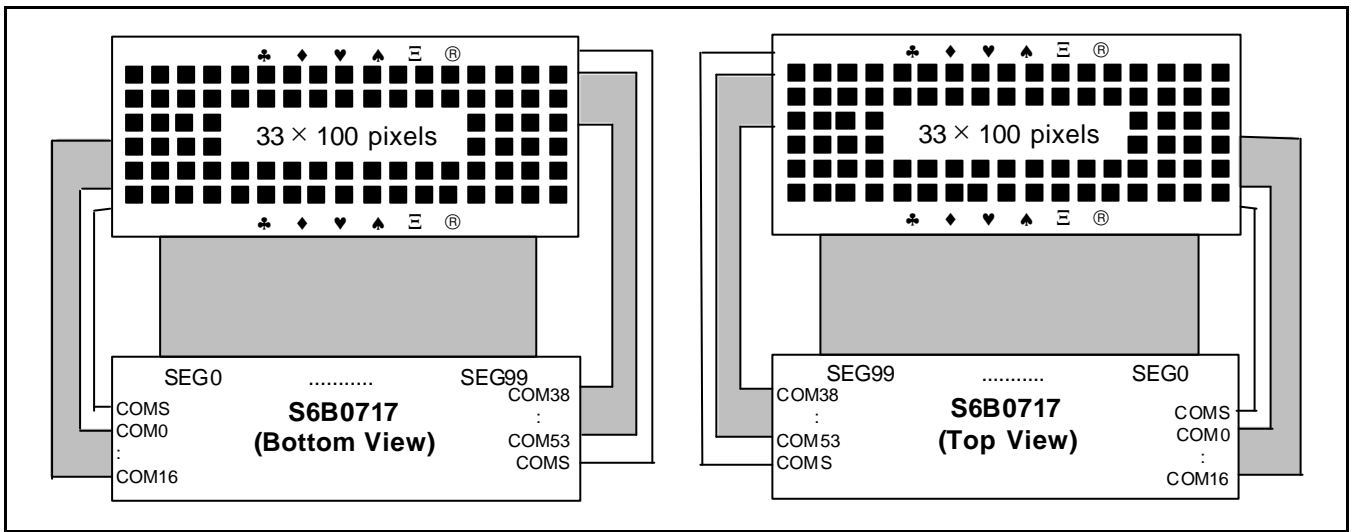


Figure 52. SHL = 1, ADC = 0

Figure 53. SHL = 1, ADC = 1

Multiple Chip Configuration

- 55COM (54COM + 1COMS) ^ 200SEG (100SEG ^ 2)

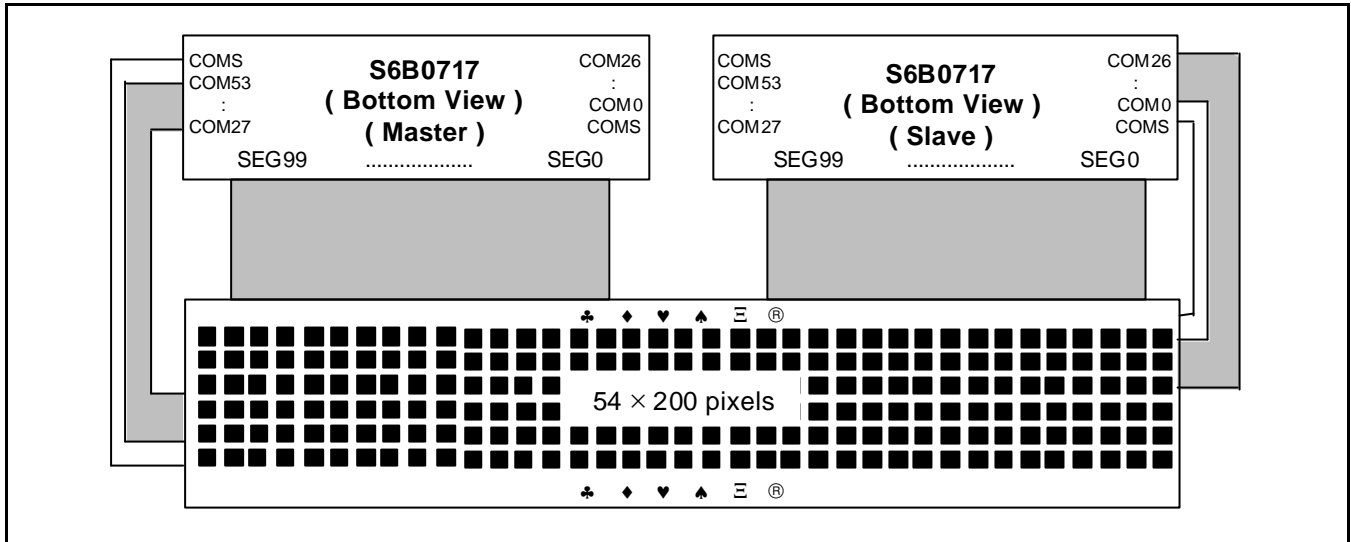


Figure 54. SHL = 0, ADC = 1

- ◆ Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

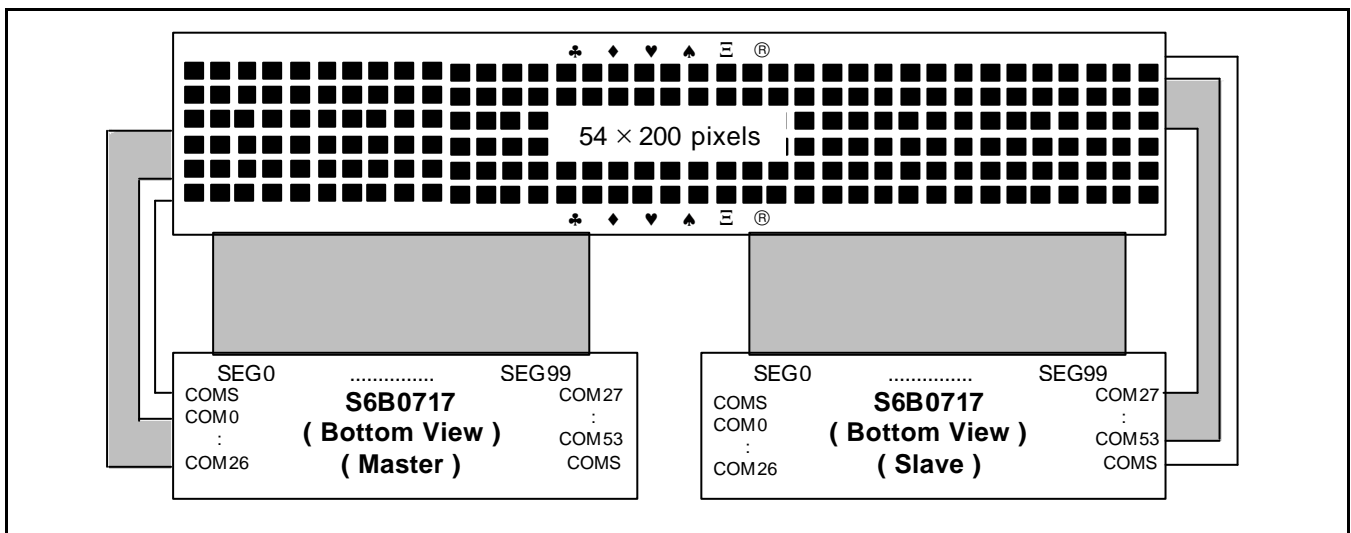


Figure 55. SHL = 1, ADC = 0

- ◆ Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- 110COM (108COM + 2COMS) ^ 100SEG

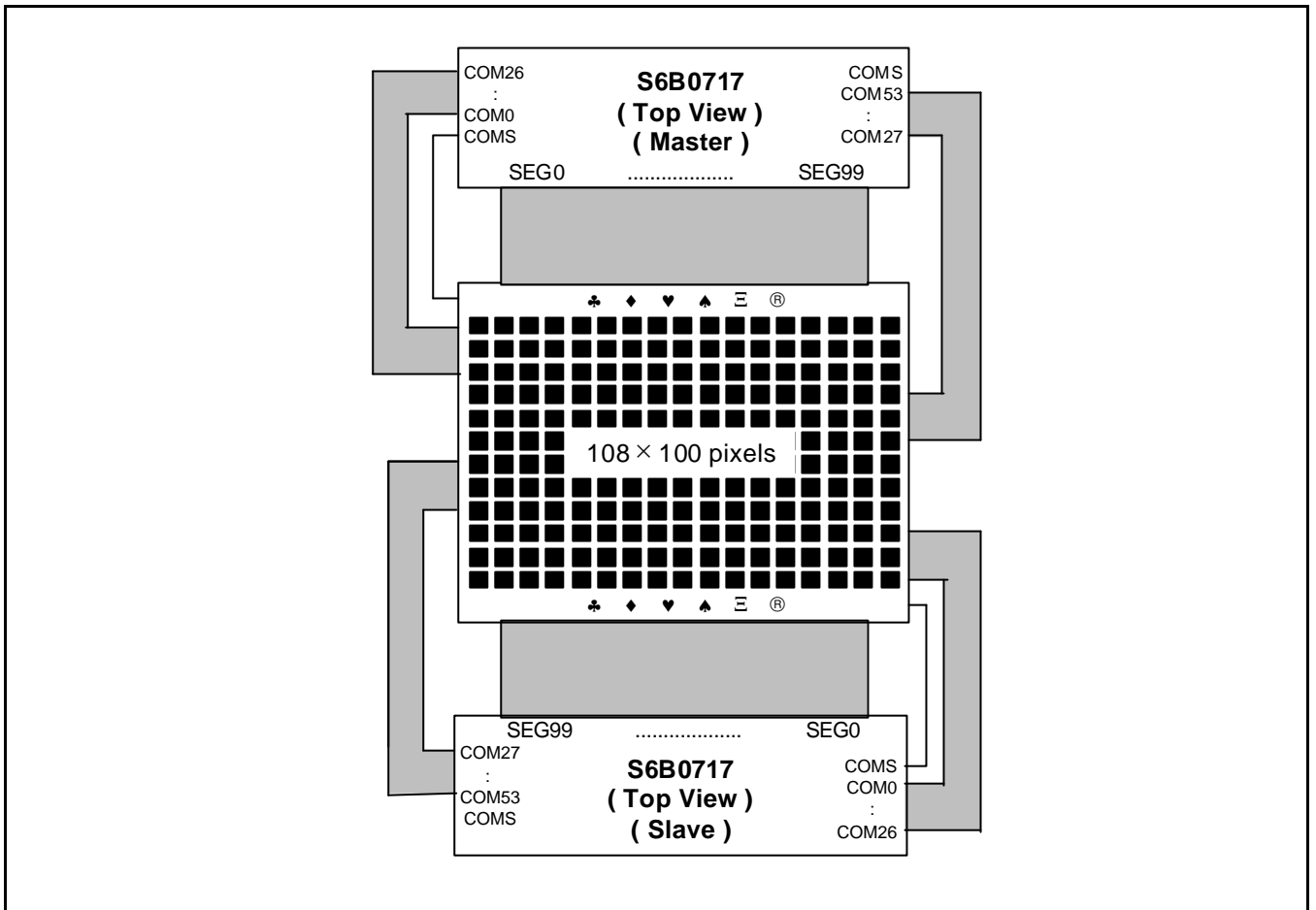


Figure 56. 110COM (108COM + 2COMS) ^ 100SEG

- ◆ Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4
- ◆ Common / Segment output direction select
  - Master chip: SHL = 0, ADC = 0
  - Slave chip: SHL = 1, ADC = 1