DATA SHEET

PCF2119x-2
LCD controllers/drivers

Product specification 28. August 2000
File under Integrated Circuits, IC12

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 16 characters + 160 icons, or 1-line display of up to 32 characters + 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - Configurable 4 (3, 2) * voltage multiplier generating LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCD}: –0.16 to –0.24 %/K (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- Display Data RAM: 80 characters
- Character Generator ROM: 240, 5 × 8 characters
- Character Generator RAM: 16, 5 × 8 characters; 4 characters used to drive 160 icons, 8 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I^2C-bus interface
- CMOS compatible
- 18 row and 80 column outputs
- Multiplex rates 1 : 18 (for normal operation), 1 : 9 (for single line operation) and 1 : 2 (for icon only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD1} - V_{SS}$ = 1.5 to 5.5 V (chip may be driven with two battery cells)
- HVgen supply voltage range, $V_{DD2,3} - V_{SS}$ = 2.2 to 4.0V
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Direct mode to save current consumption for icon mode and Mux 1 : 9 (depending on V_{DD2} value and LCD liquid properties)
- Very low current consumption (20 to 200 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2 μA.

1.1 Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2119x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2-line by 16 or 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter ‘x’ in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PC2119RU/2	–	chip with bumps in tray	–
PC2119SU/2	–	chip with bumps in tray	–
PC2119VU/2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

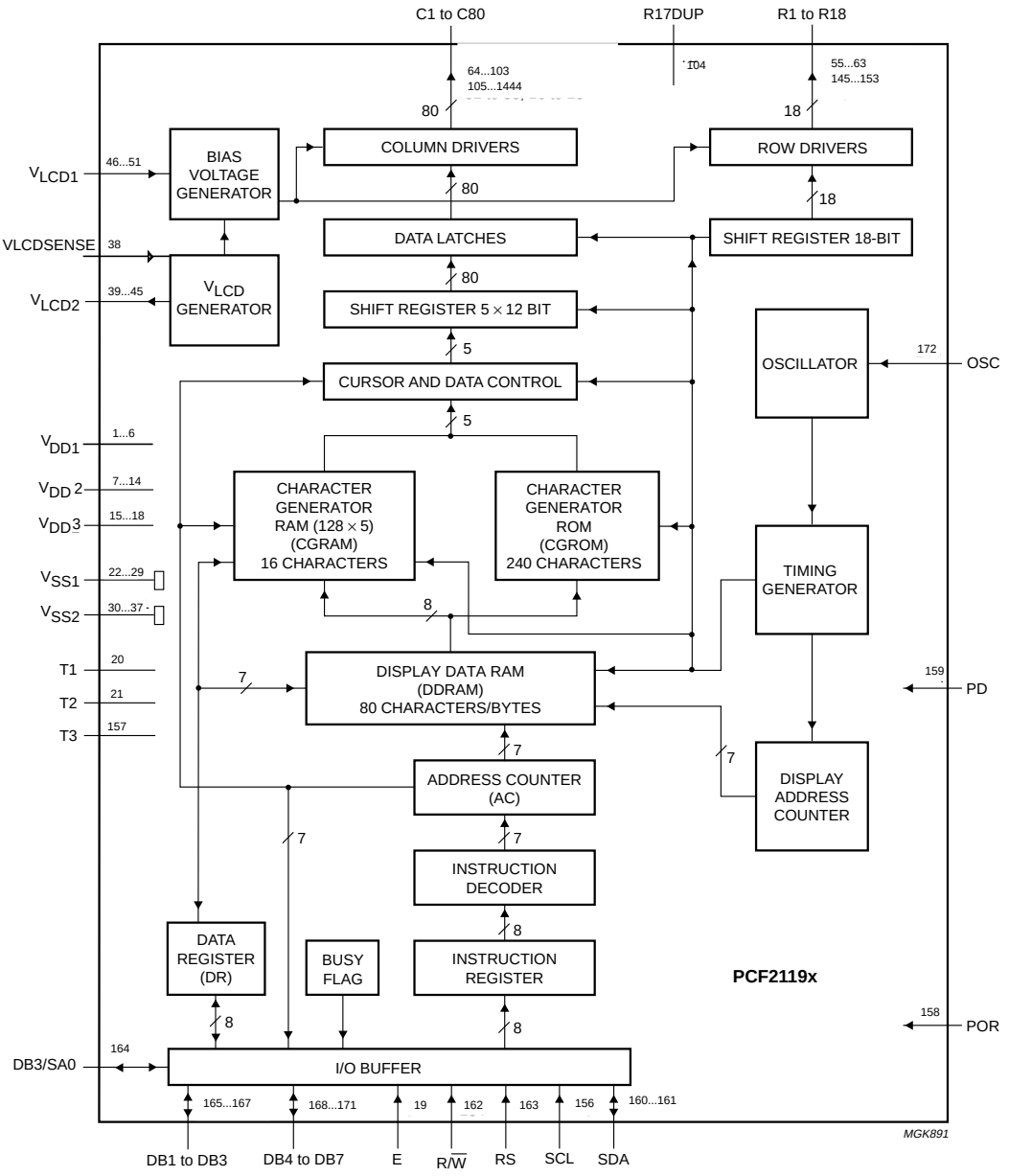


Fig.1 Block diagram.

6 PAD INFORMATION

The identification of each pad and its location is given in Chapter 18.

6.1 Pad functions

Table 1 Pad function description

SYMBOL	DESCRIPTION
V_{DD1}	Logic supply voltage
$V_{DD2,3}$	High voltage generator supply voltages (always put $V_{DD2} = V_{DD3}$).
V_{SS1}	This is the ground pad for all except the high voltage generator.
V_{SS2}	This is the ground pad for the high voltage generator.
V_{LCD1}	This input is used for the generation of the LCD bias levels.
V_{LCD2}	This is the V_{LCD} output pad if V_{LCD} is generated internally. This pad must be connected to V_{LCD1}.
$V_{LCDSENSE}$	This input (V_{LCD}) is used for the voltage multiplier's regulation circuitry. This pad must be connected to V_{LCD2}.
E	The data bus clock input is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock; note 1.
T1	These are three test pads. T1 and T2 must be connected to V_{SS1}; T3 is left open-circuit and is not user accessible.
T2	
T3	
R1 to R18; R17DUP	LCD row driver outputs R1 to R18; these pads output the row select waveforms to the display; R17 and R18 drive the icons. R17 has two pads R17 and R17DUP.
C1 to C80	LCD column driver outputs C1 to C80.
SCL	I^2C-bus serial clock input; note 1.
POR	External power-on reset input.
PD	PD selects the chip power-down mode; for normal operation PD = 0.
SDA	I^2C-bus serial data input/output; note 1.
R/$\overline{W}$	This is the read/write input. R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation. This pad has an internal pull-up resistor.
RS	The RS input selects the register to be accessed for read and write. RS = 0, selects the instruction register for write and the busy flag and address counter for read. RS = 1, selects the data register for both read and write. This pad has an internal pull-up resistor.
DB0 to DB7	The 8-bit bidirectional data bus (3-state) transfers data between the system controller and the PCF2119x. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit. Data bus line DB3 has an alternative function (SA0), when selected this is the I^2C-bus address pad. Each data line has its own internal pull-up resistor; note 1.
OSC	Oscillator or external clock input. When the on-chip oscillator is used this pad must be connected to V_{DD1}.

Note

1. When the I^2C-bus is used, the parallel interface pad E must be at logic 0. In the I^2C-bus read mode DB0 - DB2 and DB3 - DB7 should be connected to V_{DD1} or left open-circuit.
   a) When the parallel bus is used, pads SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open-circuit.
   b) If the 4-bit interface is used without reading out from the PCF2119x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB4 can either be set to V_{SS1} or V_{DD1} instead of leaving them open-circuit.

7 FUNCTIONAL DESCRIPTION

7.1 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The voltage generator is controlled by two internal 6-bit registers: V_A and V_B. The nominal LCD operating voltage at room temperature is given by the relationship:

$$V_{OP(nom)} = (\text{integer value of register} \times 0.08) + 1.82$$

7.2 Programming ranges

Programmed value: 1 to 63. Voltage: 1.90 to 6.86 V. T_{ref} = 27 °C.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

Value 0 for V_A and V_B switches the generator off (i.e. V_A = 0 in character mode, V_B = 0 in icon mode).

Usually register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode.

When V_{LCD} is generated on-chip the V_{LCD} pads should be decoupled to V_{SS} with a suitable capacitor. The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the voltage generator and the direct mode are switched off, an external voltage may be supplied at connected pads $V_{LCD1,2}$. $V_{LCD1,2}$ may be higher or lower than V_{DD}.

During direct mode (program DM register bit) the internal voltage generator is turned off and the V_{LCD} output voltage is directly connected to V_{DD2}. This reduces the current consumption during icon mode and Mux 1 : 9 (depending on V_{DD2} value and LCD liquid properties).

The LCD supply voltage generator ensures that, as long as V_{DD} is in the valid range (2.2 to 4 V), the required peak voltage V_{OP} = 6.5 V can be generated at any time.

7.3 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} < 5 V for most LCD liquids. The intermediate bias levels for the different multiplex rates are shown in Table 2. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 2 Bias levels as a function of multiplex rate

MULTIPLEX RATE	NUMBER OF LEVELS	V_1	V_2	V_3	V_4	V_5	V_6
1 : 18	5	V_{op}	3/4[1]	1/2	1/2	1/4	V_{ss}
1 : 9	5	V_{op}	3/4	1/2	1/2	1/4	V_{ss}
1 : 2	4	V_{op}	2/3	2/3	1/3	1/3	V_{ss}

Note

1. The values in the above table are given relative to $V_{op} - V_{ss}$, e.g. 3/4 means 3/4 × ($V_{op} - V_{ss}$).

7.4 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pad must be connected to V_{DD}.

7.5 External clock

If an external clock is to be used this is input at the OSC pad. The resulting display frame frequency is given by:

$$f_{frame} = \frac{f_{OSC}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.6 Power-on reset

The PC2119x must be reset externally. This is an internal synchronous reset that requires 3 OSC cycles to be executed after release of the external reset signal. If no external reset is performed, the chip might start-up in an unwanted state. The external reset is active high.

7.7 Power-down mode

The chip can be put into power-down mode by applying an external active high level to the PD pad. In power-down mode all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAMs and the chip state are preserved. Instruction execution during power-down is possible when pad OSC is externally clocked.

7.8 Registers

The PCF2119x has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as ‘display clear’ and ‘cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM).

The instruction register can be written to but not read from by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the ‘read data’ instruction.

7.9 Busy flag

The busy flag indicates the internal status of the PCF2119x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pad DB7 when RS = 0 and R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is at logic 0 or waiting for the required number of cycles.

7.10 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands ‘set CGRAM address’ and ‘set DDRAM address’. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and R/$\overline{W}$ = 1.

7.11 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Fig.2. With no display shift the characters represented by the codes in the first 32 RAM locations starting at address 00H in line 1 are displayed. Figures 3 and 4 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap-around operations for the various modes are shown in Table 3.

Table 3 Address space and wrap-around operation

MODE	1 × 32	2 × 16	1 × 9
Address space	00 to 4F	00 to 27; 40 to 67	00 to 27
Read/write wrap-around (moves to next line)	4F to 00	27 to 40; 67 to 00	27 to 00
Display shift wrap-around (stays within line)	4F to 00	27 to 00; 67 to 40	27 to 00

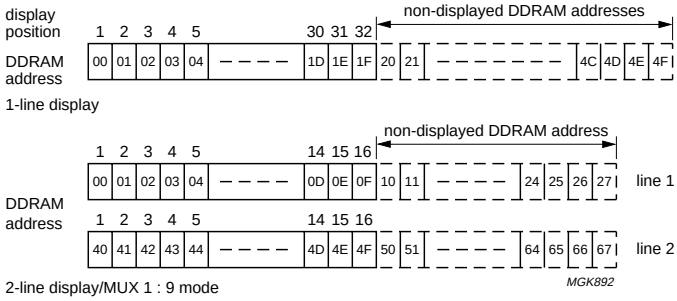


Fig.2 DDRAM to display mapping: no shift.

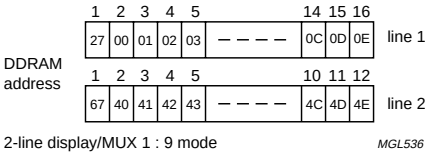


Fig.3DDRAM to display mapping: right shift

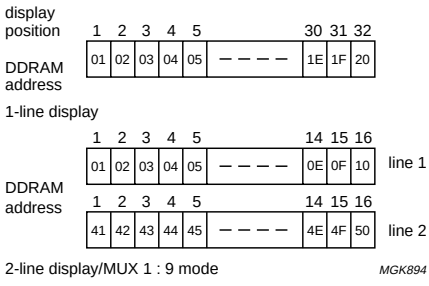


Fig.4DDRAM to display mapping; left shift

7.12 Character Generator ROM (CGROM)

The Character Generator ROM generates 240 character patterns in a 5×8 dot format from 8-bit character codes. Figure 6 to 8 show the character sets that are currently implemented.

7.13 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the Character Generator RAM. Some CGRAM characters (see Fig.17) are also used to drive icons (6 if icons blink and both icon rows are used in the application; 3 if no blink but both icon rows are used in the application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.6). Figure 9 shows the addressing principle for the CGRAM.

7.14 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.5 at the DDRAM address contained in the address counter.

When the address counter contains the CGRAM address the cursor will be inhibited.

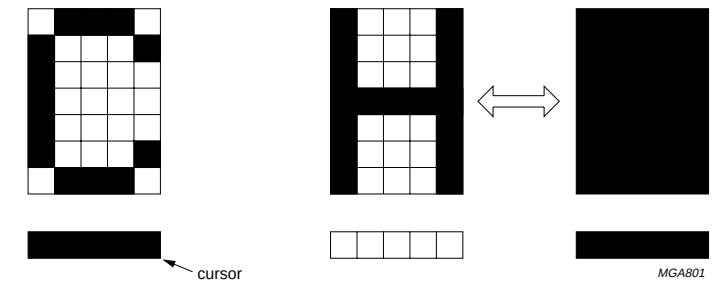
7.15 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.16 LCD row and column drivers

The PCF2119x contains 18 row and 80 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 10 to 13 show typical waveforms. Unused outputs should be left unconnected.



5 x 7 dot character font alternating display

cursor display example blink display example

Fig.5 Cursor and blink display examples.

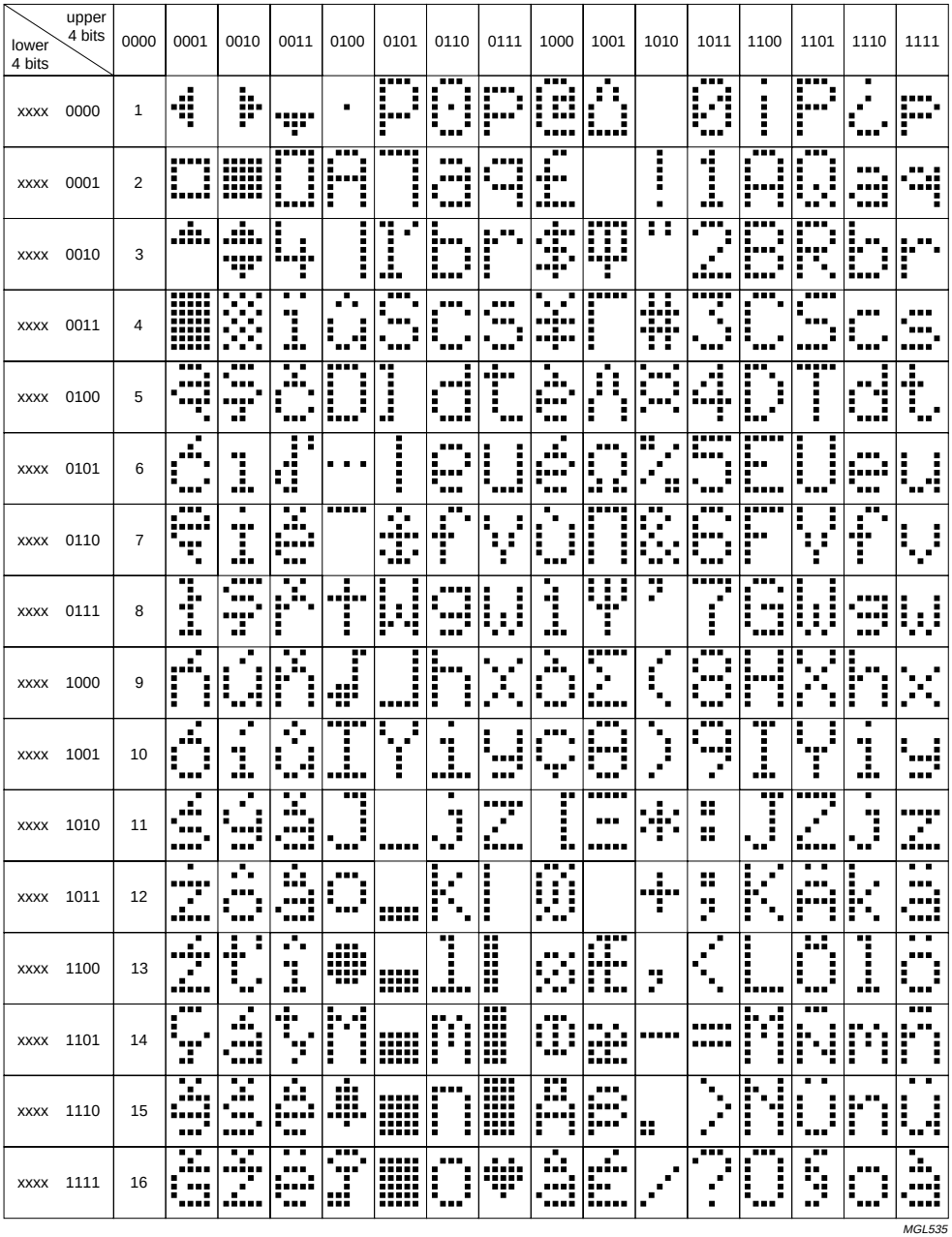


Fig.6 Character set ‘R’ in CGROM.

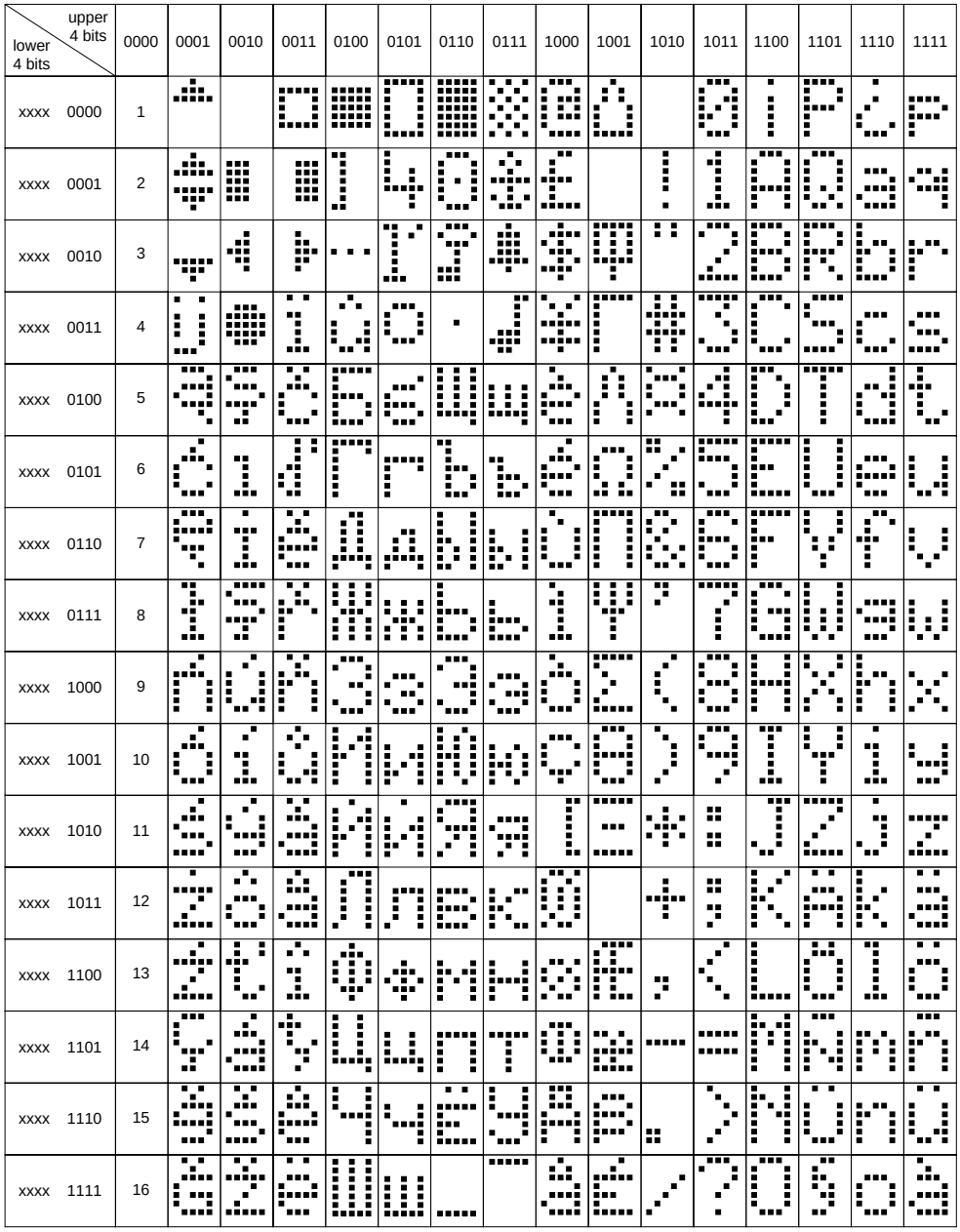


Fig.7 Character set ‘S’ in CGROM.

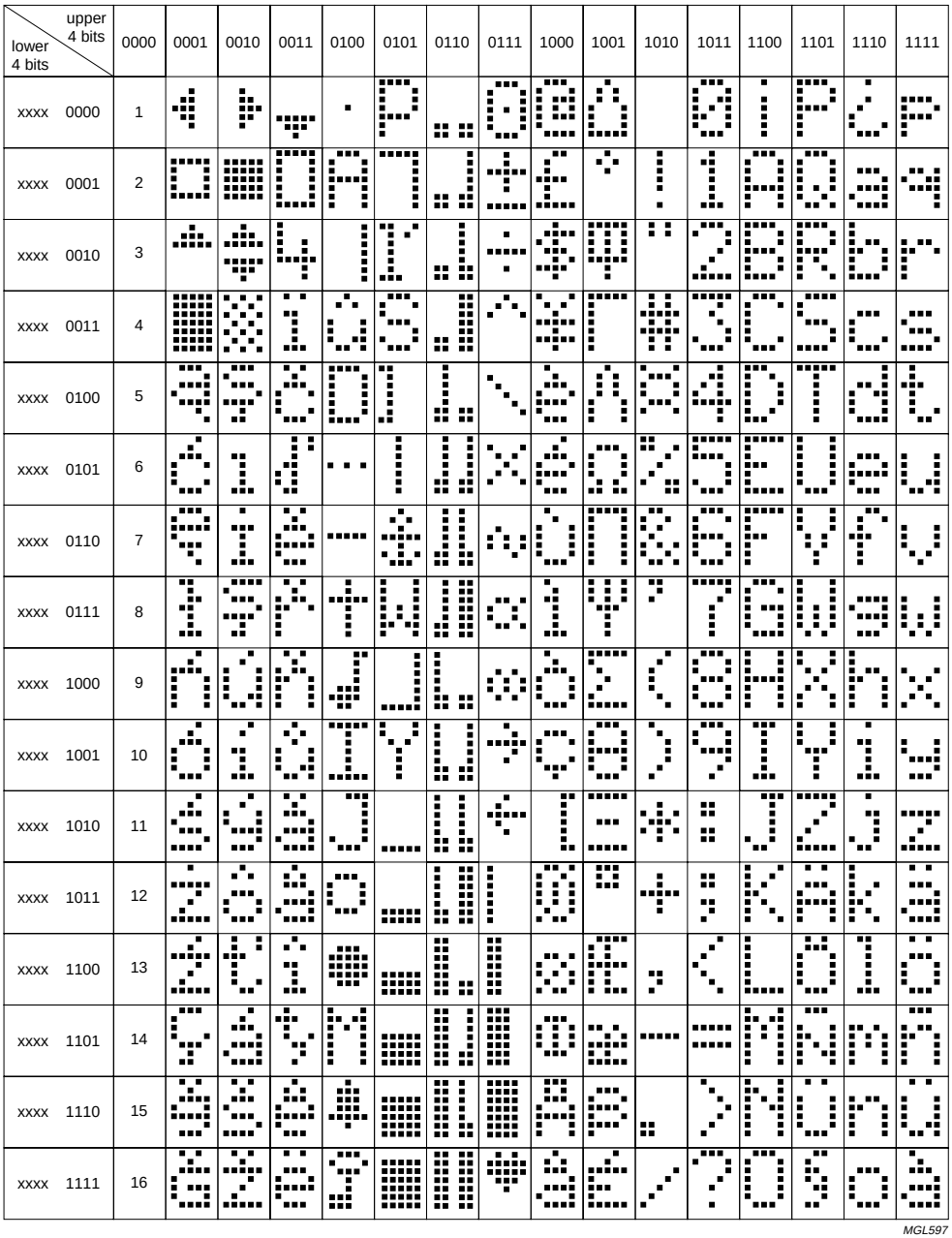
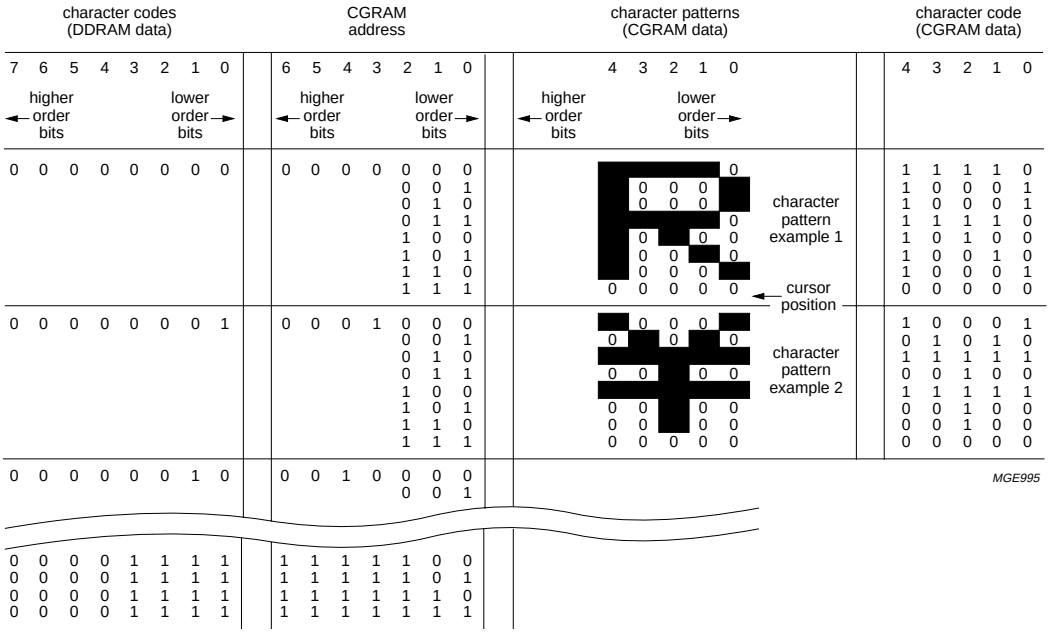


Fig.8 Character set ‘V’ in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.6.

As shown in Figs 6 and 7, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the ‘set CGRAM address’ command. Bit 6 can be set using the ‘set DDRAM address’ command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘read busy flag and address counter’ command.

Fig.9 Relationship between CGRAM addresses, data and display patterns.

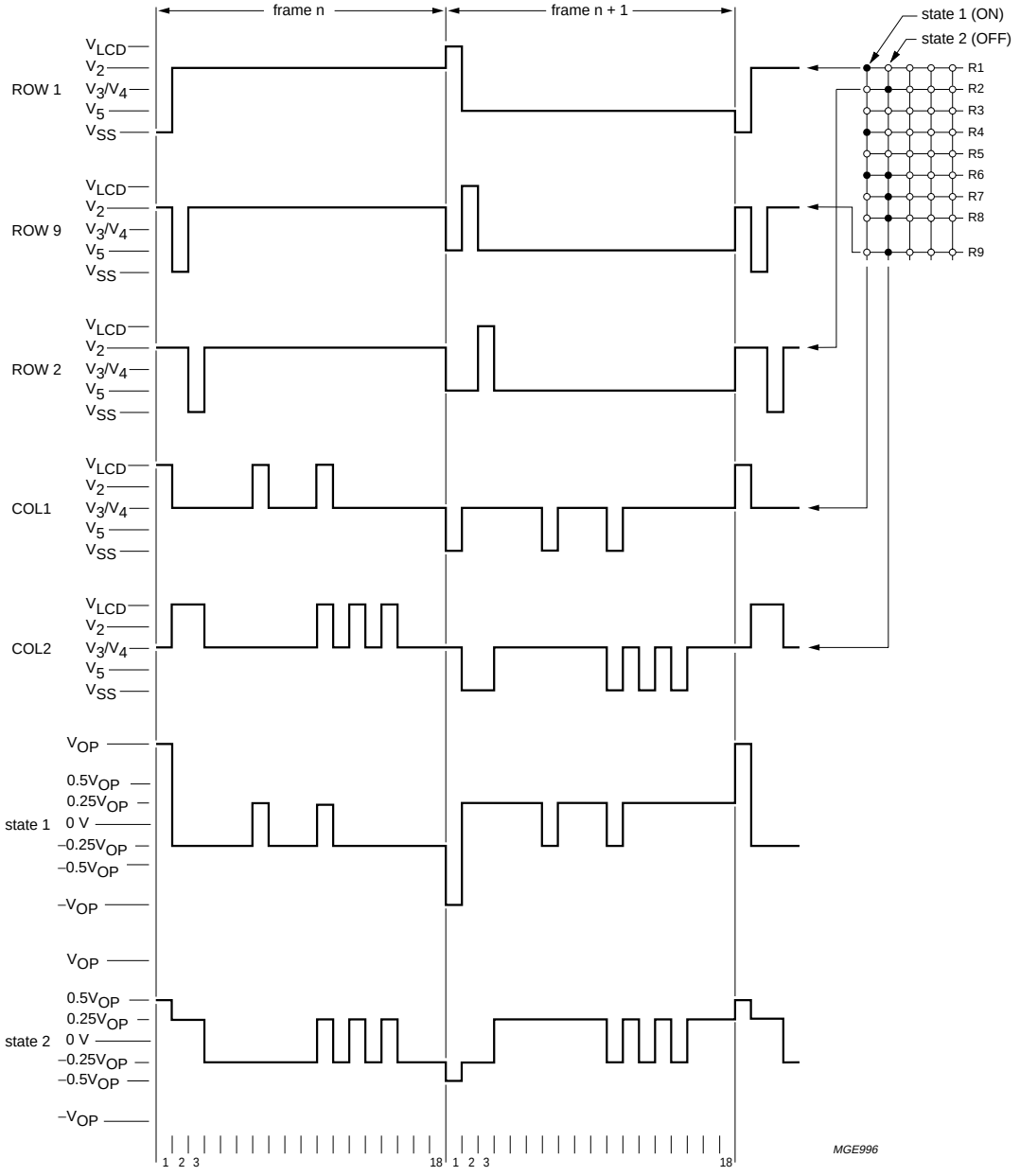


Fig.10 MUX 1 : 18 LCD waveforms; character mode.

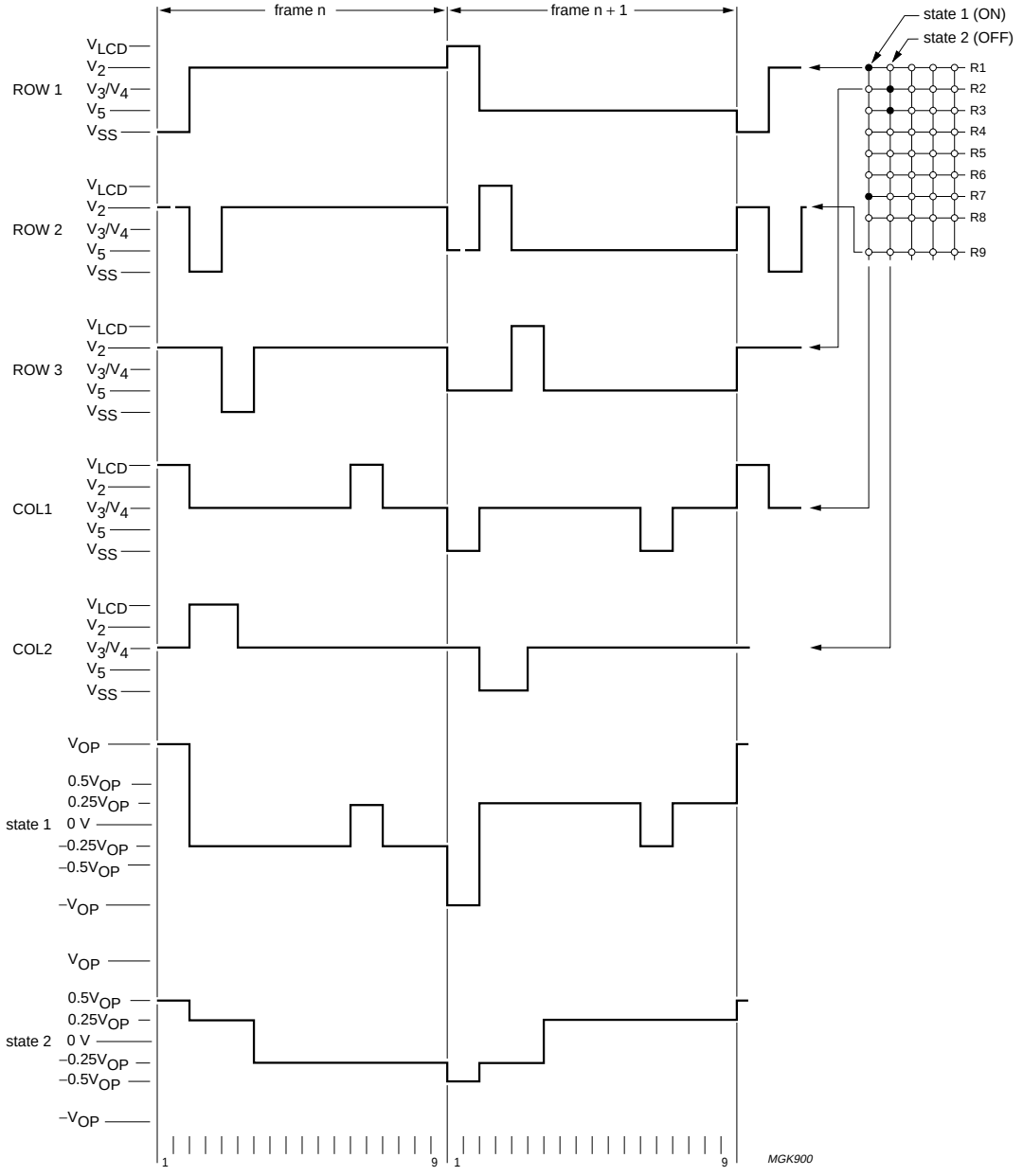


Fig.11 MUX 1 : 9 LCD waveforms; character mode. R10 to 18 to be left open.

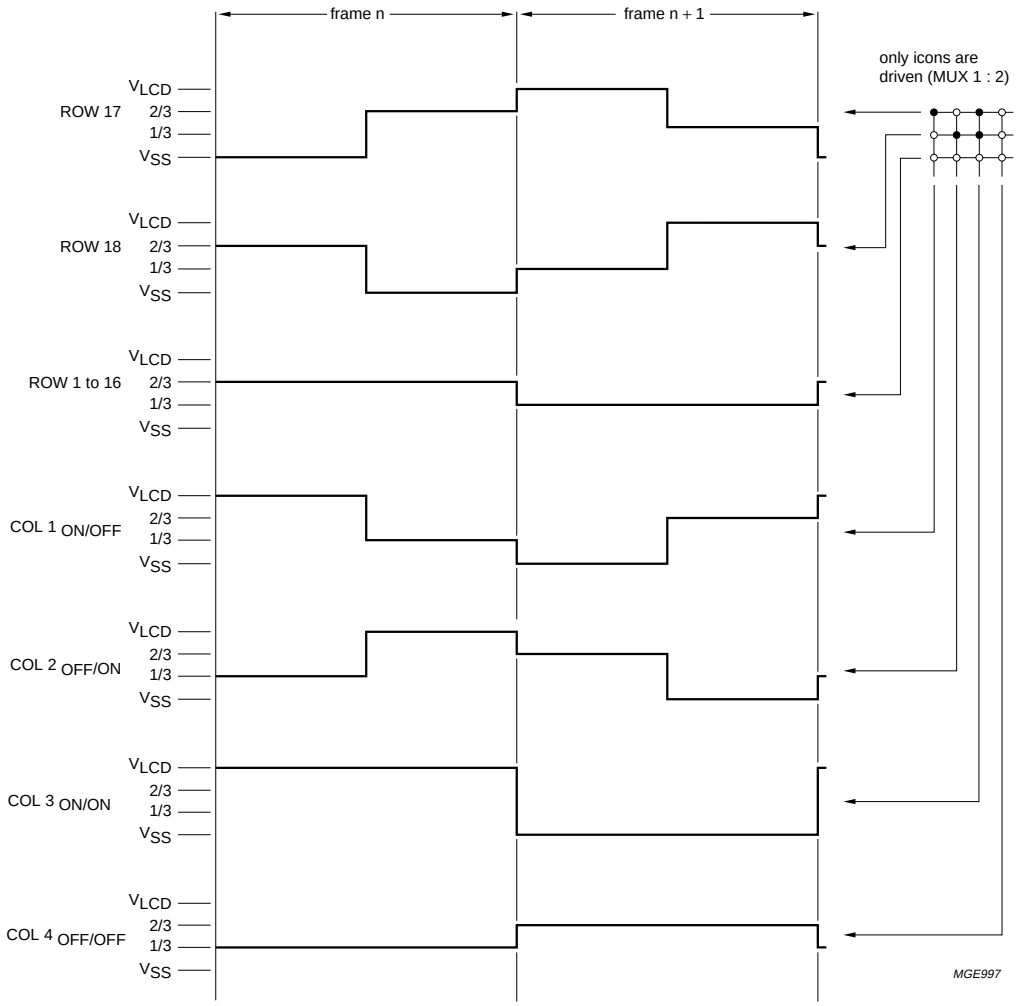
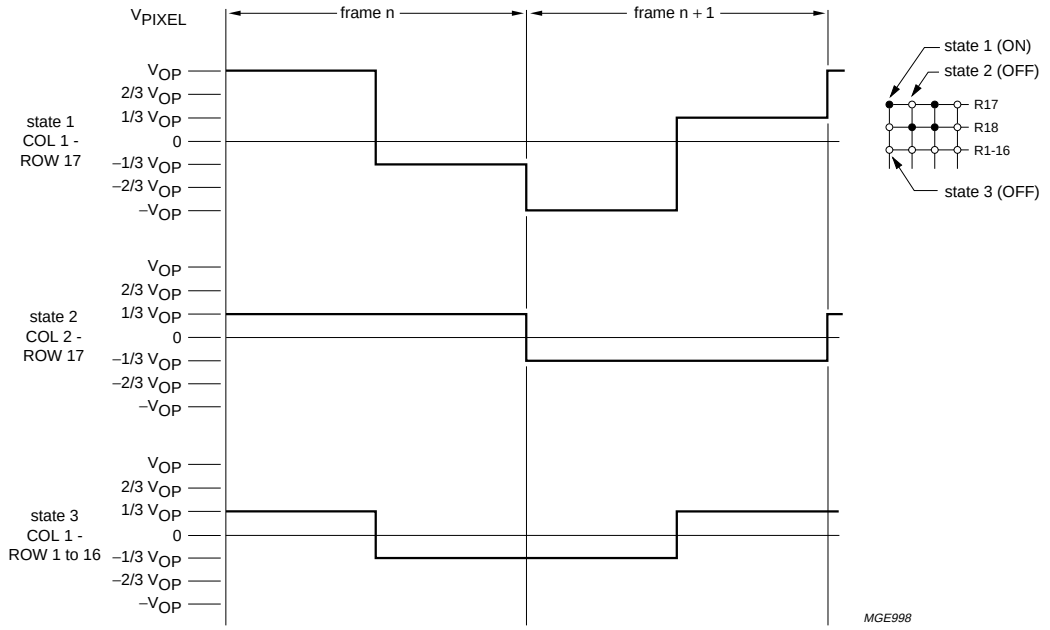


Fig.12 MUX 1 : 2 LCD waveforms; icon mode.



$V_{ON(rms)} = 0.745V_{OP}$

$V_{OFF(rms)} = 0.333V_{OP}$

$D = \frac{V_{ON}}{V_{OFF}} = 2.23$

Fig.13 MUX 1 : 2 LCD waveforms; icon mode.

7.17 Reset function

The PCF2119x must be reset externally when power is turned on. The reset executes a ‘clear display’, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 4.

Table 4 State after reset

STEP	FUNCTION	CONTROL BIT STATE	CONDITION
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
		SL = 0	MUX 1 : 18 mode
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 18 and 19		
6	icon control	IM, IB, DM = 000	icons, icon blink and direct mode disabled
7	display/screen configuration	L = 0; P = 0; Q = 0	default configurations
8	V_{LCD} temperature coefficient	TC1 = 0; TC2 = 0	default temperature coefficient
9	set V_{LCD}	V_A = 0; V_B = 0 (V_{LCD} generator off)	
10	I^2C-bus interface reset		
11	Set HVgen stages	S1, S0 = 10	HVgen set to 3 internal stages (4 * voltage multiplier)

8 INSTRUCTIONS

Only two PCF2119x registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of MPUs which operate at different speeds or to allow interface to peripheral control ICs.
The PCF2119x operation is controlled by the instructions shown in Table 6 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2119x functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the MPU program load.
The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the ‘read busy flag’ and ‘read address’ instructions will be executed. Because the busy flag is set to a logic 1 while an instruction is being executed, check to ensure it is a logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 6. An instruction sent while the busy flag is logic 1 will not be executed.

Table 5 Instruction set for I^2C-bus commands

CONTROL BYTE								COMMAND BYTE								I^2C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 6 Instruction set with parallel bus commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	SL	H	sets interface Data Length (DL) and number of display lines (M); single line/MUX 1 : 9 (SL), extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	A_C							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into the power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command ‘set DDRAM address’; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon control	0	0	0	0	0	0	1	IM	IB	DM	set icon mode (IM), icon blink (IB), direct mode(DM)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set temperature coefficient (TCx)	3
Set HVgen stages	0	0	0	1	0	0	0	0	S1	S0	set internal HVgen stages (S1,S0 = 11 not allowed)	3
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register V_A or V_B (V)	3

Note

1. X = don't care.

Table 7 Explanations of symbols used in Table 6

BIT	STATE	
	LOGIC 0	**LOGIC 1**
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (no impact, if M = 1 or SL = 1)	left/right screen: standard connection (as in PCF2114)	left/right screen: mirrored connection (as in PCF2116)
	1st 16 characters of 32: columns are from 1 to 80	1st 16 characters of 32: columns are from 1 to 80
	2nd 16 characters of 32: columns are from 1 to 80	2nd 16 characters of 32: columns are from 80 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 80	column data: right to left; column data is displayed from 80 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
DM	direct mode disabled	direct mode enabled
V	set V_A	set V_B
M (no impact, if SL = 1)	1-line by 32 display	2-line by 16 display
SL	MUX 1 : 18 (1 × 32 or 2 × 16 character display)	MUX 1 : 9 (1 × 16 character display)
C_0	last control byte; see Table 5	another control byte follows after data/command

Table 8 Explanation of TC1 and TC2 used in Table 6

TC1	TC2	DESCRIPTION
0	0	V_{LCD} temperature coefficient 0
1	0	V_{LCD} temperature coefficient 1
0	1	V_{LCD} temperature coefficient 2
1	1	V_{LCD} temperature coefficient 3; for ranges for TC see Chapter 13

Table 9 Explanation of S1 and S0 used in Table 6

S1	S0	DESCRIPTION
0	0	set internal HVgen stages to 1 (2 * voltage multiplier)
0	1	set internal HVgen stages to 2 (3 * voltage multiplier)
1	0	set internal HVgen stages to 3 (4 * voltage multiplier)
1	1	do not use

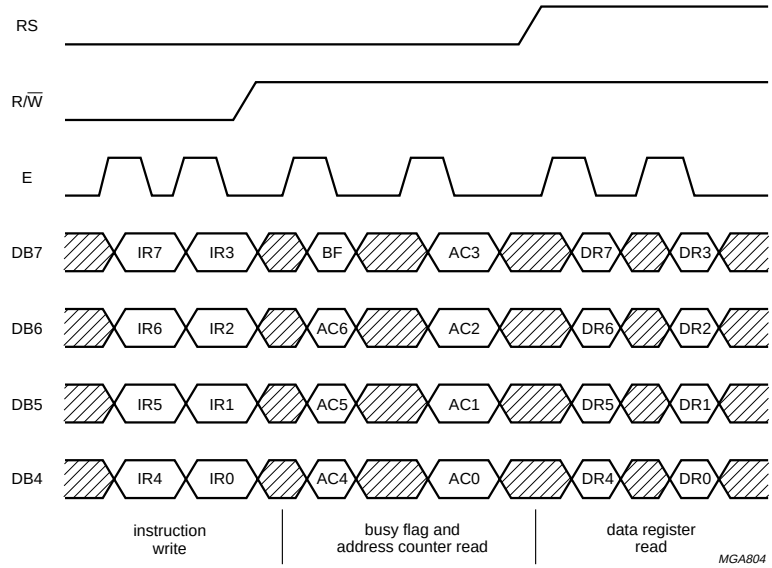
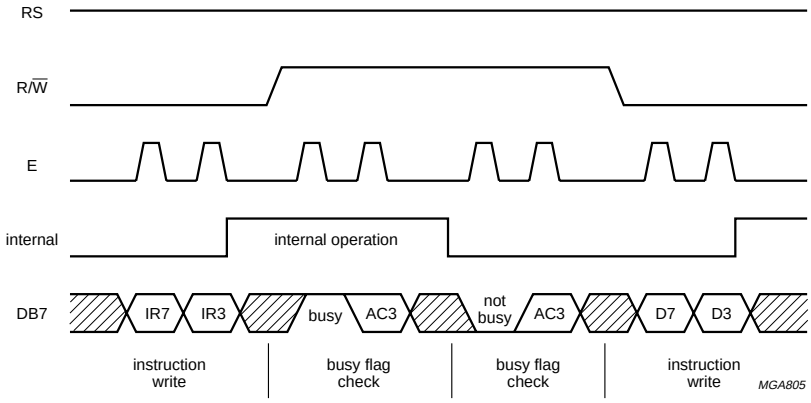


Fig.14 4-bit transfer example.



IR7, IR3: instruction 7th, 3rd bit.
AC3: address counter 3rd bit.
D7, D3: data 7th, 3rd bit.

Fig.15 An example of 4-bit data transfer timing sequence.

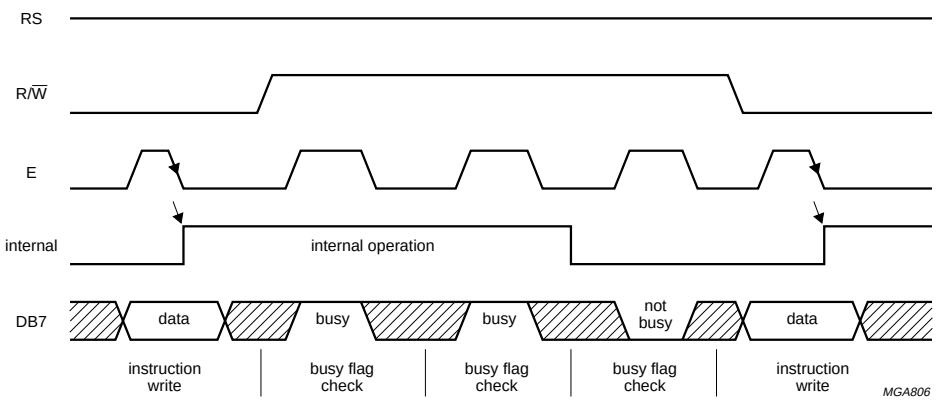


Fig.16 Example of busy flag checking timing sequence.

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = 0, the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to a logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure I_{DD} <1 μA, the parallel bus pads DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open-circuit and PD to V_{DD}. Recovery from power-down mode: PD back to logic 0, if necessary OSC back to V_{DD} and send a 'display control' instruction with D = 1.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second, with $f_{blink} = \frac{f_{OSC}}{52\,224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on M, SL and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set M, SL and H to their required values.

'Function set' from the I^2C-bus interface sets the DL bit to logic 1.

8.6.2 M

Selects either 1-line by 32 display (M = 0) or 2-line by 16 display (M = 1).

8.6.3 SL

Selects MUX 1 : 9, 1-line by 16 display (independent of M and L). Only rows 1 to 8 and 17 are to be used. All other rows must be left open-circuit. The DDRAM map is the same as in the 2-line by 16 display mode, however, the second line is not displayable.

8.6.4 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A5 to A0). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A6 to A0). With the 'set CGRAM address' command, only bits 5 to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A6 to A0). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and read address

'Read busy flag' and 'read address' read the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter expressed in binary A6 to A0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D7 to D0 to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D4 to D0 of CGRAM data are valid, bits D7 to D5 are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D7 to D0 from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while E is HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the data register:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display' and 'return home') do not modify the data register content.

9 EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

9.1 New instructions

H = 1, sets the chip into alternate instruction set mode.

9.2 Icon control

The PCF2119x can drive up to 160 icons. See Fig.17 for CGRAM to icon mapping.

9.3 IM

When IM = 0, the chip is in character mode. In the character mode characters and icons are driven (MUX 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (MUX 1 : 2) and the V_{LCD} voltage generator, if used, produces the V_{LCD} voltage as programmed in register V_B.

9.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0, icon blink is disabled. Icon data is stored in CGRAM character 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons).

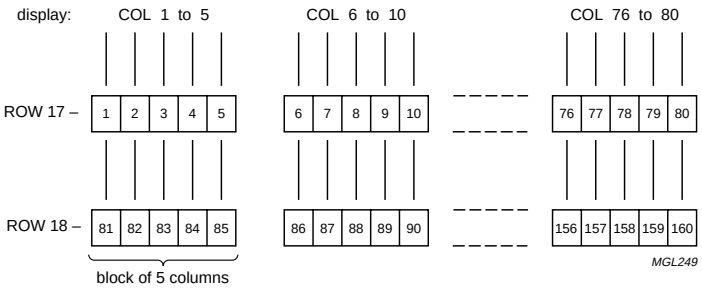
When IB = 1, icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons). These bits also define icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 10 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM character 0 to 2	state 2: CGRAM character 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
76-80	even	17/76-80	0 0 0 0 0 0 0 1	0 0 0 1 1 1 1 1	1 1 1 1 1	
81-85	even	18/1-5	0 0 0 0 0 0 1 0	0 0 1 0 0 0 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	even	18/76-80	0 0 0 0 0 0 1 1	0 0 1 1 1 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	odd (blink)	18/76-80	0 0 0 0 0 1 1 1	0 1 1 1 1 1 1 1	0 0 1 1 0	

MGK999

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 3 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 7 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.17 CGRAM to icon mapping.

9.5 Normal/icon mode operation

IM	CONDITION	V_{LCD}
0	character mode	generates V_A
1	icon mode	generates V_B

9.6 Direct mode

When DM = 0, the chip is not in direct mode. Either the internal voltage generator or an external voltage may be used to achieve the necessary V_{LCD} value.

When DM = 1, the chip is in direct mode. The internal voltage generator is turned off and the V_{LCD} output is directly connected to the HVgen supply voltage V_{DD2}.

The direct mode can be used to reduce the current consumption when the required V_{LCD} output voltage is close to the V_{DD2} supply voltage. This can be the case in icon mode or in Mux 1:9 (depending on LCD liquid properties).

9.7 Voltage multiplier control

S[1:0}

A software configurable voltage multiplier is incorporated and can be set via the “Set HVgen stages” command.

The voltage multiplier control can be used to reduce current consumption by disconnecting internal voltage multiplier stages (depending on the required V_{LCD} output voltage).

9.8 Screen configuration

L: default is L = 0.

L = 0: the two halves of a split screen are connected in a standard way i.e. column 1/81, 2/82 to 80/160.

L = 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/160, 2/159 to 80/81. This allows single layer PCB or glass layout.

9.9 Display configuration

P, Q: default is P, Q = 0.

P = 1: mirrors the column data.

Q = 1: mirrors the row data.

9.10 TC1 and TC2

Default is TC1 and TC2 = 0. This selects the default temperature coefficient for the internally generated V_{LCD}. TC1 and TC2 = 10, 01 and 11 selects alternative temperature coefficients 1, 2 and 3 respectively.

9.11 Set V_{LCD}

The V_{LCD} value is programmed by instruction. Two on-chip registers hold V_{LCD} values for the character mode and the icon mode respectively (V_A and V_B). The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip.

V_{LCD} programming:

1. Send ‘function set’ instruction with H = 1
2. Send ‘set V_{LCD}’ instruction to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During ‘display off’ and power-down the V_{LCD} generator is also disabled.
3. Send ‘function set’ instruction with H = 0 to resume normal programming.

9.12 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 11.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 11 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	Icon mode (control bit IM)
Display on	Display off (control bit D)
HV generator operating	Direct mode
Any mode	Power-down (PD pad)

Table 12 Use of the V_A and V_B registers

MODE	V_A	V_B
Normal operation	V_{LCD} character mode	V_{LCD} icon mode

10 INTERFACES TO MPU

10.1 Parallel interface

The PCF2119x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Section 6.1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pads DB7 to DB4 for the transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction, see Figs 14 to 16 for examples of bus protocol.

In 4-bit mode, pads DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

10.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

10.2.1 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C-bus configuration for the different PCF2119x read and write cycles is shown in Figs 22 to 24. The slow down feature of the I²C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the PCF2119x.

10.2.2 DEFINITIONS

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

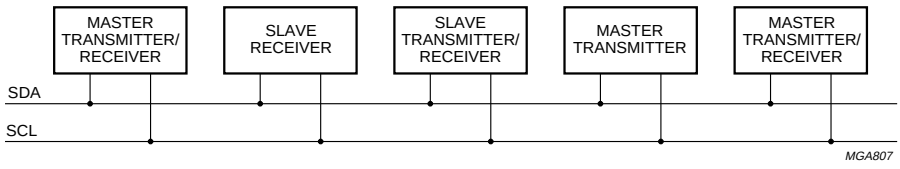


Fig.18 System configuration.

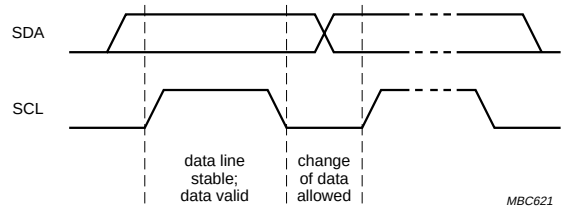


Fig.19 Bit transfer.

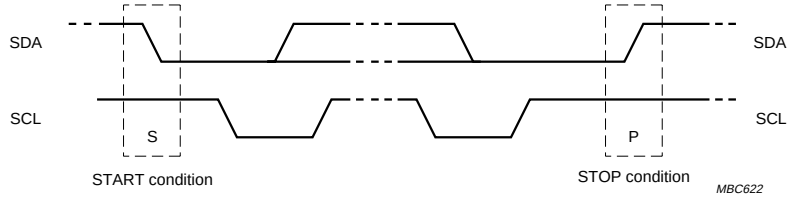


Fig.20 Definition of START and STOP conditions.

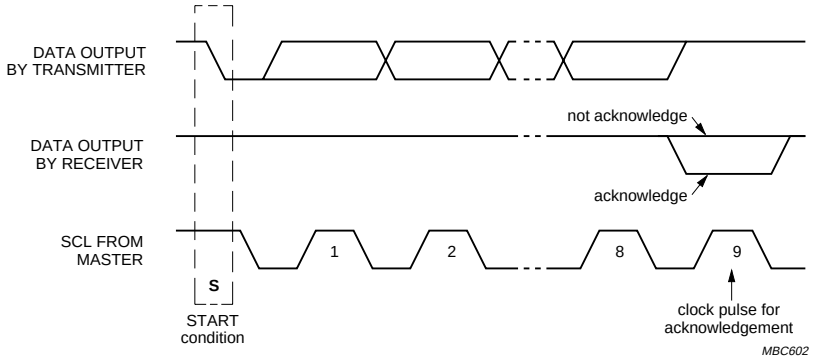


Fig.21 Acknowledgement on the I^2C-bus.

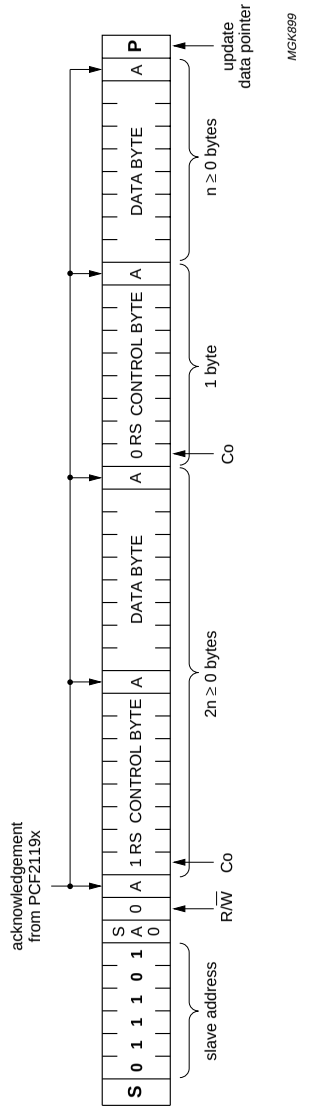


Fig.22 Master transmits to slave receiver; write mode.

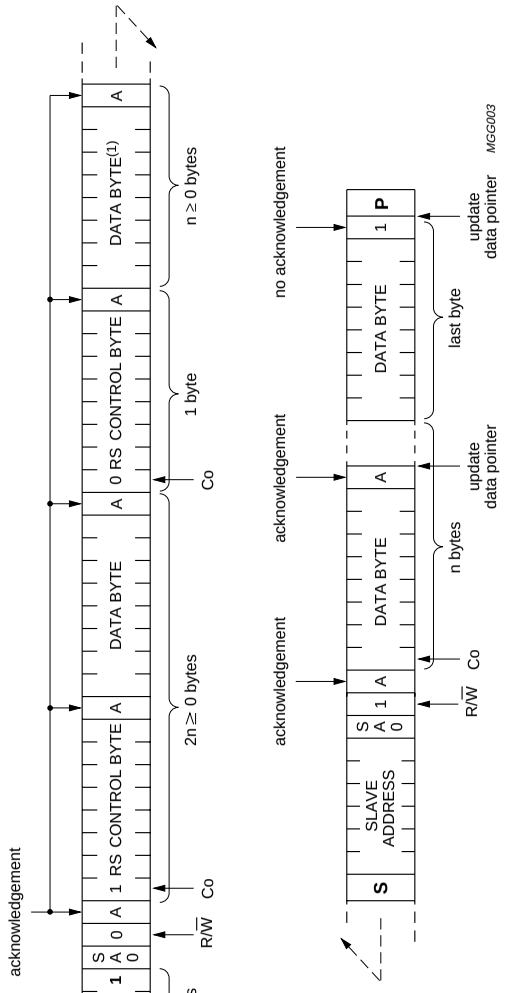


Fig.23 Master reads after setting word address; writes word address, set RS; 'read data'.

(1) Last data byte is a dummy byte (may be omitted).

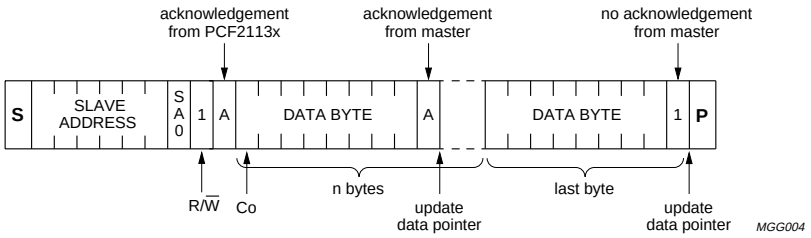


Fig.24 Master reads slave immediately after first byte; read mode (RS previously defined).

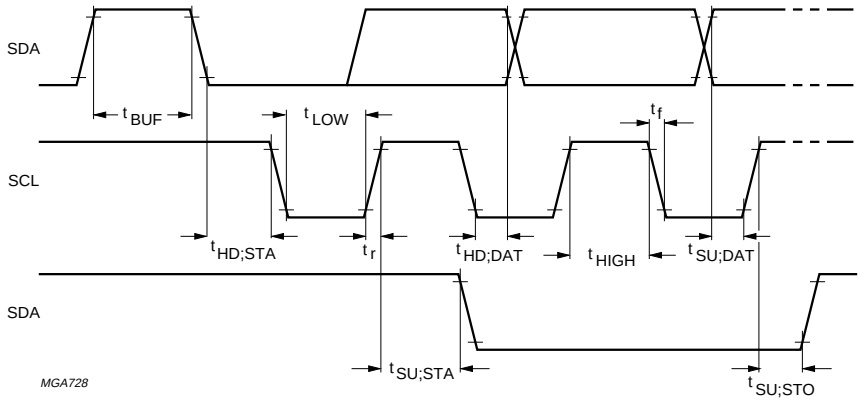


Fig.25 I^2C-bus timing diagram.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	Logic supply voltage	–0.5	+6.5	V
$V_{DD2,3}$	High voltage generator supply voltages	–0.5	+4.5	V
V_{LCD}	LCD supply voltage	–0.5	+7.5	V
$V_{I(VDD)}$ / $V_{O(VDD)}$	input/output voltage (any V_{DD} related input/output)	–0.5	V_{DD} + 0.5	V
$V_{I(VLCD)}$ / $V_{O(VLCD)}$	input/output voltage (any V_{LCD} related input/output)	–0.5	V_{LCD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	$V_{DD1,2,3}$, $V_{SS1,2}$ or V_{LCD} current	–50	+50	mA
V_{HMB}	electrostatic handling voltage according Human Body Model (C=100pF, R=1.5kOhm)		1.8	kV
V_{MM}	electrostatic handling voltage according Machine Model(c=200pF, L=0.75uH)		150	V
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

12 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

13 DC CHARACTERISTICS

V_{DD1} = 1.5 to 5.5 V; $V_{DD2,3}$ = 2.2 to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	Logic supply voltage		1.5	–	5.5	V
$V_{DD2,3}$	High voltage generator supply voltages	internal V_{LCD} generation ($V_{DD2,3} < V_{LCD}$)	2.2	–	4.0	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	**ground supply current**	**external V_{LCD}**; note 1				
I_{SS1}	ground supply current 1		–	70	120	µA
I_{SS3}	ground supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	35	80	µA
I_{SS4}	ground supply current 4	icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	25	45	µA
I_{SS5}	ground supply current 5	power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	0.5	5	µA
I_{SS}	**ground supply current**	**internal V_{LCD}**; note 1and 3				
I_{SS6}	ground supply current 6		–	190	400	µA
I_{SS8}	ground supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	135	400	µA
I_{SS9}	ground supply current 9	icon mode; V_{DD} = 2.5 V; V_{LCD} = 2.5 V; note 2	–	85	–	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
$V_{IL(osc)}$	LOW-level input voltage pad OSC	V_{DD} = V_{DDmin}, V_{DDmax}	V_{SS1}	–	V_{DD1} – 1.2	V
$V_{IH(osc)}$	HIGH-level voltage pad OSC	V_{DD} = V_{DDmin}, V_{DDmax}	V_{DD1} – 0.1	–	V_{DD1}	V
$I_{OL(DB)}$	LOW-level output current pads DB7 to DB0	V_{OL} = 0.4 V; V_{DD1} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current pads DB7 to DB0	V_{OH} = 4 V; V_{DD1} = 5 V	–1	–8	–	mA
I_{pu}	pull-up current pads DB7 to DB0	V_I = V_{SS1}, V_{DDmin}, V_{DDmax}	0.04	0.15	1	µA
I_L	leakage current	V_I = $V_{DD1,2,3}$ or $V_{SS1,2}$	–1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL2}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	μA
C_i	input capacitance		–	5	-	pF
$I_{OL\ (SDA)}$	low-level output current SDA	V_{OL} = 0.4 V ; $V_{DD} > 2V$ $V_{OL} = 0.2V_{DD}$; $V_{DD} < 2V$	3 2			mA mA
LCD outputs						
$R_{O(ROW)}$	row output resistance pads R1 to R18	note 4	–	10	30	kΩ
$R_{O(COL)}$	column output resistance pads C1 to C80	note 4	–	15	40	kΩ
$V_{bias(tol)}$	bias tolerance pads R1 to R18 and C1 to C80	note 5	–	20	130	mV
$V_{VLCD(tol)}$	V_{LCD} tolerance	T_{amb} = 25 °C; note 3 $V_{LCD} < 3$ V $V_{LCD} < 4$ V $V_{LCD} < 5$ V $V_{LCD} < 6$ V	 – – – –	 – – – –	 160 200 260 340	 mV mV mV mV
TC0	V_{LCD} temperature coefficient 0		–	–0.16	–	%/K
TC1	V_{LCD} temperature coefficient 1		–	–0.18	–	%/K
TC2	V_{LCD} temperature coefficient 2		–	–0.21	–	%/K
TC3	V_{LCD} temperature coefficient 3		–	–0.24	–	%/K

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
3. LCD outputs are open-circuit; HV generator is on; load current I_{VLCD} (at V_{LCD}) = 5 μA.
4. Resistance of output terminals (R1 to R18 and C1 to C80) with a load current of 10 μA; outputs measured one at a time; external V_{LCD} ; V_{LCD} = 3 V, $V_{DD1,2,3}$ = 3 V.
5. LCD outputs open-circuit; external V_{LCD}.

14 AC CHARACTERISTICS

V_{DD1} = 1.5 to 5.5 V; $V_{DD2,3}$ = 2.2 to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	95	147	Hz
f_{OSC}	oscillator frequency (not available at any pad)		140	250	450	kHz
$f_{OSC(ext)}$	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after power-down	note 3	–	200	300	µs
$t_{W(R,PD)}$	reset and power down high level pulse width		1			us
$t_{SW(R,PD)}$	tolerable spike width on PD and Reset pads				90	ns
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MPU TO PCF2119x)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2119X TO MPU)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time	V_{DD1} > 2.2 V	–	–	150	ns
		V_{DD1} > 1.5 V	–	–	250	ns
$t_{h(D)}$	data hold time		5	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock high period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL, SDA rise time	note 2, 3	15 + 0.1 C_B	–	300	ns
t_f	SCL, SDA fall time	note 2, 3	15 + 0.1 C_B	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	Bus free time between STOP and START condition		1.3			us

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. C_B = total capacitance of one bus line in pF.
3. Tested on a sample basis.

15 TIMING CHARACTERISTICS

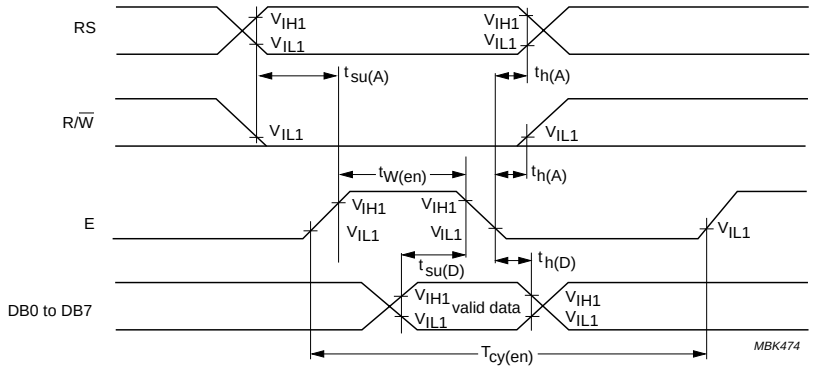


Fig.26 Parallel bus write operation sequence; writing data from MPU to PCF2119x.

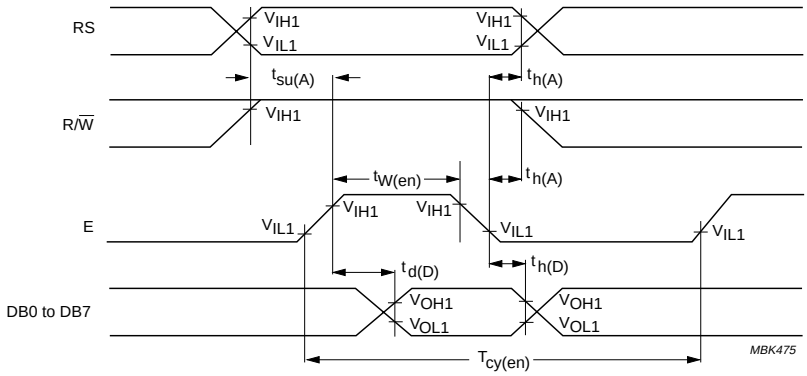


Fig.27 Parallel bus read operation sequence; reading data from PCF2119x to MPU.

16 APPLICATION INFORMATION

16.1 General application information

The required minimum value for the external capacitors in an application with the PCF2119x-2 are:

C_{ext} for $V_{LCD}/V_{SS1,2}$ = min. 100nF, for $V_{DD1,2,3}$ / $V_{SS1,2}$ = 470nF.

Higher capacitor values are recommended for ripple reduction.

For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections. Optimized values for these tracks are below 50 Ohm for the supply and below 100 Ohm for the I/O connections. Higher track resistance reduces performance and increase current consumption.

To avoid accidental triggering of power-on reset (especially in COG applications), the supplies must be adequately decoupled. Depending on power supply quality, V_{DD1} may have to be rised above the specified minimum.

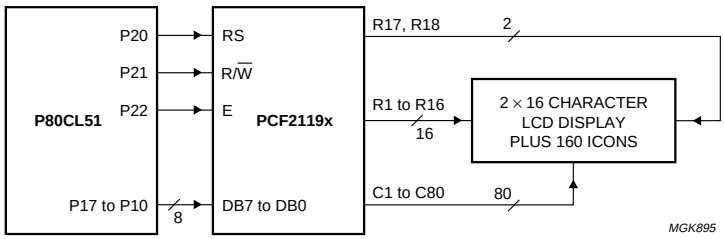


Fig.28 Direct connection to 8-bit MPU; 8-bit bus.

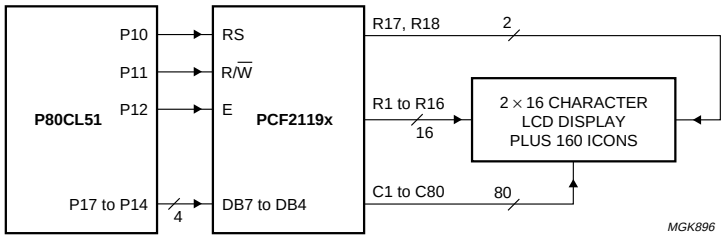


Fig.29 Direct connection to 8-bit MPU; 4-bit bus.

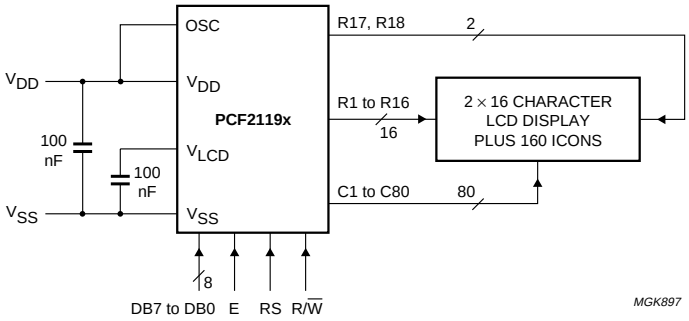


Fig.30 Typical application using parallel interface.

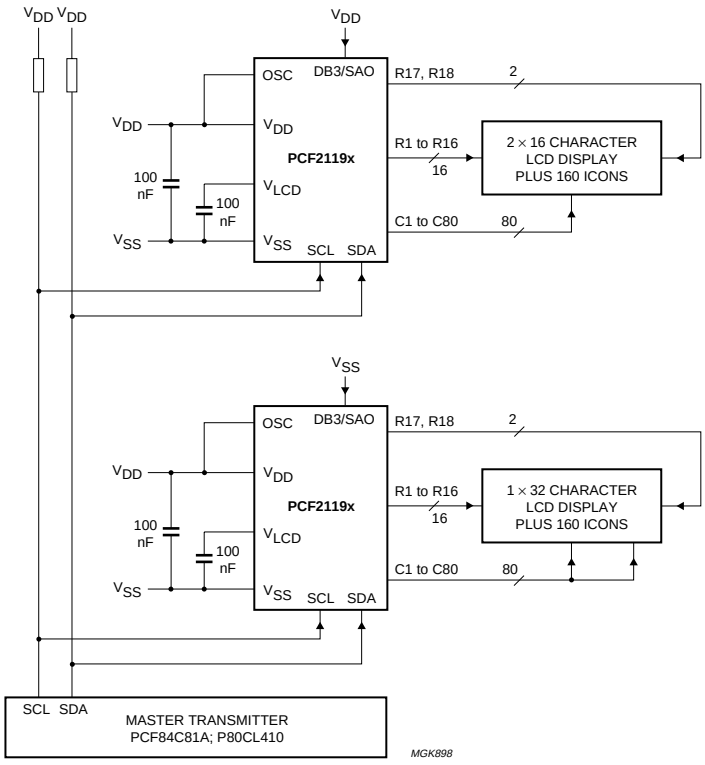


Fig.31 Application using I²C-bus interface.

16.2 Charge pump characteristic

In Fig. 32 - 34 typical graphs of the total power consumption of the PCF2119-2 using the internal charge pump are given. They are obtained under the following conditions :

- ambient temperature 25C
- $V_{DD1} = V_{DD2} = V_{DD3}$ = 2.2 (min), 2.7 (typ), 4V (max)
- normal mode
- Fosc = internal oscillator
- MUX 1:18
- typical load current I_{VLCD} = 10 uA

For each multiplication factor there is a separate line. A line ends where it is not possible to get a higher voltage under its conditions (a higher multiplication factor is needed to get higher voltages).

Connecting different displays may result in different current consumptions. This affects the efficiency and the optimal multiplication factor to be used to generate a certain output voltage.

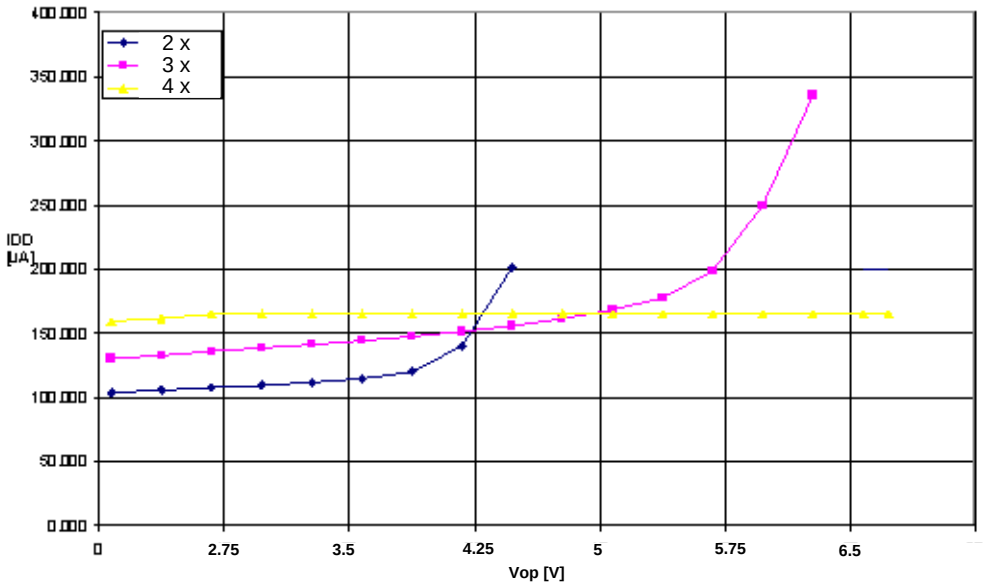


Fig.32 Typical charge pump characteristic for V_{DD} = 2.2 V.

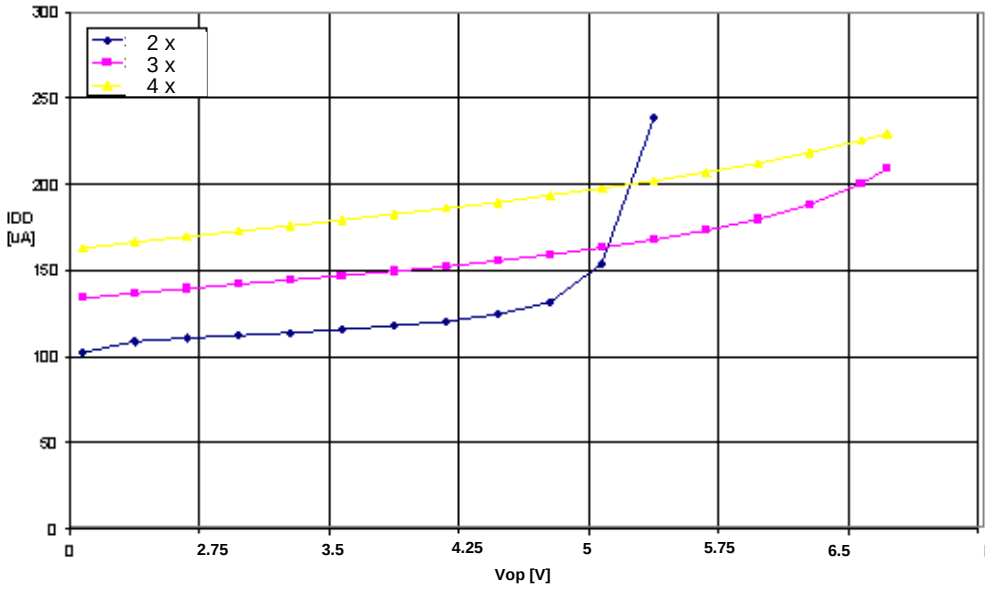


Fig.33 Typical charge pump characteristic for V_{DD} = 2.7 V.

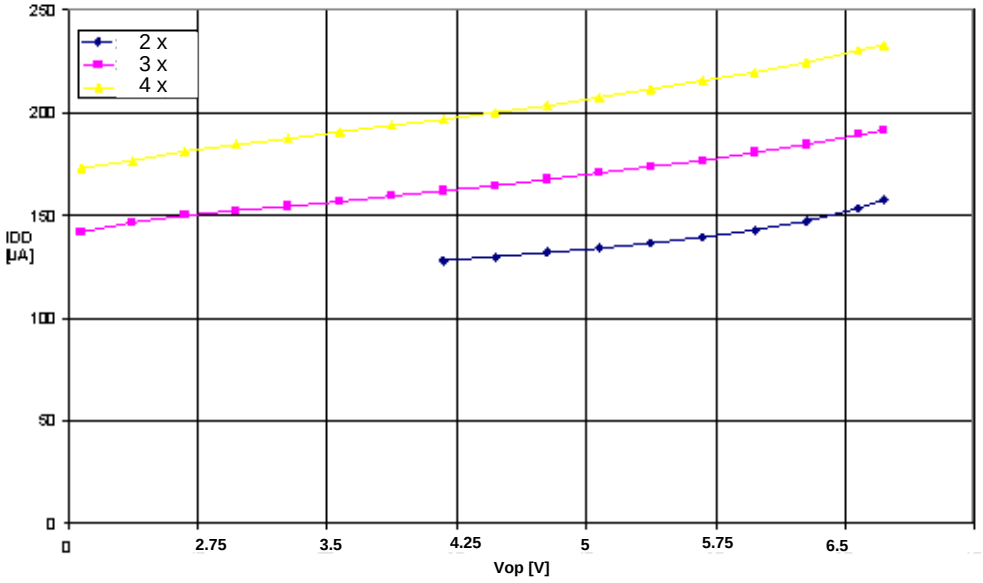


Fig.34 Typical charge pump characteristic for V_{DD} = 4 V.

16.3 8-bit operation, 1-line display using external reset

Table 14 shows an example of a 1-line display in 8-bit operation. The PCF2119x functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

16.4 4-bit operation, 1-line display using external reset

The program must set functions prior to a 4-bit operation, see Table 13. When power is turned on, 8-bit operation is automatically selected and the PCF2119x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 13 step 3). Thus, DB4 to DB7 of the 'function set' are written twice.

16.5 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 6). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

16.6 I^2C-bus operation, 1-line display

A control byte is required with most commands (see Table 17).

Table 13 4-bit operation, 1-line display example; using external reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 14 8-bit operation, 1-line display example; using external reset (character set ‘A’)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes ‘H’
7 to 11			
12	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes ‘S’
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
14	‘write data’ to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
15	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes ‘M’
16			

STEP	INSTRUCTION	DISPLAY	OPERATION
17	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	writes ‘O’
18	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROK<u>O</u>**	shifts only the cursor position to the left
19	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICRO<u>K</u>O**	shifts only the cursor position to the left
20	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROC<u>O</u>**	writes ‘C’ correction; the display moves to the left
21	cursor/display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	shifts the display and cursor to the right
22	cursor/display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
23	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes ‘M’
24			
25	return home 0 0 0 0 0 0 0 0 1 0	**<u>P</u>HILIPS M**	returns both display and cursor to the original position (address 0)

Table 15 8-bit operation, 1-line display and icon example; using external reset (character set ‘A’)

STEP	INTRODUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	‘write data’ to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appears
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	‘write data’ to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INTRODUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the cursor is incremented by 1 and shifted to the right
16	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes ‘H’
17 to 20		|	
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 16 8-bit operation, 2-line display example; using external reset

STEP	INTRODUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 1 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10		|	
11	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes ‘S’
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	‘write data’ to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes ‘M’
14 to 19		|	

STEP	INTRODUCTION	DISPLAY	OPERATION
20	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS MICROCO_**	writes ‘O’
21	‘write data’ to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS MICROCO_**	sets mode for display shift at the time of write
22	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**HILIPS ICROCOM_**	writes ‘M’; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS MICROCOM**	returns both display and cursor to the original position (address 0)

Table 17 Example of I²C-bus operation; 1-line display (using external reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2119x
3	send a control byte for ‘function set’ Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for ‘write data’ Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	**P**_	writes ‘P’; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
11	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH**_	writes ‘H’

STEP	I²C BYTE	DISPLAY	OPERATION
12 to 15		| | | |	
16	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS**_	writes ‘S’
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS**_	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS**_	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a ‘set address’ nor a ‘read data’ has been performed; therefore the content of the DR was unknown; the R/W has to be set to 1 while still in I²C-write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions
23	‘read data’: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface

STEP	I^2C BYTE	DISPLAY	OPERATION
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I^2C interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	no master acknowledge; after the content of the I^2C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted
26	I^2C stop	**PHILIPS**	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 18 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after external reset has been applied										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait more than 40 μs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					↓					
Initialization ends										

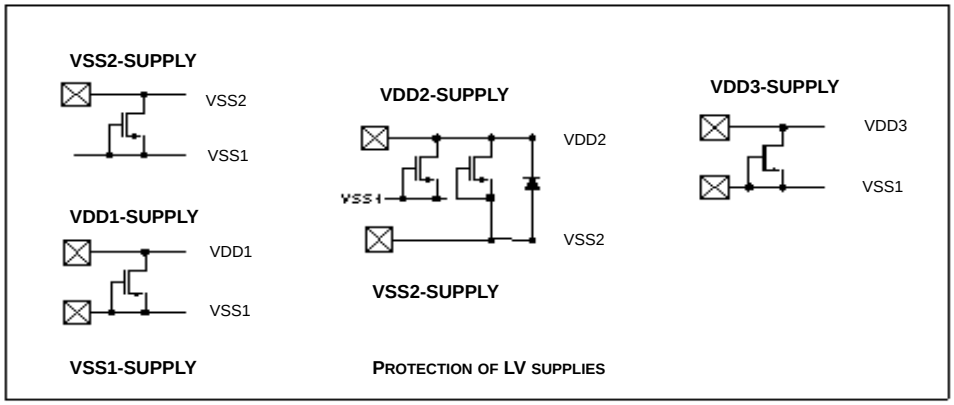
Note

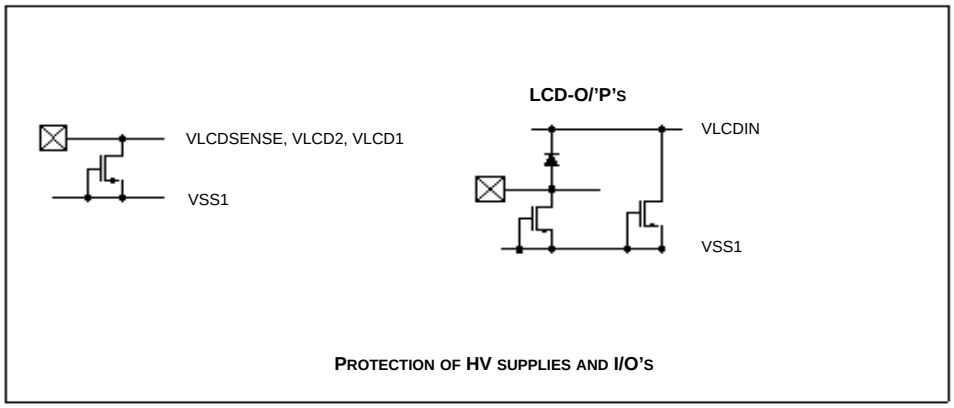
1. X = don't care.

Table 19 Initialization by instruction, 4-bit interface; not applicable for I^2C-bus operation

STEP						DESCRIPTION
power-on or unknown state						
			|			
Wait 2 ms after external reset has been applied						
			|			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			|			
Wait 2 ms						
			|			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			|			
Wait 40 μs						
			|			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			|			BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
			|			
Initialization ends						

17 DEVICE PROTECTION DIAGRAM





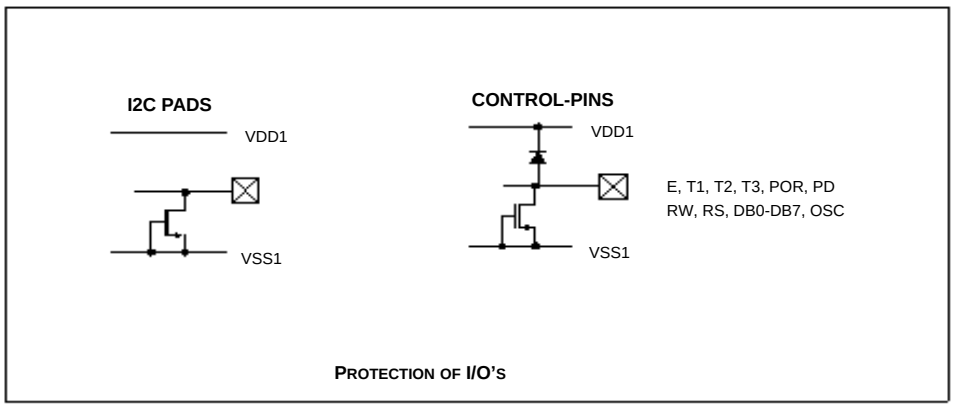
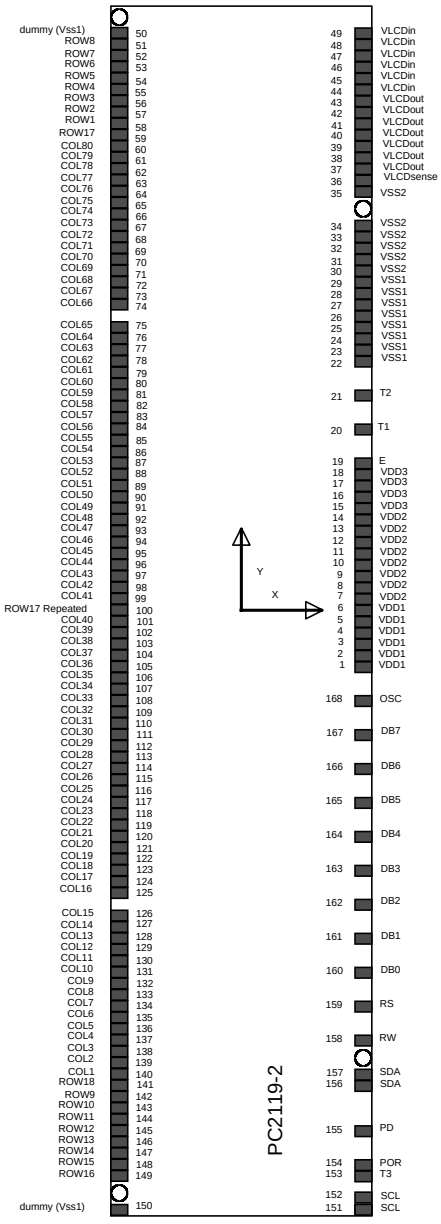


Fig.35 ESD protection diagram

18 BONDING PAD LOCATIONS



Chip size : 1.81 mm x 7.64 mm

Fig.36 Bonding pad locations.

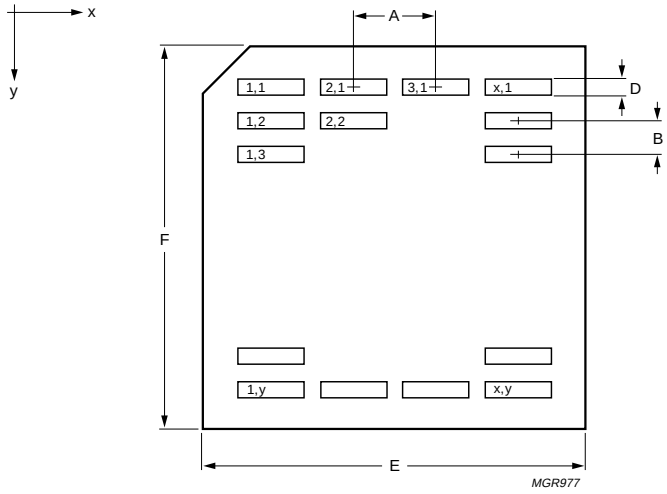
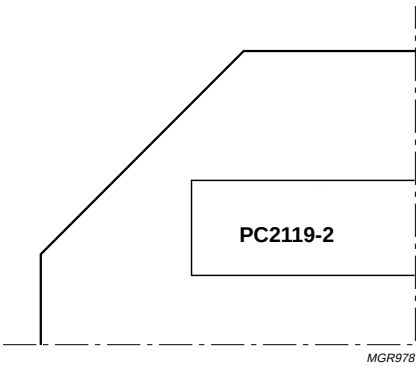


Fig.37 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.38 Tray alignment.

Table 20 Dimensions for Fig.37

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	10.16 mm
B	pocket pitch, y direction	4.45 mm
C	pocket width, x direction	7.74 mm
D	pocket width, y direction	1.91 mm
E	tray width, x direction	50.8 mm
F	tray width, y direction	50.8 mm
x	number of pockets in x direction	4
y	number of pockets in y direction	10

Table 21 Bonding pad locations
Dimensions in µm; all x/y coordinates are referenced to centre of chip; see Fig.36

SYMBOL	PAD	x	y
V_{DD1}	1	745	- 274
V_{DD1}	2	745	– 204
V_{DD1}	3	745	- 134
V_{DD1}	4	745	- 64
V_{DD1}	5	745	6
V_{DD1}	6	745	76
V_{DD2}	7	745	146
V_{DD2}	8	745	216
V_{DD2}	9	745	286
V_{DD2}	10	745	356
V_{DD2}	11	745	426
V_{DD2}	12	745	496
V_{DD2}	13	745	566
V_{DD2}	14	745	636
V_{DD3}	15	745	706
V_{DD3}	16	745	776
V_{DD3}	17	745	846
V_{DD3}	18	745	916
E	19	745	986
T1	20	745	1196
T2	21	745	1406
V_{SS1}	22	745	1616
V_{SS1}	23	745	1686
V_{SS1}	24	745	1756
V_{SS1}	25	745	1826
V_{SS1}	26	745	1896
V_{SS1}	27	745	1966
V_{SS1}	28	745	2036
V_{SS1}	29	745	2106
V_{SS2}	30	745	2176
V_{SS2}	31	745	2246
V_{SS2}	32	745	2316
V_{SS2}	33	745	2386
V_{SS2}	34	745	2456
V_{SS2}	35	745	2666
$V_{LCDSENSE}$	36	745	2736
V_{LCD2}	37	745	2806
V_{LCD2}	38	745	2876
V_{LCD2}	39	745	2946
V_{LCD2}	40	745	3016
V_{LCD2}	41	745	3086
V_{LCD2}	42	745	3156
V_{LCD2}	43	745	3226
V_{LCD1}	44	745	3296
V_{LCD1}	45	745	3366

SYMBOL	PAD	x	y
V_{LCD1}	46	745	3436
V_{LCD1}	47	745	3506
V_{LCD1}	48	745	3576
V_{LCD1}	49	745	3646
Dummy (V_{SS1})	50	- 745	3576
R8	51	- 745	3506
R7	52	- 745	3436
R6	53	- 745	3366
R5	54	- 745	3296
R4	55	- 745	3226
R3	56	- 745	3156
R2	57	- 745	3086
R1	58	- 745	3016
R17	59	- 745	2946
C80	60	- 745	2876
C79	61	- 745	2806
C78	62	- 745	2736
C77	63	- 745	2666
C76	64	- 745	2596
C75	65	- 745	2526
C74	66	- 745	2456
C73	67	- 745	2386
C72	68	- 745	2316
C71	69	- 745	2246
C70	70	- 745	2176
C69	71	- 745	2106
C68	72	- 745	2036
C67	73	- 745	1966
C66	74	- 745	1896
C65	75	- 745	1756
C64	76	- 745	1686
C63	77	- 745	1616
C62	78	- 745	1546
C61	79	- 745	1476
C60	80	- 745	1406
C59	81	- 745	1336
C58	82	- 745	1266
C57	83	- 745	1196
C56	84	- 745	1126
C55	85	- 745	1056
C54	86	- 745	986
C53	87	- 745	916
C52	88	- 745	846
C51	89	- 745	776
C50	90	- 745	706

SYMBOL	PAD	x	y
C49	91	- 745	636
C48	92	- 745	566
C47	93	- 745	496
C46	94	- 745	426
C45	95	- 745	356
C44	96	- 745	286
C43	97	- 745	216
C42	98	- 745	146
C41	99	- 745	76
R17DUP	100	- 745	6
C40	101	- 745	- 64
C39	102	- 745	- 134
C38	103	- 745	- 204
C37	104	- 745	- 274
C36	105	- 745	- 344
C35	106	- 745	- 414
C34	107	- 745	- 484
C33	108	- 745	- 554
C32	109	- 745	- 624
C31	110	- 745	- 694
C30	111	- 745	- 764
C29	112	- 745	- 834
C28	113	- 745	- 904
C27	114	- 745	- 974
C26	115	- 745	- 1044
C25	116	- 745	- 1114
C24	117	- 745	- 1184
C23	118	- 745	- 1254
C22	119	- 745	- 1324
C21	120	- 745	- 1394
C20	121	- 745	- 1464
C19	122	- 745	- 1534
C18	123	- 745	- 1604
C17	124	- 745	- 1674
C16	125	- 745	- 1744
C15	126	- 745	- 1884
C14	127	- 745	- 1954
C13	128	- 745	- 2024
C12	129	- 745	- 2094
C11	130	- 745	- 2164
C10	131	- 745	- 2234
C9	132	- 745	- 2304
C8	133	- 745	- 2374
C7	134	- 745	- 2444
C6	135	- 745	- 2514
C5	136	- 745	- 2584
C4	137	- 745	- 2654
C3	138	- 745	- 2724
C2	139	- 745	- 2794

SYMBOL	PAD	x	y
C1	140	- 745	- 2864
R18	141	- 745	- 2934
R9	142	- 745	- 3004
R10	143	- 745	- 3074
R11	144	- 745	- 3144
R12	145	- 745	- 3214
R13	146	- 745	- 3284
R14	147	- 745	- 3354
R15	148	- 745	- 3424
R16	149	- 745	- 3494
Dummy (V_{SS1})	150	- 745	- 3704
SCL	151	745	- 3704
SCL	152	745	- 3634
T3	153	745	- 3494
POR	154	745	- 3424
PD	155	745	- 3214
SDA	156	745	- 3004
SDA	157	745	- 2934
R/$\overline{W}$	158	745	- 2584
RS	159	745	- 2374
DB0	160	745	- 2164
DB1	161	745	- 1954
DB2	162	745	- 1744
DB3 / SA0	163	745	- 1534
DB4	164	745	- 1324
DB5	165	745	- 1114
DB6	166	745	- 904
DB7	167	745	- 694
OSC	168	745	- 484
Rec. Pat. 1	169	745	- 2689
Rec. Pat. 2	169	745	2561
Rec. Pat. 3	169	-745	3681
Rec. Pat. 4	170	-745	- 3599

Table 22 Bump size

PARAMETER	VALUE	UNIT
Type	galvanic pure Au	–
Bump width	50 ±6	µm
Bump length	90 ±6	µm
Bump height	17.5 ±5	µm
Height difference in one die	<2	µm
Convex deformation	<5	µm
Pad size, aluminium	62 × 100	µm
Passivation opening CBB	36 × 76	µm
Wafer thickness	380 ±25	µm