19-0143; Rev 1; 2/95

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

Digitally Adjustable LCD Bias Supply

MAX749

General Description

The MAX749 generates negative LCD-bias contrast voltages from 2V to 6V inputs. Full-scale output voltage can be scaled to -100V or greater, and is digitally adjustable in 64 equal steps by an internal digital-to-analog converter (DAC). Only seven small surface-mount components are required to build a complete supply. The output voltage can also be adjusted using a PWM signal or a potentiometer.

A unique current-limited control scheme reduces supply current and maximizes efficiency, while a high switching frequency (up to 500kHz) minimizes the size of external components. Quiescent current is only 60µA max and is reduced to under 15µA in shutdown mode. While shut down, the MAX749 retains the voltage set point, simplifying software control. The MAX749 drives either an external P-channel MOSFET or a PNP transistor.

Features

- **+2.0V to +6.0V Input Voltage Range**
- **Flexible Control of Output Voltage:**
  - **Digital Control**
  - **Potentiometer Adjustment**
  - **PWM Control**
- **Output Voltage Range Set by One Resistor**
- **Low, 60µA Max Quiescent Current**
- **15µA Max Shutdown Mode**
- **Small Size – 8-Pin SO and Plastic DIP Packages**

Applications

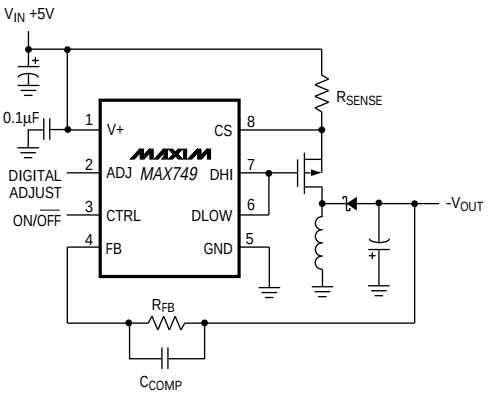
Notebook Computers
Laptop Computers
Palmtop Computers
Personal Digital Assistants
Communicating Computers
Portable Data-Collection Terminals

Ordering Information

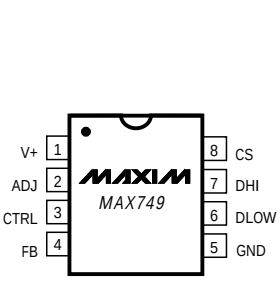
PART	TEMP. RANGE	PIN-PACKAGE
MAX749CPA	0°C to +70°C	8 Plastic DIP
MAX749CSA	0°C to +70°C	8 SO
MAX749C/D	0°C to +70°C	Dice*
MAX749EPA	-40°C to +85°C	8 Plastic DIP
MAX749ESA	-40°C to +85°C	8 SO

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



DIP/SO

ABSOLUTE MAXIMUM RATINGS

V+ .....-0.3V, +7V
CTRL, ADJ, FB, DLOW, DHI, CS.....-0.3V, (V+ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW

Operating Temperature Ranges:
MAX749C_A.....0°C to +70°C
MAX749E_A.....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(2V < V+ < 6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Voltage			2		6	V
FB Source Current	I_{FBS}	On power-up or reset, V_{FB} = 0V (Note 1)	12.80	13.33	13.86	µA
Zero-Count FB Current		V_{FB} = 0V	0.45		0.55	I_{FBS}
Full-Count FB Current		V_{FB} = 0V	1.43		1.53	I_{FBS}
FB Offset Voltage					±15	mV
DAC Step Size (Note 2)		Monotonicity guaranteed, V_{FB} = 0V	1.00	1.56	2.12	%I_{FBS}
DAC Linearity (Note 2)		V_{FB} = 0V			±1	%I_{FBS}
Supply Rejection		V+ = 2V to 6V, full-count current			1.5	%I_{FBS}
Switching Frequency				100 to 500		kHz
Logic Input Current		0V < V_{IN} < V+, CTRL, ADJ			±100	nA
Logic High Threshold (Note 3)	V_{IH}	CTRL, ADJ	1.6			V
Logic Low Threshold (Note 3)	V_{IL}	CTRL, ADJ			0.4	V
Quiescent Current					60	µA
Shutdown Current					15	µA
V+ to CS Voltage		Current-limit trip voltage	110	140	180	mV
DHI Source Current		V+ = 2V, V_{DHI} = 1V	24	50		mA
DHI Drive Level		No load	V+ - 50mV	V+		V
DLOW On Resistance		V+ = 2V, V_{DLOW} = 0.5V		5	10	Ω

Note 1: The device is in regulation when V_{FB} = 0V (see Figures 3 - 6).
Note 2: These tests performed at V+ = 3.3V. Operation over supply range is guaranteed by supply rejection test of full-count current.
Note 3: V_{IH} is guaranteed by design to be 1.8V min for V+ = 2V to 6V for $T_A = T_{MIN}$ to T_{MAX}. V_{IL} is guaranteed by design from $T_A = T_{MIN}$ to T_{MAX}.

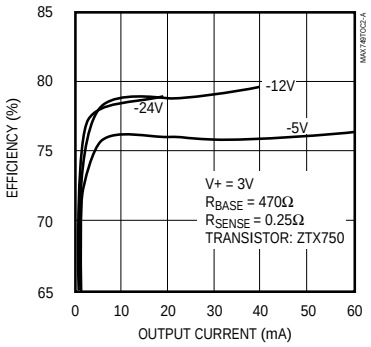
TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C MIN	T_A = +25°C TYP	T_A = +25°C MAX	$T_A = T_{MIN}$ to T_{MAX} MIN	$T_A = T_{MIN}$ to T_{MAX} MAX	UNITS
Minimum Reset Pulse Width	t_R	V+ = 2V		125	300		400	ns
		V+ = 5V		25	85		100	
Minimum Reset Setup	t_{RS}	Not tested	0			0		ns
Minimum Reset Hold	t_{RH}	Not tested	0			0		ns
Minimum ADJ High Pulse Width	t_{SH}	V+ = 2V		15	85		100	ns
		V+ = 5V		10	85		100	
Minimum ADJ Low Pulse Width	t_{SL}	V+ = 2V		170	400		500	ns
		V+ = 5V		60	150		200	
Minimum ADJ Low to CTRL Low	t_{SD}	V+ = 2V		70	200		250	ns
		V+ = 5V		20	85		100	

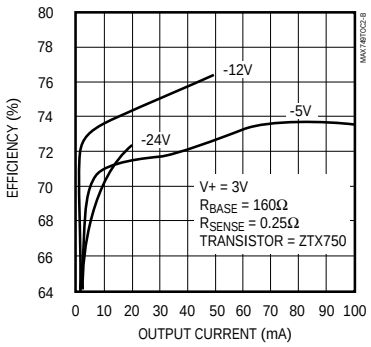
Typical Operating Characteristics

(T_A = +25°C, L = 47µH, unless otherwise noted.)

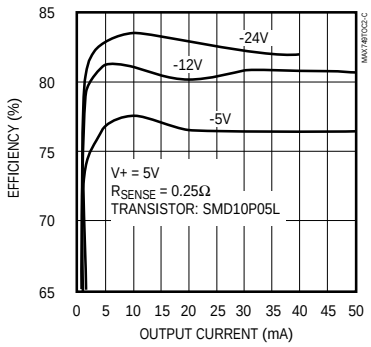
EFFICIENCY vs. OUTPUT CURRENT – PNP



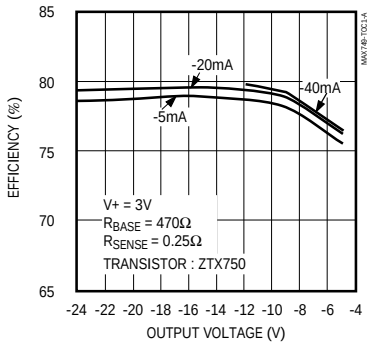
EFFICIENCY vs. OUTPUT CURRENT – PNP



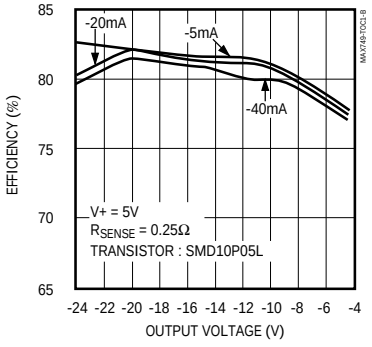
EFFICIENCY vs. OUTPUT CURRENT – MOSFET



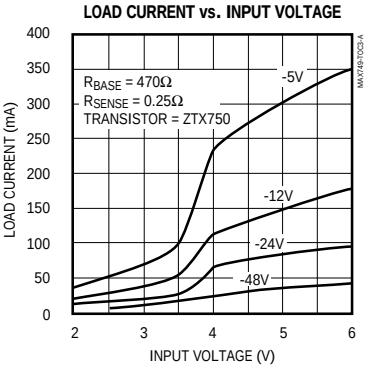
EFFICIENCY vs. OUTPUT VOLTAGE



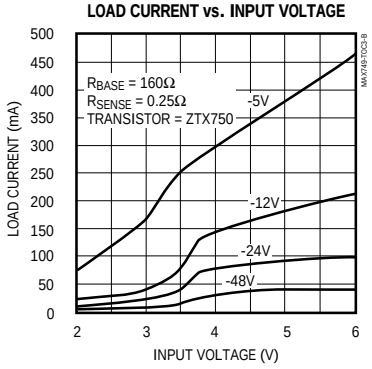
EFFICIENCY vs. OUTPUT VOLTAGE



LOAD CURRENT vs. INPUT VOLTAGE



LOAD CURRENT vs. INPUT VOLTAGE

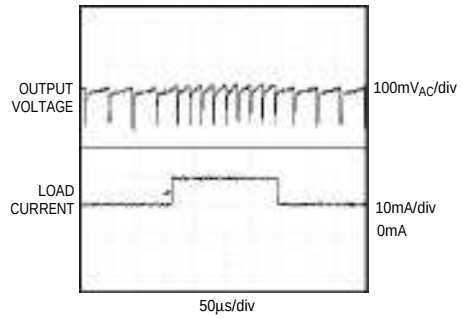


Digitally Adjustable LCD Bias Supply

Typical Operating Characteristics (continued)

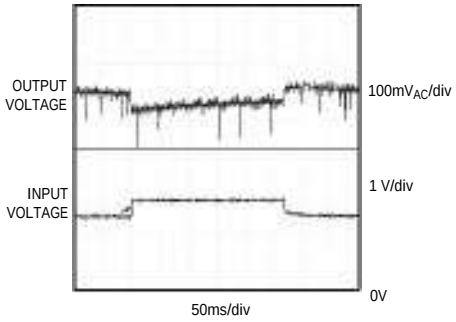
(T_A = +25°C, L = 47µH, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



V_{OUT} = -15V
TRANSISTOR = ZTX750

LINE-TRANSIENT RESPONSE



V_{OUT} = -15V
I_{LOAD} = 5mA
TRANSISTOR = ZTX750

Pin Description

PIN	NAME	FUNCTION
1	V+	+2V to +6V Input Voltage to power the MAX749 and external circuitry. When using an external P-channel MOSFET, V+ must exceed the MOSFET's gate threshold voltage.
2	ADJ	Logic Input. When CTRL is high, a rising edge on ADJ increments an internal counter. When CTRL is low, the counter is reset to mid-scale when ADJ is high. When ADJ is low, the counter does not change (regardless of activity on CTRL) as long as V+ is applied.
3	CTRL	Logic Input. When CTRL and ADJ are low, the MAX749 is shut down, but the counter is not reset. When CTRL is low, the counter is reset to mid-scale when ADJ is high. The device is always on when CTRL is high.
4	FB	Feedback Input for output full-scale voltage selection. $-V_{OUT(MAX)} = (R_{FB}) \times (20\mu A)$ where R_{FB} is connected from FB to $-V_{OUT}$. The device is in regulation when V_{FB} = 0V.
5	GND	Ground
6	DLOW	Output Driver Low. Connect to DHI when using an external P-channel MOSFET. When using an external PNP transistor, connect a resistor R_{BASE} from DLOW to the base of the PNP to set the maximum base-drive current.
7	DHI	Output Driver High. Connect to the gate of the external P-channel transistor, or to the base of the external PNP transistor.
8	CS	Current-Sense Input. The external transistor is turned off when current through the sense resistor, R_{SENSE}, brings CS below V+ by 140mV (typ).

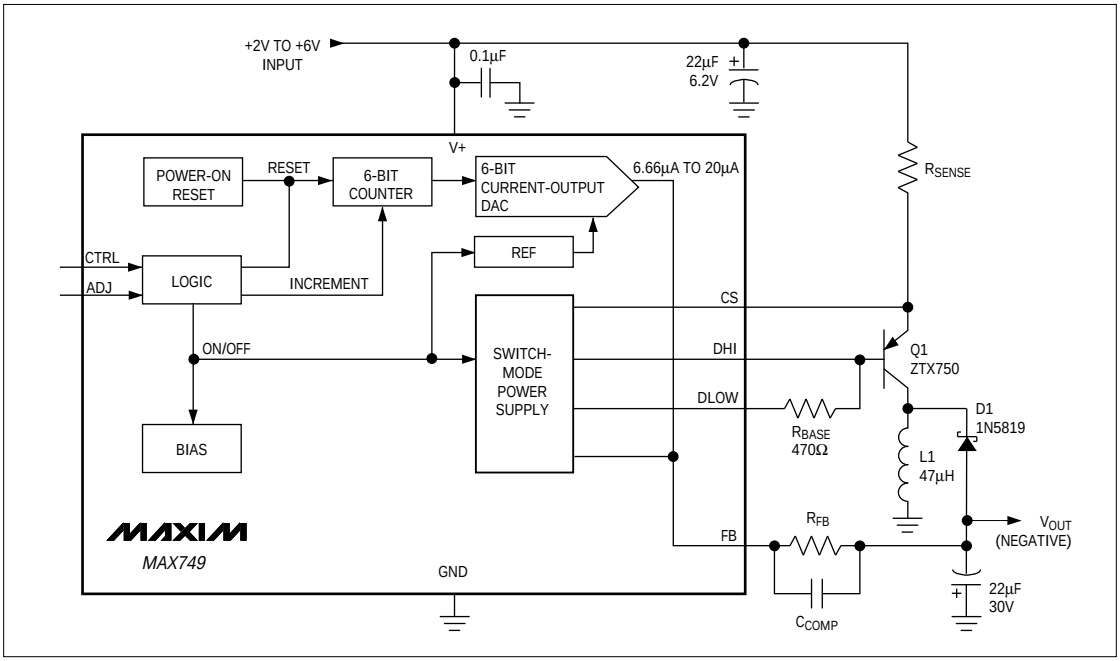


Figure 1. Block Diagram, Showing External Circuitry Using a PNP Transistor

Detailed Description

The MAX749 is a negative-output inverting power controller that can drive an external PNP transistor or P-channel MOSFET. An external resistor and an internal DAC control the output voltage (Figure 1).

The MAX749 is designed to operate from 2V to 6V inputs, ideal for operation from low-voltage batteries. In systems with higher-voltage batteries, such as notebook computers, the MAX749 may also be operated from the regulated +5V supply. A high-efficiency +5V regulator, such as the MAX782, is an ideal source for the MAX749. In this example, the MAX749 efficiency (80%) is compounded with the MAX782 efficiency (95%): 80% x 95% = 76%, which is still high.

Operating Principle

The MAX749 and the external components shown in the *Typical Operating Circuit* form a flyback converter. When the external transistor is on, current flows through the current-sense resistor, the transistor, and the coil. Energy is stored in the core of the coil during this phase, and the diode does not conduct. When the transistor turns off, current flows from the output through the diode and the coil, driving the output negative. Feedback control adjusts the external transistor's timing to provide a regulated negative output voltage.

The MAX749's unique control scheme combines the ultra-low supply current of pulse-skipping, pulse-frequency modulation (PFM) converters with the high full-load efficiency characteristic of pulse-width modulation (PWM) converters. This control scheme allows the device to achieve high efficiency over a wide range of loads. The current-sense function and high operating frequency allow the use of tiny external components.

Switching control is accomplished through the combination of a current limit in the switch plus on- and off-time limits (Figure 2).

Once turned on, the transistor stays on until either:

- the maximum on-time one-shot turns it off (8µs later), or
- the switch current reaches its limit (as determined by the current-sense resistor and the current comparator).

Digitally Adjustable LCD Bias Supply

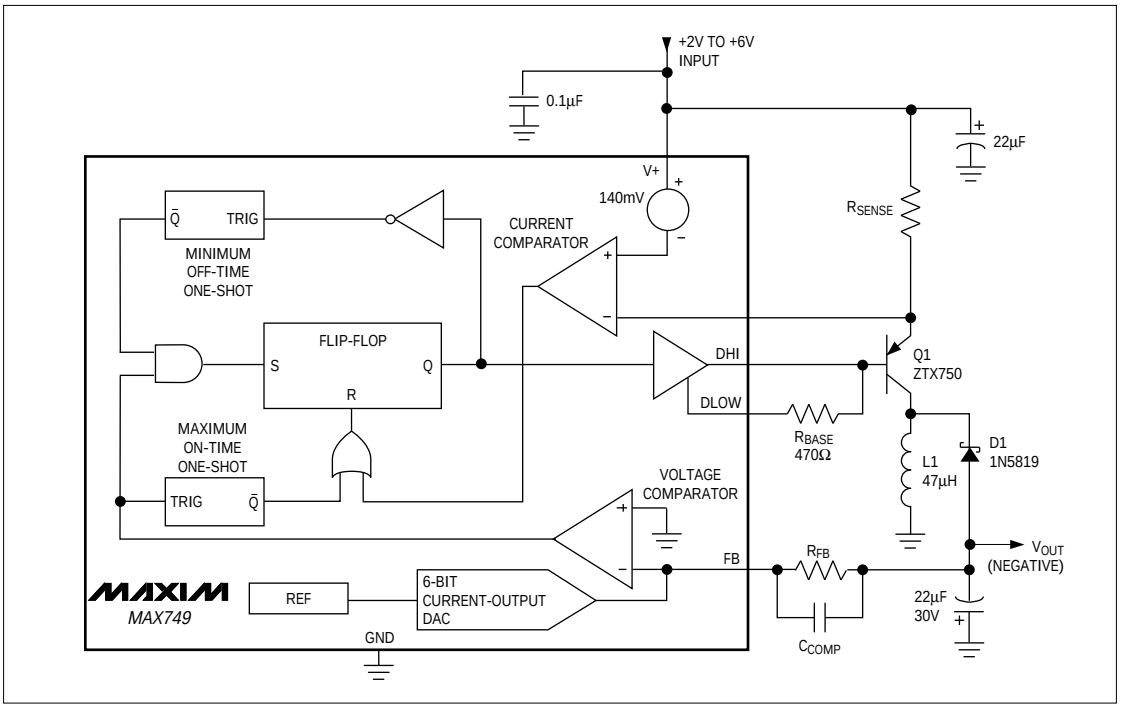


Figure 2. Switch-Mode Power-Supply Section Block Diagram

Once turned off, a one-shot holds the switch off for a minimum of 1µs, and the switch either stays off (if the output is in regulation), or turns on again (if the output is out of regulation).

With light loads, the transistor switches for one or more cycles and then turns off, much like a traditional PFM converter. With heavy loads, the transistor stays on until the switch current reaches the current limit; it then shuts off for 1µs, and immediately turns on again until the next time the switch current reaches its limit. This cycle repeats until the output is in regulation.

Output Voltage Control

The output voltage is set using a single external resistor and the internal current-output DAC (Figure 1). The full-scale output voltage is set by selecting the feedback resistor, R_{FB}. The output voltage is controlled from 33% to 100% of the full-scale output by an internal 64-step DAC/counter.

On power-up or after a reset, the counter sets the DAC output to mid-range. Each rising edge of ADJ increments the DAC output. When incremented beyond full scale, the counter rolls over and sets the DAC to the minimum value. In this way, a single pulse applied to ADJ increases the DAC set point by one step, and 63 pulses decrease the set point by one step.

Table 1 is the logic table for the CTRL and ADJ inputs, which control the internal DAC and counter. Figures 3-7 show various timing specifications and different ways of incrementing and resetting the DAC, and of placing it in the low-power standby mode. As long as the timing specifications for ADJ and CTRL are observed, any sequence of operations can be implemented.

Table 1. Input Truth Table

ADJ	CTRL	RESULT
Low	Low	Shut down
High	Low	Reset counter to mid-range. The device is not shut down.
X	High	On
	High	Increment the counter

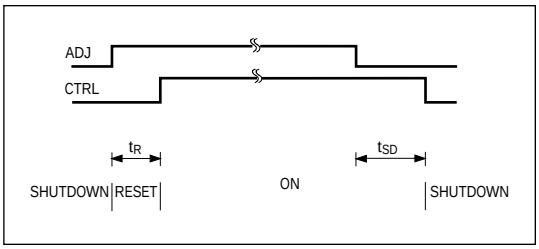


Figure 3. Shutdown-Reset-On-Shutdown Sequence of Operation. The device is not shut down during reset.

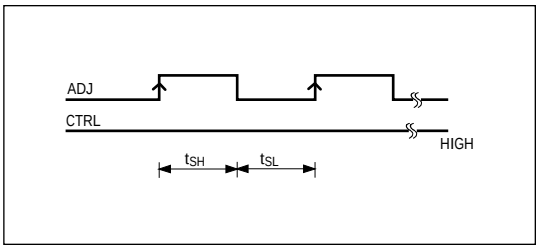


Figure 4. Count-Up Operation

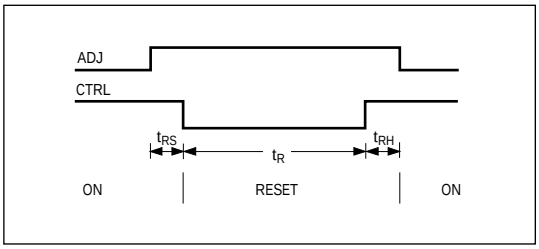


Figure 5. Reset Sequence without Shutdown. The device is not shut down during reset.

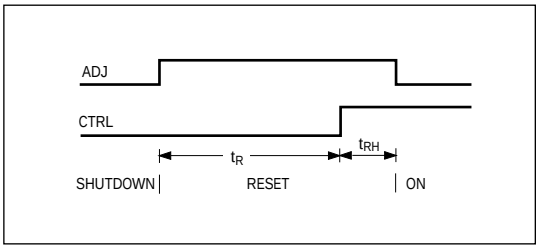


Figure 6. Reset Sequence with Shutdown

In Figure 3, the MAX749 is reset when it is taken out of shutdown, which sets the output at mid-scale. Figure 4 shows how to increment the counter. Figure 5 illustrates a reset without shutting the device down.

Figure 7 provides an example of a sequence of operations: Starting from shutdown, the device is turned on, incremented, reset to mid-scale without being shut down, incremented again, and finally shut down.

Shutdown Mode

When CTRL and ADJ are both low, the MAX749 is shut down (Table 1): The internal reference and biasing circuitry turn off, the output voltage drops to zero, and the supply current drops to 15µA. The MAX749 retains its DAC setting, simplifying software control.

Reset Mode

If ADJ is high when CTRL is low, the DAC set point is reset to mid-scale and the MAX749 is not shut down. Mid-scale is 32 steps from the minimum, 31 steps from the maximum.

Design Procedure and Component Selection

Setting the Output Voltage

The MAX749's output voltage is set using an external resistor and the internal current-output DAC. The full-scale output voltage is set by selecting the feedback resistor R_{FB} according to the formula:

$$-V_{OUT(MAX)} = R_{FB} \times 20\mu A \text{ (Figure 1).}$$

The device is in regulation when V_{FB} = 0V.

DAC Adjustment

On power-up or after a reset, the counter sets the DAC output to mid-range, and $-V_{OUT} = R_{FB} \times 13.33\mu A$. Each rising edge of ADJ increments the counter (and therefore the DAC output) in the direction of $-V_{OUT(MAX)}$ by one count. When incremented beyond $-V_{OUT(MAX)}$, the

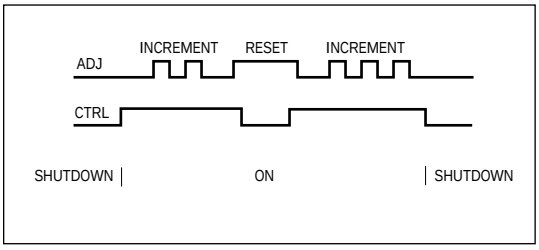


Figure 7. Control Sequence Example (see Output Voltage Control section)

Digitally Adjustable LCD Bias Supply

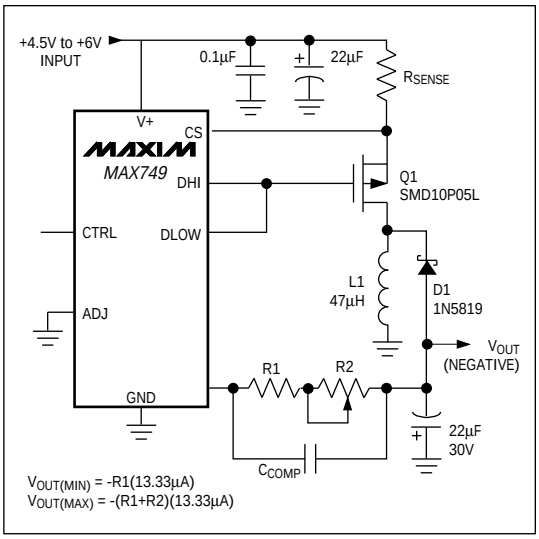


Figure 8. Using a Potentiometer to Adjust the Output Voltage

counter rolls over and sets the DAC to $-V_{OUT(MIN)}$, where $-V_{OUT(MIN)} = R_{FB}$ x 6.66µA. In other words, a single rising edge of ADJ increments the DAC output by one, and 63 rising edges of ADJ decrement the DAC output by one.

Potentiometer Adjustment

It is also possible to adjust the output voltage using a potentiometer instead of the internal DAC (Figure 8). On power-up (V+ applied), the internal current source is set to mid-scale, or 13.33µA. Choose R1 and R2 with the following equations:

$$R1 = -V_{OUT(MIN)}/13.33\mu A$$

$$R2 = -V_{OUT(MAX)}/13.33\mu A - R1.$$

Where the potentiometer can be varied from 0 (producing $V_{OUT(MIN)}$) to R2Ω (producing $V_{OUT(MAX)}$). Notice that ADJ is connected to ground, allowing the device to be shut down.

PWM Adjustment

A positive pulse-width modulated (PWM) logic signal (e.g., from a microcontroller) can control the MAX749's output voltage. Use the PWM signal to pull up the FB pin through a suitable resistor. An RC network on the PWM output would also be required. In this configuration, the longer the PWM signal remains high, the more negative the MAX749's output will be driven.

Current-Sense Resistor

The current-sense resistor limits the peak switch current to 140mV/R_{SENSE}, where R_{SENSE} is the value of the current-sense resistor, and 140mV is the typical current-sense comparator threshold (see V+ to CS Voltage in the *Electrical Characteristics*).

To maximize efficiency and reduce the size and cost of the external components, minimize the peak current. However, since the output current is a function of the peak current (Figures 9a-9e), the limit should not be set too low.

No calculations are required to choose the proper current-sense resistor; simply follow this two-step procedure:

1. Determine:
   - the minimum input voltage, $V_{IN(MIN)}$,
   - the maximum output voltage, $V_{OUT(MAX)}$, and
   - the maximum output current, $I_{OUT(MAX)}$.

For example, assume that the output voltage must be adjustable to -24V ($V_{OUT(MAX)}$ = -24V) at up to 30mA ($I_{OUT(MAX)}$ = 30mA). The supply voltage ranges from 4.75V to 6V ($V_{IN(MIN)}$ = 4.75V).

2. In Figures 9a-9e, locate the graph drawn for the appropriate output voltage (which is either the desired output voltage or, if that is not shown, the graph for the nearest voltage more negative than the desired output). On this graph find the curve for the highest R_{SENSE} (the lowest current limit) with an output current that is adequate **at the lowest input voltage.**

In this example, select the -24V output graph, Figure 9d. We then want a curve where I_{OUT} is ≥30mA with a 4.75V input. The 0.3Ω R_{SENSE} graph shows 25mA of output current with a 4.75V input, so we look next at the 0.25Ω R_{SENSE} graph. It shows I_{OUT} = 30mA for V_{IN} = 4.75V and V_{OUT} = -24V. Therefore select R_{SENSE} = 0.25Ω. This provides a current limit in the range 440mA to 720mA.

Alternatively, a 0.2Ω sense resistor can be used. This gives a current limit in the range 550mA to 900mA, but enables over 40mA to be generated at -24V with input voltages down to 4.5V. A 0.2Ω resistor may be easier to obtain than an 0.25Ω resistor.

The theoretical design curves shown in Figures 9a-9e assume the minimum (worst-case) value for the current-limit comparator threshold. Having selected the current-sense resistor, the maximum current limit is given by 180mV/R_{SENSE}. Use the maximum current-limit figure when choosing the transistor, coil, and diode.

IRC (see Table 2) makes surface-mount resistors with preferred values including: 0.1Ω, 0.2Ω, 0.3Ω, 0.5Ω, and 1.0Ω.

Choosing an Inductor

Practical inductor values range from 22µH to 100µH, and 47µH is normally a good choice. Inductors with a ferrite core or equivalent are recommended. The inductor's saturation current rating – the current at which the core begins to saturate and the inductance falls to 80% or 90% of its nominal value – should ideally equal the current limit (see *Current-Sense Resistor* section). However, because the current is limited by the MAX749, the inductor can safely be driven into saturation with only a slight impact on efficiency.

For highest efficiency, use a coil with low resistance, preferably under 300mΩ. To minimize radiated noise, use a toroid, pot-core, or shielded inductor.

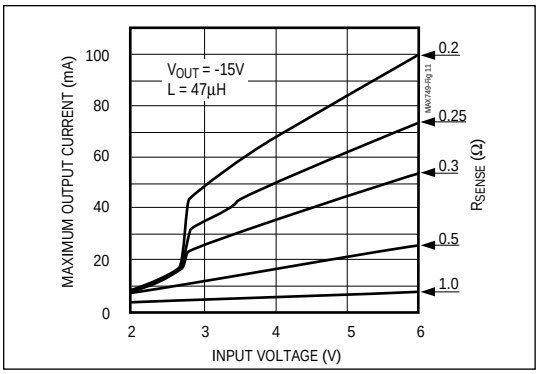


Figure 9c. Maximum Output Current vs. Input Voltage, V_{OUT} = -15V

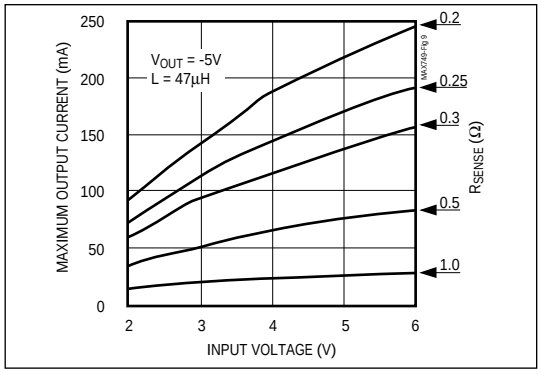


Figure 9a. Maximum Output Current vs. Input Voltage, V_{OUT} = -5V

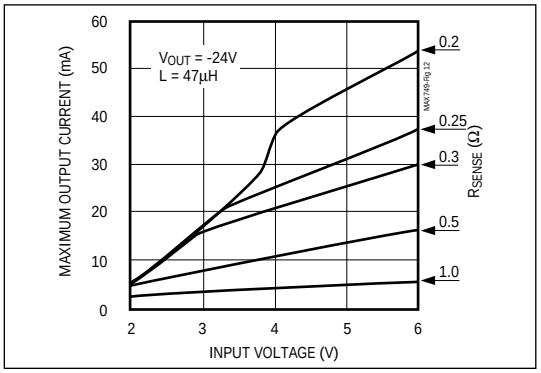


Figure 9d. Maximum Output Current vs. Input Voltage, V_{OUT} = -24V

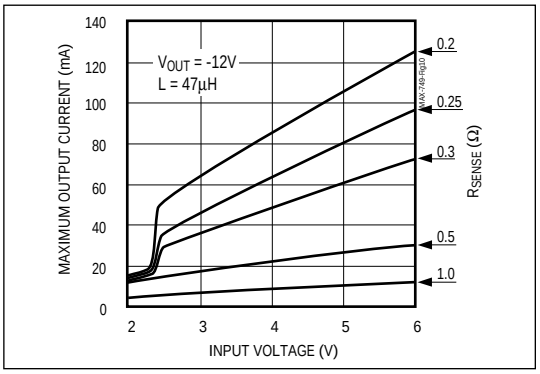


Figure 9b. Maximum Output Current vs. Input Voltage, V_{OUT} = -12V

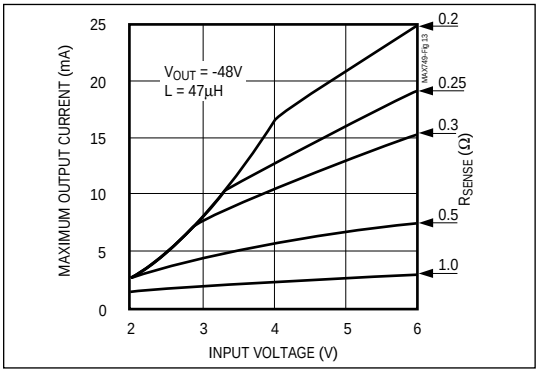


Figure 9e. Maximum Output Current vs. Input Voltage, V_{OUT} = -48V

Digitally Adjustable LCD Bias Supply

The Sumida CD54-470N (47µH, 720mA, 370mΩ) is suitable for a wide range of applications, and the larger CD105-470N (47µH, 1.17A, 170mΩ) permits higher current levels and efficiencies.

Diode Selection

The MAX749's high switching frequency demands a high-speed rectifier. Schottky diodes such as the 1N5817-1N5822 family are recommended. Choose a diode with an average current rating approximately equal to the peak current, as determined by $180mV/R_{SENSE}$ and a breakdown voltage greater than $V+ + |-V_{OUTMAX}|$.

External Switching Transistor

The MAX749 can drive a PNP transistor or a P-channel logic-level MOSFET. The choice of a power switch is dictated by the input voltage range, cost, and efficiency.

MOSFETs provide the highest efficiency because they do not draw any DC gate-drive current (see *Typical Operating Characteristics* graphs). However, a gate-source voltage of several volts is needed to turn on a MOSFET, so a 5V or greater input supply is required (although this restriction may change as lower-threshold P-channel MOSFETs become available). PNP transistors, meanwhile, may be used over the entire 2V to 6V operating voltage range of the MAX749.

When using a MOSFET, connect DHI and DLOW to its gate (see *Typical Operating Circuit*). When using a PNP transistor, connect DHI to its base, and connect a resistor between the base and DLOW (R_{BASE}) (Figure 1). The PNP transistor is turned off quickly by the direct pull-up of DHI, and turned on by the base current provided through R_{BASE}. This resistor limits the transistor's base-drive current to $(V_{IN} - 140mV - V_{BE})/R_{BASE}$, where V_{IN} is the input voltage, 140mV is the drop across R_{SENSE}, V_{BE} is the transistor's base-emitter voltage, and R_{BASE} is the current-limiting resistor. For maximum efficiency, make R_{BASE} as large as possible, but small enough so that the transistor is always driven into saturation.

Highest efficiency with a PNP transistor comes from using a device with a low collector-emitter saturation voltage and a high current gain. Use a fast-switching type. For example the Zetex ZTX792A has switching speeds of 40ns (t_{ON}) and 500ns (t_{OFF}).

The transistor must have a collector-to-emitter (PNP) or drain-to-source (MOSFET) voltage rating greater than the input-to-output voltage differential ($V_{IN} - V_{OUT}$). In either case the transistor must have a current rating that exceeds the peak current set by the current-sense resistor.

PNP transistors are generally less expensive than P-channel MOSFETs. Table 2 lists some suppliers of switching transistors suitable for use with the MAX749.

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coiltronics	(305) 781-8900	(305) 782-4163
Gowanda	(716) 532-2234	(716) 532-2702
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	81-3-3607-511	81-3-3607-5428
CAPACITORS		
Kemet	(803) 963-6300	(803) 963-6322
Matsuo	(714) 969-2491	(714) 960-6492
Nichicon	(708) 843-7500	(708) 843-2798
Sprague	(603) 224-1961	(603) 224-1430
Sanyo USA	(619) 661-6322	
Sanyo Japan	81-3-3837-6242	
United Chemi-Con	(714) 255-9500	(714) 255-9400
DIODES		
Motorola	(800) 521-6274	
Nihon USA	(805) 867-2555	(805) 867-2698
Nihon Japan	81-3-3494-7411	81-3-3494-7414
POWER TRANSISTORS - MOSFETS		
Harris	(407) 724-3739	(407) 724-3937
International Rectifier	(213) 772-2000	(213) 772-9028
Siliconix	(408) 988-8000	(408) 727-5414
POWER TRANSISTORS - PNP TRANSISTORS		
Zetex USA	(516) 543-7100	(516) 864-7630
Zetex UK	44 (61) 727 5105	44 (61) 627 5467
CURRENT-SENSE RESISTORS		
IRC	(512) 992-7900	(512) 992-3377

Base Resistor

The base resistor, R_{BASE} in Figure 1, controls the amount of base current in the PNP transistor. A low value for R_{BASE} increases base drive, which provides higher output currents and compensates for lower input voltages, but decreases efficiency. Conversely, a high R_{BASE} value increases efficiency but reduces the output capability, especially at low voltages. When using high-gain transistors, e.g. the Zetex ZTX750 or ZTX792, typical values for R_{BASE} are in the 150Ω to 510Ω range, but will depend on the required input voltage range and output current (see *Typical Operating Characteristics*). Lower-gain transistors require lower values for R_{BASE} and are less efficient. Larger R_{BASE} values are suitable if less output power is required.

Capacitors

Output Filter Capacitor

A 22µF, 30V surface-mount (SMT) tantalum output filter capacitor typically maintains 100mVp-p output ripple when generating -24V at 40mA from a 5V input. Smaller capacitors, down to 10µF, may be used for light loads in applications that can tolerate higher output ripple. Surface-mount capacitors are generally preferred because they lack the inductance and resistance of the leads of their through-hole equivalents.

Input Bypass Capacitor

A 22µF tantalum capacitor in parallel with a 0.1µF ceramic normally provides sufficient bypassing. **Mount the 0.1µF capacitor very close to the IC.** Larger capacitors may be needed if the incoming supply has high impedance. Less bypass capacitance is acceptable if the circuit is run off a low-impedance supply. Begin prototyping with a large bypass capacitor; when the circuit is working, reduce the bypass to the smallest value that gives good results. Although bench power supplies have low impedance at DC, they often have high impedance at the frequencies used by switching DC-DC converters.

The effective series resistance (ESR) of both the bypass and filter capacitors affects efficiency. Best performance is obtained by doubling up on the filter capacitors or using low-ESR types.

The smallest low-ESR SMT capacitors currently available are Sprague 595D series, which are about half the size of competing products. Sanyo OS-CON organic semiconductor through-hole capacitors also exhibit low ESR, and are especially useful when operation below 0°C is required. Table 2 lists the phone numbers of these and other manufacturers.

Compensation Capacitor

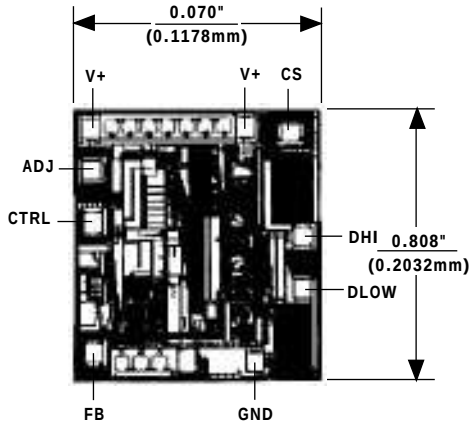
The high value of the feedback resistor makes the feedback loop susceptible to phase lag if parasitic capacitance is present at the FB pin. To compensate for this, it may be necessary to connect a capacitor, C_{COMP}, in parallel with R_{FB}. Although C_{COMP} is normally not required, the value of C_{COMP} depends upon the value of R_{FB} and on the individual circuit layout—typical values range from 0pF to 220pF.

PC Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. In particular, keep all leads short, especially the lead connected to the FB pin and those connecting Q1, L1, and D1 together. **Mount the R_{FB} resistor very close to the IC.**

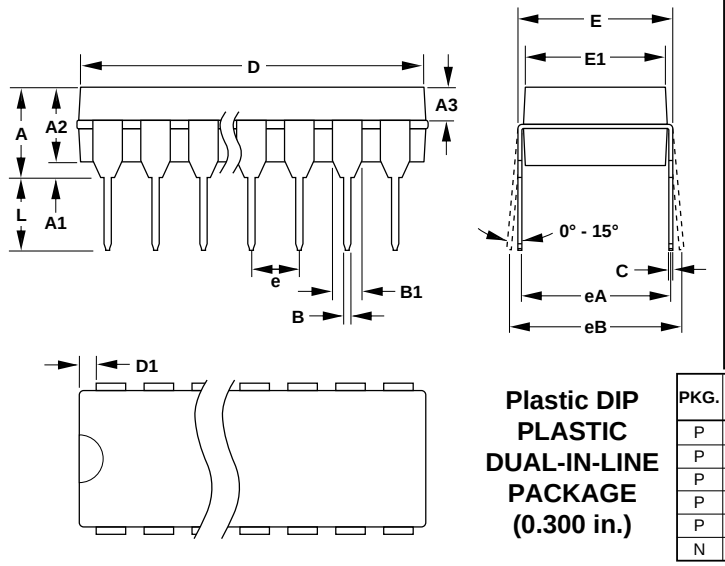
Use a star ground configuration: Connect the ground lead of the input bypass capacitor, the output capacitor, and the inductor at a common point next to the GND pin of the MAX749. Additionally, connect the positive lead of the input bypass capacitor as close as possible to the V+ pin of the IC.

Chip Topography



TRANSISTOR COUNT: 521;
SUBSTRATE CONNECTED TO GND.

Package Information

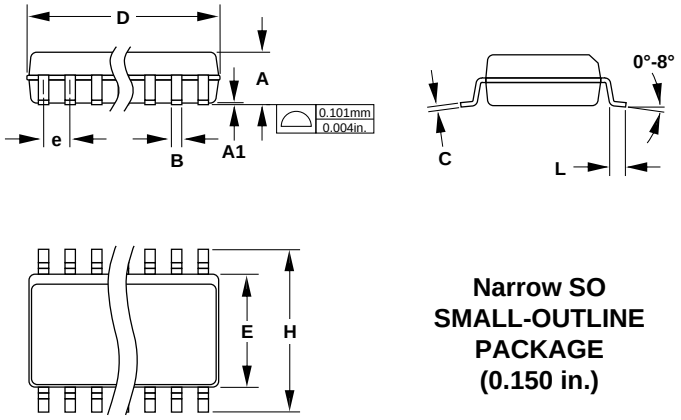


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

Narrow SO
SMALL-OUTLINE
PACKAGE
(0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A