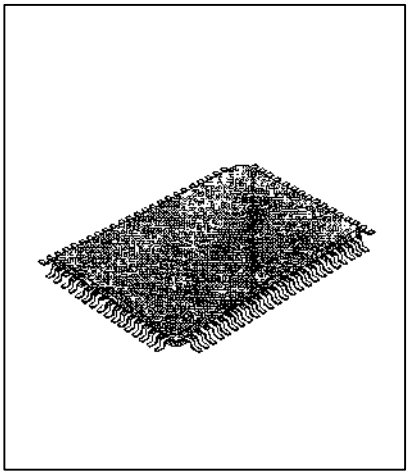
KS0106 50CH SEGMENT DRIVER FOR DOT MATRIX LCD

INTRODUCTION

80 QFP



The KS0106 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology This device consists of Display Data RAM, 50 bit data latch, 50 bit driver and decoder circuit.This device can be interfaced with 4 or 8 bit MPU directly.

FUNCTION

- Dot matrix LCD segment driver with 50 channel output.
- Input/Output signal
  - Input: parallel display data (4 or 8 bit), control signal from MPU and bias voltage (V_1, V_2, V_3, V_4, V_{EE})
  - Output; 50 channel waveform for LCD driving.
- Display data is stored in Display Data RAM from MPU.

FEATURE

- Power supply voltage: +5V±10%
- Supply voltage for display: 0~- 5.5V(V_{EE})
- Applicable LCD duty;
  (1/8, 1/12, 1/16, 1/24, 1/32)
- Interface RAM
  - Capacity: 50x8x4 (1600 bits)
  - RAM bit data

RAM bit data	H	L
Display	ON	OFF

- Interface

Driver		Controller
SEGMENT	COMMON	
other KS0106	KS0105	MPU

- High voltage CMOS process
- 80 QFP and bare chip available.

SAMSUNG ELECTRONICS

BLOCK DIAGRAM

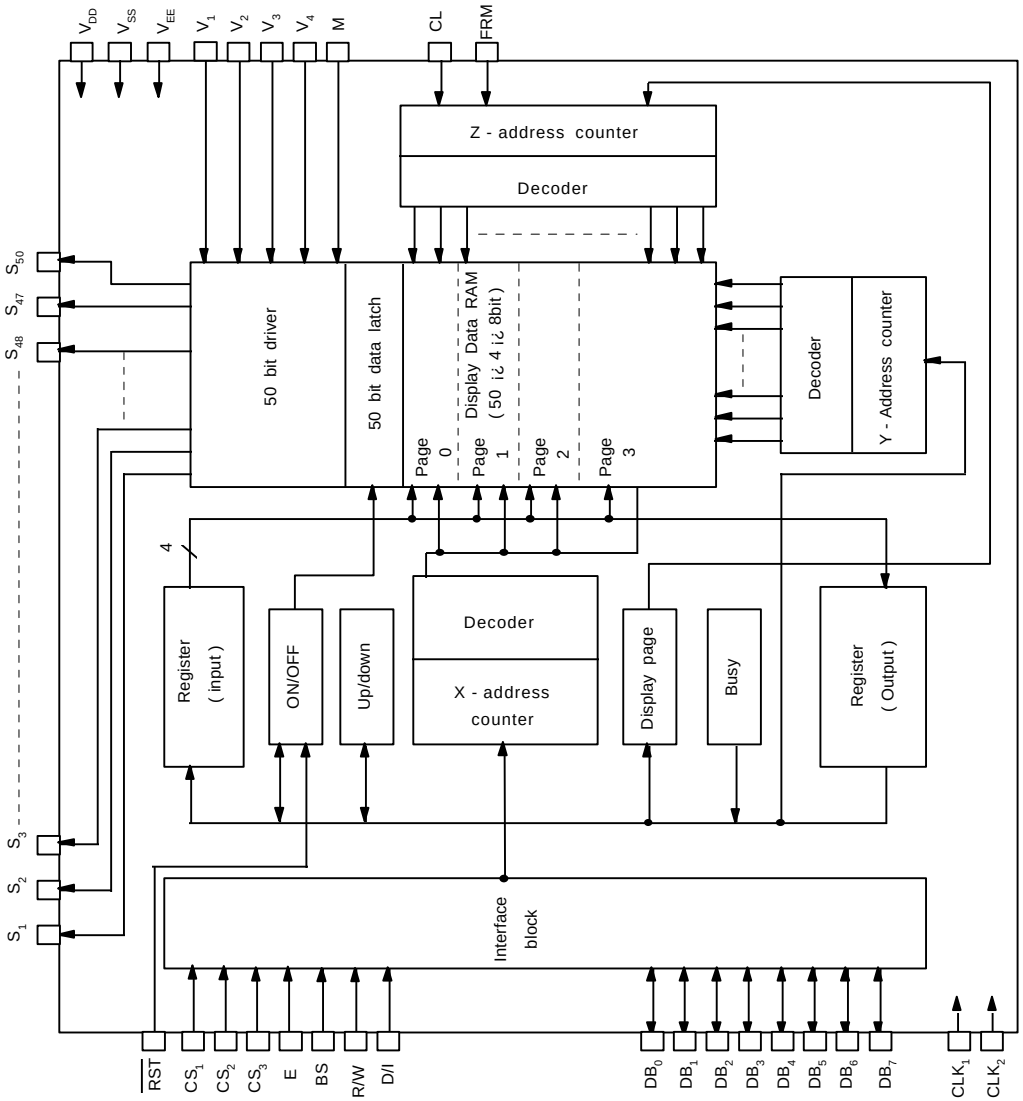


Fig 1. KS0106 functional block diagram

PIN CONFIGURATION

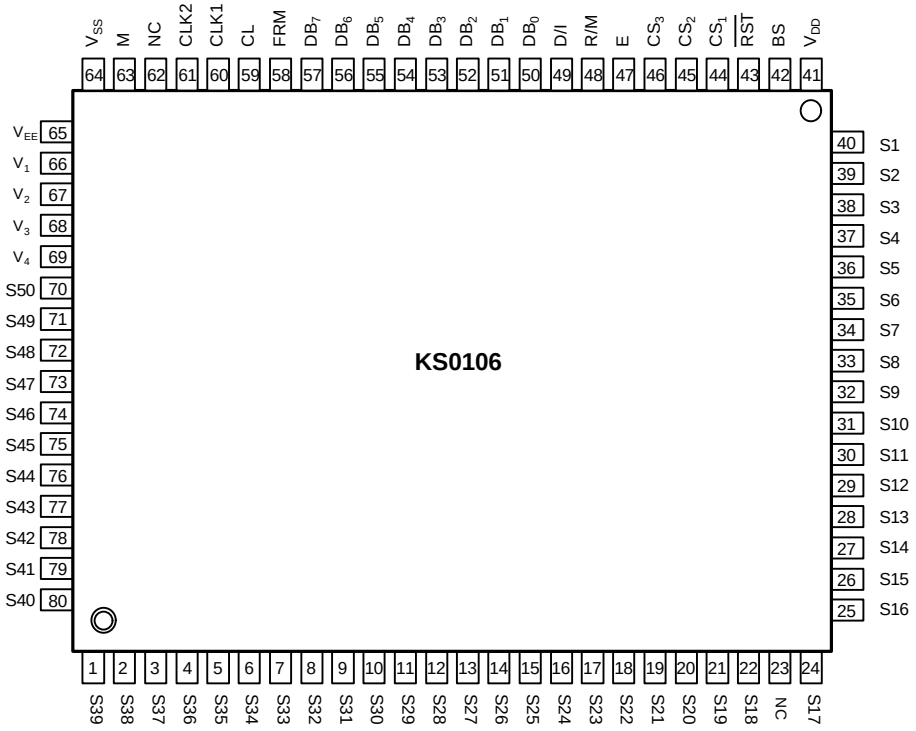


Fig. 2. 80 QFP Top View

PIN DESCRIPTION

<table>
<tr><th>PIN (No.)</th><th>INPUT/OUTPUT</th><th>NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(41)</td><td rowspan="3">Power</td><td rowspan="2">Operating Voltage</td><td>For internal logic circuit (+5V±10%)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>V_{SS}(64)</td><td>GND (0V)</td></tr>
<tr><td>V_{EE}(65)</td><td>Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V_1, V_2 (66, 67)
V_3, V_4 (68, 69)</td><td>Input</td><td>Bias Voltage</td><td>Bias supply voltage terminal to drive the LCD
<table><tr><th>Select level</th><th>Non-select level</th></tr><tr><td>V_1~V_2</td><td>V_3~V_4</td></tr></table></td><td>Power</td></tr>
<tr><td>S_1-S_{50}
(1-40, 70-80)</td><td>Output</td><td>LCD Driver Ouput</td><td>Segment signal output for LCD driving
<table><tr><th>M</th><th>D</th><th>Output level</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_1</td></tr><tr><td>L</td><td>V_3</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_2</td></tr><tr><td>L</td><td>V_4</td></tr></table></td><td>LCD</td></tr>
<tr><td>M(63)</td><td>Input</td><td>Alternated Signal for LCD driver</td><td>Alternating signal input pin for LCD driving</td><td>KS0105</td></tr>
<tr><td>CL(59)</td><td>Input</td><td>Synchronous Clock</td><td>Segment signal synchronizes the rise of CL</td><td>KS0105</td></tr>
<tr><td>FRM (58)</td><td>Input</td><td>Frame Signal</td><td>Synchronous frame signal</td><td>KS0105</td></tr>
<tr><td>CLK_1,CLK_2(60, 61)</td><td>Input</td><td>Operating Clock</td><td>Clock for internal operation (2 phase)</td><td>KS0105</td></tr>
<tr><td>D/I (49)</td><td>Input</td><td>Data/Instruction</td><td><table><tr><td>High</td><td>DB_0-DB_7 become for display data</td></tr><tr><td>Low</td><td>DB_0-DB_7 become for control data</td></tr></table></td><td>MPU</td></tr>
<tr><td>R/W(48)</td><td>Input</td><td>Read/Write</td><td><table><tr><td>H</td><td>read mode (E=H, CS_2=H, CS_3=H)</td></tr><tr><td>L</td><td>write mode (CS1=H or CS2=CS3=H)</td></tr></table></td><td>MPU</td></tr>
<tr><td>E(47)</td><td>Input</td><td>Enable</td><td><table><tr><th rowspan="2">Data of DB_0-DB_7</th><th colspan="2">Condition</th></tr><tr><th>R/W</th><th>E timing</th></tr><tr><td>latched</td><td>L</td><td>Falling edge</td></tr><tr><td>output</td><td>H</td><td>High level</td></tr></table></td><td>MPU</td></tr>
<tr><td>BS(42)</td><td>Input</td><td>Data Bus Select Signal</td><td><table><tr><td>Low</td><td>8 bit operating (DB_0-DB_7)</td></tr><tr><td>High</td><td>- 4bit operating (DB_4-DB_7)
- 8 bit data length is accessed two times in the upper and lower order.</td></tr></table></td><td>MPU</td></tr>
</table>

PIN DESCRIPTION (continued)

<table>
<tr><th>PIN (No.)</th><th>INPUT/OUTPUT</th><th>NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>$\overline{RST}$(43)</td><td>Input</td><td>Reset Signal</td><td><table><tr><td>$\overline{RST}$ =L
↓
RST =release</td><td>- Display; disappear
- Y address counter; becomes “up count state”.
- return to “Display off” state
- Up count state will be maintain untill state is changed by instruction</td></tr></table></td><td>MPU</td></tr>
<tr><td>CS_1-CS_3 (44-46)</td><td>Input</td><td>Chip Select</td><td><table><tr><th>CS_1</th><th>CS_2</th><th>CS_3</th><th>State</th></tr><tr><td>L</td><td>L</td><td>L</td><td>non-select mode</td></tr><tr><td>L</td><td>L</td><td>H</td><td>non-select mode</td></tr><tr><td>L</td><td>H</td><td>L</td><td>non-select mode</td></tr><tr><td>L</td><td>H</td><td>H</td><td>read/write enable mode</td></tr><tr><td>H</td><td>L</td><td>L</td><td>only write enable mode</td></tr><tr><td>H</td><td>L</td><td>H</td><td>only write enable mode</td></tr><tr><td>H</td><td>H</td><td>L</td><td>only write enable mode</td></tr><tr><td>H</td><td>H</td><td>H</td><td>read/write enable mode</td></tr></table></td><td>MPU</td></tr>
<tr><td>DB_0-DB_7 (50-57)</td><td>Input/Output</td><td>Data Bus</td><td>- Data bus termianl
- Bi-directional three-state
- Output state: E, R/W, CS2 and CS3=High
- Input state, high impedence:
R/W=Low and CS_1=High or R/W=Low and CS_2, CS_3=High</td><td>MPU</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (T_a=25°C)

Characteristics	Symbol	Value	Unit	Test pin
Operating Voltage	V_{DD}	-0.3~+7.0	V	V_{DD}, V_{SS}, V_{EE}
Driver Supply Voltage	V_{LCD}*1	V_{DD}-13.5~V_{DD}+0.3		
Input Voltage	V_{IN1}	-0.3~V_{DD}+0.3		M,CL, FRM,CLK1, CLK2, D/I, R/W, E, BS, $\overline{RST}$, CS_1-CS_3, DB_0-DB_7
	V_{IN2}	V_{EE}-0.3~V_{DD}+0.3		V_1, V_2, V_3,V_4
Operating Temperature	T_{OPR}	-20~+75	°C	-
Storage Temperature	T_{STG}	-55~+125		-

*1VEE : connect a protection resistor (20Ω±5%)

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, Ta=25°C)

Characteristic		Symbol	condition	Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	-	4.5	-	5.5	V	
Operating Current		I_{DD1}	f_{CK}=200kHz f_{FRM}=65Hz	-	-	100	μA	V_{DD}, V_{SS}
		I_{DD2}*2	Access cycle 1MHz at access	-	-	500		
Input Voltage (CMOS level)	High	V_{IH}	-	0.7V_{DD}	-	V_{DD}		M, FRM, CL,BS, $\overline{RST}$, CLK1, CLK2 CS_1-CS_3, E,D/I,R/W DB_0-DB_7
	Low	V_{IL}	-	0	-	0.3V_{DD}		
Output Voltage	High	V_{OH}	I_{OH}=-250μA	3.5	-	-	V	DB_0-DB_7
	Low	V_{OL}	I_{OL}=+1.6mA	-	-	0.4		
On Resistance (V-S)		R_{ON}	V_{EE}=-5V±10% Load Current;100μA	-	-	7.5	kΩ	-
Input Leakage Current		I_{LKG1}	V_{IN}=V_{DD}~V_{SS}	-1	-	1	μA	M,FRM,CL,BS,$\overline{RST}$,E, CLK_1,CLK_2,CS_1-CS_3 D/I,R/W,DB_0-DB_7
		I_{LKG2}	V_{IN}=V_{DD}~V_{EE}	-2	-	2		V_1, V_2, V_3, V_4
Operating frequency		f_{CK}	CLK_1,CLK_2, Frequency	25	-	280	KHz	CLK_1,CLK_2
Pull-up Current		I_{pu}	Pull-up	25	-	180	μA	DB_0-DB_7

*2: Current consumption when write mode.

AC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, T_a=25°C)

1) Write mode (Unit: ns)

Characteristic	Symbol	Min	Typ	Max	Test pin
Data Hold Time	t_{DH}	10	-	-	DB_0-DB_7, E
Data Set-Up Time	t_{DSU}	200	-	-	CS_1-CS_3
Address Hold Time	t_{AH}	10	-	-	R/W, E
Address Set-Up Time	t_{ASU}	140	-	-	CS_1-CS_3, D/I
E Fall Time	t_F	-	-	25	E
E Rise Time	t_R	-	-	25	
E Low Level Width	t_{WL}	450	-	-	
E High Level Width	t_{WH}	450	-	-	
E Cycle Time	t_C	1000	-	-	

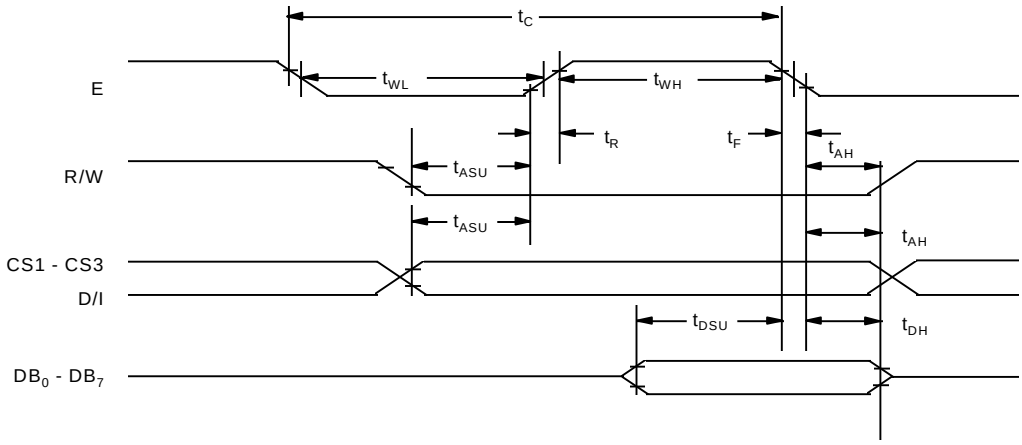


Fig. 3. Write timing characteristic

2) Read mode (Unit: ns)

Characteristic	Symbol	Min	Typ	Max	Test pin
Data Hold Time	t_{DH}	20	-	-	DB_0-DB_7, E
Data Delay Time	t_D	-	-	320	CS_1-CS_3, D/I
Address Hold Time	t_{AH}	10	-	-	R/W, E
Address Set-Up Time	t_{ASU}	140	-	-	CS_1-CS_3, D/I
E Fall Time	t_F	-	-	25	E
E Rise Time	t_R	-	-	25	
E Low Level Width	t_{WL}	450	-	-	
E High Level Width	t_{WH}	450	-	-	
E Cycle Time	t_C	1000	-	-	

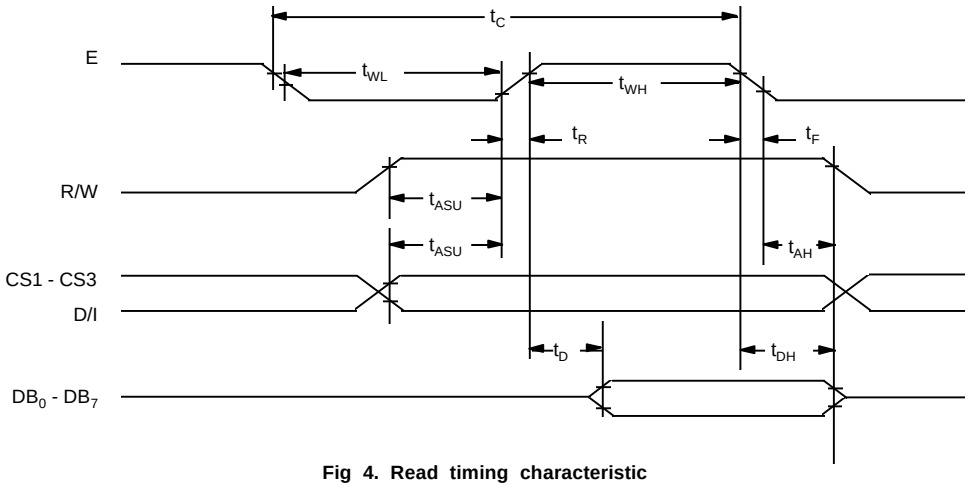
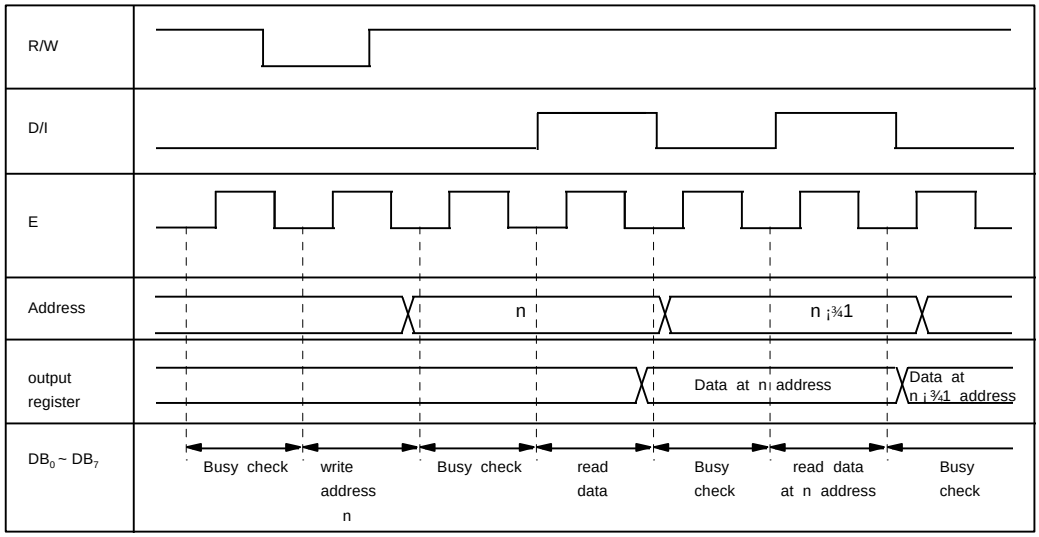


Fig 4. Read timing characteristic

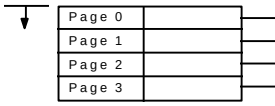
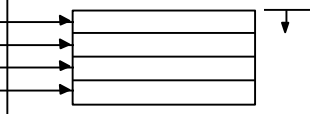
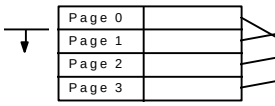
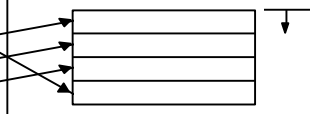
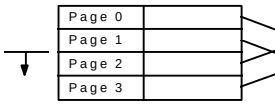
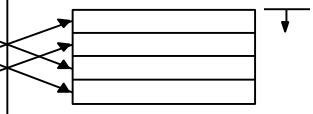
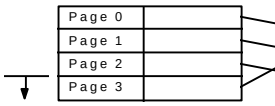
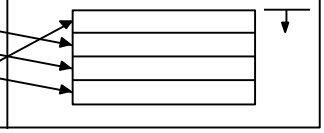
CONTROL AND DISPLAY COMMAND

Command		R/W	D/I	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Remark
Data	Read	H	H	Display Data								note 1
	Write	L	H	Display Data								
Display	ON	L	L	L	L	H	H	H	L	L	H	RAM data
	OFF	L	L	L	L	H	H	H	L	L	L	; not aftected
Up mode		L	L	L	L	H	H	H	L	H	H	In up/down mode, set
Down mode		L	L	L	L	H	H	H	L	H	L	Y address register
Diaplay start page		L	L	L	L	H	H	H	H	H	L	note 2
				L	H							
				H	L							
				H	H							
Status read		H	L	B	U/D	OFF/ON	$\overline{RESET}$	L	L	L	L	•B: BUSY •U/D: Up/Down H: up mode L: down mode • OFF/ON H: display off L: display on •$\overline{RESET}$:low active
X/Y address set		L	L	X address		Y address						X address: 0 ~ 3 Y address: 0 ~ 49

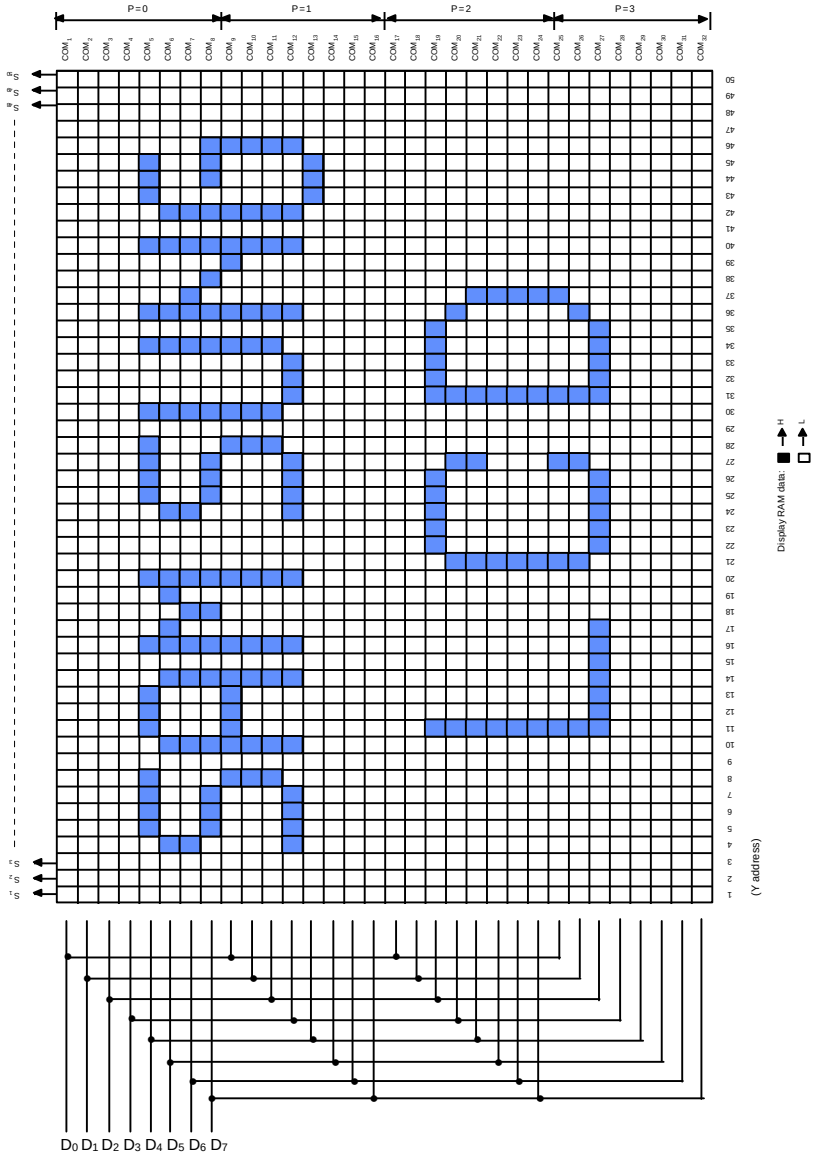
Note 1) Data read timing between address and output register



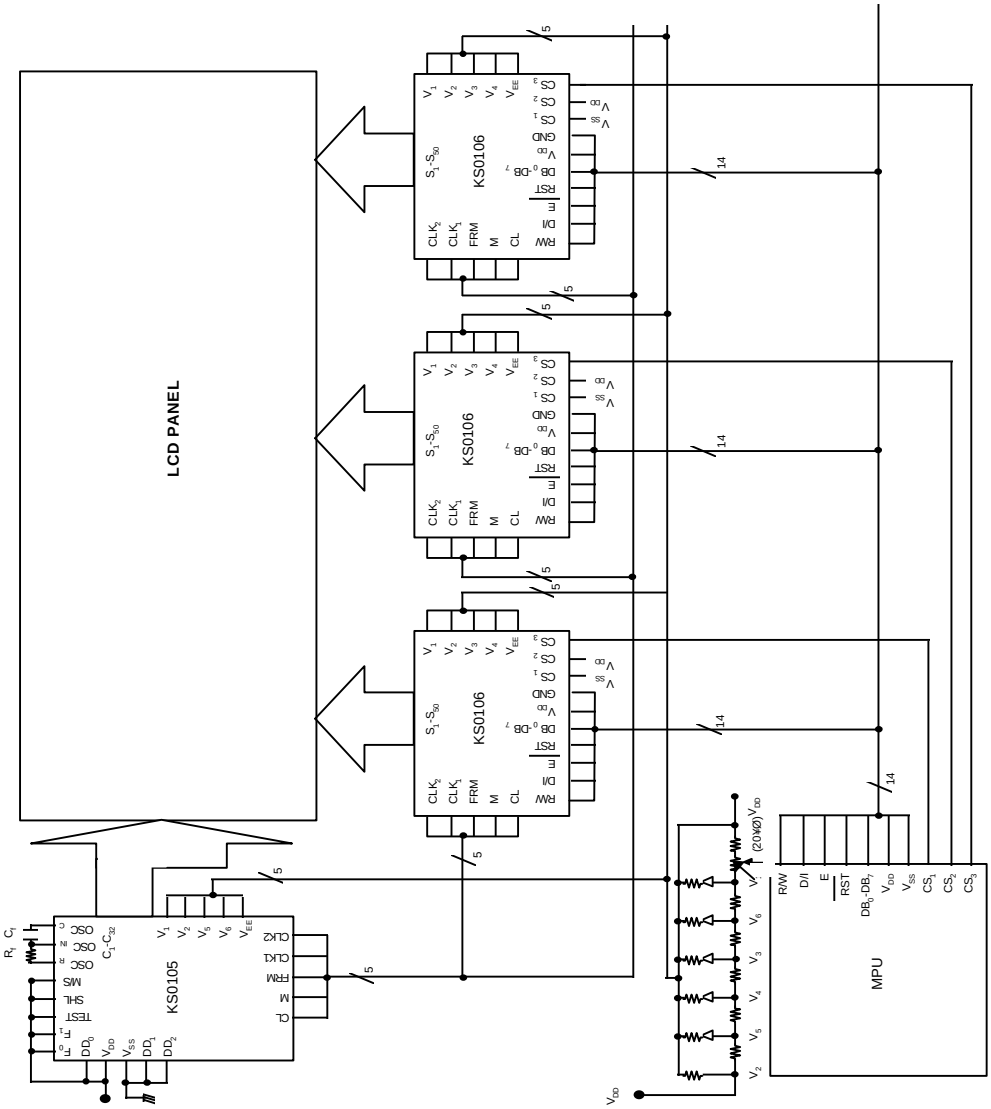
Note 2)

Condition		Start Page	Display Data RAM	LCD Display Screen
DB_7	DB_6			
L	L	0 page		
L	H	1 page		
H	L	2 page		
H	H	3 page		

Construction of Display data RAM

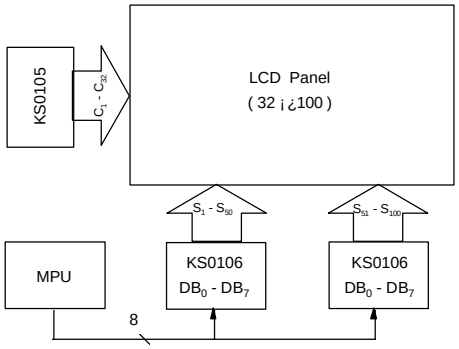


APPLICATION CIRCUIT

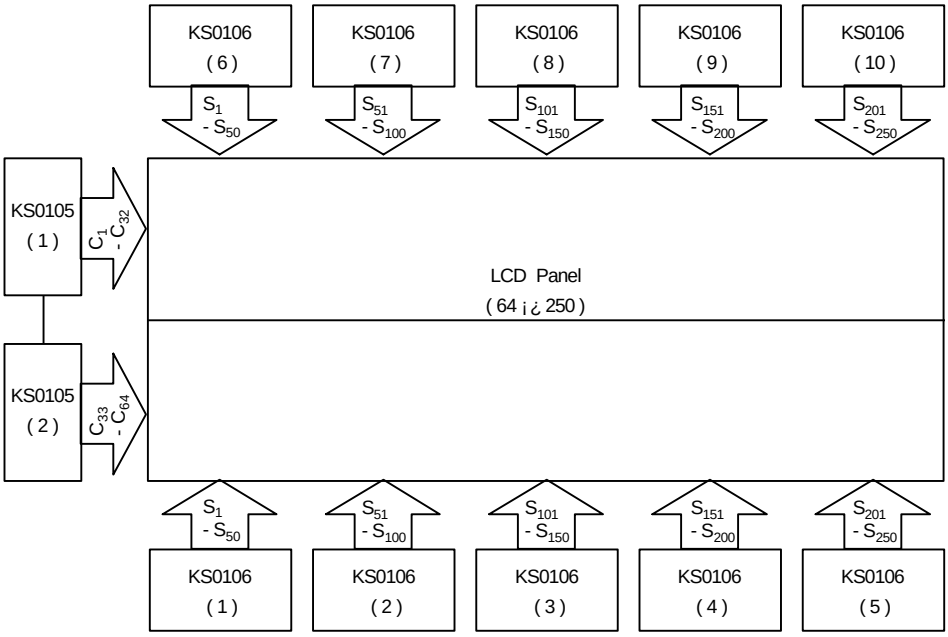


APPLICATION EXAMPLE

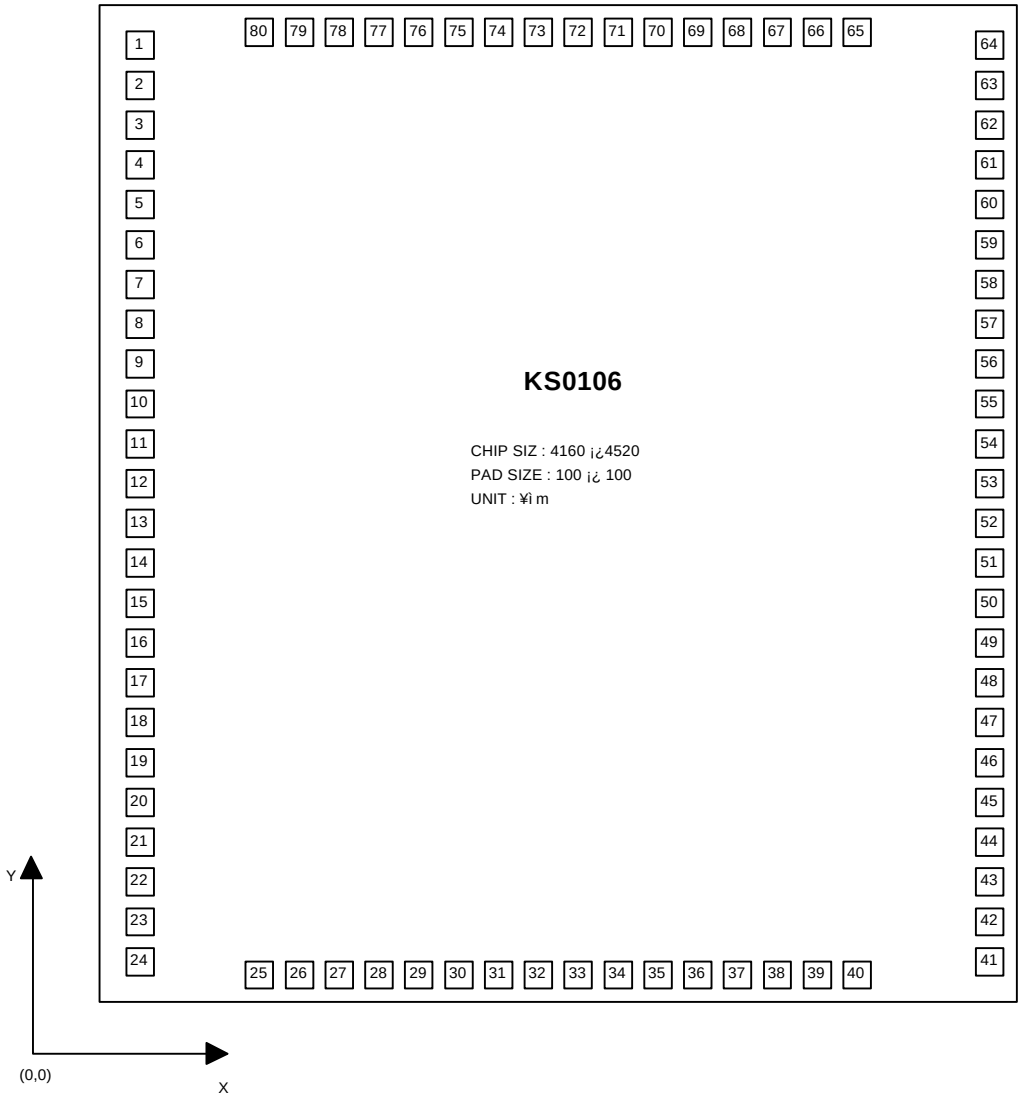
1) Sigle side display (1/32 duty)



2) Double side display (1/64 duty)



PAD DIAGRAM


80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41
25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
KS0106
CHIP SIZ : 4160 ¡¿4520
PAD SIZE : 100 ¡¿ 100
UNIT : ¥i m
Y
(0,0)
X

PAD LOCATION

UNIT (μm)

PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y
1	S39	4042	3498.5	28	S13	128	2946.5	55	DB5	2565	255.5
2	S38	4041	4362.5	29	S12	128	2762.5	56	DB6	2749	255.5
3	S37	3833	4403.5	30	S11	128	2578.5	57	DB7	2933	255.5
4	S36	3649	4403.5	31	S10	128	2394.5	58	FRM	3117	255.5
5	S35	3465	4403.5	32	S9	128	2210.5	59	CL	3301	255.5
6	S34	3281	4403.5	33	S8	128	2026.5	60	CLK1	3485	255.5
7	S33	3097	4403.5	34	S7	128	1842.5	61	CLK2	3669	255.5
8	S32	2913	4403.5	35	S6	128	1658.5	62	NC	*	*
9	S31	2729	4403.5	36	S5	128	1474.5	63	M	3853	255.5
10	S30	2545	4403.5	37	S4	128	1290.5	64	VSS	4042	362.5
11	S29	2361	4403.5	38	S3	128	1106.5	65	VEE	4042	546.5
12	S28	2177	4403.5	39	S2	128	922.5	66	V1	4042	730.5
13	S27	1921	4403.5	40	S1	128	738.5	67	V2	4042	914.5
14	S26	1737	4403.5	41	VDD	128	554.5	68	V3	4042	1098.5
15	S25	1553	4403.5	42	BS	173	255.5	69	V4	4042	1282.5
16	S24	1369	4403.5	43	RSTB	357	255.5	70	S50	4042	1474.5
17	S23	1185	4403.5	44	CS1	541	255.5	71	S49	4042	1658.5
18	S22	1001	4403.5	45	CS2	725	255.5	72	S48	4042	1842.5
19	S21	817	4403.5	46	CS3	909	255.5	73	S47	4042	2026.5
20	S20	633	4403.5	47	E	1093	255.5	74	S46	4042	2210.5
21	S19	449	4403.5	48	R/W	1277	255.5	75	S45	4042	2394.5
22	S18	265	4403.5	49	D/I	1461	255.5	76	S44	4042	2578.5
23	NC	*	*	50	DB0	1645	255.5	77	S43	4042	2762.5
24	S17	128	128	51	DB1	1829	255.5	78	S42	4042	2946.5
25	S16	128	128	52	DB2	2013	255.5	79	S41	4042	3130.5
26	S15	128	128	53	DB3	2197	255.5	80	S40	4042	3314.5
27	S14	128	128	54	DB4	2381	255.5				