

KS0105

32 CH COMMON DRIVER FOR DOT MATRIX LCD

INTRODUCTION

64 QFP

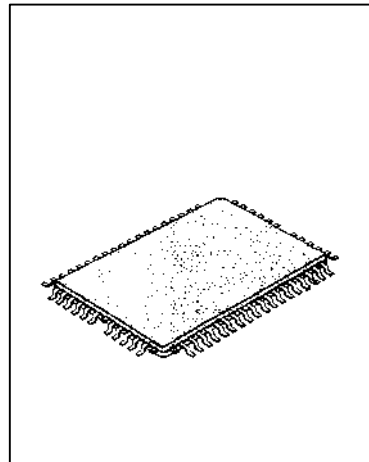
KS0105 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. This device consists of timing generator circuit, 32 bit shift register and 32 bit driver.

FUNCTION

- Dot matrix LCD common driver with 32 channel output
- Input /Output signal
 - Input: bias voltage ($V_1, V_2, V_5, V_6, V_{EE}$)
 - Output; 32 channel waveform for LCD driving and segment driver control pulse.

FEATURE

- Power supply voltage: $+5V \pm 10\%$
- Supply voltage for display: $0 \sim 5.5V (V_{EE})$
- Applicable LCD duty; selectable 7 kinds ($1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64$)
- Interface



COMMON	SEGMENT
Other KS0105	KS0106

- Oscillator frequency can be set by adjusting external capacitor and resistor
- 64 QFP or bare chip available.

BLOCK DIAGRAM

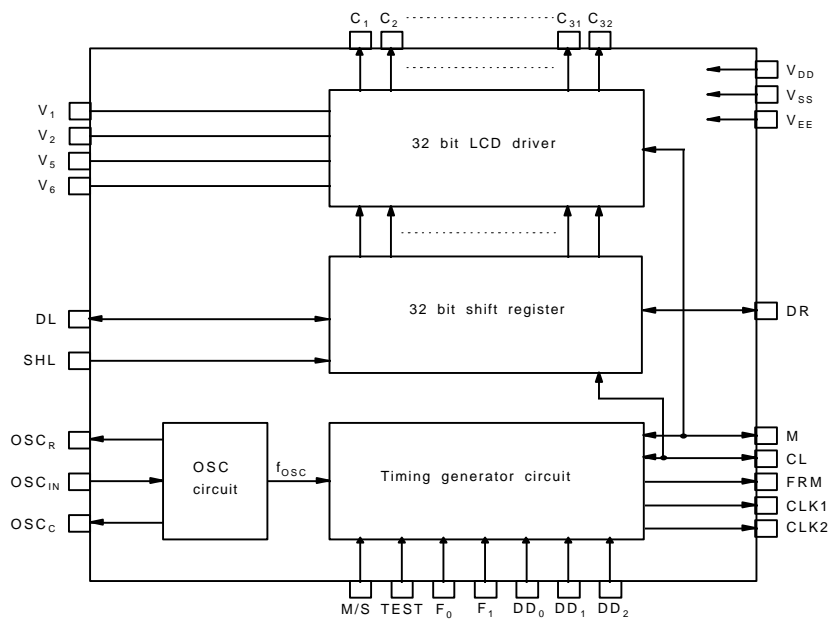
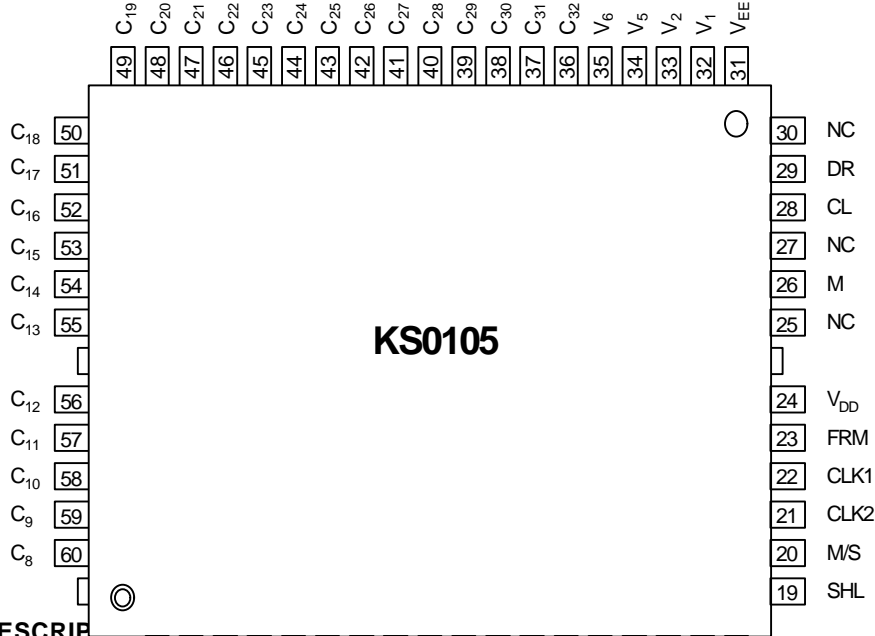


Fig 1. KS0105 Functional block diagram

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PIN CONFIGURATION



PIN DESCRIPTION

PIN(No.)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE				
V _{DD} (24)	Power	Operating Voltage	For internal logic circuit (+5V _{±10%})	Power Supply				
V _{SS} (9)		Ground	For internal logic circuit					
V _{EE} (31)		Negative Supply Voltage	For LCD driver circuit					
OSC _{IN} , OSC _R , OSC _C (15-17)		Oscillator	Generate Oscillation Frequency (refer to note 1)					
C ₁ -C ₃₂ (36-60, 1-7)	Output	Common Output	Common signal output for LCD driving (refer to note 4)	LCD				
DL, DR(8, 29)	Input/Output	Data Input or Output	Data input/output pin of internal shift register	Other KS0105				
M(26)	Input/Output	Alternated Signal For LCD Driver	Alternating signal input pin for LCD driving <table border="1" style="margin-left: 20px;"> <tr> <td>Master mode</td> <td>Output</td> </tr> <tr> <td>Slave mode</td> <td>Input</td> </tr> </table>	Master mode	Output	Slave mode	Input	KS0106
Master mode	Output							
Slave mode	Input							

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PIN DESCRIPTION (continued)

PIN(NO.)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE															
V ₁ , V ₂ (32, 33) V ₅ , V ₆ (34, 35)	Input	Bias Voltage	Bias supply voltage terminals to drive the LCD <table border="1"> <tr> <td>Select level</td> <td>Non-select level</td> </tr> <tr> <td>V₁-V₂</td> <td>V₅-V₆</td> </tr> </table>	Select level	Non-select level	V ₁ -V ₂	V ₅ -V ₆	Power											
Select level	Non-select level																		
V ₁ -V ₂	V ₅ -V ₆																		
CL (28)	Input/Output	Shift Clock	Data Shift Clock <table border="1"> <tr> <td>Master mode</td> <td>Output</td> </tr> <tr> <td>Slave mode</td> <td>Input</td> </tr> </table>	Master mode	Output	Slave mode	Input	KS0106											
Master mode	Output																		
Slave mode	Input																		
FRM (23)	Output	Frame Signal	Synchronous frame signal	KS0106															
SHL (19)	Input	Data Interface	Selection of the shift direction (slave mode) (master mode) <table border="1"> <tr> <td>SHL</td> <td>DL</td> <td>DR</td> <td>SHL</td> <td>Shift Direction</td> </tr> <tr> <td>V_{SS}</td> <td>out</td> <td>in</td> <td>V_{SS}</td> <td>DL₁:DR</td> </tr> <tr> <td>V_{DD}</td> <td>in</td> <td>out</td> <td>V_{DD}</td> <td>DL₁:DR</td> </tr> </table>	SHL	DL	DR	SHL	Shift Direction	V _{SS}	out	in	V _{SS}	DL ₁ :DR	V _{DD}	in	out	V _{DD}	DL ₁ :DR	V _{DD} or V _{SS}
SHL	DL	DR	SHL	Shift Direction															
V _{SS}	out	in	V _{SS}	DL ₁ :DR															
V _{DD}	in	out	V _{DD}	DL ₁ :DR															
CLK1, CLK2 (22, 21)	Output	Operating Clock	Clock for KS0106	KS0106															
TEST (18)	Input	-	Test pin (This pin must be connected V _{DD})	V _{DD}															
DD ₀ -DD ₂ (12-14)	Input	Select Display Duty	Can select the duty ratio according to combination of DD ₀ -DD ₂ (refer to note 2)	V _{DD} or V _{SS}															
F ₀ -F ₁ (10, 11)	Input	Select Frequency	Can select the relationship between oscillator frequency and frame frequency. (refer to note 3)	V _{DD} or V _{SS}															
M/S(20)	Input	Select Master or Slave	<ul style="list-style-type: none"> Master mode: connect V_{DD} Operated the oscillator and timing generation circuit. Slave mode: connected V_{SS} not operated the oscillator and timing generation circuit. Unnecessary pins (F₀, F₁, DD₀-DD₂, TEST) Connect V_{DD} for prevent floating current. 	V _{DD} or V _{SS}															

MAXIMUM ABSOLUTE LIMIT (T_a=25;E)

Characteristics	Symbol	Value	Unit	Test pin
Operating Voltage	V _{DD}	-0.3~+7.0	V	V _{DD} , V _{SS} , V _{EE}
Driver Supply Voltage	V _{LCD} *1	V _{DD} -13.5~V _{DD} +0.3		DL, DR, M, SHL F ₀ , F ₁ , M/S, DD ₀ -DD ₂
Input Voltage	V _{IN1}	-0.3~V _{DD} +0.3		V ₁ , V ₂ , V ₅ , V ₆
	V _{IN2} *2	V _{EE} -0.3~V _{DD} +0.3		
Operating Temperature	T _{OPR}	-20~+75	μA	-
Storage Temperature	T _{STG}	-55~+125		-

* Voltage greater than above may damage to the circuit.

*1 V_{EE} : connect a protection resistor (20Ω±5%)

*2 connect a protection resistor (47Ω±10%)



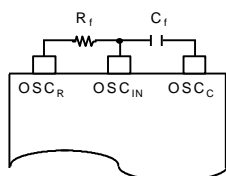
ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, T_a=25°C)

Characteristic	Symbol	condition	Min	Typ	Max	Unit	Applicable Pin	
Operating voltage	V _{DD}	-	4.5	-	5.5	V	V _{DD} , V _{SS}	
Oscillator frequency	f _{OSC}	R _f =68kΩ±2% C _f =10pF±5%	300	430	560	kHz	OSC _R , OSC _{IN} , OSC _C	
Input Voltage	High	V _{IH}	0.7V _{DD}	-	V _{DD}	V	OSC _{IN} , F ₀ , F ₁ , M, DD ₀ -DD ₂ , SHL, M/S CL, DR, DL, TEST	
	Low	V _{IL}	0	-	0.3V _{DD}			
Output voltage	High	V _{OH}	I _{OH} =-400 μs	V _{DD} -0.4	-	-	DL, DR, M, FRM	
	Low	V _{OL}	I _{OL} =400 μs	-	0.4			
On Resistance (V-C)	R _{ON}	V _{EE} =-5V+10% Load Current 150 μs	-	-	1	kΩ	-	
Input Leakage Current	I _{LKG1}	V _{IN} =V _{DD} -V _{SS}	-1	-	1	μs	OSC _{IN} , F ₀ , F ₁ , M, DD ₀ -DD ₂ , SHL, M/S CL, DR, DL, TEST	
		V _{IN} =V _{DD} -V _{EE}	-5	-	5			
Power Dissipation	Master	P _{D1}	RC Oscillation, 430kHz, 1/32 duty R _f =68kΩ±2%, C _f =10pF±5%	-	-	4.4	mW	V _{DD} , V _{SS}
	Slave	P _{D2}	Frame 70Hz, 1/32 duty	-	-	1.1		

Note 1: Oscillation frequency (fosc)

Note 4:



M	D	Output level
H	H	V ₂
	L	V ₆
L	H	V ₁
	L	V ₅

Note 2: Selects frequency Duty

Duty ratio	1/8	1/12	1/16	1/24	1/32	1/48	1/64
DD0	L	L	L	H	H	H	H
DD1	L	H	H	L	L	H	H
DD2	L	H	L	H	L	H	L
Mode	Master mode					Master/slave mode	

Note 3: Selects frequency

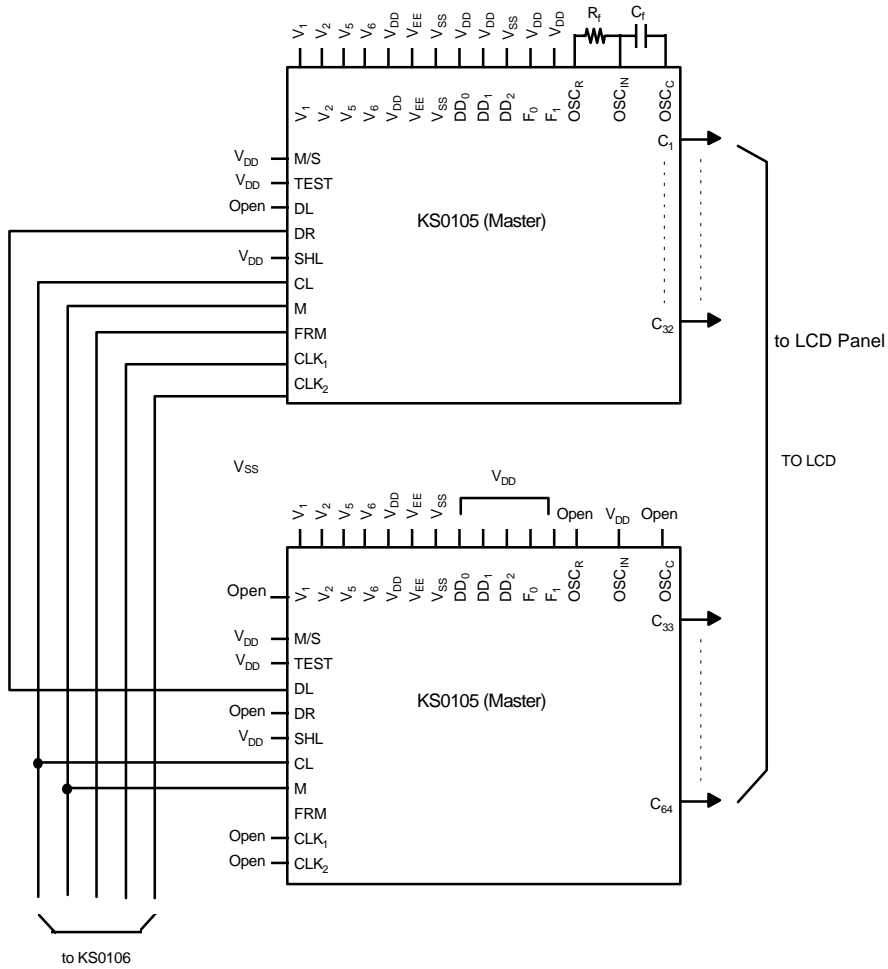
Condition		Oscillator frequency (KHz)	Frame frequency (Hz)	M signal frequency (Hz)	CLK1, CLK2 frequency (KHz)
F ₀	F ₁				
L	L	107.5	70	35	53.8
H	L	107.5	70	35	53.8
L	H	215.0	70	35	107.5
H	H	430.0	70	35	215.0

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APPLICATION CIRCUIT

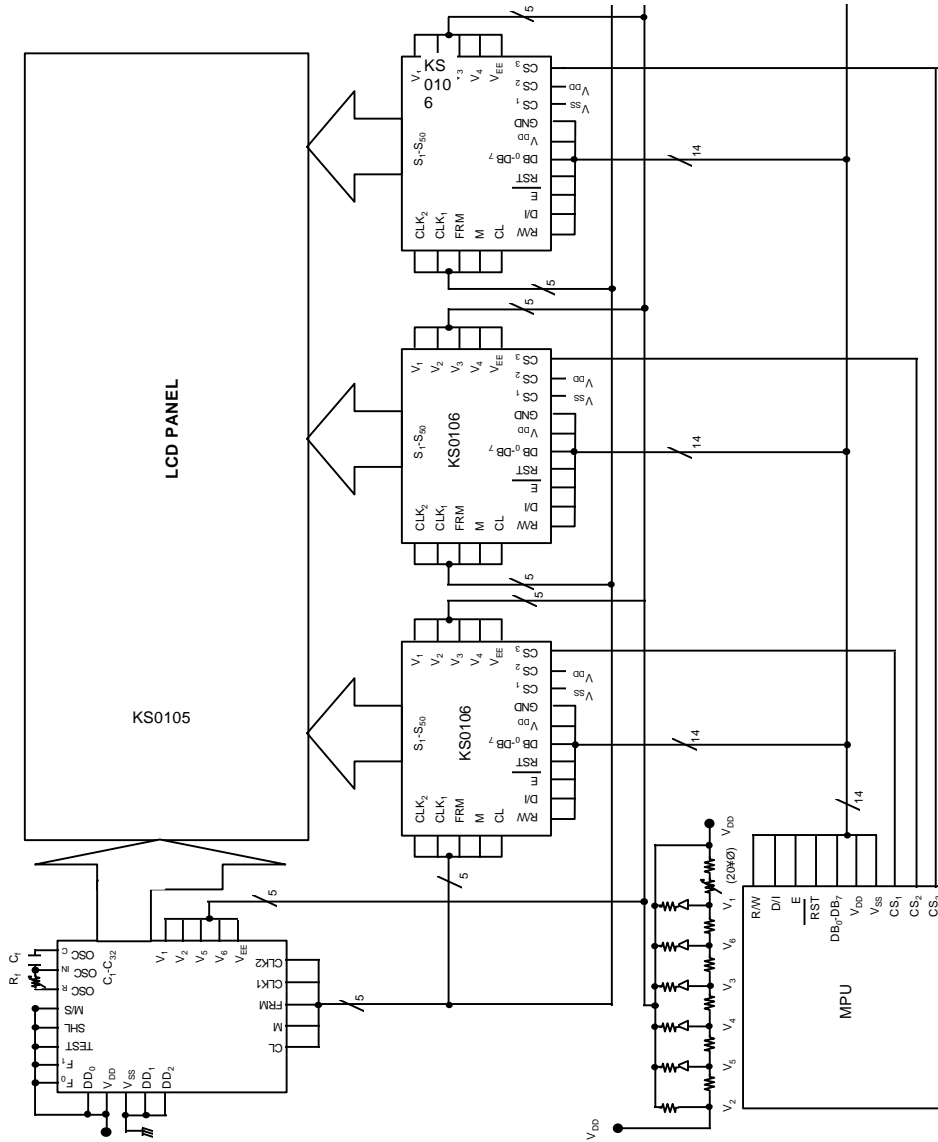
- 1/64 Duty



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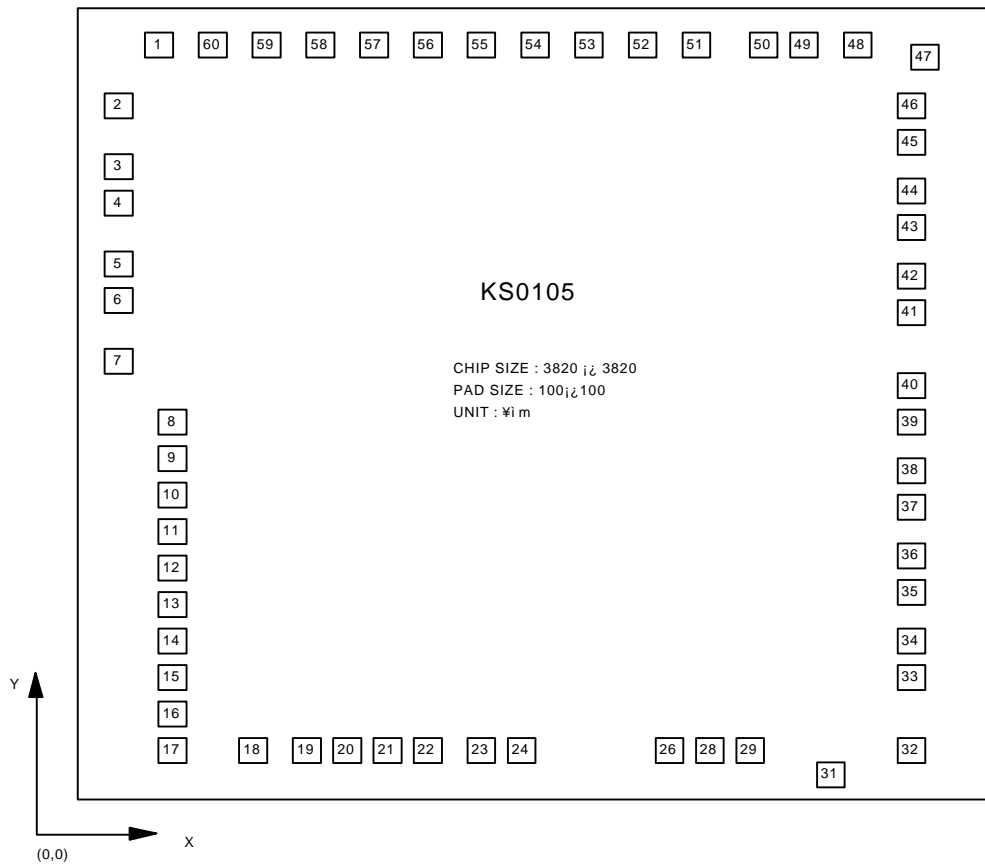
APPLICATION CIRCUIT (continued)



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PAD DIAGRAM



PAD LOCATION

UNIT (μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
1	C7	194.5	3698	33	V2	3699.5	478
2	C6	120.5	3408	34	V5	3699.5	658
3	C5	120.5	3136	35	V6	3699.5	930
4	C4	120.5	2956	36	C32	3699.5	1110
5	C3	120.5	2684	37	C31	3699.5	1382
6	C2	120.5	2504	38	C30	3699.5	1562
7	C1	120.5	2232	39	C29	3699.5	1834
8	DL	249.5	1914	40	C28	3699.5	2014
9	VSS	249.5	1718	41	C27	3699.5	2286
10	F0	249.5	1538	42	C26	3699.5	2466
11	F1	249.5	1354	43	C25	3699.5	2738
12	DD0	249.5	1170	44	C24	3699.5	2918
13	DD1	249.5	986	45	C23	3699.5	3190
14	DD2	249.5	802	46	C22	3699.5	3370
15	OSC _C	249.5	618	47	C21	3699.5	3642
16	OSC _R	249.5	434	48	C20	3642.5	3698
17	OSC _{IN}	249.5	250	49	C19	3190.5	3698
18	TEST	536.5	251	50	C18	3010.5	3698
19	SHL	720.5	251	51	C17	2738.5	3698
20	M/S	904.5	251	52	C16	2558.5	3698
21	CLK2	1088.5	251	53	C15	2286.5	3698
22	CLK1	1272.5	251	54	C14	2106.5	3698
23	FRM	1456.5	251	55	C13	1834.5	3698
24	VDD	1652.5	251	56	C12	1654.5	3698
25	NC	*	*	57	C11	1382.5	3698
26	M	2208.5	251	58	C10	1122.5	3698
27	NC	*	*	59	C9	850.5	3698
28	CL	2392.5	251	60	C8	466.5	3698
29	DR	2576.5	251				
30	NC	*	*				
31	VEE	3396.5	142				
32	V1	3699.5	206				



ELECTRONICS