HIGH-VOLTAGE ANALOG-SIGNAL IC

UCi7066

16COMx40SEG Dot Matrix LCD Controller/Driver

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MP Specifications
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The Coolest LCD Driver, Ever!!

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UCi7066

16COMx40SEG Dot Matrix LCD Controller/Driver

INTRODUCTION

The UCi7066c dot-matrix LCD controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix LCD under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix LCD are internally provided on one chip, a minimal system which can be interfaced with this controller/driver.

The UCi7066c character generator ROM is extended to generate two hundred and forty (240) 5x8 (5x11) dot character fonts for a total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the UCi7066c is suitable for any portable battery-driven product requiring low power dissipation.

The UCi7066c LCD driver consists of 16 COM signal drivers and 40 SEG signal drivers which can extend display size by cascading SEG driver UCi7065 or UCi7063. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single UCi7066c can display up to one 8-character line or two 8-character lines.

MAIN APPLICATIONS

- Portable battery-driven Products

FEATURE HIGHLIGHTS

- 5 x 8 and 5 x 11 dot matrix possible
- Low power operation support: 2.7V ~ 5.5V
- Wide range of LCD driver power: 3.0V ~ 18V
- Correspond to high speed MPU bus interface
  - 2 MHz (when VCC = 5V)
- Support industry standard 4-wire (S8), 3-wire (S9), and 2-wire (I^2C) serial bus and 4-bit or 8-bit parallel bus (6800).
- 80 x 8-bit display RAM (80 characters max.)
- 13,200-bit character generator ROM for a total of 240 character fonts (5x8 dot or 5x11 dot)
- 64 x 8-bit character generator RAM
  - 8 character fonts (5 x 8 dot)
  - 4 character fonts (5 x 11 dot)
- 16-COM x 40-SEG LCD driver
- Programmable duty cycles
  - 1/8 for one line of 5 x 8 dots with cursor
  - 1/11 for one line of 5 x 11 dots & cursor
  - 1/16 for two lines of 5 x 8 dots & cursor
- Wide range of instruction functions:
  Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Automatic reset circuit that initializes the controller/driver after power-ON
- Internal oscillator with external resistors
- Low power consumption
- Packages available:
  - Bare Chip

Remark: Contact UltraChip for a visual inspection document (03-DOC-093).

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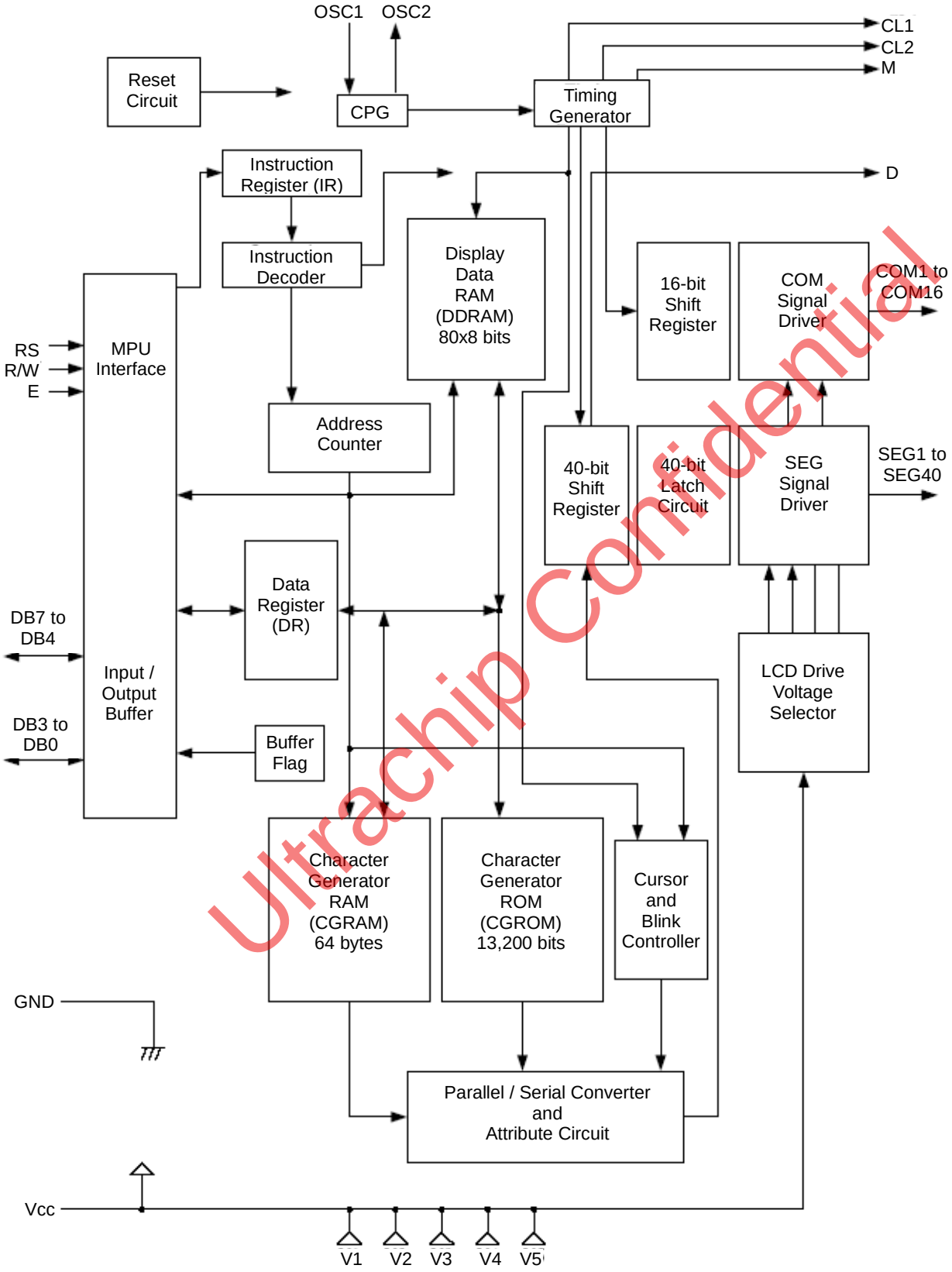
BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	I^2C	Package	Description
UCi7066cBXB-N0-01	Yes	Bare die	Support Character: English / Japan
UCi7066cBXB-N0-02	Yes	Bare die	Support Character: English / European
UCi7066cBXB-N0-03	Yes	Bare die	Support Character: English / European
UCi7066cBXB-N0-05	Yes	Bare die	Support Character: English / European
UCi7066cBXB-N0-06	Yes	Bare die	Support Character: English / European

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General Notes

APPLICATION INFORMATION
For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER
All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

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CONTACT DETAILS
UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Count</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">MPU Pins</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>Register selection.
L: (for write) Instruction register Busy flag
(for read) Address Counter
H: (for write and read) Data register</td></tr>
<tr><td>R/W</td><td>1</td><td>I</td><td>Read or Write selection
L: Write H: Read
<table>
<tr><th>RS</th><th>R/W</th><th>Operation</th></tr>
<tr><td>L</td><td>L</td><td>Instruction Write (MPU writes instruction code into IR)</td></tr>
<tr><td>L</td><td>H</td><td>DB7: Read Busy Flag, DB6~DB0: Address Counter</td></tr>
<tr><td>H</td><td>L</td><td>Data Write (MPU writes data into DR)</td></tr>
<tr><td>H</td><td>H</td><td>Data Read (MPU reads data from DR)</td></tr>
</table></td></tr>
<tr><td>E</td><td>1</td><td>I</td><td>Starts Data-Read or Data-Write</td></tr>
<tr><td>SERMODE</td><td>1</td><td>I</td><td>Mode selection.
L: 6800 mode
H: Serial mode (2-wire/I^2C, 3-wire/S9, or 4-wire/S8)
Connect to L internally.</td></tr>
<tr><td>DB7~DB0</td><td>8</td><td>I/O</td><td>Bi-directional tri-state data bus pins.
Used for data transfer and receive between the MPU and the UCi7066c.
DB7 can be used as a busy flag. DB3~DB0 are not used during 4-bit operation.
<table>
<tr><th>MODE</th><th>SERMODE</th><th>DB7</th><th>DB6</th><th>DB5</th><th>DB4</th><th>DB3</th><th>DB2</th><th>DB1</th><th>DB0</th></tr>
<tr><td>6800 - 4bit</td><td>L</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>--</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>6800 - 8bit</td><td>L</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>S8</td><td>H</td><td>H</td><td>L</td><td>CS1</td><td>SDA</td><td>SCL</td><td>CS0</td><td>--</td><td>--</td></tr>
<tr><td>S9</td><td>H</td><td>H</td><td>H</td><td>CS1</td><td>SDA</td><td>SCL</td><td>CS0</td><td>--</td><td>--</td></tr>
<tr><td>I^2C</td><td>H</td><td>L</td><td>H</td><td>ID1</td><td>ID0</td><td>--</td><td>--</td><td>SCL</td><td>SDA</td></tr>
</table>
In original design, only one chip select I/O, specified in DB[2].
In SPI-S8/S9 mode, SPI-S8/S9 slave is selected when DB[5] (CS1)=”1” and DB[2] (CS0)=”0”.
In I^2C mode, I^2C slave is selected when DB[5]=ID1 (head byte) and DB[4]=ID0 (head byte).</td></tr>
<tr><td colspan="4">Power Supply Pins</td></tr>
<tr><td>V5~V1</td><td>5</td><td>–</td><td>Power supply for LCD drive. Vcc – V5 = 18V (Max.)</td></tr>
<tr><td>Vcc, GND</td><td>2</td><td>–</td><td>Vcc: 2.7V ~ 5.5V
GND: 0V</td></tr>
<tr><td colspan="4">Note: The relationship must be maintained: Vcc ⩾ V1 ⩾ V2 ⩾ V3 ⩾ V4 ⩾ V5</td></tr>
<tr><td colspan="4">LCD pins</td></tr>
<tr><td>COM16~COM1</td><td>16</td><td>O</td><td>COM signals. Unused pins are changed to non-selection waveform.
COM16~COM9 are non-selection waveforms at 1/8 duty factor.
COM16~COM12 are non-selection waveforms at 1/11 duty factor.</td></tr>
<tr><td>SEG40~SEG1</td><td>40</td><td>O</td><td>SEG signals.</td></tr>
</table>

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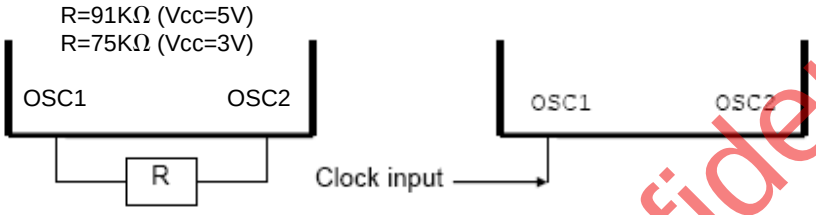
Pin	Count	Type	Description
Extension Driver			
CL1	1	O	Clock to latch serial data D sent to the extension driver.
CL2	1	O	Clock to shift serial data D.
M	1	O	Switch signal for converting the liquid crystal drive waveform to AC.
D	1	O	Character Pattern Data corresponding to each SEG signal.
Oscillation pins			
OSC1, OSC2	2	–	Oscillation resistor clock. When crystal oscillation is performed, a resistor much be connected externally. When the pin input is an external clock, it must be input to OSC1.

Remark: There are two clock options:



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CONTROL REGISTERS

UCi7066 contains registers which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, starting with a summary table, followed by a detailed instruction-by-instruction description.

Bits: Number of Bits of the register.
Default: Numbers shown in Bold font are default values after Power-Up-Reset and System-Reset.

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>I/D</td><td>1</td><td></td><td>Increament/Decreament of DDRAM address (cursor or blink).
0: Cursor/blink moves to left and DDRAM address is decreased by 1.
1: Cursor/blink moves to right and DDRAM address is increased by 1.</td></tr>
<tr><td>S</td><td>1</td><td></td><td>Shift of entire display
When doing DDRAM-read (CGRAM read/write) operation or S = 0, shift of entire display is not performed.
When doing DDRAM write operation and S = 1, shift of entire display is performed according to I/D value (I/D ="1" : shift left, I/D = "0" : shift right).</td></tr>
<tr><td>D</td><td>1</td><td></td><td>Display ON/OFF control bit.
0: Display OFF, but display data are remained in DDRAM.
1: Display ON</td></tr>
<tr><td>C</td><td>1</td><td></td><td>Cursor ON/OFF control bit.
0 : Cursor is disappeared in current display, but I/D remains its data.
1: Cursor is turned ON.</td></tr>
<tr><td>B</td><td>1</td><td></td><td>Cursor Blink ON/OFF control bit.
0: Blink is OFF
1: Cursor blink is ON, that performs alternate between all the high data and display character at the cursor position.</td></tr>
<tr><td>S/C</td><td>1</td><td></td><td>Shift Cursor or Display (right or left).
0: Shift Cursor
1: Shift Display</td></tr>
<tr><td>R/L</td><td>1</td><td></td><td>Shift (cursor or display) Right or Left.
0: Shift Left
1: Shift Right
<table>
<tr><th>S/C</th><th>R/L</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Shift cursor to the left</td></tr>
<tr><td>0</td><td>1</td><td>Shift cursor to the right</td></tr>
<tr><td>1</td><td>0</td><td>Shift display to the left. Cursor shifts together with the display.</td></tr>
<tr><td>1</td><td>1</td><td>Shift display to the right. Cursor shifts together with the display.</td></tr>
</table></td></tr>
<tr><td>DL</td><td>1</td><td></td><td>Interface data length control bit. 8-bit or 4-bit bus mode selecting signal.
0: 4-bit bus mode with MPU. In 4-bit bus mode, it needs to transfer 4-bit data by two times.
1: 8-bit bus mode with MPU.</td></tr>
<tr><td>N</td><td>1</td><td></td><td>Display line number control bit
0: 1-line display mode.
1: 2-line display mode is set.</td></tr>
<tr><td>F</td><td>1</td><td></td><td>Display font type control bit
0: 5x8 dots format display mode
1: 5x11 dots format display mode.</td></tr>
</table>

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Name	Bits	Default	Description
AC	7		DDRAM/CGRAM address, transferred from IR. After Writing to or reading from DDRAM/CGRAM, AC is automatically +1 (increased by 1) or -1 (decreased by 1), respectively.
BF	1		BUSY Flag. 1: BUSY. Internal operation is being processed.

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COMMAND TABLE

The following is a list of host commands supported by UCi7066

R/S: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: –: Don't Care

#	Command	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Action
1	Clear Display	0	0	0	0	0	0	0	0	0	1	Clear the screen
2	Return Home	0	0	0	0	0	0	0	0	1	–	Move cursor to HOME
3	Set Entry Mode	0	0	0	0	0	0	0	1	I/D	S	I/D: Left / Right S: Shift OFF/ON
4	Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D: Display OFF / ON C: Cursor OFF / ON B: Blink OFF / ON
5	Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	–	–	S/C: Screen / Cursor R/L Right / Left
6	Set Function	0	0	0	0	1	DL	N	F	–	–	DL: 4-bit / 8-bit, N: 1-line / 2-line F: 5x8 / 5x11
7	Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	
8	Set DDRAM address	0	0	1	AC12	AC11	AC10	AC9	AC8	AC7	AC6	
9	Read Busy Flag and address	0	1	BF	AC19	AC18	AC17	AC16	AC15	AC14	AC13	
10	Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to RAM
11	Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from RAM
For S8/S9 Mode												
12	Status Read	1	1	0	0	0	0	0	0	0	0	Read status
		0	1	BF	AC19	AC18	AC17	AC16	AC15	AC14	AC13	

Note:

Ensure that UCi7066 is not in the BUSY state (BF = 0) before sending an instruction from the MPU to the UCi7066. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself.

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COMMAND DESCRIPTION

R/S: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: –: Don't Care

(1) CLEAR DISPLAY

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Write spaces to DDRAM addresses	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

This command clears all the display data by writing "20H" (space code) to all DDRAM address, and sets DDRAM address to "00H" into AC (address counter). It returns cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

(2) RETURN HOME

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Return Cursor to its original point	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**-**

This command returns cursor Home. It sets DDRAM address to "00H" into the address counter, returns cursor to its original site and returns display to its original status, if shifted. Contents of DDRAM do not change.

(3) SET ENTRY MODE

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set Shift ON/OFF, Right/Left	0	0	**0**	**0**	**0**	**0**	**0**	**1**	I/D	S

This command set the moving direction of cursor and display.

I/D: Increment / Decrement of DDRAM address (cursor or blink).

0: Cursor/blink moves to left and DDRAM address is decreased by 1.

1: Cursor/blink moves to right and DDRAM address is increased by 1.

CGRAM operates the same as DDRAM, when read from or write to CGRAM.

S: Shift of entire display

When doing DDRAM-read (CGRAM read/write) operation or S = 0, shift of entire display is not performed.

When doing DDRAM write operation and S = 1, shift of entire display is performed according to I/D value (I/D ="1" : shift left, I/D = "0" : shift right).

S	I/D	Effect
0	--	(Shift not performed)
1	0	Shift the display to the right
	1	Shift the display to the left

(4) DISPLAY ON/OFF

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set display, cursor, and blink ON/OFF	0	0	**0**	**0**	**0**	**0**	**1**	D	C	B

This command controls the display/cursor/blink ON/OFF's 1-bit register.

D: Display ON/OFF control bit.

0: Display OFF, but display data are remained in DDRAM.

1: Display ON

C: Cursor ON/OFF control bit.

0: cursor is disappeared in current display, but I/D remains its data.

1: Cursor is turned ON.

B: Cursor Blink ON/OFF control bit.

0: Blink is OFF

1: Cursor blink is ON, that performs alternate between all the high data and display character at the cursor position.

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(5) CURSOR OR DISPLAY SHIFT

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Shift Cursor or display right / left	0	0	**0**	**0**	**0**	**1**	S/C	R/L	**-**	**-**

Shift right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all lines. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC
0	0	Shift cursor to the left	AC=AC-1
0	1	Shift cursor to the right	AC=AC+1
1	0	Shift display to the left. Cursor follows the display shift.	AC=AC
1	1	Shift display to the right. Cursor follows the display shift.	AC=AC

(6) SET FUNCTION

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Select bus mode, display mode	0	0	**0**	**0**	**1**	DL	N	F	**-**	**-**

DL: Interface data length control bit. 8-bit or 4-bit bus mode selecting signal.

0: 4-bit bus mode with MPU. In 4-bit bus mode, it needs to transfer 4-bit data by two times.

1: 8-bit bus mode with MPU.

N: Display line number control bit

0: 1-line display mode.

1: 2-line display mode is set.

F: Display font type control bit

0: 5x8 dots format display mode

1: 5x11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5x8	1/8
	1	1	5x11	1/11
1	--	2	5x8	1/16

(7) SET CGRAM ADDRESS

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set CGRAM address=AC[5:0]	0	0	0	1	#	#	#	#	#	#

This command sets CGRAM address to AC, and makes CGRAM data available from MPU.

(8) SET DDRAM ADDRESS

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set DDRAM address=AC[6:0]	0	0	1	#	#	#	#	#	#	#

This command sets DDRAM address to AC and makes DDRAM data available from MPU.

In 1-line display mode (when N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (when N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

(9) READ BUSY FLAG AND ADDRESS

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Read BF & AC[6:0]	0	1	BF	#	#	#	#	#	#	#

BF: BUSY Flag.

1 : BUSY. Internal operation is being processed. The next instruction cannot be accepted during this time.

AC: stores DDRAM/CGRAM address, transferred from IR. After Writing to or reading from DDRAM/CGRAM, AC is automatically increased or decreased by 1, respectively.

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(10) WRITE DATA TO CGRAM OR DDRAM

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Write 1-byte data to RAM	1	0	#	#	#	#	#	#	#	#

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM (or CGRAM) is set by the previous address set instruction “Set DDRAM Address” (or “Set CGRAM Address”). Set RAM instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased or decreased by 1, according to the entry mode.

(11) READ DATA FROM CGRAM OR DDRAM

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Read 1-byte data from RAM	1	1	#	#	#	#	#	#	#	#

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous Set address instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

■ For S8/S9 mode

(12) STATUS READ

Action	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Read Status	1	1	0	0	0	0	0	0	0	0
	0	1	BF	AC19	AC18	AC17	AC16	AC15	AC14	AC13

BF: BUSY Flag.

1 : BUSY. Internal operation is being processed. The next instruction cannot be accepted during this time.

AC: stores DDRAM/CGRAM address, transferred from IR. After Writing to or reading from DDRAM/CGRAM, AC is automatically increased or decreased by 1, respectively.

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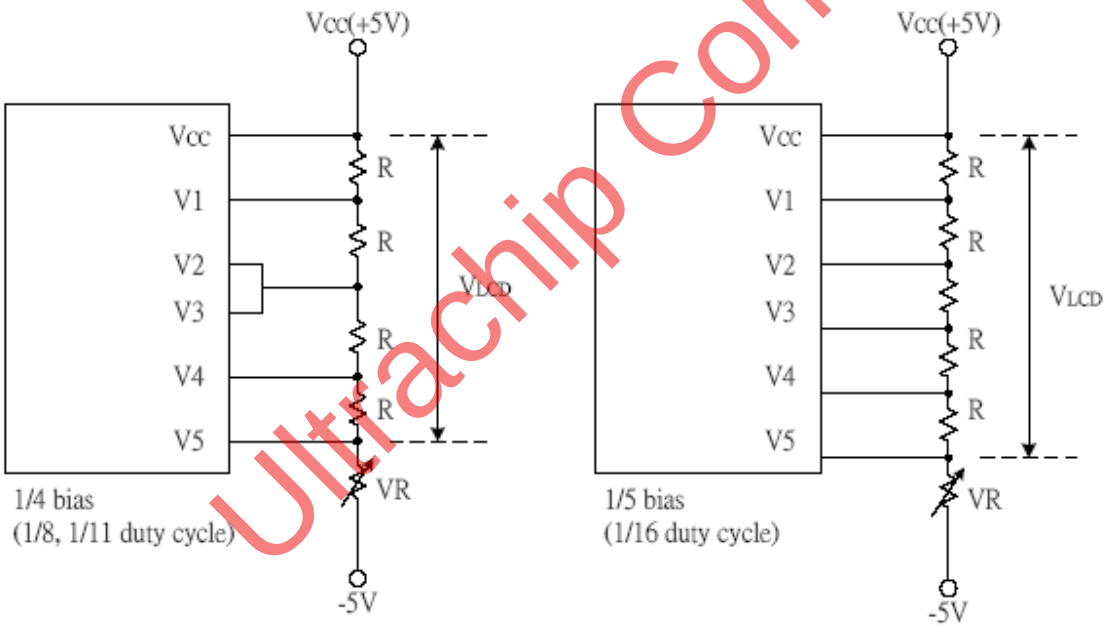
LCD DRIVER CIRCUIT

Supply Voltage for LCD Drive

There are different voltages that supply to UCi7066c's pins (V1~V5) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

Supply Voltage	Duty Factor : 1/8, 1/11 Bias : 1/4	Duty Factor : 1/16 Bias : 1/5
V1	$Vcc - \frac{1}{4} V_{LCD}$	$Vcc - \frac{1}{5} V_{LCD}$
V2	$Vcc - \frac{1}{2} V_{LCD}$	$Vcc - \frac{2}{5} V_{LCD}$
V3	$Vcc - \frac{1}{2} V_{LCD}$	$Vcc - \frac{3}{5} V_{LCD}$
V4	$Vcc - \frac{3}{4} V_{LCD}$	$Vcc - \frac{4}{5} V_{LCD}$
V5	$Vcc - V_{LCD}$	$Vcc - V_{LCD}$



If VEE ≤13V, VR is not required; while if VEE>13V, VR is needed (500~1K)

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RESET & POWER MANAGEMENT

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the UCi7066c when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5x8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note:

If the electrical characteristics conditions listed in the table Power Supply Conditions are not met, the internal reset circuit will not operate normally and will fail to initialize the UCi7066c. For such a case, initialization must be performed by the MPU as explain below:

Initializing by Instruction

8-bit Interface (fosc=270kHz)

1. Power ON
2. Wait >40mS after Vcc>4.5V
3. Set Function

RS	R/W	DB7~0							
0	0	**0**	**0**	**1**	**1**	**N**	**F**	**-**	**-**

(BF cannot be checked before this instruction.)

4. Wait > 37uS
5. Set Function

RS	R/W	DB7~0							
0	0	**0**	**0**	**1**	**1**	**N**	**F**	**-**	**-**

(BF cannot be checked before this instruction.)

6. Wait > 37uS
7. Display ON/OFF control

RS	R/W	DB7~0							
0	0	**0**	**0**	**0**	**0**	**1**	**D**	**C**	**B**

8. Wait > 37uS
9. Display clear

RS	R/W	DB7~0							
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

10. Wait > 1.52mS
11. Set Entry mode

RS	R/W	DB7~0							
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**I/D**	**S**

4-bit Interface (fosc=270kHz)

1. Power ON
2. Wait >40mS after Vcc>4.5V
3. Set Function

RS	R/W	DB7~0							
0	0	**0**	**0**	**1**	**1**	**-**	**-**	**-**	**-**

(BF cannot be checked before this instruction.)

4. Wait > 37uS
5. Set Function

RS	R/W	DB7~0							
0	0	**0**	**0**	**1**	**0**	**-**	**-**	**-**	**-**
0	0	**N**	**F**	**-**	**-**	**-**	**-**	**-**	**-**

(BF cannot be checked before this instruction.)

6. Wait > 37uS
7. Set Function

RS	R/W	DB7~0							
0	0	**0**	**0**	**1**	**0**	**-**	**-**	**-**	**-**
0	0	**N**	**F**	**-**	**-**	**-**	**-**	**-**	**-**

(BF cannot be checked before this instruction.)

8. Wait > 37uS
9. Display ON/OFF control

RS	R/W	DB7~0							
0	0	**0**	**0**	**0**	**0**	**-**	**-**	**-**	**-**
0	0	**1**	**D**	**C**	**B**	**-**	**-**	**-**	**-**

10. Wait > 37uS
11. Display clear

RS	R/W	DB7~0							
0	0	**0**	**0**	**0**	**0**	**-**	**-**	**-**	**-**
0	0	**0**	**0**	**0**	**1**	**-**	**-**	**-**	**-**

12. Wait > 1.52mS
13. Set Entry mode

RS	R/W	DB7~0							
0	0	**0**	**0**	**0**	**0**	**-**	**-**	**-**	**-**
0	0	**0**	**0**	**I/D**	**S**	**-**	**-**	**-**	**-**

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Initial Program Code Example for 8051 MPU (8-bit Interface)

```
;-----------------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK       ;CURSOR MOVES TO RIGHT
        CALL    DELAY37uS
;-----------------------------------------------------------------------
MAIN_START:

        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
;-----------------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        CLR     RS                      ;EX:Port 3.0
        CLR     RW                      ;EX:Port 3.1
        SETB    E                       ;EX:Port 3.2
        MOV     P1,A                    ;EX:Port 1=Data Bus
        CLR     E
        MOV     P1,#FFH                 ;For Check Busy Flag
        RET
;-----------------------------------------------------------------------
CHK_BUSY:                               ;Check Busy Flag
        CLR     RS
        SETB    RW
        SETB    E
        JB      P1.7,$
        CLR     E
        RET
```

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Initial Program Code Example for 8051 MPU (4-bit Interface)

```
;-----------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK
        CALL    DELAY37uS
;-----------------------------------------------------------
MAIN_START:
        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
```

```
;-----------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        PUSH    A
        ANL     A,#F0H
        CLR     RS              ;EX:Port 3.0
        CLR     RW              ;EX:Port 3.1
        SETB    E               ;EX:Port 3.2
        MOV     P1,A            ;EX:Port1=Data Bus
        CLR     E
        POP     A
        SWAP    A
WRINS_ONCE:
        ANL     A,#F0H
        CLR     RS
        CLR     RW
        SETB    E
        MOV     P1,A
        CLR     E
        MOV     P1,#FFH         ;For Check Bus Flag
        RET
;-----------------------------------------------------------
CHK_BUSY:                       ;Check Busy Flag
        PUSH    A
        MOV     P1,#FFH
$1
        CLR     RS
        SETB    RW
        SETB    E
        MOV     A,P1
        CLR     E
        MOV     P1,#FFH
        CLR     RS
        SETB    RW
        SETB    E
        NOP
        CLR     E
        JB      A.7,$1
        POP     A
        RET
```

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HOST INTERFACE

The UCi7066c supports 1 parallel bus protocols, 6800 (8-bit bus width), and 3 serial bus protocols (4-wire, 3-wire, and 2-wire). Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Connect unused control pins and data bus pins to V_{DD} or V_{SS}.

DL:

This chip has all two kinds of interface type with MPU: 4-bit bus and 8-bit bus. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

DL=0	4-bit bus mode
DL=1	8-bit bus mode

During read or write operation, two 8-bit registers are used: data register (DR) and instruction register (IR).

DR:

The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

IR:

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

RS, R/W:

To select register, use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction-Write operation (MPU Write Instruction code into IR)
L	H	Read Busy Flag (DB7) and address counter (DB0~DB6)
H	L	Data-Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Table: Various kinds of operations according to RS and R/W bits

Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High. Before checking BF, be sure to wait at least 80uS. Do NOT always keep the "E" pin "High" for checking BF.

Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

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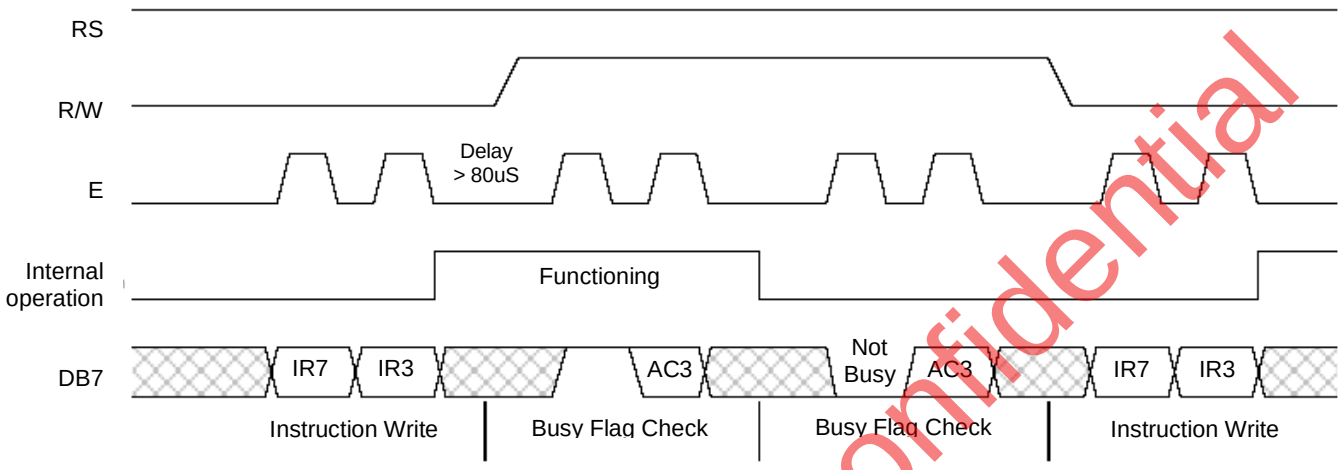
PARALLEL INTERFACE

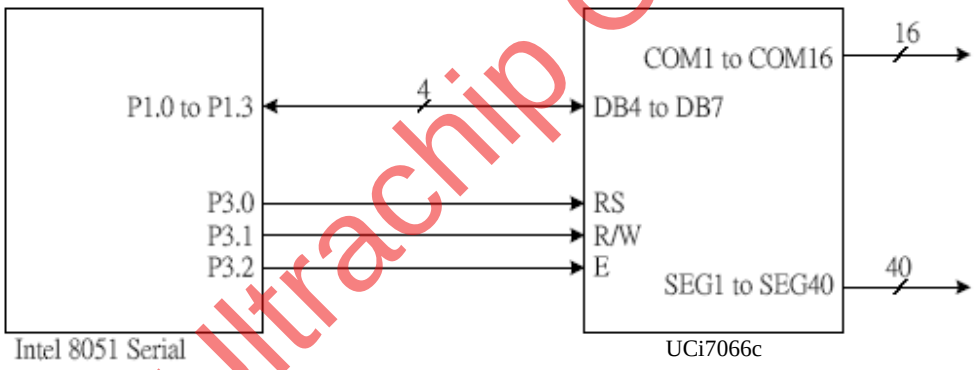
4-bit Interface

For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the UCi7066c and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

Example of Busy Flag Check timing sequence



Intel 8051 interface



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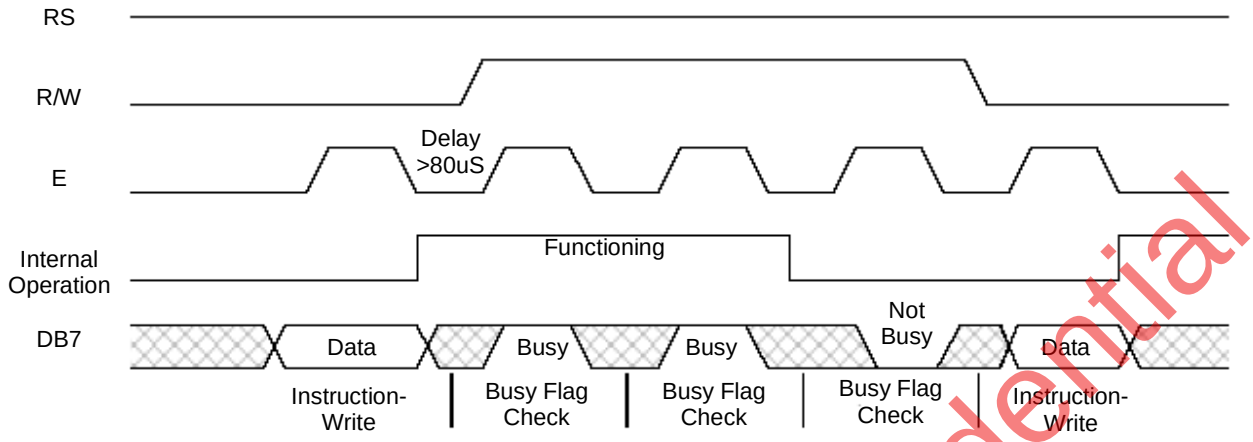
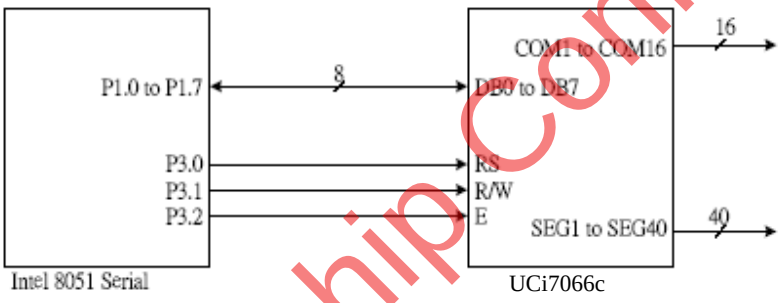
8-bit Interface

For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

Example of Busy Flag Check timing sequence



Intel 8051 Interface



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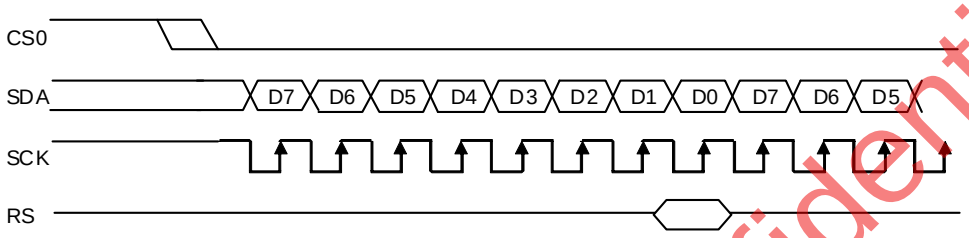
SERIAL INTERFACE

UCi7066 supports 3 serial modes, one 4-wire SPI mode (S8), one 3-wire SPI mode (S9) and one 2-wire mode (I^2C). Bus interface mode is determined by the wiring of the SERMODE. D[7:6]. See table in last page for more detail.

S8 (4-wire) Interface

Only write operations are supported in 4-wire serial mode. Pins CS[1:0] are used for chip select and bus cycle reset. Pin RS is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If RS=0, the data byte will be decoded as command. If RS=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin RD is examined when SCK is pulled low for the LSB (D3) of each token.

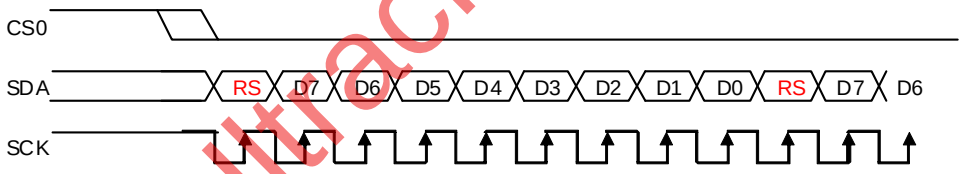


4-wire Serial Interface (S8)

S9 (3-wire) Interface

Only write operations are supported in this 3-wire serial mode. Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is RS, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If RS=0, the data byte will be decoded as command. If RS=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending RS information explicitly in the bit stream, control pin RS is not used, and should be connected to either VDD or VSS. The toggle of CS0 for each byte of data/command is recommended but optional.



3-wire Serial Interface (S9)

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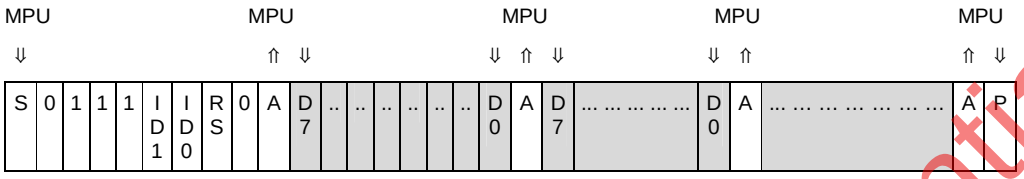
2-wire Serial Interface (I^2C)

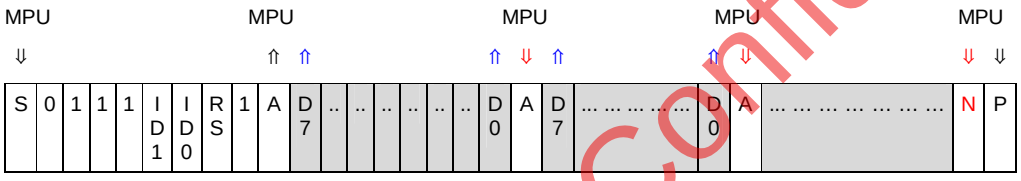
When SERMODE is set to “H” and D[7:6] are set to ”LH”, UCi7066 is configured as a I^2C Bus signaling protocol compliant slave device. Please refer to I^2C standard for details of the bus signaling protocol. Please refer to AC Characteristic section for timing parameters of UltraChip implementation.

Each UCi7066c’s I^2C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (RS, 0:Control, 1:Data), and the direction of the transfer (R/W, 0:Write, 1:Read).

Since both WR and RS are expressed explicitly in the header byte, the control pins CS[1:0], R/W, RD and RS are not used in I^2C mode and should be connected to VSS.



2-wire Serial Interface (I^2C) – Write mode



2-wire Serial Interface (I^2C) – Read mode

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DISPLAY DATA RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure below for the relationships between DDRAM addresses and positions on the LCD.

Higher order bits			Lower order bits				Example: DDRAM Address 4Fh.						
AC6	AC5	AC4	AC3	AC2	AC1	AC0	1	0	0	1	1	1	1

Figure: DDRAM Address

The DDRAM address (ADD) is set in the address counter (AC) as hexadecimal.

1-line display (N = 0)

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the UCi7066, 8 characters are displayed. See Figure below.

Display Position (Digit)	1	2	3	4	5	6		78	79	80
DDRAM Address	00	01	02	03	04	05	… …	4D	4E	4F

Figure: 1-line Display

When the display shift operation is performed, the DDRAM address shifts. (See the Figure below.)

Display Position	1	2	3	4	5	6	7	8
DDRAM Address	00	01	02	03	04	05	06	07
For shift left	01	02	03	04	05	06	07	08

Display Position	1	2	3	4	5	6	7	8
DDRAM Address	00	01	02	03	04	05	06	07
For shift right	4F	00	01	02	03	04	05	06

Figure: 1-line x 8-character Display Example

2-line display (N = 1)

Case 1: When the number of display characters is less than 40x2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the UCi7066c is used, 8 characters x 2 lines are displayed. See Figure below.

Display Position	1	2	3	4	5	6		38	39	40
DDRAM Address	00	01	02	03	04	05	… …	25	26	27
(Hex)	40	41	42	43	44	45	… …	65	66	67

Figure: 2-line Display

Case 2: For a 16-character x 2-line display, the UCi7066 can be extended using one 40-output extension driver. When display shift operation is performed, the DDRAM address shifts. See Figure below.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure: 2-line x 16-character Display Example

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Character Generator ROM (CGROM)

The character generator ROM generates 5x8-dot or 5x11-dot character patterns from 8-bit character codes. It can generate 240 5x8-dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 11 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of the table in the Appendix section to show the character patterns stored in CGRAM.

See the table below for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

LCD Driver Circuit

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40-bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch.

In 1-line display mode case, COM1~COM8 have 1/8 duty or COM1~COM11 have 1/11duty, and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position.
   The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.
   If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown in the table below, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 for non-selection.

"-" indicates no effect.

Character Code (DDRAM Data)								CGRAM Addr.						Character Patterns (CGRAM Data)							
B7	B6	B5	B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
					0	0	0				0	0	1				0	0	1	0	0
					0	0	0				0	1	0				0	0	1	0	0
					0	0	0				0	1	1				0	0	1	0	0
					0	0	0				1	0	0				0	0	1	0	0
					0	0	0				1	0	1				0	0	1	0	0
					0	0	0				1	1	0				0	0	1	0	0
					0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
					0	0	1				0	0	1				1	0	0	0	1
					0	0	1				0	1	0				1	0	0	0	1
					0	0	1				0	1	1				1	1	1	1	0
					0	0	1				1	0	0				1	0	1	0	0
					0	0	1				1	0	1				1	0	0	1	0
					0	0	1				1	1	0				1	0	0	0	1
					0	0	1				1	1	1				0	0	0	0	0

Relationship among CGRAM Addresses, Character Codes (DDRAM), and Character patterns (CGRAM Data)

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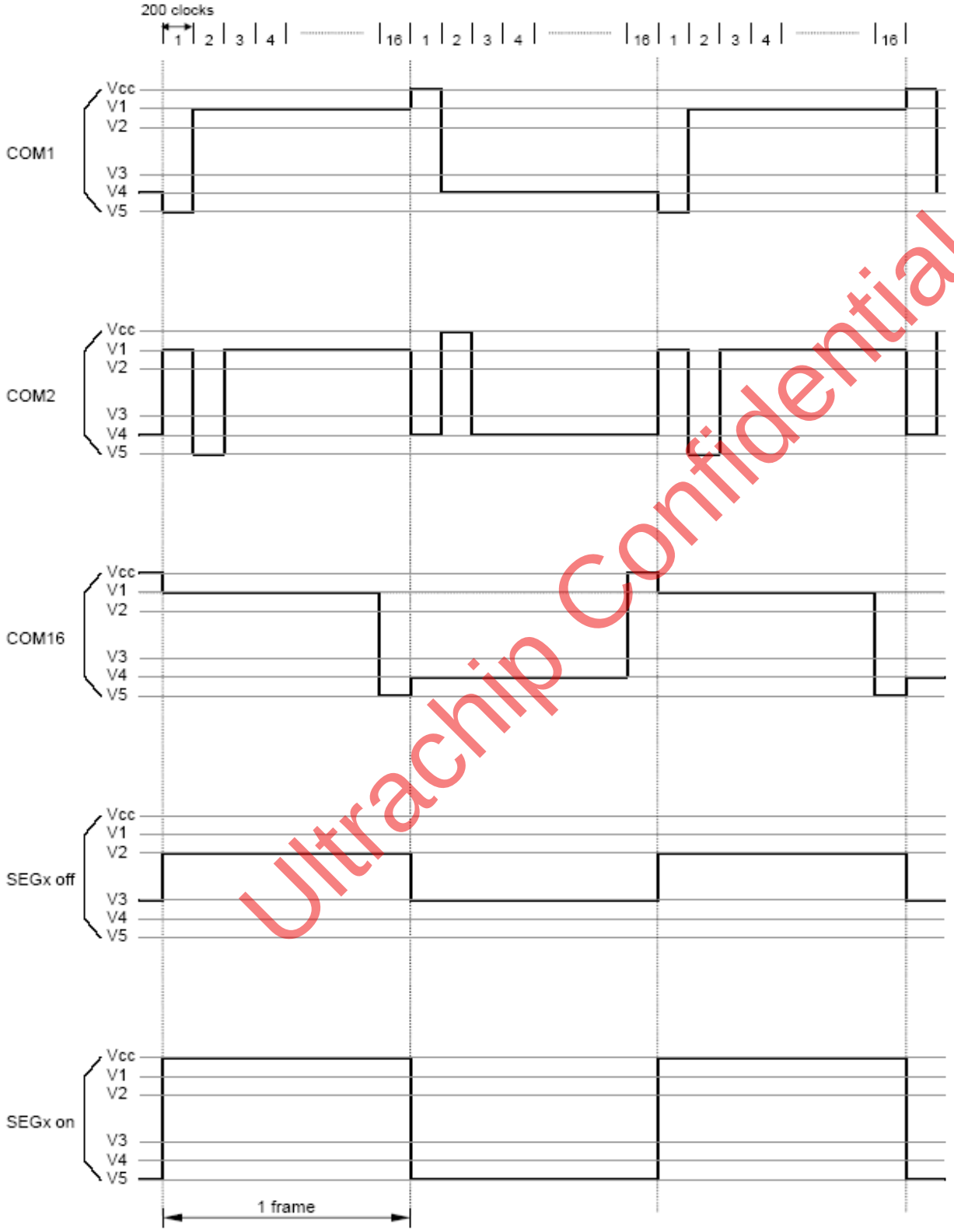
LCD Frequency

Assuming the oscillation frequency = 270kHz, 1 clock cycle time = 3.7uS, 1/16 duty; 1/5 bias,

➔ 1 frame = 3.7uS x 200 x 16 = 1184uS = 11.8mS (84.7Hz)



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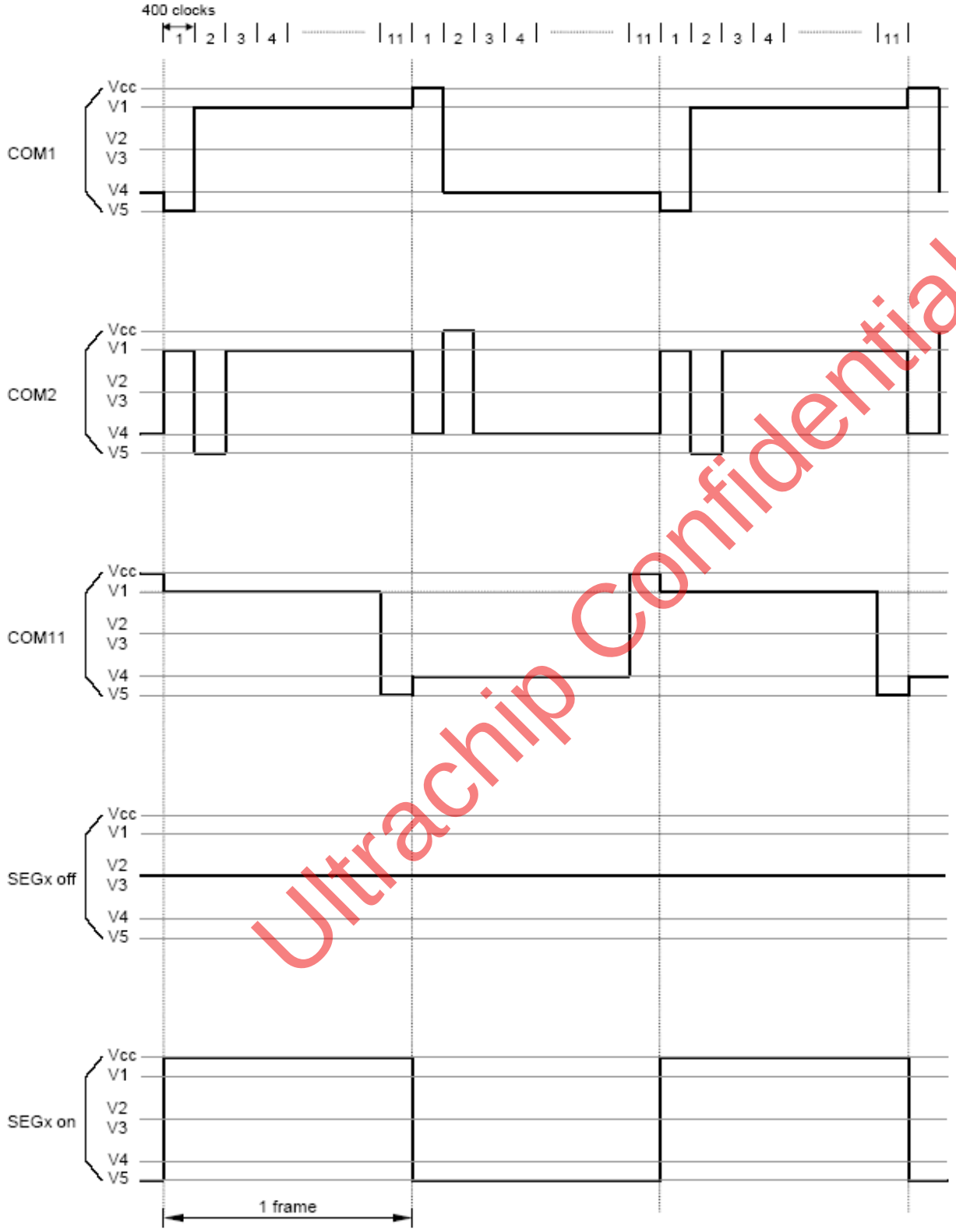
Assuming the oscillation frequency = 270kHz, 1 clock cycle time = 3.7uS, 1/11 duty; 1/4 bias,

➔ 1 frame = 3.7uS x 400 x 11 = 16280uS = 16.3mS (61.3Hz)



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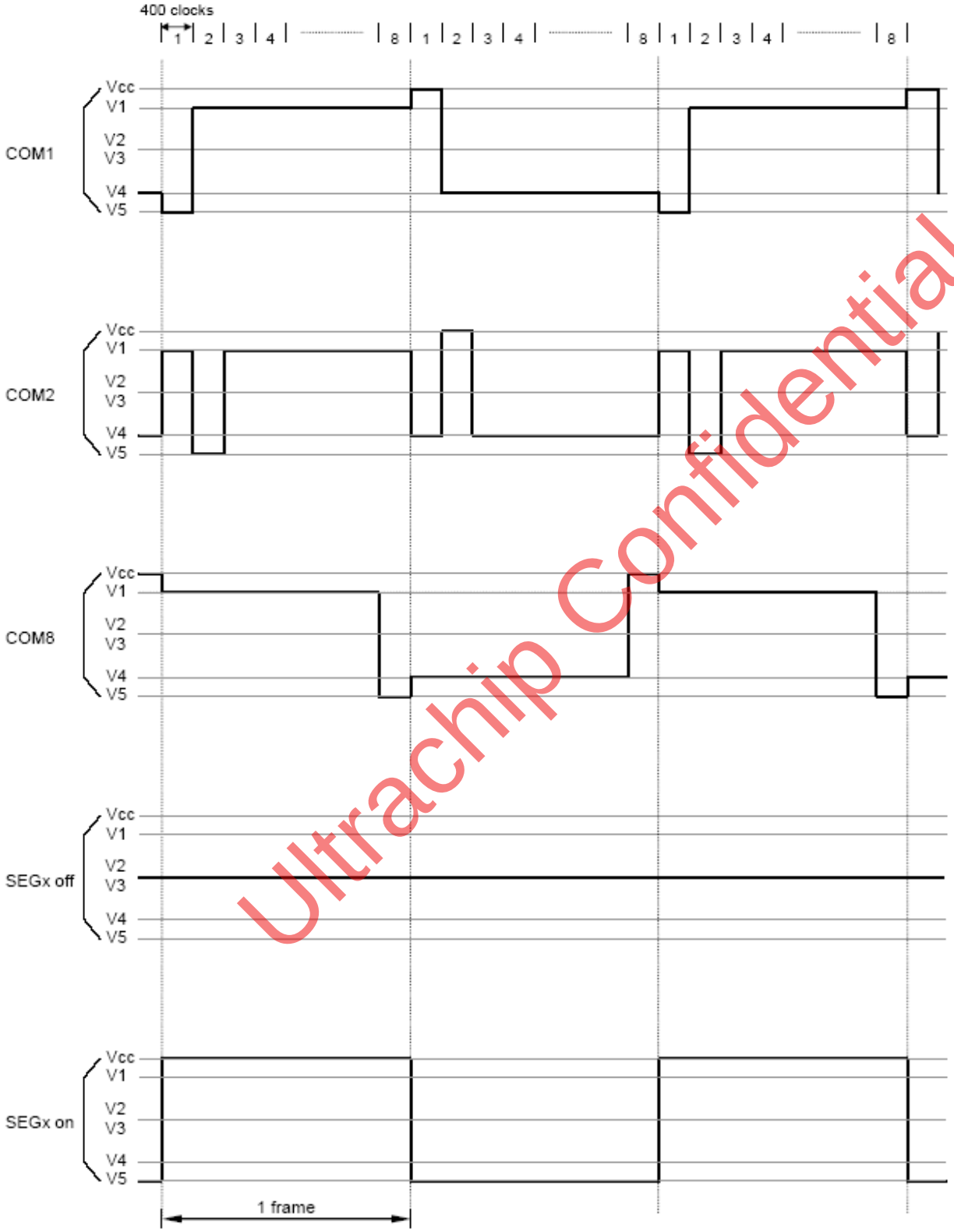
Assuming the oscillation frequency = 270kHz, 1 clock cycle time = 3.7uS, 1/8 duty; 1/4 bias,

➔ 1 frame = 3.7uS x 400 x 8 = 11840uS = 11.8mS (84.7Hz)



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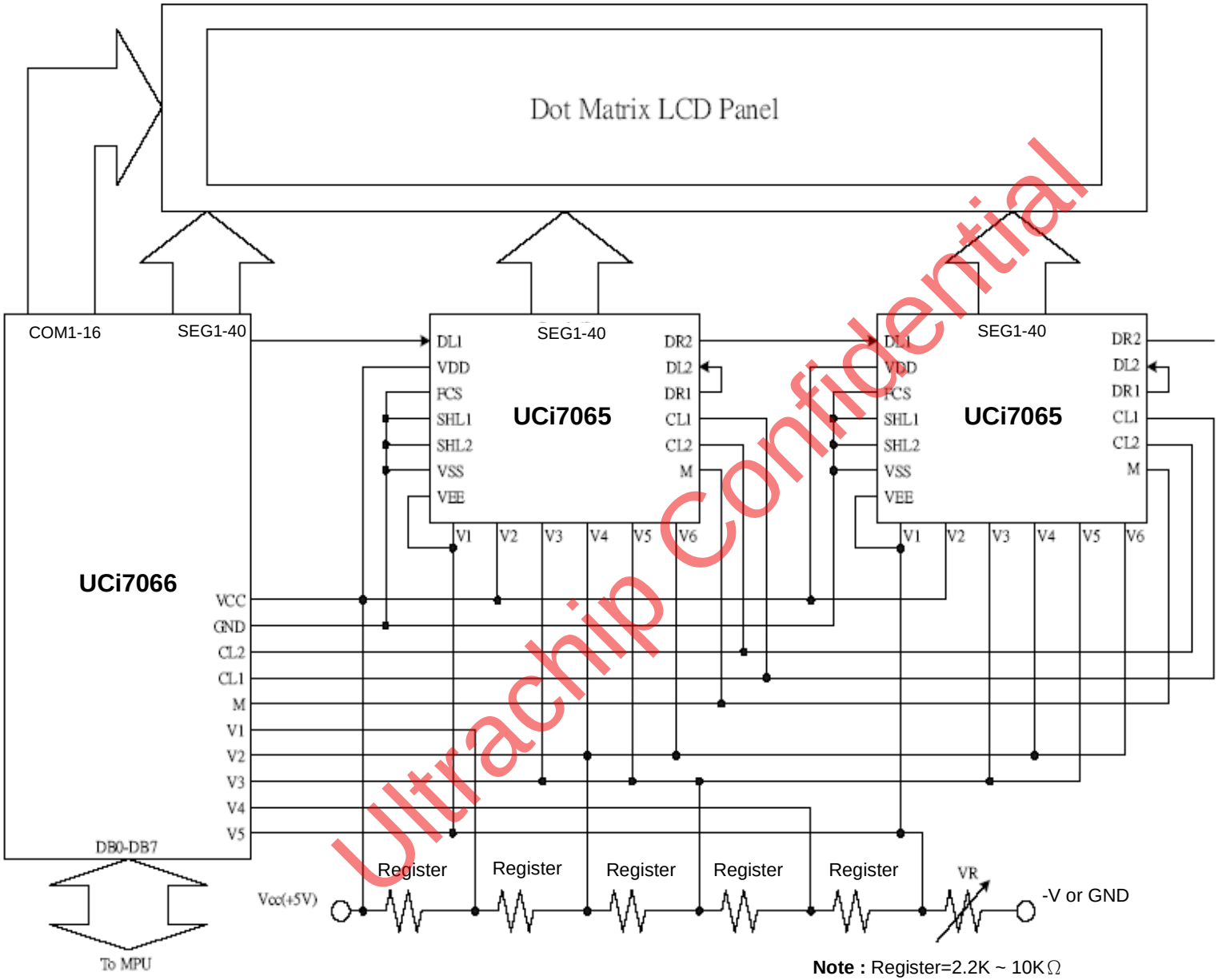
APPLICATION CIRCUIT



Note : Register=2.2K ~ 10KΩ
VR=10K ~ 30KΩ

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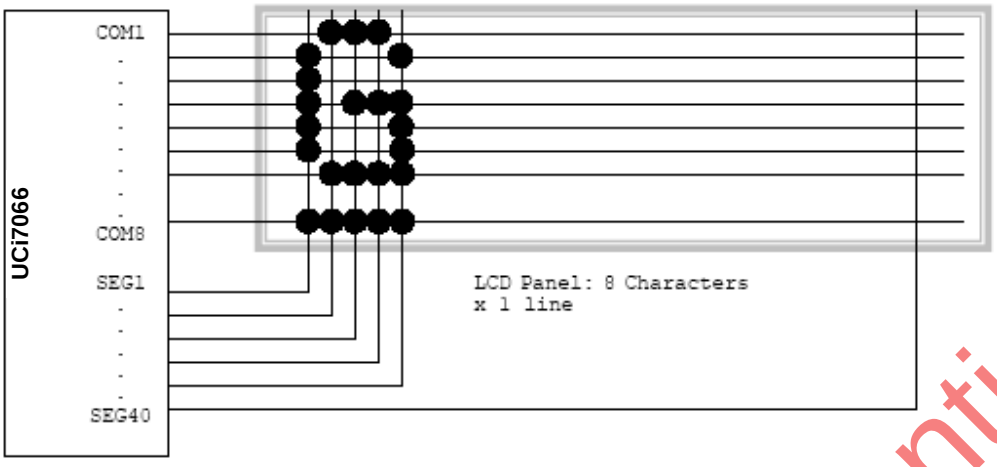
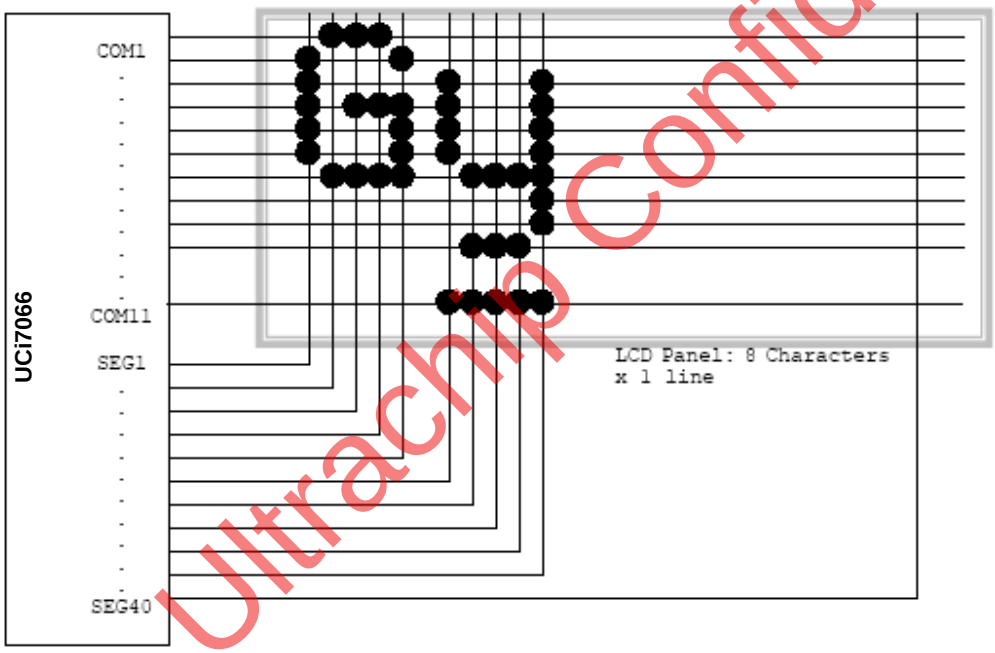
Connection with LCD

5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



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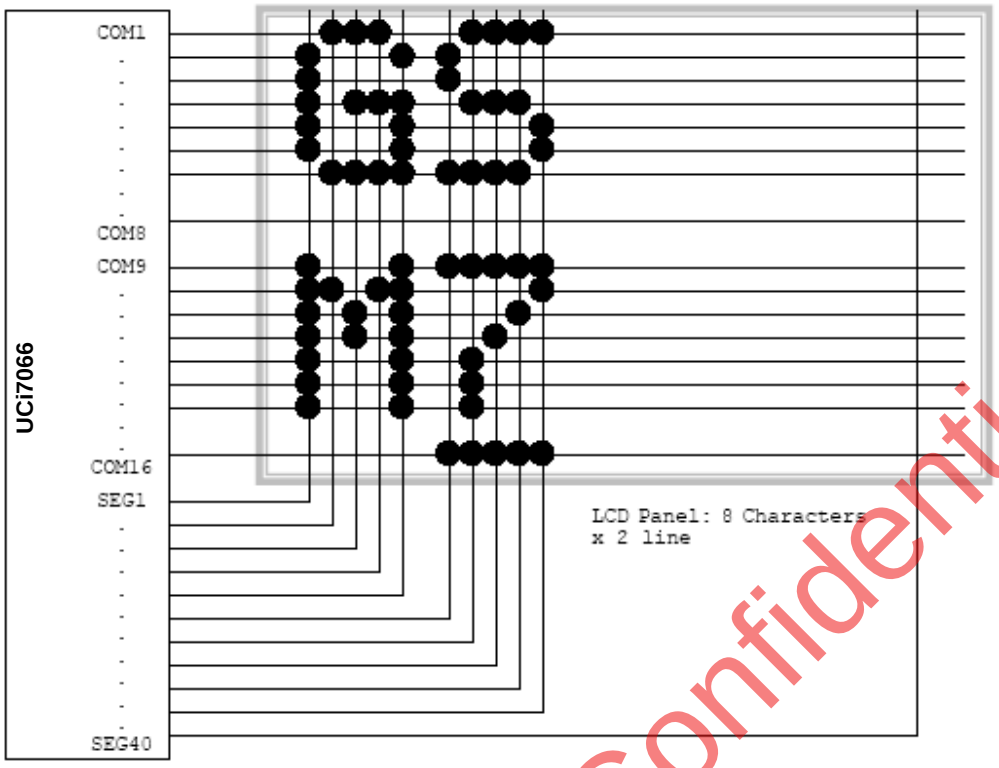
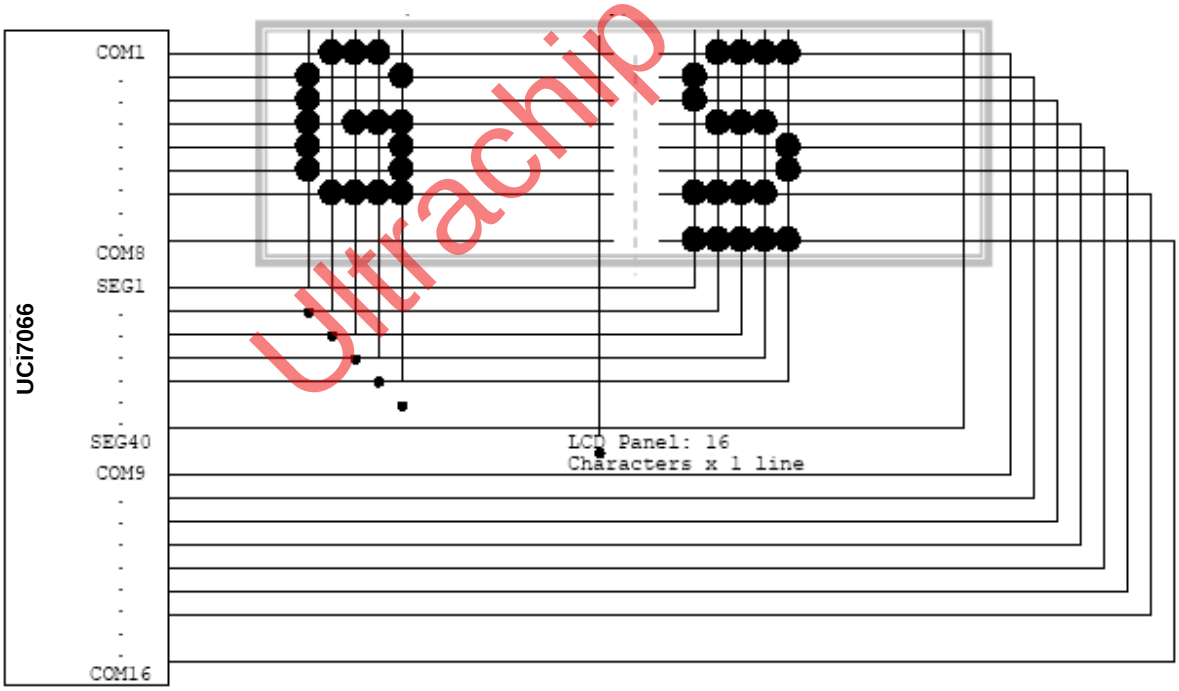
5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



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ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Range	Unit
V_{CC}	Power Supply Voltage	–0.3 ~ +7.0	V
V_{LCD}	LCD Driver Voltage	Vcc-15.0 ~ Vcc+0.3	V
V_{IN}	Input Voltage	–0.3 ~ Vcc+0.3	V
T_A	Operating Temperature	–40 ~ +90	^{o}C
T_{STD}	Storage Temperature	–55 ~ +125	^{o}C

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DC CHARACTERISTICS

Vcc=2.7V~4.5V, Vss=0V, Ta=25°C

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
Vcc	Operating Voltage	–	2.7	–	4.5	V
VLCD	LCD Voltage	Vcc-V5	3.0	–	18.0	V
VIH1	Input Voltage – High (Except OSC1)		0.7Vcc		Vcc	V
VIL1	Input Voltage – Low (Except OSC1)		–0.3	–	0.55	V
VIH2	Input Voltage – High (OSC1)		0.7Vcc	–	Vcc	V
VIL2	Input Voltage – Low (OSC1)		–	–	0.2Vcc	V
VOH1	Output Voltage – High (DB7~DB0)	IOH=–0.1mA	0.75Vcc	–	–	V
VOL1	Output Voltage – Low (DB7~DB0)	IOL=0.1mA	–	–	0.2Vcc	V
VOH2	Output Voltage – High (Except DB7~DB0)	IOH=–0.04mA	0.8Vcc	–	Vcc	V
VOH2	Output Voltage – Low (Except DB7~DB0)	IOL=0.04mA	–	–	0.2Vcc	V
RCOM	Resistance – COM	VLCD=4V, Id=0.05mA	–	2	20	kΩ
RSEG	Resistance – SEG	VLCD=4V, Id=0.05mA	–	2	30	kΩ
ICC	Power Supply Current	fosc=270kHz, Vcc=3.0V	–	0.1	0.25	mA
ILEAK	Input leadage Current	Vin=0V to Vcc	–1	–	1	uA
IPUP	Pull-up MOS Current	Vcc=3V	–10	–50	–120	uA

Vcc=4.5V~5.5V, Vss=0V, Ta=25°C

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
Vcc	Operating Voltage	–	4.5	–	5.5	V
VLCD	LCD Voltage	Vcc-V5	3.0	–	18.0	V
VIH1	Input Voltage – High (Except OSC1)		0.7Vcc		Vcc	V
VIL1	Input Voltage – Low (Except OSC1)		–0.3	–	0.6	V
VIH2	Input Voltage – High (OSC1)		Vcc–1	–	Vcc	V
VIL2	Input Voltage – Low (OSC1)		–0.2	–	1.0	V
VOH1	Output Voltage – High (DB7~DB0)	IOH=–0.025mA	2.4	–	Vcc	V
VOL1	Output Voltage – Low (DB7~DB0)	IOL=1.2mA	–	–	0.4	V
VOH2	Output Voltage – High (Except DB7~DB0)	IOH=–0.04mA	0.9Vcc	–	Vcc	V
VOH2	Output Voltage – Low (Except DB7~DB0)	IOL=0.04mA	–	–	0.1Vcc	V
RCOM	Resistance – COM	VLCD=4V, Id=0.05mA	–	2	20	kΩ
RSEG	Resistance – SEG	VLCD=4V, Id=0.05mA	–	2	30	kΩ
ICC	Power Supply Current	fosc=270kHz, Vcc=5.0V	–	0.35	0.6	mA
ILEAK	Input leadage Current	Vin=0V to Vcc	–1	–	1	uA
IPUP	Pull-up MOS Current	Vcc=5V	–50	–125	–250	uA

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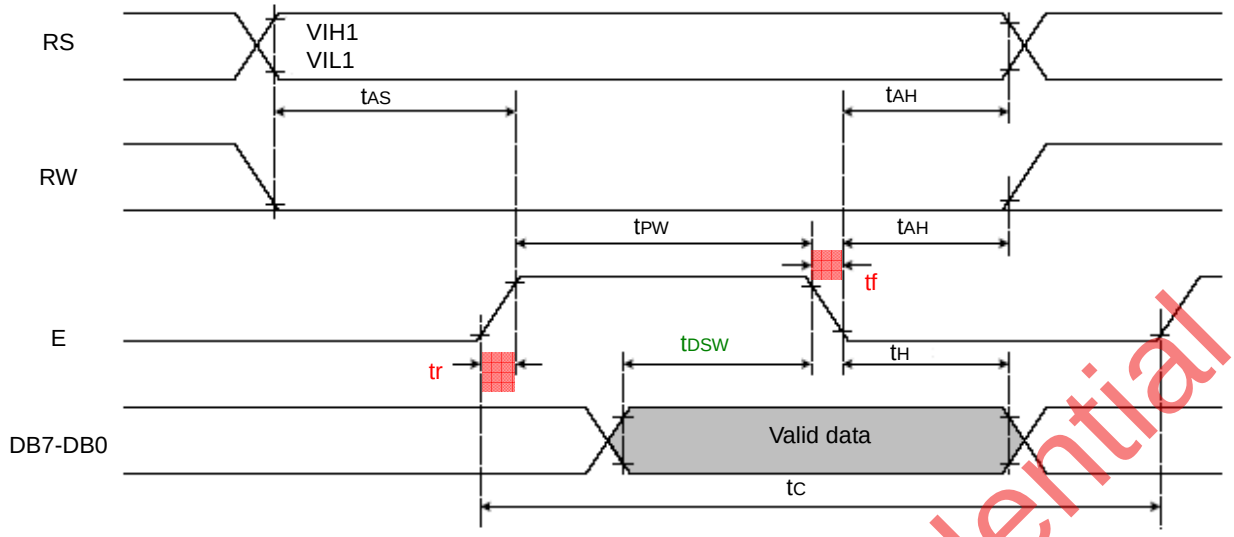
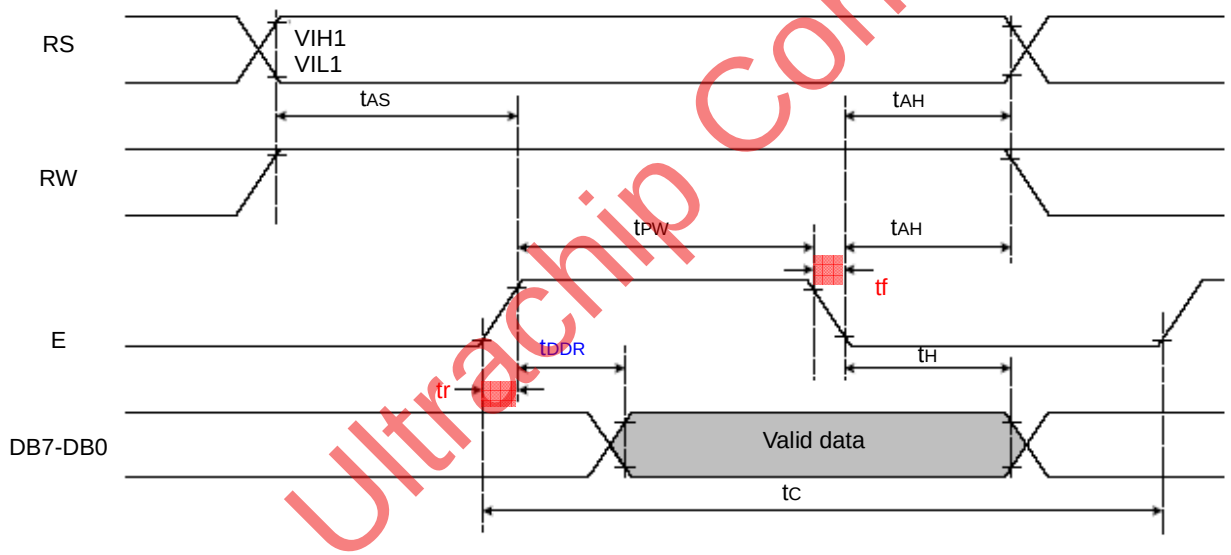
AC CHARACTERISTICS



(6800 Write data to UCi7066c)



(6800 Read data from UCi7066c)

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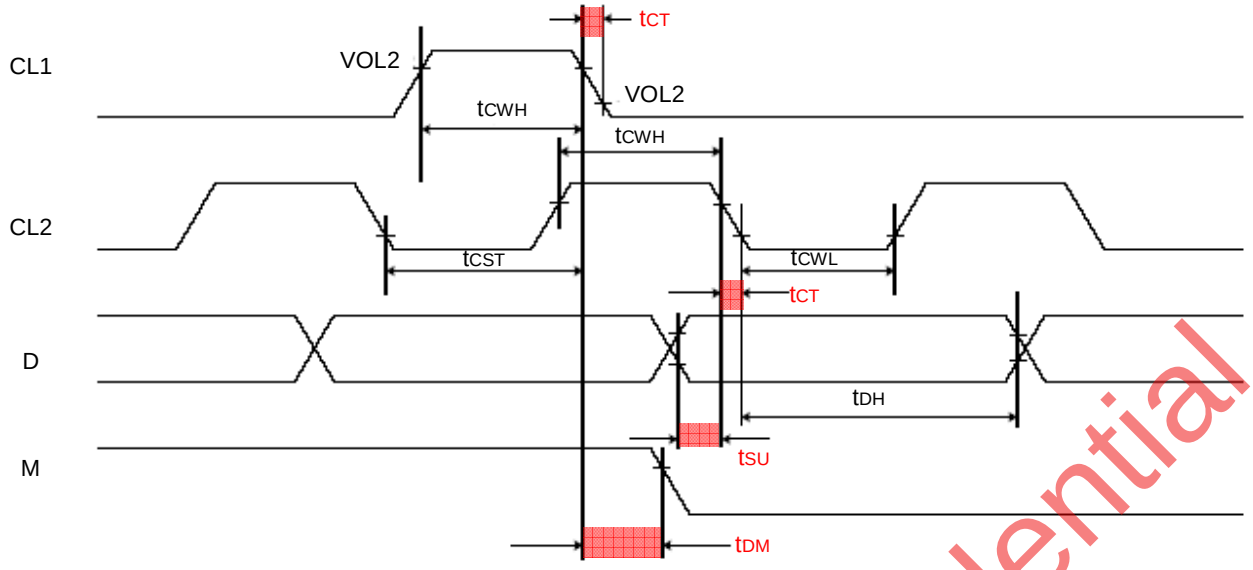
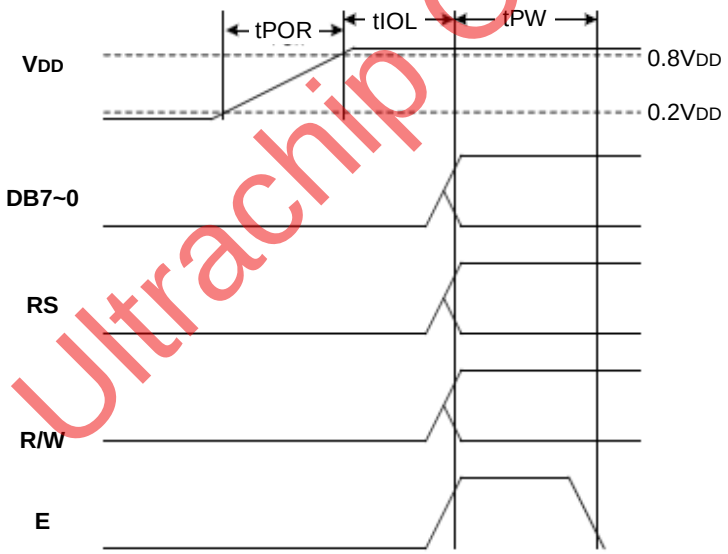


(with External Driver)

Power Supply Conditions



Symbol	Characteristics	Description	Min	Typ.	Max.	Unit
tPOR	Power Rise time	Power rise time that will trigger internal POR circuit	0.1		100	mS
tIOL	I/O Low time	The period that I/O is kept LOW	40			mS
tPW	Enable Pulse width	Please refer to the following tables				

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T_A = 25°C, Vcc=2.7V~4.5V

Symbol	Characteristic	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
fosc	OSC Frequency	R=750KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	--	125	270	410	KHz
	Duty Cycle	--	45	50	55	%
t_R, t_F	Rising/Falling Time	--	–	–	0.2	uS
Write Mode (MPU writes data to UCi7066)						
tc	Enable Cycle Time	Pin E	1200	–	–	nS
tpw	Enable Pulse Width	Pin E	460	–	–	nS
t_R, t_F	Rising/Falling Time	Pin E	–	–	25	nS
t_{AS}	Address Setup Time	Pin: RS, RW, E	0	–	–	nS
t_{AH}	Address Hold Time	Pin: RS, RW, E	10	–	–	nS
t_{DSW}	Data Setup Time	Pin: DB7~DB0	80	–	–	nS
t_H	Data Hold Time	Pin: DB7~DB0	10	–	–	nS
Read Mode (MPU reads data from UCi7066)						
tc	Enable Cycle Time	Pin E	1200	–	–	nS
tpw	Enable Pulse Width	Pin E	480	–	–	nS
t_R, t_F	Rising/Falling Time	Pin E	–	–	25	nS
t_{AS}	Address Setup Time	Pin: RS, RW, E	0	–	–	nS
t_{AH}	Address Hold Time	Pin: RS, RW, E	10	–	–	nS
t_{DDR}	Data Setup Time	Pin: DB7~DB0	–	–	320	nS
t_H	Data Hold Time	Pin: DB7~DB0	10	–	–	nS
Interface Mode with LCD Driver (UCi7065)						
t_{CWH}	Clock Pulse Width – High	Pin: CL1, CL2	800	–	–	nS
t_{CWL}	Clock Pulse Width – Low	Pin: CL1, CL2	800	–	–	nS
t_{CST}	Clock Setup Time	Pin: CL1, CL2	500	–	–	nS
t_{SU}	Data Setup Time	Pin: D	300	–	–	nS
t_{DH}	Data Hold Time	Pin: D	300	–	–	nS
t_{DM}	M Delay Time	Pin: M	0	–	2000	nS

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T_A = 25°C, Vcc=4.5V~5V

Symbol	Characteristic	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
fosc	OSC Frequency	R=91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	--	125	270	410	KHz
	Duty Cycle	--	45	50	55	%
t_R, t_F	Rising/Falling Time	--	--	--	0.2	uS
Write Mode (MPU writes data to UCi7066)						
tc	Enable Cycle Time	Pin E	1200	--	--	nS
tpw	Enable Pulse Width	Pin E	140	--	--	nS
t_R, t_F	Rising/Falling Time	Pin E	--	--	25	nS
t_{AS}	Address Setup Time	Pin: RS, RW, E	0	--	--	nS
t_{AH}	Address Hold Time	Pin: RS, RW, E	10	--	--	nS
t_{DSW}	Data Setup Time	Pin: DB7~DB0	40	--	--	nS
t_H	Data Hold Time	Pin: DB7~DB0	10	--	--	nS
Read Mode (MPU reads data from UCi7066)						
tc	Enable Cycle Time	Pin E	1200	--	--	nS
tpw	Enable Pulse Width	Pin E	140	--	--	nS
t_R, t_F	Rising/Falling Time	Pin E	--	--	25	nS
t_{AS}	Address Setup Time	Pin: RS, RW, E	0	--	--	nS
t_{AH}	Address Hold Time	Pin: RS, RW, E	10	--	--	nS
t_{DDR}	Data Setup Time	Pin: DB7~DB0	--	--	100	nS
t_H	Data Hold Time	Pin: DB7~DB0	10	--	--	nS
Interface Mode with LCD Driver (UCi7065)						
t_{CWH}	Clock Pulse Width, High	Pin: CL1, CL2	800	--	--	nS
t_{CWL}	Clock Pulse Width, Low	Pin: CL1, CL2	800	--	--	nS
t_{CST}	Clock Setup Time	Pin: CL1, CL2	500	--	--	nS
t_{SU}	Data Setup Time	Pin: D	300	--	--	nS
t_{DH}	Data Hold Time	Pin: D	300	--	--	nS
t_{DM}	M Delay Time	Pin: M	0	--	2000	nS

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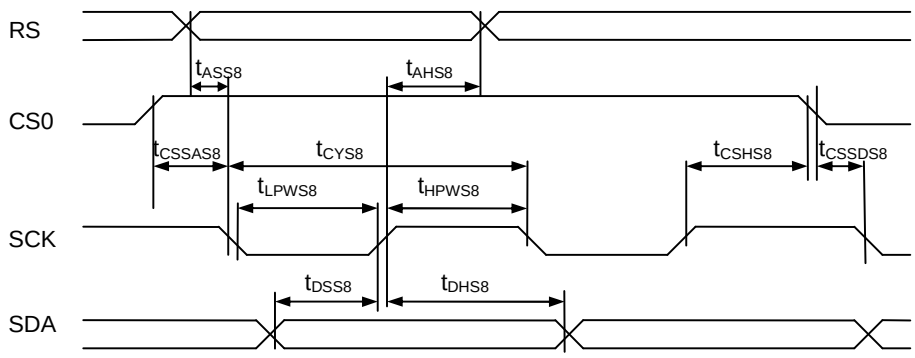

Serial Bus Timing Characteristics (for S8)

T_A = 25°C, Vcc=2.7V~4.5V

Symbol	Signal	Description	Min.	Typ.	Max.	Unit
t_{ASS8}	RS	Address setup time	0		–	nS
t_{AHS8}		Address hold time	20		–	nS
t_{CYS8}	SCK	System cycle time	140		–	nS
t_{LPWS8}		Low pulse width	65		–	nS
t_{HPWS8}		High pulse width	65		–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time	30 20		–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1, CS0	Chip select setup time	10 20 10			nS

T_A = 25°C, Vcc=4.5V~5V

Symbol	Signal	Description	Min.	Typ.	Max.	Unit
t_{ASS8}	RS	Address setup time	0		–	nS
t_{AHS8}		Address hold time	20		–	nS
t_{CYS8}	SCK	System cycle time	140		–	nS
t_{LPWS8}		Low pulse width	65		–	nS
t_{HPWS8}		High pulse width	65		–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time	30 20		–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1, CS0	Chip select setup time	10 20 10			nS

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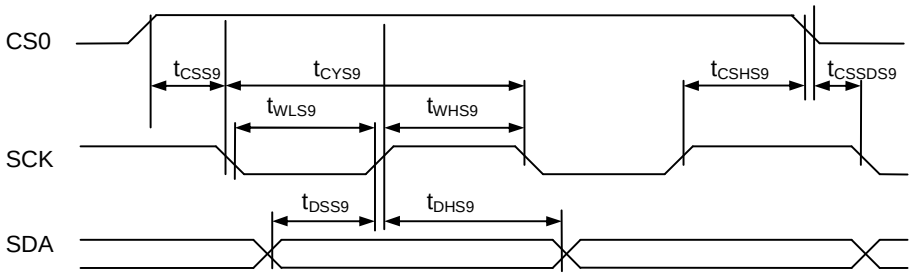

Serial Bus Timing Characteristics (for S9)

T_A = 25°C, Vcc=2.7V~4.5V

Symbol	Signal	Description	Min.	Typ.	Max.	Unit
t_{ASS8}	RS	Address setup time	0		–	nS
t_{AHS8}		Address hold time	20		–	nS
t_{CYS8}	SCK	System cycle time	140		–	nS
t_{LPWS8}		Low pulse width	65		–	nS
t_{HPWS8}		High pulse width	65		–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time	30 20		–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1, CS0	Chip select setup time	10 20 10			nS

T_A = 25°C, Vcc=4..5V~5V

Symbol	Signal	Description	Min.	Typ.	Max.	Unit
t_{ASS8}	RS	Address setup time	0		–	nS
t_{AHS8}		Address hold time	20		–	nS
t_{CYS8}	SCK	System cycle time	140		–	nS
t_{LPWS8}		Low pulse width	65		–	nS
t_{HPWS8}		High pulse width	65		–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time	30 20		–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1, CS0	Chip select setup time	10 20 10			nS

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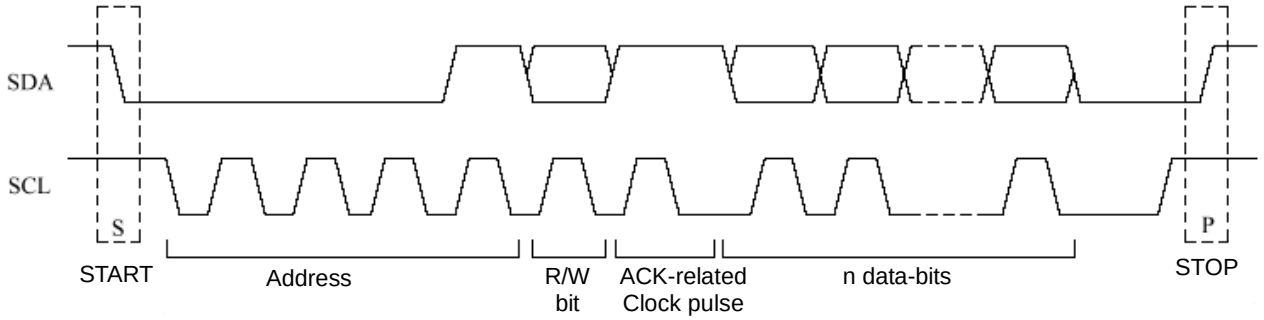

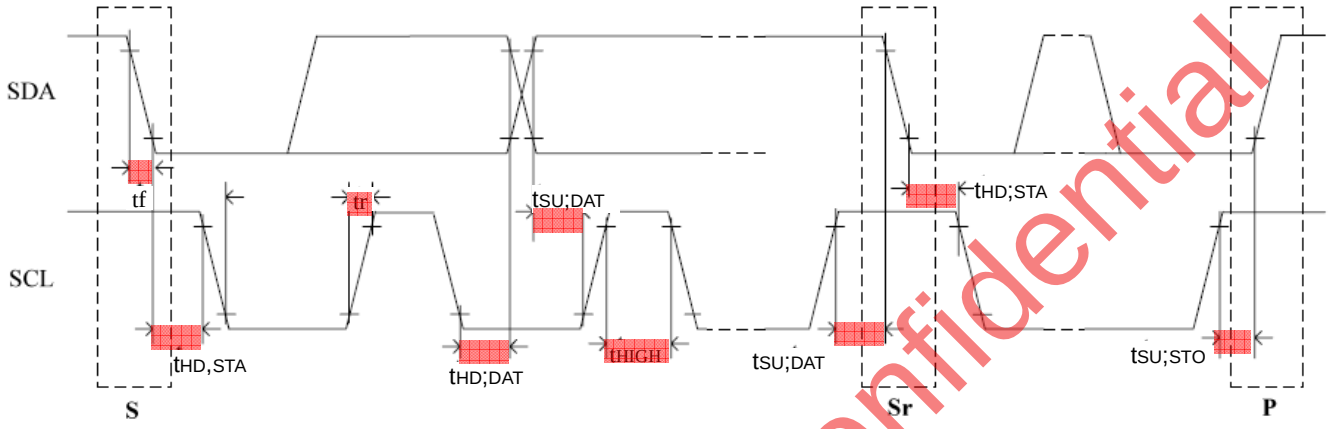

Serial Bus Timing Characteristics (for I²C MCU)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TA = 25°C, Vcc=2.7V~4.5V						
fSCL	SCL Clock Frequency		0	–	400	kHz
tSU, tSTA	Set-up time for START condition		600	–	–	nS
tHD, tSTA	Hold time for START condition		600	–	–	nS
tLOW	Low period of the SCL clock		1300	–	–	nS
tHIGH	High period of the SCL clock		600	–	–	nS
tSU, tDAT	Data setup time		100	–	–	nS
tHD, tDAT	Data hold time		–	–	900	nS
tr	Rise time of both SDA and SCL signals		T.B.D	–	300	nS
tf	Fall time of both SDA and SCL signals		T.B.D	–	300	nS
tSU, tSTO	Setup time for STOP condition		600	–	–	nS
TA = 25°C, Vcc=24.5V~5.5V						
fSCL	SCL Clock Frequency		0	–	400	kHz
tSU, tSTA	Set-up time for START condition		600	–	–	nS
tHD, tSTA	Hold time for START condition		600	–	–	nS
tLOW	Low period of the SCL clock		1300	–	–	nS
tHIGH	High period of the SCL clock		600	–	–	nS
tSU, tDAT	Data setup time		100	–	–	nS
tHD, tDAT	Data hold time		–	–	900	nS
tr	Rise time of both SDA and SCL signals		T.B.D	–	300	nS
tf	Fall time of both SDA and SCL signals		T.B.D	–	300	nS
tSU, tSTO	Setup time for STOP condition		600	–	–	nS

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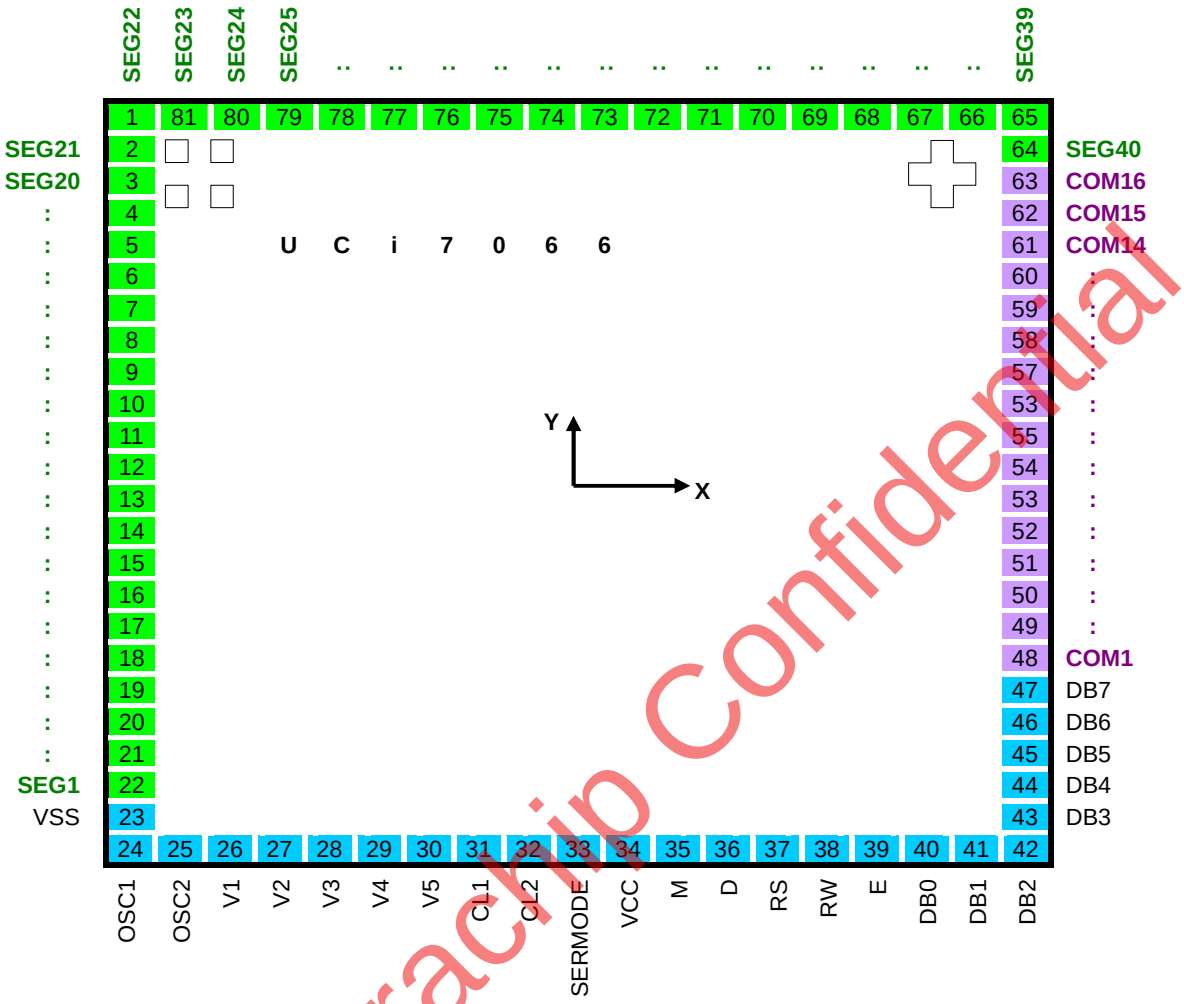
PHYSICAL DIMENSIONS



Note: Connect the substrate to VDD.

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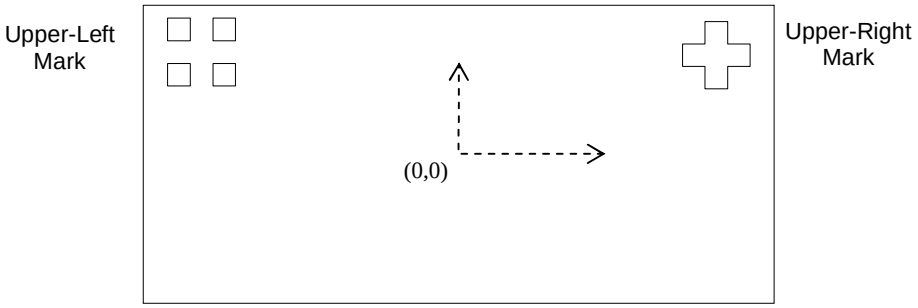
Die / Bump Information:

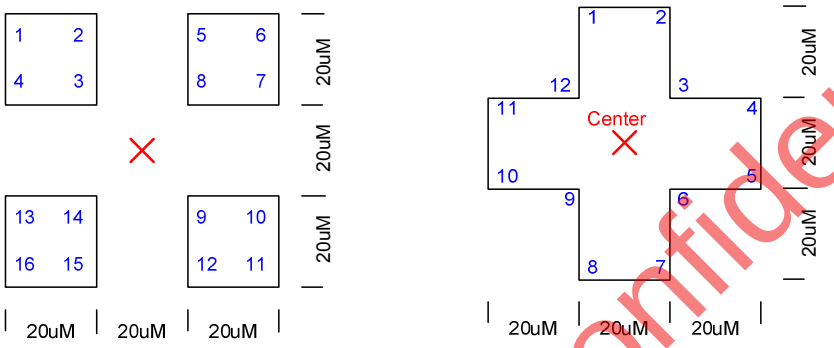
Die Size:	(2180μM ± 20uM) x (2410μM ± 20μM)
Die Thickness:	400μM ± 20μM
Die TTV:	DMAX – DMIN ≤ 2μM
Pad Size:	80μM x 80μM
Bump Pitch:	120μM
Coordinate origin:	Chip center
Pad reference:	Pad center

ALIGNMENT MARK INFORMATION

LOCATION :



SHAPE :



COORDINATES :

Point	Upper-Left Mark		Down-Left Mark	
	X	Y	X	Y
Center (X)	-903.335	1022.2	903.835	1022.2
1	-933.335	1052.2	893.385	1052.2
2	-913.335	1052.2	913.835	1052.2
3	-913.335	1032.2	913.835	1032.2
4	-933.335	1032.2	933.835	1032.2
5	-893.335	1052.2	933.835	1012.2
6	-873.335	1052.2	913.938	1012.2
7	-873.335	1032.2	913.835	992.2
8	-893.335	1032.2	893.835	992.2
9	-893.335	1012.2	893.835	1012.2
10	-873.335	1012.2	873.835	1012.2
11	-873.335	992.2	873.835	1032.2
12	-893.335	992.2	893.835	1032.2
13	-933.335	1012.2	–	–
14	-913.335	1012.2	–	–
15	-913.335	992.2	–	–
16	-933.335	992.2	–	–

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PAD COORDINATES

No.	Pad	X	Y	W	H
1	SEG22	-1020	1140	90	80
2	SEG21	-1025	1029	80	80
3	SEG20	-1025	931	80	80
4	SEG19	-1025	833	80	80
5	SEG18	-1025	735	80	80
6	SEG17	-1025	637	80	80
7	SEG16	-1025	539	80	80
8	SEG15	-1025	441	80	80
9	SEG14	-1025	343	80	80
10	SEG13	-1025	245	80	80
11	SEG12	-1025	147	80	80
12	SEG11	-1025	49	80	80
13	SEG10	-1025	-49	80	80
14	SEG9	-1025	-147	80	80
15	SEG8	-1025	-245	80	80
16	SEG7	-1025	-343	80	80
17	SEG6	-1025	-441	80	80
18	SEG5	-1025	-539	80	80
19	SEG4	-1025	-637	80	80
20	SEG3	-1025	-735	80	80
21	SEG2	-1025	-833	80	80
22	SEG1	-1025	-931	80	80
23	VSS	-1025	-1029	80	80
24	OSC1	-1020	-1140	90	80
25	OSC2	-900	-1140	90	80
26	V1	-780	-1140	90	80
27	V2	-660	-1140	90	80
28	V3	-540	-1140	90	80
29	V4	-420	-1140	90	80
30	V5	-300	-1140	90	80
31	CL1	-180	-1140	90	80
32	CL2	-60	-1140	90	80
33	SERMODE	53	-1140	80	80
34	VCC	159	-1140	80	80
35	M	265	-1140	80	80
36	D	371	-1140	80	80
37	RS	477	-1140	80	80
38	RW	583	-1140	80	80
39	E	689	-1140	80	80
40	DB0	795	-1140	80	80
41	DB1	901	-1140	80	80
42	DB2	1020	-1140	90	80

No.	Pad	X	Y	W	H
43	DB3	1025	-1029	80	80
44	DB4	1025	-931	80	80
45	DB5	1025	-833	80	80
46	DB6	1025	-735	80	80
47	DB7	1025	-637	80	80
48	COM1	1025	-539	80	80
49	COM2	1025	-441	80	80
50	COM3	1025	-343	80	80
51	COM4	1025	-245	80	80
52	COM5	1025	-147	80	80
53	COM6	1025	-49	80	80
54	COM7	1025	49	80	80
55	COM8	1025	147	80	80
56	COM9	1025	245	80	80
57	COM10	1025	343	80	80
58	COM11	1025	441	80	80
59	COM12	1025	539	80	80
60	COM13	1025	637	80	80
61	COM14	1025	735	80	80
62	COM15	1025	833	80	80
63	COM16	1025	931	80	80
64	SEG40	1025	1029	80	80
65	SEG39	1020	1140	90	80
66	SEG38	900	1140	90	80
67	SEG37	780	1140	90	80
68	SEG36	660	1140	90	80
69	SEG35	540	1140	90	80
70	SEG34	420	1140	90	80
71	SEG33	300	1140	90	80
72	SEG32	180	1140	90	80
73	SEG31	60	1140	90	80
74	SEG30	-60	1140	90	80
75	SEG29	-180	1140	90	80
76	SEG28	-300	1140	90	80
77	SEG27	-420	1140	90	80
78	SEG26	-540	1140	90	80
79	SEG25	-660	1140	90	80
80	SEG24	-780	1140	90	80
81	SEG23	-900	1140	90	80

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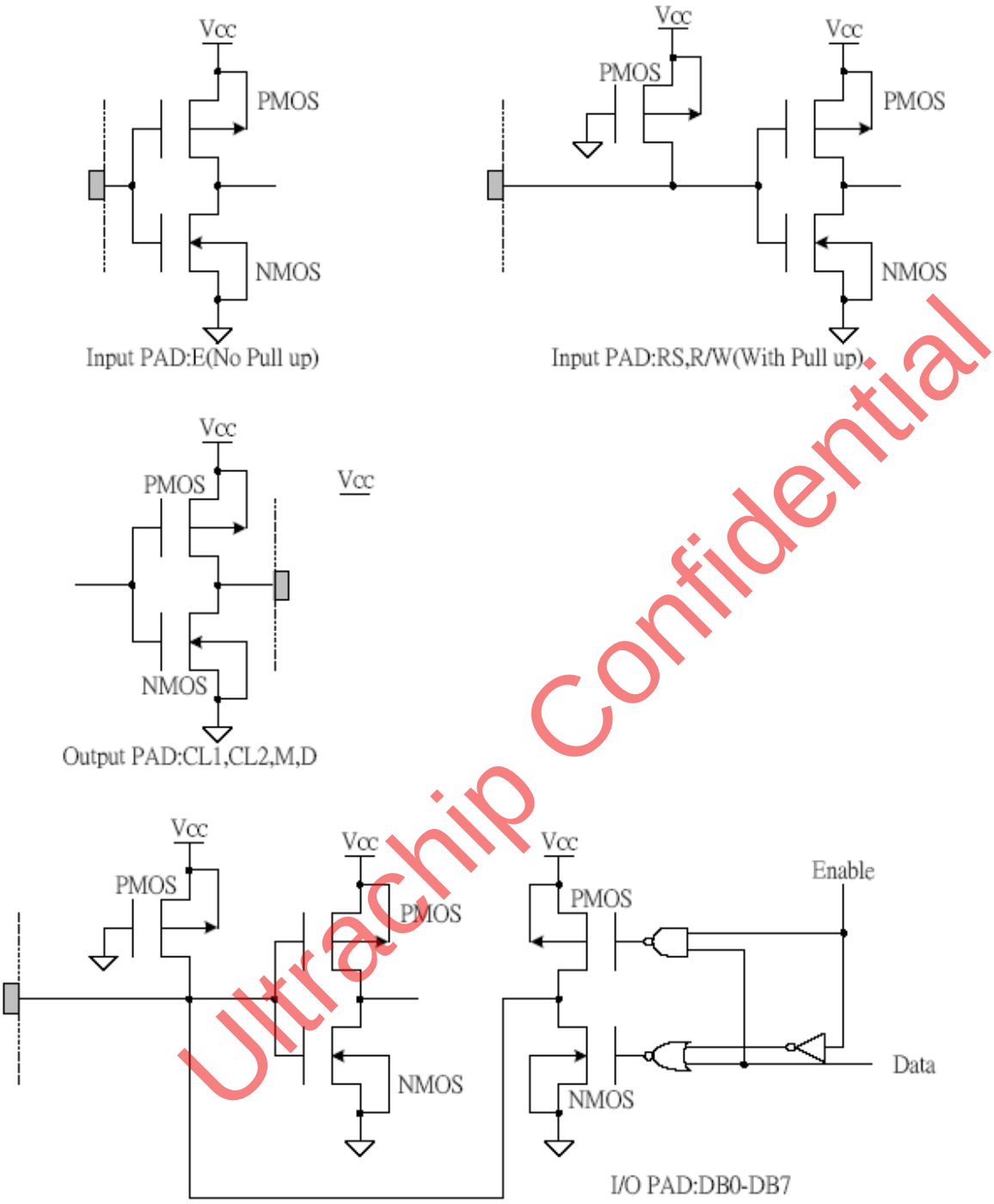
I/O Pad Configuration



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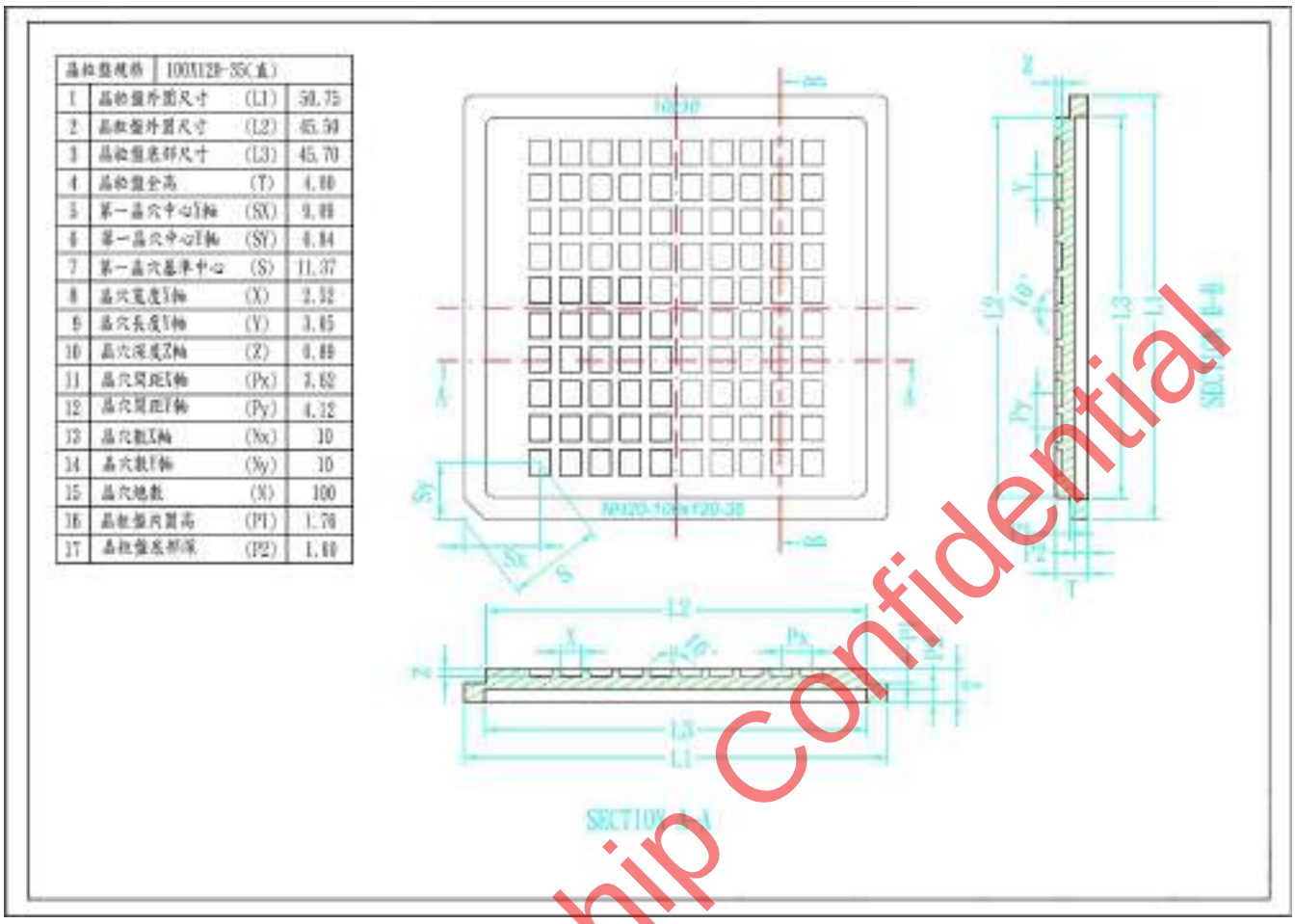
TRAY INFORMATION



晶粒盤規格	100X120-35(直)		
1	晶粒盤外圍尺寸	(L1)	50.75
2	晶粒盤外圍尺寸	(L2)	45.50
3	晶粒盤底部尺寸	(L3)	45.70
4	晶粒盤全高	(T)	4.00
5	第一晶穴中心X軸	(SX)	9.88
6	第一晶穴中心Y軸	(SY)	6.84
7	第一晶穴基準中心	(S)	11.37
8	晶穴寬度X軸	(X)	2.52
9	晶穴長度Y軸	(Y)	3.65
10	晶穴深度Z軸	(Z)	0.89
11	晶穴間距X軸	(Px)	3.62
12	晶穴間距Y軸	(Py)	4.22
13	晶穴數X軸	(Nx)	10
14	晶穴數Y軸	(Ny)	10
15	晶穴總數	(N)	100
16	晶粒盤內圍高	(P1)	1.70
17	晶粒盤底部深	(P2)	1.00

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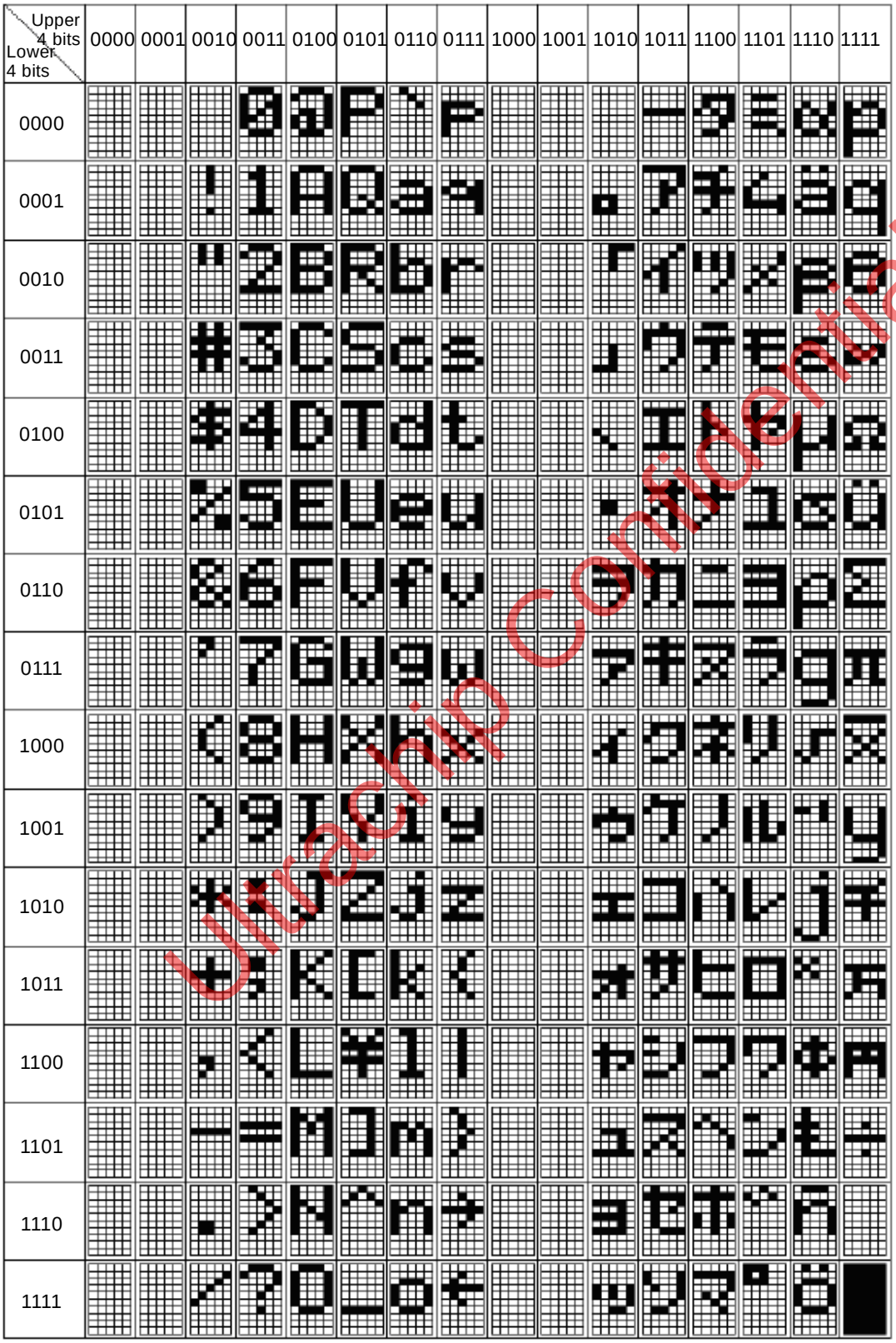
APPENDIX

Correspondence between Character Codes and Character Patterns (ROM Code: 0A) **No. 7066-01**



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No. 7066-02

Upper 4 bits / Lower 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

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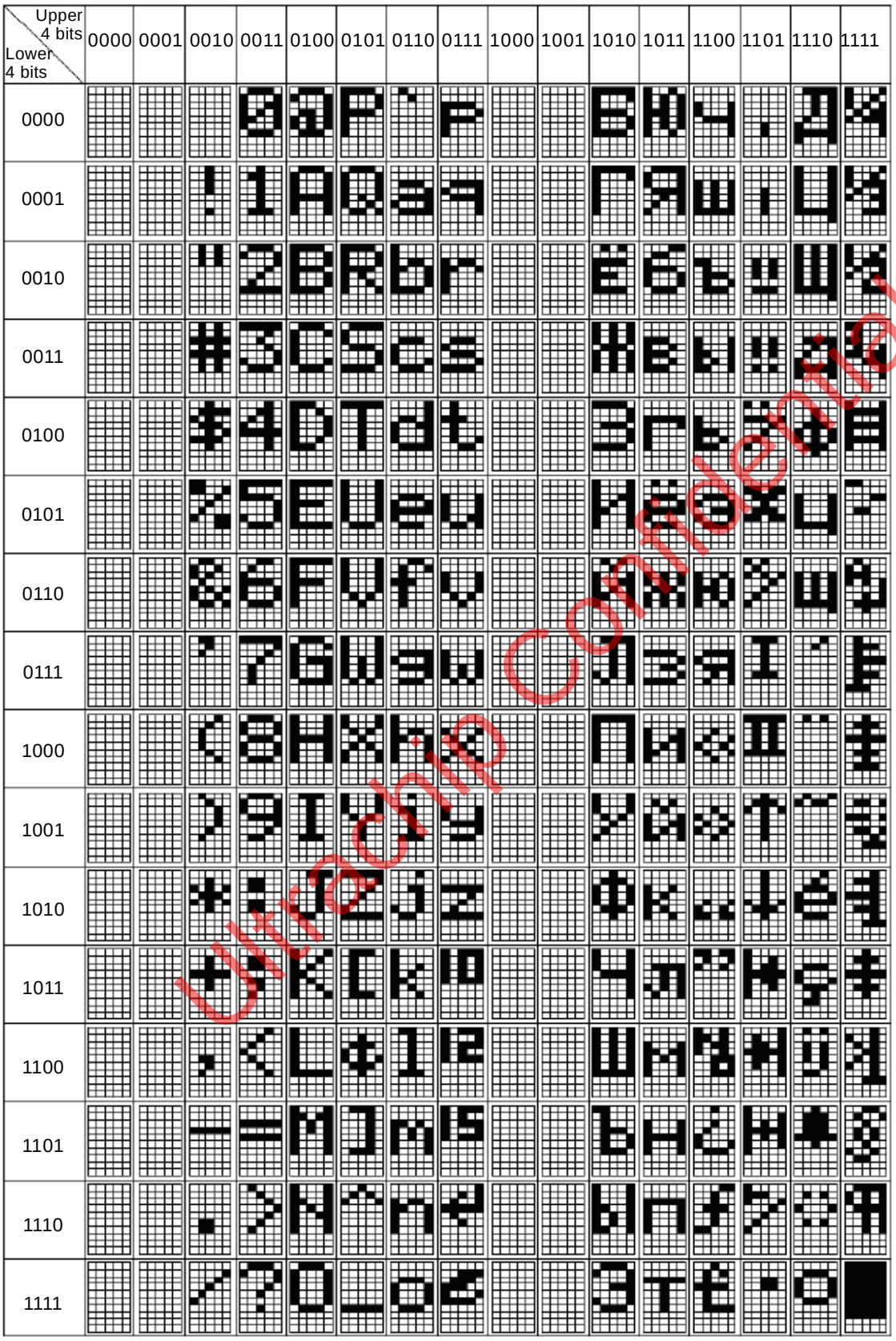
No. 7066-03



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No. 7066-05

Upper 4 bits / Lower 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

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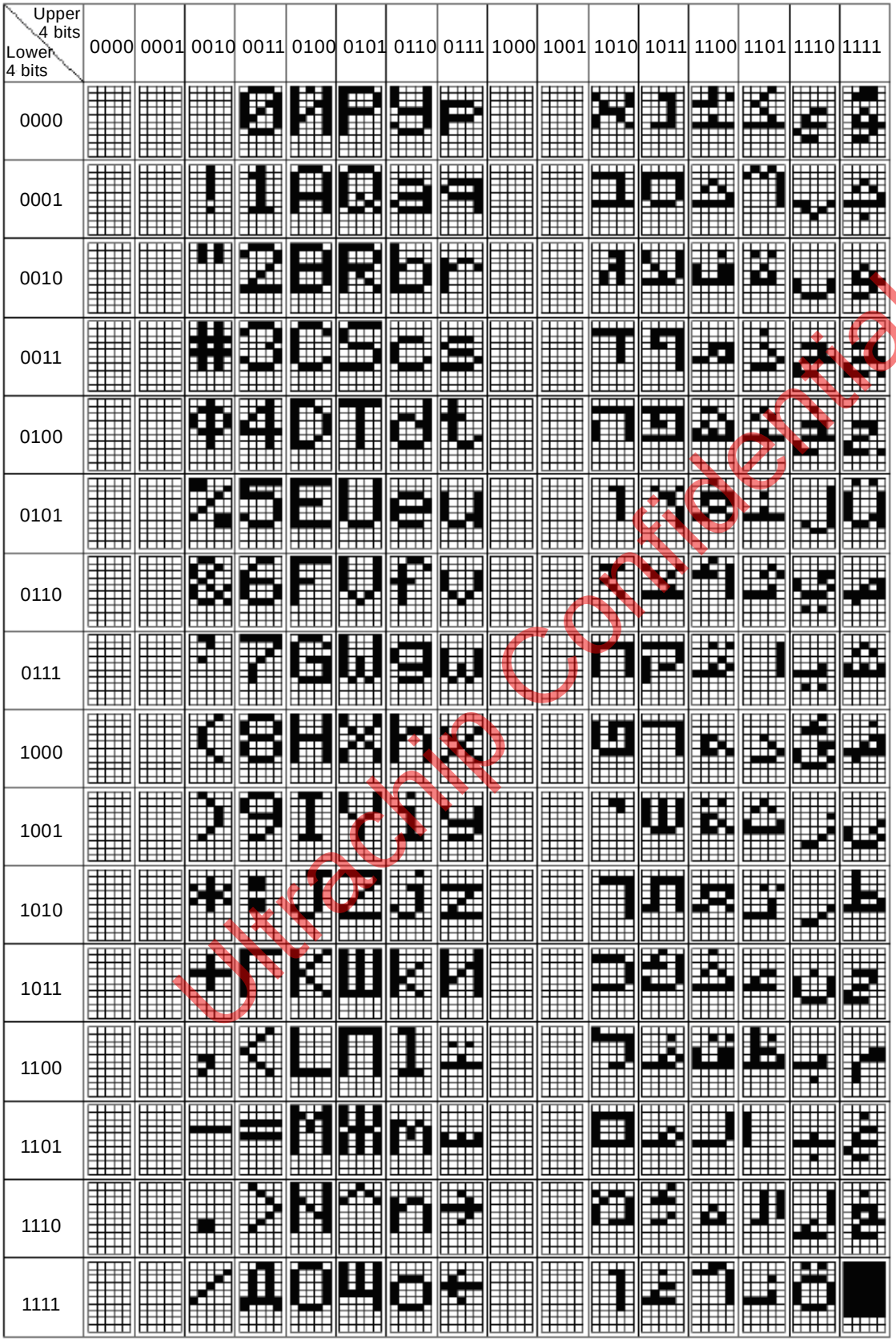
No. 7066-06



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REVISION HISTORY

Revision	Contents	Date
1.0	(First Release)	Feb. 4, 2016

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