UC1701x

65x132 STN Controller-Driver

MP Specifications
Revision 1.0

November 7, 2008

ULTRACHIP

The Coolest LCD Driver, Ever!

Table of Content

UC1701x

Single-Chip, Ultra-Low Power
65COM by 132SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1701x is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver support 65x132 graphics STN LCD panels.

- Support both row ordered and column ordered display buffer RAM access.

- Support industry standard 8-bit parallel bus (8080 or 6800 mode) and 4-wire serial bus (S8) interface.

- Ultra-low power consumption under all display patterns.

- Fully programmable Mux Rate and Bias Ratio allow many flexible power management options.

- 7-x internal charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.

- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.

- Very low pin count (10-pin) allows exceptional image quality in COG format on conventional ITO glass.

- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.

- V_{DD} range (Typ.):   1.8V ~ 3.3V
  $V_{DD2/3}$ range(Typ.): 2.5V ~ 3.3V
  LCD V_{OP} range: 3.9V ~ 11.5V

- Available in gold bump dies

- COM/SEG bump information
  Bump pitch: 27 µM
  Bump gap: 12 µM
  Bump surface: 2077.5 µM^2

ORDERING INFORMATION

Part Number	I²C	Description
UC1701xGAA	No	Gold Bumped Die

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

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All die are tested and are guaranteed to comply with all data sheet limits up to the point of. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

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BLOCK DIAGRAM

POWER ON & RESET CONTROL	
CLOCK & TIMING GENERATOR	
CONTROL & STATUS REGISTER	

COLUMN ADDRESS GENERATOR

PAGE ADDRESS GENERATOR

DATA RAM I/O BUFFER

DISPLAY DATA RAM

ROW ADDRESS GENERATOR

LEVEL SHIFTER

COM DRIVERS

DISPLAY DATA LATCHES

COMMAND

LEVEL SHIFTERS

HOST INTERFACE

SEG DRIVERS

V_{LCD} & BIAS GENERATOR

C_L

C_{B0} C_{B1}
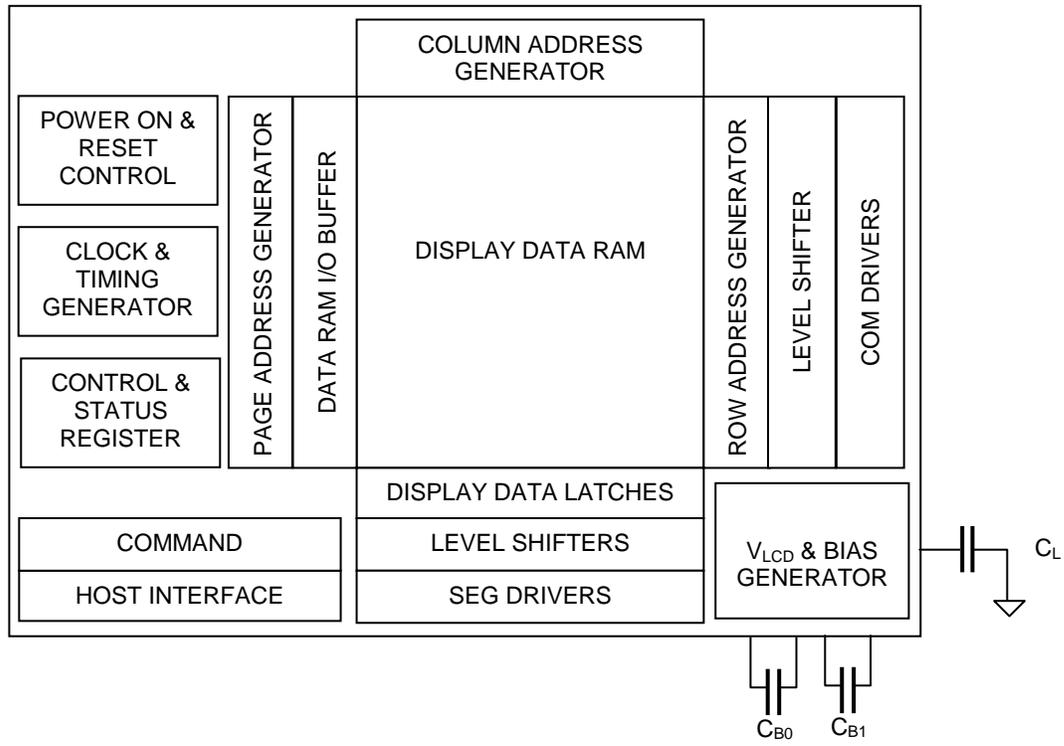
PIN DESCRIPTION

| Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD} V_{DD2} V_{DD3}	PWR	3 4 2	V_{DD} supplies for Display Data RAM and digital logic, V_{DD2} supplies for V_{LCD} and V_D generator, V_{DD3} supplies for V_{BIAS} and other analog circuits. V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	2 4	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.
			LCD POWER SUPPLY & VOLTAGE CONTROL
V_{B0+} V_{B0-} V_{B1+} V_{B1-}	PWR	2 2 4 2	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. In COG application, the resistance of these ITO traces directly affects the SEG driving strength of the resulting LCD module. Minimize these trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	2 2	Main LCD Power Supply. When V_{LCD} is used, connect these pins together. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the ITO trace resistance around 70~100 Ω.

NOTE

- Recommended capacitor values:
  C_B: 2.2μF/5V or 100~250x(LCD load capacitance).
  C_L: 330nF/25V is appropriate for most applications.

Name	Type	Pins	Description
HOST INTERFACE			
BM0 BM1	I	1 1	Bus mode: The interface bus mode is determined by BM[1:0] and {D7, D6} by the following relationship: 	BM[1:0]	{D7, D6}	Mode
---	---	---
11	Data	6800/8-bit
10	Data	8080/8-bit
0x	SDA, SCK	4-wire SPI w/ 8-bit token (S8: conventional)	
CS0	I	1	Chip Select. Chip is selected when CS0 = "L". When the chip is not selected, D[7:0] will be of high impedance.
RST	I	1	When RST="L", all control registers are re-initialized by their default states. Since UC1701x has built-in Power-On Reset and Software Reset command, RST pin is not required for proper chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.
CD	I	1	Select Control data or Display data for read/write operation. "L": Control data "H": Display data
WR0 WR1	I	1 1	WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details. In parallel mode, the meaning of WR[1:0] depends on which interface it is in, 6800 or 8080 mode. In serial interface modes, these two pins are not used, Connect them to V_{SS} or V_{DD}.
DT1 DT2	I	1 1	Duty selection. 	DT2	DT1	Duty
---	---	---
0	0	1/65
0	1	1/49
1	0	1/33
1	1	1/55	
D7~D0	I/O	8	Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[7] to SDA, D[6] to SCK. |	D7	D6	D5	D4	D3	D2	D1	D0
---	---	---	---	---	---	---	---	---
BM=1x (8-bit)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BM=0x (S8)	SDA	SCK	--	--	--	--	--	--	 Always connect unused pins to either V_{SS} or V_{DD}.
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG132	HV	132	SEG (column) driver outputs. Support up to 132 pixels. Leave unused SEG drivers open-circuit.
COM1 ~ COM64	HV	64	COM (row) driver outputs. Support up to 64 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 64, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 64] open-circuit.
CIC	HV	2	Icon driver outputs. Leave it open if not used.

Name	Type	Pins	Description
MISC. PINS			
V$_{DDX}$		4	Auxiliary V$_{DD}$. This pin is connected to the main V$_{DD}$ bus within the IC. It's provided to facilitate chip configurations in COG application. There's no need to connect V$_{DDX}$ to main V$_{DD}$ externally and it should _NOT_ be used to provide V$_{DD}$ power to the chip.
TST4	I	1	Test control. There's an on-chip pull-up resistor for TST4. Leave it open during normal use.
TST2	I/O	1	Test I/O pins. Leave these pins open during normal use.
Dummy		11	Dummy pins are NOT connected inside the IC.

Note: Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, COM_X_ or SEG_X_ will correspond to index _X_-1, and the value range for those index register will be 0~63 for COM and 0~131 for SEG.

RECOMMENDED COG LAYOUT

CS0
RST
CD
WR0
WR1
D0
D1
D2
D3
D4
D5
D6
D7

VDD

VSS

VB0+
VB0-
VB1-
VB1+
VLCDIN
VLCDOUT

BM0
BM1
DT1
DT2

UC1701x Bump View
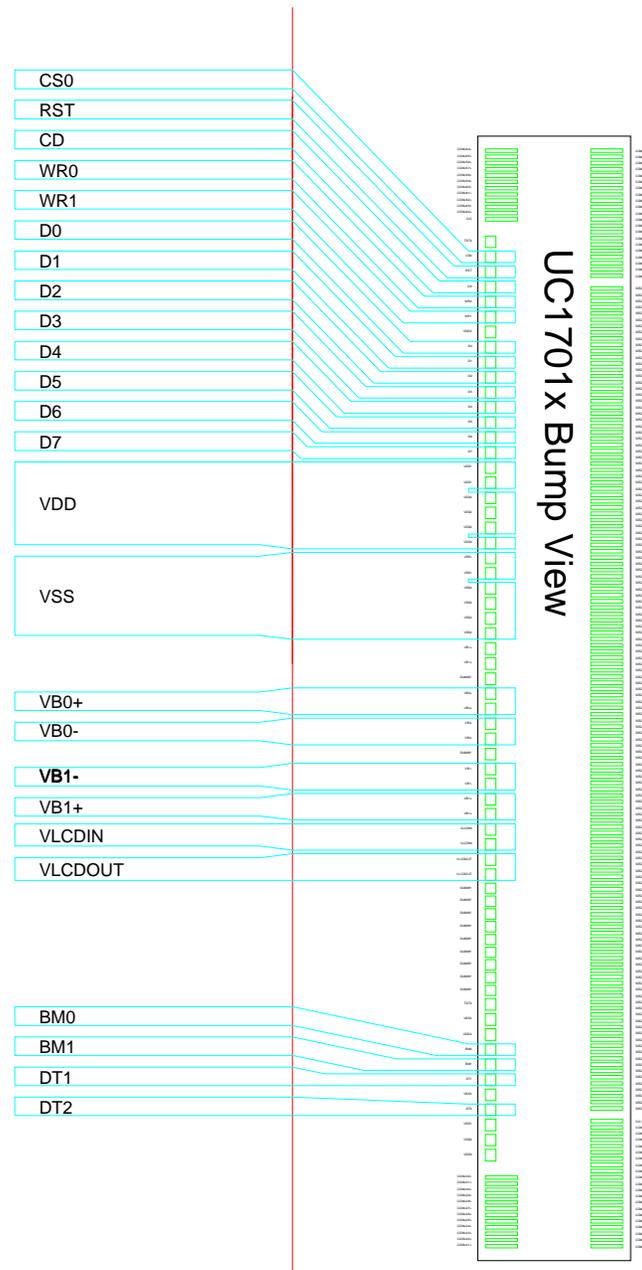
NOTES FOR V$_{DD}$ WITH COG:

The operation condition, V$_{DD}$=1.8V (typical), should be satisfied under all operating conditions. UC1701x's peak current (I$_{DD}$) can be up to ~15mA during high speed data-write to UC1701x's on-chip SRAM. Such high pulsing current mandates very careful design of V$_{DD}$ and V$_{SS}$ ITO trances in COG modules. When V$_{DD}$ and V$_{SS}$ trace resistance is not low enough, the pulsing I$_{DD}$ current can cause the actual on-chip V$_{DD}$ to drop to below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1701x contains registers, which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, Command Table and Command Description.

Name: The Symbolic reference of the register.
            Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	6	00H	Scroll Line. Scroll the displayed image up by *SL* rows. The valid SL value is between 0 (for no scrolling) and 63. Setting SL outside of this range causes undefined effects on the displayed image. This register does not affect icon output CIC.
CA	8	00H	Column Address of DDRAM (Display Data RAM). Value range is 0~131. (Used in Host to access DDRAM)
PA	4	0H	Page Address of DDRAM. Value range 0~8. (Used in Host to access DDRAM)
BR	1	0H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS} varies according to Duty selected: <table><tr><td></td><td>**BR=0**</td><td>**BR=1**</td></tr><tr><td>Duty=1/65</td><td>1/9</td><td>1/7</td></tr><tr><td>Duty=1/49</td><td>1/8</td><td>1/6</td></tr><tr><td>Duty=1/33</td><td>1/6</td><td>1/5</td></tr><tr><td>Duty=1/55</td><td>1/8</td><td>1/6</td></tr></table>
PM	6	20H	Adjust contrast of LCD panel display.
PC	6	20H	Power Control. PC [0] : Voltage Follower. (Default **0: OFF**) PC [1] : Voltage Regular. (Default **0: OFF**) PC [2] : Booster Ratio. (Default **0: OFF**) PC [5:3]: Resistor Ratio for V_{LCD}. (Default **100b**) 000b~111b : Rb/Ra ratio setting
CR	8	0H	Return Column Address. Useful for cursor implementation.
AC3	1	0H	Address Control. AC3: CUM: Cursor update mode, (Default **0: OFF**) When CUM=1, CA increment on write only, wrap around suspended
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse (bit-wise data inversion. Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) When DC[2] is set to 0, the IC will enter Sleep Mode
LC	2	0H	LCD Control: LC[0]: MX, Mirror X SEG/Column sequence inversion (Default: **OFF**) LC[1]: MY, Mirror Y COM/Row sequence inversion (Default: **OFF**)

Name	Bits	Default	Description
APC0 APC1	8 8	90H --	Advanced Program Control. For UltraChip only. Do *NOT* use.
			APC0 [7] : TC, V_{BIAS} temperature compensation coefficient (%-per-^{o}C) 0b : TC curve definition = -0.05% / ^{o}C **1b : TC curve definition = -0.11% / ^{o}C**
			APC0 [1:0] : WA, automatic column/row Wrap Around. WA[0] : **0: PA wrap around disable** 1: PA wrap around enable. WA[1] : **0: CA wrap around disable** 1: CA wrap around enable.
			APC1[7:0] : For UltraChip's use only.
Status Registers			
BZ, MX, DE, RST	1	0	BZ : Set to 1 when system is busy. Commands can only be accepted when BZ=0. MX : Mirror X-axle (i.e. SEG or column) DE : Set to 1 when display enabled. RST : Reset flag. RST=1 when reset is in progress.

COMMAND TABLE

The following is a list of host commands supported by UC1701x

C/D: 0: Control,   1: Data
W/R: 0: Write Cycle,   1: Read Cycle

Useful Data bits   –   Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	BZ	MX	DE	RST	0	0	0	0	Get Status	--
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB			0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	000b
6.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
7.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
8.	Set V$_{LCD}$ Resistor Ratio	0	0	0	0	1	0	0	#	#	#	Set PC[5:3]	100b
9.	Set Electronic Volume (double-byte command)	0	0	1	0	0	0	0	0	0	1		
				0	0	#	#	#	#	#	#	Set PM[5:0]	20H
10.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
11.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
12.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
13.	Set SEG Direction	0	0	1	0	1	0	0	0	0	#	Set LC[0]	0b
14.	Set COM Direction	0	0	1	1	0	0	#	-	-	-	Set LC[1]	0b
15.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
16.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
17.	Set LCD Bias Ratio	0	0	1	0	1	0	0	0	1	#	Set BR	0b
18.	Set Cursor Update Mode	0	0	1	1	1	0	0	0	0	0	AC3=1, CR=CA	N/A
19.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC3=0, CA=CR.	N/A
20.	Set Static Indicator OFF	0	0	1	0	1	0	1	1	0	0	NOP	N/A
21.	Set Static Indicator ON	0	0	1	0	1	0	1	1	0	1	NOP	N/A
	Set Static Indicator			-	-	-	-	-	-	-	-		
22.	Set Booster Ratio (double-byte command)	0	0	1	1	1	1	1	0	0	0	NOP	00b
				0	0	0	0	0	0	#	#		
23.	Set Power Save (compound command)	0	0	#	#	#	#	#	#	#	#	Display OFF & All Pixel ON	N/A
24.	Set Test Control (double-byte command)	0	0	1	1	1	1	1	1	TT		For UCI only Do NOT use	N/A
				-	#	#	#	#	#	#	#		
25.	Set Adv. Program Control 0 (double-byte command)	0	0	1	1	1	1	1	0	1	0		
				#	0	0	1	0	0	#	#	Set TC, WA[1:0]	90H
26.	Set Adv. Program Control 1 (double-byte command)	0	0	1	1	1	1	1	0	1	1	For UCI only Set APC1	
				#	#	#	#	#	#	#	#		N/A

* Other than commands listed above, all other bit patterns result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Write/Read Data Byte (Command 1,2) access Display Data RAM based on Page Address (PA) register and Column Address (CA) register. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	BZ	MX	DE	RST	0	0	0	0

BZ: BZ=1 when busy. The system accepts commands only when BZ=0.
MX: Mirror X. Status of register LC[0]
DE: Display Enable flag. DE=1 when display is enabled.
RST: RST flag. RST=1 when reset is in progress.

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB, CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB, CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: 0~131

5. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Power Control, PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

Set PC[2:0] to enable the built-in charge pump.

PC[2] : 0 – Boost OFF   1 – Boost ON
PC[1] : 0 – Voltage Regular OFF   1 – Voltage Regular ON
PC[0] : 0 – Voltage Follower OFF   1 – Voltage Follower ON

6. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line, SL[5:0]	0	0	**0**	**1**	SL5	SL4	SL3	SL2	SL1	SL0

Set the scroll line number. Range : 0~63

Scroll line setting will scroll the displayed image up by *SL* rows. Icon output CIC will not be affected by `Set Scroll Line` command.

Image row 0	row 0
:	:
Image row N-1	:
Image row N	
:	
Image row 63	row 63

SL=0

Image row N	row 0
:	:
:	:
Image row 63	
Image row 0	
:	
Image row N-1	row 63

SL=N
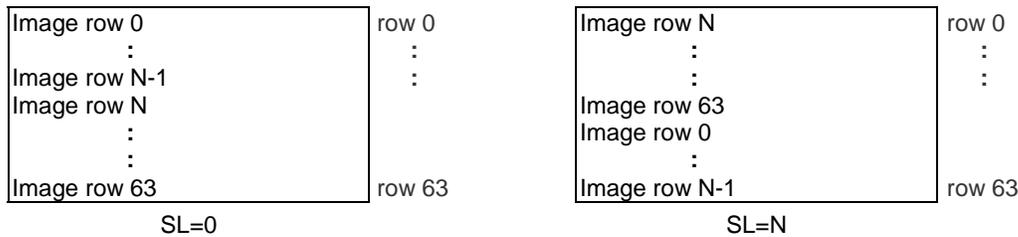
7. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address, PA[3:0]	0	0	1	0	1	1	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = 0~8.

8. Set V_{LCD} Resistor Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{LCD} Resistor Ratio, PC[5:3]	0	0	**0**	**0**	**1**	**0**	**0**	PC5	PC4	PC3

Configure PC[5:3] to set internal Resistor Ratio, Rb/Ra, for the V_{LCD} Voltage regulator to adjust the contrast of the display panel:

PC[5:3] : 000b~111b – 1+Rb/Ra ratio. Default : 100b. Refer to V_{LCD} Quick Reference for "1+Rb/Ra" ratio.

$V_{LCD}=((1+Rb/Ra) \times Vev) \times (1+(T-25)\times C_T\%)$ $Vev=(1-(63-PM)/162)\times V_{REF}$

where Rb and Ra are internal resistors,
V_{REF} is on-chip contrast voltage, and
PM is a vaule of electronic volume

9. Set Electronic Volume

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Electronic Volume, PM[5:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
			0	**0**	PM5	PM4	PM3	PM2	PM1	PM0

Set PM[5:0] for electronic volume "PM" for VLCD voltage regulator to adjust contrast of LCD panel display

Effective range : 0~63. Default : 32

10. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON, DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM. Default : 0

11. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display, DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

12. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable, DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1701x will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers.

13. Set SEG Direction

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Segment Direction, LC[0]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	MX

Set LC[0] for SEG (column) mirror (MX). **Default : 0**

MX is implemented by reversing the mapping order between RAM and SEG (column) electrodes. The data stored in RAM is not affected by MX command. Yet, MX has immediate effect on the display image.

14. Set COM Direction

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Common Direction, LC[1]	0	0	**1**	**1**	**0**	**0**	MY	-	-	-

Set LC[1] for COM (row) mirror (MY).

MY is implemented by reversing the mapping between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. Yet, MY has immediate effect on the display image.

15. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

16. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for "no operation".

17. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio, BR	0	0	1	0	1	0	0	0	1	BR

Select voltage bias ratio required for LCD. **Default : 0**

The setting of Bias ratio varies according to Duty:

DUTY	BR = 0	BR = 1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

18. Set Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Cursor Update Mode	0	0	1	1	1	0	0	0	0	0

This command is used for set cursor update mode function. When cursor update mode sets, UC1701x will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation. The set cursor update mode can be used to implement "write after read RAM" function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when reset cursor update mode.

The purpose of this pair commands and their feature is to support "write after read" function for cursor implementation.

19. Reset Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0

Set AC3=0 and CA=CR.

20. Set Static Indicator OFF

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Turn OFF Static Indicator	0	0	1	0	1	0	1	1	0	0

No Operation.

21. Set Static Indicator ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Turn ON Static Indicator	0	0	1	0	1	0	1	1	0	1
	0	0	-	-	-	-	-	-	-	-

No Operation.

22. Set Booster Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Booster Ratio	0	1	1	1	1	1	1	0	0	0
(Double-byte command)			0	0	0	0	0	0	-	-

This command is used for "No Operation".

23. Set Power Save

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Power Save (Compound Command)	0	0	#	#	#	#	#	#	#	#

24. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	1	1	1	1	1	1	1	TT	
(Double-byte command)			-	#	#	#	#	#	#	#

This command is for UltraChip's Test only. Do NOT use.

25. Set Advanced Program Control 0

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control, APC0 [7:0]	0	0	1	1	1	1	1	0	1	0
(Double-byte command)			TC	0	0	1	0	0	WA1	WA0

TC : APC0 [7], V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
   TC : 0b = -0.05%/^{o}C,   **1b = -0.11%/^{o}C**

WA : APC0 [1:0], Automatic column/row wrap around.
   WA[0] : **0: PA WA disable**   1: PA WA enable.
   WA[1] : **0: CA WA disable**   1: CA WA enable.

26. Set Advanced Program Control 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control, APC1 [7:0]	0	0	1	1	1	1	1	0	1	1
(Double-byte command)			APC1 register parameter							

For UltraChip only. Please Do _NOT_ use.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1701x via registers CEN, DST, DEN, and partial display control flags LC[4].

Combined with low power partial display mode and a low bias ratio of 6, UC1701x can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (BR) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1701x supports four *BR* as listed below. BR can be selected by software program.

	Bias Ratio	
Duty	BR=0	BR=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

The temperature compensation coefficients is -0.11% per ^{o}C.

V_{LCD} GENERATION

V_{LCD} is supplied by internal charge pump. The source of V_{LCD} is controlled by PC[2:0]. For good product reliability, it is recommended to keep V_{LCD} under 11.5V for all temperature conditions.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *PC[5:3]* (V_{LCD} Resistor Ratio) with the following relationship:

$$V_{LCD}=((1+Rb/Ra) \times Vev) \times (1+(T-25)xC_T\%)$$

$$Vev=(1-(63-PM)/162)xV_{REF}$$

where

Ra and Rb are two design constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is value of electronic volume,

V_{REG} is on-chip contrast voltage,

T is the ambient temperature in ^{O}C, and

C_T is temperature compensation coefficient.

V_{LCD} FINE TUNING

Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LEM design

LOAD DRIVING STRENGTH

The power supply circuit of UC1701x is designed to handle LCD panels with loading up to ~24nF using 20-Ω/Sq ITO glass with $V_{DD2/3} \geqslant$ 2.4V. For larger LCD panels, use lower resistance ITO glass packaging.

V~LCD~ QUICK REFERENCE
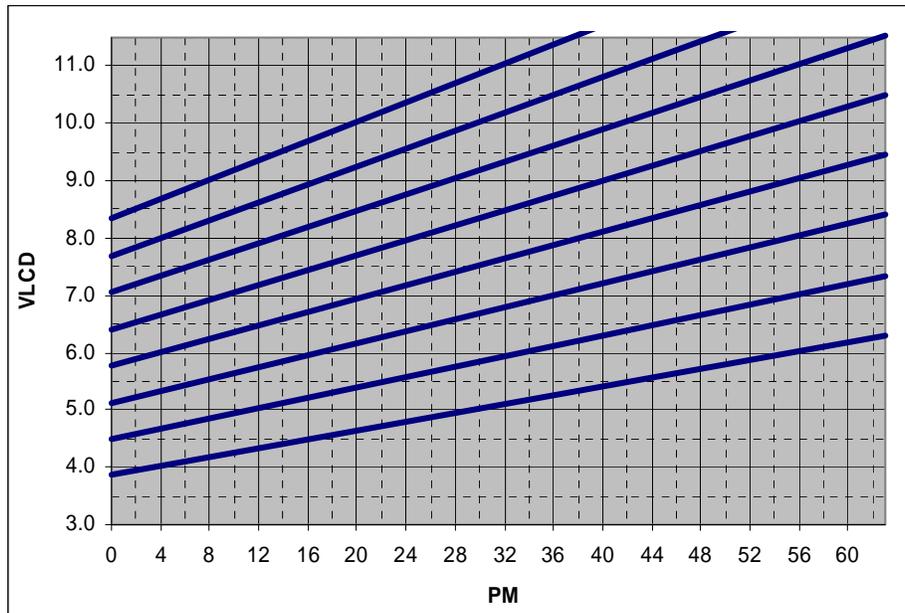
V~LCD~ Programming Curve.

PC[5:3]	1+Rb/Ra	V~REF~	PM	V~LCD~ Range (V)
000b	3.769	1.68	0	3.87
			63	6.33
001b	4.396	1.68	0	4.51
			63	7.38
010b	5.020	1.68	0	5.15
			63	8.43
011b	5.643	1.68	0	5.79
			63	9.48
100b	6.266	1.68	0	6.43
			63	10.53
101b	6.891	1.68	0	7.08
			62	11.51
110b	7.517	1.68	0	7.72
			48	11.46
111b	8.143	1.68	0	8.36
			37	11.48

Note: For good product reliability, keep V~LCD~ under **11.5V** over all temperature.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT
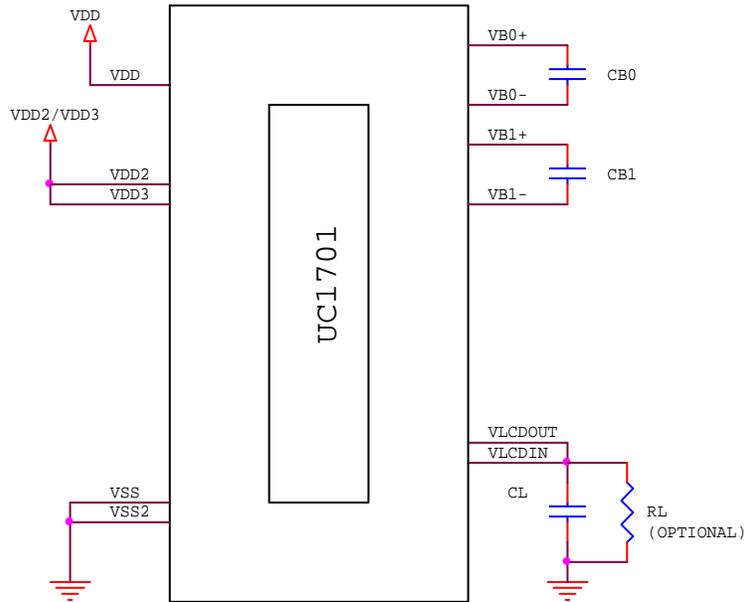
FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_{Bx} : 2.2 µF/5V or 100~250x LCD load capacitance.

C_L : 330nF(25V) is appropriate for most applications.

R_L: 3.3M~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1701x contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

4 different frame rates are provided based on different Mux-Rate for system design flexibility.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COMx, where x = 1~64, refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1701x will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1",and UC1701x will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1701x can be as short as 153μS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 9.23\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 2.76\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 6.30\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / (# of column), where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, and crosstalk will increase.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72~0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Example:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/65	1/9	10.6%	9.6%	7.5%
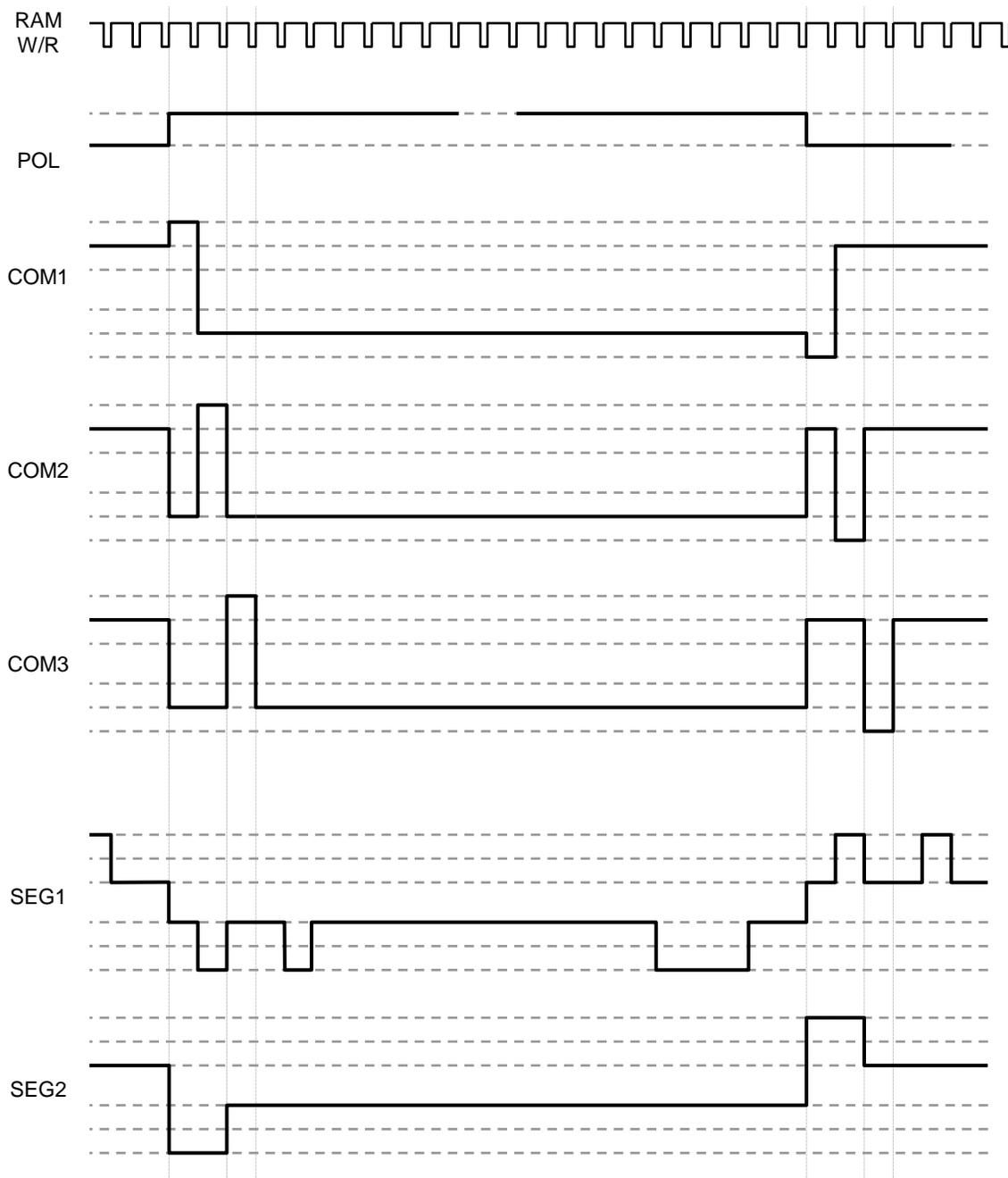
FIGURE 2: COM and SEG Electrode Driving Waveform

THE COMMON OUTPUT STATUS SELECT CIRCUIT

In the UC1701x chips, the COM output scan direction can be selected by the common output status select command. (See the table below for details.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Duty	Direction	COM[1:16]	COM[17:24]	COM[25:27]	COM[28:37]	COM[38:40]	COM[41:48]	COM[49:64]	COMS
1/65	0	COM [1:64]							COMS
	1	COM [64:1]							
1/49	0	COM[1:24]		NC			COM [25:48]		COMS
	1	COM[48:25]		NC			COM [24:1]		
1/33	0	COM[1:16]	NC					COM[17:32]	COMS
	1	COM[32:17]	NC					COM[16:1]	
1/55	0	COM [1:27]			NC	COM [28:54]			COMS
	1	COM [54:28]			NC	COM [27:1]			

Table 2: Duty Layout

HOST INTERFACE

As summarized in the table below, UC1701x supports two 8-bit parallel bus protocols and one serial bus protocol. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

		Bus Type		
		8080	**6800**	**S8 (4-wire)**
Width		8-bit	8-bit	Serial
Access		Read / Write		Write only
Control & Data Pins	BM[1:0]	10	11	00
	CS0	Chip Select		
	CD	Control/Data		
	WR0	$\overline{\text{WR}}$	R/$\overline{\text{W}}$	–
	WR1	$\overline{\text{RD}}$	EN	–
	DB[5:0]	Data		–
	DB[7:6]	Data		DB[6]=SCK, DB[7]=SDA

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Bus Interface	CS Init. Bus State	RESET Init. Bus State
8-bit	✔	–	✔
S8	✔	✔	✔

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- RESET can be pin reset / soft reset / power on reset.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1701x internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either `Set CA` or

`Set PA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.
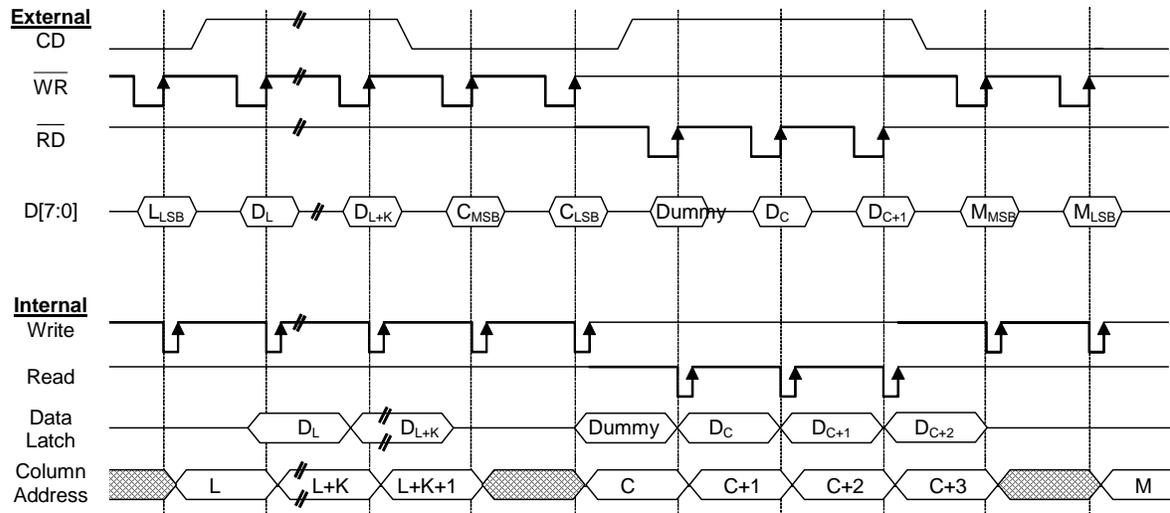
Figure 3: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1701x supports 1 serial modes: 4-wire SPI mode (S8). Bus interface mode is determined by the wiring of the BM[1:0]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.
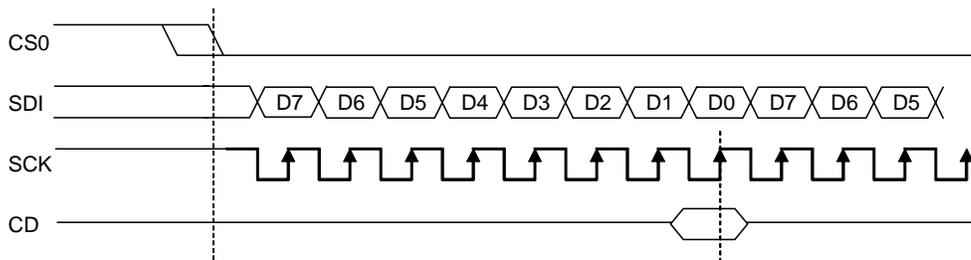
Figure 4: 4-wire Serial Interface (S8)

HOST INTERFACE REFERENCE CIRCUIT
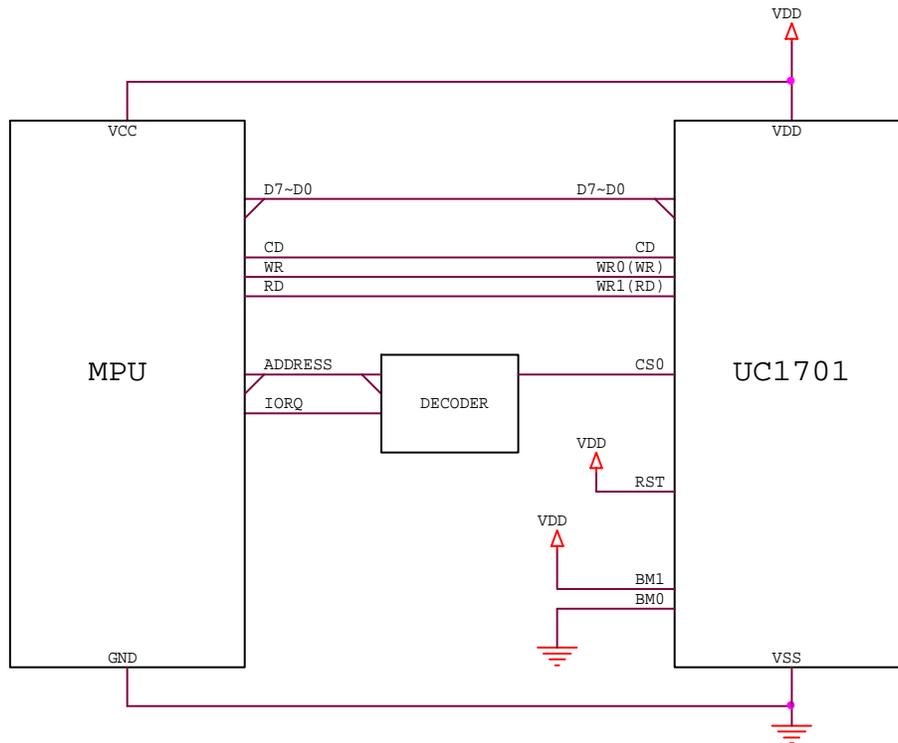
FIGURE 5: 8080/8bit parallel mode reference circuit
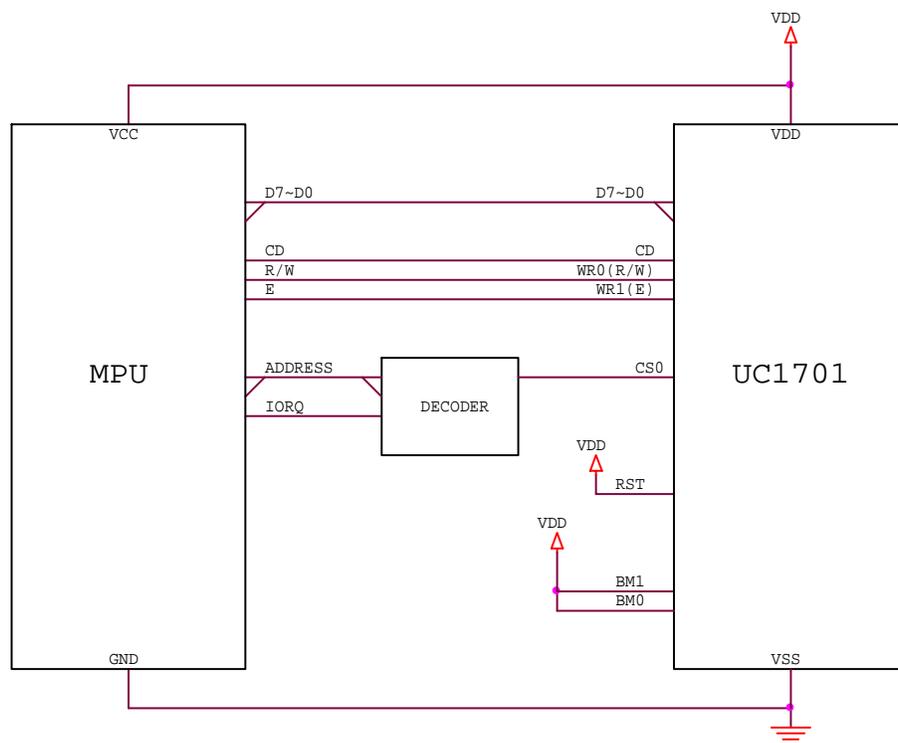
FIGURE 6: 6800/8bit parallel mode reference circuit
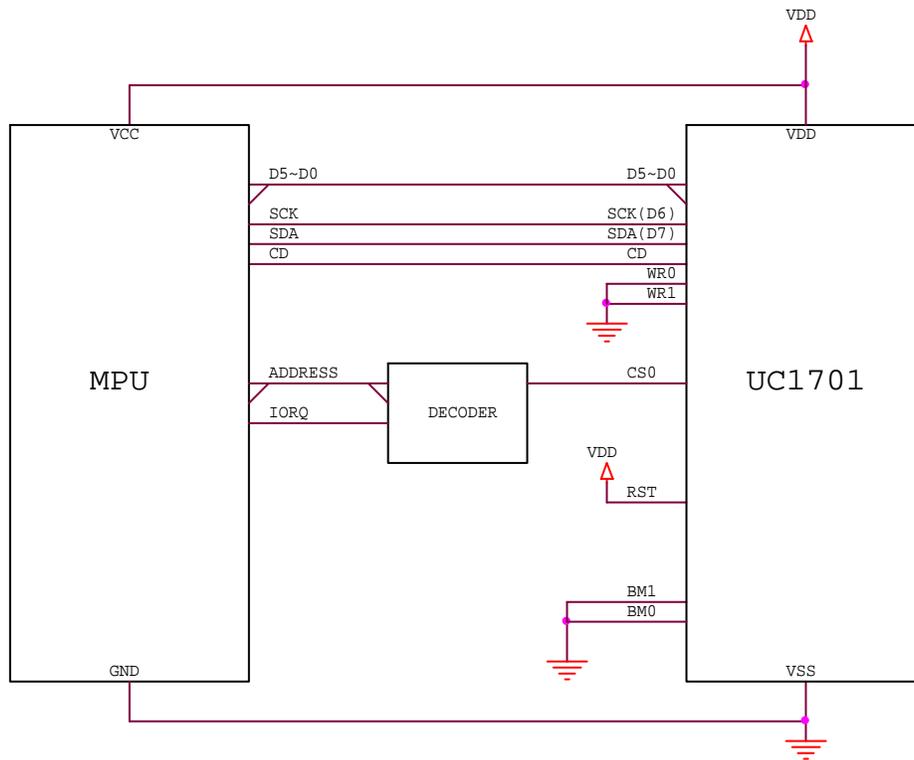
FIGURE 7: Serial-8 serial mode reference circuit

Note

- The ID pins are for production control. The connection will affect the content of D[7] of the 1st byte of the `Get Status` command. Connect to V_{DD} for "H" or V_{SS} for "L".

- RST pin is optional. When the RST pin is not used, connect it to V_{DD}.

- When using I²C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.

- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data is stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 65x132.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (131–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
$Line = SL$
Otherwise
$Line = Mod(Line+1, 64)$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
$Line = Mod(SL + MR - 1, 64)$
Otherwise
$Line = Mod(Line-1, 64)$

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

Memory mapping table:

PA[3:0]	0	Line Address	Page	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=25	MY=1 SL=25	MY=1 SL=25
0000	D0	00H	Page 0	C1	C49	C64	C48	C25	C9
	D1	01H		C2	C50	C63	C47	C24	C8
	D2	02H		C3	C51	C62	C46	C23	C7
	D3	03H		C4	C52	C61	C45	C22	C6
	D4	04H		C5	C53	C60	C44	C21	C5
	D5	05H		C6	C54	C59	C43	C20	C4
	D6	06H		C7	C55	C58	C42	C19	C3
	D7	07H		C8	C56	C57	C41	C18	C2
0001	D0	08H	Page 1	C9	C57	C56	C40	C17	C1
	D1	09H		C10	C58	C55	C39	C16	---
	D2	0AH		C11	C59	C54	C38	C15	---
	D3	0BH		C12	C60	C53	C37	C14	---
	D4	0CH		C13	C61	C52	C36	C13	---
	D5	0DH		C14	C62	C51	C35	C12	---
	D6	0EH		C15	C63	C50	C34	C11	---
	D7	0FH		C16	C64	C49	C33	C10	---
0010	D0	10H	Page 2	C17	C1	C48	C32	C9	---
	D1	11H		C18	C2	C47	C31	C8	---
	D2	12H		C19	C3	C46	C30	C7	---
	D3	13H		C20	C4	C45	C29	C6	---
	D4	14H		C21	C5	C44	C28	C5	---
	D5	15H		C22	C6	C43	C27	C4	---
	D6	16H		C23	C7	C42	C26	C3	---
	D7	17H		C24	C8	C41	C25	C2	---
0011	D0	18H	Page 3	C25	C9	C40	C24	C1	---
	D1	19H		C26	C10	C39	C23	C64	C48*
	D2	1AH		C27	C11	C38	C22	C63	C47
	D3	1BH		C28	C12	C37	C21	C62	C46
	D4	1CH		C29	C13	C36	C20	C61	C45
	D5	1DH		C30	C14	C35	C19	C60	C44
	D6	1EH		C31	C15	C34	C18	C59	C43
	D7	1FH		C32	C16	C33	C17	C58	C42
0100	D0	20H	Page 4	C33	C17	C32	C16	C57	C41
	D1	21H		C34	C18	C31	C15	C56	C40
	D2	22H		C35	C19	C30	C14	C55	C39
	D3	23H		C36	C20	C29	C13	C54	C38
	D4	24H		C37	C21	C28	C12	C53	C37
	D5	25H		C38	C22	C27	C11	C52	C36
	D6	26H		C39	C23	C26	C10	C51	C35
	D7	27H		C40	C24	C25	C9	C50	C34
0101	D0	28H	Page 5	C41	C25	C24	C8	C49	C33
	D1	29H		C42	C26	C23	C7	C48	C32
	D2	2AH		C43	C27	C22	C6	C47	C31
	D3	2BH		C44	C28	C21	C5	C46	C30
	D4	2CH		C45	C29	C20	C4	C45	C29
	D5	2DH		C46	C30	C19	C3	C44	C28
	D6	2EH		C47	C31	C18	C2	C43	C27
	D7	2FH		C48	C32	C17	C1	C42	C26
0110	D0	30H	Page 6	C49	C33	C16	---	C41	C25
	D1	31H		C50	C34	C15	---	C40	C24
	D2	32H		C51	C35	C14	---	C39	C23
	D3	33H		C52	C36	C13	---	C38	C22
	D4	34H		C53	C37	C12	---	C37	C21
	D5	35H		C54	C38	C11	---	C36	C20
	D6	36H		C55	C39	C10	---	C35	C19
	D7	37H		C56	C40	C9	---	C34	C18
0111	D0	38H	Page 7	C57	C41	C8	---	C33	C17
	D1	39H		C58	C42	C7	---	C32	C16
	D2	3AH		C59	C43	C6	---	C31	C15
	D3	3BH		C60	C44	C5	---	C30	C14
	D4	3CH		C61	C45	C4	---	C29	C13
	D5	3DH		C62	C46	C3	---	C28	C12
	D6	3EH		C63	C47	C2	---	C27	C11
	D7	3FH		C64	C48	C1	---	C26	C10
1000	D0	40H	Page 8	CIC	CIC	CIC	CIC	CIC	CIC

MUX: | 65 | 49 | 65 | 49 |

Segment order:
- MX = 0: SEG1, SEG2, SEG3, SEG4, SEG5, SEG6, SEG7, SEG8 ... SEG128, SEG129, SEG130, SEG131, SEG132
- MX = 1: SEG132, SEG131, SEG130, SEG129, SEG128, SEG127, SEG126, SEG125 ... SEG5, SEG4, SEG3, SEG2, SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 (D7-D0) : 11100000b
⇒ Page 0 SEG 2 (D7-D0) : 00110011b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1701x has two different types of Reset:
Power-ON-Reset and System-Reset.

Power-ON-Reset is performed right after V_{DD} is connected to power. Power-On-Reset will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the System Reset.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means System Reset.

The differences between hardware reset and software reset are

Procedure	Hardware Reset	Software Reset
Display OFF: DC[2]=0, all SEGs/COMs output at V$_{SS}$	V	X
Normal Display: DC[0]=0, DC[1]=0	V	X
SEG Normal Direction: MX=0	V	X
Clear Serial Counter and Shift Register (if using Serial Interface)	V	X
Bias Selection: BR=0	V	X
Booster Level BL[1:0]=0	V	X
Exit Power Saving Mode	V	X
Power Control OFF: PC[2:0]=000b	V	X
Exit Cursor Update mode	V	V
Scroll Line SL[5:0]=0	V	V
Column Address CA[7:0]=0	V	V
Page Address PA[3:0]=0	V	V
COM Normal Direction: MY=0	V	V
V$_{LCD}$ Regulation Ratio PC[5:3]=100b	V	V
PM[5:0]=10 0000b	V	V
Exit Test Mode	V	V

RESET STATUS

When UC1701x enters RESET sequence:

- Operation mode will be "Reset"

- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1701x has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:
Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter power saving mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, and C_L. To drain these capacitors, use Reset command to activate the on-chip draining circuit..

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Even though UC1701x consumes very little energy in Sleep mode (typically under 2μA); however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1701x contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1701x internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1701x power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmer is required to wait for only 5 ~ 10 mS before starting to issue commands to UC1701x. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

Turn on the Power

Set RST Low

Wait ≥ 1 mS

Set RST High

Wait ≥ 5 mS

(Issue commands)

Wait for MTP-READ ≥ 120mS

Set LCD Bias Ratio (BR)

Set Electronic Volume (PM)

Set Display Enable (AFH)
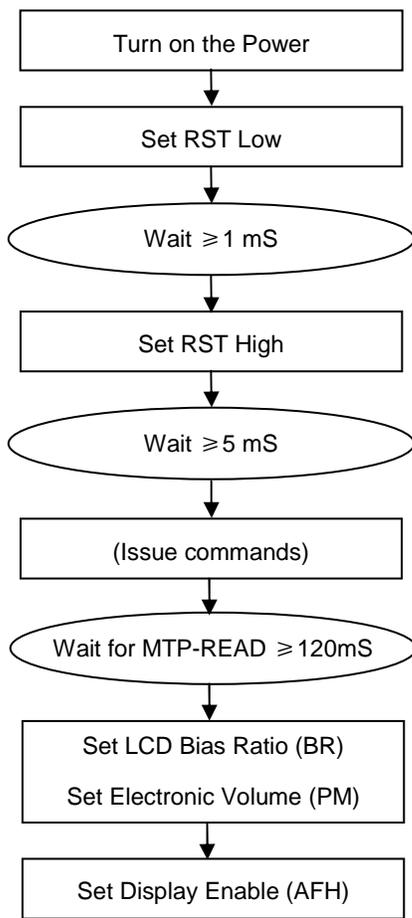
FIGURE 8: Reference Power-Up Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1503t enters Sleep mode from Display mode by issuing Set Display Disable command and setting all-pixel-ON.

To exit Sleep mode, set All-pixel-OFF.

Display Mode

Set Display OFF (AEH)
Set All-pixel-ON (A5H)

Sleep Mode

Set All-pixel-OFF (A4H)

Set Display Enable (AFH)
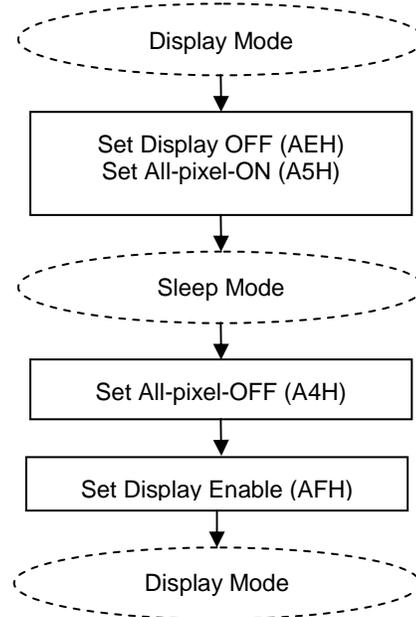
Display Mode

FIGURE 6: Reference Enter/Exit Sleep Mode Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

Reset command

Wait ~1 mS

Turn OFF the power
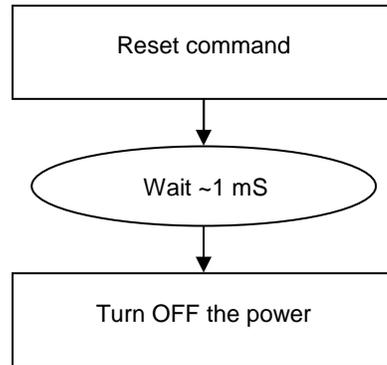
FIGURE 9: Reference Power-Down Sequence

Either V_{DD} or $V_{DD2/3}$ may be turned on first.

$T_{Wait} > 10mS$
$V_{DD} < 0.1V$

$V_{DD2/3} \geq 2.5V$
$V_{DD} \geq 1.8V$
$V_{DD2/3} \geq V_{DD}$

$T_f < 10$ mS

$10\mu S < T_1 < 10$ mS
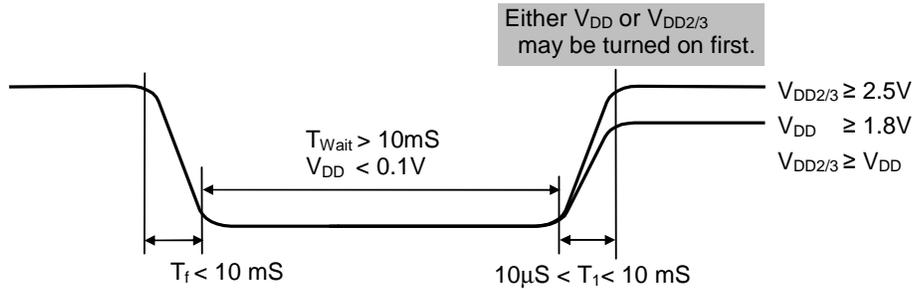
Figure 10: Power Off-On Sequence

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D   The type of the interface cycle. It can be either Command (0) or Data (1)
W/R   The direction of data flow of the cycle. It can be either Write (0) or Read (1).
Type   Required: These items are required
            Customized: These items are not necessary if customer parameters are the same as default
            Advanced: We recommend new users to skip these commands and use default values.
            Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~5mS after V_{DD} is ON
A	0	0	1	1	1	1	1	0	1	0	Set Adv. Program Control 0	
			1	0	0	1	0	0	1	1		Set Wrap Around Enable
C	0	0	1	0	1	0	0	0	0	#	Set SEG Direction	Set up LCD format specific
C	0	0	1	1	0	0	#	–	–	–	Set COM Direction	parameters, MX, MY, etc.
C	0	0	1	0	1	0	0	0	1	#	Set LCD Bias Ratio	LCD specific operating
R	0	0	1	0	0	0	0	0	0	1	Set Electronic Volume	voltage setting
	0	0	0	0	#	#	#	#	#	#		
O	1	0	#	#	#	#	#	#	#	#		
	.	.	.	.	.	.	.	.	.	.	Write display RAM	Set up display image
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image
	.	.	.	.	.	.	.	.	.	.		update is optional. Data in
	.	.	.	.	.	.	.	.	.	.		the RAM is retained through
	1	0	#	#	#	#	#	#	#	#		the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1700 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1701x require special "ESD Sensitivity" consideration in particular:

Test Mode Pins		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		150V	150V	2000V	1500V
LCM Digital Interface		300V	250V	3000V	3000V
LCM HV Interface	TST1/2/4	300V	300V	3000V	3000V
	C_B pins	300V	300V	3000V	3000V
	V_{LCDIN}	250V	300V	3000V	3000V
	V_{LCDOUT}	300V	300V	3000V	3000V
PWR/GND		--	300V	--	3000V

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 - notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+13.2	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V

2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65	1.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.4	2.5~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geq$ 2.4V, 25°C			11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geq$ 2.4V, 25°C	0.80		1.32	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3}$ = 3.3V, Temp = 85°C			50	µA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		2000	3000	Ω
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		2000	3000	Ω
F_{FR}	Average Frame Rate	Duty=1/65	-10%	77	+10%	Hz
		Duty=1/49		153		
		Duty=1/33		76		
		Duty=1/55		136		

POWER CONSUMPTION

V_{DD} = 2.7 V,   Bias Ratio = 0b,   PM = 32,
V_{LCD} = 8.49 V   Frame Rate = 77Hz, C_L = 330 nF,
Mux Rate = 65,   Bus mode = 6800,   All outputs are open circuit.
C_B = 2.2 µF   Temperature = 25°C

Display Pattern	Conditions	Typ.	Max.
All-OFF	Bus = idle	190	304
2-pixel checker	Bus = idle	192	308
1-pixel checker	Bus = idle	203	325
-	Bus = idle (standby current)	-	5

AC CHARACTERISTICS
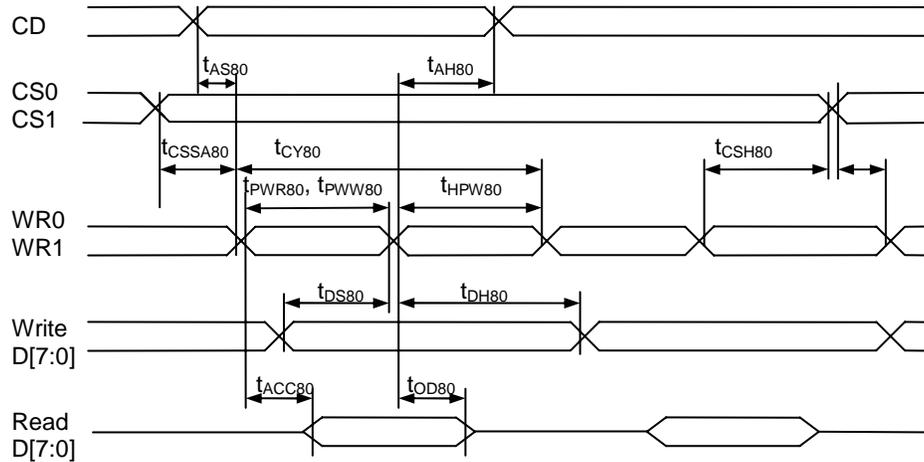
FIGURE 11: Parallel Bus Timing Characteristics (for 8080 MCU)

$(2.5V \leqslant V_{DD} < 3.3V$, Ta= −30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address	setup time		0	–	nS
			hold time		5		
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select	setup time		5	–	nS
			hold time		5		
t_{CY80}		Cycle time	read		120	–	nS
			write		80		
t_{PWR80} t_{PWW80}	WR1 WR0	Pulse width	read		60	–	nS
			write		40		
t_{HPW80}	WR0, WR1	High pulse width	read		60	–	nS
			write		40		
t_{DS80} t_{DH80}	D7~D0	Data	setup time		30	–	nS
			hold time		0		
t_{ACC80} t_{OD80}		Read access time Output disable time		$C_L = 100pF$	– 20	60 –	nS

$(1.65V \leqslant V_{DD} < 2.5V$, Ta= −30 to +85°C)

| Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address	setup time		0	–	nS
			hold time		0		
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select	setup time		5	–	nS
			hold time		5		
t_{CY80}		System cycle time	read		240	–	nS
			write		160		
t_{PWR80} t_{PWW80}	WR1 WR0	Pulse width	read		120	–	nS
			write		80		
t_{HPW80}	WR0, WR1	High pulse width	read		120	–	nS
			write		80		
t_{DS80} t_{DH80}	D7~D0	Data	setup time		60	–	nS
			hold time		0		
t_{ACC80} t_{OD80}		Read access time Output disable time		$C_L = 100pF$	– 50	100 –	nS
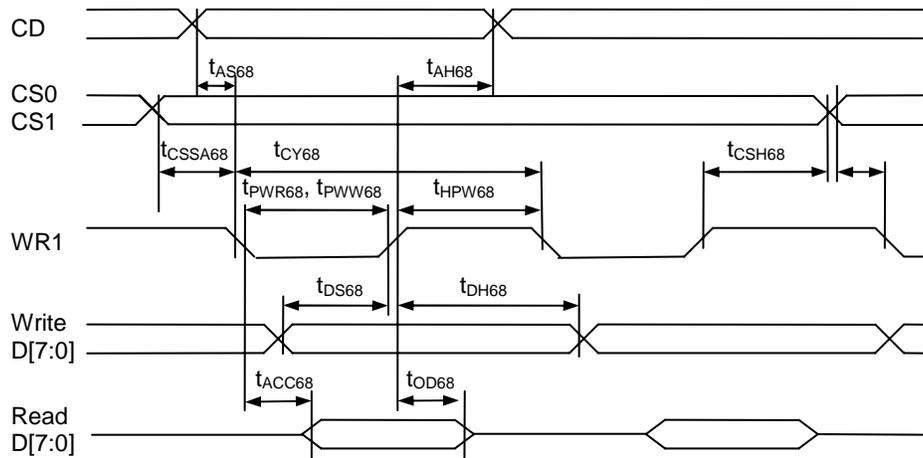
FIGURE 12: Parallel Bus Timing Characteristics (for 6800 MCU)

$(2.5V \leqslant V_{DD} < 3.3V, Ta= -30$ to $+85^{\circ}C)$

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address	setup time		0	–	nS
			hold time		0		
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select	setup time		5	–	nS
			hold time		5		
t_{CY68}		System cycle time	read		120	–	nS
			write		80		
t_{PWR68} t_{PWW68}	WR1	Pulse width	read		60	–	nS
			write		40		
t_{HPW68}		High pulse width	read		60	–	nS
			write		40		
t_{DS68} t_{DH68}	D7~D0	Data	setup time		30	–	nS
			hold time		0		
t_{ACC68} t_{OD68}		Read access time Output disable time		$C_L = 100pF$	– 50	60 –	nS

$(1.65V \leqslant V_{DD} < 2.5V, Ta= -30$ to $+85^{\circ}C)$

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address	setup time		0	–	nS
			hold time		0		
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select	setup time		5		nS
			hold time		5		
t_{CY68}		cycle time	read		240	–	nS
			write		160		
t_{PWR68} t_{PWW68}	WR1	Pulse width	read		120	–	nS
			write		80		
t_{HPW68}		High pulse width	read		120	–	nS
			write		80		
t_{DS68} t_{DH68}	D7~D0	Data	setup time		60	–	nS
			hold time		0		
t_{ACC68} t_{OD68}		Read access time Output disable time		$C_L = 100pF$	– 100	100 –	nS
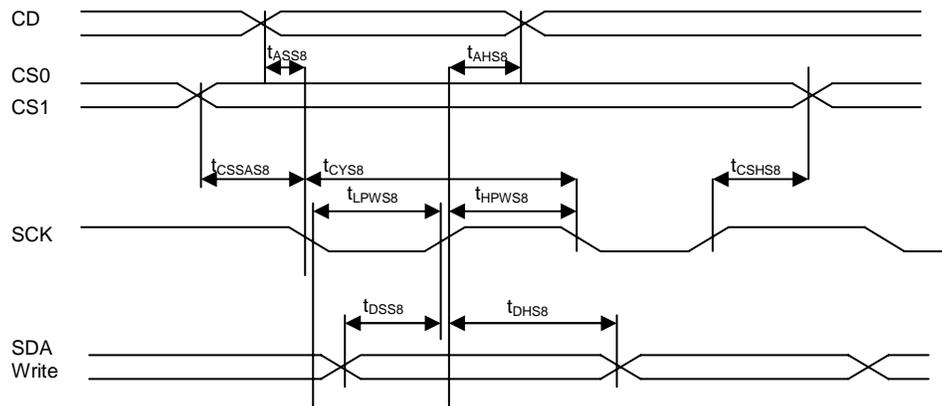
FIGURE 13: Serial Bus Timing Characteristics (for S8)

$(2.5V \leqslant V_{DD} < 3.3V$, Ta= −30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{ASS8}	CD	Address	setup time		0	–	nS
t_{AHS8}			hold time		0		
t_{CSSAS8}	CS1/CS0	Chip select	setup time		5	–	nS
t_{CSHS8}			hold time		5		
t_{CYS8}		Cycle time	read		100	–	nS
			write		30		
t_{LPWS8}	SCK	Low pulse width	read		50	–	nS
			write		15		
t_{HPWS8}		High pulse width	read		50	–	nS
			write		15		
t_{DSS8}	SDA	Data	setup time		12	–	nS
t_{DHS8}			hold time		0		

$(1.65V \leqslant V_{DD} < 2.5V$, Ta= −30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{ASS8}	CD	Address	setup time		0	–	nS
t_{AHS8}			hold time		0		
t_{CSSAS8}	CS1/CS0	Chip select	setup time		10	–	nS
t_{CSHS8}			hold time		10		
t_{CYS8}		Cycle time	read		130	–	nS
			write		60		
t_{LPWS8}	SCK	Low pulse width	read		65	–	nS
			write		30		
t_{HPWS8}		High pulse width	read		65	–	nS
			write		30		
t_{DSS8}	SDA	Data	setup time		24	–	nS
t_{DHS8}			hold time		0		
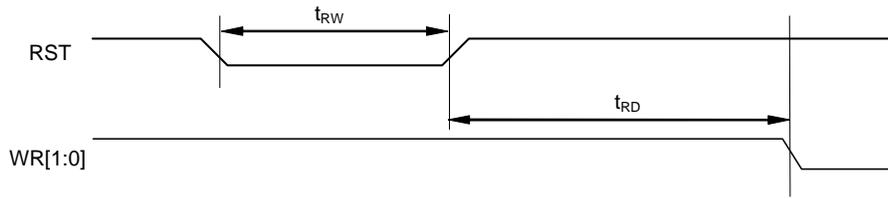
FIGURE 14: Reset Characteristics

(1.65V ≤ V_{DD} < 3.3V, Ta= −30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		6	–	mS

PHYSICAL DIMENSIONS

DIE SIZE:
4850 μM x 660 μM ± 40 μM

DIE THICKNESS:
400 μM ± 20 μM

BUMP HEIGHT:
15 μM ± 3 μM
(H_{MAX} – H_{MIN}) within die ≤ 2 μM

BUMP SIZE:
15 μM x 138.5 μM ± 2 μM (Typ.)

BUMP PITCH:
27 μM

BUMP GAP:
12 μM

COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

(Drawing and coordinates are for the Circuit/Bump view.)
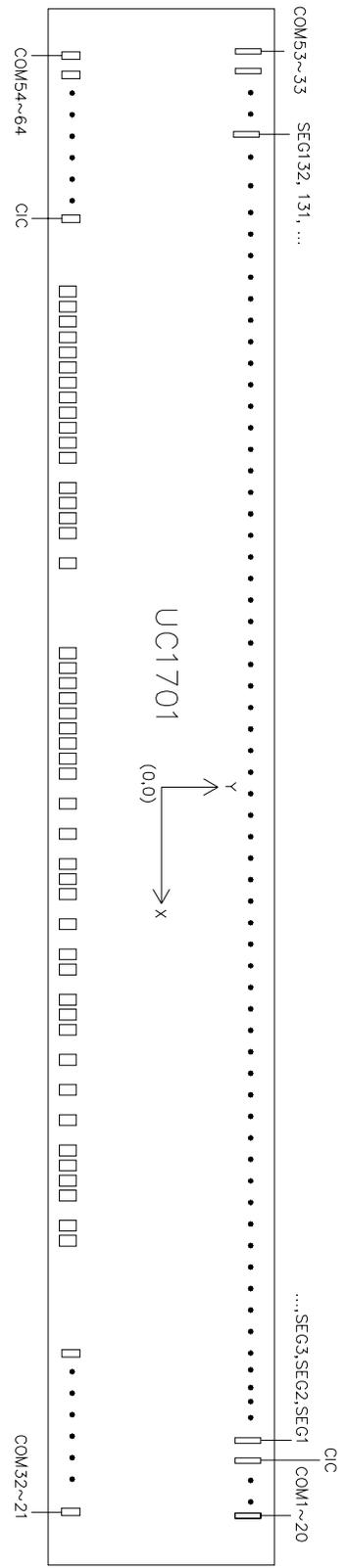
ALIGNMENT MARK INFORMATION
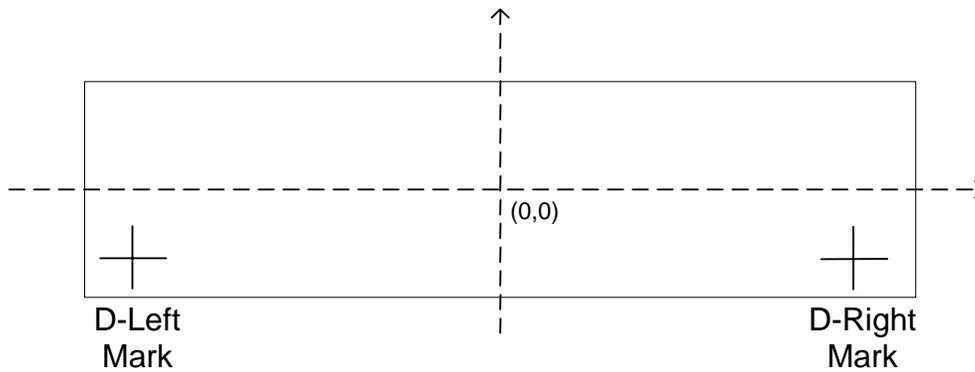
SHAPE OF THE ALIGNMENT MARK:
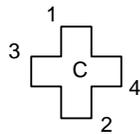
NOTE:

Alignment mark is on Metal3 under Passivation.

The "+" mark is symmetric both horizontally and vertically.

COORDINATES:

	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	-1984.5	-149.5	1969.5	-149.5
2	-1969.5	-184.5	1984.5	-184.5
3	-1994.5	-159.5	1959.5	-159.5
4	-1959.5	-174.5	1994.5	-174.5
C	-1977	-167	1977	-167

TOP METAL AND PASSIVATION:

SiN / 7KÅ

SiO2 / 5KÅ

Metal3 / 9KÅ

FOR PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H	#	Pad	X	Y	W	H	#	Pad	X	Y	W	H
1	COM54	-2363	-227.75	15	138.5	59	DUMMY	985	-274.5	45	45	117	SEG9	1552.5	227.75	15	138.5
2	COM55	-2336	-227.75	15	138.5	60	DUMMY	1040	-274.5	45	45	118	SEG10	1525.5	227.75	15	138.5
3	COM56	-2309	-227.75	15	138.5	61	DUMMY	1095	-274.5	45	45	119	SEG11	1498.5	227.75	15	138.5
4	COM57	-2282	-227.75	15	138.5	62	DUMMY	1150	-274.5	45	45	120	SEG12	1471.5	227.75	15	138.5
5	COM58	-2255	-227.75	15	138.5	63	DUMMY	1205	-274.5	45	45	121	SEG13	1444.5	227.75	15	138.5
6	COM59	-2228	-227.75	15	138.5	64	DUMMY	1260	-274.5	45	45	122	SEG14	1417.5	227.75	15	138.5
7	COM60	-2201	-227.75	15	138.5	65	TST2	1320	-274.5	50	45	123	SEG15	1390.5	227.75	15	138.5
8	COM61	-2174	-227.75	15	138.5	66	VSSL	1385	-274.5	50	45	124	SEG16	1363.5	227.75	15	138.5
9	COM62	-2147	-227.75	15	138.5	67	VDDX	1450	-274.5	50	45	125	SEG17	1336.5	227.75	15	138.5
10	COM63	-2120	-227.75	15	138.5	68	BM0	1515	-274.5	50	45	126	SEG18	1309.5	227.75	15	138.5
11	COM64	-2093	-227.75	15	138.5	69	BM1	1580	-274.5	50	45	127	SEG19	1282.5	227.75	15	138.5
12	CIC	-2066	-227.75	15	138.5	70	DT1	1645	-274.5	50	45	128	SEG20	1255.5	227.75	15	138.5
13	TST4	-1970	-274.5	50	45	71	VSSX	1710	-274.5	50	45	129	SEG21	1228.5	227.75	15	138.5
14	CS0	-1905	-274.5	50	45	72	DT2	1775	-274.5	50	45	130	SEG22	1201.5	227.75	15	138.5
15	RST	-1840	-274.5	50	45	73	VDD1	1840	-274.5	50	45	131	SEG23	1174.5	227.75	15	138.5
16	CD	-1775	-274.5	50	45	74	VDD2	1905	-274.5	50	45	132	SEG24	1147.5	227.75	15	138.5
17	WR0	-1710	-274.5	50	45	75	VDD3	1970	-274.5	50	45	133	SEG25	1120.5	227.75	15	138.5
18	WR1	-1645	-274.5	50	45	76	COM32	2066	-227.75	15	138.5	134	SEG26	1093.5	227.75	15	138.5
19	VDDX	-1580	-274.5	50	45	77	COM31	2093	-227.75	15	138.5	135	SEG27	1066.5	227.75	15	138.5
20	D0	-1515	-274.5	50	45	78	COM30	2120	-227.75	15	138.5	136	SEG28	1039.5	227.75	15	138.5
21	D1	-1450	-274.5	50	45	79	COM29	2147	-227.75	15	138.5	137	SEG29	1012.5	227.75	15	138.5
22	D2	-1385	-274.5	50	45	80	COM28	2174	-227.75	15	138.5	138	SEG30	985.5	227.75	15	138.5
23	D3	-1320	-274.5	50	45	81	COM27	2201	-227.75	15	138.5	139	SEG31	958.5	227.75	15	138.5
24	D4	-1255	-274.5	50	45	82	COM26	2228	-227.75	15	138.5	140	SEG32	931.5	227.75	15	138.5
25	D5	-1190	-274.5	50	45	83	COM25	2255	-227.75	15	138.5	141	SEG33	904.5	227.75	15	138.5
26	D6	-1125	-274.5	50	45	84	COM24	2282	-227.75	15	138.5	142	SEG34	877.5	227.75	15	138.5
27	D7	-1060	-274.5	50	45	85	COM23	2309	-227.75	15	138.5	143	SEG35	850.5	227.75	15	138.5
28	VDD1	-995	-274.5	50	45	86	COM22	2336	-227.75	15	138.5	144	SEG36	823.5	227.75	15	138.5
29	VDD1	-930	-274.5	50	45	87	COM21	2363	-227.75	15	138.5	145	SEG37	796.5	227.75	15	138.5
30	VDD2	-865	-274.5	50	45	88	COM20	2363	227.75	15	138.5	146	SEG38	769.5	227.75	15	138.5
31	VDD2	-800	-274.5	50	45	89	COM19	2336	227.75	15	138.5	147	SEG39	742.5	227.75	15	138.5
32	VDD2	-735	-274.5	50	45	90	COM18	2309	227.75	15	138.5	148	SEG40	715.5	227.75	15	138.5
33	VDD3	-670	-274.5	50	45	91	COM17	2282	227.75	15	138.5	149	SEG41	688.5	227.75	15	138.5
34	VSS1	-605	-274.5	50	45	92	COM16	2255	227.75	15	138.5	150	SEG42	661.5	227.75	15	138.5
35	VSS1	-540	-274.5	50	45	93	COM15	2228	227.75	15	138.5	151	SEG43	634.5	227.75	15	138.5
36	VSS2	-475	-274.5	50	45	94	COM14	2201	227.75	15	138.5	152	SEG44	607.5	227.75	15	138.5
37	VSS2	-410	-274.5	50	45	95	COM13	2174	227.75	15	138.5	153	SEG45	580.5	227.75	15	138.5
38	VSS2	-345	-274.5	50	45	96	COM12	2147	227.75	15	138.5	154	SEG46	553.5	227.75	15	138.5
39	VSS2	-280	-274.5	50	45	97	COM11	2120	227.75	15	138.5	155	SEG47	526.5	227.75	15	138.5
40	VB1+	-215	-274.5	50	45	98	COM10	2093	227.75	15	138.5	156	SEG48	499.5	227.75	15	138.5
41	VB1+	-150	-274.5	50	45	99	COM9	2066	227.75	15	138.5	157	SEG49	472.5	227.75	15	138.5
42	DUMMY	-85	-274.5	50	45	100	COM8	2039	227.75	15	138.5	158	SEG50	445.5	227.75	15	138.5
43	VB0+	-20	-274.5	50	45	101	COM7	2012	227.75	15	138.5	159	SEG51	418.5	227.75	15	138.5
44	VB0+	45	-274.5	50	45	102	COM6	1985	227.75	15	138.5	160	SEG52	391.5	227.75	15	138.5
45	VB0-	110	-274.5	50	45	103	COM5	1958	227.75	15	138.5	161	SEG53	364.5	227.75	15	138.5
46	VB0-	175	-274.5	50	45	104	COM4	1931	227.75	15	138.5	162	SEG54	337.5	227.75	15	138.5
47	DUMMY	240	-274.5	50	45	105	COM3	1904	227.75	15	138.5	163	SEG55	310.5	227.75	15	138.5
48	VB1-	305	-274.5	50	45	106	COM2	1877	227.75	15	138.5	164	SEG56	283.5	227.75	15	138.5
49	VB1-	370	-274.5	50	45	107	COM1	1850	227.75	15	138.5	165	SEG57	256.5	227.75	15	138.5
50	VB1+	435	-274.5	50	45	108	CIC	1823	227.75	15	138.5	166	SEG58	229.5	227.75	15	138.5
51	VB1+	500	-274.5	50	45	109	SEG1	1768.5	227.75	15	138.5	167	SEG59	202.5	227.75	15	138.5
52	VLCDIN	565	-274.5	50	45	110	SEG2	1741.5	227.75	15	138.5	168	SEG60	175.5	227.75	15	138.5
53	VLCDIN	630	-274.5	50	45	111	SEG3	1714.5	227.75	15	138.5	169	SEG61	148.5	227.75	15	138.5
54	VLCDOUT	695	-274.5	50	45	112	SEG4	1687.5	227.75	15	138.5	170	SEG62	121.5	227.75	15	138.5
55	VLCDOUT	760	-274.5	50	45	113	SEG5	1660.5	227.75	15	138.5	171	SEG63	94.5	227.75	15	138.5
56	DUMMY	820	-274.5	45	45	114	SEG6	1633.5	227.75	15	138.5	172	SEG64	67.5	227.75	15	138.5
57	DUMMY	875	-274.5	45	45	115	SEG7	1606.5	227.75	15	138.5	173	SEG65	40.5	227.75	15	138.5
58	DUMMY	930	-274.5	45	45	116	SEG8	1579.5	227.75	15	138.5	174	SEG66	13.5	227.75	15	138.5

#	Pad	X	Y	W	H
175	SEG67	-13.5	227.75	15	138.5
176	SEG68	-40.5	227.75	15	138.5
177	SEG69	-67.5	227.75	15	138.5
178	SEG70	-94.5	227.75	15	138.5
179	SEG71	-121.5	227.75	15	138.5
180	SEG72	-148.5	227.75	15	138.5
181	SEG73	-175.5	227.75	15	138.5
182	SEG74	-202.5	227.75	15	138.5
183	SEG75	-229.5	227.75	15	138.5
184	SEG76	-256.5	227.75	15	138.5
185	SEG77	-283.5	227.75	15	138.5
186	SEG78	-310.5	227.75	15	138.5
187	SEG79	-337.5	227.75	15	138.5
188	SEG80	-364.5	227.75	15	138.5
189	SEG81	-391.5	227.75	15	138.5
190	SEG82	-418.5	227.75	15	138.5
191	SEG83	-445.5	227.75	15	138.5
192	SEG84	-472.5	227.75	15	138.5
193	SEG85	-499.5	227.75	15	138.5
194	SEG86	-526.5	227.75	15	138.5
195	SEG87	-553.5	227.75	15	138.5
196	SEG88	-580.5	227.75	15	138.5
197	SEG89	-607.5	227.75	15	138.5
198	SEG90	-634.5	227.75	15	138.5
199	SEG91	-661.5	227.75	15	138.5
200	SEG92	-688.5	227.75	15	138.5
201	SEG93	-715.5	227.75	15	138.5
202	SEG94	-742.5	227.75	15	138.5
203	SEG95	-769.5	227.75	15	138.5
204	SEG96	-796.5	227.75	15	138.5
205	SEG97	-823.5	227.75	15	138.5
206	SEG98	-850.5	227.75	15	138.5
207	SEG99	-877.5	227.75	15	138.5
208	SEG100	-904.5	227.75	15	138.5
209	SEG101	-931.5	227.75	15	138.5
210	SEG102	-958.5	227.75	15	138.5
211	SEG103	-985.5	227.75	15	138.5
212	SEG104	-1012.5	227.75	15	138.5
213	SEG105	-1039.5	227.75	15	138.5
214	SEG106	-1066.5	227.75	15	138.5
215	SEG107	-1093.5	227.75	15	138.5
216	SEG108	-1120.5	227.75	15	138.5
217	SEG109	-1147.5	227.75	15	138.5
218	SEG110	-1174.5	227.75	15	138.5
219	SEG111	-1201.5	227.75	15	138.5
220	SEG112	-1228.5	227.75	15	138.5
221	SEG113	-1255.5	227.75	15	138.5
222	SEG114	-1282.5	227.75	15	138.5
223	SEG115	-1309.5	227.75	15	138.5
224	SEG116	-1336.5	227.75	15	138.5
225	SEG117	-1363.5	227.75	15	138.5
226	SEG118	-1390.5	227.75	15	138.5
227	SEG119	-1417.5	227.75	15	138.5
228	SEG120	-1444.5	227.75	15	138.5
229	SEG121	-1471.5	227.75	15	138.5
230	SEG122	-1498.5	227.75	15	138.5
231	SEG123	-1525.5	227.75	15	138.5
232	SEG124	-1552.5	227.75	15	138.5
233	SEG125	-1579.5	227.75	15	138.5
234	SEG126	-1606.5	227.75	15	138.5

#	Pad	X	Y	W	H
235	SEG127	-1633.5	227.75	15	138.5
236	SEG128	-1660.5	227.75	15	138.5
237	SEG129	-1687.5	227.75	15	138.5
238	SEG130	-1714.5	227.75	15	138.5
239	SEG131	-1741.5	227.75	15	138.5
240	SEG132	-1768.5	227.75	15	138.5
241	COM33	-1823	227.75	15	138.5
242	COM34	-1850	227.75	15	138.5
243	COM35	-1877	227.75	15	138.5
244	COM36	-1904	227.75	15	138.5
245	COM37	-1931	227.75	15	138.5
246	COM38	-1958	227.75	15	138.5
247	COM39	-1985	227.75	15	138.5
248	COM40	-2012	227.75	15	138.5
249	COM41	-2039	227.75	15	138.5
250	COM42	-2066	227.75	15	138.5
251	COM43	-2093	227.75	15	138.5
252	COM44	-2120	227.75	15	138.5
253	COM45	-2147	227.75	15	138.5
254	COM46	-2174	227.75	15	138.5
255	COM47	-2201	227.75	15	138.5
256	COM48	-2228	227.75	15	138.5
257	COM49	-2255	227.75	15	138.5
258	COM50	-2282	227.75	15	138.5
259	COM51	-2309	227.75	15	138.5
260	COM52	-2336	227.75	15	138.5
261	COM53	-2363	227.75	15	138.5

TRAY INFORMATION

晶粒盤規格		199\34-24(橫)
1	晶粒盤外圍尺寸 (L1)	50.75
2	晶粒盤外圍尺寸 (L2)	45.50
3	晶粒盤底部尺寸 (L3)	45.70
4	晶粒盤全高 (T)	4.00
5	第一晶穴中心X軸 (SX)	6.45
6	第一晶穴中心Y軸 (SY)	4.27
7	第一晶穴基準中心 (S)	7.73
8	晶穴寬度X軸 (X)	5.05
9	晶穴長度Y軸 (Y)	0.86
10	晶穴深度Z軸 (Z)	0.61
11	晶穴間距X軸 (Px)	6.31
12	晶穴間距Y軸 (Py)	2.01
13	晶穴數X軸 (Nx)	7
14	晶穴數Y軸 (Ny)	22
15	晶穴總數 (N)	154
16	晶粒盤內圍高 (P1)	1.76
17	晶粒盤底部深 (P2)	1.60

SECTION A-A

20-199x34-24

7X22=154
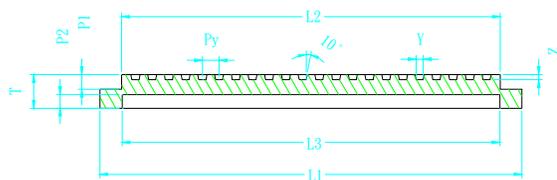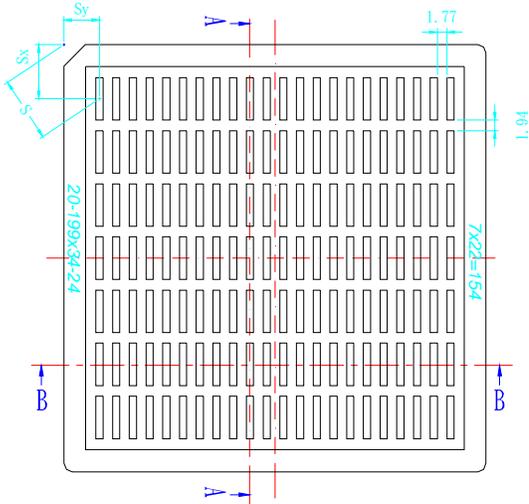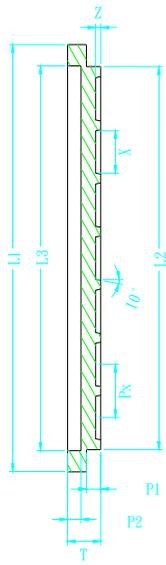
SECTION B-B

<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e11 ohm/SQ
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: Max. 0.1mm
6. We can put a piece of Lint free paper between the two trays.
7. The die thickness is 0.4 mm
8. The bottom of pocketRough pattern

Unless Otherwise Specified		
General Roughness		N/A
Unit		mm
Tolerance	Dimension	+/-0.1
	Angle	N/A

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	First release	Jul. 29, 2008

0.7	(1) A new register, APC, is added.
	    (Section "Control Registers", page 10)
	
	(2) Command "Set Advanced Program Control" is split into 2 commands.
	    (Section "Command Table", - (25)(26), page 12;
	        "Command Description" – (25)(26), page 17)
	
	(3) The sample codes for Power-Up are updated.
	    (Section "Sample Command Sequences for Power Management", page 34)
	
	(4) The tray drawing is updated.
	    (Section "Tray Information", page 46)
		Aug. 8, 2008

0.8	(1) V$_{LCD}$ data are updated.
	    (Section "V$_{LCD}$ Quick Reference", page 19)
	
	(2) The description on Mux-Rate is updated.
	    (Section "LCD Display Controls" – Clock & Timing Generator, page 21)
	
	(3) Power consumption data present.
	    (Section "Specifications" – Power Consumption, page 37)
	
	(4) Some AC timings are adjusted.
	    (Section "AC Characteristics", Pp 38~40)
		Aug. 27, 2008

1.0	(1) The setting of WR[1:0] in S8 mode is updated: 0 → –
	    (Section "Pin Description" – WR1~0, page 7;
	        "Host Interface", page 25)
	
	(2) Power Up and Enter/Exit Sleep Mode sequences are updated.
	    (Section "Reset & Power Management", page 32)
	
	(3) ESD data are corrected.
	    (Section "ESD Consideration", page 36)
		Nov. 7, 2008