HIGH-VOLTAGE MIXED-SIGNAL IC

UC1628

163 x 256 STN LCD Controller-Driver

MP Specifications
Datasheet Revision: 1.1

IC Version: c_A
June 24, 2020

ULTRACHIP

The Coolest LCD Driver, Ever!!

TABLE OF CONTENT

UC1628

Single-Chip, Ultra-Low Power
163COM x 256SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1628c is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1628c contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, battery operated hand held devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 163x256 graphics STN LCD panels.
- A software-readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both page ordered and column ordered display buffer RAM access.
- Support industry standard 4-wire (S8), and 2-wire (I^2C) serial interface and 8-bit parallel bus (8080 or 6800).
- Fully programmable Mux Rate, partial display window, Bias Ratio and Frame Rate allow many flexible power management options.
- Four software programmable frame rates. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 5 temperature compensation coefficients.
- Self-configuring 9x charge pump with on-chip pumping capacitors. Only 3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (7 pins for S8 or 5 pins for I^2C) allows exceptional image quality in COG format on conventional ITO glass.
- Built-in temperature sensor
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range (Typ.) : 2.8V ~ 3.3V
  $V_{DD2/3}$ (analog) range (Typ.) : 2.8V ~ 3.3V
  LCD V_{OP} range: 6.35V ~ 17.52V
- OTP trimming available to support precise LCD contrast matching.
- Suitable ACF size: 3uM or 4uM
- Available in gold bump dies
  Bump pitch: 23.2 μM
  Bump space: 12 μM ± 3μM
  Bump surface: 1500.8 μM^2

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document..

ORDERING INFORMATION

Part Number	OTP	I²C	Description
UC1628cGAA	Yes	Yes	Gold bumped die, Bump Height: 10uM
UC1628cGBA	Yes	Yes	Gold bumped die, Bump Height: 15uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I²C

The implementation of I²C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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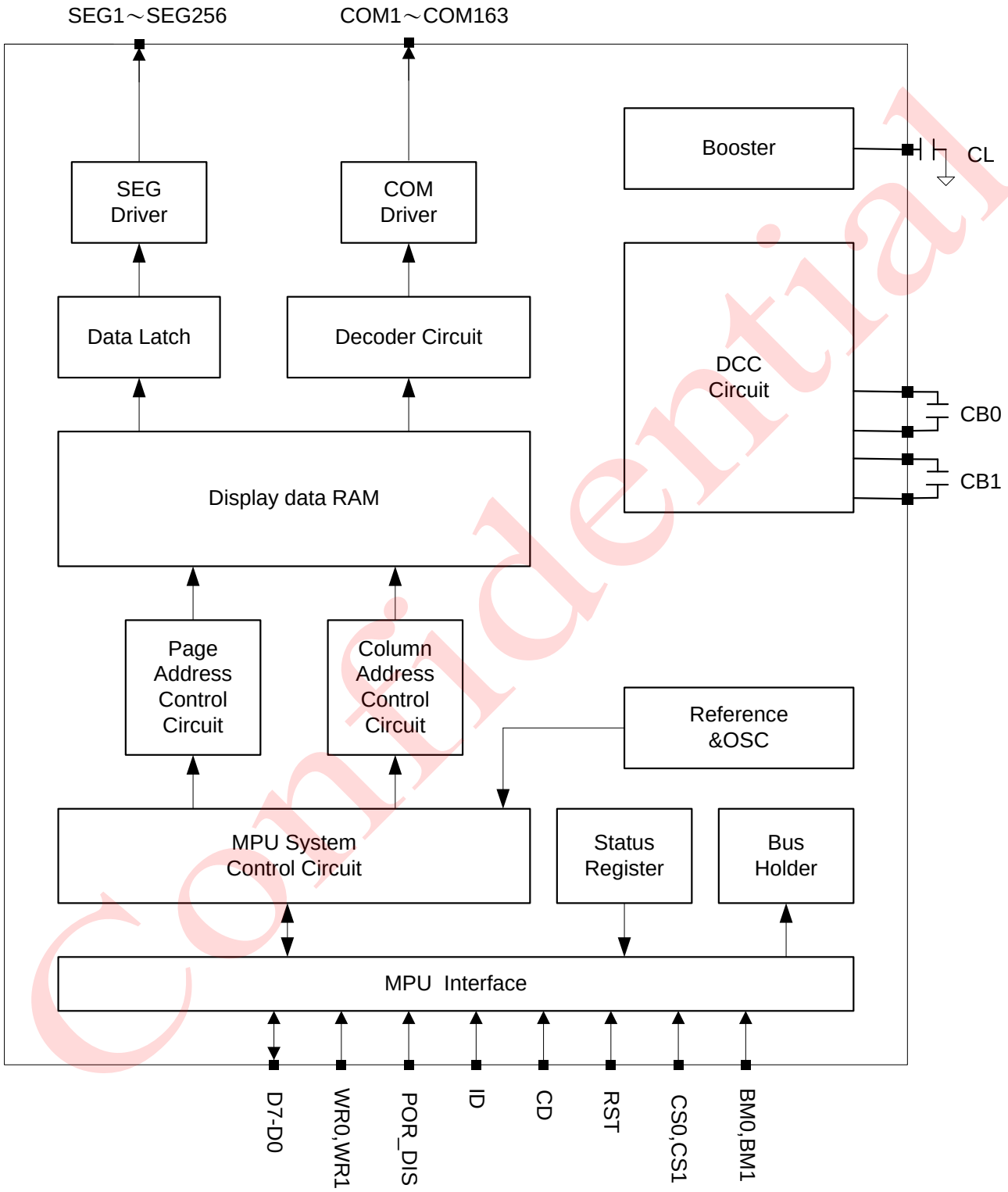
BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name (Pad Name)	Type	# of Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	14 13 5	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geq V_{DD2/3} \geq V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	15 13	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node. Connect Vss and Vss2 together.
V_{SSX}		6	Auxiliary V_{SS}. This pin is connected to the main V_{SS} bus within the IC. It's provided to facilitate chip configurations in COG application. There's no need to connect V_{SSX} to main V_{SS} externally and it should *NOT* be used to provide V_{SS} power to the chip.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B0+}, V_{B0-} V_{B1+}, V_{B1-} (VB0P_pad, VB0N_pad, VB1P_pad, VB1N_pad)	PWR	3, 3 3, 3	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} of values between V_{BX+}~V_{BX-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT} (VLCDIN_pad, VLCDOUT_pad)	PWR	4 5	High voltage LCD Power Supply. Capacitor C_L should be connected between V_{LCDOUT} and V_{SS}. When C_L is used, keep the trace resistance under 70Ω. When using internal pump, connect V_{LCDIN} and V_{LCDOUT} together. When using external pump, connect V_{LCDIN} to external power and connect a capacitor between V_{LCDOUT} and Vss.

NOTE

- Recommended capacitor values:
  C_{BX} : For panels of 3-inch or smaller, use 2.2uF (25V) capacitor;
  For panels bigger than 3 inches, use 5μF (25V) capacitor or higher.
  (Capacitor size depends on panel capacitance loading and actual image performance.)
  C_L : 330nF (25V) is appropriate for most applications.
- To avoid the correction of digital signals being affected by the charging/discharging of V_{BX}, do not overlay C_{BX} with the digital layout while FPC wiring.

<table>
<tr><th>Pin Name
(Pad Name)</th><th>Type</th><th># of Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1
(BM_pad<0>
BM_pad<1>)</td><td>I</td><td>2
2</td><td>Bus mode: The interface bus mode is determined by BM[1:0]:
<table>
<tr><th>Mode</th><th>BM[1:0]</th></tr>
<tr><td>8080 (8-bit)</td><td>10</td></tr>
<tr><td>6800 (8-bit)</td><td>11</td></tr>
<tr><td>4-wire SPI w/ 8-bit token (S8)</td><td>01</td></tr>
<tr><td>2-wire SPI (I²C)</td><td>00</td></tr>
</table></td></tr>
<tr><td>CS0
CS1
(CS_pad<0>
CS_pad<1>)</td><td>I</td><td>2
2</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, DB[7:0] will be high impedance.</td></tr>
<tr><td>RST
(RST_pad)</td><td>I</td><td>2</td><td>When RST=”L”, IC is in RESET state and all control registers are re-initialized to their default states.
An RC Filter has been included on-chip. There is no need for external RC noise filter.
Connect the RST pin to MCU for reset control.</td></tr>
<tr><td>CD
(CD_pad)</td><td>I</td><td>2</td><td>Select Control data or Display data for read/write operation.
”L”: Control data ”H”: Display data / command</td></tr>
<tr><td>ID
(ID_pad)</td><td>I</td><td>2</td><td>ID pin is for production control.
The connection will affect the content of PID when using the <code>Get Status</code> command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1
(WR_pad<0>
WR_pad<1>)</td><td>I</td><td>2
2</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>DB7~DB0
(DATA_pad<7> ~
DATA_pad<0>)</td><td>I/O</td><td>2x8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect DB[0] to SCK, DB[3] to SDAI for write and DB[5:4] to SDAO for read. SDAI and SDAO may be connected together if necessary.
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8-bit
(BM=1x)</td><td colspan="8">DB[7:0]</td></tr>
<tr><td>S8
(BM=01)</td><td>–</td><td>–</td><td>SDAO</td><td>SDAO</td><td>SDAI</td><td>–</td><td>–</td><td>SCK</td></tr>
<tr><td>I²C
(BM=00)</td><td>–</td><td>–</td><td>SDAO</td><td>SDAO</td><td>SDAI</td><td>–</td><td>–</td><td>SCK</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
</table>

Pin Name (Pad Name)	Type	# of Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG256 (SEG_pad<1> ~ SEG_pad<256>)	HV	256	SEG (column) driver outputs. Support up to 256 pixels. Leave unused drivers open-circuit.
COM1 ~ COM162 (COM_pad<1> ~ COM_pad<162>)	HV	162	COM (row) driver outputs. Support up to 162 rows. Leave unused COM drivers open-circuit.
ICON (ICONH_PAD, ICONL_PAD)	HV	1 1	Either one can be used as an ICON driver output. Leave it open if not used.
Note: Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, COM*x* or SEG*x* will correspond to index *x*-1, and the value ranges for those index registers will be 0~161 for COM and 0~255 for SEG.			
MISC. PINS			
POR_DIS (POR_DIS_pad)	I	2	Power-ON reset control. Connect POR_DIS to V_{DD} for "H"; to V_{SS} for "L". "L": Power-ON Reset Enabled "H": Power-ON Reset Disabled
TST2	I/O	2	Test I/O pin for UltraChip's use only. Leave it open during normal use.
TST4	I	3	TST4 is the high voltage programming power supply for OTP operation. For COG design with OTP options, please wire out TST4 with an ITO trace resistance < 70 Ω. Insulate it after programming. Leave TST4 floating if not under programming situation.
Dummy (DUMMY1~ DUMMY4)	–	4	Dummy pins are NOT connected inside the IC.
Note: R_L: Around 10MΩ, to act as a draining circuit when V_{DD} is shut down abruptly.			

RECOMMENDED WIRING RESISTANCE IN COG CASE:

Pin Type	Pin Name	Resistance
Power Supply	VDD1, VDD2, VDD3, VSS, VSSX, VLCDIN, VLCDOUT, VB0+, VB0-, VB1+, VB1-	< 100Ω
Logic	BM0, BM1, CS0, CS1, RST, CD, ID, WR0, WR1, DB7~DB0, POR, DIS, TST2	< 1KΩ
Others	TST4	< 70Ω

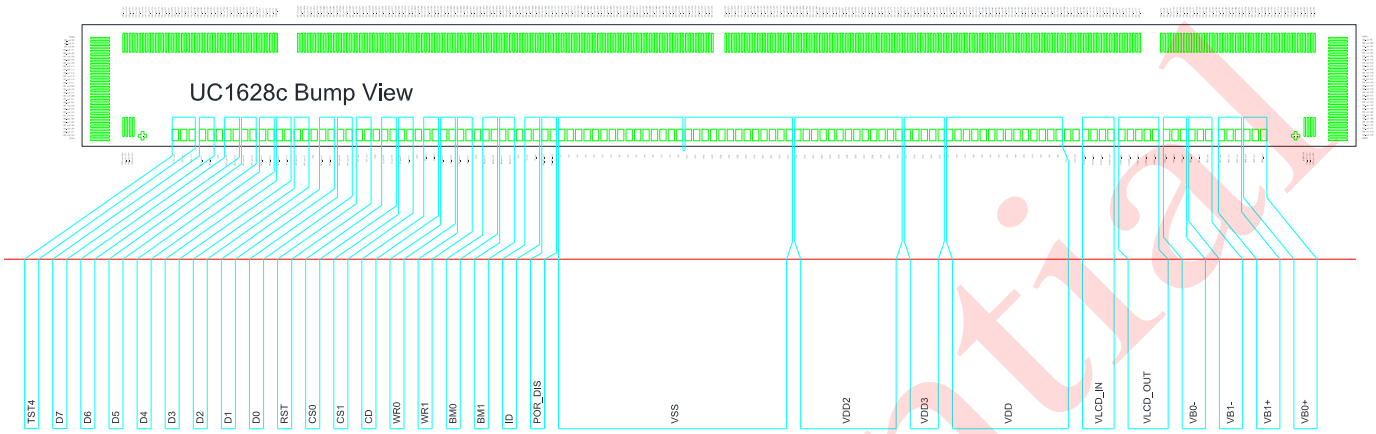
Note:

(1) The values in the table above may not be ideal for specific applications.

(2) For VDD ITO layout, it is recommended to separate VDD1, VDD2 and VDD3's ITO traces to minimize the effect of system noise.

(3) Connect Vss and Vss2 together.

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The typical operation condition of UC1628c, $V_{DD} \geqslant 2.7V$, $V_{DD2/3} > 2.7V$, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 20 Ω or lower; V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} drop to below 2.7V during high speed data-write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1628c contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1628c will be described in the next two sections: Command Table and Command Description.

Name: The Symbolic reference of the register.
Note that some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after Pin-Reset.

Name	# of Bits	Default	Description
SL	8	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and 161. Setting SL outside of this range will cause undefined effect on the displayed image.
CA	8	00H	Column Address of Display Data RAM (Used in Host for Display Data RAM access. Value range: 0 ~ 255)
PA	5	00H	Page Address of Display Data RAM (Used in Host to access Display Data RAM. Value range: 0 ~ 21) PA=21 for ICON line.
BR	3	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 000b: 6 001b: 10 010b: 11 **011b: 12** 100b: 13 101b: 14
TC	6	04H	Temperature Compensation (per °C) TC[2:0]: 000b: -0.00% **100b: -0.05%** 101b: -0.10% 110b: -0.15% 111b: -0.20% TC[3]: Vlcd Temperature Compensation Curve Control. **0: Disable** 1: Enable TC[4]: FR Temperature Compensation Curve Control. **0: Disable** 1: Enable TC[5]: Temperature Sensor Control. **0: Disable** 1: Enable
ST	8	N/A	ST[7:0]: Temperature.
TP	4	N/A	TP[3:0] Select: 0001b: Temp A 0010b: Temp B 0011b: Temp C 0100b: Temp D 0101b: Temp E 0110b: Temp F 0111b: Temp G 1000b: Temp H 1001b: Temp I
TEMPA	8	1Eh	1EH: -30°C (Min. Temperature can be set to -45 °C)
TEMPB	8	28H	28H: -20°C (TEMPA+8) ≤ TEMPB ≤ (TEMPA+31)
TEMPC	8	32H	32H: -10°C (TEMPB+8) ≤ TEMPC ≤ (TEMPB+31)
TEMPD	8	3CH	3CH: 0°C (TEMPC+8) ≤ TEMPD ≤ (TEMPC+31)
TEMPE	8	55H	55H: +25°C (TEMPD+8) ≤ TEMPE ≤ (TEMPD+31)
TEMPF	8	6EH	6EH: +50°C (TEMPE+8) ≤ TEMPF ≤ (TEMPE+31)
TEMPG	8	78H	78H: +60°C (TEMPF+8) ≤ TEMPG ≤ (TEMPF+31)
TEMPH	8	82H	82H: +70°C (TEMPG+8) ≤ TEMPH ≤ (TEMPG+31)
TEMPI	8	91H	91H: +85°C (TEMPH+8) ≤ TEMPI ≤ (TEMPH+31); TEMPI ≤ 164 (104°C) (Max. Temperature can be set to +90 °C)
PM	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage when TC[3]=0
PMA	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPA.
PMB	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPB; |PMB-PMA| ≤ 63
PMC	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPC; |PMC-PMB| ≤ 63
PMD	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPD; |PMD-PMC| ≤ 63
PME	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPE; |PME-PMD| ≤ 63
PMF	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPF; |PMF-PME| ≤ 63

Name	# of Bits	Default	Description
PMG	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPG; |PMG-PMF| ≤ 63
PMH	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPH; |PMH-PMG| ≤ 63
PMI	8	54H	Electronic Potentiometer to fine tune V_{LCD} voltage at TEMPI; |PMI-PMH| ≤ 63
FR	5	0DH	Frame Rate when TC[4]=0
FRA	5	0DH	Frame Rate at TEMPA.
FRB	5	0DH	Frame Rate at TEMPB.
FRC	5	0DH	Frame Rate at TEMPC.
FRD	5	0DH	Frame Rate at TEMPD.
FRE	5	0DH	Frame Rate at TEMPE.
FRF	5	0DH	Frame Rate at TEMPF.
FRG	5	0DH	Frame Rate at TEMPG.
FRH	5	0DH	Frame Rate at TEMPH.
FRI	5	0DH	Frame Rate at TEMPI.
PC	1	1H	Power Control. 0b: External V_{LCD} **1b: Internal V_{LCD}** (10x charge pump)
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**)
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0 : Column (CA) first** 1 : Row (PA) first AC[2]: PID: PA (Page Address) auto increment direction (**0 : +1** 1 : -1) AC[3]: CUM – Cursor Update Mode. (Default **0:OFF**) When CUM=1, CA increases at Write only and Wrap Around will be suspended.
LC	4	1H	LCD Control: LC[0]: Icon line display ON/OFF (Default: **1b: ON**) LC[1]: MX, Mirror X. SEG/Page_C sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**)LC[3]: Partial Display Control **0b: Disable** Mux-Rate = CEN+1+LC[0]x1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1+LC[0]x1
NIV	7	00H	N-line Inversion: NIV[5:0]: **000000b: Disable Inversion Function** 000001b~111111b: Invert every 2~64 lines NIV[6]: 0b: **no-XOR** 1b: XOR
CSF	1	0H	COM Scan Function **0: Interlace Scan** 1: Progressive Scan
CEN DST DEN	8 8 8	A1H 00H A1H	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = (the actual number of pixel rows on the LCD) - 1 CEN ⩾ DEN ⩾ (DST+ 9)

Name	# of Bits	Default	Description
OTPC	5	10H	OTP Programming Control: OTPC[2:0] : OTP command **000 : Idle** 001 : Normal Read 010 : Read for Program 011 : Program 1xx : For UltraChip use only. OTPC[3] : OTP Enable (automatically cleared after each OTP command) OTPC[4] : Use/Ignore OTP value. 0: Ignore **1: Use**
OTPA	6	00H	OTP cell address.
APC	8x4	N/A	For UltraChip only. Do *NOT* use.
Status Register			
POR	1	PIN	Access the connected status of POR_dis pin. 1/0 : disable/enable POR
PID	1	PIN	Access the connected status of ID pin.
OE	1	-	OTP flag: 1 for OTP version, 0 for non-OTP version.
OP	1	-	OTP programming in-progress
OD	1	-	OTP Read done.
PMO	6	00H	PM offset. PMO[5]=1: The effective PM value, PMV = PM – PMO[4:0] PMO[5]=0: The effective PM value, PMV = PM + PMO[4:0]

COMMAND SUMMARY

The following is a list of host commands supported by UC1628c:

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte (double-byte command)	0	0	0	0	0	0	0	0	0	1	Write 1 byte	N/A
		1	0	#	#	#	#	#	#	#	#		
2.	Read Data Byte (double-byte command)	0	0	0	0	0	0	0	0	1	0	Read 1 byte	N/A
		1	1	#	#	#	#	#	#	#	#		
3.	Get Status (triple-byte command)	0	0	0	0	0	0	0	0	1	1	Get Status	N/A
		1	1	POR	MX	MY	PID	DE	OD	OE	OP		
		1	1	Ver[1:0]		PMO[5:0]							
4.	Set Column Address (double-byte command)	0	0	0	0	0	0	0	1	0	0	Set CA[7:0]	00H
		1	0	#	#	#	#	#	#	#	#		
5.	Set Temp. vs. Vop Control	0	0	0	0	0	1	0	0	0	#	Set TC[3]	0b
6.	Set Temp. vs. FR Control	0	0	0	0	0	1	0	0	1	#	Set TC[4]	0b
7.	Set Temp. Sensor Control	0	0	0	0	0	1	0	1	0	#	Set TC[5]	0b
8.	Set FR at Different temperature (triple-byte command)	0	0	0	0	0	1	0	1	1	0	Set TP[3:0] Set FR[4:0]	N/A
		1	0	0	0	0	0	#	#	#	#		
		1	0	0	0	0	#	#	#	#	#		
9.	Set FR (triple-byte command)	0	0	0	0	0	1	0	1	1	0	Set FR[4:0]	01101b
		1	0	0	0	0	0	0	0	0	0		
		1	0	0	0	0	#	#	#	#	#		
10.	Set Temperature Point (triple-byte command)	0	0	0	0	0	1	0	1	1	1	Set TP[3:0] Set ST[7:0]	N/A
		1	0	0	0	0	0	#	#	#	#		
		1	0	#	#	#	#	#	#	#	#		
11.	Set Temp. Compensagion	0	0	0	0	1	0	0	#	#	#	Set TC[2:0]	100b
12.	Set Pump Control	0	0	0	0	1	0	1	1	0	#	Set PC	1b
13.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	R = 0, 1 ,2 or 3	N/A
		1	0	#	#	#	#	#	#	#	#	Set APC[R][7:0]	
14.	Set Scroll Line	0	0	0	1	0	0	0	0	0	0	Set SL[7:0]	00H
		1	0	#	#	#	#	#	#	#	#		
15.	Set Page Address	0	0	0	1	1	0	0	0	0	0	Set PA[4:0]	00H
		1	0	0	0	0	#	#	#	#	#		
16.	Set PM at Different temperature (triple-byte command)	0	0	1	0	0	0	0	0	0	1	Set TP[3:0] Set PM[7:0]	N/A
		1	0	0	0	0	0	#	#	#	#		
		1	0	#	#	#	#	#	#	#	#		
17.	Set PM (triple-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	54H
		1	0	0	0	0	0	0	0	0	0		
		1	0	#	#	#	#	#	#	#	#		

#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
18.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[3]	0b: Disable
19.	Set COM Scan Function	0	0	1	0	0	0	0	1	1	#	Set CSF	0b: Interlace
20.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
21.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
22.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
23.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	001b
24.	Set N-Line Inversion (double-byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H
		1	0	0	#	#	#	#	#	#	#		
25.	Set Display Enable unlock Set Display Enable	0	0	1	1	0	0	1	0	0	1	Set DC[2]	0b
		1	0	1	0	1	0	1	1	0	#		
26.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
27.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only.	N/A
		1	0	#	#	#	#	#	#	#	#	Do not use.	
28.	Set LCD Bias Ratio	0	0	1	1	1	0	1	#	#	#	Set BR[2:0]	011b
29.	Reset Cursor update mode	0	0	1	1	1	1	0	1	1	0	AC[3]=0, CA=CR	N/A
30.	Set Cursor update mode	0	0	1	1	1	1	0	1	1	1	AC[3]=1, CR=CA	N/A
31.	Set COM End (double-byte command)	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]	161
		1	0	#	#	#	#	#	#	#	#		
32.	Set Partial Display Start (double-byte command)	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]	0
		1	0	#	#	#	#	#	#	#	#		
33.	Set Partial Display End (double-byte command)	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	161
		1	0	#	#	#	#	#	#	#	#		
34.	Set OTP Operation Control (double-byte command)	0	0	1	0	1	1	1	0	0	0	Set OTPC[4:0]	00H
		1	0	0	0	0	#	#	#	#	#		
35.	Set OTP Write Address (double-byte command)	0	0	1	0	1	1	1	0	0	1	Set OTPA[5:0]	00H
		1	0	0	0	#	#	#	#	#	#		

Warning: Any bit patterns other than the commands listed above may result in undefined behavior.

COMMAND DESCRIPTION

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data (double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	8-bit data write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data (double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	1	1	8-bit data from SRAM							

Write/Read Data Byte (command 1, 2) operation uses internal Page Address register (PA) and Column Address register (CA). Four rows of LCD pixel image are defined as one row in SRAM. Each column of pixel corresponds to one column of SRAM data. PA and CA registers can be programmed by issuing `Set Page Address` and `Set Column Address` commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of PA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and PA will be increased or decreased, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 20), PA will be wrapped around to the other end of RAM and continue.

After issuing command 1 or 2, multiple bytes of data may be written or read, respectively, until next command is input. For 8-bit interface, the first cycle of read is a dummy read. Please ignore the data read out.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status (triple-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	1	1	POR	MX	MY	PID	DE	OD	OE	OP
	1	1	Ver[1:0]		PMO[5:0]					

Status 1 definitions:

- POR: Power-On-Reset status of accessing to POR_DIS pin. (0: POR enabled, 1: POR disabled)
- MX: Status of register LC[0], mirror X.
- MY: Status of register LC[1], mirror Y.
- PID: Provide connection status of accessing to ID pin.
- DE: Display enable flag. DE=1 when display is enabled
- OD: OTP Read done.
- OE: OTP flag (1: OTP version, 0 : non-OTP version)
- OP: OTP Programming in progress.

Status 2 definitions:

- Ver[1:0]: IC Version Code, 00 ~ 11. Default: 00
- PMO[5:0]: PM offset value.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address CA[7:0] (double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
	1	0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

Set SRAM column address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~255 (Default: 0)

(5) SET TEMPERATURE VS VOP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temp. vs Vop Control, TC[3]	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	TC3

TC[3]: V_{LCD} Temperature Compation Curve Control. **0b: Disable** 1b: Enable

(6) SET TEMPERATURE VS FR CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temp. vs FR Control, TC[4]	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	TC4

TC[4]: FR Temperature Compation Curve Control. **0b: Disable** 1b: Enable

(7) SET TEMPERATURE SENSOR CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temp. Sensor Control, TC[5]	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	TC5

TC[5]: Temperature Sensor Control **0b: Disable** 1b: Enable

(8) SET FR AT DIFFERENT TEMPERATURE WHEN TC[4]=1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TP[3:0], FR[4:0] (triple-byte command)	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**
	1	0	**0**	**0**	**0**	**0**	TP3	TP2	TP1	TP0
	1	0	**0**	**0**	**0**	FR4	FR3	FR2	FR1	FR0

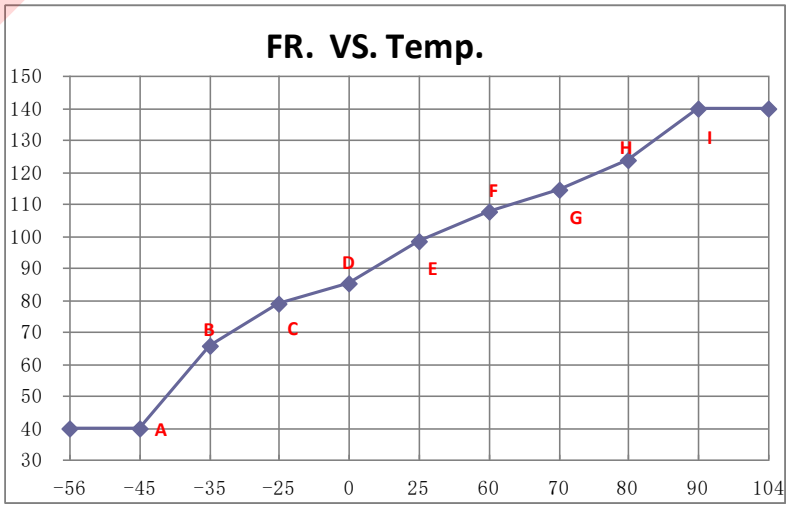
TP[3:0]: Select Temperature point.

0001b: Temp A 0010b: Temp B 0011b: Temp C 0100b: Temp D
0101b: Temp E 0110b: Temp F 0111b: Temp G 1000b: Temp H
1001b: Temp I

FR[4:0]: Frame Rate Setting. See command (9) for detail.

Example:

TP[3:0]	Temp. (°C)	FR[4:0]	FR(Hz)
--	-56	**--**	40.0
TEMPA	-45	FRA	40.0
TEMPB	-35	FRB	65.8
TEMPC	-25	FRC	78.7
TEMPD	0	FRD	85.2
TEMPE	25	FRE	98.1
TEMPF	60	FRF	107.7
TEMPG	70	FRG	114.2
TEMPH	80	FRH	123.9
TEMPI	90	FRI	140.0
--	104	--	140.0



(9) SET FR WHEN TC[4]=0

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set FR[4:0] (triple-byte command)	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**
	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	1	0	**0**	**0**	**0**	FR4	FR3	FR2	FR1	FR0

FR[4:0]: Frame Rate Setting. (Default: **0Dh: 81.9Hz**)

FR[4:0]	Fps (Hz)
00000	40.0
00001	43.2
00010	46.5
00011	49.7
00100	52.9
00101	56.1
00110	59.4
00111	62.6

FR[4:0]	Fps (Hz)
01000	65.8
01001	69.0
01010	72.3
01011	75.5
01100	78.7
01101	**81.9**
01110	85.2
01111	88.4

FR[4:0]	Fps (Hz)
10000	91.6
10001	94.8
10010	98.1
10011	101.3
10100	104.5
10101	107.7
10110	111.0
10111	114.2

FR[4:0]	Fps (Hz)
11000	117.4
11001	120.6
11010	123.9
11011	127.1
11100	130.3
11101	133.5
11110	136.8
11111	140.0

(10) SET TEMPERATURE POINT

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TP[3:0], TS[7:0] (triple-byte command)	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**
	1	0	**0**	**0**	**0**	**0**	TP3	TP2	TP1	TP0
	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

TP[3:0]: Select Temperature point.

TC[4]=1: 0001b: Temp A, 0010b: Temp B, 0011b: Temp C, 0100b: Temp D
0101b: Temp E, 0110b: Temp F, 0111b: Temp G, 1000b: Temp H
1001b: Temp I

TS[7:0]: Temperature

TS[7:0]	Temp.	TS[7:0]	Temp.	TS[7:0]	Temp.	TS[7:0]	Temp.	TS[7:0]	Temp.	TS[7:0]	Temp.
0F	-45	28	-20	41	5	5A	30	73	55	8C	80
10	-44	29	-19	42	6	5B	31	74	56	8D	81
11	-43	2A	-18	43	7	5C	32	75	57	8E	82
12	-42	2B	-17	44	8	5D	33	76	58	8F	83
13	-41	2C	-16	45	9	5E	34	77	59	90	84
14	-40	2D	-15	46	10	5F	35	78	60	91	85
15	-39	2E	-14	47	11	60	36	79	61	92	86
16	-38	2F	-13	48	12	61	37	7A	62	93	87
17	-37	30	-12	49	13	62	38	7B	63	94	88
18	-36	31	-11	4A	14	63	39	7C	64	95	89
19	-35	32	-10	4B	15	64	40	7D	65	96	90
1A	-34	33	-9	4C	16	65	41	7E	66	-	-
1B	-33	34	-8	4D	17	66	42	7F	67	-	-
1C	-32	35	-7	4E	18	67	43	80	68	-	-
1D	-31	36	-6	4F	19	68	44	81	69	-	-
1E	-30	37	-5	50	20	69	45	82	70	-	-
1F	-29	38	-4	51	21	6A	46	83	71	-	-
20	-28	39	-3	52	22	6B	47	84	72	-	-
21	-27	3A	-2	53	23	6C	48	85	73	-	-
22	-26	3B	-1	54	24	6D	49	86	74	-	-
23	-25	3C	-0	55	25	6E	50	87	75	-	-
24	-24	3D	1	56	26	6F	51	88	76	-	-
25	-23	3E	2	57	27	70	52	89	77	-	-
26	-22	3F	3	58	28	71	53	8A	78	-	-
27	-21	40	4	59	29	72	54	8B	79	-	-

(11) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[2:0]	0	0	**0**	**0**	**1**	**0**	**0**	TC2	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

TC[2:0]	Temperature Compensation
000b	-0.00% per °C
100b (Default)	**-0.05% per °C**
101b	-0.10% per °C
110b	-0.15% per °C
111b	-0.20% per °C

(12) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC	0	0	**0**	**0**	**1**	**0**	**1**	**1**	**0**	PC

Set PC to program the build-in charge pump stages.

PC	Pump Control
0b	External V_{LCD}
1b (Default)	**Internal V_{LCD} (9x charge pump)**

When using external pump, setting PM is still necessary.

(13) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(double-byte command)	1	0	APC[R][7:0] register parameter							

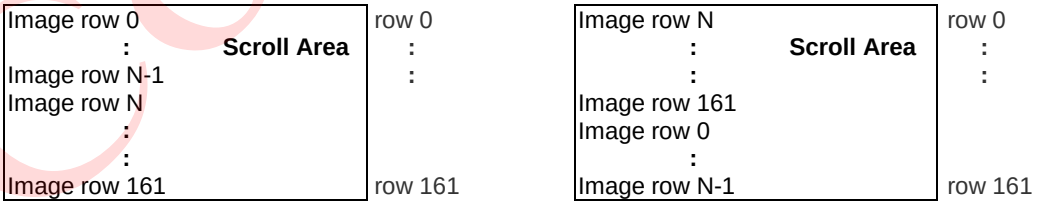
For UltraChip's use only. Please do NOT use.

(14) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line, SL[7:0]	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
	0	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 161.



(15) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA [4:0]	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
	0	0	**0**	**0**	**0**	PA4	PA3	PA2	PA1	PA0

Used in Host for RAM access. Possible value = **0**~21.

PA[4:0] : set Display Data RAM page address (Default: **0**)

PA=21: for ICON line.

(16) SET PM AT DIFFERENT TEMPERATURE WHEN TC[3]=1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TP[3:0], PM[7:0] (triple-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	**0**	**0**	**0**	**0**	TP3	TP2	TP1	TP0
	1	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

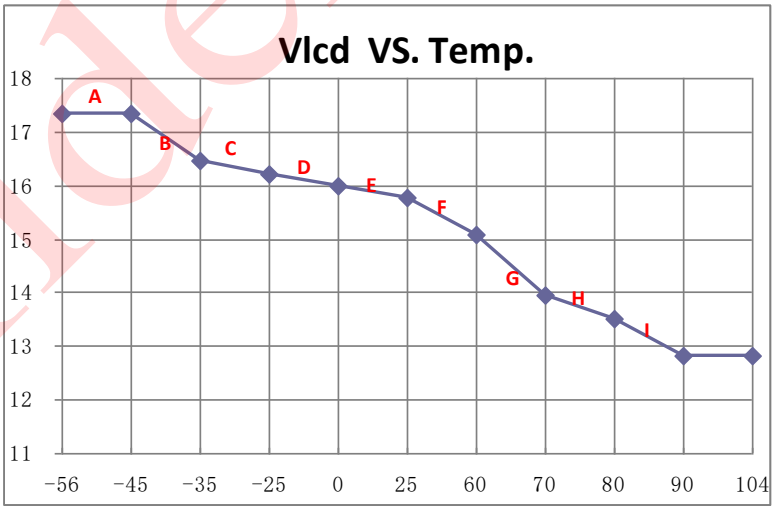
TP[3:0]: Select Temperature point. See Command (10) for setting.

0001b: Temp A 0010b: Temp B 0011b: Temp C 0100b: Temp D
0101b: Temp E 0110b: Temp F 0111b: Temp G 1000b: Temp H
1001b: Temp I

PM[7:0]: Program V_{BIAS} Potentiometer. See Command (17) for detail.

Example:

TP[3:0]	Temp. (°C)	PM[7:0]	PM
--	-56	--	210
TEMPA	-45	PMA	210
TEMPB	-35	PMB	170
TEMPC	-25	PMC	160
TEMPD	0	PMD	150
TEMPE	25	PME	140
TEMPF	60	PMF	110
TEMPG	70	PMG	60
TEMPH	80	PMH	40
TEMPI	90	PMI	10
--	104	--	10



(17) SET PM WHEN TC[3]=0

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set PM [7:0] (triple-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	1	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255** (Default: **54H**, that is 84 in decimal)

(18) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [3]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC3

This command is used to enable partial display function.

LC[3]	Partial Display function	Mux-Rate
0b (Default)	**Disabled**	= CEN+1+LC[0]x1 (DST, DEN not used.)
1b	Enabled	= DEN-DST+1+LC[0]x1

(19) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**1**	CSF

CSF	COM scan function
0b (Default)	**Interlace scan**
1b	Progressive Scan

(20) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increase by one.

AC[1]: Auto-Increment order
0 : column (CA) increase (+1) first until CA reaches CA boundary, then PA will increase by (+/-1).
1 : page (PA) increase (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2]: PID, Page Address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether Page Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and PA.

(21) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM. **(Default 0: OFF)**

(22) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM. **(Default 0: OFF)**

(23) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	LC2/MY	LC1/MX	LC0

This command is used for programming LC[2:0] for COM (page) mirror (MY), SEG (column) mirror (MX).

LC0 controls the Icon line's display ON or OFF. **(Default 1: ON)**

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 39-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data. **(Default 1: OFF)**

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image. **(Default 1: OFF)**

Display Data Direction	Function Setting			Image in Display Data Ram (Start : ●) (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	MY LC[2]	
Normal	0	0	0	
Y-mirror	0	0	1	
X-mirror	0	1	0	
X-mirror Y-mirror	0	1	1	

(24) SET N-LINE INVERSION

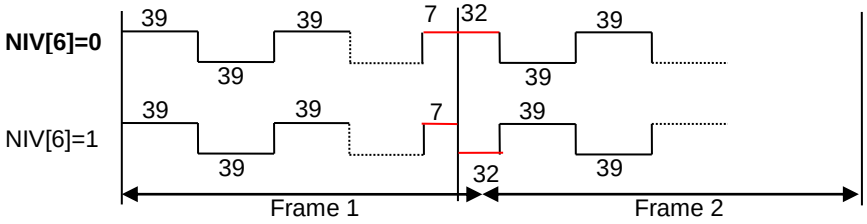
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-Line Inversion NIV [6:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(double-byte command)	1	0	**0**	NIV6	NIV5	NIV4	NIV3	NIV2	NIV1	NIV0

This command is used for programming NIV[6:0] for N-Line Inversion.

NIV[6]	Exclusive
0b (Default)	**no-XOR**
1b	XOR

NIV [5:0]	Inversion
00 0000b	**Disable Inversion Function**
00 0001b	Invert every 2 lines
:	:
11 1111b	Invert every 64 lines

Example:



(25) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [3:2]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**
(double-byte command)	1	0	**1**	**0**	**1**	**0**	**1**	**1**	**0**	DC2

DC[2]: Display ON/OFF (Default: **0: OFF**)

(26) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(27) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Test Control	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(double-byte command)	1	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(28) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [2:0]	0	0	**1**	**1**	**1**	**0**	**1**	BR2	BR1	BR0

Bias ratio definition:

000b = 6 001b = 10 010b = 11 **011b = 12 (Default)**
100b = 13 101b = 14

(29) RESET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update mode	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**

This command is used to reset cursor update mode function. It will clear cursor update mode flag (AC[3]=0), and CA will be restored to its previous value, which was stored in CR (via Set Cursor Update Mode command), and CA and PA increment will return to its normal condition.

(30) SET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Cursor Update mode	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**

Set Cursor Update mode is used to turn ON the Cursor Update mode function. AC[3] will be set to 1 and register CR will be set to the value of register CA.

When AC[3]=1, column address (CA) will only increase with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support “Read-Modify-Write” for cursor implementation.

(31) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(double-byte command)	1	0	CEN [7:0] register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-pages in the LCD. Default : **161**.

(32) SET PARTIAL DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(double-byte command)	1	0	DST [7:0] register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. Default value: **0**.

(33) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(double-byte command)	1	0	DEN [7:0] register parameter							

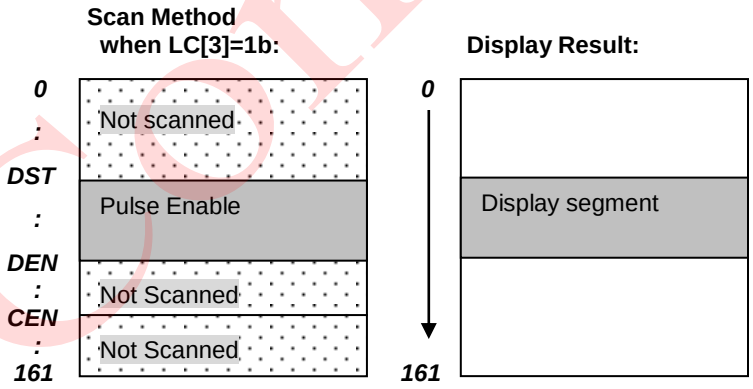
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. Default value: **161**.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[3]=1b (Partial Display enabled), the Mux-Rate is narrowed down to DEN-DST+1+LC[0]x1. When MUX rate is reduced, reduce the Frame rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted.

For minimum power consumption, set LC[3]=1b, set (DST, DEN, CEN) to minimize MUX rate, use slowest frame rate which satisfies the flicker requirement, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(34) SET OTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTPC (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	1	0	**0**	**0**	**0**	OTPC[4:0] register parameter				

This command is for OTP operation control:

OTPC[2:0] : OTP command

000 : Idle 001 : Normal Read
010 : Read for Program 011 : Program
1xx : For UltraChip use only.

OTPC[3] : OTP Enable, automatically cleared each time after OTP command is done. **Default: 0b**
OTPC[4] : Ignore/Use OTP. 0: Ignore **1: Use (Default)**

DC[2] and OTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all OTP operations will be blocked, and, when OTP operation is active, set DC[2] to 1 will be blocked.

(35) SET OTP WRITE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTPA (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	1	0	**0**	**0**	OTPA[5:0] register parameter					

This command enables Write to selected OTP bits. When OTPA=x, the x-th bit of the OTP memory will be programmed to “1”. Unprogrammed OTP bits will not be changed.

OTPA[5:0]: Set PMO bit address. **Default: 00H.**

This command is only valid when OTPC[3]=1.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1628c via registers CEN, DST, DEN, and partial display control LC[3].

UC1628c can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

BR = V_{LCD}/V_{BIAS},
where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux+1}$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=163), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to loose visibility.

UC1628c supports six (6) *BRs* as listed below. BR can be selected by software program.

BR	0	1	2	3	4	5
Bias Ratio	6	10	11	12	13	14

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Five (5) different temperature compensation coefficients can be selected via software. The 5 coefficients are given below:

TC	0	4	5	6	7
% per ^{o}C	-0.00	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[0].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

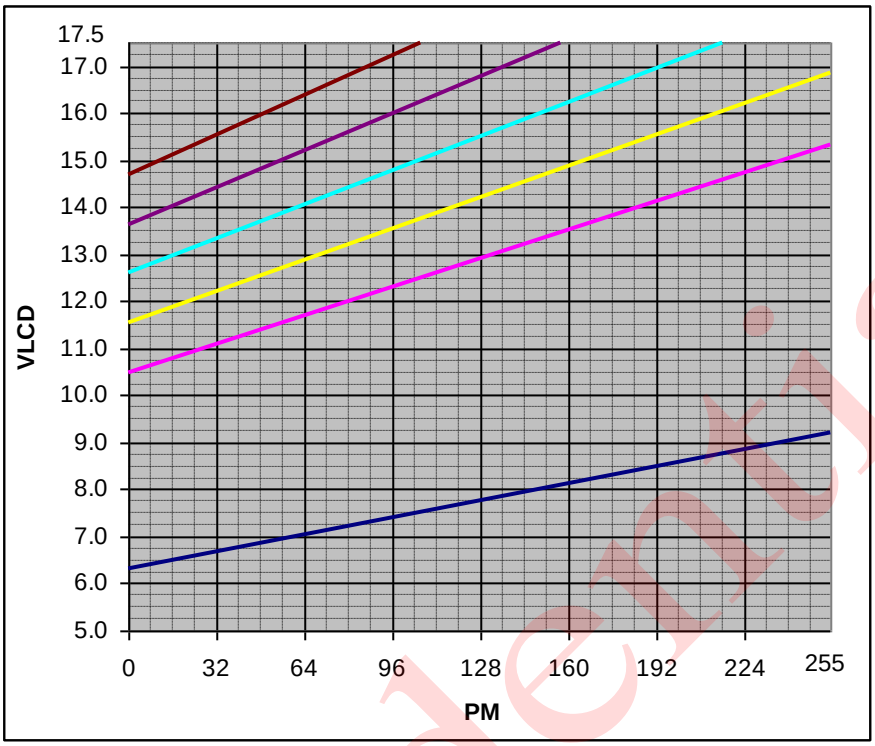
Gray shade LCD is sensitive to even a 1.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best results, software or OTP-based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1628c is designed to handle LCD panels with load capacitance up to ~15nF when V_{DD2} = 2.8V. 15nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels, use higher V_{DD}.

V_{LCD} QUICK REFERENCE



V_{LCD} Relationship to BR and PM at 25 °C

BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
6	6.347	11.346	0	6.35
			255	9.24
10	10.556	18.879	0	10.56
			255	15.37
11	11.601	20.764	0	11.60
			255	16.90
12	12.637	22.640	0	12.64
			215	17.50
13	13.682	24.522	0	13.68
			156	17.51
14	14.728	26.385	0	14.73
			106	17.52

Note:

1. For good product reliability, keep $V_{LCD(MAX)}$ under **17.52V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

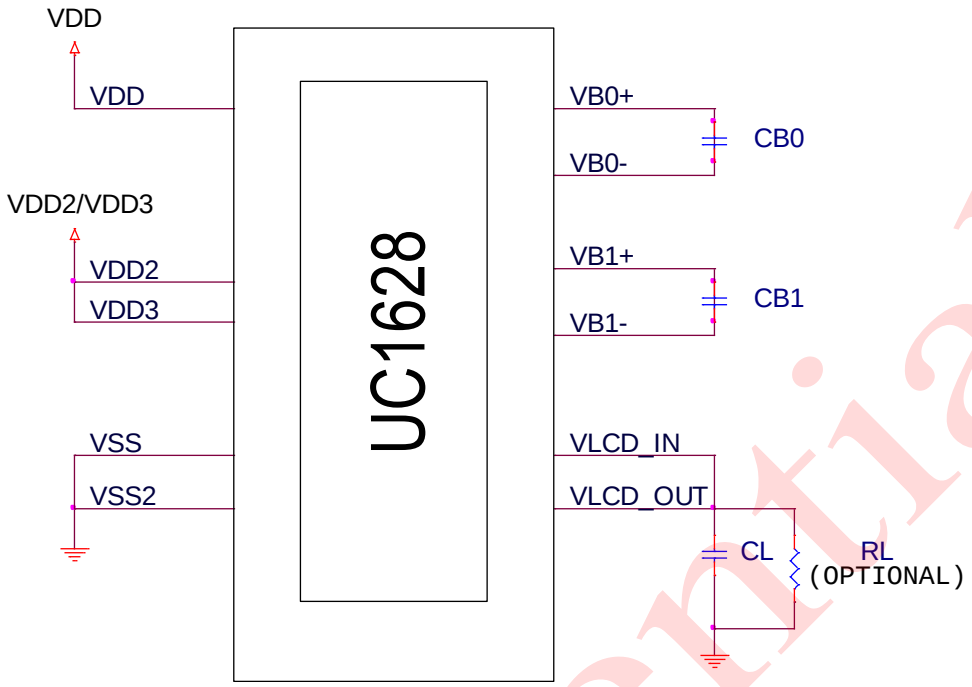


FIGURE 1.a: Reference circuit using INTERNAL Hi-V generator circuit

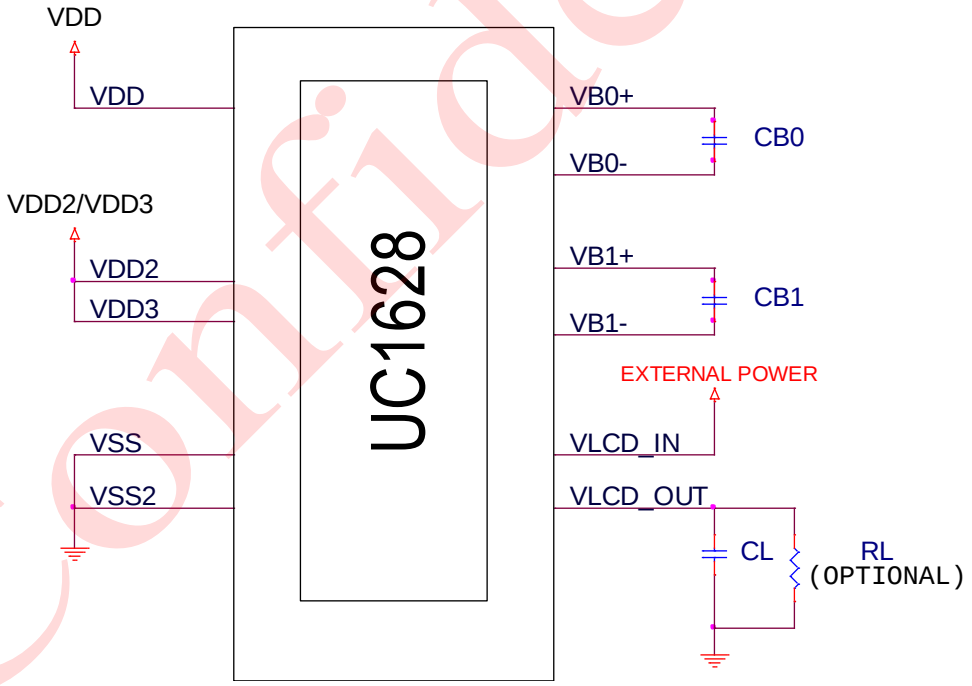


FIGURE 1.b: Reference circuit using EXTERNAL Hi-V generator circuit

Sample component values:

- C_{BX}: For panels of 3-inch or smaller, use 2.2uF (25V) capacitor;
  For panels bigger than 3 inches, use 5μF (25V) capacitor or higher.
  (Capacitor size depends on panel capacitance loading and actual image performance.)
- C_L: 330nF (25V) is appropriate for most applications.
- R_L: Around 10M Ω, to act as a draining circuit when V_{DD} is shut down abruptly.

Note:
The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1628c contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

32 different frame rates are provided for system design flexibility. The frame rate is controlled by register FR[4:0]. When Mux-Rate is above 109, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 109, 82, 55 and 41, frame rate will be scaled down by 1.5, 2, 3 and 4 times automatically to reduce power consumption.

When fast LC material with ($tr + tf$) < 160mS is used, faster frame rate may be required to maintain good contrast ratio at operating temperature >50ºC.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM or SEG drivers are in idle mode, their respective outputs are shorted to Vss.

DRIVER ARRANGEMENTS

The naming convention is: COM(x), where x=1~162, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CSF, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1628c will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1628c will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

SL register is used to implement scroll function.

PARTIAL DISPLAY

UC1628c provides flexible control of Mux Rate and active display area. Please refer to related Command Description for more detail.

ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1628c can be as short as 30μS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize V_{DD}, V_{SS} noise, and ensure sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

COM TRACE

Excessive RC decay of COM scanning pulse can cause fluctuation of contrast and increase the crosstalk of COM direction.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 1.8\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} – RC_{MIN} | < 0.44\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

SEG TRACE

Excessive RC decay of SEG signal can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.5\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD}/#_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10}) / V_{10} = (V_{ON}-V_{OFF}) / V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics. V90 and V10 refers to the applied voltage required to achieve 90% and 10% of the ultimate transmission at saturating voltages respectively.

And V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/160	1/12	7.93%	6.3%	5.7%
1/160	1/11	7.77%	6.2%	5.6%

HOST INTERFACE

As summarized in the table below, UC1628c supports 2 parallel bus protocols in 8-bit bus width, and 2 serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type			
		Parallel		Serial	
		8080	6800	S8 (4-wire)	I^2C (2-wire)
Width		8-bit	8-bit	–	
Access		Read (data and status) / Write			Write
Control & Data Pins	BM[1:0]	10	11	01	00
	CS[1:0]	Chip Select			A[3:2]
	CD	Control/ Data			0
	WR0	$\overline{WR}$	R/ $\overline{W}$	0	
	WR1	$\overline{RD}$	EN	0	
	DB[7:6]	Data	Data	–	
	DB[5:4]	Data	Data	SDAO	
	DB[3]	Data	Data	SDAI	
	DB[2:1]	Data	Data	–	
	DB[0]	Data	Data	SCK	

* Connect unused control pins and data bus pins to V_{SS}.

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1628c internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, by either `Set CA`, or `Set PA` command.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT BUS OPERATION

UC1628c supports 8-bit bus width.

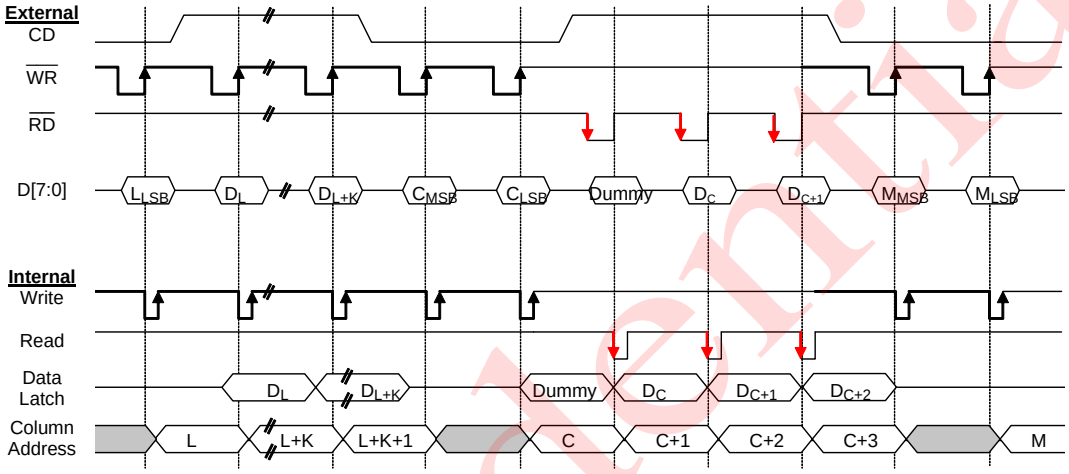


FIGURE 3: 8-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1628c supports 2 serial modes, a 4-wire SPI mode (S8), and a 2-wire SPI mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Read status and write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

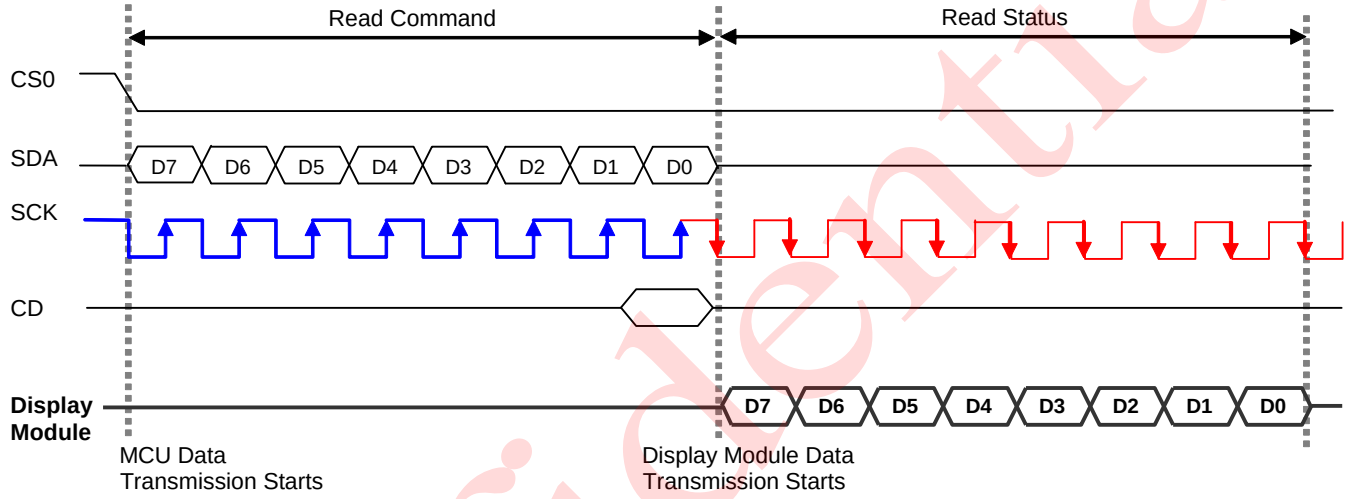


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

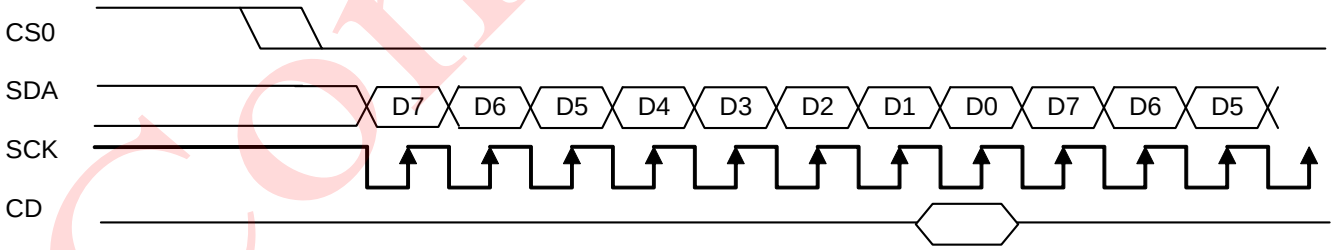


FIGURE 4.b: 4-wire Serial Interface (S8) – Write

2-WIRE SERIAL INTERFACE (I²C)

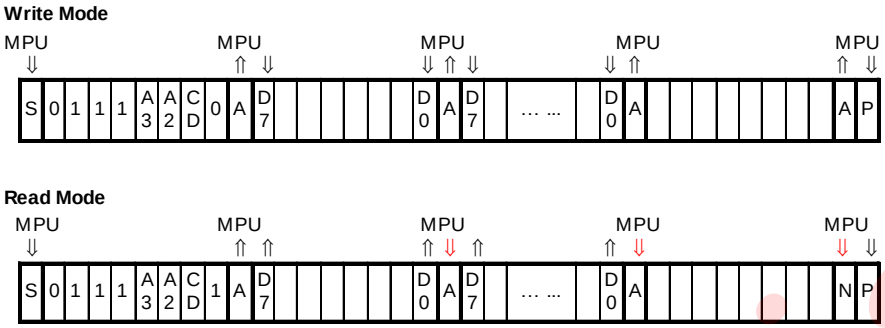


FIGURE 6: 2-wire Serial Interface (I2C)

When BM[1:0] is set to "LL", UC1628c is configured as a I²C Bus signaling protocol compliant slave device. Please refer to I²C standard for details of the bus signaling protocol. Please refer to AC Characteristic section for timing parameters of UltraChip's implementation.

In this mode, pins CS[1:0] become A[3:2] and are used to configure UC1628c's device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I²C mode.

Each UC1628c's I²C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I²C mode and should be connected to V_{SS}.

The direction (read or write) and the content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1628c will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either MCU or UC1628c) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the MCU.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.

HOST INTERFACE REFERENCE CIRCUIT

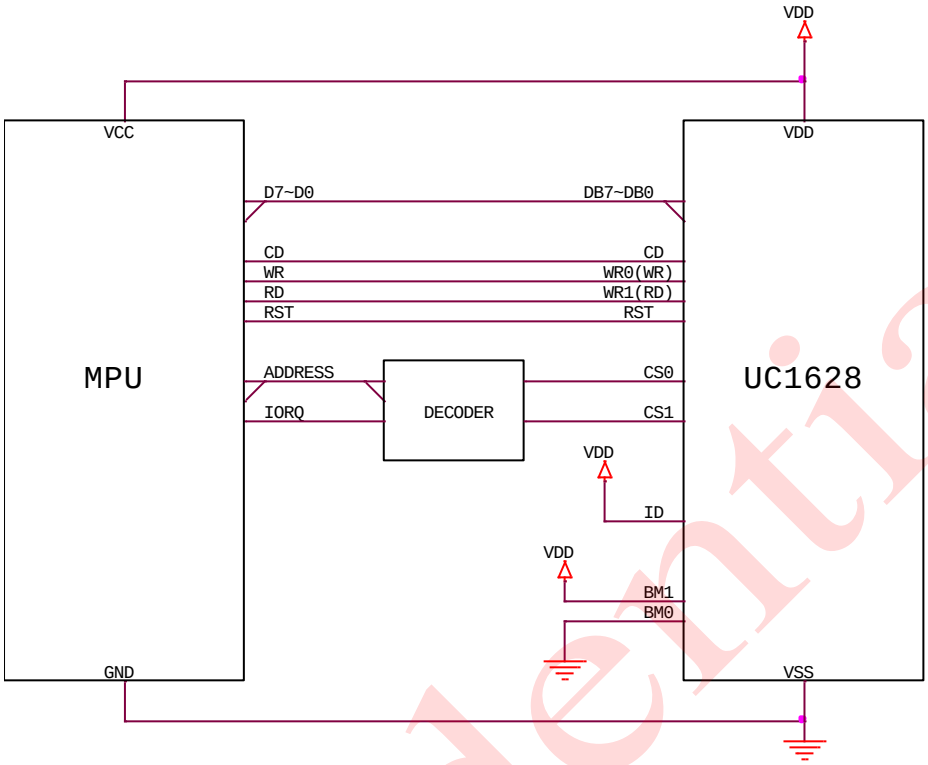


FIGURE 7: 8080/8-bit parallel mode reference circuit

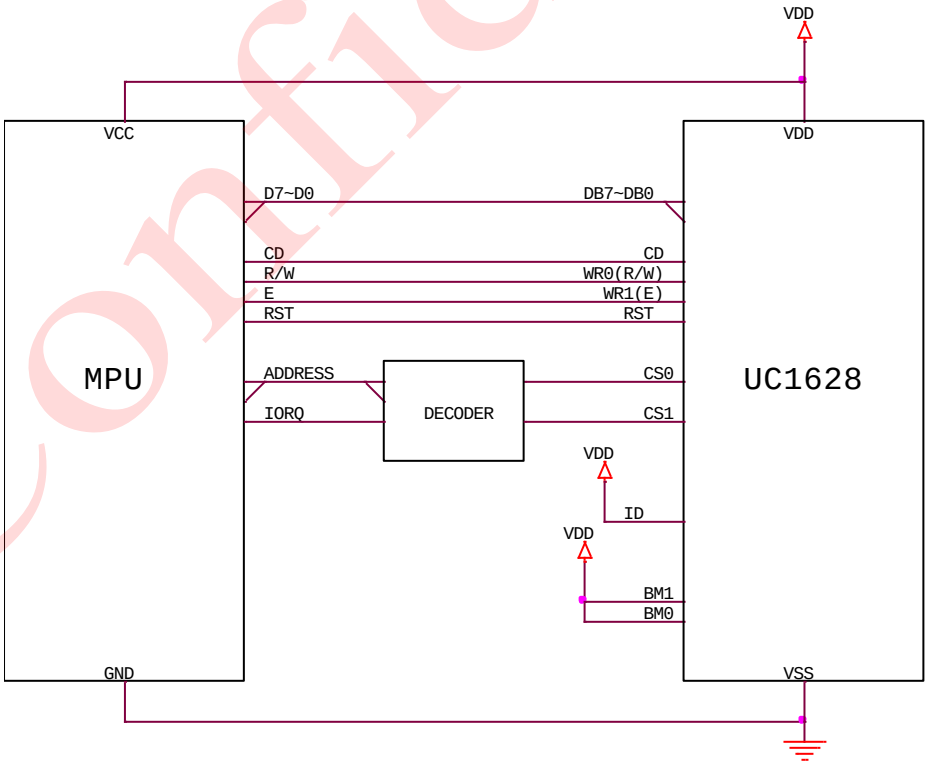


FIGURE 8: 6800/8-bit parallel mode reference circuit

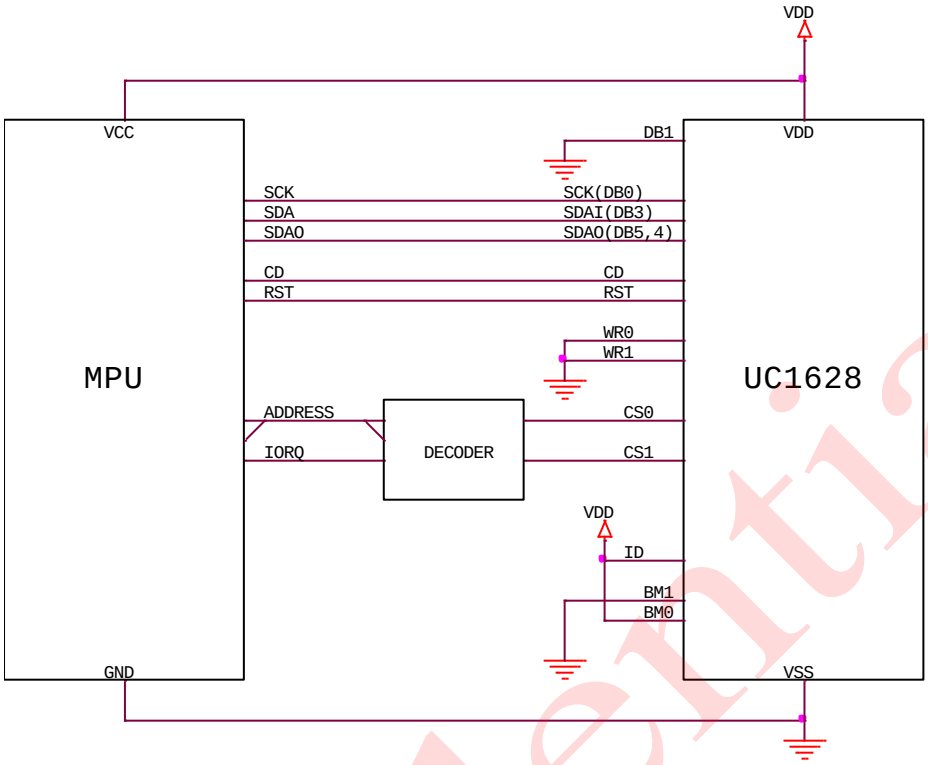


FIGURE 9: 4-Wire SPI (S8) serial mode reference circuit

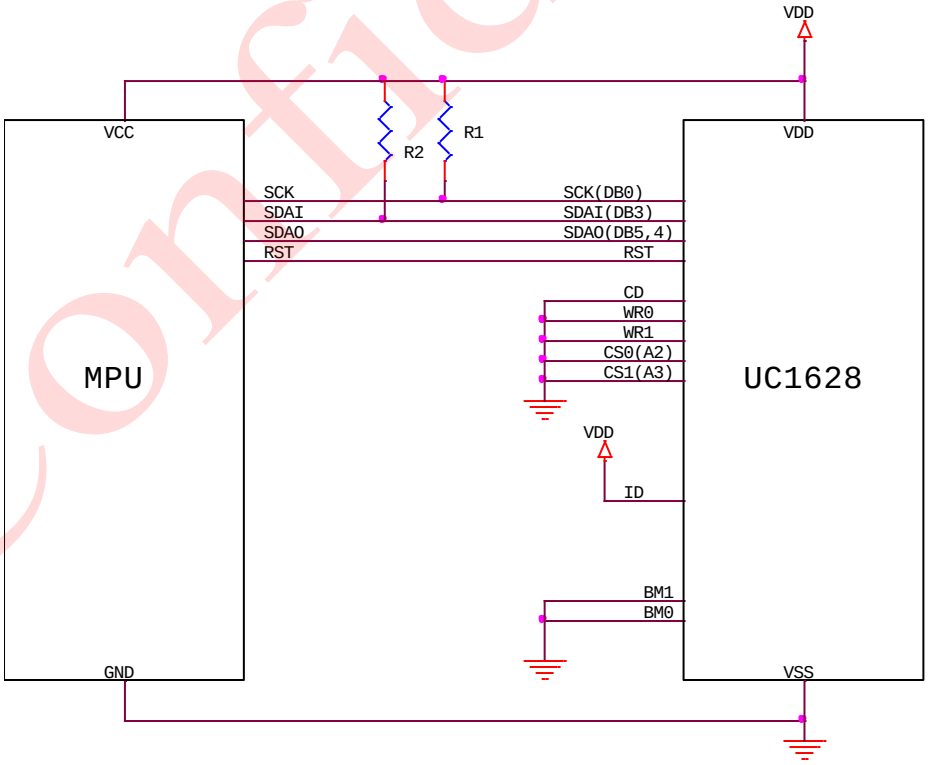


FIGURE 11: 2-Wire SPI (I^2C) serial mode reference circuit

Note:

1. When using Read function:

(8080) Set WR1=0 (6800) Set WR1=1 → data output will be enabled. (Serial) Set SCK=0	(8080) Set WR1=1 (6800) Set WR1=0 → data output will be disabled. (Serial) Set SCK=1

2. It is REQUIRED to set MPU's data port to 1 before Data Read or Status Read actions.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 163x256.

After setting CA and PA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and page data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing `Set Page Address` and `Set Page_C Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (255), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of row, CA will be reset to 0 and PA will increase or decrease, depending on the setting of row Increment Direction (PID, AC[2]), and when PA reaches the boundary of RAM (i.e. PA = 0 or 20), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (255–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*, 162)

Where Mod is the modular operator and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line* reaches *162*. Effects such as row scrolling, row swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX-1*, *162*)
where MUX = CEN + 1

Otherwise
Line = Mod (*Line*, *162*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

Data	Line Addr
D0	00H
D1	01H
D2	02H
D3	03H
D4	04H
D5	05H
D6	06H
D7	07H
D0	08H
D1	09H
D2	0AH
D3	0BH
D4	0CH
D5	0DH
D6	0EH
D7	0FH
…	…
D0	A0H
D1	A1H
D0	A0H

RAM

1	0							Page0									
1	0																
0	1																
1	1																
1	0																
0	1																
0	1																
0	0																
								Page1									
								…									
								Page20									
								Page21									

	MY=0		MY=1	
	SL=0	SL=8	SL=0	SL=8
	R1	R155	R162	R8
	R2	R156	R161	R7
	R3	R157	R160	R6
	R4	R158	R159	R5
	R5	R159	R158	R4
	R6	R160	R157	R3
	R7	R161	R156	R2
	R8	R162	R155	R1
	R9	R1	R154	R162
	R10	R2	R153	R161
	R11	R3	R152	R160
	R12	R4	R151	R159
	R13	R5	R150	R158
	R14	R6	R149	R157
	R15	R7	R148	R156
	R16	R8	R147	R155
	…	…	…	…
	R161	R153	R2	R10
	R162	R154	R1	R9
	ICON	ICON	ICON	ICON
			MUX=16	

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8					SEG253	SEG254	SEG255	SEG256
MX=1	SEG256	SEG255	SEG254	SEG253	SEG252	SEG251	SEG250	SEG249					SEG4	SEG3	SEG2	SEG1

Example: When MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown are:

For 8-bit bus width:

Page0, SEG1: D[7:0] : 00011011b
Page0, SEG2: D[7:0] : 01101100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1628c has two different types of Reset:

Power-ON-Reset and *Pin-Reset*

Power-ON-Reset is performed right after V_{DD} is connected to power.

Pin Reset can also be activated by connecting the RST pin to ground.

In the following discussions, Reset means *Pin Reset*.

RESET STATUS

When UC1628c enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1628c has three operating modes:
Reset, Sleep, and Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
Host Interface	Disabled	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, *Set Display Enable* will initiate Operation Mode transitions.

When DC[2] is modified by *Set Display Enable*, Operation Mode will be updated automatically. There is no other action required to enter Sleep mode.

The Operation Mode changes are synchronized with the edges of UC1628c's internal clock. To ensure consistent system states, wait at least 10μS after issuing the `Set Display Enable` command.

Action	Mode
RST_ pin pulled "L" Power ON reset	Reset
Set Driver Enable to "0"	Sleep
Set Driver Enable to "1"	Normal

Table 5: Mode changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1628c consumes very little energy in Sleep mode (typically under 5μA).

EXITING SLEEP MODE

UC1628c contains internal logic to check whether V_{LCD} and V_D are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1628c's internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

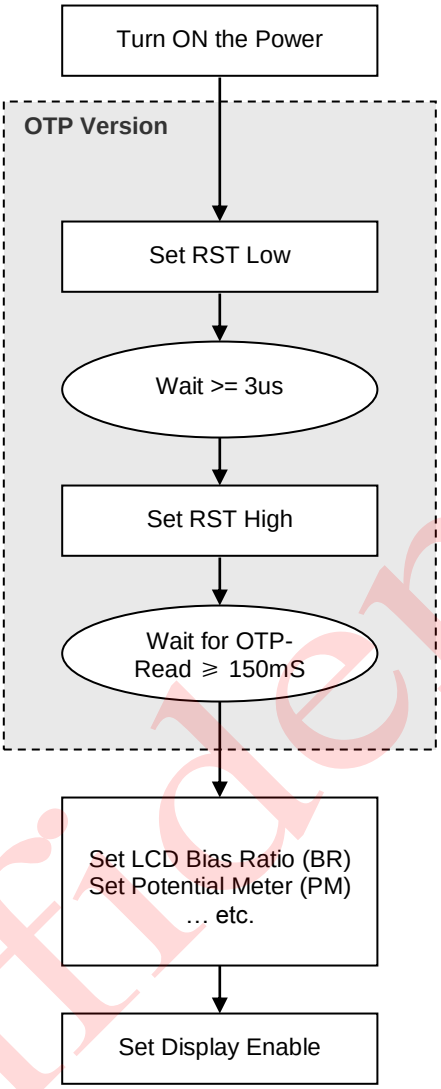


Figure 12: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned on first:

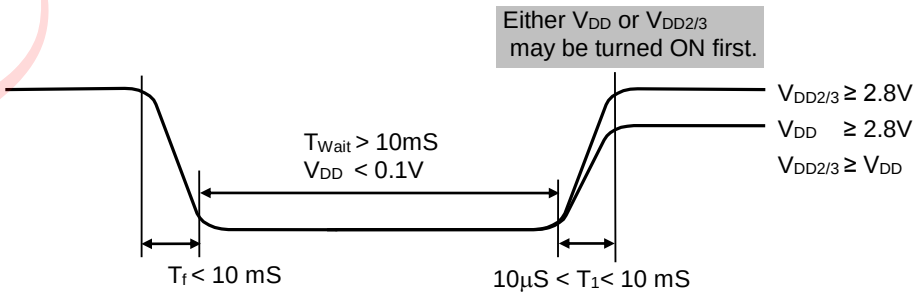


Figure 13: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1628c enters Sleep mode from Display mode by issuing Set Display Disable command.

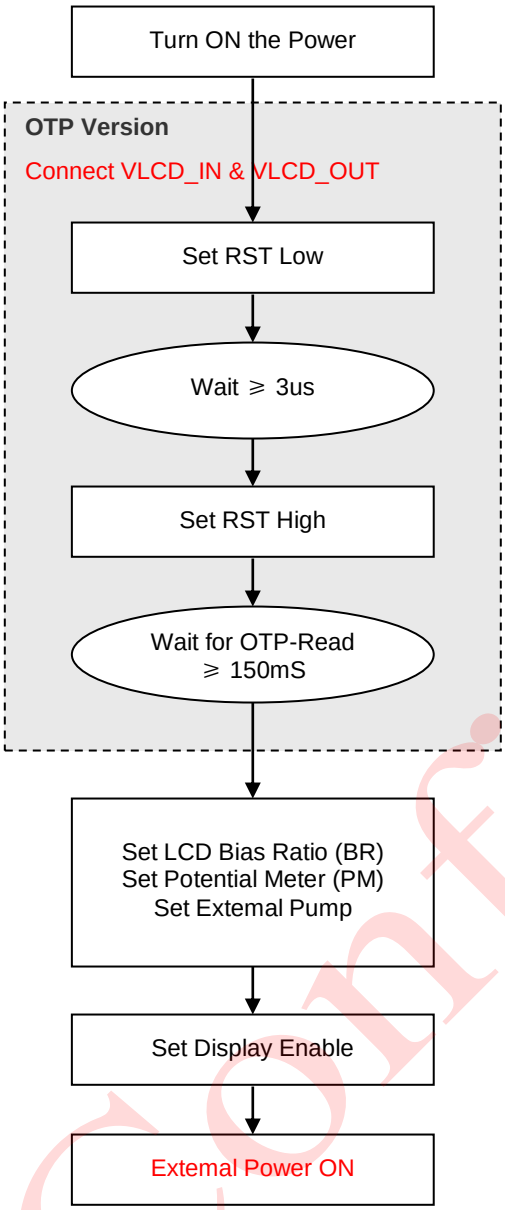


FIGURE 14: Reference Enter/Exit Sleep Mode Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

When internal V_{LCD} is not used, UC1628c will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

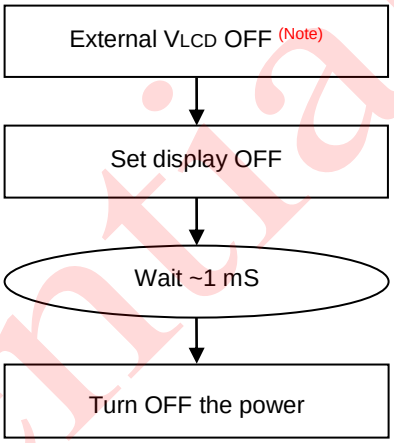


FIGURE 15: Reference Power-Down Sequence

Note: When using internal pump, ignore the "External V_{LCD} OFF" step.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type
- Required: These items are required
- Customized: These items are not necessary if customer parameters are the same as default
- Advanced: We recommend new users to skip these commands and use default values.
- Optional: These commands depend on what users want to do.

C/D — The type of the interface cycle. It can be either Command (0) or Data (1)

W/R — The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Wait ⩽ 3mS	
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 5mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS after RST is High.
C	0	0	0	0	1	0	0	#	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	1	Set LCD Mapping	
A	0	0	0	0	1	0	1	1	0	1	Set Pump Control	
C	0	0	1	1	1	0	1	#	#	#	Set Bias Ratio	LCD specific operating voltage setting
R	0	0	1	0	0	0	0	0	0	1	Set V_{BIAS} Potentiometer	
	0	0	0	0	0	0	0	0	0	0		
	1	0	#	#	#	#	#	#	#	#		
O	0	0	0	0	0	0	0	0	0	1	Write display RAM	Set up display image
	1	0	#	#	#	#	#	#	#	#		
	.	.	.	.	.	.	.	.	.	.		
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	1	0	0	1	0	0	1	Set Display Enable	
	1	0	1	0	1	0	1	1	0	1		

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	0	0	1	0	0	1	Set Display OFF	
	1	0	1	0	1	0	1	1	0	0		
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	0	0	1	0	0	1	Set DisplayOFF	
	1	0	1	0	1	0	1	1	0	0		
C	0	0	0	0	0	0	0	0	0	1	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
	1	0	#	#	#	#	#	#	#	#		
	.	.	.	.	.	.	.	.	.	.		
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	1	0	0	1	0	0	1	Set Display Enable	
	1	0	1	0	1	0	1	1	0	1		

OTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for OTP Program operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

OTP operations (Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type
- Required: These items are required
- Customized: These items are not necessary if customer parameters are the same as default
- Advanced: We recommend new users to skip these commands and use default values.
- Optional: These commands depend on what users want to do.

C/D: The type of the interface cycle. It can be either Command (0) or Data (1)

W/R: The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) OTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	-	-	-	-	-	-	-	-	-	-	Set RST pin Low	Wait 5 mS after RST is Low
R	-	-	-	-	-	-	-	-	-	-	Set RST pin High	
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON Reset	Wait ~150mS
R	0	0	0	0	0	1	0	1	1	0	Set Frame Rate	Set FR[4:0]=01101b
	1	0	0	0	0	0	0	0	0	0		
	1	0	0	0	0	0	1	1	0	1		
												Add TST4 voltage (8V)
R	0	0	1	0	1	1	1	0	0	1	Set OTP Write Address	Set OTP Write Address
	1	0	0	0	0	0	0	0	0	0		OTPA[5:0]:00H
R	0	0	1	0	1	1	1	0	0	0	Set OTP Program	Set OTP Program enable
	1	0	0	0	0	1	1	0	1	1		OTPC[4:0]:1BH
												Wait ~150mS
R	0	0	1	0	1	1	1	0	0	0	Set OTP Program	Set OTP Program leave
	1	0	0	0	0	1	1	0	0	0		OTPC[4:0]:18H
												Leave TST4 voltage
R	0	0	1	0	1	1	1	0	0	0	Set OTP Program	Set OTP Program Read
	1	0	0	0	0	1	1	0	1	0		OTPC[4:0]:1AH
												Wait ~20mS
R	0	0	0	0	0	0	0	0	1	1	Get Status	Check OTP Status until OP=0, OE=1, OD=1
	1	1	-	-	-	-	-	OD	OE	OP		
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.
* Leave TST4 floating if not under programming situation.

(2) OTP read Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	-	-	-	-	-	-	-	-	-	-	Set RST pin Low	Wait 5 mS after RST is Low
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON Reset	Wait ~150mS
R	0	0	1	0	1	1	1	0	0	0	Set OTP Program	Set OTP Program Read
	1	0	0	0	0	1	1	0	1	0		OTPC[4:0]:1AH
												Wait ~20mS
R	0	0	0	0	0	0	0	0	1	1	Get Status	Check OTP Status until OP=0, OE=1 OD=1
	1	1	-	-	-	-	-	OD	OE	OP		
R												

* It is recommended that users read fist all the bits to be programmed.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1 and 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Generated voltage (-40^{O}C ~ +85^{O}C)	-0.3	+18	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-45	+90	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damage to the device. These are stress rating only. This device should be operated under DC/AC characteristics condition for normal operation. Exposure to over the DC/AC characteristics conditions for extended periods may affect device reliability and function operation.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.7	2.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.7	2.8~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.7V, 25^{O}C	6.35	14.5	17.52	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.7V, 25^{O}C	1.05		1.53	V
V_{IL}	Input logic LOW				0.2V_{DD}	V
V_{IH}	Input logic HIGH		0.8V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD}	V
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current	V_{IN} = V_{DD} or V_{SS}			1.5	μA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85 ºC			10	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 17.49V		1	2	kΩ
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 17.49V		1	2	kΩ
f_{FRAME}	Average Frame rate	FR[4:0] = 01101b	-10%	81.9	+10%	Hz

POWER CONSUMPTION

V_{DD} = 2.7 V, Bias Ratio = 011b , PM = 84,
V_{LCD} = 14.51 V, Frame Rate = 81.9 Hz, Mux Rate = 163
Bus mode = 6800, C_L =330 nF, C_B = 2.2 μF,
Temperature = 25ºC, All HV outputs are open circuit.

Display Pattern	Conditions	Typical	Maximum	Unit
All-OFF	Bus = idle	540	810	μA
All-ON	Bus = idle	545	817	μA
2-pixel checker	Bus = idle	770	1150	μA
-	Reset (standby current)	< 3	5	μA

AC CHARACTERISTICS

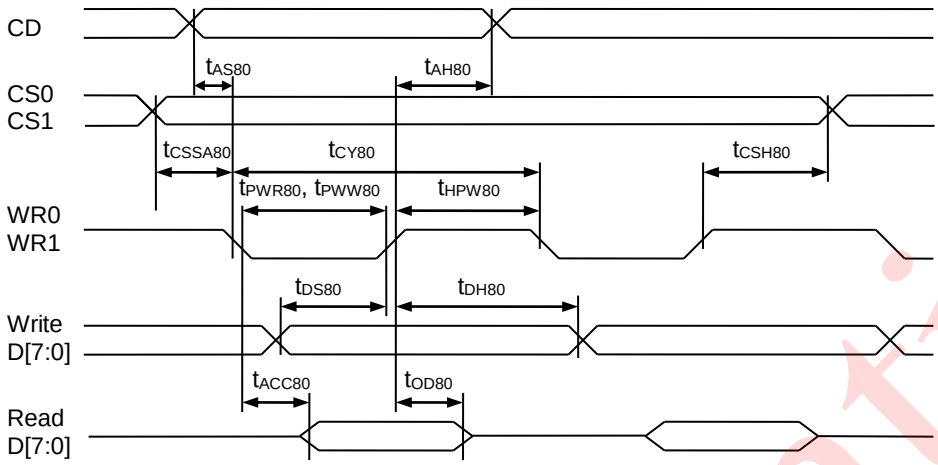


FIGURE 16: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –45 to +90°C)				(read / write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY80}	WR0, WR1	System cycle time		430 / 280	–	nS
t_{PWR80}		Pulse width		200 / --		
t_{PWW80}		Pulse width		-- / 125		
t_{HPW80}		High pulse width		200 / 125		
t_{DS80} t_{DH80}	Write D7~D0	Data setup time Data hold time		-- / 45 -- / 10	–	nS
t_{ACC80} t_{OD80}	Read D7~D0	Read access time Output disable time	C_L = 100pF	– / -- 100 / --	200 –	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

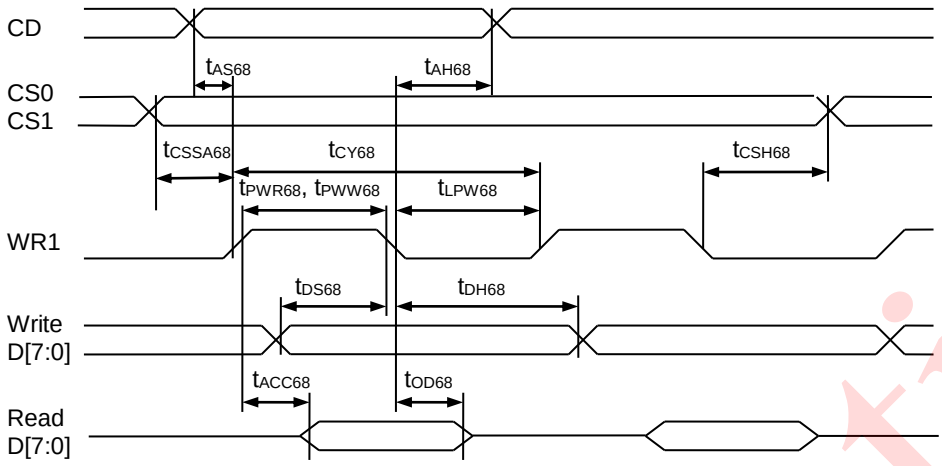


FIGURE 17: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –45 to +90°C)				(read / write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY68}	WR0, WR1	System cycle time		430 / 280	–	nS
t_{PWR68}		Pulse width		200 / –-		
t_{PWW68}		Pulse width		–- / 125		
t_{LPW68}		High pulse width		200 / 125		
t_{DS68} t_{DH68}	Write D7~D0	Data setup time Data hold time		-- / 45 -- / 10	–	nS
t_{ACC68} t_{OD68}	Read D7~D0	Read access time Output disable time	C_L = 100pF	– / -- 100 / --	200 –	nS

Note: tr (rising time), tf (falling time) : ⩽ 15nS

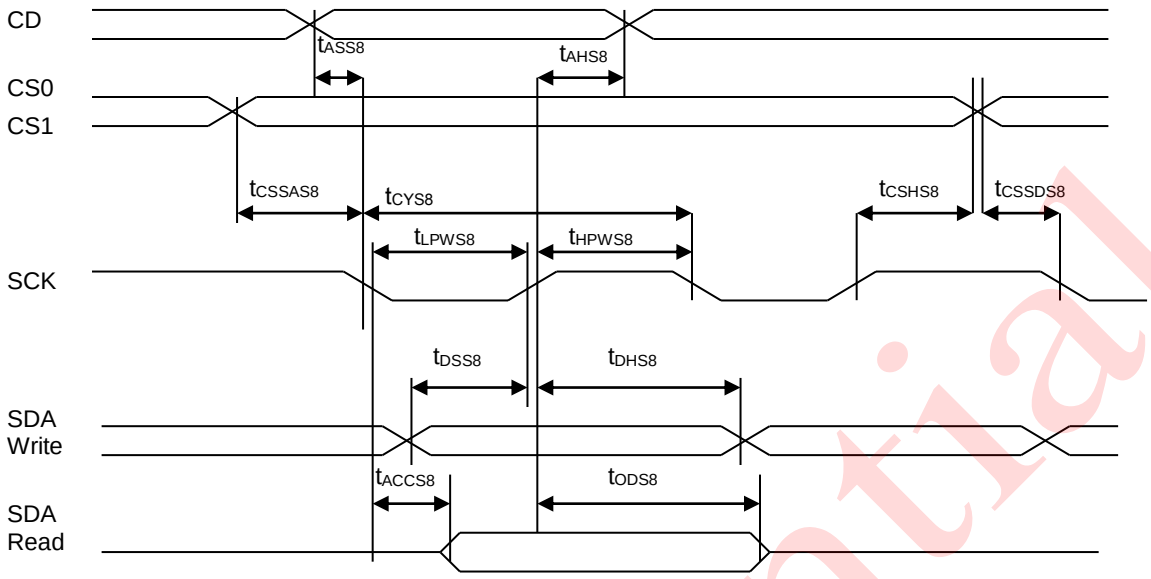


FIGURE 18: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –45 to +90°C)				(read / write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		15		
t_{CSSAS8}	CS1/CS0	Chip select setup time		5	–	nS
t_{CSHS8}		Chip select hold time		15		
t_{CYS8}	SCK	System cycle time		430 / 220	–	nS
t_{LPWS8}		Low pulse width		200 / 95		
t_{HPWS8}		High pulse width		200 / 95		
t_{DSS8}	SDA (Write)	Data setup time		-- / 25	–	nS
t_{DHS8}		Data hold time		-- / 15		
t_{ACCS8}	SDA (Read)	Read access time	C_L = 100pF	– / --	200	nS
t_{ODS8}		Output disable time		30 / --	–	

Note: tr (rising time), tf (falling time) : ⩽ 15nS

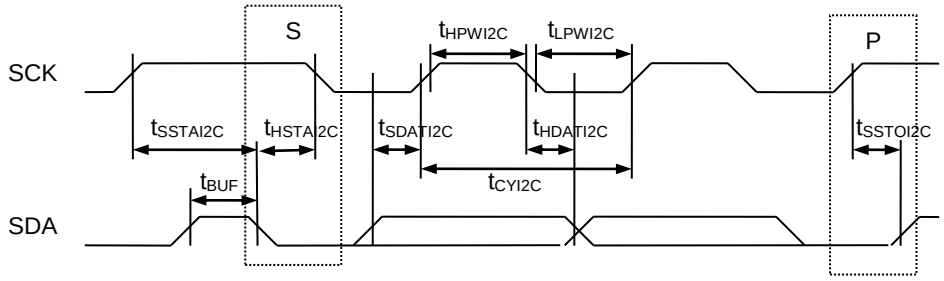


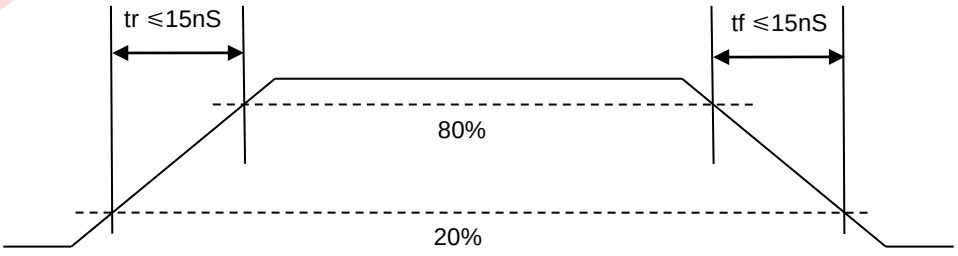
FIGURE 20: Serial Bus Timing Characteristics (for I^2C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –45 to +90°C)				(Read / Write)		
t_{CYI2C}	SCK	SCK cycle time		530 / 230	–	nS
t_{LPWI2C}		Low pulse width		250 / 100	–	nS
t_{HPWI2C}		High pulse width		250 / 100	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		55	–	nS
t_{HDAI2C}		Data hold time		10	–	nS
$t_{SSTAI2C}$		START Setup time		10	–	nS
$t_{HSTAI2C}$		START Hold time		55	–	nS
$t_{SSTOI2C}$		STOP setup time		10	–	nS
t_{BUF}		Bus Free time between STOP and START condition		75	–	nS

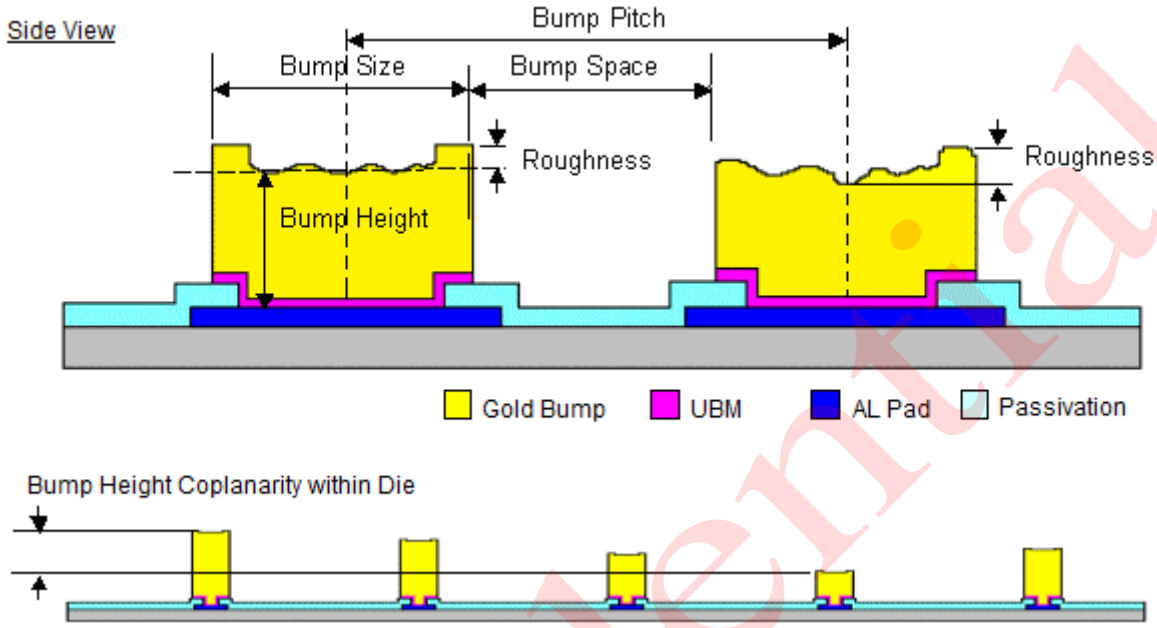
Note: tr (rising time), tf (falling time) : ⩽ 15nS

Note:

For each mode, the signal's rising and falling times (tr, tf) are stipulated to be equal to or less than 15nS each.



PHYSICAL DIMENSIONS

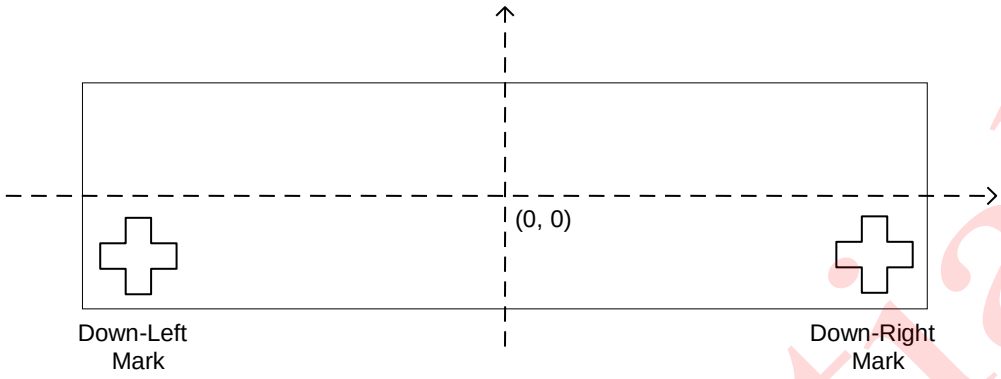


Die / Bump Information:

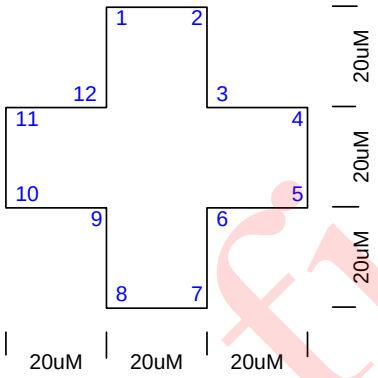
Die Size:	(9066µM ± 40µM) x (861µM ± 40µM)
Die Thickness:	300µM ± 20µM
Die TTV:	$D_{MAX} - D_{MIN} \leqslant 2\mu M$
Bump Height:	10µM ± 3µM (Part number: UC1628cGAA)
	15µM ± 3µM (Part number: UC1628cGBA)
	$H_{MAX} - H_{MIN} \leqslant 2\mu M$
Bump Size:	11.2µM x 134µM ± 2µM
Bump Pitch:	23.2µM
Bump Space:	12µM ± 3µM
Hardness:	90Hv ± 25Hv
Shear force:	$\geqslant$ 5g/mil^2
Bump Area:	1500.8µM^2
Coordinate origin:	(0, 0)
Chip center:	(0, 0)
Pad reference:	Pad center

ALIGNMENT MARK INFORMATION

LOCATION OF THE ALIGNMENT MARK:



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment marks are on Top Metal and under Passivation.

The "+" mark is symmetric both horizontally and vertically.

COORDINATES:

	Down-Left Mark		Down-Right Mark	
	X	Y	X	Y
1	-4113	-326.5	4093	-326.5
2	-4093	-326.5	4113	-326.5
3	-4093	-346.5	4113	-346.5
4	-4073	-346.5	4133	-346.5
5	-4073	-366.5	4133	-366.5
6	-4093	-366.5	4113	-366.5
7	-4093	-386.5	4113	-386.5
8	-4113	-386.5	4093	-386.5
9	-4113	-366.5	4093	-366.5
10	-4133	-366.5	4073	-366.5
11	-4133	-346.5	4073	-346.5
12	-4113	-346.5	4093	-346.5

PAD COORDINATES

No.	Pad	X	Y	W	H
1	DUMMY1	-4404.9	334.8	134	11.2
2	COM_pad<95>	-4404.9	311.6	134	11.2
3	COM_pad<97>	-4404.9	288.4	134	11.2
4	COM_pad<99>	-4404.9	265.2	134	11.2
5	COM_pad<101>	-4404.9	242	134	11.2
6	COM_pad<103>	-4404.9	218.8	134	11.2
7	COM_pad<105>	-4404.9	195.6	134	11.2
8	COM_pad<107>	-4404.9	172.4	134	11.2
9	COM_pad<109>	-4404.9	149.2	134	11.2
10	COM_pad<111>	-4404.9	126	134	11.2
11	COM_pad<113>	-4404.9	102.8	134	11.2
12	COM_pad<115>	-4404.9	79.6	134	11.2
13	COM_pad<117>	-4404.9	56.4	134	11.2
14	COM_pad<119>	-4404.9	33.2	134	11.2
15	COM_pad<121>	-4404.9	10	134	11.2
16	COM_pad<123>	-4404.9	-13.2	134	11.2
17	COM_pad<125>	-4404.9	-36.4	134	11.2
18	COM_pad<127>	-4404.9	-59.6	134	11.2
19	COM_pad<129>	-4404.9	-82.8	134	11.2
20	COM_pad<131>	-4404.9	-106	134	11.2
21	COM_pad<133>	-4404.9	-129.2	134	11.2
22	COM_pad<135>	-4404.9	-152.4	134	11.2
23	COM_pad<137>	-4404.9	-175.6	134	11.2
24	COM_pad<139>	-4404.9	-198.8	134	11.2
25	COM_pad<141>	-4404.9	-222	134	11.2
26	COM_pad<143>	-4404.9	-245.2	134	11.2
27	COM_pad<145>	-4404.9	-268.4	134	11.2
28	COM_pad<147>	-4404.9	-291.6	134	11.2
29	COM_pad<149>	-4404.9	-314.8	134	11.2
30	COM_pad<151>	-4404.9	-338	134	11.2
31	COM_pad<153>	-4404.9	-361.2	134	11.2
32	DUMMY2	-4404.9	-384.4	134	11.2
33	COM_pad<155>	-4237.8	-293.5	11.2	134
34	COM_pad<157>	-4214.6	-293.5	11.2	134
35	COM_pad<159>	-4191.4	-293.5	11.2	134
36	COM_pad<161>	-4168.2	-293.5	11.2	134
37	TST4_pad	-3869.7	-351	45	82
38	TST4_pad	-3809.7	-351	45	82
39	TST4_pad	-3749.7	-351	45	82
40	DATA_pad<7>	-3676.2	-351	45	82
41	DATA_pad<7>	-3616.2	-351	45	82
42	VSSX	-3556.2	-351	45	82
43	DATA_pad<6>	-3496.2	-351	45	82
44	DATA_pad<6>	-3436.2	-351	45	82
45	DATA_pad<5>	-3376.2	-351	45	82
46	DATA_pad<5>	-3316.2	-351	45	82
47	DATA_pad<4>	-3248.6	-351	45	82
48	DATA_pad<4>	-3188.6	-351	45	82
49	DATA_pad<3>	-3128.6	-351	45	82
50	DATA_pad<3>	-3068.6	-351	45	82
51	DATA_pad<2>	-3001	-351	45	82
52	DATA_pad<2>	-2941	-351	45	82
53	VSSX	-2881	-351	45	82
54	DATA_pad<1>	-2821	-351	45	82
55	DATA_pad<1>	-2761	-351	45	82
56	DATA_pad<0>	-2693.4	-351	45	82
57	DATA_pad<0>	-2633.4	-351	45	82

No.	Pad	X	Y	W	H
58	RST_pad	-2559.5	-351	45	82
59	RST_pad	-2499.5	-351	45	82
60	VSSX	-2439.5	-351	45	82
61	CS_pad<0>	-2379.5	-351	45	82
62	CS_pad<0>	-2319.5	-351	45	82
63	CS_pad<1>	-2259.5	-351	45	82
64	CS_pad<1>	-2199.5	-351	45	82
65	VSSX	-2139.5	-351	45	82
66	CD_pad	-2079.5	-351	45	82
67	CD_pad	-2019.5	-351	45	82
68	WR_pad<0>	-1959.5	-351	45	82
69	WR_pad<0>	-1899.5	-351	45	82
70	WR_pad<1>	-1839.5	-351	45	82
71	WR_pad<1>	-1779.5	-351	45	82
72	VSSX	-1719.5	-351	45	82
73	BM_pad<0>	-1659.5	-351	45	82
74	BM_pad<0>	-1599.5	-351	45	82
75	BM_pad<1>	-1539.5	-351	45	82
76	BM_pad<1>	-1479.5	-351	45	82
77	VSSX	-1419.5	-351	45	82
78	ID_pad	-1359.5	-351	45	82
79	ID_pad	-1299.5	-351	45	82
80	POR_DIS_pad	-1239.5	-351	45	82
81	POR_DIS_pad	-1179.5	-351	45	82
82	VSS	-1119.5	-351	45	82
83	VSS	-1059.5	-351	45	82
84	VSS	-999.5	-351	45	82
85	VSS	-939.5	-351	45	82
86	VSS	-879.5	-351	45	82
87	VSS	-819.5	-351	45	82
88	VSS	-759.5	-351	45	82
89	VSS	-699.5	-351	45	82
90	VSS	-639.5	-351	45	82
91	VSS	-579.5	-351	45	82
92	VSS	-519.5	-351	45	82
93	VSS	-459.5	-351	45	82
94	VSS	-399.5	-351	45	82
95	VSS	-339.5	-351	45	82
96	VSS	-279.5	-351	45	82
97	VSS2	-219.5	-351	45	82
98	VSS2	-159.5	-351	45	82
99	VSS2	-99.5	-351	45	82
100	VSS2	-39.5	-351	45	82
101	VSS2	20.5	-351	45	82
102	VSS2	80.5	-351	45	82
103	VSS2	140.5	-351	45	82
104	VSS2	200.5	-351	45	82
105	VSS2	260.5	-351	45	82
106	VSS2	320.5	-351	45	82
107	VSS2	380.5	-351	45	82
108	VSS2	440.5	-351	45	82
109	VSS2	500.5	-351	45	82
110	VDD2	560.5	-351	45	82
111	VDD2	620.5	-351	45	82
112	VDD2	680.5	-351	45	82
113	VDD2	740.5	-351	45	82
114	VDD2	800.5	-351	45	82

No.	Pad	X	Y	W	H
115	VDD2	860.5	-351	45	82
116	VDD2	920.5	-351	45	82
117	VDD2	980.5	-351	45	82
118	VDD2	1040.5	-351	45	82
119	VDD2	1100.5	-351	45	82
120	VDD2	1160.5	-351	45	82
121	VDD2	1220.5	-351	45	82
122	VDD2	1280.5	-351	45	82
123	VDD3	1340.5	-351	45	82
124	VDD3	1400.5	-351	45	82
125	VDD3	1460.5	-351	45	82
126	VDD3	1520.5	-351	45	82
127	VDD3	1580.5	-351	45	82
128	VDD	1640.5	-351	45	82
129	VDD	1700.5	-351	45	82
130	VDD	1760.5	-351	45	82
131	VDD	1820.5	-351	45	82
132	VDD	1880.5	-351	45	82
133	VDD	1940.5	-351	45	82
134	VDD	2000.5	-351	45	82
135	VDD	2060.5	-351	45	82
136	VDD	2120.5	-351	45	82
137	VDD	2180.5	-351	45	82
138	VDD	2240.5	-351	45	82
139	VDD	2300.5	-351	45	82
140	VDD	2360.5	-351	45	82
141	VDD	2420.5	-351	45	82
142	TST2_pad	2480.5	-351	45	82
143	TST2_pad	2540.5	-351	45	82
144	VLCDIN_pad	2608.5	-351	45	82
145	VLCDIN_pad	2668.5	-351	45	82
146	VLCDIN_pad	2728.5	-351	45	82
147	VLCDIN_pad	2788.5	-351	45	82
148	VLCDOUT_pad	2867.42	-351	45	82
149	VLCDOUT_pad	2927.42	-351	45	82
150	VLCDOUT_pad	2987.42	-351	45	82
151	VLCDOUT_pad	3047.42	-351	45	82
152	VLCDOUT_pad	3107.42	-351	45	82
153	VB0N_pad	3185.02	-351	45	82
154	VB0N_pad	3245.02	-351	45	82
155	VB0N_pad	3305.02	-351	45	82
156	VB1N_pad	3365.02	-351	45	82
157	VB1N_pad	3425.02	-351	45	82
158	VB1N_pad	3485.02	-351	45	82
159	VB1P_pad	3576.22	-351	45	82
160	VB1P_pad	3636.22	-351	45	82
161	VB1P_pad	3696.22	-351	45	82
162	VB0P_pad	3756.22	-351	45	82
163	VB0P_pad	3816.22	-351	45	82
164	VB0P_pad	3876.22	-351	45	82
165	ICONH_PAD	4168.2	-293.5	11.2	134
166	COM_pad<162>	4191.4	-293.5	11.2	134
167	COM_pad<160>	4214.6	-293.5	11.2	134
168	COM_pad<158>	4237.8	-293.5	11.2	134
169	DUMMY3	4404.9	-384.4	134	11.2
170	COM_pad<156>	4404.9	-361.2	134	11.2
171	COM_pad<154>	4404.9	-338	134	11.2
172	COM_pad<152>	4404.9	-314.8	134	11.2
173	COM_pad<150>	4404.9	-291.6	134	11.2

No.	Pad	X	Y	W	H
174	COM_pad<148>	4404.9	-268.4	134	11.2
175	COM_pad<146>	4404.9	-245.2	134	11.2
176	COM_pad<144>	4404.9	-222	134	11.2
177	COM_pad<142>	4404.9	-198.8	134	11.2
178	COM_pad<140>	4404.9	-175.6	134	11.2
179	COM_pad<138>	4404.9	-152.4	134	11.2
180	COM_pad<136>	4404.9	-129.2	134	11.2
181	COM_pad<134>	4404.9	-106	134	11.2
182	COM_pad<132>	4404.9	-82.8	134	11.2
183	COM_pad<130>	4404.9	-59.6	134	11.2
184	COM_pad<128>	4404.9	-36.4	134	11.2
185	COM_pad<126>	4404.9	-13.2	134	11.2
186	COM_pad<124>	4404.9	10	134	11.2
187	COM_pad<122>	4404.9	33.2	134	11.2
188	COM_pad<120>	4404.9	56.4	134	11.2
189	COM_pad<118>	4404.9	79.6	134	11.2
190	COM_pad<116>	4404.9	102.8	134	11.2
191	COM_pad<114>	4404.9	126	134	11.2
192	COM_pad<112>	4404.9	149.2	134	11.2
193	COM_pad<110>	4404.9	172.4	134	11.2
194	COM_pad<108>	4404.9	195.6	134	11.2
195	COM_pad<106>	4404.9	218.8	134	11.2
196	COM_pad<104>	4404.9	242	134	11.2
197	COM_pad<102>	4404.9	265.2	134	11.2
198	COM_pad<100>	4404.9	288.4	134	11.2
199	COM_pad<98>	4404.9	311.6	134	11.2
200	DUMMY4	4404.9	334.8	134	11.2
201	COM_pad<96>	4237.8	302.5	11.2	134
202	COM_pad<94>	4214.6	302.5	11.2	134
203	COM_pad<92>	4191.4	302.5	11.2	134
204	COM_pad<90>	4168.2	302.5	11.2	134
205	COM_pad<88>	4145	302.5	11.2	134
206	COM_pad<86>	4121.8	302.5	11.2	134
207	COM_pad<84>	4098.6	302.5	11.2	134
208	COM_pad<82>	4075.4	302.5	11.2	134
209	COM_pad<80>	4052.2	302.5	11.2	134
210	COM_pad<78>	4029	302.5	11.2	134
211	COM_pad<76>	4005.8	302.5	11.2	134
212	COM_pad<74>	3982.6	302.5	11.2	134
213	COM_pad<72>	3959.4	302.5	11.2	134
214	COM_pad<70>	3936.2	302.5	11.2	134
215	COM_pad<68>	3913	302.5	11.2	134
216	COM_pad<66>	3889.8	302.5	11.2	134
217	COM_pad<64>	3866.6	302.5	11.2	134
218	COM_pad<62>	3843.4	302.5	11.2	134
219	COM_pad<60>	3820.2	302.5	11.2	134
220	COM_pad<58>	3797	302.5	11.2	134
221	COM_pad<56>	3773.8	302.5	11.2	134
222	COM_pad<54>	3750.6	302.5	11.2	134
223	COM_pad<52>	3727.4	302.5	11.2	134
224	COM_pad<50>	3704.2	302.5	11.2	134
225	COM_pad<48>	3681	302.5	11.2	134
226	COM_pad<46>	3657.8	302.5	11.2	134
227	COM_pad<44>	3634.6	302.5	11.2	134
228	COM_pad<42>	3611.4	302.5	11.2	134
229	COM_pad<40>	3588.2	302.5	11.2	134
230	COM_pad<38>	3565	302.5	11.2	134
231	COM_pad<36>	3541.8	302.5	11.2	134
232	COM_pad<34>	3518.6	302.5	11.2	134

No.	Pad	X	Y	W	H
233	COM_pad<32>	3495.4	302.5	11.2	134
234	COM_pad<30>	3472.2	302.5	11.2	134
235	COM_pad<28>	3449	302.5	11.2	134
236	COM_pad<26>	3425.8	302.5	11.2	134
237	COM_pad<24>	3402.6	302.5	11.2	134
238	COM_pad<22>	3379.4	302.5	11.2	134
239	COM_pad<20>	3356.2	302.5	11.2	134
240	COM_pad<18>	3333	302.5	11.2	134
241	COM_pad<16>	3309.8	302.5	11.2	134
242	COM_pad<14>	3286.6	302.5	11.2	134
243	COM_pad<12>	3263.4	302.5	11.2	134
244	COM_pad<10>	3240.2	302.5	11.2	134
245	COM_pad<8>	3217	302.5	11.2	134
246	COM_pad<6>	3193.8	302.5	11.2	134
247	COM_pad<4>	3170.6	302.5	11.2	134
248	COM_pad<2>	3147.4	302.5	11.2	134
249	SEG_pad<1>	2994	302.5	11.2	134
250	SEG_pad<2>	2970.8	302.5	11.2	134
251	SEG_pad<3>	2947.6	302.5	11.2	134
252	SEG_pad<4>	2924.4	302.5	11.2	134
253	SEG_pad<5>	2901.2	302.5	11.2	134
254	SEG_pad<6>	2878	302.5	11.2	134
255	SEG_pad<7>	2854.8	302.5	11.2	134
256	SEG_pad<8>	2831.6	302.5	11.2	134
257	SEG_pad<9>	2808.4	302.5	11.2	134
258	SEG_pad<10>	2785.2	302.5	11.2	134
259	SEG_pad<11>	2762	302.5	11.2	134
260	SEG_pad<12>	2738.8	302.5	11.2	134
261	SEG_pad<13>	2715.6	302.5	11.2	134
262	SEG_pad<14>	2692.4	302.5	11.2	134
263	SEG_pad<15>	2669.2	302.5	11.2	134
264	SEG_pad<16>	2646	302.5	11.2	134
265	SEG_pad<17>	2622.8	302.5	11.2	134
266	SEG_pad<18>	2599.6	302.5	11.2	134
267	SEG_pad<19>	2576.4	302.5	11.2	134
268	SEG_pad<20>	2553.2	302.5	11.2	134
269	SEG_pad<21>	2530	302.5	11.2	134
270	SEG_pad<22>	2506.8	302.5	11.2	134
271	SEG_pad<23>	2483.6	302.5	11.2	134
272	SEG_pad<24>	2460.4	302.5	11.2	134
273	SEG_pad<25>	2437.2	302.5	11.2	134
274	SEG_pad<26>	2414	302.5	11.2	134
275	SEG_pad<27>	2390.8	302.5	11.2	134
276	SEG_pad<28>	2367.6	302.5	11.2	134
277	SEG_pad<29>	2344.4	302.5	11.2	134
278	SEG_pad<30>	2321.2	302.5	11.2	134
279	SEG_pad<31>	2298	302.5	11.2	134
280	SEG_pad<32>	2274.8	302.5	11.2	134
281	SEG_pad<33>	2251.6	302.5	11.2	134
282	SEG_pad<34>	2228.4	302.5	11.2	134
283	SEG_pad<35>	2205.2	302.5	11.2	134
284	SEG_pad<36>	2182	302.5	11.2	134
285	SEG_pad<37>	2158.8	302.5	11.2	134
286	SEG_pad<38>	2135.6	302.5	11.2	134
287	SEG_pad<39>	2112.4	302.5	11.2	134
288	SEG_pad<40>	2089.2	302.5	11.2	134
289	SEG_pad<41>	2066	302.5	11.2	134
290	SEG_pad<42>	2042.8	302.5	11.2	134
291	SEG_pad<43>	2019.6	302.5	11.2	134

No.	Pad	X	Y	W	H
292	SEG_pad<44>	1996.4	302.5	11.2	134
293	SEG_pad<45>	1973.2	302.5	11.2	134
294	SEG_pad<46>	1950	302.5	11.2	134
295	SEG_pad<47>	1926.8	302.5	11.2	134
296	SEG_pad<48>	1903.6	302.5	11.2	134
297	SEG_pad<49>	1880.4	302.5	11.2	134
298	SEG_pad<50>	1857.2	302.5	11.2	134
299	SEG_pad<51>	1834	302.5	11.2	134
300	SEG_pad<52>	1810.8	302.5	11.2	134
301	SEG_pad<53>	1787.6	302.5	11.2	134
302	SEG_pad<54>	1764.4	302.5	11.2	134
303	SEG_pad<55>	1741.2	302.5	11.2	134
304	SEG_pad<56>	1718	302.5	11.2	134
305	SEG_pad<57>	1694.8	302.5	11.2	134
306	SEG_pad<58>	1671.6	302.5	11.2	134
307	SEG_pad<59>	1648.4	302.5	11.2	134
308	SEG_pad<60>	1625.2	302.5	11.2	134
309	SEG_pad<61>	1602	302.5	11.2	134
310	SEG_pad<62>	1578.8	302.5	11.2	134
311	SEG_pad<63>	1555.6	302.5	11.2	134
312	SEG_pad<64>	1532.4	302.5	11.2	134
313	SEG_pad<65>	1509.2	302.5	11.2	134
314	SEG_pad<66>	1486	302.5	11.2	134
315	SEG_pad<67>	1462.8	302.5	11.2	134
316	SEG_pad<68>	1439.6	302.5	11.2	134
317	SEG_pad<69>	1416.4	302.5	11.2	134
318	SEG_pad<70>	1393.2	302.5	11.2	134
319	SEG_pad<71>	1370	302.5	11.2	134
320	SEG_pad<72>	1346.8	302.5	11.2	134
321	SEG_pad<73>	1323.6	302.5	11.2	134
322	SEG_pad<74>	1300.4	302.5	11.2	134
323	SEG_pad<75>	1277.2	302.5	11.2	134
324	SEG_pad<76>	1254	302.5	11.2	134
325	SEG_pad<77>	1230.8	302.5	11.2	134
326	SEG_pad<78>	1207.6	302.5	11.2	134
327	SEG_pad<79>	1184.4	302.5	11.2	134
328	SEG_pad<80>	1161.2	302.5	11.2	134
329	SEG_pad<81>	1138	302.5	11.2	134
330	SEG_pad<82>	1114.8	302.5	11.2	134
331	SEG_pad<83>	1091.6	302.5	11.2	134
332	SEG_pad<84>	1068.4	302.5	11.2	134
333	SEG_pad<85>	1045.2	302.5	11.2	134
334	SEG_pad<86>	1022	302.5	11.2	134
335	SEG_pad<87>	998.8	302.5	11.2	134
336	SEG_pad<88>	975.6	302.5	11.2	134
337	SEG_pad<89>	952.4	302.5	11.2	134
338	SEG_pad<90>	929.2	302.5	11.2	134
339	SEG_pad<91>	906	302.5	11.2	134
340	SEG_pad<92>	882.8	302.5	11.2	134
341	SEG_pad<93>	859.6	302.5	11.2	134
342	SEG_pad<94>	836.4	302.5	11.2	134
343	SEG_pad<95>	813.2	302.5	11.2	134
344	SEG_pad<96>	790	302.5	11.2	134
345	SEG_pad<97>	766.8	302.5	11.2	134
346	SEG_pad<98>	743.6	302.5	11.2	134
347	SEG_pad<99>	720.4	302.5	11.2	134
348	SEG_pad<100>	697.2	302.5	11.2	134
349	SEG_pad<101>	674	302.5	11.2	134
350	SEG_pad<102>	650.8	302.5	11.2	134

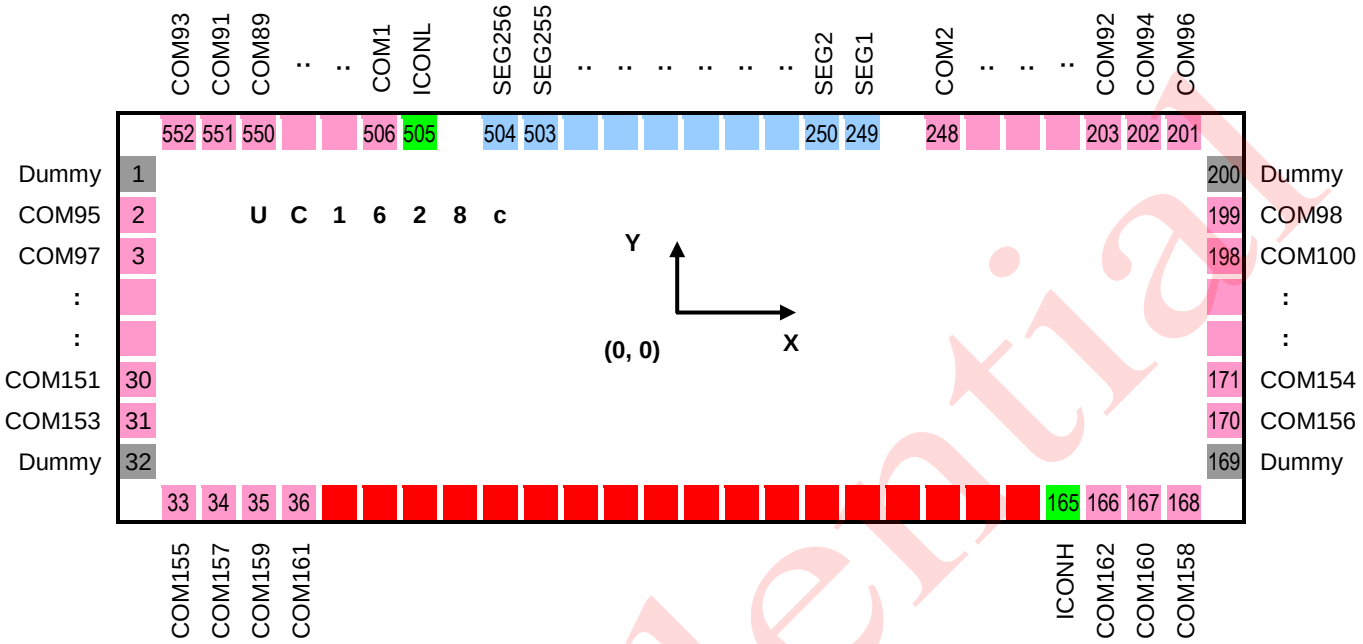
No.	Pad	X	Y	W	H
351	SEG_pad<103>	627.6	302.5	11.2	134
352	SEG_pad<104>	604.4	302.5	11.2	134
353	SEG_pad<105>	581.2	302.5	11.2	134
354	SEG_pad<106>	558	302.5	11.2	134
355	SEG_pad<107>	534.8	302.5	11.2	134
356	SEG_pad<108>	511.6	302.5	11.2	134
357	SEG_pad<109>	488.4	302.5	11.2	134
358	SEG_pad<110>	465.2	302.5	11.2	134
359	SEG_pad<111>	442	302.5	11.2	134
360	SEG_pad<112>	418.8	302.5	11.2	134
361	SEG_pad<113>	395.6	302.5	11.2	134
362	SEG_pad<114>	372.4	302.5	11.2	134
363	SEG_pad<115>	349.2	302.5	11.2	134
364	SEG_pad<116>	326	302.5	11.2	134
365	SEG_pad<117>	302.8	302.5	11.2	134
366	SEG_pad<118>	279.6	302.5	11.2	134
367	SEG_pad<119>	256.4	302.5	11.2	134
368	SEG_pad<120>	233.2	302.5	11.2	134
369	SEG_pad<121>	210	302.5	11.2	134
370	SEG_pad<122>	186.8	302.5	11.2	134
371	SEG_pad<123>	163.6	302.5	11.2	134
372	SEG_pad<124>	140.4	302.5	11.2	134
373	SEG_pad<125>	117.2	302.5	11.2	134
374	SEG_pad<126>	94	302.5	11.2	134
375	SEG_pad<127>	70.8	302.5	11.2	134
376	SEG_pad<128>	47.6	302.5	11.2	134
377	SEG_pad<129>	-47.6	302.5	11.2	134
378	SEG_pad<130>	-70.8	302.5	11.2	134
379	SEG_pad<131>	-94	302.5	11.2	134
380	SEG_pad<132>	-117.2	302.5	11.2	134
381	SEG_pad<133>	-140.4	302.5	11.2	134
382	SEG_pad<134>	-163.6	302.5	11.2	134
383	SEG_pad<135>	-186.8	302.5	11.2	134
384	SEG_pad<136>	-210	302.5	11.2	134
385	SEG_pad<137>	-233.2	302.5	11.2	134
386	SEG_pad<138>	-256.4	302.5	11.2	134
387	SEG_pad<139>	-279.6	302.5	11.2	134
388	SEG_pad<140>	-302.8	302.5	11.2	134
389	SEG_pad<141>	-326	302.5	11.2	134
390	SEG_pad<142>	-349.2	302.5	11.2	134
391	SEG_pad<143>	-372.4	302.5	11.2	134
392	SEG_pad<144>	-395.6	302.5	11.2	134
393	SEG_pad<145>	-418.8	302.5	11.2	134
394	SEG_pad<146>	-442	302.5	11.2	134
395	SEG_pad<147>	-465.2	302.5	11.2	134
396	SEG_pad<148>	-488.4	302.5	11.2	134
397	SEG_pad<149>	-511.6	302.5	11.2	134
398	SEG_pad<150>	-534.8	302.5	11.2	134
399	SEG_pad<151>	-558	302.5	11.2	134
400	SEG_pad<152>	-581.2	302.5	11.2	134
401	SEG_pad<153>	-604.4	302.5	11.2	134
402	SEG_pad<154>	-627.6	302.5	11.2	134
403	SEG_pad<155>	-650.8	302.5	11.2	134
404	SEG_pad<156>	-674	302.5	11.2	134
405	SEG_pad<157>	-697.2	302.5	11.2	134
406	SEG_pad<158>	-720.4	302.5	11.2	134
407	SEG_pad<159>	-743.6	302.5	11.2	134
408	SEG_pad<160>	-766.8	302.5	11.2	134
409	SEG_pad<161>	-790	302.5	11.2	134

No.	Pad	X	Y	W	H
410	SEG_pad<162>	-813.2	302.5	11.2	134
411	SEG_pad<163>	-836.4	302.5	11.2	134
412	SEG_pad<164>	-859.6	302.5	11.2	134
413	SEG_pad<165>	-882.8	302.5	11.2	134
414	SEG_pad<166>	-906	302.5	11.2	134
415	SEG_pad<167>	-929.2	302.5	11.2	134
416	SEG_pad<168>	-952.4	302.5	11.2	134
417	SEG_pad<169>	-975.6	302.5	11.2	134
418	SEG_pad<170>	-998.8	302.5	11.2	134
419	SEG_pad<171>	-1022	302.5	11.2	134
420	SEG_pad<172>	-1045.2	302.5	11.2	134
421	SEG_pad<173>	-1068.4	302.5	11.2	134
422	SEG_pad<174>	-1091.6	302.5	11.2	134
423	SEG_pad<175>	-1114.8	302.5	11.2	134
424	SEG_pad<176>	-1138	302.5	11.2	134
425	SEG_pad<177>	-1161.2	302.5	11.2	134
426	SEG_pad<178>	-1184.4	302.5	11.2	134
427	SEG_pad<179>	-1207.6	302.5	11.2	134
428	SEG_pad<180>	-1230.8	302.5	11.2	134
429	SEG_pad<181>	-1254	302.5	11.2	134
430	SEG_pad<182>	-1277.2	302.5	11.2	134
431	SEG_pad<183>	-1300.4	302.5	11.2	134
432	SEG_pad<184>	-1323.6	302.5	11.2	134
433	SEG_pad<185>	-1346.8	302.5	11.2	134
434	SEG_pad<186>	-1370	302.5	11.2	134
435	SEG_pad<187>	-1393.2	302.5	11.2	134
436	SEG_pad<188>	-1416.4	302.5	11.2	134
437	SEG_pad<189>	-1439.6	302.5	11.2	134
438	SEG_pad<190>	-1462.8	302.5	11.2	134
439	SEG_pad<191>	-1486	302.5	11.2	134
440	SEG_pad<192>	-1509.2	302.5	11.2	134
441	SEG_pad<193>	-1532.4	302.5	11.2	134
442	SEG_pad<194>	-1555.6	302.5	11.2	134
443	SEG_pad<195>	-1578.8	302.5	11.2	134
444	SEG_pad<196>	-1602	302.5	11.2	134
445	SEG_pad<197>	-1625.2	302.5	11.2	134
446	SEG_pad<198>	-1648.4	302.5	11.2	134
447	SEG_pad<199>	-1671.6	302.5	11.2	134
448	SEG_pad<200>	-1694.8	302.5	11.2	134
449	SEG_pad<201>	-1718	302.5	11.2	134
450	SEG_pad<202>	-1741.2	302.5	11.2	134
451	SEG_pad<203>	-1764.4	302.5	11.2	134
452	SEG_pad<204>	-1787.6	302.5	11.2	134
453	SEG_pad<205>	-1810.8	302.5	11.2	134
454	SEG_pad<206>	-1834	302.5	11.2	134
455	SEG_pad<207>	-1857.2	302.5	11.2	134
456	SEG_pad<208>	-1880.4	302.5	11.2	134
457	SEG_pad<209>	-1903.6	302.5	11.2	134
458	SEG_pad<210>	-1926.8	302.5	11.2	134
459	SEG_pad<211>	-1950	302.5	11.2	134
460	SEG_pad<212>	-1973.2	302.5	11.2	134
461	SEG_pad<213>	-1996.4	302.5	11.2	134
462	SEG_pad<214>	-2019.6	302.5	11.2	134
463	SEG_pad<215>	-2042.8	302.5	11.2	134
464	SEG_pad<216>	-2066	302.5	11.2	134
465	SEG_pad<217>	-2089.2	302.5	11.2	134
466	SEG_pad<218>	-2112.4	302.5	11.2	134
467	SEG_pad<219>	-2135.6	302.5	11.2	134
468	SEG_pad<220>	-2158.8	302.5	11.2	134

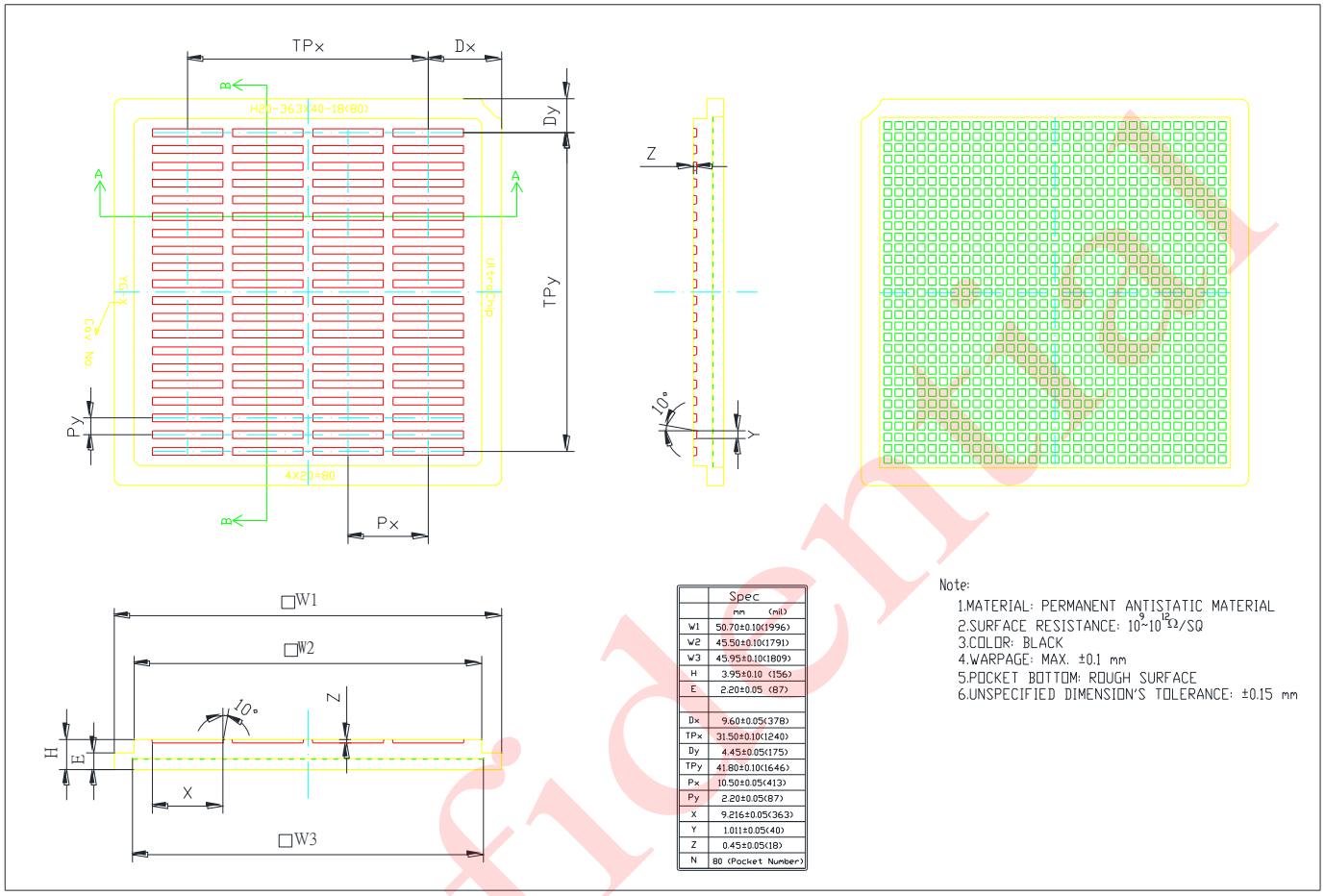
No.	Pad	X	Y	W	H
469	SEG_pad<221>	-2182	302.5	11.2	134
470	SEG_pad<222>	-2205.2	302.5	11.2	134
471	SEG_pad<223>	-2228.4	302.5	11.2	134
472	SEG_pad<224>	-2251.6	302.5	11.2	134
473	SEG_pad<225>	-2274.8	302.5	11.2	134
474	SEG_pad<226>	-2298	302.5	11.2	134
475	SEG_pad<227>	-2321.2	302.5	11.2	134
476	SEG_pad<228>	-2344.4	302.5	11.2	134
477	SEG_pad<229>	-2367.6	302.5	11.2	134
478	SEG_pad<230>	-2390.8	302.5	11.2	134
479	SEG_pad<231>	-2414	302.5	11.2	134
480	SEG_pad<232>	-2437.2	302.5	11.2	134
481	SEG_pad<233>	-2460.4	302.5	11.2	134
482	SEG_pad<234>	-2483.6	302.5	11.2	134
483	SEG_pad<235>	-2506.8	302.5	11.2	134
484	SEG_pad<236>	-2530	302.5	11.2	134
485	SEG_pad<237>	-2553.2	302.5	11.2	134
486	SEG_pad<238>	-2576.4	302.5	11.2	134
487	SEG_pad<239>	-2599.6	302.5	11.2	134
488	SEG_pad<240>	-2622.8	302.5	11.2	134
489	SEG_pad<241>	-2646	302.5	11.2	134
490	SEG_pad<242>	-2669.2	302.5	11.2	134
491	SEG_pad<243>	-2692.4	302.5	11.2	134
492	SEG_pad<244>	-2715.6	302.5	11.2	134
493	SEG_pad<245>	-2738.8	302.5	11.2	134
494	SEG_pad<246>	-2762	302.5	11.2	134
495	SEG_pad<247>	-2785.2	302.5	11.2	134
496	SEG_pad<248>	-2808.4	302.5	11.2	134
497	SEG_pad<249>	-2831.6	302.5	11.2	134
498	SEG_pad<250>	-2854.8	302.5	11.2	134
499	SEG_pad<251>	-2878	302.5	11.2	134
500	SEG_pad<252>	-2901.2	302.5	11.2	134
501	SEG_pad<253>	-2924.4	302.5	11.2	134
502	SEG_pad<254>	-2947.6	302.5	11.2	134
503	SEG_pad<255>	-2970.8	302.5	11.2	134
504	SEG_pad<256>	-2994	302.5	11.2	134
505	ICONH_PAD	-3147.4	302.5	11.2	134
506	COM_pad<1>	-3170.6	302.5	11.2	134
507	COM_pad<3>	-3193.8	302.5	11.2	134
508	COM_pad<5>	-3217	302.5	11.2	134
509	COM_pad<7>	-3240.2	302.5	11.2	134
510	COM_pad<9>	-3263.4	302.5	11.2	134
511	COM_pad<11>	-3286.6	302.5	11.2	134
512	COM_pad<13>	-3309.8	302.5	11.2	134
513	COM_pad<15>	-3333	302.5	11.2	134
514	COM_pad<17>	-3356.2	302.5	11.2	134
515	COM_pad<19>	-3379.4	302.5	11.2	134
516	COM_pad<21>	-3402.6	302.5	11.2	134
517	COM_pad<23>	-3425.8	302.5	11.2	134
518	COM_pad<25>	-3449	302.5	11.2	134
519	COM_pad<27>	-3472.2	302.5	11.2	134
520	COM_pad<29>	-3495.4	302.5	11.2	134
521	COM_pad<31>	-3518.6	302.5	11.2	134
522	COM_pad<33>	-3541.8	302.5	11.2	134
523	COM_pad<35>	-3565	302.5	11.2	134
524	COM_pad<37>	-3588.2	302.5	11.2	134
525	COM_pad<39>	-3611.4	302.5	11.2	134
526	COM_pad<41>	-3634.6	302.5	11.2	134
527	COM_pad<43>	-3657.8	302.5	11.2	134

No.	Pad	X	Y	W	H
528	COM_pad<45>	-3681	302.5	11.2	134
529	COM_pad<47>	-3704.2	302.5	11.2	134
530	COM_pad<49>	-3727.4	302.5	11.2	134
531	COM_pad<51>	-3750.6	302.5	11.2	134
532	COM_pad<53>	-3773.8	302.5	11.2	134
533	COM_pad<55>	-3797	302.5	11.2	134
534	COM_pad<57>	-3820.2	302.5	11.2	134
535	COM_pad<59>	-3843.4	302.5	11.2	134
536	COM_pad<61>	-3866.6	302.5	11.2	134
537	COM_pad<63>	-3889.8	302.5	11.2	134
538	COM_pad<65>	-3913	302.5	11.2	134
539	COM_pad<67>	-3936.2	302.5	11.2	134
540	COM_pad<69>	-3959.4	302.5	11.2	134
541	COM_pad<71>	-3982.6	302.5	11.2	134
542	COM_pad<73>	-4005.8	302.5	11.2	134
543	COM_pad<75>	-4029	302.5	11.2	134
544	COM_pad<77>	-4052.2	302.5	11.2	134
545	COM_pad<79>	-4075.4	302.5	11.2	134
546	COM_pad<81>	-4098.6	302.5	11.2	134
547	COM_pad<83>	-4121.8	302.5	11.2	134
548	COM_pad<85>	-4145	302.5	11.2	134
549	COM_pad<87>	-4168.2	302.5	11.2	134
550	COM_pad<89>	-4191.4	302.5	11.2	134
551	COM_pad<91>	-4214.6	302.5	11.2	134
552	COM_pad<93>	-4237.8	302.5	11.2	134

Output Pad Location



TRAY INFORMATION



REVISION HISTORY

Revision	Contents	Date
0.6	(First Release)	Nov. 28, 2016
0.8	(1) Line Rate → Frame Rate (2) Power Consumption (Max.) data are provided.	Mar. 29, 2017
1.0	(1) The description for pins Vss and Vss2 is enriched. (2) The description for pin RST is enriched. (3) The ITO drawing is updated.	Jun. 27, 2017
1.1	Updata COMMAND SUMMARY.	Jun. 24, 2020