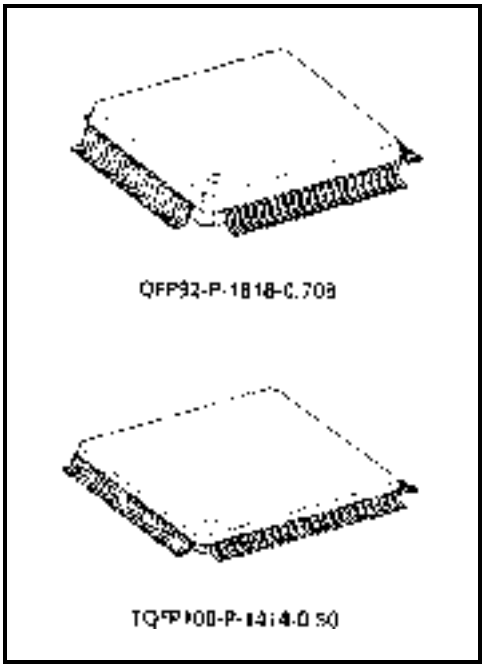
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6A40

ROW DRIVER FOR A DOT MATRIX LCD

The T6A40 is a 68−channel−output row driver for an STN dot matrix LCD. The T6A40 features −28 V LCD drive voltage. The T6A40 is able to drive LCD panels with a duty ratio of up to 1 / 240. It is recommended for use with the T6A39 / T6A39A.

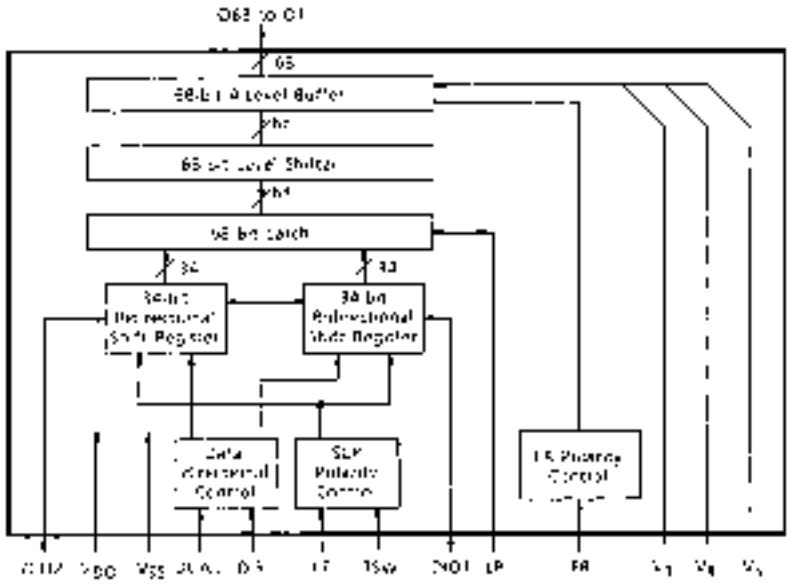


Weight
QFP92P−1818−0.70B : 1.45 g (typ.)
TQFP100−P−1414−0.50 : 0.45 g (typ.)

Features

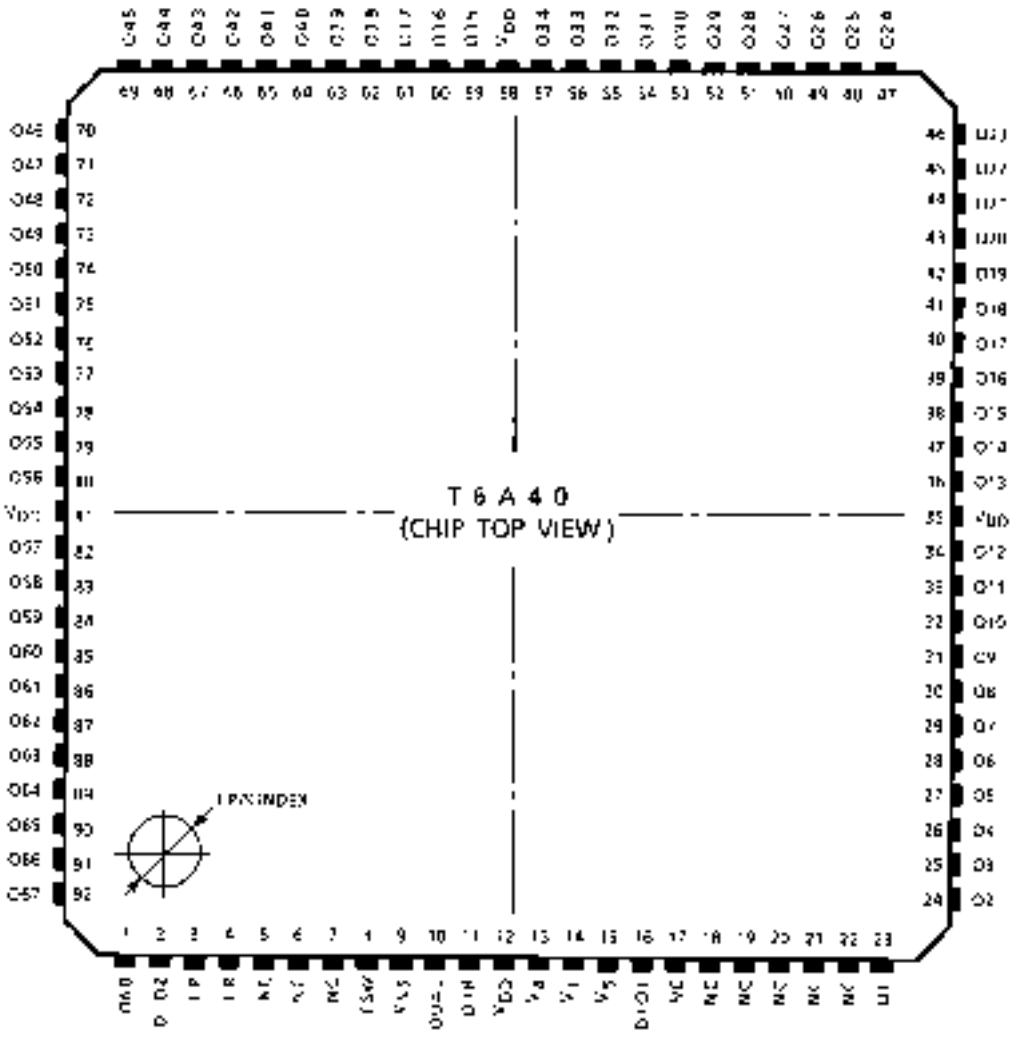
- Display duty application : to 1 / 240
- LCD drive signal : 68
- Data transfer : 1−bit bidirectional
  (1) O68 ← O1
  (2) O68 → O1
  (3) O1 → O34, O35 ← O68
- LCD drive voltage : −8 to −28 V (max −30 V)
- Operating voltage : 4.5 to 5.5 V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 1.5 kΩ (max) (12.8 V, 1 / 9 bias)
- LCD drive output timing : Change on falling edge of LP

Block Diagram



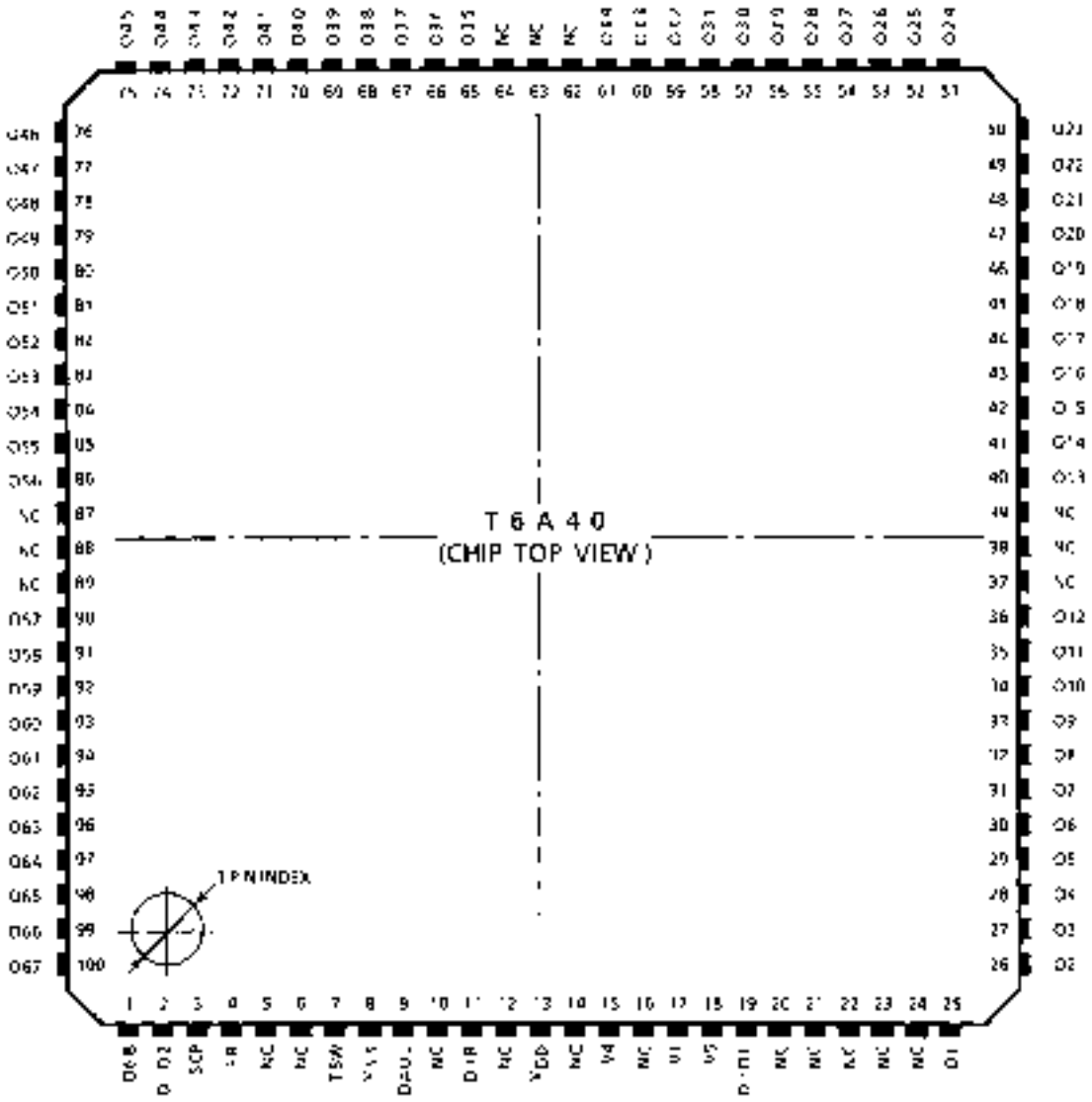
Pin Assignment

QFP92 P 1818 0.708



Pin Assignment

TQFP100 P-1414-0.50



Pin Functions

Pin Name	I / O	Functions	Level
O1 to O68	Output	Output for LCD drive signal	V_{DD} to V_5
DIO1, DIO2	I / O	Input / output for shift data	V_{DD} to V_{SS}
LP	Input	(Shift Clock Pulse) Input for shift clock pulse	
FR	Input	(Frame) Input for frame signal	
DUAL	Input	(Dual Mode) Terminal for dual input mode or single input mode select	
DIR	Input	(Direction) Input for data flow direction select	
TSW	Input	(Terminal Switch) When tied to V_{SS}: (O1 to O68) output on the rising edge of LP When tied to V_{DD}: (O1 to O68) output on the falling edge of LP	
V_{DD}	—	Power supply for internal logic (5 V)	—
V_{SS}	—	Power supply for internal logic (0 V)	
V_1	—	Power supply for LCD drive circuit	
V_4	—	Power supply for LCD drive circuit	
V_5	—	Power supply for LCD drive circuit	

Relation Between FR, Data Input and Output Level

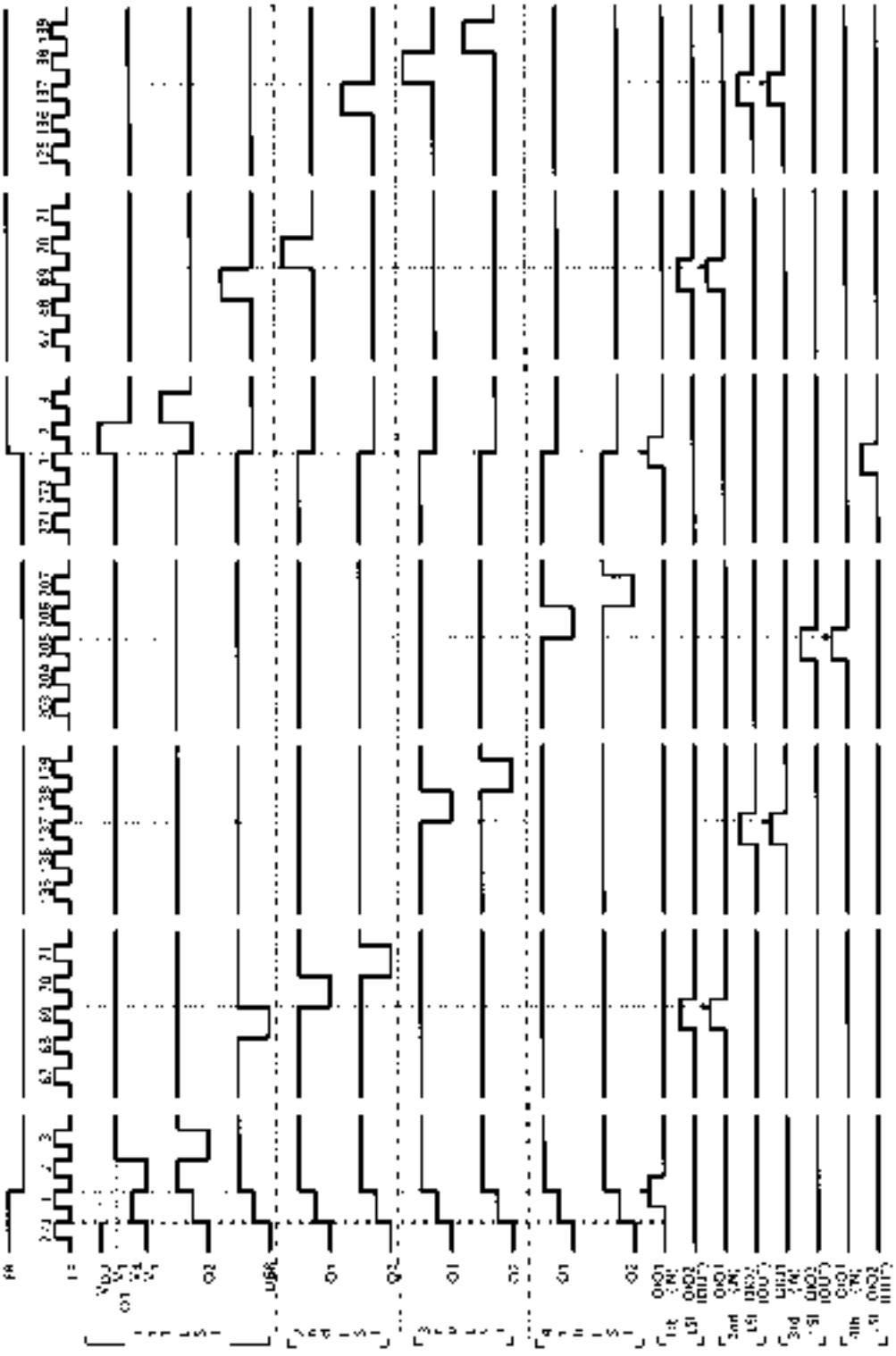
F R	Data Input (DIO1, DIO2)	Output Level
L	L	V_1
L	H	V_5
H	L	V_4
H	H	V_{DD}

Data Input Format

DUAL	DIR	Data	Data Input	
			DIO 1	DIO 2
V_{DD}	V_{DD}	O1 → O34	IN	IN
		O68 → O35		
V_{SS}	V_{DD}	O1 → O68	IN	OUT
V_{DD}	V_{SS}	O68 → O1	OUT	IN
V_{SS}	V_{SS}			

Timing Diagram

DIR = H, DUAL = L, TSW = H



Absolute Maximum Ratings
(Ensure that the Following Conditions are Maintained, $V_{DD} \geq V_1 \geq V_4 \geq V_5$, V_{SS} = 0 V)

Item	Symbol	Pin Name	Rating	Unit
Supply Voltage 1	V_{DD}	V_{DD}	−0.3 to 7.0	V
Supply Voltage 2	V_1	V_1	V_{DD} − 30.0 to V_{DD} + 0.3	V
Supply Voltage 3	V_4	V_4	V_{DD} − 30.0 to V_{DD} + 0.3	V
Supply Voltage 4	V_5	V_5	V_{DD} − 30.0 to V_{DD} + 0.3	V
Input Voltage	V_{IN}	(Note 1)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	−20 to 75	°C
Storage Temperature	T_{stg}	—	−55 to 125	°C

Note 1: FR, DIR, DIO1, DIO2, DUAL, TSW, LP

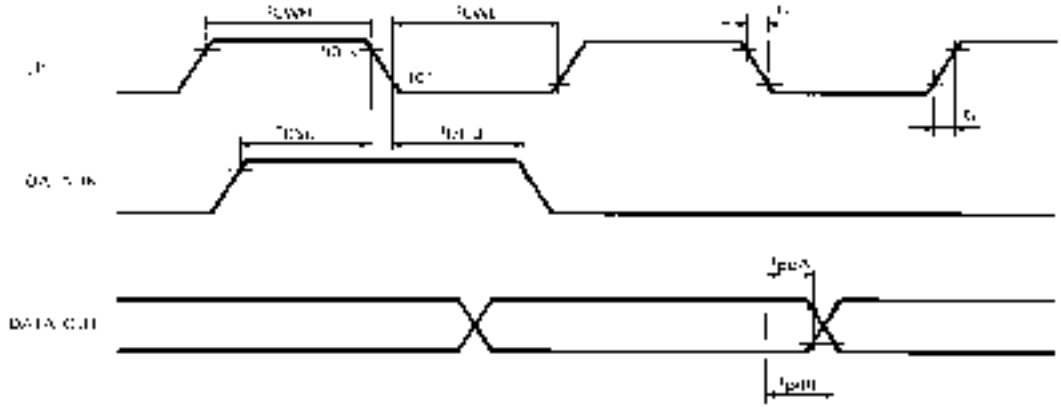
Electrical Characteristics
DC Characteristics
Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, $V_5 = (V_{DD} - 23)$ V ± 10%, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit	Pin Name
Supply Voltage1		V_{DD}	—	—		4.5	5.0	5.5	V	V_{DD}
Supply Voltage 2		V_5	—	—		V_{DD} −28	—	V_{DD} −8.0	V	V_5
Input Voltage	H Level	V_{IH}	—	(Note 2)		V_{DD} −0.8	—	V_{DD}	V	FR, DIR, DIO1, DIO2, DUAL, LP, TSW
	L Level	V_{IL}		(Note 2)		0	—	0.8		
Output Voltage	H Level	V_{OH}	—	I_{OH} = −0.5 mA		V_{DD} −0.5	—	V_{DD}	V	DIO1, DIO2
	L Level	V_{OL}		I_{OL} = 0.5 mA		—	—	0.5		
Output Resis−tance	H Level	R_{OH}	—	$V_{OUT} = V_{DD}$ − 0.5 V	(Note 3)	—	—	1.2	kΩ	O1 to O68
	M Level	R_{OM}		$V_{OUT} = V_1$ ± 0.5 V	(Note 3)	—	—	1.2		
		R_{OM}		$V_{OUT} = V_4$ ± 0.5 V	(Note 3)	—	—	1.2		
	L Level	R_{OL}		$V_{OUT} = V_5$ + 0.5 V	(Note 3)	—	—	1.2		
Current Consumption		I_{SS}	—	V_{DD} = 5.5 V V_5 = −22.5 V f_{FR} = 35.5 Hz f_{LP} = 7.1 kHz O1 to O68: no load	Input Data: f_{DIO} = 71 Hz (Duty: 1 / 100) Input Voltage: H = V_{DD}, L = V_{SS} (Note 3)	—	2.0	4.0	μA	V_{SS}

Note 2: R_L = 3 kΩ, C_L = 1500 pF

Note 3: V_{DD} = 5.0 V, V_5 = −7.8 V, $V_1 = V_{DD} - 1 / 9 (V_{DD} - V_5)$, $V_4 = V_{DD} - 8 / 9 (V_{DD} - V_5)$

AC Characteristics



Test Conditions (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, V_5 = (V_{DD} − 23) V ± 10%, Ta = −20 to 75°C)

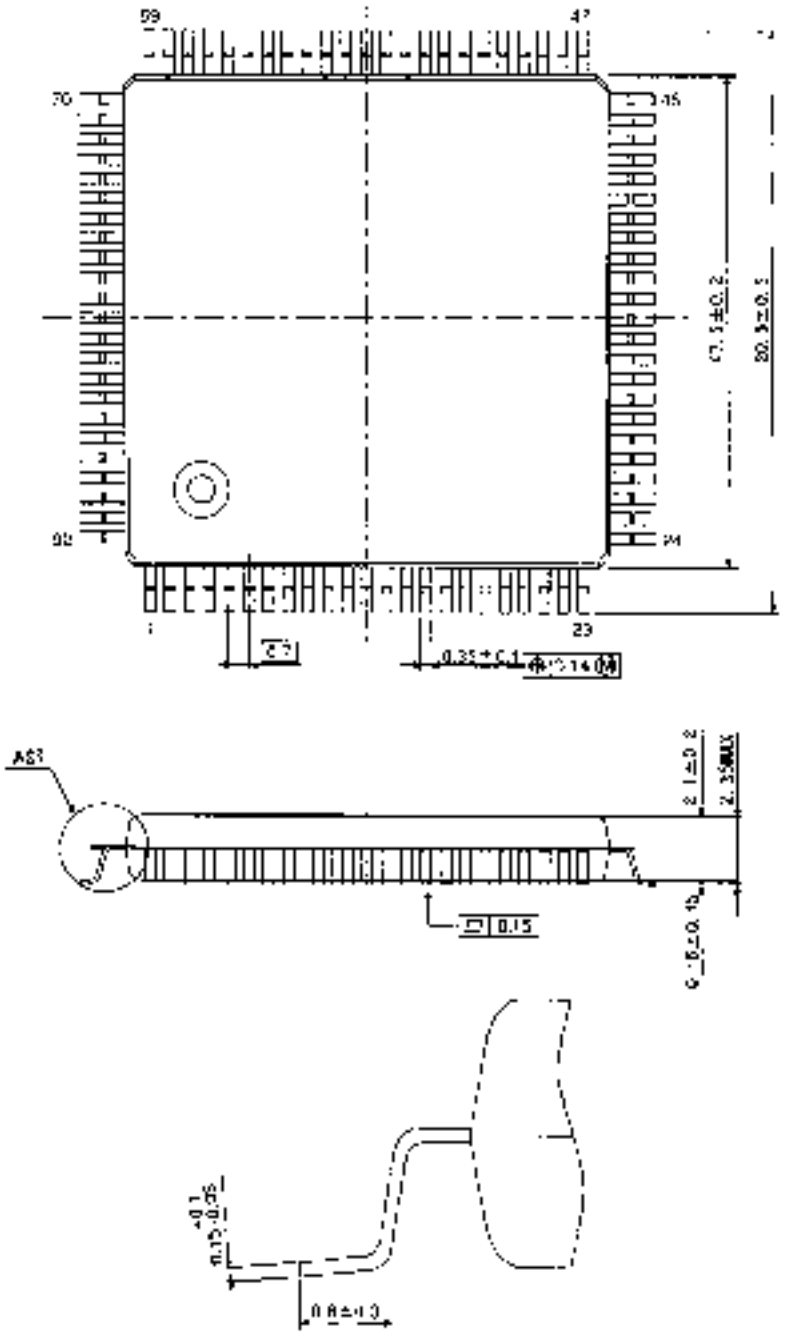
Item	Symbol	Test Condition	Min	Max	Unit
SCP Pulse Width H	t_{CWH}	LP	30	—	ns
SCP Pulse Width L	t_{CWL}	LP	1	—	µs
Input Rise / Fall Time	t_r, t_f	LP, FR, DIO1, DIO2	—	50	ns
Data Set−up Time	t_{DSU}	DIO1, DIO2	30	—	ns
Data Hold Time	t_{DHD}	DIO1, DIO2	50	—	ns
Output Data Delay Time A	tpdA	DIO1, DIO2 (Note 4)	80	—	ns
Output Data Delay Time B	tpdB	DIO1, DIO2 (Note 4)	—	1	µs

Note 4: C_L = 10 pF

NOTE: Insert the bypass capacitor (0.1 µF) between V_{DD} and V_{SS} to decrease power supply noise. Place the bypass capacitor as close to the LSI as possible.

Package Dimensions

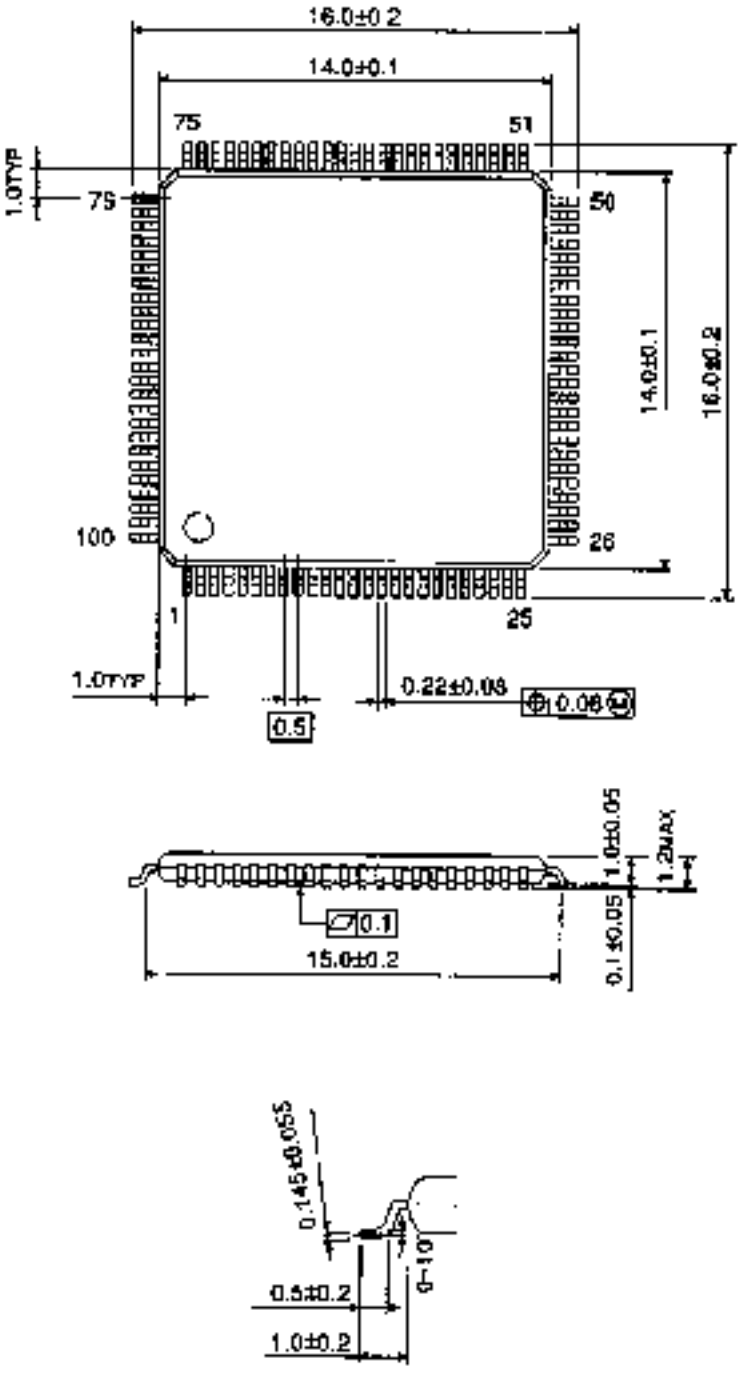
QFP92-P-1618-0.70B Unit : mm



Weight : 1.45g (typ.)

Package Dimensions

TQFP100-P-1414-0.50 Unit : mm



Weight : 0.45 g (Typ.)