ST8008

80 Output LCD Segment Driver IC

PRELIMINARY

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■ DESCRIPTION

The ST8008 is a 80-output segment driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary. The ST8008 is good as a segment driver, and it can create a low power consuming, high-resolution LCD.

■ FEATURES

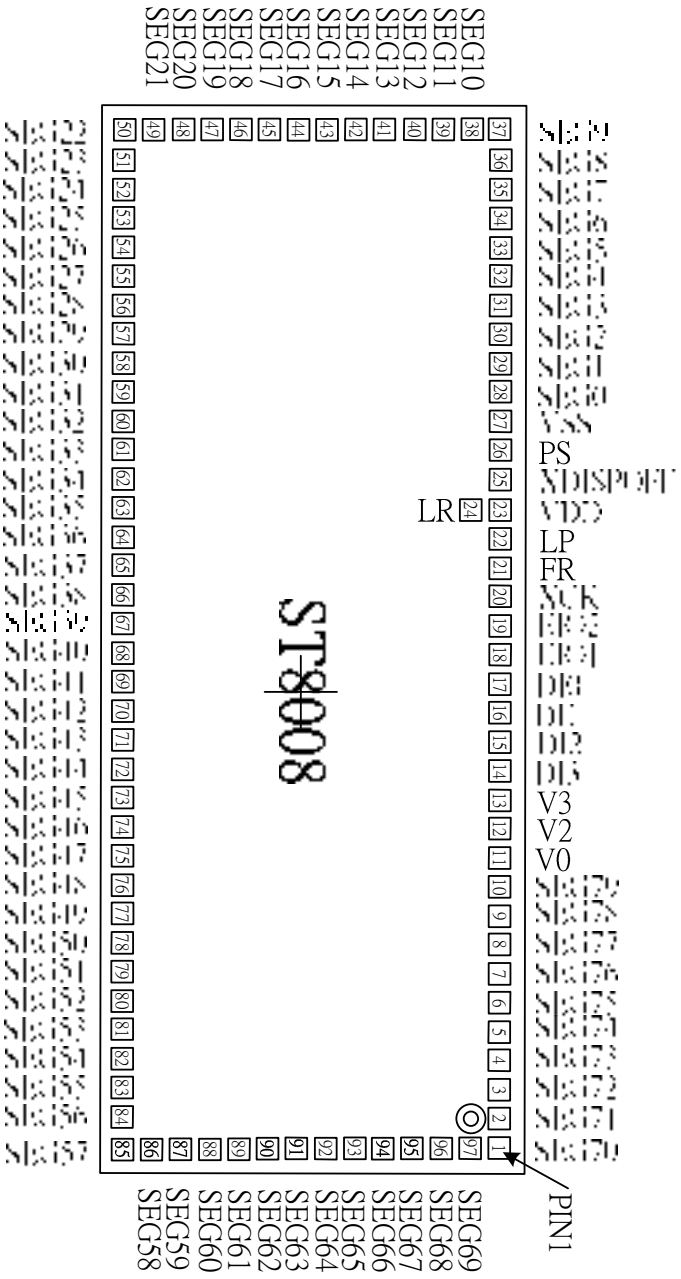
- Number of LCD drive outputs: 80
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Package: 96-pin COB.

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 80 bits of input data
- Line latch circuits are reset when XDISPOFF active

■ Pad Arrangement

Chip size: 3800(μm)X1560(μm)
Pad size: 80(μm)X80(μm)
Pin Pitch: 100(μm)~120(μm)
Origin: chip center(0,0)
Chip Thiclness:19 mil



Substrate Connect to Vss.

Pad Location Coordinates

Pad No	Function	X	Y
1	CS[70]	1785	665
2	CS[71]	1665	665
3	CS[72]	1555	665
4	CS[73]	1450	665
5	CS[74]	1350	665
6	CS[75]	1250	665
7	CS[76]	1150	665
8	CS[77]	1050	665
9	CS[78]	950	665
10	CS[79]	850	665
11	V0	750	665
12	V2	650	665
13	V3	550	665
14	ED[3]	450	665
15	ED[2]	350	665
16	ED[1]	250	665
17	ED[0]	150	665
18	EIO1	50	665
19	EIO2	-50	665
20	XCKPAD	-150	665
21	FRPAD	-250	665
22	LPPAD	-350	665
23	VDD	-450	665
24	LRPAD	-450	517.15
25	XDISPAD	-550	665
26	PSPAD	-650	665
27	VSS	-750	665
28	CS[0]	-850	665
29	CS[1]	-950	665
30	CS[2]	-1050	665
31	CS[3]	-1150	665
32	CS[4]	-1250	665
33	CS[5]	-1350	665
34	CS[6]	-1450	665
35	CS[7]	-1555	665
36	CS[8]	-1665	665

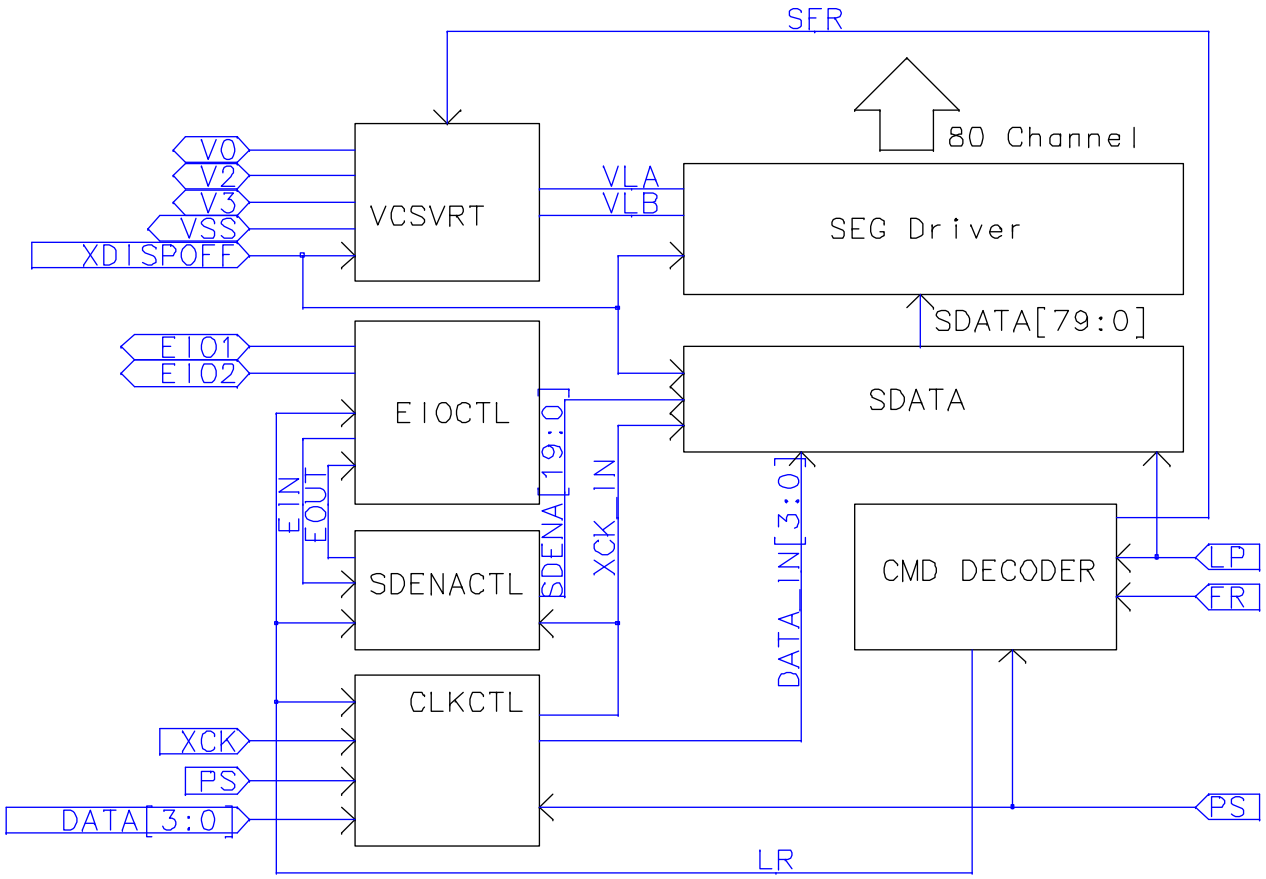
Pad No	Function	X	Y
37	CS[9]	-1785	665
38	CS[10]	-1785	555
39	CS[11]	-1785	450
40	CS[12]	-1785	350
41	CS[13]	-1785	250
42	CS[14]	-1785	150
43	CS[15]	-1785	50
44	CS[16]	-1785	-50
45	CS[17]	-1785	-150
46	CS[18]	-1785	-250
47	CS[19]	-1785	-350
48	CS[20]	-1785	-450
49	CS[21]	-1785	-555
50	CS[22]	-1785	-665
51	CS[23]	-1665	-665
52	CS[24]	-1555	-665
53	CS[25]	-1450	-665
54	CS[26]	-1350	-665
55	CS[27]	-1250	-665
56	CS[28]	-1150	-665
57	CS[29]	-1050	-665
58	CS[30]	-950	-665
59	CS[31]	-850	-665
60	CS[32]	-750	-665
61	CS[33]	-650	-665
62	CS[34]	-550	-665
63	CS[35]	-450	-665
64	CS[36]	-350	-665
65	CS[37]	-250	-665
66	CS[38]	-150	-665
67	CS[39]	-50	-665
68	CS[40]	50	-665
69	CS[41]	150	-665
70	CS[42]	250	-665
71	CS[43]	350	-665
72	CS[44]	450	-665

Pad No	Function	X	Y
73	CS[45]	550	-665
74	CS[46]	650	-665
75	CS[47]	750	-665
76	CS[48]	850	-665
77	CS[49]	950	-665
78	CS[50]	1050	-665
79	CS[51]	1150	-665
80	CS[52]	1250	-665
81	CS[53]	1350	-665
82	CS[54]	1450	-665
83	CS[55]	1555	-665
84	CS[56]	1665	-665
85	CS[57]	1785	-665
86	CS[58]	1785	-555
87	CS[59]	1785	-450
88	CS[60]	1785	-350
89	CS[61]	1785	-250
90	CS[62]	1785	-150
91	CS[63]	1785	-50
92	CS[64]	1785	50
93	CS[65]	1785	150
94	CS[66]	1785	250
95	CS[67]	1785	350
96	CS[68]	1785	450
97	CS[69]	1785	555

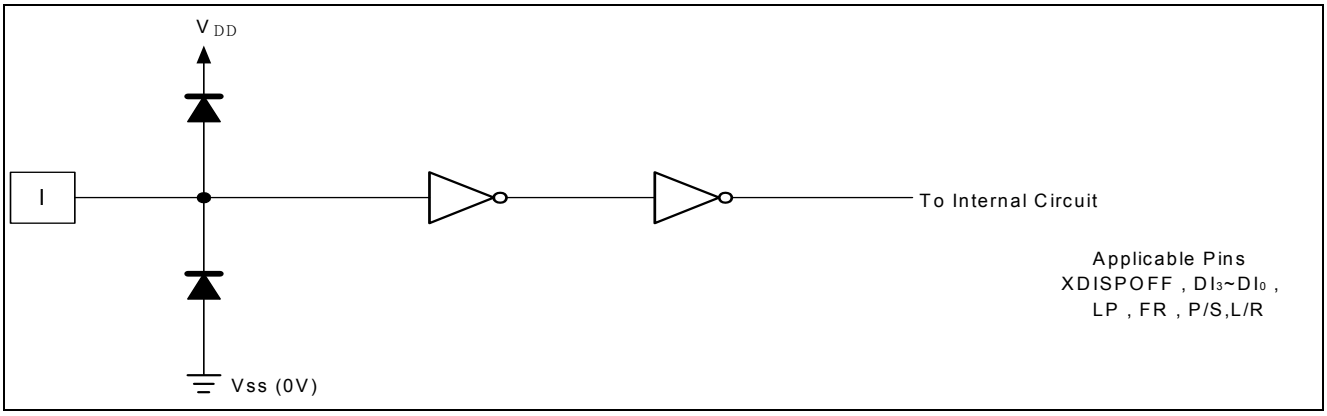
PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION	No of Num
SEG0-SEG79	O	LCD drive output	80
V0,V2,V3	P	Power supply for LCD drive	3
XDISPOFF	I	Control input for output of non-select level	1
VDD	P	Power supply for logic system (+2.5 to +5.5 V)	1
EIO2, EIO1	I/O	Input/output for chip selection at segment mode and FLM input output function at com/seg mix mode or common mode	2
DI0-DI3	I	Display data input at segment mode	4
XCK	I	Clock input for taking display data at segment mode	1
L/R	I	Display data shift direction selection	
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode	1
FR	I	AC-converting signal input for LCD drive waveform	1
P/S	I	This is the parallel data input/serial data input switch terminal. P/S=”H”: Parallel data input. P/S=”L”: Serial data input.	1
VSS	P	Ground (0 V)	1

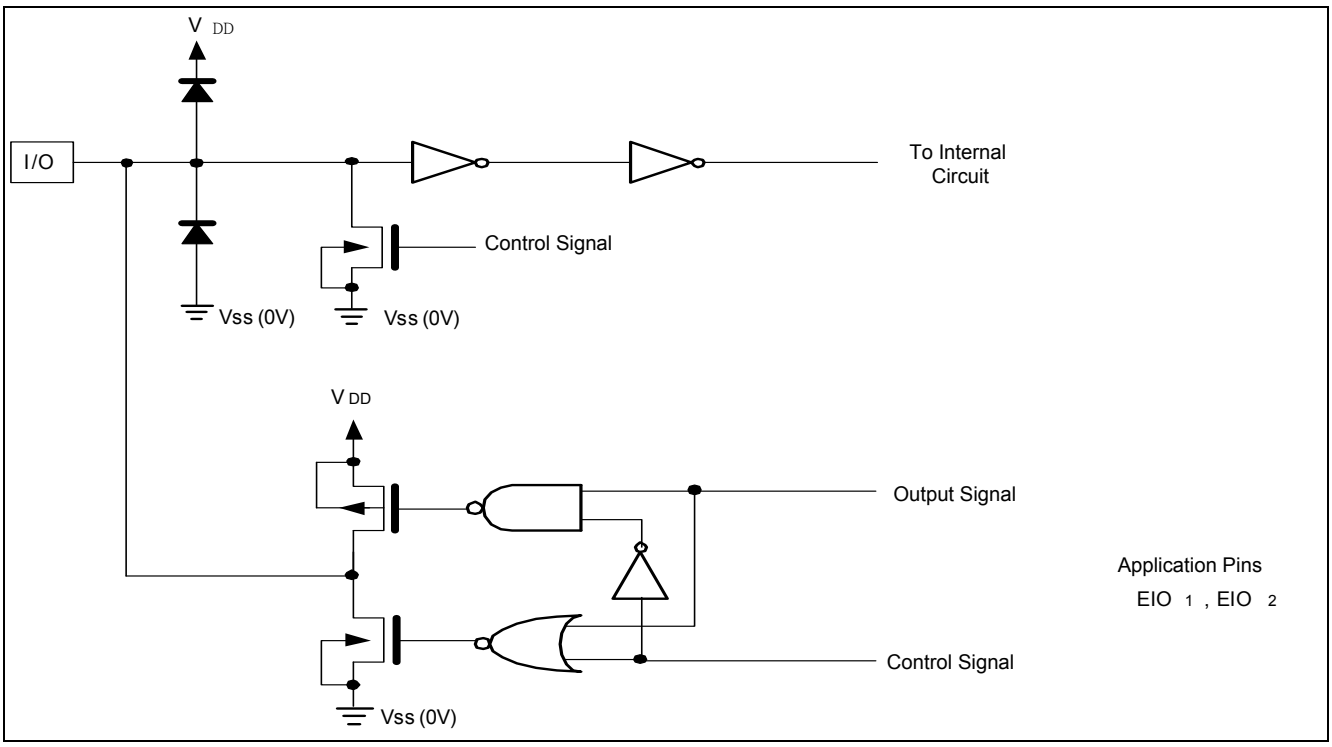
■ BLOCK DIAGRAM



INPUT/OUTPUT CIRCUITS



Input Circuit



Input/Output Circuit

■ FUNCTIONAL DESCRIPTION

◆ Pin Functions

SYMBOL	FUNCTION
VDD	Logic system power supply pin, connected to +2.5 to +5.5 V.
VSS	Ground pin, connected to 0 V.
V0 V2 V3	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below. • V0 ≧V2 ≧V3≧Vss
DI3-DI0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI3-DI0. • In serial input mode, input data into the 1 pin DI0. Connect DI3-DI1 to VSS or VDD • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data * Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
XDISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to VSS level "L", the LCD drive output pins (SEG0~SEG79) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V2 or V3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
P/S	Interface Mode selection pin • When P/S is “H” then parallel data input mode.

	When P/S is “L” the serial data input mode,
L/R	Input pin for selecting the reading direction of display data. **Default value is LOW** • When set to V_{SS} level "L", data is read sequentially from SEG_{79} to SEG_0. • When set to V_{DD} level "H", data is read sequentially from SEG_0 to SEG_{79}. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
EIO1, EIO2	Input/output pins for chip selection. AT segment mode: • When L/R input is at VSS level "L", EIO1 is set for output, and EIO2 is set for input(connect to Vss). • When L/R input is at VDD level "H", EIO1 is set for input(connect to Vss), and EIO2 is set for output. • During output, set to "H" while LP • XCK is "H" and after 80 bits of data have been read, set to "L” for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 80 bits of data have been read.
SEG0–SEG79	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V0, V2, V3, and Vss) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

◆ Functional Operations

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (SEG0-SEG79)
L	L	H	V3
L	H	H	Vss
H	L	H	V2
H	H	H	V0
X	X	L	Vss

TRUTH TABLE

NOTES:

- L : VSS (0 V), H : VDD (+2.5 to +5.5 V),
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage that is assigned by specification for each power pin.

◆ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(A) 4-bit Parallel Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				20 CLOCK	19 CLOCK	18 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI0	SEG0	SEG4	SEG8	…	SEG68	SEG72	SEG76
			DI1	SEG1	SEG5	SEG9	…	SEG69	SEG73	SEG77
			DI2	SEG2	SEG6	SEG10	…	SEG70	SEG74	SEG78
			DI3	SEG3	SEG7	SEG11	…	SEG71	SEG75	SEG79
H	Input	Output	DI0	SEG79	SEG75	SEG71	…	SEG11	SEG7	SEG3
			DI1	SEG78	SEG74	SEG70	…	SEG10	SEG6	SEG2
			DI2	SEG77	SEG73	SEG69	…	SEG9	SEG5	SEG1
			DI3	SEG76	SEG72	SEG68	…	SEG8	SEG4	SEG0

(B) Serial Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				80 CLOCK	79 CLOCK	78 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI0	SEG0	SEG1	SEG2	…	SEG77	SEG78	SEG79
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X
H	Input	Output	DI0	SEG79	SEG78	SEG77	…	SEG2	SEG1	SEG0
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X

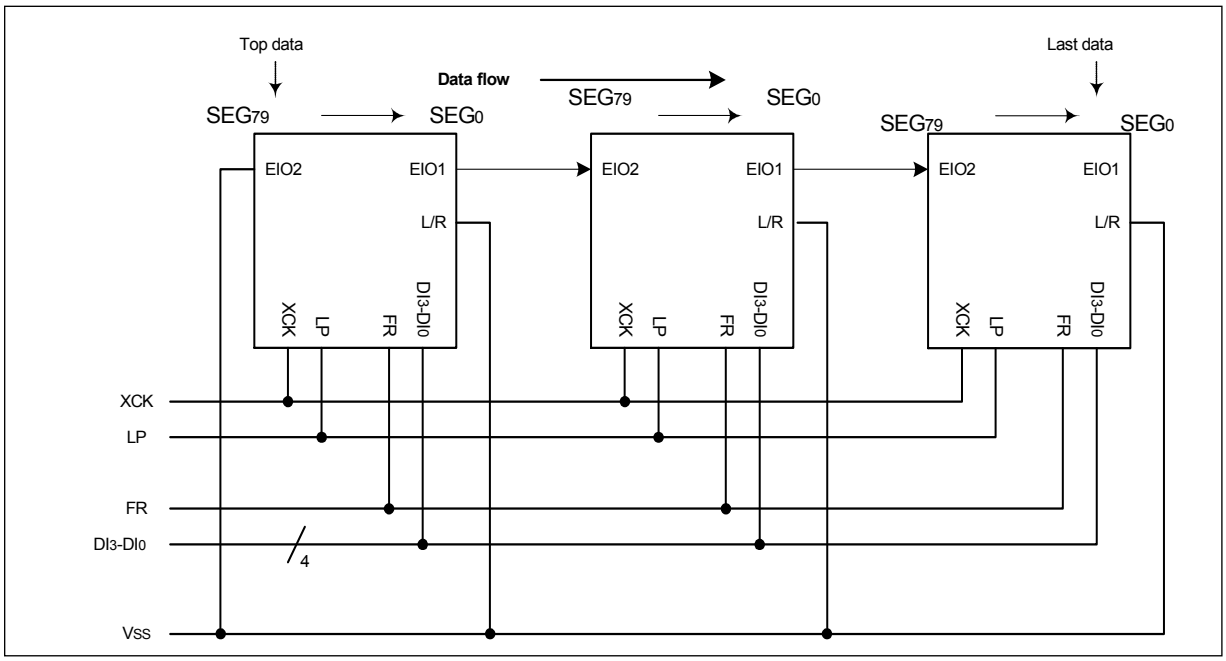
NOTES:

- L : VSS (0 V), H : VDD (+2.5 to +5.5 V), X : Don't care

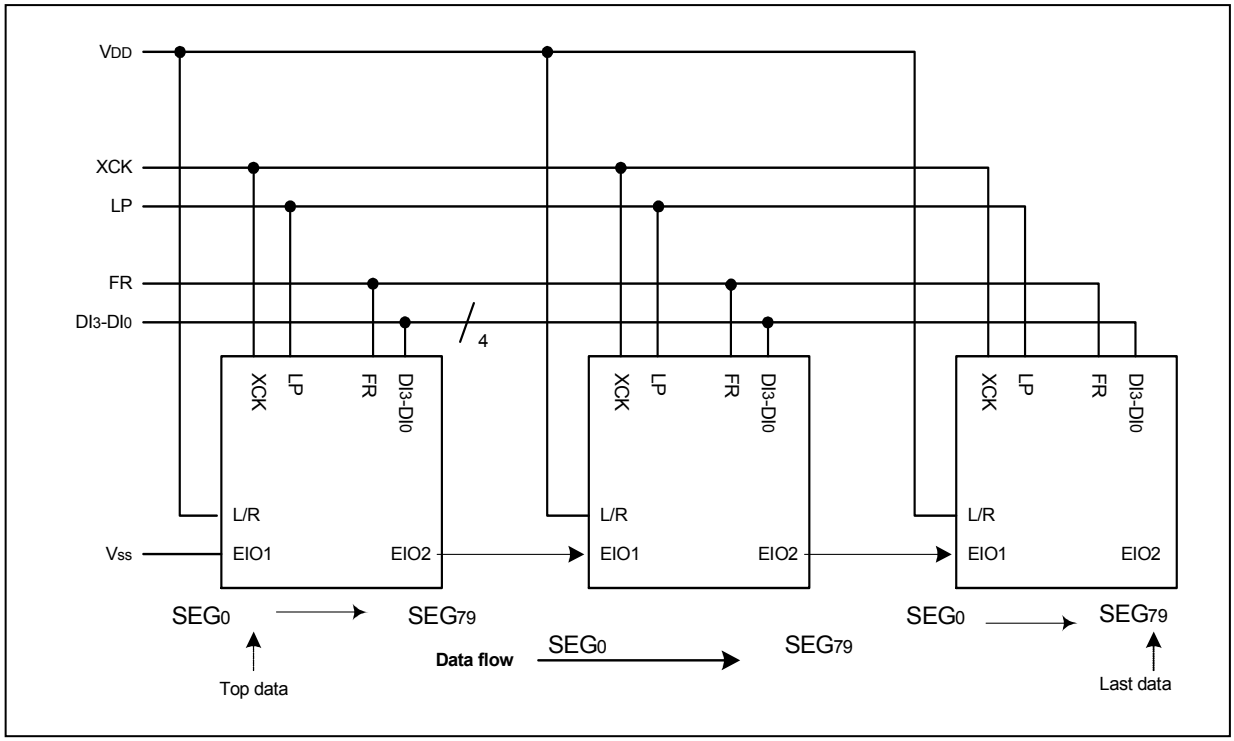
  "Don't care" should be fixed to "H" or "L", avoiding floating.

◆ Connection examples of plural segment drivers

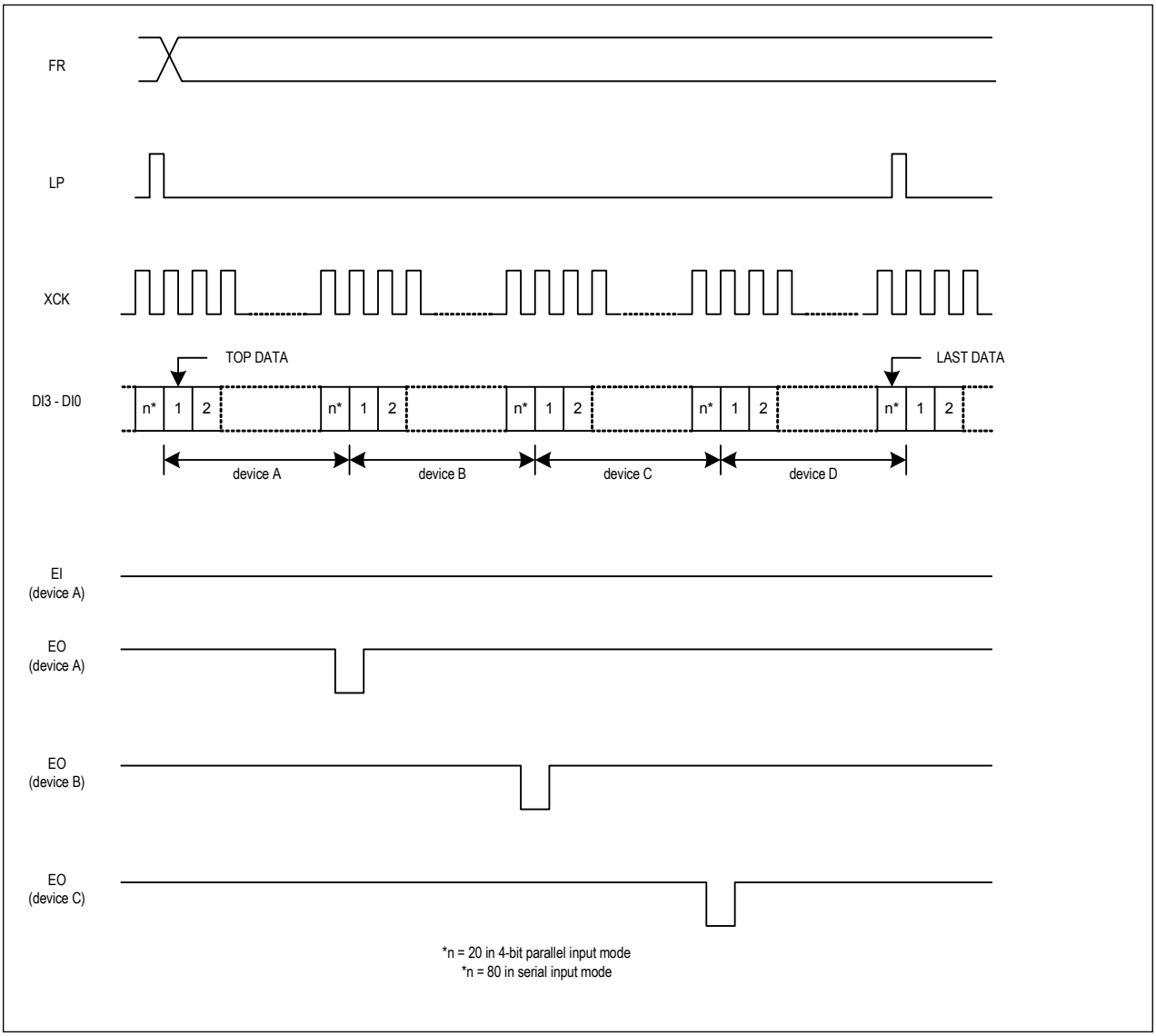
(A) When L/R = "L"



(B) When L/R = "H"



◆ Timing chart of 4-device cascade connection of segment drivers



◆ PRECAUTIONS

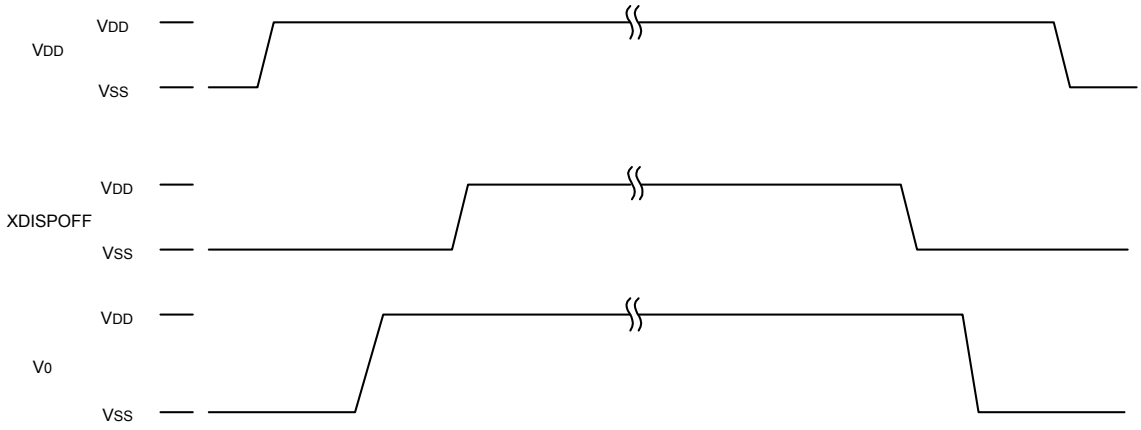
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power

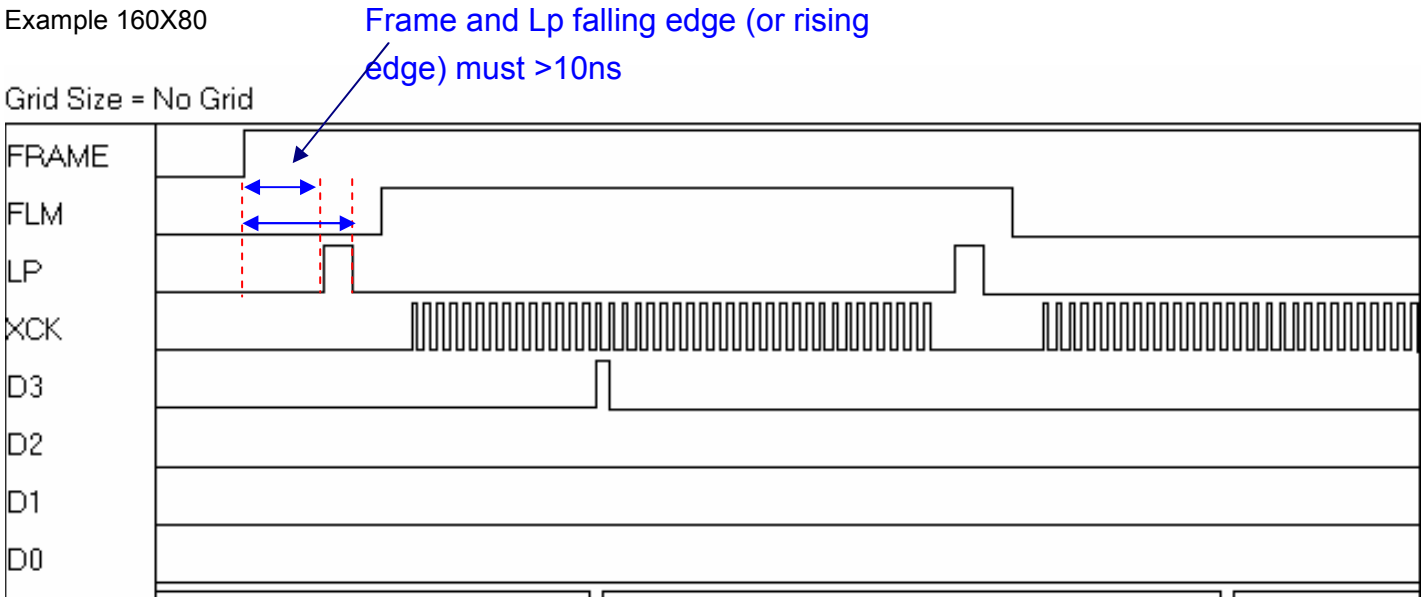
And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on XDISPOFF function. After that, cancel the XDISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level Vss on XDISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here

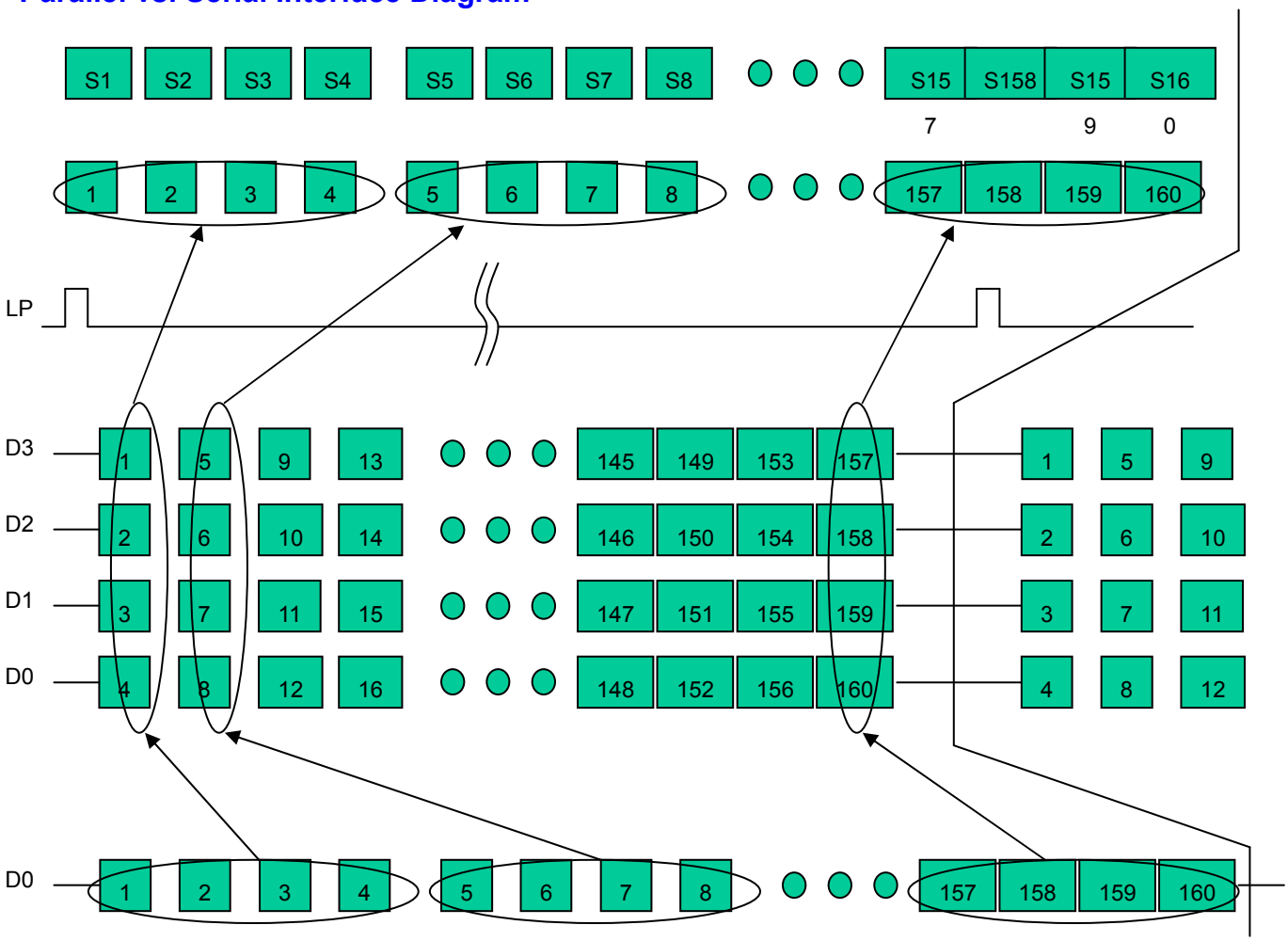


Application Timing Block:

Example 160X80



Parallel vs. Serial Interface Diagram



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3~+7.0	V	1,2
	V_2	V_2	V_{DD}-10~ V_{DD}+0.3		
	V_3	V_3	-0.3~V_{5S}+10	V	
Input voltage	V_I	$D1_4$-DI_0, XCK, LP, L/R, FR, EIO_1, EIO_2, XDISPOFF	-0.3 to V_{DD}+0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

■ RECOMMENDED OPERATING Conditions

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	VDD	VDD	+2.5		+5.5	V	1, 2
Supply voltage (2)	V0	V0	+6.0		+16.0	V	
Operating temperature	TOPR		-20		+85	°C	

NOTES:

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that V2 ≧V3 ≧VSS.

■ ELECTRICAL CHARACTERISTICS

◆ DC Characteristics

(V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	VIL		DI3-DI0, XCK, LP, L/R FR, EIO1, EIO2, XDISPOFF			0.2VDD	V	
Input "High" voltage	VIH			0.8VDD			V	
Output "Low" voltage	VOL	IOL = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	VOH	IOH = -0.4 mA		VDD-0.4			V	
Input leakage current	ILIL	VI = VSS	DI3-DI0, XCK, LP, LIR, FR, EIO1, EIO2, XDISPOFF			-10	μA	
	ILIH	VI = VDD				+10	μA	
Output resistance	RON	|ΔVON| =0.5V, V0 = 30 V	SEG0-SEG79		1.5	2.0	kΩ	
Standby current	ISTB		VSS			50	μA	1
Supply current (1) (Non-selection)	ISS		VSS			2.0	mA	2
Supply current (2)	I0		V0			0.9	mA	4

NOTES:

1. V_{DD} = +3.0 V, V_0 = +12.0 V
2. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{SS}. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

◆ AC Characteristics

(V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 11ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES: 1. Takes the cascade connection into consideration.

2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	tWCK	tR,tF ≤ 10ns	66			ns	1
Shift clock "H" pulse width	tWCKH		23			ns	
Shift clock "L" pulse width	tWCKL		23			ns	
Data setup time	tDS		15			ns	
Data hold time	tDH		23			ns	
Latch pulse "H" pulse width	tWLPH		30			ns	
Shift clock rise to latch pulse rise time	tLD		0			ns	
Shift clock fall to latch pulse fall time	tSL		50			ns	
Latch pulse rise to shift clock rise time	tLS		30			ns	
Latch pulse fall to shift clock fall time	tLH		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	tS		15			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
DISPOFF removal time	tSD		100			ns	
DISPOFF "L" pulse width	tWDL		1.2			µs	
Output delay time (1)	tD	CL = 15 pF			41	ns	
Output delay time (2)	tPD1, tPD2	CL = 15 pF			1.2	µs	
Output delay time (3)	tPD3	CL = 15 pF			1.2	µs	

NOTES:1. Takes the cascade connection into consideration.

2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

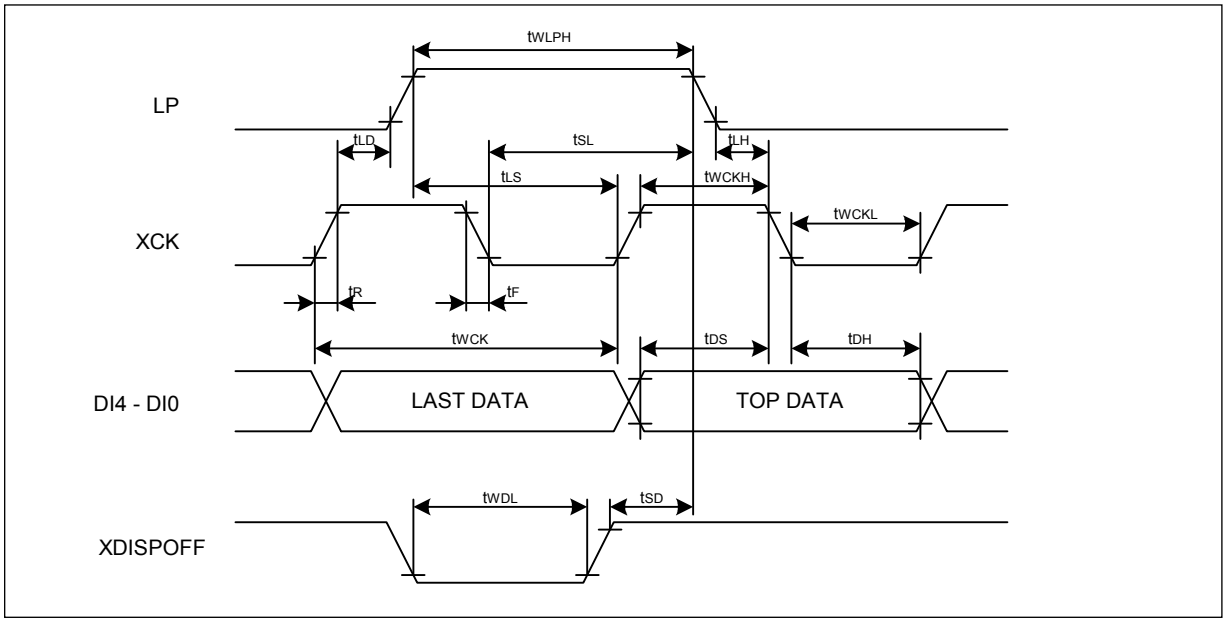
(V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

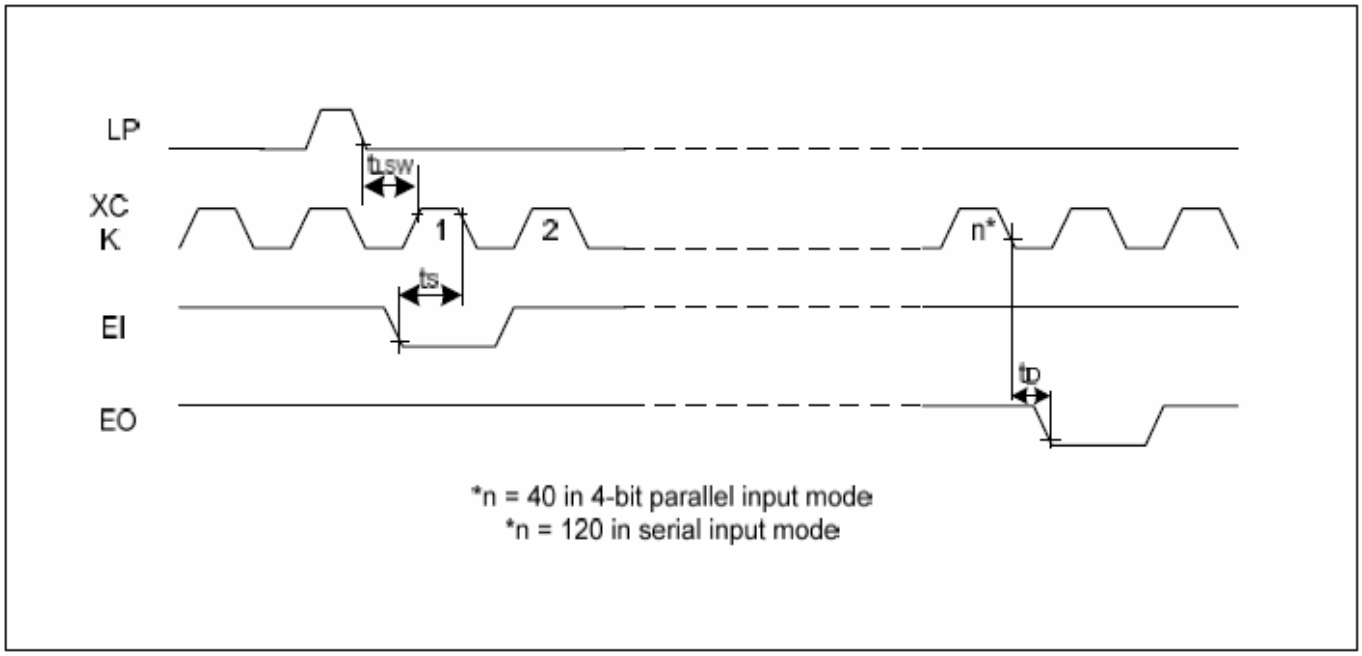
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

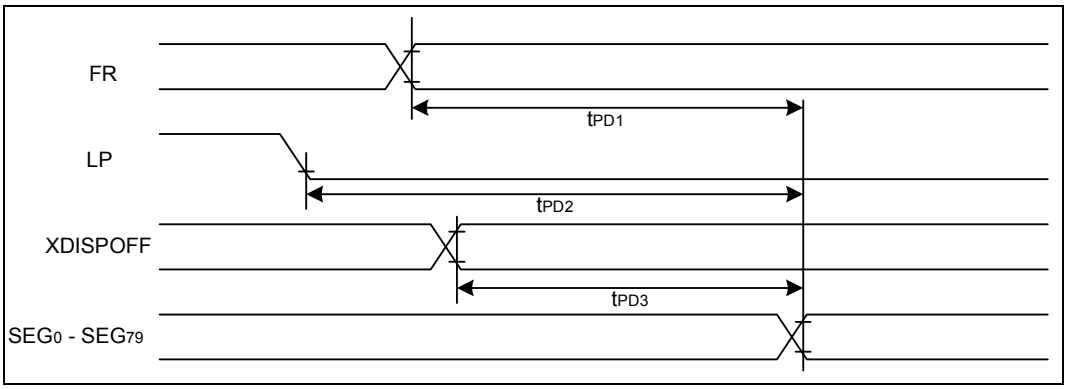
NOTES:1. Takes the cascade connection into consideration.

2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

◆ Timing Chart of Segment Mode

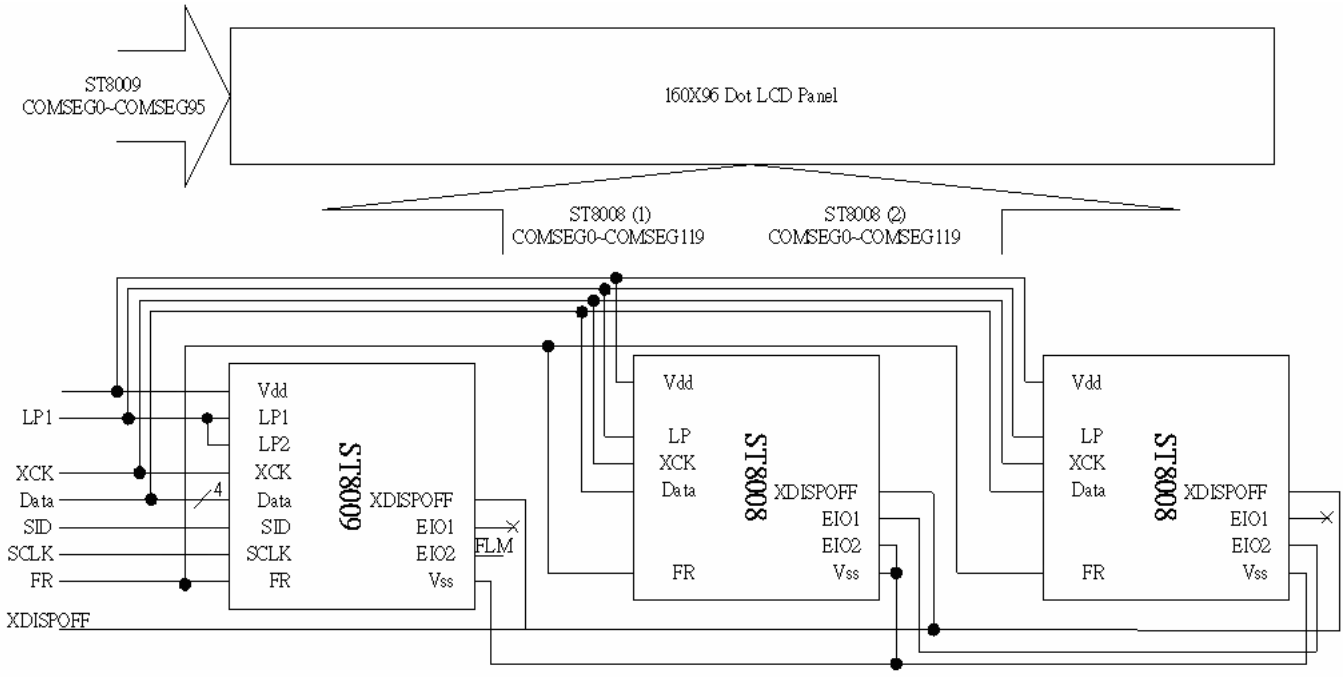






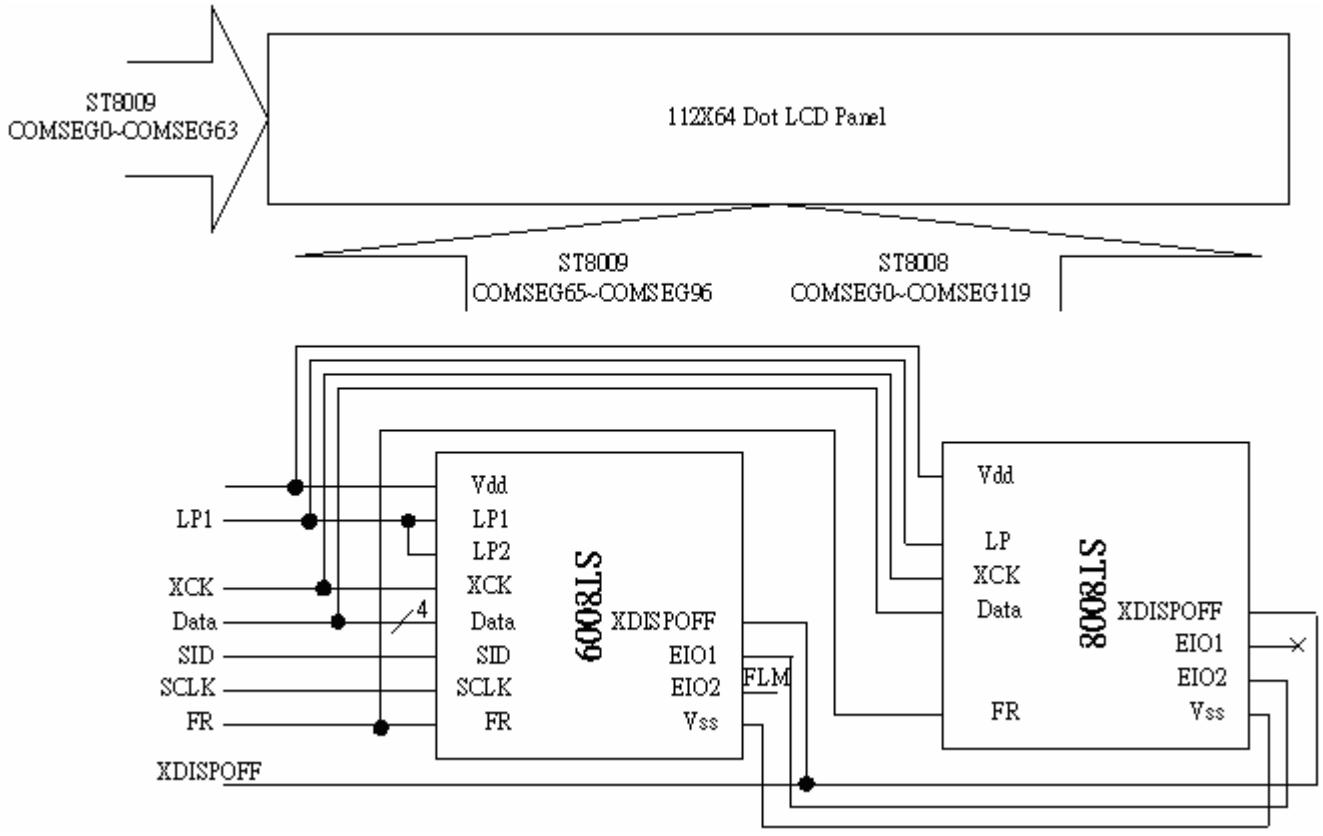
Application Circuit

(a) When use one ST8009 and two ST8008 (160X96)



Note: L/R select Vss

(b) When use one ST8009 and one ST8008 (112X64)



ST8008 Serial Specification Revision History

ST8008 Serial Specification Revision History		
Version	**Date**	**Description**
0.0	**2004/01/05**	**Preliminary version**
0.1	**2004/04/05**	**Add application timing block diagram**
0.2	**2004/09/08**	**Define timing of segment mode .**
0.3	**2005/02/14**	**Revise graph of ST8008(SID, SCLK)**