Sitronix

ST7598

344 x 88 Dot Matrix LCD Controller/Driver

INTRODUCTION

ST7598 is a single-chip LSI for graphic dot-matrix LCD systems. It incorporates power system, LCD controller and drivers for common/segment outputs. ST7598 can be connected directly to a microprocessor with 8-bit parallel interface or 4-line serial interface (SPI-4) or 3-line serial interface (SPI-3). Display data sent from MCU is stored into internal Display Data RAM (DDRAM) of 344x88 bits. ST7598 contains 344 segment-output and 88 common-output. The display data bits in DDRAM are directly related to the pixels on LCD panel. With built-in oscillation circuit and low power consumption power circuits, ST7598 can drive LCD panel without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

- 344 segment outputs / 88 common outputs

On-chip Display Data RAM

- Capacity: 344 x 88 = 30,272 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MCU
- 4-Line serial interface (8-bit)
- 3-Line serial interface (9-bit)
- Temperature / PROM data (register value) can be read by 8-bit parallel and 4-Line/3-Line serial interface

External RSTB (Hardware Reset) Pin

On-chip Oscillator Circuit

- Internal oscillator requires no external component (external clock input is also supported)

On-chip Low Power Analog Circuit

- Voltage booster with external boost-capacitors
- Built-in voltage regulator with programmable contrast
- Built-in PROM (Programmable Read-Only Memory) for V3 fine tune (3 times programmable)
- Built-in voltage follower supports LCD bias voltage
  Available bias : 1/6 ~ 1/13
- Support external power supply

Display Function

- Support interlace-scanning method
- N-lines inversion
- Programmable temperature compensation: 16-slopes from -40~87℃ (16-sections, 8℃/section)

Operating Voltage Range

- Digital Power (VDD1, VDD3): 3.0V ~ 5.0V (TYP.)
- Analog Power (VDD2): 3.0V ~ 5.0V (TYP.)

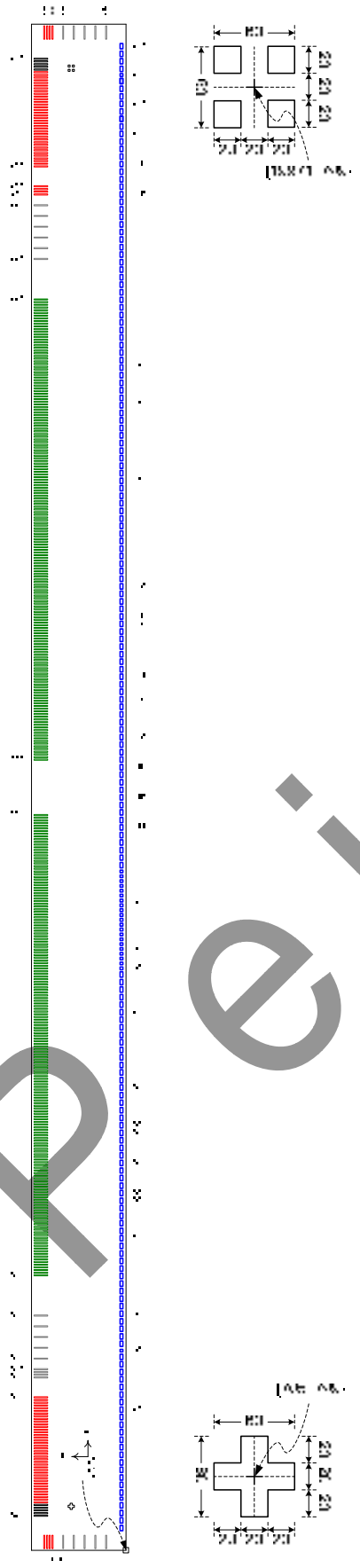
LCD Operating Voltage Range

- Maximum Vop: 22.2V (Vop=V3-MV3, i.e. V3=11.1V)

Package Type: COG & COF

ST7598	6800, 8080, 4-Line & 3-Line Interface	ST

PAD ARRANGEMENT



Chip Size: 20706 x 1276 (+/- 15) Unit: um

Chip Thickness	480	Bump Height	15
PAD		**Bump Size**	
1~9, 216~224		96 x 26	
10~13, 15~33, 35~84, 106~210, 212~215		80 x 45	
14, 34, 85~105, 211		30 x 45	
225~673		26 x 96	
PAD		**Minimal Pitch**	
1~9, 216~224, 225~673		40	
10~215		52.5	
* Refer to “PAD CENTER COORDINATES” for ITO layout			

PAD CENTER COORDINATES

PAD	NAME	X	Y
1	COM[3]	64.5	1163
2	COM[2]	64.5	1123
3	COM[1]	64.5	1083
4	COM[0]	64.5	1043
5	Reserve	64.5	883
6	Reserve	64.5	723
7	Reserve	64.5	563
8	Reserve	64.5	403
9	Reserve	64.5	243
10	Dummy	205.5	39
11	Dummy	310.5	39
12	Dummy	415.5	39
13	Dummy	520.5	39
14	Dummy	599.25	39
15	VPP	678	39
16	VPP	783	39
17	EXTB	888	39
18	T20	993	39
19	T19	1098	39
20	T18	1203	39
21	CSB	1308	39
22	RSTB	1413	39
23	A0	1518	39
24	RWR	1623	39
25	ERD	1728	39
26	D0	1833	39
27	D1	1938	39
28	D2	2043	39
29	D3	2148	39
30	D4	2253	39
31	D5	2358	39
32	D6	2463	39
33	D7	2568	39
34	VSS	2646.75	39
35	MODE	2725.5	39
36	CLS	2830.5	39
37	IF2	2935.5	39
38	IF1	3040.5	39
39	VDD2	3145.5	39
40	VDD2	3250.5	39
41	VDD2	3355.5	39
42	VDD2	3460.5	39
43	VDD2	3565.5	39
44	VDD2	3670.5	39
45	VDD2	3775.5	39
46	VDD2	3880.5	39

PAD	NAME	X	Y
47	VDD2	3985.5	39
48	VDD2	4090.5	39
49	VDD	4195.5	39
50	VDD	4300.5	39
51	VDD	4405.5	39
52	VDD	4510.5	39
53	VDD	4615.5	39
54	VDD3	4720.5	39
55	VD1O	4825.5	39
56	VD1O	4930.5	39
57	VD1O	5035.5	39
58	VD1O	5140.5	39
59	VD1I	5245.5	39
60	VD1I	5350.5	39
61	VD1I	5455.5	39
62	VD1I	5560.5	39
63	VSS3	5665.5	39
64	VSS	5770.5	39
65	VSS	5875.5	39
66	VSS	5980.5	39
67	VSS	6085.5	39
68	VSS	6190.5	39
69	VSS2	6295.5	39
70	VSS2	6400.5	39
71	VSS2	6505.5	39
72	VSS2	6610.5	39
73	VSS2	6715.5	39
74	VSS2	6820.5	39
75	VSS2	6925.5	39
76	VSS2	7030.5	39
77	VSS2	7135.5	39
78	VSS2	7240.5	39
79	VC	7345.5	39
80	VC	7450.5	39
81	VC	7555.5	39
82	VC	7660.5	39
83	VC	7765.5	39
84	VC	7870.5	39
85	T17	7949.25	39
86	T16	8001.75	39
87	T15	8054.25	39
88	T14	8106.75	39
89	TFCOM0	8159.25	39
90	T13	8211.75	39
91	T12	8264.25	39
92	T11	8316.75	39

PAD	NAME	X	Y
93	T10	8369.25	39
94	T9	8421.75	39
95	T8	8474.25	39
96	T7	8526.75	39
97	T6	8579.25	39
98	TFCOM1	8631.75	39
99	T5	8684.25	39
100	T4	8736.75	39
101	T3	8789.25	39
102	T2	8841.75	39
103	T1	8894.25	39
104	T0	8946.75	39
105	VREF	8999.25	39
106	TCAP	9078	39
107	V2	9183	39
108	V2	9288	39
109	V2	9393	39
110	V2	9498	39
111	V1	9603	39
112	V1	9708	39
113	V1	9813	39
114	V1	9918	39
115	MV1	10023	39
116	MV1	10128	39
117	MV1	10233	39
118	MV1	10338	39
119	MV2	10443	39
120	MV2	10548	39
121	MV2	10653	39
122	MV2	10758	39
123	V3I	10863	39
124	V3I	10968	39
125	V3I	11073	39
126	V3I	11178	39
127	V3S	11283	39
128	V3O	11388	39
129	V3O	11493	39
130	V3O	11598	39
131	MV3OI	11703	39
132	MV3OI	11808	39
133	MV3OI	11913	39
134	MV3OI	12018	39
135	MV3OI	12123	39
136	MV3OI	12228	39
137	MV3OI	12333	39
138	MV3S	12438	39
139	CB1P	12543	39
140	CB1P	12648	39

PAD	NAME	X	Y
141	CB1P	12753	39
142	CB1P	12858	39
143	CB1N	12963	39
144	CB1N	13068	39
145	CB1N	13173	39
146	CB1N	13278	39
147	AVDD	13383	39
148	AVDD	13488	39
149	AVDD	13593	39
150	AVDD	13698	39
151	AVDD	13803	39
152	AVDD	13908	39
153	AVDD	14013	39
154	AVDD	14118	39
155	AVDD	14223	39
156	AVDD	14328	39
157	CA1P	14433	39
158	CA1P	14538	39
159	CA1P	14643	39
160	CA1P	14748	39
161	CA1P	14853	39
162	CA1P	14958	39
163	CA1P	15063	39
164	CA1P	15168	39
165	CA1P	15273	39
166	CA1P	15378	39
167	CA1N	15483	39
168	CA1N	15588	39
169	CA1N	15693	39
170	CA1N	15798	39
171	CA1N	15903	39
172	CA2P	16008	39
173	CA2P	16113	39
174	CA2P	16218	39
175	CA2P	16323	39
176	CA2P	16428	39
177	CA2P	16533	39
178	CA2P	16638	39
179	CA2P	16743	39
180	CA2P	16848	39
181	CA2P	16953	39
182	CA2N	17058	39
183	CA2N	17163	39
184	CA2N	17268	39
185	CA2N	17373	39
186	CA2N	17478	39
187	NAVDD	17583	39
188	NAVDD	17688	39

PAD	NAME	X	Y
189	NAVDD	17793	39
190	NAVDD	17898	39
191	NAVDD	18003	39
192	NAVDD	18108	39
193	NAVDD	18213	39
194	NAVDD	18318	39
195	CD1P	18423	39
196	CD1P	18528	39
197	CD1P	18633	39
198	CD1P	18738	39
199	CD1N	18843	39
200	CD1N	18948	39
201	CD1N	19053	39
202	CD1N	19158	39
203	CD2P	19263	39
204	CD2P	19368	39
205	CD2P	19473	39
206	CD2P	19578	39
207	CD2N	19683	39
208	CD2N	19788	39
209	CD2N	19893	39
210	CD2N	19998	39
211	Dummy	20076.75	39
212	Dummy	20155.5	39
213	Dummy	20260.5	39
214	Dummy	20365.5	39
215	Dummy	20470.5	39
216	Reserve	20611.5	243
217	Reserve	20611.5	403
218	Reserve	20611.5	563
219	Reserve	20611.5	723
220	Reserve	20611.5	883
221	COM[4]	20611.5	1043
222	COM[5]	20611.5	1083
223	COM[6]	20611.5	1123
224	COM[7]	20611.5	1163
225	Dummy	20364.49	1181.5
226	Dummy	20324.49	1181.5
227	Dummy	20284.49	1181.5
228	Dummy	20244.49	1181.5
229	Dummy	20204.49	1181.5
230	COM[12]	20164.49	1181.5
231	COM[13]	20124.49	1181.5
232	COM[14]	20084.49	1181.5
233	COM[15]	20044.49	1181.5
234	COM[20]	20004.49	1181.5
235	COM[21]	19964.49	1181.5
236	COM[22]	19924.49	1181.5

PAD	NAME	X	Y
237	COM[23]	19884.49	1181.5
238	COM[28]	19844.49	1181.5
239	COM[29]	19804.49	1181.5
240	COM[30]	19764.49	1181.5
241	COM[31]	19724.49	1181.5
242	COM[36]	19684.49	1181.5
243	COM[37]	19644.49	1181.5
244	COM[38]	19604.49	1181.5
245	COM[39]	19564.49	1181.5
246	COM[44]	19524.49	1181.5
247	COM[45]	19484.49	1181.5
248	COM[46]	19444.49	1181.5
249	COM[47]	19404.49	1181.5
250	COM[52]	19364.49	1181.5
251	COM[53]	19324.49	1181.5
252	COM[54]	19284.49	1181.5
253	COM[55]	19244.49	1181.5
254	COM[60]	19204.49	1181.5
255	COM[61]	19164.49	1181.5
256	COM[62]	19124.49	1181.5
257	COM[63]	19084.49	1181.5
258	COM[68]	19044.49	1181.5
259	COM[69]	19004.49	1181.5
260	COM[70]	18964.49	1181.5
261	COM[71]	18924.49	1181.5
262	COM[76]	18884.49	1181.5
263	COM[77]	18844.49	1181.5
264	COM[78]	18804.49	1181.5
265	COM[79]	18764.49	1181.5
266	COM[84]	18644.24	1181.5
267	COM[85]	18604.24	1181.5
268	COM[86]	18564.24	1181.5
269	COM[87]	18524.24	1181.5
270	Reserve	18364.24	1181.5
271	Reserve	18204.24	1181.5
272	Reserve	18044.24	1181.5
273	Reserve	17884.24	1181.5
274	Reserve	17724.24	1181.5
275	Reserve	17564.24	1181.5
276	SEG[343]	17301.57	1181.5
277	SEG[342]	17261.57	1181.5
278	SEG[341]	17221.57	1181.5
279	SEG[340]	17181.57	1181.5
280	SEG[339]	17141.57	1181.5
281	SEG[338]	17101.57	1181.5
282	SEG[337]	17061.57	1181.5
283	SEG[336]	17021.57	1181.5
284	SEG[335]	16981.57	1181.5

PAD	NAME	X	Y
285	SEG[334]	16941.57	1181.5
286	SEG[333]	16901.57	1181.5
287	SEG[332]	16861.57	1181.5
288	SEG[331]	16821.57	1181.5
289	SEG[330]	16781.57	1181.5
290	SEG[329]	16741.57	1181.5
291	SEG[328]	16701.57	1181.5
292	SEG[327]	16661.57	1181.5
293	SEG[326]	16621.57	1181.5
294	SEG[325]	16581.57	1181.5
295	SEG[324]	16541.57	1181.5
296	SEG[323]	16501.57	1181.5
297	SEG[322]	16461.57	1181.5
298	SEG[321]	16421.57	1181.5
299	SEG[320]	16381.57	1181.5
300	SEG[319]	16341.57	1181.5
301	SEG[318]	16301.57	1181.5
302	SEG[317]	16261.57	1181.5
303	SEG[316]	16221.57	1181.5
304	SEG[315]	16181.57	1181.5
305	SEG[314]	16141.57	1181.5
306	SEG[313]	16101.57	1181.5
307	SEG[312]	16061.57	1181.5
308	SEG[311]	16021.57	1181.5
309	SEG[310]	15981.57	1181.5
310	SEG[309]	15941.57	1181.5
311	SEG[308]	15901.57	1181.5
312	SEG[307]	15861.57	1181.5
313	SEG[306]	15821.57	1181.5
314	SEG[305]	15781.57	1181.5
315	SEG[304]	15741.57	1181.5
316	SEG[303]	15701.57	1181.5
317	SEG[302]	15661.57	1181.5
318	SEG[301]	15621.57	1181.5
319	SEG[300]	15581.57	1181.5
320	SEG[299]	15541.57	1181.5
321	SEG[298]	15501.57	1181.5
322	SEG[297]	15461.57	1181.5
323	SEG[296]	15421.57	1181.5
324	SEG[295]	15381.57	1181.5
325	SEG[294]	15341.57	1181.5
326	SEG[293]	15301.57	1181.5
327	SEG[292]	15261.57	1181.5
328	SEG[291]	15221.57	1181.5
329	SEG[290]	15181.57	1181.5
330	SEG[289]	15141.57	1181.5
331	SEG[288]	15101.57	1181.5
332	SEG[287]	15061.57	1181.5

PAD	NAME	X	Y
333	SEG[286]	15021.57	1181.5
334	SEG[285]	14981.57	1181.5
335	SEG[284]	14941.57	1181.5
336	SEG[283]	14901.57	1181.5
337	SEG[282]	14861.57	1181.5
338	SEG[281]	14821.57	1181.5
339	SEG[280]	14781.57	1181.5
340	SEG[279]	14741.57	1181.5
341	SEG[278]	14701.57	1181.5
342	SEG[277]	14661.57	1181.5
343	SEG[276]	14621.57	1181.5
344	SEG[275]	14581.57	1181.5
345	SEG[274]	14541.57	1181.5
346	SEG[273]	14501.57	1181.5
347	SEG[272]	14461.57	1181.5
348	SEG[271]	14421.57	1181.5
349	SEG[270]	14381.57	1181.5
350	SEG[269]	14341.57	1181.5
351	SEG[268]	14301.57	1181.5
352	SEG[267]	14261.57	1181.5
353	SEG[266]	14221.57	1181.5
354	SEG[265]	14181.57	1181.5
355	SEG[264]	14141.57	1181.5
356	SEG[263]	14101.57	1181.5
357	SEG[262]	14061.57	1181.5
358	SEG[261]	14021.57	1181.5
359	SEG[260]	13981.57	1181.5
360	SEG[259]	13941.57	1181.5
361	SEG[258]	13901.57	1181.5
362	SEG[257]	13861.57	1181.5
363	SEG[256]	13821.57	1181.5
364	SEG[255]	13781.57	1181.5
365	SEG[254]	13741.57	1181.5
366	SEG[253]	13701.57	1181.5
367	SEG[252]	13661.57	1181.5
368	SEG[251]	13621.57	1181.5
369	SEG[250]	13581.57	1181.5
370	SEG[249]	13541.57	1181.5
371	SEG[248]	13501.57	1181.5
372	SEG[247]	13461.57	1181.5
373	SEG[246]	13421.57	1181.5
374	SEG[245]	13381.57	1181.5
375	SEG[244]	13341.57	1181.5
376	SEG[243]	13301.57	1181.5
377	SEG[242]	13261.57	1181.5
378	SEG[241]	13221.57	1181.5
379	SEG[240]	13181.57	1181.5
380	SEG[239]	13141.57	1181.5

PAD	NAME	X	Y
381	SEG[238]	13101.57	1181.5
382	SEG[237]	13061.57	1181.5
383	SEG[236]	13021.57	1181.5
384	SEG[235]	12981.57	1181.5
385	SEG[234]	12941.57	1181.5
386	SEG[233]	12901.57	1181.5
387	SEG[232]	12861.57	1181.5
388	SEG[231]	12821.57	1181.5
389	SEG[230]	12781.57	1181.5
390	SEG[229]	12741.57	1181.5
391	SEG[228]	12701.57	1181.5
392	SEG[227]	12661.57	1181.5
393	SEG[226]	12621.57	1181.5
394	SEG[225]	12581.57	1181.5
395	SEG[224]	12541.57	1181.5
396	SEG[223]	12501.57	1181.5
397	SEG[222]	12461.57	1181.5
398	SEG[221]	12421.57	1181.5
399	SEG[220]	12381.57	1181.5
400	SEG[219]	12341.57	1181.5
401	SEG[218]	12301.57	1181.5
402	SEG[217]	12261.57	1181.5
403	SEG[216]	12221.57	1181.5
404	SEG[215]	12181.57	1181.5
405	SEG[214]	12141.57	1181.5
406	SEG[213]	12101.57	1181.5
407	SEG[212]	12061.57	1181.5
408	SEG[211]	12021.57	1181.5
409	SEG[210]	11981.57	1181.5
410	SEG[209]	11941.57	1181.5
411	SEG[208]	11901.57	1181.5
412	SEG[207]	11861.57	1181.5
413	SEG[206]	11821.57	1181.5
414	SEG[205]	11781.57	1181.5
415	SEG[204]	11741.57	1181.5
416	SEG[203]	11701.57	1181.5
417	SEG[202]	11661.57	1181.5
418	SEG[201]	11621.57	1181.5
419	SEG[200]	11581.57	1181.5
420	SEG[199]	11541.57	1181.5
421	SEG[198]	11501.57	1181.5
422	SEG[197]	11461.57	1181.5
423	SEG[196]	11421.57	1181.5
424	SEG[195]	11381.57	1181.5
425	SEG[194]	11341.57	1181.5
426	SEG[193]	11301.57	1181.5
427	SEG[192]	11261.57	1181.5
428	SEG[191]	11221.57	1181.5

PAD	NAME	X	Y
429	SEG[190]	11181.57	1181.5
430	SEG[189]	11141.57	1181.5
431	SEG[188]	11101.57	1181.5
432	SEG[187]	11061.57	1181.5
433	SEG[186]	11021.57	1181.5
434	SEG[185]	10981.57	1181.5
435	SEG[184]	10941.57	1181.5
436	SEG[183]	10901.57	1181.5
437	SEG[182]	10861.57	1181.5
438	SEG[181]	10821.57	1181.5
439	SEG[180]	10781.57	1181.5
440	SEG[179]	10741.57	1181.5
441	SEG[178]	10701.57	1181.5
442	SEG[177]	10661.57	1181.5
443	SEG[176]	10621.57	1181.5
444	SEG[175]	10581.57	1181.5
445	SEG[174]	10541.57	1181.5
446	SEG[173]	10501.57	1181.5
447	SEG[172]	10461.57	1181.5
448	SEG[171]	10214.43	1181.5
449	SEG[170]	10174.43	1181.5
450	SEG[169]	10134.43	1181.5
451	SEG[168]	10094.43	1181.5
452	SEG[167]	10054.43	1181.5
453	SEG[166]	10014.43	1181.5
454	SEG[165]	9974.43	1181.5
455	SEG[164]	9934.43	1181.5
456	SEG[163]	9894.43	1181.5
457	SEG[162]	9854.43	1181.5
458	SEG[161]	9814.43	1181.5
459	SEG[160]	9774.43	1181.5
460	SEG[159]	9734.43	1181.5
461	SEG[158]	9694.43	1181.5
462	SEG[157]	9654.43	1181.5
463	SEG[156]	9614.43	1181.5
464	SEG[155]	9574.43	1181.5
465	SEG[154]	9534.43	1181.5
466	SEG[153]	9494.43	1181.5
467	SEG[152]	9454.43	1181.5
468	SEG[151]	9414.43	1181.5
469	SEG[150]	9374.43	1181.5
470	SEG[149]	9334.43	1181.5
471	SEG[148]	9294.43	1181.5
472	SEG[147]	9254.43	1181.5
473	SEG[146]	9214.43	1181.5
474	SEG[145]	9174.43	1181.5
475	SEG[144]	9134.43	1181.5
476	SEG[143]	9094.43	1181.5

PAD	NAME	X	Y
477	SEG[142]	9054.43	1181.5
478	SEG[141]	9014.43	1181.5
479	SEG[140]	8974.43	1181.5
480	SEG[139]	8934.43	1181.5
481	SEG[138]	8894.43	1181.5
482	SEG[137]	8854.43	1181.5
483	SEG[136]	8814.43	1181.5
484	SEG[135]	8774.43	1181.5
485	SEG[134]	8734.43	1181.5
486	SEG[133]	8694.43	1181.5
487	SEG[132]	8654.43	1181.5
488	SEG[131]	8614.43	1181.5
489	SEG[130]	8574.43	1181.5
490	SEG[129]	8534.43	1181.5
491	SEG[128]	8494.43	1181.5
492	SEG[127]	8454.43	1181.5
493	SEG[126]	8414.43	1181.5
494	SEG[125]	8374.43	1181.5
495	SEG[124]	8334.43	1181.5
496	SEG[123]	8294.43	1181.5
497	SEG[122]	8254.43	1181.5
498	SEG[121]	8214.43	1181.5
499	SEG[120]	8174.43	1181.5
500	SEG[119]	8134.43	1181.5
501	SEG[118]	8094.43	1181.5
502	SEG[117]	8054.43	1181.5
503	SEG[116]	8014.43	1181.5
504	SEG[115]	7974.43	1181.5
505	SEG[114]	7934.43	1181.5
506	SEG[113]	7894.43	1181.5
507	SEG[112]	7854.43	1181.5
508	SEG[111]	7814.43	1181.5
509	SEG[110]	7774.43	1181.5
510	SEG[109]	7734.43	1181.5
511	SEG[108]	7694.43	1181.5
512	SEG[107]	7654.43	1181.5
513	SEG[106]	7614.43	1181.5
514	SEG[105]	7574.43	1181.5
515	SEG[104]	7534.43	1181.5
516	SEG[103]	7494.43	1181.5
517	SEG[102]	7454.43	1181.5
518	SEG[101]	7414.43	1181.5
519	SEG[100]	7374.43	1181.5
520	SEG[99]	7334.43	1181.5
521	SEG[98]	7294.43	1181.5
522	SEG[97]	7254.43	1181.5
523	SEG[96]	7214.43	1181.5
524	SEG[95]	7174.43	1181.5

PAD	NAME	X	Y
525	SEG[94]	7134.43	1181.5
526	SEG[93]	7094.43	1181.5
527	SEG[92]	7054.43	1181.5
528	SEG[91]	7014.43	1181.5
529	SEG[90]	6974.43	1181.5
530	SEG[89]	6934.43	1181.5
531	SEG[88]	6894.43	1181.5
532	SEG[87]	6854.43	1181.5
533	SEG[86]	6814.43	1181.5
534	SEG[85]	6774.43	1181.5
535	SEG[84]	6734.43	1181.5
536	SEG[83]	6694.43	1181.5
537	SEG[82]	6654.43	1181.5
538	SEG[81]	6614.43	1181.5
539	SEG[80]	6574.43	1181.5
540	SEG[79]	6534.43	1181.5
541	SEG[78]	6494.43	1181.5
542	SEG[77]	6454.43	1181.5
543	SEG[76]	6414.43	1181.5
544	SEG[75]	6374.43	1181.5
545	SEG[74]	6334.43	1181.5
546	SEG[73]	6294.43	1181.5
547	SEG[72]	6254.43	1181.5
548	SEG[71]	6214.43	1181.5
549	SEG[70]	6174.43	1181.5
550	SEG[69]	6134.43	1181.5
551	SEG[68]	6094.43	1181.5
552	SEG[67]	6054.43	1181.5
553	SEG[66]	6014.43	1181.5
554	SEG[65]	5974.43	1181.5
555	SEG[64]	5934.43	1181.5
556	SEG[63]	5894.43	1181.5
557	SEG[62]	5854.43	1181.5
558	SEG[61]	5814.43	1181.5
559	SEG[60]	5774.43	1181.5
560	SEG[59]	5734.43	1181.5
561	SEG[58]	5694.43	1181.5
562	SEG[57]	5654.43	1181.5
563	SEG[56]	5614.43	1181.5
564	SEG[55]	5574.43	1181.5
565	SEG[54]	5534.43	1181.5
566	SEG[53]	5494.43	1181.5
567	SEG[52]	5454.43	1181.5
568	SEG[51]	5414.43	1181.5
569	SEG[50]	5374.43	1181.5
570	SEG[49]	5334.43	1181.5
571	SEG[48]	5294.43	1181.5
572	SEG[47]	5254.43	1181.5

PAD	NAME	X	Y
573	SEG[46]	5214.43	1181.5
574	SEG[45]	5174.43	1181.5
575	SEG[44]	5134.43	1181.5
576	SEG[43]	5094.43	1181.5
577	SEG[42]	5054.43	1181.5
578	SEG[41]	5014.43	1181.5
579	SEG[40]	4974.43	1181.5
580	SEG[39]	4934.43	1181.5
581	SEG[38]	4894.43	1181.5
582	SEG[37]	4854.43	1181.5
583	SEG[36]	4814.43	1181.5
584	SEG[35]	4774.43	1181.5
585	SEG[34]	4734.43	1181.5
586	SEG[33]	4694.43	1181.5
587	SEG[32]	4654.43	1181.5
588	SEG[31]	4614.43	1181.5
589	SEG[30]	4574.43	1181.5
590	SEG[29]	4534.43	1181.5
591	SEG[28]	4494.43	1181.5
592	SEG[27]	4454.43	1181.5
593	SEG[26]	4414.43	1181.5
594	SEG[25]	4374.43	1181.5
595	SEG[24]	4334.43	1181.5
596	SEG[23]	4294.43	1181.5
597	SEG[22]	4254.43	1181.5
598	SEG[21]	4214.43	1181.5
599	SEG[20]	4174.43	1181.5
600	SEG[19]	4134.43	1181.5
601	SEG[18]	4094.43	1181.5
602	SEG[17]	4054.43	1181.5
603	SEG[16]	4014.43	1181.5
604	SEG[15]	3974.43	1181.5
605	SEG[14]	3934.43	1181.5
606	SEG[13]	3894.43	1181.5
607	SEG[12]	3854.43	1181.5
608	SEG[11]	3814.43	1181.5
609	SEG[10]	3774.43	1181.5
610	SEG[9]	3734.43	1181.5
611	SEG[8]	3694.43	1181.5
612	SEG[7]	3654.43	1181.5
613	SEG[6]	3614.43	1181.5
614	SEG[5]	3574.43	1181.5
615	SEG[4]	3534.43	1181.5
616	SEG[3]	3494.43	1181.5
617	SEG[2]	3454.43	1181.5
618	SEG[1]	3414.43	1181.5
619	SEG[0]	3374.43	1181.5
620	Reserve	3111.76	1181.5

PAD	NAME	X	Y
621	Reserve	2951.76	1181.5
622	Reserve	2791.76	1181.5
623	Reserve	2631.76	1181.5
624	Reserve	2471.76	1181.5
625	Reserve	2311.76	1181.5
626	Reserve	2271.76	1181.5
627	Reserve	2231.76	1181.5
628	Reserve	2191.76	1181.5
629	COM[83]	2071.51	1181.5
630	COM[82]	2031.51	1181.5
631	COM[81]	1991.51	1181.5
632	COM[80]	1951.51	1181.5
633	COM[75]	1911.51	1181.5
634	COM[74]	1871.51	1181.5
635	COM[73]	1831.51	1181.5
636	COM[72]	1791.51	1181.5
637	COM[67]	1751.51	1181.5
638	COM[66]	1711.51	1181.5
639	COM[65]	1671.51	1181.5
640	COM[64]	1631.51	1181.5
641	COM[59]	1591.51	1181.5
642	COM[58]	1551.51	1181.5
643	COM[57]	1511.51	1181.5
644	COM[56]	1471.51	1181.5
645	COM[51]	1431.51	1181.5
646	COM[50]	1391.51	1181.5
647	COM[49]	1351.51	1181.5
648	COM[48]	1311.51	1181.5
649	COM[43]	1271.51	1181.5
650	COM[42]	1231.51	1181.5
651	COM[41]	1191.51	1181.5
652	COM[40]	1151.51	1181.5
653	COM[35]	1111.51	1181.5
654	COM[34]	1071.51	1181.5
655	COM[33]	1031.51	1181.5
656	COM[32]	991.51	1181.5
657	COM[27]	951.51	1181.5
658	COM[26]	911.51	1181.5
659	COM[25]	871.51	1181.5
660	COM[24]	831.51	1181.5
661	COM[19]	791.51	1181.5
662	COM[18]	751.51	1181.5
663	COM[17]	711.51	1181.5
664	COM[16]	671.51	1181.5
665	COM[11]	631.51	1181.5
666	COM[10]	591.51	1181.5
667	COM[9]	551.51	1181.5
668	COM[8]	511.51	1181.5

PAD	NAME	X	Y
669	Dummy	471.51	1181.5
670	Dummy	431.51	1181.5
671	Dummy	391.51	1181.5
672	Dummy	351.51	1181.5
673	Dummy	311.51	1181.5

Unit : um

BLOCK DIAGRAM

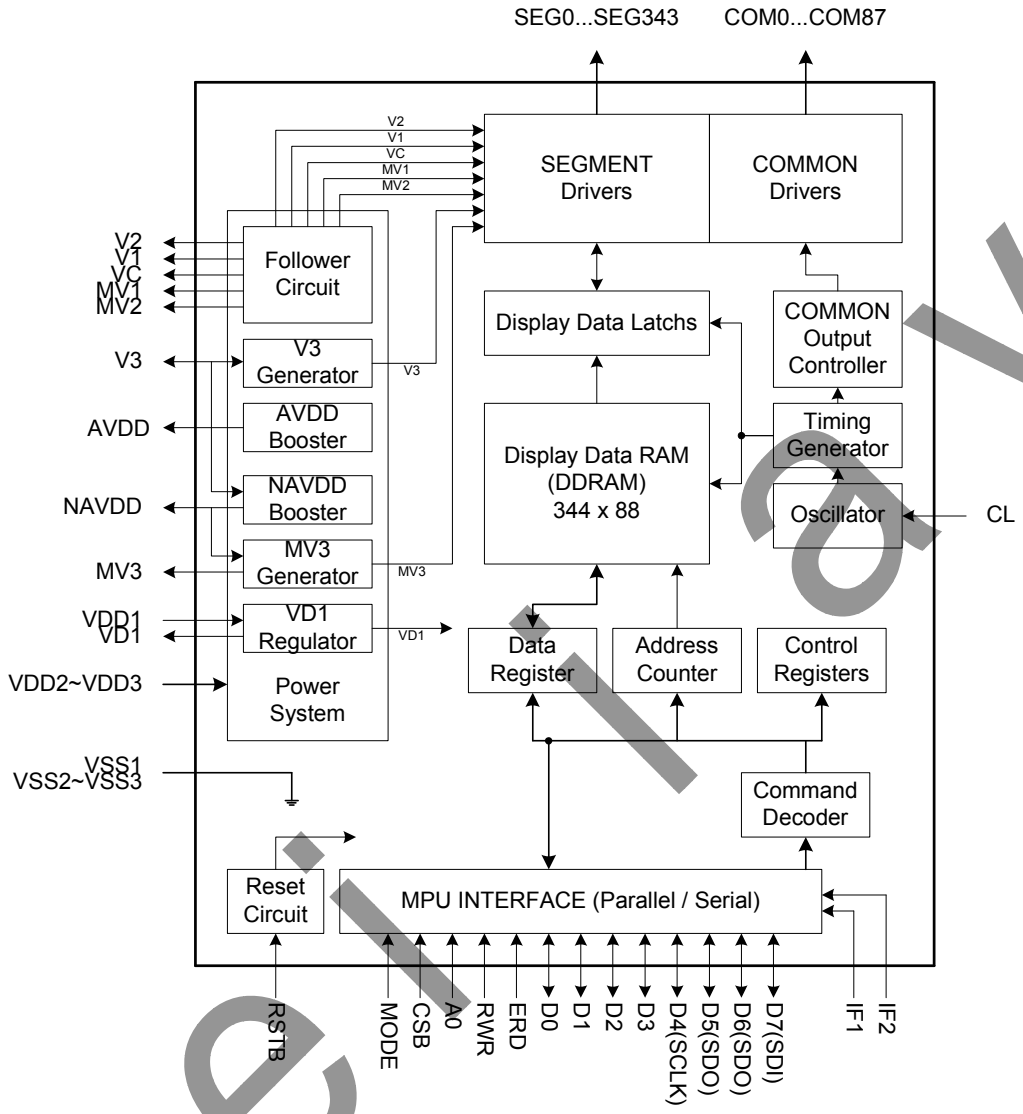


Fig. 1 Block Diagram

PIN DESCRIPTION

Power System

Name	Type	Description
VDD1	Power	VDD1 is the power of interface I/O circuit and OSC circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.
VDD2	Power	VDD2 is the analog power for booster circuit and OP.
VDD3	Power	VDD3 is the power of VREF circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.
VSS1	Power	Ground of interface, logic and OSC circuit. Ground system should be connected by FPC or PCB.
VSS2	Power	Ground of booster circuit and OP. Ground system should be connected by FPC or PCB.
VSS3	Power	Ground of VREF circuit. Ground system should be connected by FPC or PCB.
VD1I VD1O	Power	VD1I is the power source of digital circuit. VD1O is the VD1 output. VD1I and VD1O should be connected together by FPC or PCB.
V3O V3I V3S	Power	LCD driver supply. V3O is the output voltage of V3 generated by ST7598. V3I is the V3 supply of LCD drivers. V3S is the sensor of the V3 generator. V3O, V3I and V3S should be connected together by FPC.
V2	Power	LCD driver supply.
V1	Power	LCD driver supply.
VC	Power	LCD driver supply for center level. VC should be connected with ground system by FPC or PCB.
MV1	Power	LCD driver supply.
MV2	Power	LCD driver supply.
MV3OI MV3S	Power	LCD driver supply. MV3OI is the output voltage of MV3 generated by ST7598 for supply LCD drivers. MV3S is the sensor of the MV3 generator. MV3OI and MV3S should be connected together by FPC.

Name	Type	Description
AVDD	Power	DC/DC converter for LCD driver circuit. Connect a capacitor between AVDD pin and VSS2.
NAVDD	Power	DC/DC converter for LCD driver circuit. Connect a capacitor between NAVDD pin and VSS2.
CA1P CA1N CA2P CA2N	Power	DC/DC converter for LCD driver circuit. Connect a non-polar capacitor between CA1P pin and CA1N pin. Connect a non-polar capacitor between CA2P pin and CA2N pin.
CB1P CB1N	Power	DC/DC converter for LCD driver circuit. Connect a non-polar capacitor between CB1P pin and CB1N pin.
CD1P CD1N CD2P CD2N	Power	DC/DC converter for LCD driver circuit. Connect a non-polar capacitor between CD1P pin and CD1N pin. Connect a non-polar capacitor between CD2P pin and CD2N pin.

LCD Driver Outputs

Name	Type	Description
SEG0 to SEG343	Output	LCD SEG-driver outputs. One voltage level of V2, V1, VC, MV1 and MV2 is selected by combining display DDRAM.
COM0 to COM87	Output	LCD COM-driver outputs. One voltage level of V3, VC and MV3 is selected by combining display DDRAM.

Microprocessor Interface

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSTB</td><td>Input</td><td>Reset input pin. When RSTB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>IF[2:1]</td><td>Input</td><td>These pins select interface operation mode.
<table>
<tr><th>IF2</th><th>IF1</th><th>MCU interface type</th></tr>
<tr><td>H</td><td>H</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>8-bit serial (4-Line)</td></tr>
<tr><td>L</td><td>L</td><td>9-bit serial (3-Line)</td></tr>
</table>
Note: Refer to “Interface Selection” for detailed information.</td></tr>
<tr><td>CSB</td><td>Input</td><td>Chip select input pin.
CSB=“L”: This chip is selected and the MCU interface is active.
CSB=“H”: This chip is not selected and the MCU interface is disabled (D[7:0] are high impedance).</td></tr>
<tr><td>A0</td><td>Input</td><td>A0 determines whether the access is related data or command.
● In parallel interface and 4-Line SPI: A0 is register selection input.
A0 = "H": inputs on data bus are display data;
A0 = "L": inputs on data bus are command.
● A0 is not used in 3-Line SPI. Please fix to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>Input</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MCU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
R/W = “H” : read
R/W = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin.
The data are latched at the rising edge of the /WR signal.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to “H” by VDD1.</td></tr>
<tr><td>ERD</td><td>Input</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MCU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin.
R/W = “H”: When E is “H”, data bus is in output status.
R/W = “L”: The data are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, data bus is in output status.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to “H” by VDD1.</td></tr>
<tr><td>D[7:0]</td><td>I/O</td><td>The bi-directional data bus of the MCU interface. When CSB is “H”, they are high impedance.
● If using serial interface:
SDI: D7
SDO: D5, D6
SCL: D4
D0~D3 must connected to “H” by VDD1.</td></tr>
</table>

Note:

1. After VDD1 is turned ON, all MCU interface pins should not be left OPEN.
2. The un-used pins should be connected to VDD1.

PROM Pins

Name	Type	Description
VPP	Power	The programming power supply of the built-in PROM. Apply external power (VPP=7.25~7.75V, VPP_{TYP}=7.5V) here when programming (> 4mA for successful programming).
EXTB	Input	EXTB="L": Enable the extension operation mode. When programming PROM, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

System Pins

Name	Type	Description
MODE	Input	Must fix to "H" by VDD1.
CLS	Input	When using internal clock oscillator, please connect this pin to "H" by VDD1. When using external clock oscillator, please connect this pin to "L" by VSS1.
CL	I/O	When using internal clock oscillator, this pin is oscillator output. When using external clock oscillator, this pin is oscillator input.

Test Pins

Name	Type	Description
TCAP	Test	Reserved for testing only. Leave this pin open.
VREF	Test	Reserved for testing only. Leave this pin open.
T0~T19	Test	Reserved for testing only. Leave those pins open.
TFCOM0 TFCOM1	Test	Reserved for testing only. Leave those pins open.

ITO Resistance Limitation

Pin Name	ITO Resister
VPP	<50Ω
VDD1, VDD2, VDD3, VSS1, VSS2, VSS3, V3O, V3I, V3S, V2, V1, VC, MV1, MV2, MV3OI, MV3S, AVDD, NAVDD, CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, CD1P, CD1N, CD2P, CD2N	<100Ω
A0, ERD, RWR, CSB, D[7:0]	<700Ω
IF[2:1], CLS, MODE, EXTB	<1KΩ
RSTB	<10KΩ
TCAP, CL, VREF, T0~T19, TFCOM0, TFCOM1	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM87 is equal, and so is it of SEG0 ~ SEG343.
2. These Limitations include the bottleneck of ITO layout.
3. Refer to the application note for ITO layout guideline.

FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

CSB pin is used for chip selection. ST7598 can interface with a MCU when CSB is "L". If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is “H”.

Interface Selection

The interface selection is controlled by IF[3..1] pins. Please refer to the table below:

Table 1

Setting		MCU Type	Interface Pin Function				
IF2	IF1		CSB	A0	RWR	ERD	D[7:0]
H	H	Parallel 8080 series MCU	CSB	A0	/WR	/RD	D[7:0]
H	L	Parallel 6800 series MCU			R/W	E	
L	H	Serial 4-Line series MCU			-	-	D7=SDI, D[5:6]=SDO, D4=SCL, D[0:3] are not used
L	L	Serial 3-Line series MCU		-	-	-	

Note: The un-used pins are marked as “-” and should be connected to “H” by VDD1.

Parallel Interface

When parallel interface is selected, the interface transmission type will be determined by the combination of the control signals. Please refer to the table below:

Table 2

8080 series MCU		6800 series MCU		A0	CSB	Interface Transmission Type
/WR	/RD	R/W	E			
↑	H	L	↓	L	L	Write Command
↑	H	L	↓	H		Write Display Data or Parameter
H	↓	H	↑	H		Read Display Data or Parameter Start
H	↑	H	↓	H		Read Display Data or Parameter Stop

Note: Reading Display Data or Parameter is specified by the instruction before the read operation.

Serial Interface

In serial interface mode (4-Line or 3-Line), IC is active when CSB is “L”. Control signals (SDI, SDO, SCL and A0 for 4-Line) are enabled when CSB is “L”. When CSB is “H”, the MCU interface is not active and the internal shift register and counter are reset. It is recommended to set CSB to “H” after each byte transmission.

4-Line Serial Interface

In 4-Line serial interface, A0 signal is latched at the 8th rising edge of the SCL signal (refer to Fig. 2).

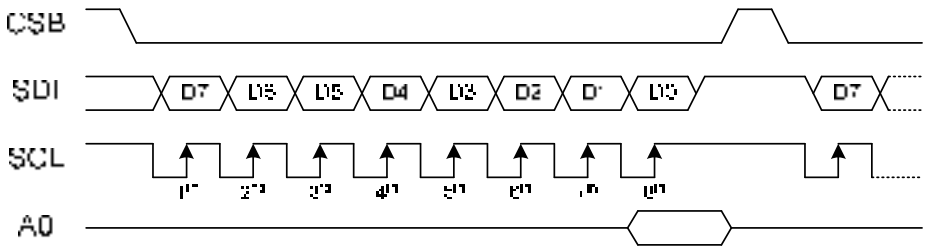


Fig. 2 Write-Operation of 4-Line Serial Interface

When entering read-related command, the information can be shifted out as shown below. The CSB signal should be kept at "L" during this period. The 1st read out data (1st Data) is 9 bits, which includes a dummy bit at the 1st bit. After 1st Data, all read out data (2nd Data and after) will be 8 bits.

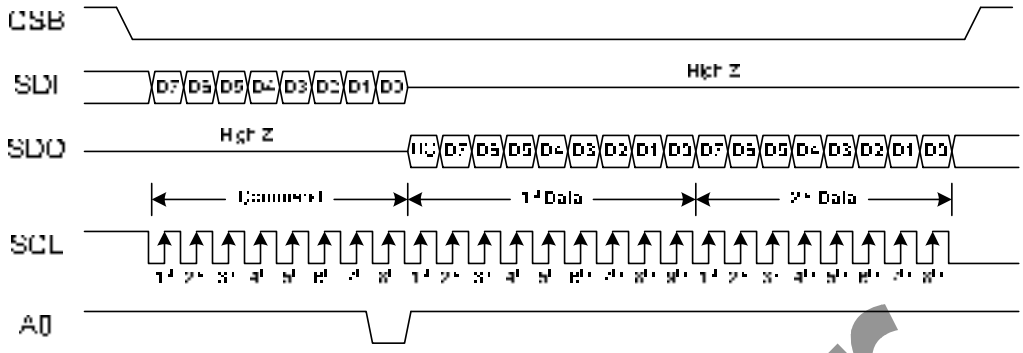


Fig. 3 Read-Operation of 4-Line Serial Interface

If CSB is set to "H" while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must input the data concerned again. In order to avoid transfer error due to incoming noise when write command or data, It is recommended to set CSB at "H" on byte basis to initialize the serial-to–parallel conversion counter and the register.

3-Line Serial Interface

In 3-Line interface, A0 signal is not available and the 1st output of SDI will be treated as A0 flag (refer to Fig. 4).

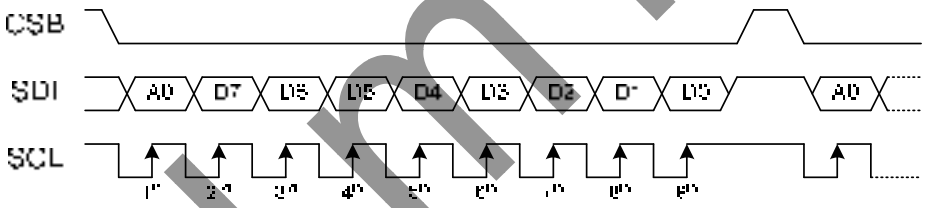


Fig. 4 Write-Operation of 3-Line Serial Interface

When entering read-related command, the information can be shifted out as shown below. The CSB signal should be kept at "L" during this period. The 1st read out data (1st Data) is 9 bits, which includes a dummy bit at the 1st bit. After 1st Data, all read out data (2nd Data and after) will be 8 bits.

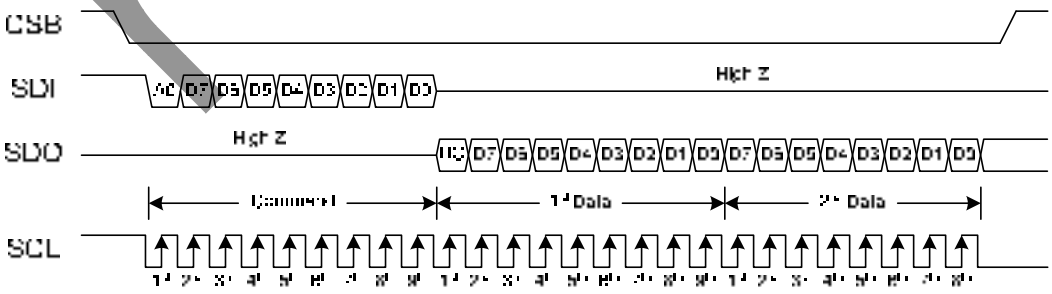


Fig. 5 Read-Operation of 3-Line Serial Interface

If CSB is set to "H" while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must input the data concerned again. In order to avoid transfer error due to incoming noise when write command or data, It is recommended to set CSB at "H" on byte basis to initialize the serial-to–parallel conversion counter and the register.

Display Data RAM (DDRAM)

ST7598 containing a 344x88 bits static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 344 columns by 88 rows. When the data bit in DDRAM is "1", the segment driver will output "ON" voltage. If it is "0", the segment driver will output "OFF" voltage. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.

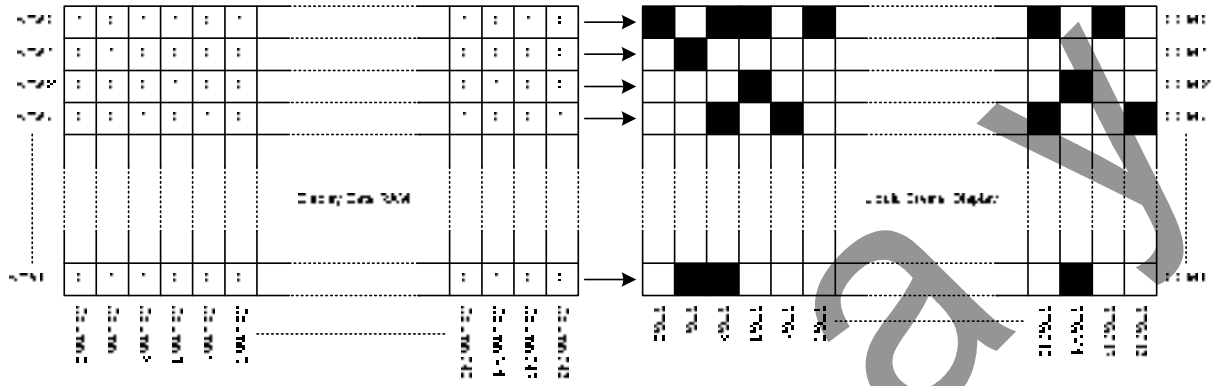


Fig. 6 DDRAM Mapping

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates a 4-bit Page Address Register which can be modified by the instruction of Page Address Set only. As shown in Fig. 7, the 88 rows are configured as 11 pages with 8-bit (for COM0~COM87 while row address direction is normal). The page address must be set before accessing DDRAM content.

Column Address Circuit

This circuit provides the column address of DDRAM. It incorporates a 9-bit Column Address Register which can be modified by the instruction of "Column Address" only. The column address must be set before accessing DDRAM content.

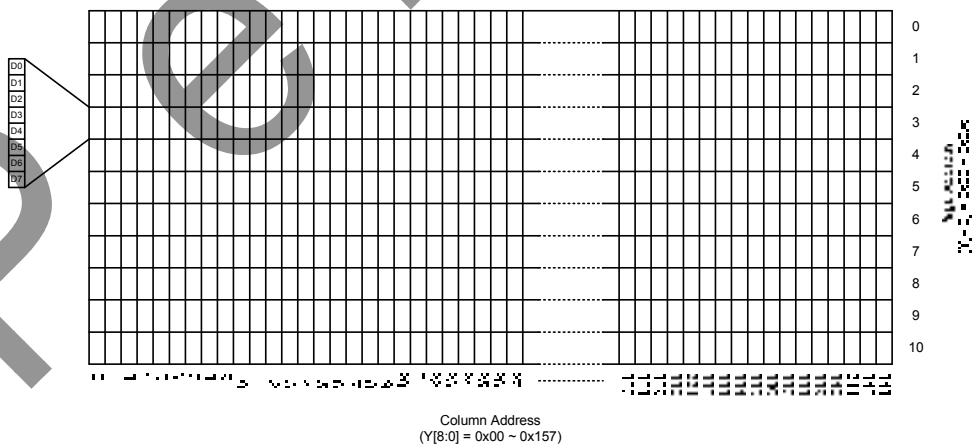


Fig. 7 DDRAM Format

Addressing

Data is downloaded into the Display Data RAM matrix in ST7598 as byte-format. The Display Data RAM has a matrix of 344 by 88 bits. The address ranges are: X=0~343 (column address), Y=0~10 (page address). Address outside these ranges is not allowed.

Addressing the target DDRAM of access is specified with the Page Address Set command and Column Address Set command. Using the Display Data Input/Output Direction command allows you to increase the address either in the page or column direction. In both case, the address is increased by one (+1) after the write or read operation.

When Display Data Input/Output Direction command setting is column direction, the column address counter is increased by 1 (+1) after the write or read operation as shown in Fig. 8. If column address counter is over 157h after data accessed, the page address is increased by one (+1) and the column address is returned to 00h respectively.

Besides, when Display Data Input/Output Direction command setting is page direction, the page address counter is increase by 1 (+1) after the write or read operation as shown in Fig. 9. If the page address counter is over 0Ah after data accessed, the column address is increased by 1 (+1) and page address is returned to 00h respectively.

Whichever direction is selected, the page address counter and column address counter are returned to 00h and 00h respectively, after the DDRAM of column address 157h and page address 0Ah is accessed.

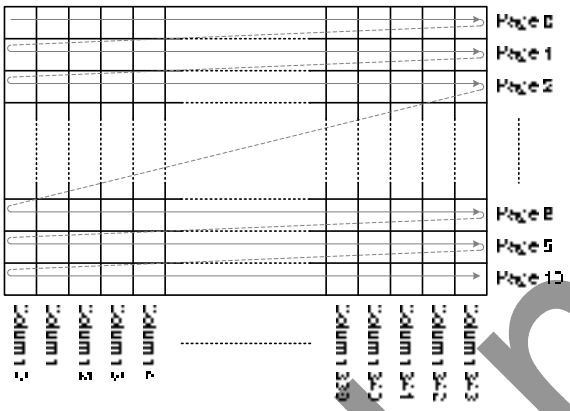


Fig. 8 Display Data Input Direction (DIR=0 & MX=0)

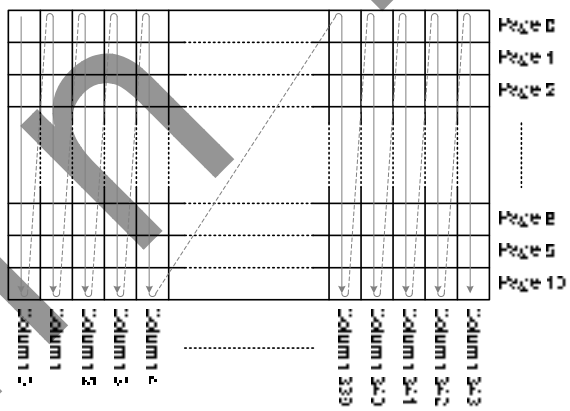


Fig. 9 Display Data Input Direction (DIR=1 & MX=0)

LCD Display Function

DDRAM Map to LCD Driver Output

The internal relation between DDRAM and LCD driver circuit (SEG/COM output path) with different MX or MY setting is illustrated below.

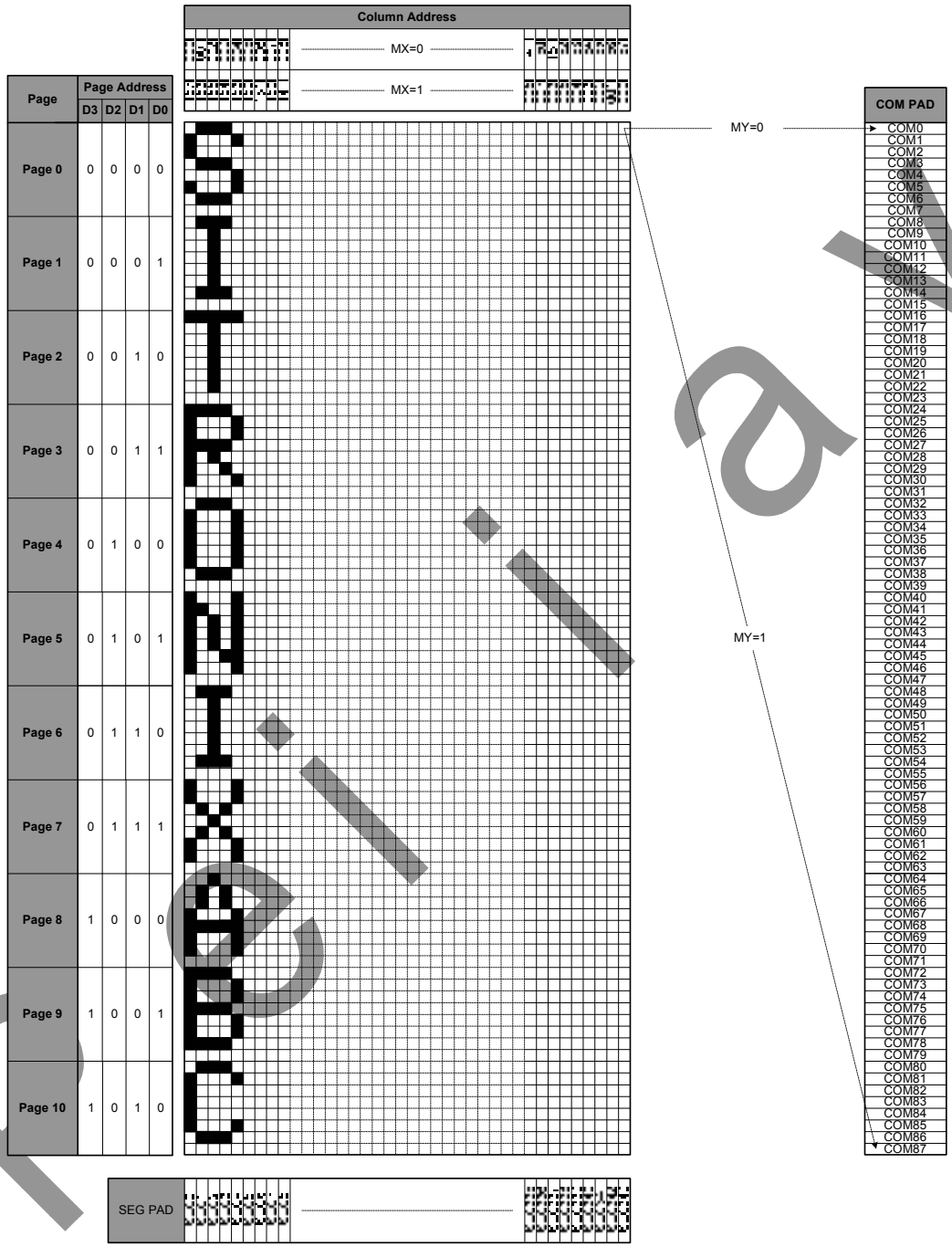


Fig. 10 DDRAM Display Direction

Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7598 is OFF, a Power OFF procedure is needed. Please refer to the OPERATION FLOW section.

External Component of Power Circuit

The recommended external power components need thirteen capacitors. The detailed values of these thirteen capacitors are determined by panel size and loading.

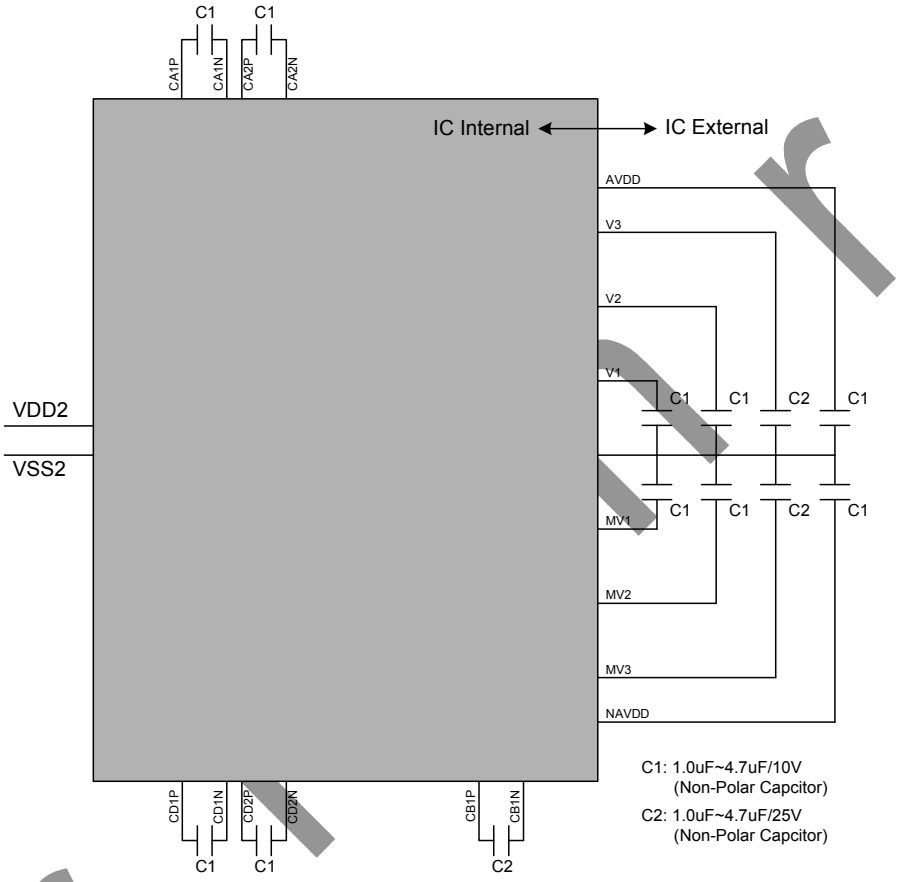


Fig. 11 Power Circuit

V3/MV3 Voltage Regulator

The built-in regulator regulates a stable voltage V3 and MV3. The voltage level of V3/MV3 can be programmed by software instruction. Besides software instruction, ST7598 also provide extra function to adjust the voltage level of V3/MV3, such as Voltage Offset and Temperature Component. The voltage level of V3/MV3 is controlled through the parameters of EV[7:0] and VOF[7:0]. EV[7:0] is set by software instruction and the VOF[7:0] is downloaded from PROM.

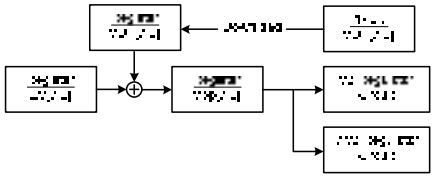


Fig. 12 V3/MV3 Generation

The V3/MV3 calculation formula is shown below. The default value of VOF[7:0] is 00h that download from PROM.

Vop[7:0] = EV[7:0] + VOF[7:0]

V3 = 6.0 + 0.02 x Vop[7:0] = 6.0 + 0.02 x (EV[7:0] + VOF[7:0])

MV3 = -6.0 - 0.02 x Vop[7:0] = -6.0 - 0.02 x (EV[7:0] + VOF[7:0])

LCD Vop = V3 - MV3

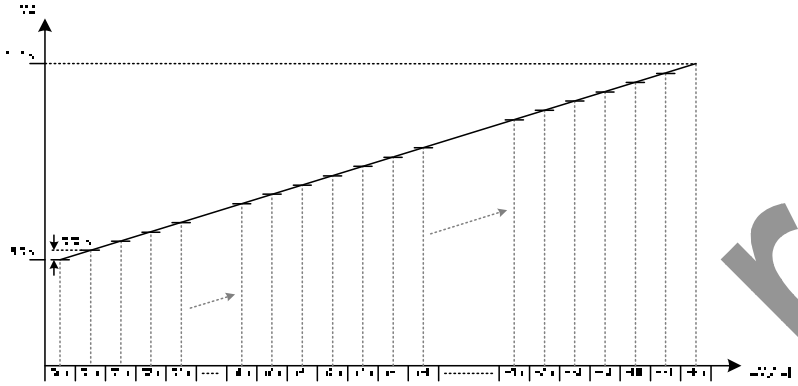


Fig. 13 V3 Programmable Range

The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2 voltage and the loading of LCD module. VOF[7:0] is 2's complement, so that VOF[7:0] can increase or decrease V3 and MV3 respectively.

VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	V3 Offset	MV3 Offset	Vop Offset
0	1	1	1	1	1	1	1	+2540 mV	-2540 mV	+5080 mV
	1	1	1	1	1	1	0	+2520 mV	-2520 mV	+5040 mV
	:	:	:	:	:	:	:	:	:	:
	0	0	0	0	0	1	0	+40 mV	-40 mV	+80 mV
	0	0	0	0	0	0	1	+20 mV	-20 mV	+40 mV
	0	0	0	0	0	0	0	0 mV	0mV	0 mV
1	1	1	1	1	1	1	1	-20 mV	+20 mV	-40 mV
	1	1	1	1	1	1	0	-40 mV	+40 mV	-80 mV
	:	:	:	:	:	:	:	:	:	:
	0	0	0	0	0	0	1	-2540 mV	+2540 mV	-5080 mV
	0	0	0	0	0	0	0	-2560 mV	+2560 mV	-5120 mV

BIAS Voltage Follower

The internal bias ratio resistors divide V3 and MV3 into four reference levels for V2, V1, MV1 and MV2. The BIAS Voltage Follower generates V2, V1, MV1 and MV2 according to these four reference levels. This circuit is operated in AVDD and NAVDD voltage system as the power source.

The available range for V2, V1, MV1 and MV2 is shown in below table.

Symbol	Available Range
V2	2.0V < V2 < 5.0V
V1	1.0V < V1 < VDD2
MV1	-VDD2 < MV2 < -1.0V
MV2	-5.0V < MV2 < -2.0V

The bias ratio and available V3, MV3 and Vop is shown in below table.

BIAS	Available V3 Range	Available MV3 Range	Available Vop Range
1/6	6.0V ~ 7.5V	-7.5V ~ -6.0V	12.0V ~ 15.0V
1/7	6.0V ~ 8.75V	-8.75V ~ -6.0V	12.0V ~ 17.5V
1/8	6.0V ~ 10.0V	-10.0V ~ -6.0V	12.0V ~ 20.0V
1/9	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V
1/10	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V
1/11	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V
1/12	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V
1/13	6.0V ~ 11.1V	-11.1V ~ -6.0V	12.0V ~ 22.2V

Note:

1. The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2 voltage and the loading of LCD module.
2. The upper limit of the available Vop is absolutely voltage level without consider temperature compensation for V3 and MV3. The voltage level of Vop must be within “Available Vop Range” after considering temperature compensation for V3 and MV3.

Power System Setup

The power system of ST7598 can be constructed in different ways. The power system can use internal power circuits or external positive level power supplies. The combination of the internal power circuits or external positive level power supplies is also allowed. The power supplies of negative voltage level for negative power system are disallowed. The following table describes how to use the power system (internal or external). Be sure both of the hardware connection and software setting must be correct.

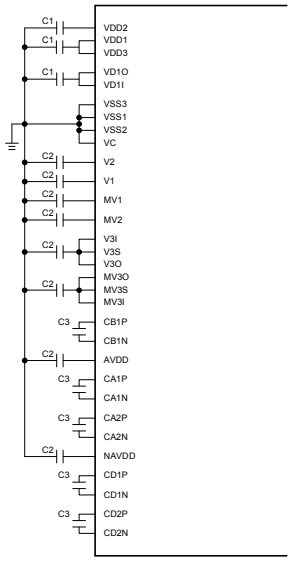
Software Setting for Power Control						Hardware Setting
VAD	V3	VPF	VMV3	VNAD	VNF	
1	-	-	-	-	-	**Internal AVDD** 1. Connect booster capacitor between CA1P and CA1N. 2. Connect booster capacitor between CA2P and CA2N. 3. Connect storage capacitor between AVDD and VSS2.
0	-	-	-	-	-	**External AVDD** 1. Connect storage capacitor between AVDD and VSS2. 2. Apply external voltage level to AVDD.
-	1	-	-	-	-	**Internal V3** 1. Connect storage capacitor between V3 and VSS2.
-	0	-	-	-	-	**External V3** 1. Connect storage capacitor between V3 and VSS2. 2. Apply external voltage level to V3.
-	-	1	-	-	-	**Internal Positive Follower** 1. Connect storage capacitor between V2 and VSS2. 2. Connect storage capacitor between V1 and VSS2.
-	-	0	-	-	-	**External Positive Follower** 1. Connect storage capacitor between V2 and VSS2. 2. Connect storage capacitor between V1 and VSS2. 3. Apply external voltage levels to V2 and V1.
-	-	-	1	1	1	**Internal NAVDD, MV3 and Negative Follower** 1. Connect booster capacitor between CD1P and CD1N. 2. Connect booster capacitor between CD2P and CD2N. 3. Connect storage capacitor between NAVDD and VSS2. 4. Connect booster capacitor between CB1P and CB1N. 5. Connect storage capacitor between MV3 and VSS2. 6. Connect storage capacitor between MV2 and VSS2. 7. Connect storage capacitor between MV1 and VSS2.

Note:

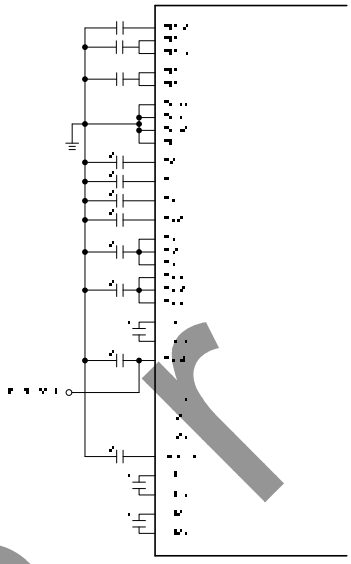
- Whether power on or power off sequence must according to section of Power ON or Power OFF to avid abnormal phenomenon.

The following figures illustrate the connection of typical power applications.

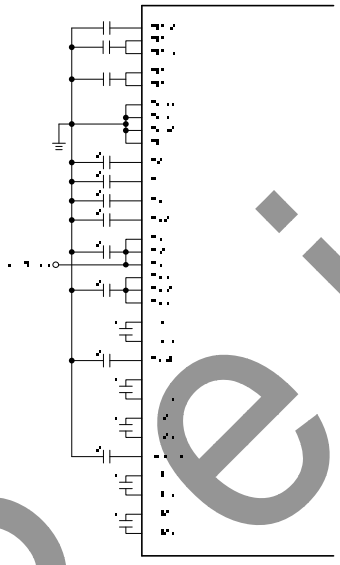
Case 1: VAD=1, V3=1, VPF=1, VMV3=1, VNAD=1, VNF=1



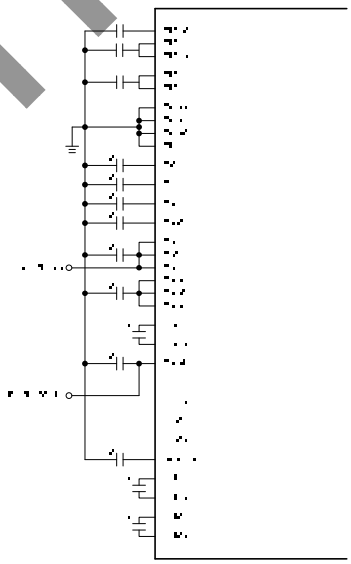
Case 2: VAD=0, V3=1, VPF=1, VMV3=1, VNAD=1, VNF=1



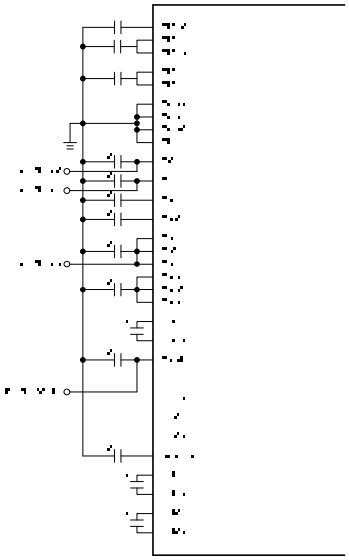
Case 3: VAD=1, V3=0, VPF=1, VMV3=1, VNAD=1, VNF=1



Case 4: VAD=0, V3=0, VPF=1, VMV3=1, VNAD=1, VNF=1



Case 5: VAD=0, V3=0, VPF=0, VMV3=1, VNAD=1, VNF=1



External Components of Power Circuit

The optimum values of C1, C2 and C3 depend on the loading of LCD panel. The value should be determined by customer. When determining the capacitor value, customer can display a pattern with large loading and than check if the capacitor makes the voltage stable or not. The following table is a quick reference for the initial setting.

Symbol	Type	Reference Value (uF)
C1	Capacitor for supply voltage regulation	0.1 ~ 4.7
C2	Capacitor for LCD voltage stabilization	1.0 ~ 4.7
C3	Capacitor for booster	1.0 ~ 4.7

Note:

1. Please place all these capacitors close to the related pin of IC.
2. If the LCD panel is large or the ITO resistance is not good, the capacitor value maybe large than the reference value. If the value is more than 10uF, customer should consider the following suggestion.
3. When the LCD panel size is large and desired display quality is unavailable by increasing the value of capacitor, it is recommended to use the LCD related power externally.
4. The acceptable voltage level of each capacitor as shown in Application Circuit.

Temperature Gradient Selection Circuit

Set V3 with Temperature Compensation (Temperature ≠ 24℃)

There are 19-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8℃. Please see Fig. 14 as below.

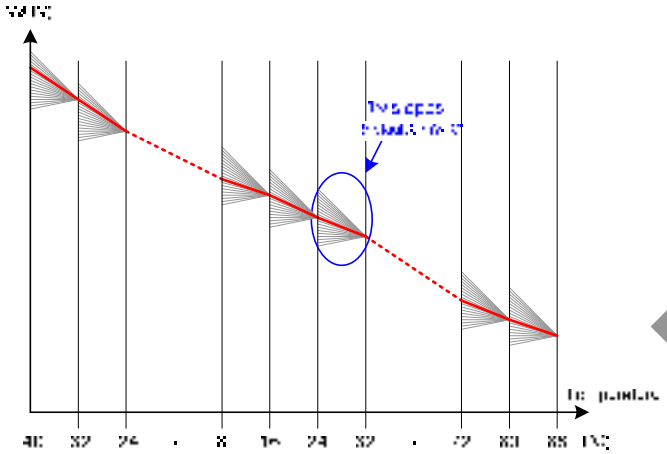


Fig. 14 Temperature Compensation Coefficient Selection

The temperature compensation circuit includes negative and positive temperature gradient slope coefficient. If the temperature gradient slope coefficient is negative (FMTx=0), the available gradient Mx is 0mV/℃, -5mV/° C, -10mV/℃, … and -75mV/℃. The parameter (MTx) of Temperature Gra dient Set instruction (where x=0, 1, 2, …, E, F) has a setting value between 0 and 15. MTx=0 results in Mx=0mV/℃ increme nt on V3, MTx=1 results in Mx=-5mV/℃ increment, …, M Tx=15 results in Mx=-15x5mV/℃ increment. If the temperatu re gradient slope coefficient is positive (FMTx=1), the available gradient Mx is 0mV/℃, 5mV/℃, 10mV/℃ and 15mV/℃. Th e parameter (MTx) of Temperature Gradient Set instruction (where x=0, 1, 2, …, E, F) has a setting value between 0 and 3. MTx=0 results in Mx=0mV/℃ increment on V3, MTx=1 results in Mx=5mV/℃ increment, MTx=2 results in Mx= 10mV/℃ increment and MTx=3 results in Mx=15mV/℃ inc rement.

Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V3 quantity due to temperature V3(T) are described in the equation shown in Table 3.

Temerature Range	Equation V0(T) at temperature=T℃
-40℃ ≤ T < -32℃	V3(T) = V3(T24) + (-32 - T) x M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) x 8
-32℃ ≤ T < -24℃	V3(T) = V3(T24) + (-24 - T) x M1 + (M2 + M3 + M4 + M5 + M6 + M7) x 8
-24℃ ≤ T < -16℃	V3(T) = V3(T24) + (-16 - T) x M2 + (M3 + M4 + M5 + M6 + M7) x 8
-16℃ ≤ T < -8℃	V3(T) = V3(T24) + (-8 - T) x M3 + (M4 + M5 + M6 + M7) x 8
-8℃ ≤ T < 0℃	V3(T) = V3(T24) + (0 - T) x M4 + (M5 + M6 + M7) x 8
0℃ ≤ T < 8℃	V3(T) = V3(T24) + (8 - T) x M5 + (M6 + M7) x 8
8℃ ≤ T < 16℃	V3(T) = V3(T24) + (16 - T) x M6 + M7 x 8
16℃ ≤ T < 24℃	V3(T) = V3(T24) + (24 - T) x M7
24℃ ≤ T < 32℃	V3(T) = V3(T24) - (T - 24) x M8
32℃ ≤ T < 40℃	V3(T) = V3(T24) - (T - 32) x M9 - M8 x 8
40℃ ≤ T < 48℃	V3(T) = V3(T24) - (T - 40) x M10 - (M9 + M8) x 8
48℃ ≤ T < 56℃	V3(T) = V3(T24) - (T - 48) x M11 - (M10 + M9 + M 8) x 8
56℃ ≤ T < 64℃	V3(T) = V3(T24) - (T - 56) x M12 - (M11 + M10 + M9 + M8) x 8
64℃ ≤ T < 72℃	V3(T) = V3(T24) - (T - 64) x M13 - (M12 + M11 + M10 + M9 + M8) x 8
72℃ ≤ T < 80℃	V3(T) = V3(T24) - (T - 72) x M14 - (M13 + M12 + M11 + M10 + M9 + M8) x 8
80℃ ≤ T < 88℃	V3(T) = V3(T24) - (T - 80) x M15 - (M14 + M13 + M12 + M11 + M10 + M9 + M8) x 8

Table 3

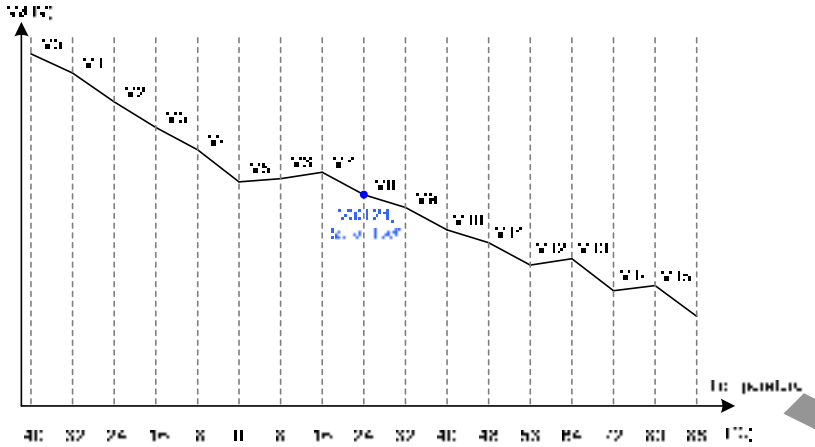


Fig. 15 Temperature Gradient Compensation

Note:

- Please make sure to avoid any kind of heating source near ST7598 such as back light, to prevent V3 is not anticipative because of temperature compensation circuit is working.

Frequency Temperature Gradient Compensation Coefficient

Register Loading Detection

ST7598 will auto-switch frame rate in different temperature such as Fig. 16. TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Set Frequency Compensation Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Operation Clock Frequency Select. The temperature hysteresis “THF” in the Fig. 16 that defines the sensitivity of internal temperature sensor and the value can be altered by instruction Temperature Hysteresis Value Set.

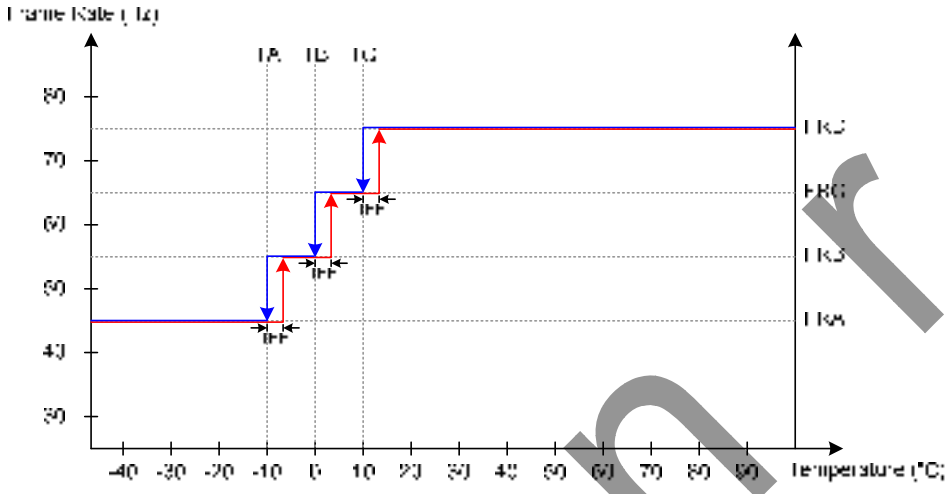


Fig. 16 Frame Rate

Note:

- The temperature compensation related features (V3 voltage level and Frame Rate frequency) are designed with the internal V3 regulator. If the internal V3 regulator is turned OFF, the features are also turned OFF.

RESET CIRCUIT

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDD1 is not stable at the time that the system power is just turned ON. The hardware reset is required to initialize internal registers after VDD1 is stable. Initialization by RSTB pin is essential before operating. The default values of registers are listed below:

Procedure	After Hardware Reset
Content of DDRAM	
Display ON/OFF	
Display Inverse	
Display All Pixel ON	
COM Scan Direction	
Page Address	
Column Address	
Display Data Input/Output Direction	
Column Address Direction	
N-Line Inversion	
N-Line Inversion ON/FF	
Read Modify Write	
Built-in Oscillator Circuit ON/OFF	
Operation Clock Frequency	
Power Control	
Booster Level	
BIAS	
Electronic Volume	
Power Discharge	
Power Save	
Temperature Gradient Compensation	
Temperature Gradient Compensation Flag	
Temperature Detection	
MLS Driving Method	
Frequency Compensation Temperature Range	
Temperature Hysteresis Value	
Test	

Table 4

INSTRUCTION TABLE

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	Set LCD display mode D=0: display off D=1: display on
Display Inverse	0	0	1	0	1	0	0	1	1	INV	Set inverse display mode INV=0: normal display INV=1: inverse display
Display All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all pixel on mode AP=0: normal display AP=1: all pixel on
COM Scan Direction	0	0	1	1	0	0	0	1	0	0	MY=0: COM0→COM87 MY=1: COM87→COM0
	1	0	0	0	0	0	0	0	1	MY	
Page Address	0	0	1	0	1	1	0	0	0	1	Set the page address of DDRAM
	1	0	0	0	0	0	Y3	Y2	Y1	Y0	
Column Address	0	0	0	0	0	1	0	0	1	1	Set the column address of DDRAM
	1	0	-	-	-	-	-	-	-	X8	
	1	0	X7	X6	X5	X4	X3	X2	X1	X0	
Display Data Write	0	0	0	0	0	1	1	1	0	1	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Read	0	0	0	0	0	1	1	1	0	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Input/Output Direction	0	0	1	0	0	0	0	1	0	DIR	Set DDRAM data input direction DIR=0: column direction DIR=1: page direction
Column Address Direction	0	0	1	0	1	0	0	0	0	MX	Set column addressing direction MX=0: SEG0→SEG343 MX=1: SEG343→SEG0
N-Line Inversion	0	0	0	0	1	1	0	1	1	0	Set N-Line inversion
	1	0	0	0	0	NL4	NL3	NL2	NL1	NL0	
N-Line Inversion ON/OFF	0	0	1	1	1	0	0	1	0	NL	Set N-Line inversion mode NL=0: N-Line inversion off NL=1: N-Line inversion on
Enable DDRAM	0	0	0	1	1	0	1	1	0	1	Enable DDRAM
	1	0	0	0	0	1	0	1	0	1	
	1	0	0	0	0	0	1	1	0	0	
Read Modify Write	0	0	1	1	1	0	0	0	0	0	Enable Read Modify Write mode
Read Modify Write End	0	0	1	1	1	0	1	1	1	0	Disable Read Modify Write mode

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Built-in Oscillator Circuit ON/OFF	0	0	1	0	1	0	1	0	1	OSC	Set built-in oscillator mode OSC=0: built-in oscillator off OSC=1: built-in oscillator on
Operation Clock Frequency	0	0	0	1	0	1	1	1	1	1	Set frame rate in different temperature range
	1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
	1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	
Power Control	0	0	0	0	1	0	0	1	0	1	Set built-in power circuits on/off
	1	0	-	-	VAD	V3	VPF	VMV3	VNAD	VNF	
Booster Level	0	0	0	0	1	0	1	0	1	1	Set the level of built-in booster circuit
	1	0	-	-	-	-	-	-	-	BL	
BIAS	0	0	1	0	1	0	0	0	1	0	Set the bias ratio of liquid crystal driving voltage
	1	0	0	0	0	0	0	BS2	BS1	BS0	
Electronic Volume	0	0	1	0	0	0	0	0	0	1	Set the V3 level for liquid crystal driving voltage
	1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
	1	0	0	0	0	0	0	0	0	0	
Power Discharge	0	0	1	1	1	0	1	0	1	0	Set power circuits discharge
	1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	
Power Save	0	0	1	0	1	0	1	0	0	PD	Set power save mode PD=0: normal mode PD=1: standby mode
Temperature Gradient Compensation	0	0	0	1	0	0	1	1	1	0	Set temperature gradient compensation coefficient
	1	0	MT1[3:0]				MT0[3:0]				
	1	0	MT3[3:0]				MT2[3:0]				
	1	0	MT5[3:0]				MT4[3:0]				
	1	0	MT7[3:0]				MT6[3:0]				
	1	0	MT9[3:0]				MT8[3:0]				
	1	0	MTB[3:0]				MTA[3:0]				
	1	0	MTD[3:0]				MTC[3:0]				
	1	0	MTF[3:0]				MTE[3:0]				
Temperature Gradient Compensation Flag	0	0	0	0	1	1	1	0	0	1	Set the slope of temperature gradient is positive or negative
	1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
	1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
Read Status	0	0	1	0	0	0	1	1	1	0	Read IC status
	1	1	D	OSC	AVD	V3	VPF	VMV3	VNAD	VNF	
	1	1	DISV	-	MY	PD	TD	NLFR	MLS	NLF	
Temperature Detection	0	0	0	1	1	0	1	0	0	TD	Set temperature detection mode TD=0: disable mode TD=1: enable mode
MLS Driving Method	0	0	1	1	1	0	0	1	1	1	Set MLS driving method
	1	0	-	-	-	NLFR	MLS	-	-	NLF	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Frequency Compensation Temperature Range	0	0	1	1	1	0	1	1	0	0	Set temperature range for frequency compensation
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Hysteresis Value	0	0	1	1	1	0	1	1	0	1	Set temperature hysteresis value
	1	0	-	-	THV5	THV4	THV3	THV2	THV1	THV0	
	1	0	-	-	-	-	THF3	THF2	THF1	THD0	
Current Temperature	0	0	1	1	1	0	1	1	1	1	Monitor current temperature
	1	1	T7	T6	T5	T4	T3	T2	T1	T0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode TE=0: normal command mode TE=1: test command mode T: select test command mode

INSTRUCTION DESCRIPTION

Display ON/OFF

This instruction turns the display ON or OFF. When ST7598 enters display off, the display output is blank regardless of the content of DDRAM. When ST7598 enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	1	1	D	D=0: Display off (Default) D=1: Display on

Display Inverse

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	1	INV	INV=0: Normal display (Default) INV=1: Inverse display

Display All Pixel ON

When ST7598 enters all pixels on mode, all display pixels are turned on regardless of the content of DDRAM. The content of DDRAM is not changed by setting Display All Pixel ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	0	AP	AP=0: Normal display (Default) AP=1: All pixel on

COM Scan Direction

This instruction defines the COM direction of scan read from DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	1	0	0	MY=0: COM0→COM87
1	0	0	0	0	0	0	0	1	MY	MY=1: COM87→COM0

Note: "-" is disable bit. It can be either logic 0 or 1.

Page Address

This instruction defines the page address corresponding to line address of DDRAM when MCU access to the DDRAM shown in Fig. 10. the detail description is showed in the section of Page Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	0	1	Y[3:0]=0h~Ah
1	0	0	0	0	0	Y3	Y2	Y1	Y0	

Note: "-" is disable bit. It can be either logic 0 or 1.

Y3	Y2	Y1	Y0	Page Address
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
:	:	:	:	:
1	0	0	0	Page 8
1	0	0	1	Page 9
1	0	1	0	Page 10

Column Address

This instruction defines the column address of DDRAM. The detail description is showed in the section of Column Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	1	1	X[8:0]=00h~157h
1	0	-	-	-	-	-	-	-	X8	
1	0	X7	X6	X5	X4	X3	X2	X1	X0	

Note: "-" is disable bit. It can be either logic 0 or 1.

X8	X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	0	0	1	Column 1
0	0	0	0	0	0	0	1	0	Column 2
:	:	:	:	:	:	:	:	:	:
1	0	1	0	1	0	1	0	1	Column 341
1	0	1	0	1	0	1	1	0	Column 342
1	0	1	0	1	0	1	1	1	Column 343

Display Data Write

This instruction is used to transfer data from MCU to DDRAM without changing status of ST7598. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Display Data Write would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	1	
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

Display Data Read

The instruction is used to transfer data from DDRAM to MCU without changing status of ST7598. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Read Display Data would be stopped when any other instruction is accepted. Read Display Data is only available via the parallel interface.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	0	
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

Display Data Input/Output Direction

This instruction defines the direction where the address counter of DDRAM is automatically increment. The detail description is showed in the section of Addressing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	1	0	DIR	DIR=0: Column direction (Default) DIR=1: Page direction

Column Address Direction

This instruction defines the addressing direction of column address as shown in Fig. 10.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	0	MX	MX=0: SEG0→SEG343 (Default) MX=1: SEG343→SEG0

N-Line Inversion

This instruction defines the liquid crystal alternating line number which alters the driving signal phase (in 4-line basis).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	1	1	0	NL[4:0]=00h~14h
1	0	0	0-	0	NL4	NL3	NL2	NL1	NL0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter NL[4:0] and the number of inverted lines is shown below.

NL4	NL3	NL2	NL1	NL0	N-Line Inversion
0	0	0	0	0	8 (4x2)
0	0	0	0	1	8 (4x2)
0	0	0	1	0	12 (4x3)
:	:	:	:	:	:
1	0	0	1	0	76 (4x19)
1	0	0	1	1	80 (4x20)
1	0	1	0	0	84 (4x21)

N-Line Inversion ON/OFF

This instruction defines the function of N-Line inversion is disable or enable. If the N-Line inversion is turning off, the liquid crystal is alternated by frame inversion.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	NL	NL=0: N-Line inversion off (Default) NL=1: N-Line inversion on

Enable DDRAM

This instruction is used to initial DDRAM and DDRAM interface for write to DDRAM or read from DDRAM. This instruction should be set in the initial flow.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	1	0	1	
1	0	0	0	0	1	0	1	0	1	
1	0	0	0	0	0	1	1	0	0	

Read Modify Write

This instruction is used to enter Read Modify Write mode. When entering Read Modify Write mode, the display data read will not increase address counter. Only the display data write will increase the address counter. This mode is maintained until the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	

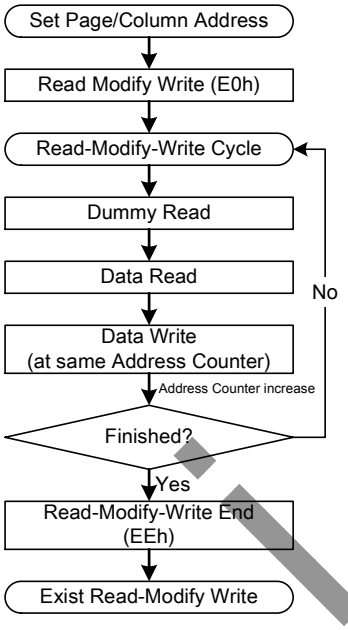


Fig. 17 Read Modify Write Flow

Read Modify Write End

This instruction is used to release the Read Modify Write mode. The page address and column address will return to initial address while the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	0	

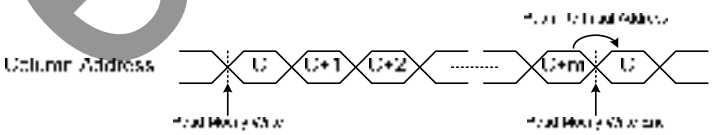


Fig. 18 Address Relationship of Read Modify Write

Built-in Oscillator Circuit ON/OFF

This instruction is used to turn on or off the built-in oscillator circuit. When the built-in power supply is used, the Built-in Oscillator Circuit ON must be executed before the instruction Power Control. If the built-in oscillator circuit is turned off while the built-in power supply is used, abnormal display may occur.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	OSC	OSC=0: Built-in oscillator off OSC=1: Built-in oscillator on

Operation Clock Frequency

This instruction defines the temperature compensation gradient of frequency which automatically adjusts the frame frequency according to the current temperature.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	1	1	FRA[3:0]: FR for -40℃~TA FRB[3:0]: FR for TA~TB FRC[3:0]: FR for TB~TC FRD[3:0]: FR for TC~88℃
1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	

This instruction is used to specify the divide-ratio of the internal operation clock (PWMCK) to the built-in oscillator frequency (fOSC). This instruction is enable only when built-in oscillator clock is turned on. If the built-in oscillator circuit is turned off, the external clock entered to CL pin is used as the internal operation clock. The below table shows the relation between the divide-ratio and the register value which is set by the parameter (FRx[3:1]). This table also illustrates the relation between the internal operation clock (PWMCK) and the display operation clock (fDCLK).

FRx[3:1]	DIV	PWMCK (kHz) fOSC/DIV	fDCLK (kHz) PWMCK/15	fFR (Hz)					
				88 Lines	80 Lines	76 Lines	72 Lines	68 Lines	64 Lines
0000	5	326.0	21.7	236	258	271	286	301	319
0001	6	271.7	18.1	197	215	226	238	251	266
0010	7	232.9	15.5	168	185	194	204	215	228
0011	8	203.8	13.6	148	162	170	179	189	200
0100	9	181.1	12.1	132	144	151	159	168	178
0101	10	163.0	10.9	118	130	136	143	151	160
0110	12	135.8	9.1	99	108	114	120	126	134
0111	14	116.4	7.8	85	93	98	103	108	115
1000	15	108.7	7.2	78	86	90	95	100	106
1001	16	101.9	6.8	74	81	85	89	94	100
1010	18	90.6	6.0	65	71	75	79	83	88
1011	20	81.5	5.4	59	64	68	71	75	79
1100	21	77.6	5.2	57	62	65	68	72	76
1101	24	67.9	4.5	49	54	56	59	63	66
1110	25	65.2	4.3	47	51	54	57	60	63
1111	28	58.2	3.9	42	46	49	51	54	57

Note:

fOSC: Oscillator frequency of the built-in oscillator circuit.

PWMCK: Internal operation clock. It is the basic clock used by the synchronous circuit of ST7598. PWMCK is obtained by dividing fOSC.

fDCLK: Display Operation Clock. It is used to specify a single duration in the sequential drive of liquid crystal. It constantly meets the relation of PWMCK/15 independent of the value of the operation clock frequency select command. The relationship will not change even when the external clock is used.

fFR: The frequency of Frame Rate.

Power Control

This instruction used to control the status of built-in power circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	1	0	1	
1	0	-	-	VAD	V3	VPF	VMV3	VNAD	VNF	

Note: "-" is disable bit. It can be either logic 0 or 1.

ST7598 provides built-in power supply for LCD driving voltage. ST7598 allows using some part(s) of the built-in power circuit(s) with some external voltage(s). The following table shows how these circuits can be controlled through this command. The detail description of power circuit setup is showed in Power System Setup. The power on/off flow please refers to the sections of Power ON and Power OFF to avoid abnormal display.

Flag	Status of Built-in Power Circuit
VAD	VAD=0: Built-in AVDD Booster Circuit OFF VAD=1: Built-in AVDD Booster Circuit ON
V3	V3=0: Built-in V3 Regulator Circuit OFF V3=1: Built-in V3 Regulator Circuit ON
VPF	VPF=0: Built-in Positive Follower Circuit OFF VPF=1: Built-in Positive Follower Circuit ON
VMV3	VMV3=0: Built-in MV3 Regulator Circuit OFF VMV3=1: Built-in MV3 Regulator Circuit ON
VNAD	VNAD=0: Built-in NAVDD Booster Circuit OFF VNAD=1: Built-in NAVDD Booster Circuit ON
VNF	VNF=0: Built-in Negative Follower Circuit OFF VNF=1: Built-in Negative Follower Circuit ON

The internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside. If the built-in oscillator circuit is used, please execute the built-in oscillator circuit turning on before the power circuit turning on. If the external oscillator is used, must operate the external oscillator before the power circuit turning on. If the internal clock is cut off during the operation of the built-in power circuit, abnormal display mat occur.

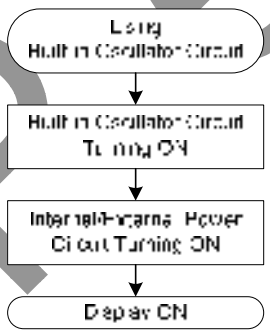


Fig. 19 Power Control (Using Built-in Oscillator)

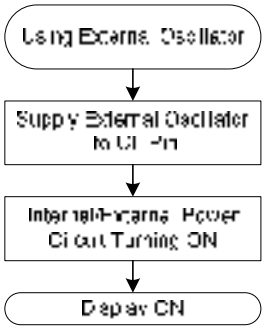


Fig. 20 Power Control (Using External Oscillator)

Booster Level

This instruction defines the booster level without change any hardware connection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	1	1	BL=0: Booster Level 1
1	0	-	-	-	-	-	-	-	BL	BL=1: Booster Level 2

Note: "-" is disable bit. It can be either logic 0 or 1.

BIAS

This instruction defines the bias ratio of voltage requirement for liquid crystal.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	1	0	
1	0	0	0	0	0	0	BS2	BS1	BS0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter BS[2:0] and the bias ratio is shown below.

BS2	BS1	BS0	BIAS Ratio
0	0	0	1/6
0	0	1	1/7
0	1	0	1/8
0	1	1	1/9
1	0	0	1/10
1	0	1	1/11
1	1	0	1/12
1	1	1	1/13

The relationship between the bias ratio and the analog voltage level is shown below.

Symbol	Voltage Level
V3	V3 = Vop/2
V2	V2 = 2 x BIAS x Vop
V1	V1 = BIAS x Vop
VC	VC = VSS2
MV1	MV1 = -BIAS x Vop
MV2	MV2 = -2 x BIAS x Vop
MV3	MV3 = -Vop/2

Electronic Volume

This instruction defines the liquid crystal driving voltage V3 that issued from built-in analog power circuit. The maximum voltage level of Vop that can be generated is dependent on the VDD2 voltage and the loading of LCD module. The detail description is showed in section of V3/MV3 Voltage Regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	0	0	1	EV[7:0]=00h~FFh
1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
1	0	0	0	0	0	0	0	0	0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter EV[7:0] and the voltage level of V3/MV3/Vop is shown below.

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	V3	MV3	Vop
0	0	0	0	0	0	0	0	6.00	-6.00	12
0	0	0	0	0	0	0	1	6.02	-6.02	12.04
0	0	0	0	0	0	1	0	6.04	-6.04	12.08
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0	11.04	-11.04	22.08
1	1	1	1	1	1	0	1	11.06	-11.06	22.12
1	1	1	1	1	1	1	0	11.08	-11.08	22.16
1	1	1	1	1	1	1	1	11.10	-11.10	22.20

Power Discharge

This instruction used to discharge the capacitor connected to the analog power supply circuit. The discharge flow please refers to the sections of Power OFF to avoid abnormal display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	0	1	0	
1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	

Flag	Status of Built-in Power Circuit
DV3	DV3=0: Disable discharge V3 DV3=1: Enable discharge V3
DVPF	DVPF=0: Disable discharge positive follower (V2 & V1) DVPF=1: Enable discharge positive follower (V2 & V1)
DVNF	DVNF=0: Disable discharge negative follower (MV1 & MV2) and NAVDD DVNF=1: Enable discharge negative follower (MV1 & MV2) and NAVDD
DVMV3	DVMV3=0: Disable discharge MV3 DVMV3=1: Enable discharge MV3

Note:

1. Do not discharge before related power is turned off while using internal power system.
2. Do not discharge before related power is turned off while using external power system.

Power Save

This instruction defines the status of chip is normal mode or standby mode. When ST7598 enters the standby mode, the mode causes the LCD module entering the minimum power consumption. Besides, the internal analog circuit will be turned off without discharge power and the display will turn off.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	PD	PD=0: Normal mode PD=1: Standby mode

Temperature Gradient Compensation

This instruction defines the temperature gradient compensation coefficient. Depend on the instruction of Temperature Gradient Compensation Flag, the temperature gradient slope can be set either positive or negative. The detail description is showed in the section of Temperature Gradient Selection Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	1	1	1	0	MTx[3:0]=0h~Fh (Negative TC) MTx[3:0]=0h~3h (Positive TC)
1	0	MT1[3:0]				MT0[3:0]				
1	0	MT3[3:0]				MT2[3:0]				
1	0	MT5[3:0]				MT4[3:0]				
1	0	MT7[3:0]				MT6[3:0]				
1	0	MT9[3:0]				MT8[3:0]				
1	0	MTB[3:0]				MTA[3:0]				
1	0	MTD[3:0]				MTC[3:0]				
1	0	MTF[3:0]				MTE[3:0]				

The related temperature range and available setting value of MTx[3:0] is shown below.

Flag	Temperature Range	Negative TC Value	Positive TC Value
MT0[3:0]	-40℃ ≤ T < -32℃	0h~Fh	0h~3h
MT1[3:0]	-32℃ ≤ T < -24℃	0h~Fh	0h~3h
MT2[3:0]	-24℃ ≤ T < -16℃	0h~Fh	0h~3h
MT3[3:0]	-16℃ ≤ T < -8℃	0h~Fh	0h~3h
MT4[3:0]	-8℃ ≤ T < 0℃	0h~Fh	0h~3h
MT5[3:0]	0℃ ≤ T < 8℃	0h~Fh	0h~3h
MT6[3:0]	8℃ ≤ T < 16℃	0h~Fh	0h~3h
MT7[3:0]	16℃ ≤ T < 24℃	0h~Fh	0h~3h
MT8[3:0]	24℃ ≤ T < 32℃	0h~Fh	0h~3h
MT9[3:0]	32℃ ≤ T < 40℃	0h~Fh	0h~3h
MTA[3:0]	40℃ ≤ T < 48℃	0h~Fh	0h~3h
MTB[3:0]	48℃ ≤ T < 56℃	0h~Fh	0h~3h
MTC[3:0]	56℃ ≤ T < 64℃	0h~Fh	0h~3h
MTD[3:0]	64℃ ≤ T < 72℃	0h~Fh	0h~3h
MTE[3:0]	72℃ ≤ T < 80℃	0h~Fh	0h~3h
MTF[3:0]	80℃ ≤ T < 88℃	0h~Fh	0h~3h

The relationship between the parameters FMTx/MTx[3:0] and the voltage level of V3/MV3/Vop is shown below. The FMTx is set by instruction of Temperature Gradient Compensation Flag.

FMTx	MTx3	MTx2	MTx1	MTx0	V3(mV/℃)	MV3(mV/℃)	Vop(mV/℃)
0	0	0	0	0	0	0	0
	0	0	0	1	-5	5	-10
	0	0	1	0	-10	10	-20
	0	0	1	1	-15	15	-30
	0	1	0	0	-20	20	-40
	0	1	0	1	-25	25	-50
	0	1	1	0	-30	30	-60
	0	1	1	1	-35	35	-70
	1	0	0	0	-40	40	-80
	1	0	0	1	-45	45	-90
	1	0	1	0	-50	50	-100
	1	0	1	1	-55	55	-110
	1	1	0	0	-60	60	-120
	1	1	0	1	-65	65	-130
	1	1	1	0	-70	70	-140
	1	1	1	1	-75	75	-150
1	0	0	0	0	0	0	0
	0	0	0	1	5	-5	10
	0	0	1	0	10	-10	20
	0	0	1	1	15	-15	30

Temperature Gradient Compensation Flag

This instruction defines the temperature gradient compensation coefficient is negative or positive temperature gradient compensation coefficient.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	1	0	0	1	FMTx=0: Negative TC FMTx=1: Positive TC
1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	

Read Status

This instruction can read out the status of ST7598.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	1	1	0	
1	1	D	OSC	AVD	V3	VPF	VMV3	VNAD	VNF	
1	1	DISV	-	MY	PD	TD	NLFR	MLS	NLF	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the flag and the status of IC is shown below.

Flag	Function	0	1
D	Display ON/OFF	OFF	ON
OSC	Built-in OSC Circuit ON/OFF	OFF	ON
AVD	AVDD ON/OFF	OFF	ON
V3	V3 ON/OFF	OFF	ON
VPF	Positive Follower ON/OFF	OFF	ON
VMV3	MV3 ON/OFF	OFF	ON
VNAD	NAVDD ON/OFF	OFF	ON
VNF	Negative Follower ON/OFF	OFF	ON
DISV	Power Discharge ON/OFF	OFF	ON
MY	COM Output Direction	Normal	Reverse
PD	Power Save	Normal	Standby
TD	Temperature Detection ON/OFF	OFF	ON
NLFR	N-Line Inversion Reset by Frame ON/OFF	ON	OFF
MLS	MLS Dispersion/Non-dispersion	Dispersion	Non-dispersion
NLF	N-Line Inversion Reset by Field ON/OFF	ON	OFF

Temperature Detection

This instruction defines the status of temperature detection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	0	0	TD	TD=0: Disable mode TD=1: Enable mode

MLS Driving Method

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	1	1	
1	0	-	-	-	NLFR	MLS	-	-	NLF	

Note: "-" is disable bit. It can be either logic 0 or 1.

Flag	Status
NLFR	NLFR=0: N-Line Inversion Reset by Frame Inversion ON NLFR=1: N-Line Inversion Reset by Frame Inversion OFF
MLS	MLS=0: MLS Dispersion Drive MLS=1: MLS Non-dispersion Drive
NLF	NLF=0: N-Line Inversion Reset by Field Inversion ON NLF=1: N-Line Inversion Reset by Field Inversion OFF

The relationship between parameters (NL, NLFR, MLS and NLF) and COM output method is shown below.

A. 20 lines display without N-Line inversion (NL=0, NLFR=x, MLS=1, NLF=x)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			+ + + +					- - - -		
COM[15:12]				+ + + +					- - - -	
COM[19:16]					+ + + +					- - - -

B. 20 lines display without N-Line inversion (NL=0, NLFR=x, MLS=0, NLF=x)

COM	Positive Frame				Negative Frame			
	Field 1	Field 2	Field 3	Field 4	Field 1	Field 2	Field 3	Field 4
COM[3:0]	+	+	+	+	-	-	-	-
COM[7:4]	+	+	+	+	-	-	-	-
COM[11:8]	+	+	+	+	-	-	-	-
COM[15:12]	+	+	+	+	-	-	-	-
COM[19:16]	+	+	+	+	-	-	-	-

C. 12-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1, MLS=1, NLF=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					+ + + +			
COM[11:8]			+ + + +					+ + + +		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					- - - -					- - - -

D. 12-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1, MLS=0, NLF=0)

COM	Positive Frame				Negative Frame			
	Field 1	Field 2	Field 3	Field 4	Field 1	Field 2	Field 3	Field 4
COM[3:0]	+	+	+	+	+	+	+	+
COM[7:4]	+	+	+	+	+	+	+	+
COM[11:8]	+	+	+	+	+	+	+	+
COM[15:12]	-	-	-	-	-	-	-	-
COM[19:16]	-	-	-	-	-	-	-	-

E. 12-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0, MLS=1, NLF=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			+ + + +					- - - -		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					- - - -					+ + + +

F. 12-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0, MLS=0, NLF=0)

COM	Positive Frame				Negative Frame			
	Field 1	Field 2	Field 3	Field 4	Field 1	Field 2	Field 3	Field 4
COM[3:0]	+	+	+	+	-	-	-	-
COM[7:4]	+	+	+	+	-	-	-	-
COM[11:8]	+	+	+	+	-	-	-	-
COM[15:12]	-	-	-	-	+	+	+	+
COM[19:16]	-	-	-	-	+	+	+	+

G. 8-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1, MLS=1, NLF=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					+ + + +				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			- - - -					- - - -		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					+ + + +					+ + + +

H. 12-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1, MLS=0, NLF=1)

COM	Positive Frame				Negative Frame			
	Field 1	Field 2	Field 3	Field 4	Field 1	Field 2	Field 3	Field 4
COM[3:0]	+	-	-	-	+	+	+	-
COM[7:4]	+	+	-	-	-	+	+	+
COM[11:8]	+	+	+	-	-	-	+	+
COM[15:12]	-	+	+	+	-	-	-	+
COM[19:16]	-	-	+	+	+	-	-	-

I. 8-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0, MLS=1, NLF=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			- - - -					+ + + +		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					+ + + +					- - - -

J. 12-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0, MLS=0, NLF=1)

COM	Positive Frame				Negative Frame			
	Field 1	Field 2	Field 3	Field 4	Field 1	Field 2	Field 3	Field 4
COM[3:0]	+	-	-	-	-	+	+	+
COM[7:4]	+	+	-	-	-	-	+	+
COM[11:8]	+	+	+	-	-	-	-	+
COM[15:12]	-	+	+	+	+	-	-	-
COM[19:16]	-	-	+	+	+	+	-	-

NOP

"No Operation" instruction. ST7598 will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	1	No operation

Frequency Compensation Temperature Range

This instruction defines the temperature range for automatic frame rate adjustment according to current temperature as shown in Fig. 16.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	0	TA[6:0]=00h~7Fh TB[6:0]=00h~7Fh TC[6:0]=00h~7Fh
1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The target temperature add 40 will become the decimal value of register TA[6:0]/TB[6:0]/TC[6:0].

Temp. Range Value	Temp. Rising State (℃)	Temp. Falling State (℃)	Restriction
Freq. Changing Point A (TA)	(TA[6:0]-40)+THF[3:0]	TA[6:0]-40	TB[6:0]>TA[6:0]-THF[3:0] TC[6:0]>TB[6:0]-THF[3:0]
Freq. Changing Point B (TB)	(TB[6:0]-40)+THF[3:0]	TB[6:0]-40	
Freq. Changing Point C (TC)	(TC[6:0]-40)+THF[3:0]	TC[6:0]-40	

Example:

If TA wants to be set at -10℃, TA[6:0]=-10+40=30=1Eh

If TB wants to be set at 0℃, TB[6:0]=0+40=40=28h

If TC wants to be set at 10℃, TC[6:0]=10+40=50=32h

Temperature Hysteresis Value

This instruction defines the temperature detection threshold. THV[5:0] used to set the hysteresis value while the current temperature increase/decrease over this setting temperature, the internal detected temperature will increase/decrease by this setting temperature. If the current temperature increase/decrease less than this setting temperature, the internal detected temperature is keep the same temperature. THF[3:0] used to set the hysteresis value while the temperature change around at the junction between two different frame rate. The changing point of frame rate is depend on the instruction of Frequency Compensation Temperature Range and THF[3:0].

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	1	THV[5:0]=00h~3Fh THF[3:0]=00h~0Fh
1	0	-	-	THV5	THV4	THV3	THV2	THV1	THV0	
1	0	-	-	-	-	THF3	THF2	THF1	THF0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter THV[5:0] and the temperature hysteresis for Vop is shown below.

THV5	THV4	THV3	THV2	THV1	THV0	Temp. Hysteresis for Vop
0	0	0	0	0	0	0℃
0	0	0	0	0	1	0.5℃
0	0	0	0	1	0	1.0℃
:	:	:	:	:	:	:
1	1	1	1	0	1	31.5℃
1	1	1	1	1	0	31.0℃
1	1	1	1	1	1	31.5℃

The relationship between the parameter THF[3:0] and the temperature hysteresis for frame rate is shown below.

THF3	THF2	THF1	THF0	Temp. Hysteresis for FR
0	0	0	0	0℃
0	0	0	1	1℃
0	0	1	0	2℃
:	:	:	:	:
1	1	0	1	13℃
1	1	1	0	14℃
1	1	1	1	15℃

Current Temperature

This instruction used to detect current temperature. If the value of T[7:0] is 00h means the internal detected temperature is -40℃ (T[7:0]x0.5-40). The tolerance of internal de tected temperature is depend on the parameter of THV[5:0]. This function is used for Vop and frame rate compensation. It can not used to replace a real temperature sensor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	1	
1	1	T7	T6	T5	T4	T3	T2	T1	T0	

Test

This instruction is reserved for IC testing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	1	1	TE	T	TE=0: Normal command mode TE=1: Test command mode T: Select test command mode

INSTRUCTION TABLE (PROM Function)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode
TE=1 & T=1											
Vop Increase	0	0	1	1	1	1	0	1	1	0	Vop increase one step
Vop Decrease	0	0	1	1	1	1	0	1	1	1	Vop decrease one step
Vop Offset	0	0	1	1	0	1	0	0	1	1	Vop offset
	1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
PROM WR/RD Control	0	0	1	0	0	1	0	0	0	1	PROM WR/RD control WR/RD=0: enable PROM read WR/RD=1: enable PROM write
	1	0	0	0	WR /RD	0	0	0	0	0	
PROM Control Out	0	0	1	0	0	1	0	0	1	0	Cancel PROM control function
PROM Write	0	0	1	0	0	1	0	0	1	1	PROM programming procedure
PROM Read	0	0	1	0	0	1	0	1	0	0	PROM up-load procedure
PROM Auto Read Control	0	0	1	0	0	1	0	1	1	0	PROM Auto Read Control XARD=0: enable auto read XARD=1: disable auto read
	1	0	0	0	0	XARD	0	0	0	0	

INSTRUCTION DESCRIPTION (PROM Function)

Vop Increase

This instruction is used to increase Vop step by one

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	1	1	0	

Vop Decrease

This instruction is used to decrease Vop step by one

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	1	1	1	

Vop Offset

This instruction is used to adjust Vop step.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	1	1	
1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	

PROM WR/RD Control

This instruction is used to set the status of PROM that write to PROM or read from PROM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	0	1	WR/RD=0: Enable PROM read RW/RD=1: Enable PROM write
1	0	0	0	WR /RD	0	0	0	0	0	

PROM Control Out

This instruction is used to cancel PROM control function.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	0	

PROM Write

This instruction is used to trigger PROM programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	1	

PROM Read

This instruction is used to trigger PROM up-load procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	0	0	

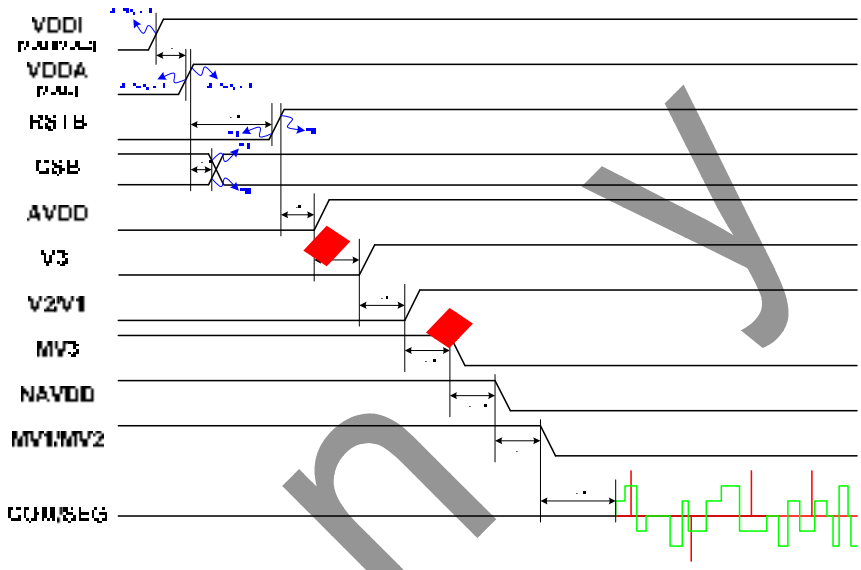
PROM Auto Read Control

This instruction is used to set status of PROM auto read function is enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	1	0	
1	0	0	0	0	XARD	0	0	0	0	

OPERATION FLOW

Power ON

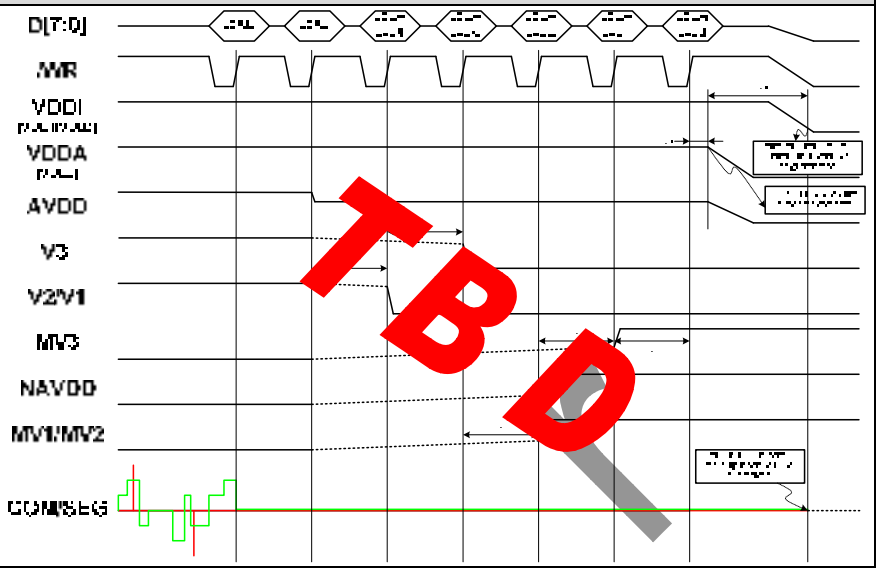
Reference Operation Flow	Operation Sequence
	Case 1: RSTB=L while Power ON  **Case 2: RSTB=H while Power ON** 

Item	Symbol	Requirement	Description
VDDA power ON delay	t_{ON-VA}		● VDDI and VDDA can be applied in any order. IC will NOT be damaged when one of VDDI and VDDA is ON but another is OFF. ● Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.
RSTB input time	t_{ON-RST}		● RESB=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RSTB. ● Increasing t_{ON-RST} can cover the power stable time difference in customer's system. ● RESB has priority over CSB.
CSB input time	t_{ON-CS}		● CSB can be input at any time after power is stable.
AVDD power on delay	t_{ON-AVD}		● The internal or external analog power can be turn on after reset procedure is finished.
V3 power on delay	t_{ON-V3}		● V3 power must turn on after AVDD power is stable.
Positive follower power on delay	t_{ON-VPF}		● Positive follower power (V2 & V1) must turn on after V3er is stable.
MV3 power on delay	t_{ON-MV3}		● MV3 power must turn on before NAVDD, MV1 and MV2 are turn on.
NAVDD power on delay	$t_{ON-NAVD}$		● NAVDD power must turn on after MV3 power is stable.
Negative follower power on delay	t_{ON-VNF}		● Negative follower power (MV1 & MV2) must turn on after NAVDD power is stable.
Display on delay	t_{ON-DSP}		● The LCD display can be turn on after the analog power is stable to avoid abnormal display.

Note:

1. If RSTB is held high or unstable during power ON, a successful hardware reset by RSTB is required after VDDI and VDDA are both stable (as illustrated in Case 2). Otherwise, correct functionality can NOT be guaranteed.
2. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON. The specification listed below just wants to prevent abnormal display on LCD module.
3. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rate voltage. The power stable time depends on system and the time is not included in this specification (customer should consider this factor).

Power OFF

Referential Operation Flow	Operation Sequence
	

Item	Symbol	Requirement	Description
Positive follower power off delay	$t_{OFF-VPF}$		● Positive follower power should discharged after positive follower is turn off. ● Positive follower power can be turned off by instructions of Power Save and Power Control.
V3 power off delay	t_{OFF-V3}		● V3 power should discharged after V3 is turn off. ● V3 power can be turned off by instruction Power Save and Power Control.
Negative follower power off delay	$t_{OFF-VNF}$		● Negative follower power must turn off before MV3 is turn off.
MV3 power off delay	$t_{OFF-MV3}$		● MV3 power must turn off after negative follower and NAVDD are turn off.
Analog circuit discharge off delay	$t_{OFF-DSC}$		● Analog discharge should disable after analog circuit discharge procedure is finished.
VDDA power off delay	t_{OFF-VA}		● Turn VDDA off after discharge procedure is finished. ● AVDD fall as VDDA falling.
VDDI power off delay	t_{OFF-VI}		● If VDDI and VDDA are separated, turn VDDI off after VDDA. ● The AVDD falling time depends on the LCD module and power circuit on the application system.

PROM Operation

Referential PROM Burning Flow

Referential PROM Operation Code

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ABSOLUTE MAXIMUM RATINGS

VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1 & VDD3)		V
Analog Power supply voltage	VDDA (VDD2)		V
LCD Power supply voltage	V3		V
LCD Power supply voltage	V2, V1		V
LCD Power supply voltage	AVDD		V
LCD Power supply voltage	NAVDD		V
LCD Power supply voltage	MV1, MV2		V
LCD Power supply voltage	MV3		V
MCU Interface Input Voltage	VIN		V
MCU Interface Output Voltage	VOUT		V
Operating temperature	TOPR		℃
Storage temperature	TSTR		℃

Note:

1. All voltages are respect to VSS1 unless otherwise noted (VSS1=VSS2=VSS3).
2. Stresses exceed the ranges listed above may cause permanent damage to IC.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Insure the voltage levels always match the correct relation (except Power ON and Power OFF sequence):
   V3 > AVDD > V2 > V1 > VSS2 > MV1 > MV2 > NAVDD > MV3

DC CHARACTERISTICS

VSS1=VSS2=VSS3 =0V and Ta = –40 ~ 85 ℃, unless otherwise sp ecified.

Item	Symbol	Condition		Related Pin	Rating			Unit
					Min.	Typ.	Max.	
Digital Operating Voltage	VDDI			VDD1, VDD3	2.7	–	5.5	V
Analog Operating Voltage	VDDA			VDD2	2.7	–	5.5	V
Input High-level Voltage	V_{IH}			MCU Interface	0.7*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}			MCU Interface	VSS1	–	0.3*VDD1	V
Output High-level Voltage	V_{OH}	I_{OH}=1.0mA, VDD1=2.7V		D[7:0] TSYNC	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}	I_{OL}=–1.0mA, VDD1=2.7V		D[7:0] TSYNC	VSS1	–	0.2*VDD1	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS1		MCU Interface	–1.0	–	1.0	µA
ON Resistance of LCD Drivers	R_{ON}	Ta=25℃	Vop=15.0V, BIAS=1/10 △V=10%	COM Drivers	–		–	KΩ
			Vop=15.0V, BIAS=1/10 △V=10%	SEG Drivers	–		–	KΩ
Operation Clock	f_{OSC}	Ta = 25℃		–	–	1630	–	KHz

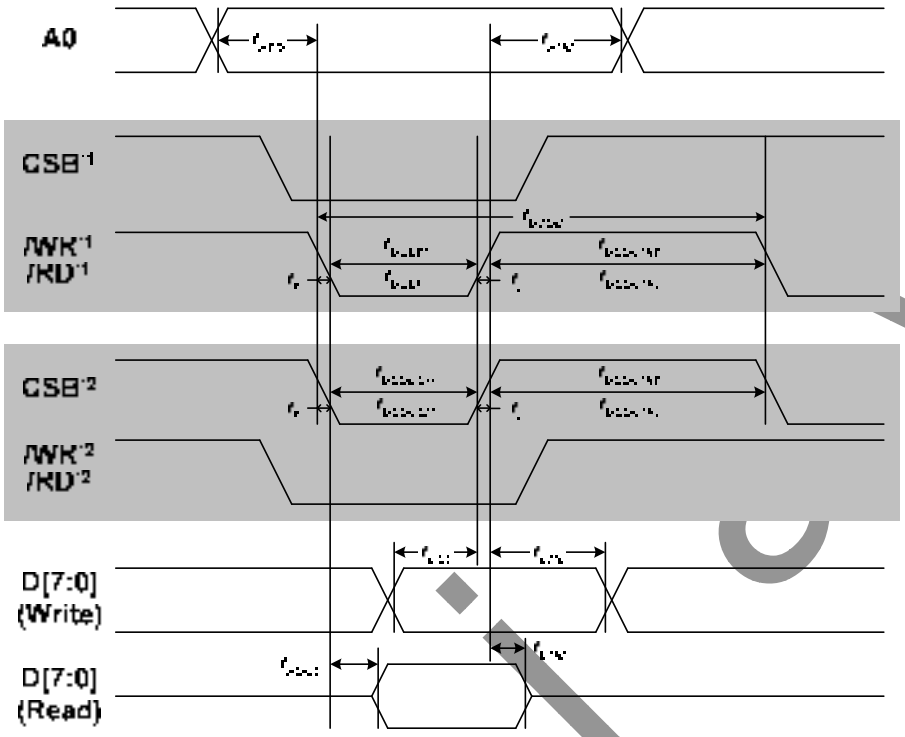
The current consumed by whole IC (bare die) with internal power system:

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display ON Pattern: SNOW (Static)	ISS	VDDI=VDDA=3.3V, Booster Level1, Vop = 15V, Bias=1/10 N-Line OFF, f_{FR}= Hz, Ta=25°C	–		–	µA
Standby	ISS	VDDI=VDDA=3.3V, Ta=25°C	–		–	µA

Note: The current is DC characteristic of a “Bare Chip”.

TIMING CHARATERISTIC

System Bus Timing for 8080 MCU Interface



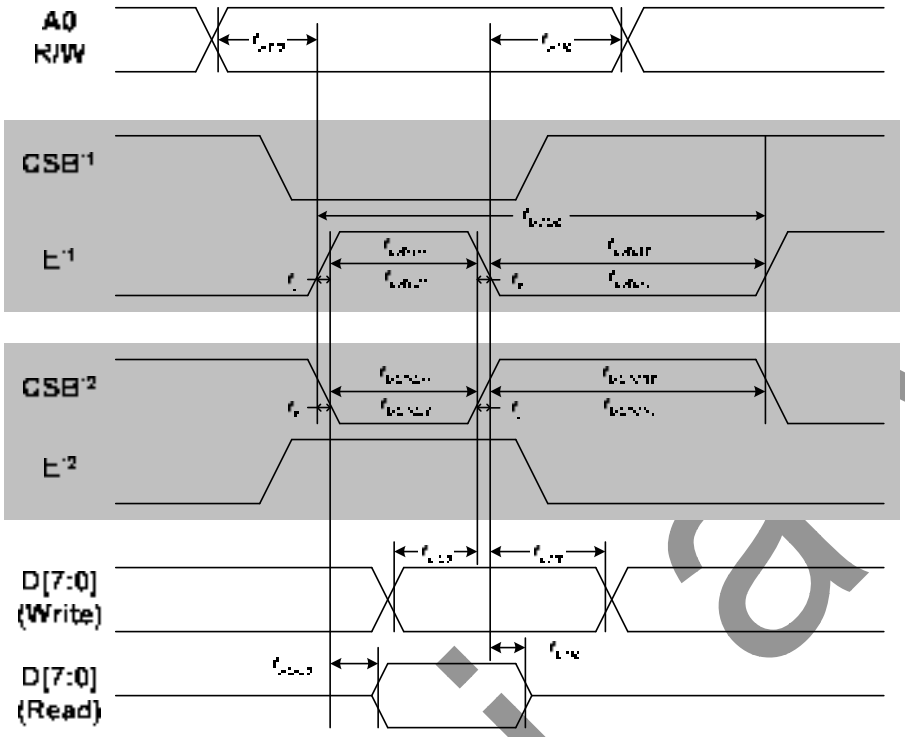
VDD1 = 3.0V~5.0V , Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8			—	ns
Address hold time		tAH8			—	
System cycle time	/WR	tCYC8			—	
/WR L pulse width (WRITE)		tCCLW			—	
/WR H pulse width (WRITE)		tCCHW			—	
/RD L pulse width (READ)	/RD	tCCLR			—	
/RD H pulse width (READ)		tCCHR			—	
CSB L pulse width (WRITE)	CSB	tCSCCLW			—	
CSB H pulse width (WRITE)		tCSCCHW			—	
CSB L pulse width (READ)		tCSCCLR			—	
CSB H pulse width (READ)		tCSCCHR			—	
WRITE Data setup time	D[7:0]	tDS8			—	
WRITE Data hold time		tDH8			—	
READ access time		tACC8	CL = 100 pF	—		
READ Output disable time		tOH8	CL = 100 pF			

Note:

1. This is in case of making the access by /WR or /RD, setting the CSB=Low.
2. This is in case of making the access by CSB, setting the /WR or /RD=High.
3. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
4. All timing is specified using 20% and 80% of VDD1 as the reference.
5. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level.

System Bus Timing for 6800 MCU Interface



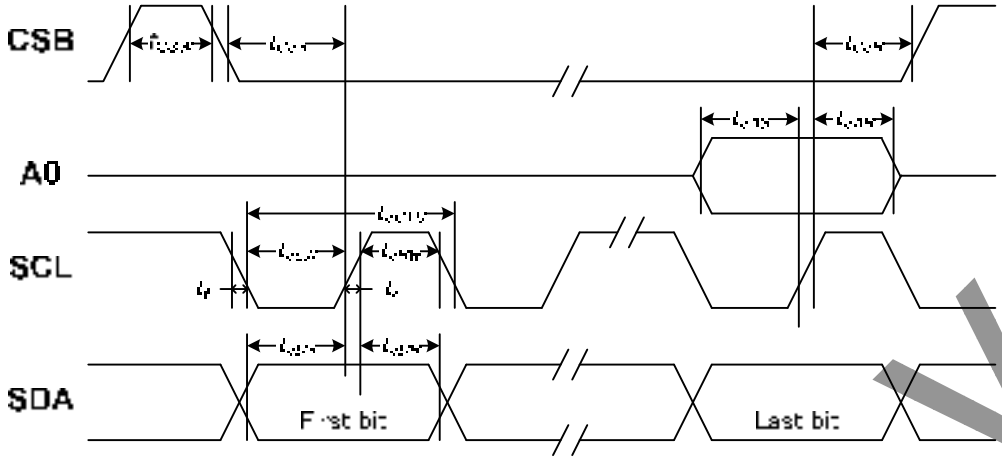
VDD1 = 3.0V~5.0V , Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6			—	ns
Address hold time		tAH6			—	
System cycle time	E	tCYC6			—	
Enable L pulse width (WRITE)		tEWLW			—	
Enable H pulse width (WRITE)		tEWHW			—	
Enable L pulse width (READ)		tEWLR			—	
Enable H pulse width (READ)		tEWHR			—	
CSB L pulse width (WRITE)	CSB	tCSWLW			—	
CSB H pulse width (WRITE)		tCSWHW			—	
CSB L pulse width (READ)		tCSWLR			—	
CSB H pulse width (READ)		tCSWHR			—	
Write data setup time	D[7:0]	tDS6			—	
Write data hold time		tDH6			—	
Read data access time		tACC6	CL = 100 pF	—		
Read data output disable time		tOH6	CL = 100 pF			

Note:

1. This is in case of making the access by E, setting the CSB=Low.
2. This is in case of making the access by CSB, setting the E=High.
3. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.
4. All timing is specified using 20% and 80% of VDD1 as the reference.
5. tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

System Bus Timing for 4-Line SPI MCU Interface



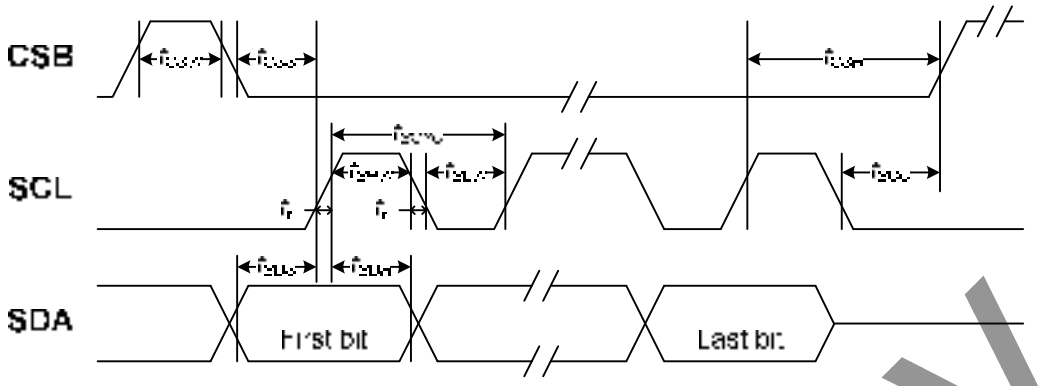
VDD1 = 3.0V~5.0V , Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC			—	ns
SCL “H” pulse width		tSHW			—	
SCL “L” pulse width		tSLW			—	
Address setup time	A0	tSAS			—	
Address hold time		tSAH			—	
Data setup time	SDA	tSDS			—	
Data hold time		tSDH			—	
Read data access time		tACC				
Read data output disable time		tOH				
CSB-SCL time	CSB	tCSS			—	
CSB-SCL time		tCSH			—	
CSB “H” pulse width		tCSW				

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

System Bus Timing for 3-Line SPI MCU Interface



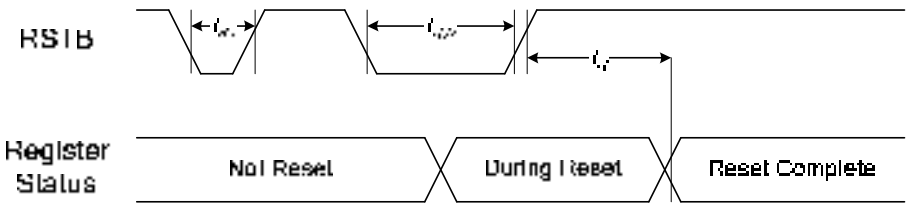
VDD1 = 3.0V~5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Serial Clock Period	SCL	tSCYC			—	ns
SCL “H” pulse width		tSHW			—	
SCL “L” pulse width		tSLW			—	
Data setup time	SDA	tSDS			—	
Data hold time		tSDH			—	
Read data access time		tACC			—	
Read data output disable time		tOH			—	
CSB-SCL time	CSB	tCSS			—	
CSB-SCL time		tCSH			—	
CSB “H” pulse width		tCSW			—	

Note:

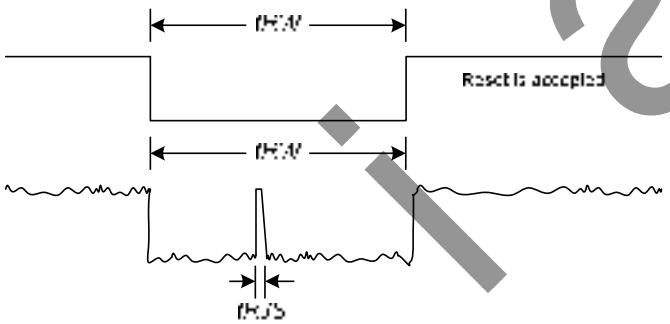
1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 30% and 70% of VDD1 as the standard.

Reset Timing



VDD1 = 3.0V~5.0V , Ta = 25°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—		ns
Reset “L” pulse width		tRW			—	
Reset rejection		tRJ		—		
Reset rejection (for noise spike)		tRJS		—		



Note:

- When tRW is less than 5us, the reset procedure will not start. If tRW is longer than 10us, the IC is executing reset procedure. If tRW is between 5us and 10us, the reset procedure starts.

APPLICATION NOTE

ITO Layout Guide

The ITO layout suggestion is shown as below:

- **For V3, MV3, VD1, VSS and VDD**

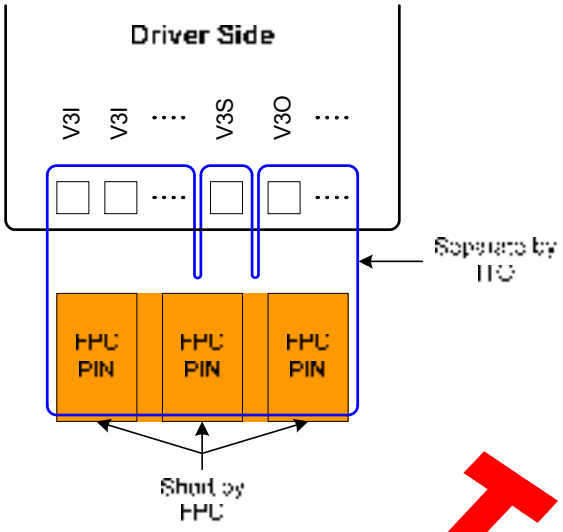


Fig. 21 V3 ITO Layout

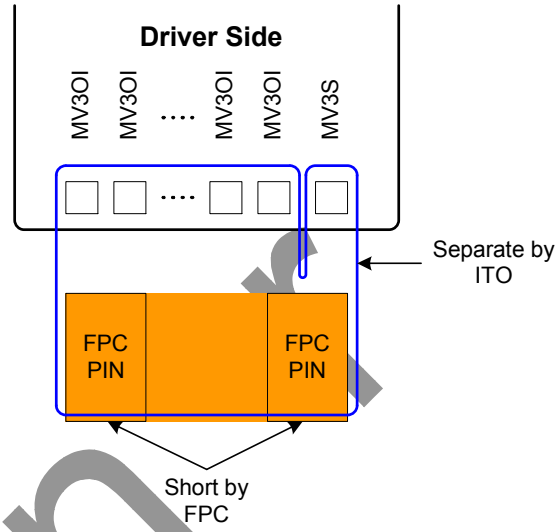


Fig. 22 MV3 ITO Layout

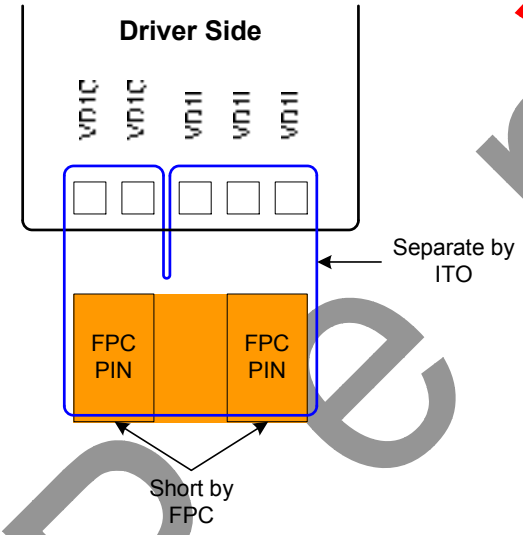


Fig. 23 VD1 ITO Layout

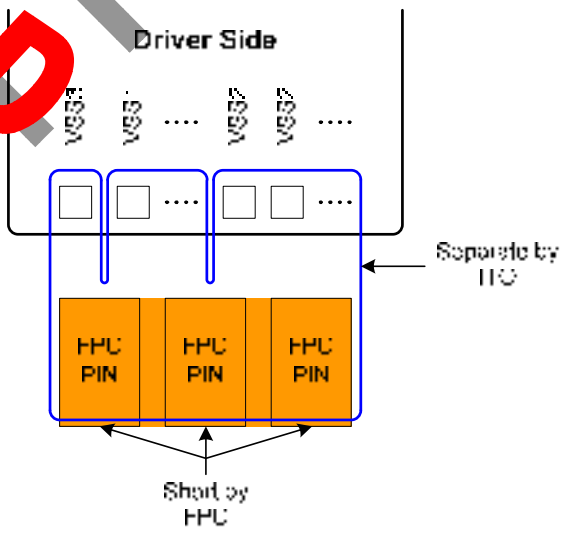


Fig. 24 VSS ITO Layout

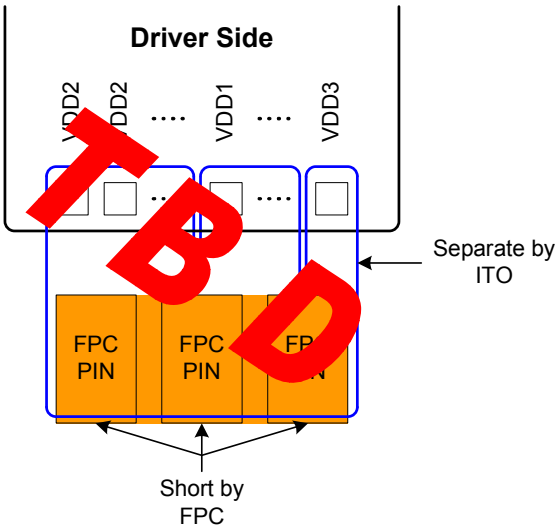


Fig. 25 VDD ITO Layout

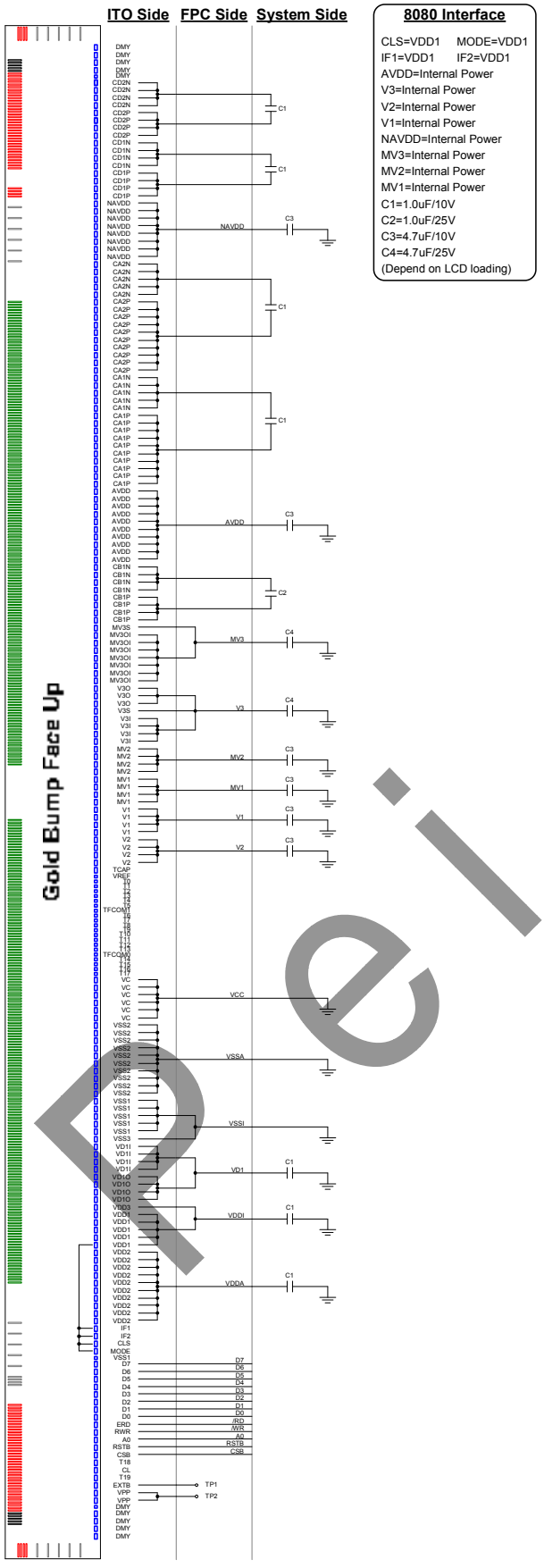
- **For VPP**

  This is the power source for programming the internal PROM. If the ITO resistance is too high, the operation current will cause the voltage drop while programming PROM. Please try to keep the ITO resistance as low as possible.

Selection of Liquid Crystal

Application Circuit

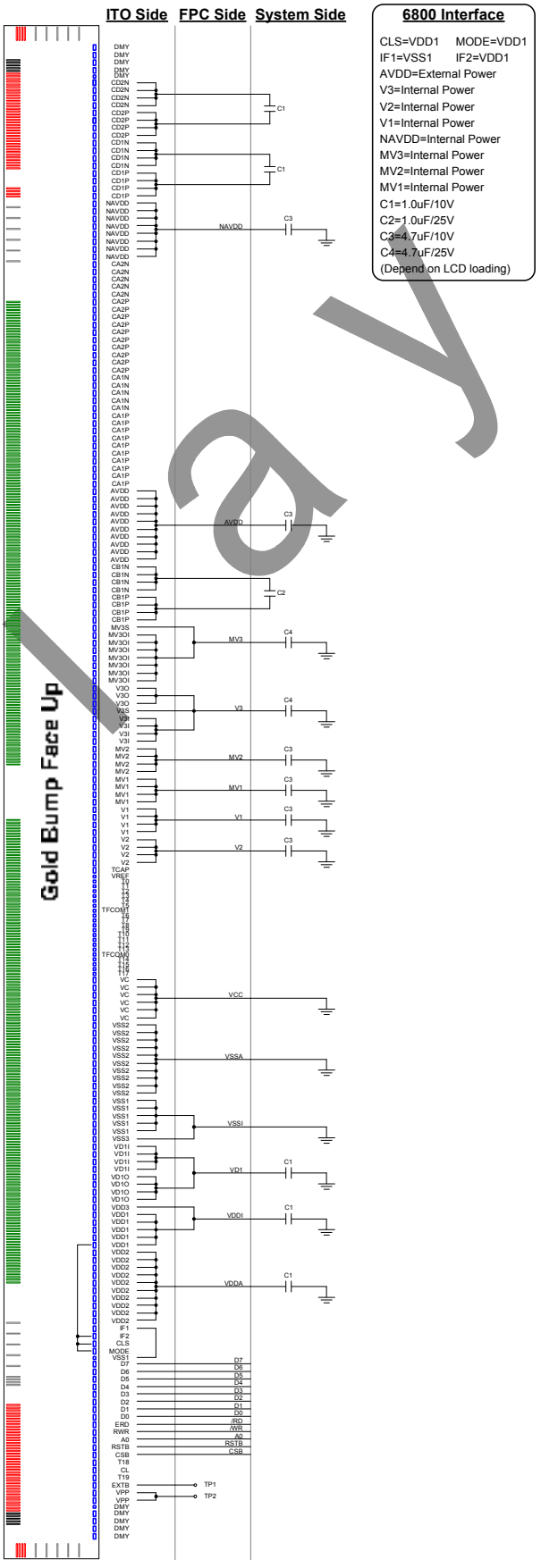
Parallel 8080 Interface



8080 Interface

CLS=VDD1 MODE=VDD1
IF1=VDD1 IF2=VDD1
AVDD=Internal Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/10V
C2=1.0uF/25V
C3=4.7uF/10V
C4=4.7uF/25V
(Depend on LCD loading)

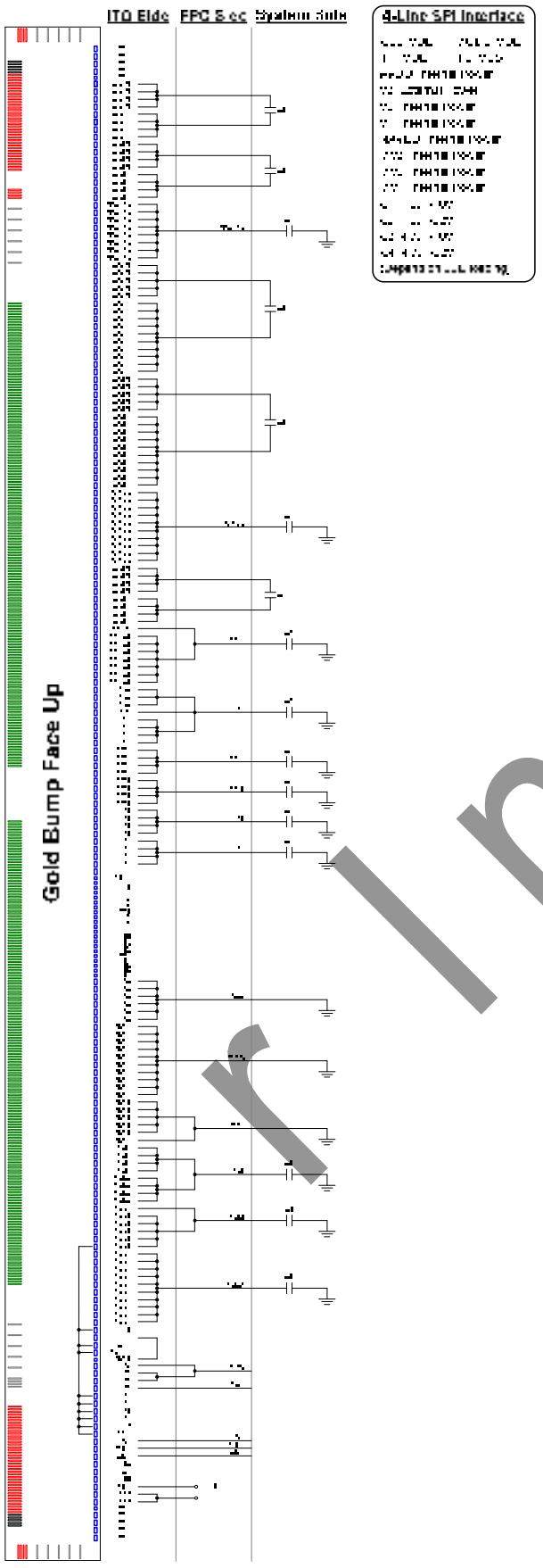
Parallel 6800 Interface



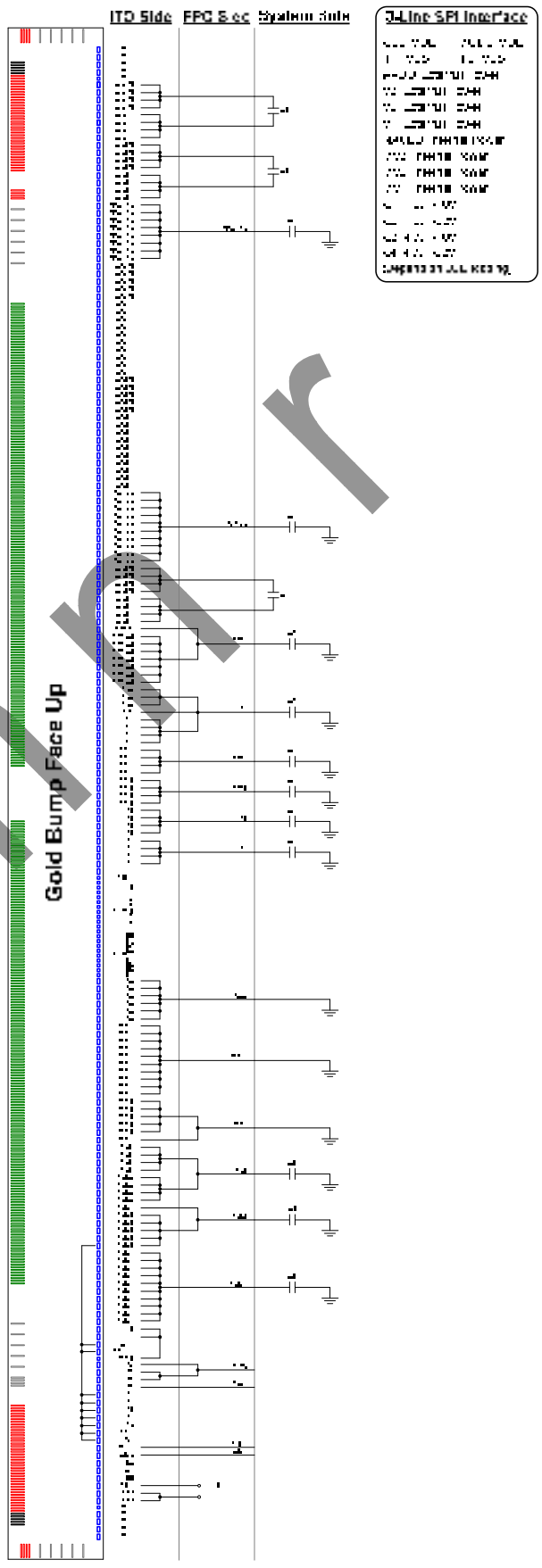
6800 Interface

CLS=VDD1 MODE=VDD1
IF1=VSS1 IF2=VDD1
AVDD=External Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/10V
C2=1.0uF/25V
C3=4.7uF/10V
C4=4.7uF/25V
(Depend on LCD loading)

Serial 4-Line SPI



Serial 3-Line SPI



REVERSION HISTORY

Version	Date	Description
0.0	2010/08/25	● Draft version.
0.1	2010/09/30	● Modify maximum Vop range. ● Modify PAD ARRANGEMENT and PAD CENTER COORDINATES. ● Modify the pin description of TFCOM0 and TFCOM1. ● Modify Application Circuit.
0.1a	2010/12/16	● Modify the mistake of PAD ARRANGEMENT.
0.1b	2011/01/17	● Modify the mistake of PAD ARRANGEMENT.
0.2	2011/01/20	● Set version to Ver-0.2 and release.
0.3	2011/01/26	● Fix feature description mistake (Page 1, “built-in” boost-capacitors -> “external”).
0.4	2011/02/09	● Fix typing mistakes in figures: DDRAM Display Direction & Temperature Compensation Coefficient Selection. ● Fix typing mistakes in figures: Temperature Compensation Coefficient Selection. ● Add the items of ITO Resistance Limitation. ● Modify the figure of Power Circuit. ● Modify the recommended capacitor value of Application Circuit.
0.5	2011/03/14	● Fix mistakes in Page 1 (Feature list): Remove Programmable Display Duty Temperature Compensation: 16-“slopes”.