Sitronix

ST7591

160 x 132 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7591 is a single-chip LSI for graphic dot-matrix LCD systems. It incorporates power system, LCD controller and liquid crystal drivers: 160 segment & 132 common outputs. It can be connected to a microprocessor direct through 8-bit parallel interface or 4-line serial interface (SPI-4). Display data is stored in the internal Display Data RAM (DDRAM, 160x132 bits). The display data bits in DDRAM are directly related to the pixels on LCD panel. With built-in oscillation circuit and low power consumption power circuits, ST7591 can drive LCD panel without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

2. FEATURES

Single-chip LCD Controller & Driver

On-chip Display Data RAM (DDRAM)

- Capacity: 160 x 132 = 21,120 bits
- Directly display RAM pattern from DDRAM
- Support Display Data Vertical Scrolling

LCD Driver Output Circuits

- 160 segment outputs x 132 common outputs
- Support Interlace Mode for LCD layout
- Support Master/Slave Mode
- Programmable Display Line
- Optional N-Line Inversion

Microprocessor Interface

- Bidirectional 8-bit parallel interface supports: 8080-series and 6800-series MPU
- Serial interface (SPI-4) is also supported (write only)

External Hardware Reset Pin (RSTB)

Built-in Oscillation Circuit

- No external component (support external clock)
- Programmable Frame Rate

Low Power Consumption Analog Circuit

- Programmable Voltage Booster
- High-accuracy Voltage Regulator with contrast control and programmable Temperature Compensation (19 slopes and 16 sections, 8℃/section : −40~88℃)
- Voltage Follower for LCD bias voltages
- Built-in PROM for Vop fine tune

Wide Operation Voltage Range

- VDD1-VSS1=3V~5V (Typical)
- VDD2-VSS2=3V~5V (Typical)

LCD Operation Voltage Range

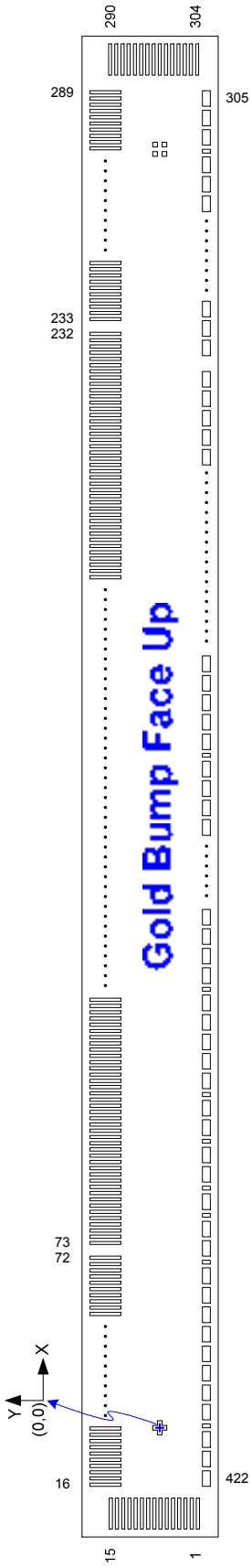
- Maximum V3: 9V
- Minimum MV3: -9V

Temperature Range: -40~85℃

Available Package:

- COG: ST7591-G2
- COF: ST7591-AC01

3-1. ST7591 COG OUTLINE

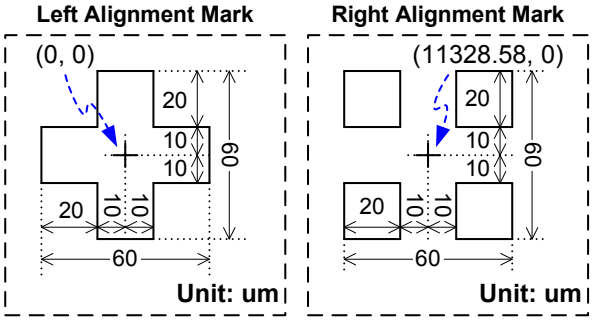


Unit: um

Part Number	Chip Thickness
ST7591	480
Chip Size (XxY)	**Bump Height**
12700 x 780	15
Pad Number	**Pad Pitch (Minimum)**
72~73, 232~233	100
1~15, 16~72, 73~232, 233~289, 290~304	43
330~331	157.5
309~330, 331~359, 361~392, 394~398, 400~401, 403~404, 408~409, 411~418	105
307~309, 359~361, 392~394, 398~400, 401~403, 404~408, 409~411, 418~420	78.75
305~307, 420~422	103.75
Pad Number	**Bump Size (X x Y)**
1~15, 290~304	96 x 26
16~289	26 x 96
308, 360, 393, 399, 402, 405, 407, 410, 419	30 x 45
305~307, 309~359, 361~392, 394~398, 400~401, 403~404, 406, 408~409, 411~418, 420~422	80 x 45
*** Refer to section "PAD CENTER COORDINATES" for ITO layout.**	

Alignment Mark

The alignment mark information is shown below:



3-2. PAD CENTER COORDINATES

PAD No.	PAD Name	X	Y
1	COM131	-424.21	-237.61
2	COM130	-424.21	-194.61
3	COM129	-424.21	-151.61
4	COM128	-424.21	-108.61
5	COM127	-424.21	-65.61
6	COM126	-424.21	-22.61
7	COM125	-424.21	20.39
8	COM124	-424.21	63.39
9	COM123	-424.21	106.39
10	COM122	-424.21	149.39
11	COM121	-424.21	192.39
12	COM120	-424.21	235.39
13	COM119	-424.21	278.39
14	COM118	-424.21	321.39
15	COM117	-424.21	364.39
16	Dummy	-262.21	381.89
17	Dummy	-219.21	381.89
18	Dummy	-176.21	381.89
19	Dummy	-133.21	381.89
20	Dummy	-90.21	381.89
21	Dummy	-47.21	381.89
22	COM116	-4.21	381.89
23	COM115	38.79	381.89
24	COM114	81.79	381.89
25	COM113	124.79	381.89
26	COM112	167.79	381.89
27	COM111	210.79	381.89
28	COM110	253.79	381.89
29	COM109	296.79	381.89
30	COM108	339.79	381.89
31	COM107	382.79	381.89
32	COM106	425.79	381.89
33	COM105	468.79	381.89
34	COM104	511.79	381.89
35	COM103	554.79	381.89
36	COM102	597.79	381.89
37	COM101	640.79	381.89
38	COM100	683.79	381.89
39	COM99	726.79	381.89
40	COM98	769.79	381.89
41	COM97	812.79	381.89
42	COM96	855.79	381.89
43	COM95	898.79	381.89
44	COM94	941.79	381.89
45	COM93	984.79	381.89
46	COM92	1027.79	381.89

PAD No.	PAD Name	X	Y
47	COM91	1070.79	381.89
48	COM90	1113.79	381.89
49	COM89	1156.79	381.89
50	COM88	1199.79	381.89
51	COM87	1242.79	381.89
52	COM86	1285.79	381.89
53	COM85	1328.79	381.89
54	COM84	1371.79	381.89
55	COM83	1414.79	381.89
56	COM82	1457.79	381.89
57	COM81	1500.79	381.89
58	COM80	1543.79	381.89
59	COM79	1586.79	381.89
60	COM78	1629.79	381.89
61	COM77	1672.79	381.89
62	COM76	1715.79	381.89
63	COM75	1758.79	381.89
64	COM74	1801.79	381.89
65	COM73	1844.79	381.89
66	COM72	1887.79	381.89
67	COM71	1930.79	381.89
68	COM70	1973.79	381.89
69	COM69	2016.79	381.89
70	COM68	2059.79	381.89
71	COM67	2102.79	381.89
72	COM66	2145.79	381.89
73	SEG159	2245.79	381.89
74	SEG158	2288.79	381.89
75	SEG157	2331.79	381.89
76	SEG156	2374.79	381.89
77	SEG155	2417.79	381.89
78	SEG154	2460.79	381.89
79	SEG153	2503.79	381.89
80	SEG152	2546.79	381.89
81	SEG151	2589.79	381.89
82	SEG150	2632.79	381.89
83	SEG149	2675.79	381.89
84	SEG148	2718.79	381.89
85	SEG147	2761.79	381.89
86	SEG146	2804.79	381.89
87	SEG145	2847.79	381.89
88	SEG144	2890.79	381.89
89	SEG143	2933.79	381.89
90	SEG142	2976.79	381.89
91	SEG141	3019.79	381.89
92	SEG140	3062.79	381.89

PAD No.	PAD Name	X	Y
93	SEG139	3105.79	381.89
94	SEG138	3148.79	381.89
95	SEG137	3191.79	381.89
96	SEG136	3234.79	381.89
97	SEG135	3277.79	381.89
98	SEG134	3320.79	381.89
99	SEG133	3363.79	381.89
100	SEG132	3406.79	381.89
101	SEG131	3449.79	381.89
102	SEG130	3492.79	381.89
103	SEG129	3535.79	381.89
104	SEG128	3578.79	381.89
105	SEG127	3621.79	381.89
106	SEG126	3664.79	381.89
107	SEG125	3707.79	381.89
108	SEG124	3750.79	381.89
109	SEG123	3793.79	381.89
110	SEG122	3836.79	381.89
111	SEG121	3879.79	381.89
112	SEG120	3922.79	381.89
113	SEG119	3965.79	381.89
114	SEG118	4008.79	381.89
115	SEG117	4051.79	381.89
116	SEG116	4094.79	381.89
117	SEG115	4137.79	381.89
118	SEG114	4180.79	381.89
119	SEG113	4223.79	381.89
120	SEG112	4266.79	381.89
121	SEG111	4309.79	381.89
122	SEG110	4352.79	381.89
123	SEG109	4395.79	381.89
124	SEG108	4438.79	381.89
125	SEG107	4481.79	381.89
126	SEG106	4524.79	381.89
127	SEG105	4567.79	381.89
128	SEG104	4610.79	381.89
129	SEG103	4653.79	381.89
130	SEG102	4696.79	381.89
131	SEG101	4739.79	381.89
132	SEG100	4782.79	381.89
133	SEG99	4825.79	381.89
134	SEG98	4868.79	381.89
135	SEG97	4911.79	381.89
136	SEG96	4954.79	381.89
137	SEG95	4997.79	381.89
138	SEG94	5040.79	381.89
139	SEG93	5083.79	381.89
140	SEG92	5126.79	381.89

PAD No.	PAD Name	X	Y
141	SEG91	5169.79	381.89
142	SEG90	5212.79	381.89
143	SEG89	5255.79	381.89
144	SEG88	5298.79	381.89
145	SEG87	5341.79	381.89
146	SEG86	5384.79	381.89
147	SEG85	5427.79	381.89
148	SEG84	5470.79	381.89
149	SEG83	5513.79	381.89
150	SEG82	5556.79	381.89
151	SEG81	5599.79	381.89
152	SEG80	5642.79	381.89
153	SEG79	5685.79	381.89
154	SEG78	5728.79	381.89
155	SEG77	5771.79	381.89
156	SEG76	5814.79	381.89
157	SEG75	5857.79	381.89
158	SEG74	5900.79	381.89
159	SEG73	5943.79	381.89
160	SEG72	5986.79	381.89
161	SEG71	6029.79	381.89
162	SEG70	6072.79	381.89
163	SEG69	6115.79	381.89
164	SEG68	6158.79	381.89
165	SEG67	6201.79	381.89
166	SEG66	6244.79	381.89
167	SEG65	6287.79	381.89
168	SEG64	6330.79	381.89
169	SEG63	6373.79	381.89
170	SEG62	6416.79	381.89
171	SEG61	6459.79	381.89
172	SEG60	6502.79	381.89
173	SEG59	6545.79	381.89
174	SEG58	6588.79	381.89
175	SEG57	6631.79	381.89
176	SEG56	6674.79	381.89
177	SEG55	6717.79	381.89
178	SEG54	6760.79	381.89
179	SEG53	6803.79	381.89
180	SEG52	6846.79	381.89
181	SEG51	6889.79	381.89
182	SEG50	6932.79	381.89
183	SEG49	6975.79	381.89
184	SEG48	7018.79	381.89
185	SEG47	7061.79	381.89
186	SEG46	7104.79	381.89
187	SEG45	7147.79	381.89
188	SEG44	7190.79	381.89

PAD No.	PAD Name	X	Y
189	SEG43	7233.79	381.89
190	SEG42	7276.79	381.89
191	SEG41	7319.79	381.89
192	SEG40	7362.79	381.89
193	SEG39	7405.79	381.89
194	SEG38	7448.79	381.89
195	SEG37	7491.79	381.89
196	SEG36	7534.79	381.89
197	SEG35	7577.79	381.89
198	SEG34	7620.79	381.89
199	SEG33	7663.79	381.89
200	SEG32	7706.79	381.89
201	SEG31	7749.79	381.89
202	SEG30	7792.79	381.89
203	SEG29	7835.79	381.89
204	SEG28	7878.79	381.89
205	SEG27	7921.79	381.89
206	SEG26	7964.79	381.89
207	SEG25	8007.79	381.89
208	SEG24	8050.79	381.89
209	SEG23	8093.79	381.89
210	SEG22	8136.79	381.89
211	SEG21	8179.79	381.89
212	SEG20	8222.79	381.89
213	SEG19	8265.79	381.89
214	SEG18	8308.79	381.89
215	SEG17	8351.79	381.89
216	SEG16	8394.79	381.89
217	SEG15	8437.79	381.89
218	SEG14	8480.79	381.89
219	SEG13	8523.79	381.89
220	SEG12	8566.79	381.89
221	SEG11	8609.79	381.89
222	SEG10	8652.79	381.89
223	SEG9	8695.79	381.89
224	SEG8	8738.79	381.89
225	SEG7	8781.79	381.89
226	SEG6	8824.79	381.89
227	SEG5	8867.79	381.89
228	SEG4	8910.79	381.89
229	SEG3	8953.79	381.89
230	SEG2	8996.79	381.89
231	SEG1	9039.79	381.89
232	SEG0	9082.79	381.89
233	COM0	9182.79	381.89
234	COM1	9225.79	381.89
235	COM2	9268.79	381.89
236	COM3	9311.79	381.89

PAD No.	PAD Name	X	Y
237	COM4	9354.79	381.89
238	COM5	9397.79	381.89
239	COM6	9440.79	381.89
240	COM7	9483.79	381.89
241	COM8	9526.79	381.89
242	COM9	9569.79	381.89
243	COM10	9612.79	381.89
244	COM11	9655.79	381.89
245	COM12	9698.79	381.89
246	COM13	9741.79	381.89
247	COM14	9784.79	381.89
248	COM15	9827.79	381.89
249	COM16	9870.79	381.89
250	COM17	9913.79	381.89
251	COM18	9956.79	381.89
252	COM19	9999.79	381.89
253	COM20	10042.79	381.89
254	COM21	10085.79	381.89
255	COM22	10128.79	381.89
256	COM23	10171.79	381.89
257	COM24	10214.79	381.89
258	COM25	10257.79	381.89
259	COM26	10300.79	381.89
260	COM27	10343.79	381.89
261	COM28	10386.79	381.89
262	COM29	10429.79	381.89
263	COM30	10472.79	381.89
264	COM31	10515.79	381.89
265	COM32	10558.79	381.89
266	COM33	10601.79	381.89
267	COM34	10644.79	381.89
268	COM35	10687.79	381.89
269	COM36	10730.79	381.89
270	COM37	10773.79	381.89
271	COM38	10816.79	381.89
272	COM39	10859.79	381.89
273	COM40	10902.79	381.89
274	COM41	10945.79	381.89
275	COM42	10988.79	381.89
276	COM43	11031.79	381.89
277	COM44	11074.79	381.89
278	COM45	11117.79	381.89
279	COM46	11160.79	381.89
280	COM47	11203.79	381.89
281	COM48	11246.79	381.89
282	COM49	11289.79	381.89
283	COM50	11332.79	381.89
284	Dummy	11375.79	381.89

PAD No.	PAD Name	X	Y
285	Dummy	11418.79	381.89
286	Dummy	11461.79	381.89
287	Dummy	11504.79	381.89
288	Dummy	11547.79	381.89
289	Dummy	11590.79	381.89
290	COM51	11752.79	364.39
291	COM52	11752.79	321.39
292	COM53	11752.79	278.39
293	COM54	11752.79	235.39
294	COM55	11752.79	192.39
295	COM56	11752.79	149.39
296	COM57	11752.79	106.39
297	COM58	11752.79	63.39
298	COM59	11752.79	20.39
299	COM60	11752.79	-22.61
300	COM61	11752.79	-65.61
301	COM62	11752.79	-108.61
302	COM63	11752.79	-151.61
303	COM64	11752.79	-194.61
304	COM65	11752.79	-237.61
305	Dummy	11594.29	-280.61
306	Dummy	11490.54	-280.61
307	Dummy	11386.79	-280.61
308	Dummy	11308.04	-280.61
309	MV1	11229.29	-280.61
310	MV1	11124.29	-280.61
311	MV1	11019.29	-280.61
312	V1	10914.29	-280.61
313	V1	10809.29	-280.61
314	V1	10704.29	-280.61
315	V3OUT	10599.29	-280.61
316	V3OUT	10494.29	-280.61
317	V3OUT	10389.29	-280.61
318	V3IN	10284.29	-280.61
319	V3IN	10179.29	-280.61
320	V3IN	10074.29	-280.61
321	V3IN	9969.29	-280.61
322	V3S	9864.29	-280.61
323	MV3S	9759.29	-280.61
324	MV3IN	9654.29	-280.61
325	MV3IN	9549.29	-280.61
326	MV3IN	9444.29	-280.61
327	MV3IN	9339.29	-280.61
328	MV3OUT	9234.29	-280.61
329	MV3OUT	9129.29	-280.61
330	MV3OUT	9024.29	-280.61
331	CB1N	8866.79	-280.61
332	CB1N	8761.79	-280.61
333	CB1N	8656.79	-280.61
334	CB1P	8551.79	-280.61
335	CB1P	8446.79	-280.61
336	CB1P	8341.79	-280.61
337	CA2N	8236.79	-280.61
338	CA2N	8131.79	-280.61
339	CA2N	8026.79	-280.61
340	CA2N	7921.79	-280.61
341	CA2P	7816.79	-280.61
342	CA2P	7711.79	-280.61
343	CA2P	7606.79	-280.61
344	CA2P	7501.79	-280.61
345	CA1N	7396.79	-280.61
346	CA1N	7291.79	-280.61
347	CA1N	7186.79	-280.61
348	CA1N	7081.79	-280.61
349	CA1P	6976.79	-280.61
350	CA1P	6871.79	-280.61
351	CA1P	6766.79	-280.61
352	CA1P	6661.79	-280.61
353	NVDD	6556.79	-280.61
354	NVDD	6451.79	-280.61
355	NVDD	6346.79	-280.61
356	NVDD	6241.79	-280.61
357	NVDD	6136.79	-280.61
358	NVDD	6031.79	-280.61
359	TCAP	5926.79	-280.61
360	Vref	5848.04	-280.61
361	VSS3	5769.29	-280.61
362	VSS1	5664.29	-280.61
363	VSS1	5559.29	-280.61
364	VSS1	5454.29	-280.61
365	VSS2	5349.29	-280.61
366	VSS2	5244.29	-280.61
367	VSS2	5139.29	-280.61
368	VSS2	5034.29	-280.61
369	VSS2	4929.29	-280.61
370	VC	4824.29	-280.61
371	VC	4719.29	-280.61
372	VDD2	4614.29	-280.61
373	VDD2	4509.29	-280.61
374	VDD2	4404.29	-280.61
375	VDD2	4299.29	-280.61
376	VDD2	4194.29	-280.61
377	VDD1	4089.29	-280.61
378	VDD1	3984.29	-280.61
379	VDD1	3879.29	-280.61
380	VDD3	3774.29	-280.61

PAD No.	PAD Name	X	Y
381	VDI	3669.29	-280.61
382	VDI	3564.29	-280.61
383	VDI	3459.29	-280.61
384	EXTB	3354.29	-280.61
385	D7	3249.29	-280.61
386	D6	3144.29	-280.61
387	D5	3039.29	-280.61
388	D4	2934.29	-280.61
389	D3	2829.29	-280.61
390	D2	2724.29	-280.61
391	D1	2619.29	-280.61
392	D0	2514.29	-280.61
393	VDD1	2435.54	-280.61
394	RWR	2356.79	-280.61
395	ERD	2251.79	-280.61
396	Reserved	2146.79	-280.61
397	A0	2041.79	-280.61
398	RSTB	1936.79	-280.61
399	VDD1	1858.04	-280.61
400	CS2	1779.29	-280.61
401	CS1B	1674.29	-280.61
402	VSS1	1595.54	-280.61
403	IF1	1516.79	-280.61
404	IF2	1411.79	-280.61

PAD No.	PAD Name	X	Y
405	VDD1	1333.04	-280.61
406	M/S	1254.29	-280.61
407	VSS1	1175.54	-280.61
408	ITR	1096.79	-280.61
409	CLS	991.79	-280.61
410	VDD1	913.04	-280.61
411	SYNC	834.29	-280.61
412	CL	729.29	-280.61
413	DOFB	624.29	-280.61
414	LED1	519.29	-280.61
415	LED2	414.29	-280.61
416	LED3	309.29	-280.61
417	VPP	204.29	-280.61
418	VPP	99.29	-280.61
419	Dummy	20.54	-280.61
420	Dummy	-58.21	-280.61
421	Dummy	-161.96	-280.61
422	Dummy	-265.71	-280.61

Note:

1. Unit: um
2. Tolerance: +/- 0.05 um.

4. BLOCK DIAGRAM

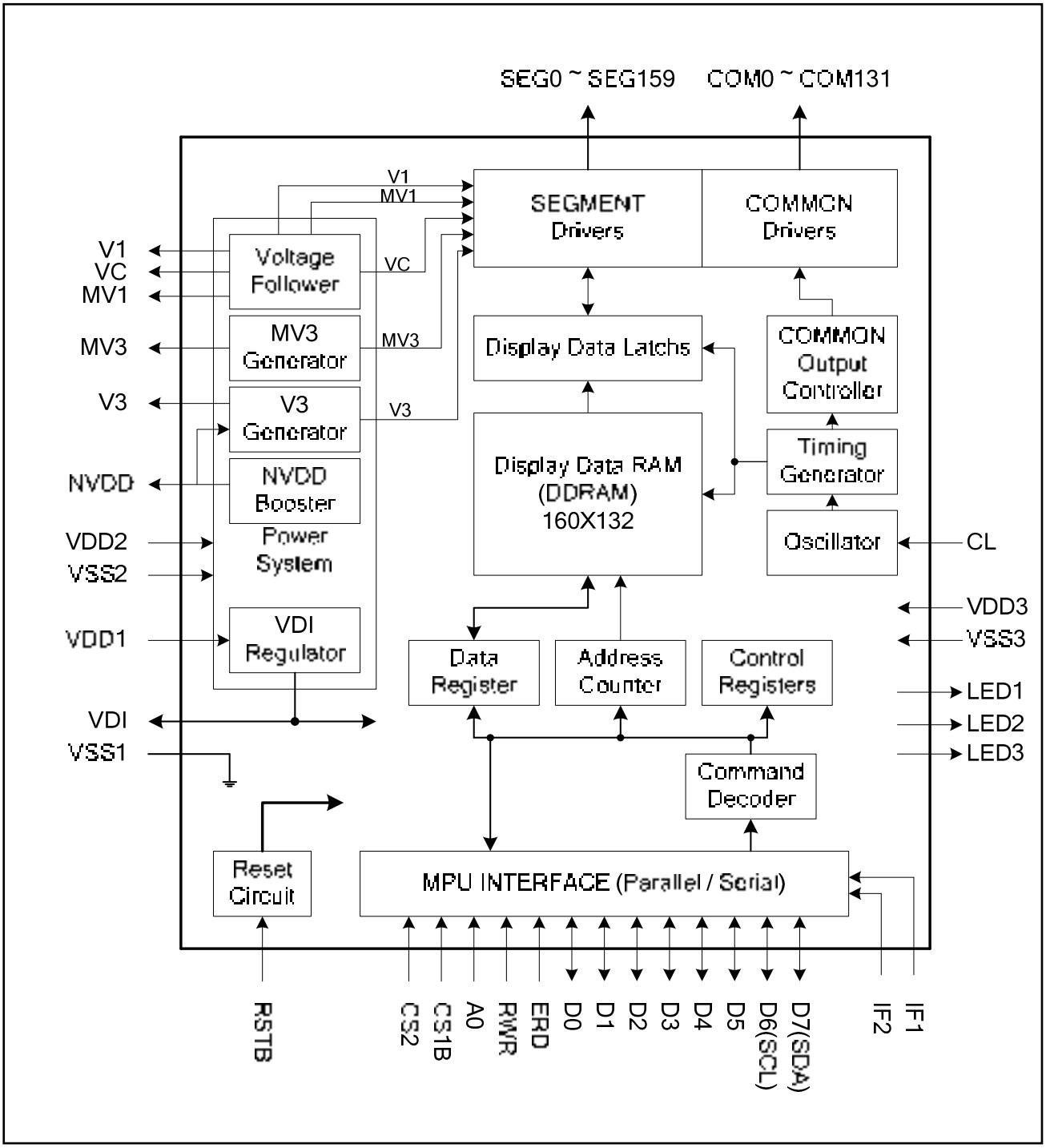


Fig. 1. Block Diagram

5. PIN DESCRIPTION

Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>IF[2:1]</td><td>I</td><td>IF2 selects the interface mode (Serial or Parallel), while IF1 selects the microprocessor type in parallel interface mode (8080-series or 6800-series).
<table>
<tr><th>IF2</th><th>IF1</th><th>Selected Interface</th></tr>
<tr><td>“H”</td><td>“H”</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>Serial 4-Line SPI Interface</td></tr>
<tr><td>“L”</td><td>“L”</td><td>Reserved (do NOT use)</td></tr>
</table>
Please refer to “APPLICATION NOTES” and “Microprocessor Interface” (Section 6) for detailed connection of the selected interface.</td></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin, when RSTB is “L”, initialization is executed.</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select pins. Interface is enabled when both CS1B is “L” and CS2 is “H”. If chip select pins are not active (CS1B=“H” or CS2=“L”), D0 to D7 become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H”: Indicates that signals on D[7:0] are display data.
A0=“L”: Indicates that signals on D[7:0] are command.</td></tr>
<tr><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When chip select pins are not active (CS1B=“H” or CS2=“L”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I</td><td>When using serial interface: 4-LINE
D7=SDA : Serial data input.
D6=SCL : Serial clock input.
D[5:0] are not used and should connect to “H” by VDD1.
When chip select pins are not active (CS1B=“H” or CS2=“L”), D[7:0] pins are high impedance.</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When IF2 is “H”,
<table>
<tr><th>IF1</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is not used in serial interface and should fix to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When IF2 is “H”,
<table>
<tr><th>IF1</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is not used in serial interface and should fix to “H” by VDD1.</td></tr>
</table>

Note: After VDD1 is turned ON, any MPU interface pins cannot be left floating.

LCD Driver Related Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>ITR</td><td>I</td><td>When ITR=“H” (VDD1), the interlace mode is enabled.
When ITR=“L” (VSS1), the interlace mode is disabled.</td></tr>
<tr><td>M/S</td><td>I</td><td>This pin controls the Master/Slave function.
M/S=“H” (VDD1): IC is in Master mode.
M/S=“L” (VSS1): IC is in Slave mode.
The Master/Slave mode defines the operation of the following pins.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th><th>Internal Clock</th><th>Power Circuits</th><th>SYNC, DOFB</th></tr>
<tr><td>H</td><td>H</td><td>Output</td><td>ON</td><td>ON *2</td><td>Output</td></tr>
<tr><td>L</td><td>L</td><td>Input *1</td><td>OFF *1</td><td>OFF *2</td><td>Input</td></tr>
</table>
Note:
1. Input from master (by CL pin).
2. The default setting uses internal power circuits of master.
3. The ITO resistance maybe causes uneven display quality. Therefore, Master/Slave is only for TCP/COF applications.</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>This pin is used to synchronize the LCD driver output timing between the master IC and the slave IC.</td></tr>
<tr><td>DOFB</td><td>I/O</td><td>This signal forces the slave IC into the Display-OFF state.</td></tr>
<tr><td>SEG[0:159]</td><td>O</td><td>LCD segment driver outputs. One of the V1, VC and MV1 levels is selected by a combination of the DDRAM data and control signals.</td></tr>
<tr><td>COM[0:131]</td><td>O</td><td>LCD common driver outputs. One of the V3, VC and MV3 levels is selected by a combination of the scan signal and field signals.</td></tr>
<tr><td>LED[1:3]</td><td>O</td><td>These pins provide LED control singles for LED backlight system.
Please note these pins are control signals. They are not LED power pins.</td></tr>
</table>

Power Supply Pins

Pin Name	Type	Description
VDD1	**Power**	Power supply for digital circuit and RAM circuit.
VSS1	**Power**	Ground for digital circuit and RAM circuit.
VDD2	**Power**	Power supply for analog circuit.
VSS2	**Power**	Ground for analog circuit. Ground system should be connected together by FPC.
VDD3	**Power**	Power of internal oscillator & Vref circuits. It is the same voltage level as VDD1. Connect with VDD1 by FPC externally.
VSS3	**Power**	Ground of internal oscillator & Vref circuits. Connect with VSS1 by FPC externally.

Clock System Pins

Pin Name	Type	Description
CLS	**I**	Clock source selection pin. CLS="H" (VDD1): enable internal clock. CLS="L" (VSS1): disable internal clock and use external clock.
CL	**I/O**	If CLS="H", the internal clock will be outputted to this pin. If CLS="L", this pin should apply the external clock (typical 1630KHz).

LCD Power System Pins

Pin Name	Type	Description
NVDD	**Power**	The negative power for analog circuit.
VDI	**Power**	This pin is reserved to monitor internal logic power status only.
V3OUT V3IN V3S	**Power**	LCD driver supply power. V3OUT is the output of the built-in V3 generator. V3IN is one of the voltage sources for COM driver circuits. V3S is the feedback pin of the built-in V3 generator. It senses the V3 voltage. V3OUT, V3IN & V3S should be connected together at FPC side.
MV3OUT MV3IN MV3S	**Power**	LCD driver supply power. MV3OUT is the output of the built-in MV3 generator. MV3IN is one of the voltage sources for COM driver circuits. MV3S is the feedback pin of the built-in MV3 generator. It senses the MV3 voltage. MV3OUT, MV3IN & MV3S should be connected together at FPC side.
V1, MV1	**Power**	These pins are LCD driver supply powers for different output levels. If using internal power circuits, these powers can be controlled by instructions. These powers should have the following relationship: V3 ≥ V1 ≥ VC (VSS2) ≥ MV1 ≥ MV3
VC	**Power**	LCD driver supply power for center level. Connect to VSS2 by system circuit externally.
CA1P, CA1N CA2P, CA2N	**Power**	Positive and negative sides of the booster capacitor. These are the booster capacitors for NVDD.
CB1P, CB1N	**Power**	Positive and negative sides of the booster capacitor. This is the booster capacitor for MV3.

Test Pins

Pin Name	Type	Description
VPP	**Power**	When writing PROM, it needs external power supply voltage 7.0V (>4mA) input to write successfully.
EXTB	**I**	The erase/write operation of the internal PROM can be executed only when EXTB="L" (VSS1). ***Note: This pin has an internal pull-up resistor and should be left OPEN (default) when not erasing/writing.***
Vref	**Test**	Reference voltage output for monitor only. Let it open.
TCAP	**Test**	Let it open.
Reserved	**-**	These pins are reserved only. Please don't connect these pins.

Recommend ITO Resistance (for COG applications)

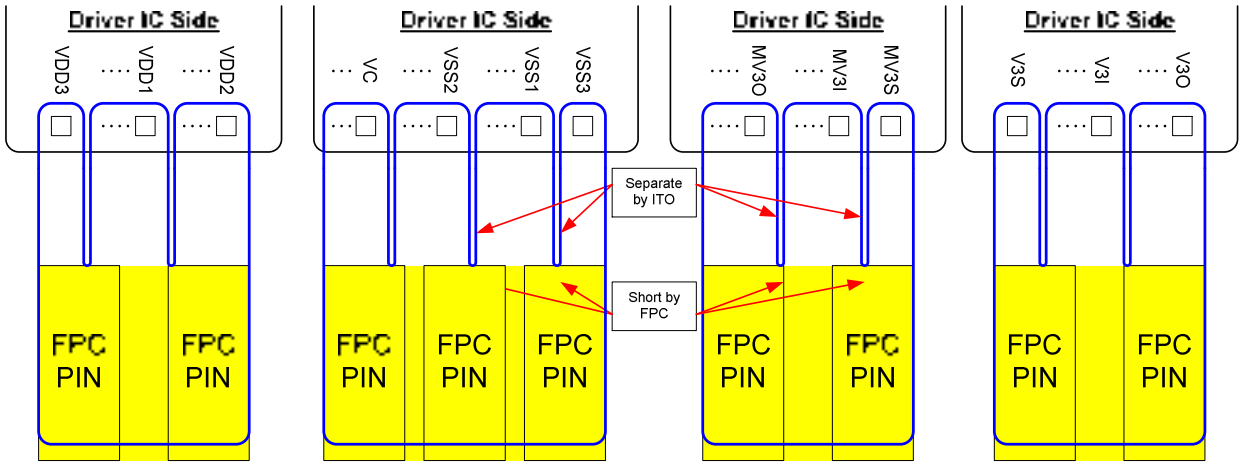
Pin Name	ITO Resistance
Vref, TCAP, LED[3:1]	Floating
VDD1, VDD2, VDD3, VDI, VSS1, VSS2, VSS3, VPP, VC	< 100Ω *3
CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, V3, V1, MV1, MV3, NVDD	< 300Ω *3
A0, RWR, ERD, CS1B, CS2, EXTB, D[7:0]	< 1KΩ
SYNC, DOFB, CL	< 3KΩ *3
ITR, M/S, IF[2:1], CLS	< 5KΩ
RSTB *1	< 10KΩ

Note:

1. It is recommended to keep the resistance of RSTB pin larger than 3KΩ (and less than 10KΩ).
2. The option setting to be "H" should connect to VDD1, and the option setting to be "L" should connect to VSS1.
3. For COG application using Master/Slave function, please keep the ITO resistance half of the table (except VPP).

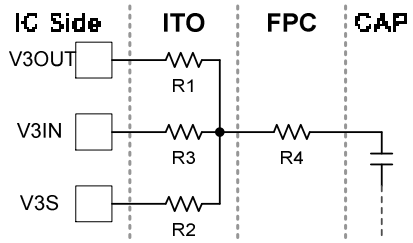
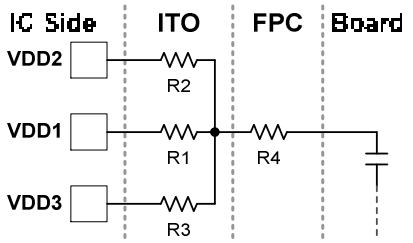
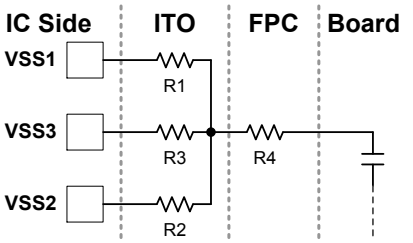
ITO Layout Notes:

1. Make sure that the ITO resistance of COM0 ~ COM131 is equal, and so is it of SEG0 ~ SEG159. These Limitations include the bottleneck of ITO layout.
2. To avoid the noise in different power system affect other power system, please separate them by ITO layout.
3. The V3 and MV3 power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.



Note:

- The bottleneck of ITO layout limits power system efficiency. Please try to avoid it.
- Exception condition: if the separating of ITO causes large resistance, please short the ITO before connecting to FPC. In this way, some of the ITO resistance will be reduced. The equivalent circuit is shown below:

V3 & MV3	*VDD*	*VSS*
		
Ideal Layout (short at FPC)	**Ideal Layout (short at FPC)**	**Ideal Layout (short at FPC)**
=> R4=0 Ohm. R2>>R1>R3.	=> R4=0 Ohm. R3>>R1>R2.	=> R4=0 Ohm. R3>>R1>R2.
Acceptable Layout (short at ITO end)	**Acceptable Layout (short at ITO end)**	**Acceptable Layout (short at ITO end)**
=> R4≠0. R2>>R1>R3>R4.	=> R4≠0. R3>>R1>R2>R4.	=> R4≠0. R3>>R1>R2>R4.
Not Acceptable:	**Not Acceptable:**	**Not Acceptable:**
=> R4 ≥ (R1 or R2 or R3).	=> R4 ≥ (R1 or R2 or R3).	=> R4 ≥ (R1 or R2 or R3).

6. FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

ST7591 has 2 chip-select pins: CS1B & CS2. When both of them are acted (CS1B="L" & CS2="H"), this IC is selected and the MPU interface is enabled to interface with MPU. When this IC is NOT selected (CS1B="H" or CS2="L"), the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance.

Interface Selection

ST7591 has 3 interface modes for MPU communication. IF2 determines parallel or serial mode as shown in Table 1.

Table 1. Parallel/Serial Interface Mode

IF2	IF1	CS1B	CS2	A0	ERD	RWR	D[7:0]	MPU Interface
"H"	"H"	CS1B	CS2	A0	E	R/W	D[7:0]	6800-series parallel interface
"H"	"L"				/RD	/WR		8080-series parallel interface
"L"	"H"				---	---	Refer to serial interface.	4-Line SPI interface

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1.

Parallel Interface

When IF2= "H", the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by "IF1" pin as shown in Table 2. The data transfer type is determined by signals on A0, ERD and RWR as shown in Table 3.

Table 2. Microprocessor Selection for Parallel Interface

IF2	IF1	CS1B	CS2	A0	ERD	RWR	D[7:0]	MPU Interface
"H"	"H"	CS1B	CS2	A0	E	R/W	D[7:0]	6800-series parallel interface
"H"	"L"				/RD	/WR		8080-series parallel interface

Table 3. Parallel Data Transfer Type

Common Pins			6800-Series		8080-Series		Description
CS1B	CS2	A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
"L"	"H"	"H"	"H"	"H"	"L"	"H"	Display data read out
		"H"	"H"	"L"	"H"	"L"	Display data write
		"L"	"H"	"H"	"L"	"H"	Internal status read
		"L"	"H"	"L"	"H"	"L"	Writes to internal register (instruction)

Setting Serial Interface

Serial Mode	IF2	IF1	CS1B	CS2	A0	ERD	RWR	D7	D6	D[5:0]
4-Line SPI interface	"L"	"H"	CS1B	CS2	A0	---	---	SDA	SCLK	---

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1.

Note:

1. The option setting to be "H" should connect to VDD1, and the option setting to be "L" should connect to VSS1.
2. Some MPU will set interface pins to be Hi-Z (high impedance) mode during power-save mode or after hardware reset. This is not allowed when the VDD1of ST7591 is turned ON. Because the floating input (especially for those control pins such as CS1B, CS2, RSTB, RWR or ERD…) maybe cause abnormal latch and cause abnormal display.

4-Line SPI interface (IF[2:1]="L,H")

When ST7591 is selected (CS1B="L" & CS2="H"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7591 is not selected (CS1B="H" or CS2="L"), the internal 8-bit shift register and 3-bit serial counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the received 8-bit parallel data is display data or instruction. A0="H" indicates the received 8-bit parallel data is display data, while A0="L" indicates it is instruction. The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCLK signal quality is very important and external noise maybe causes unexpected data/instruction latch.

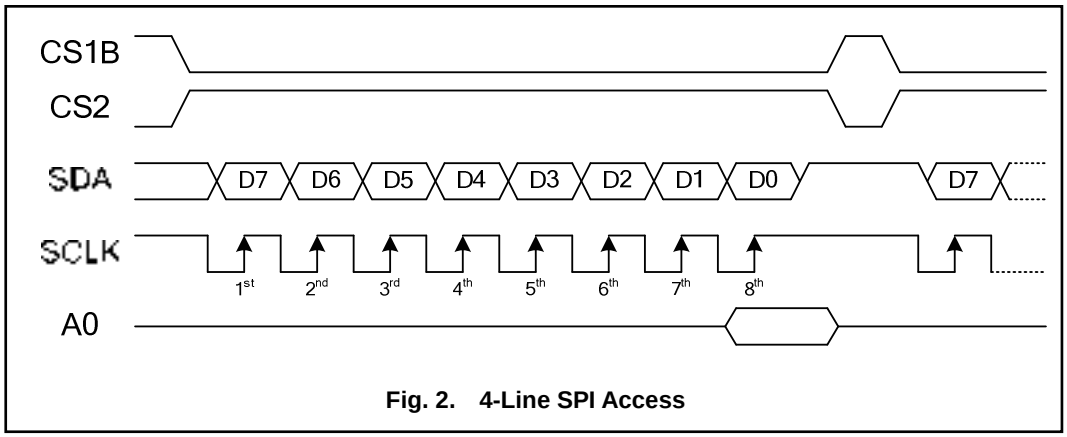


Fig. 2. 4-Line SPI Access

Data Transfer

ST7591 uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig. 3. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig. 4. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

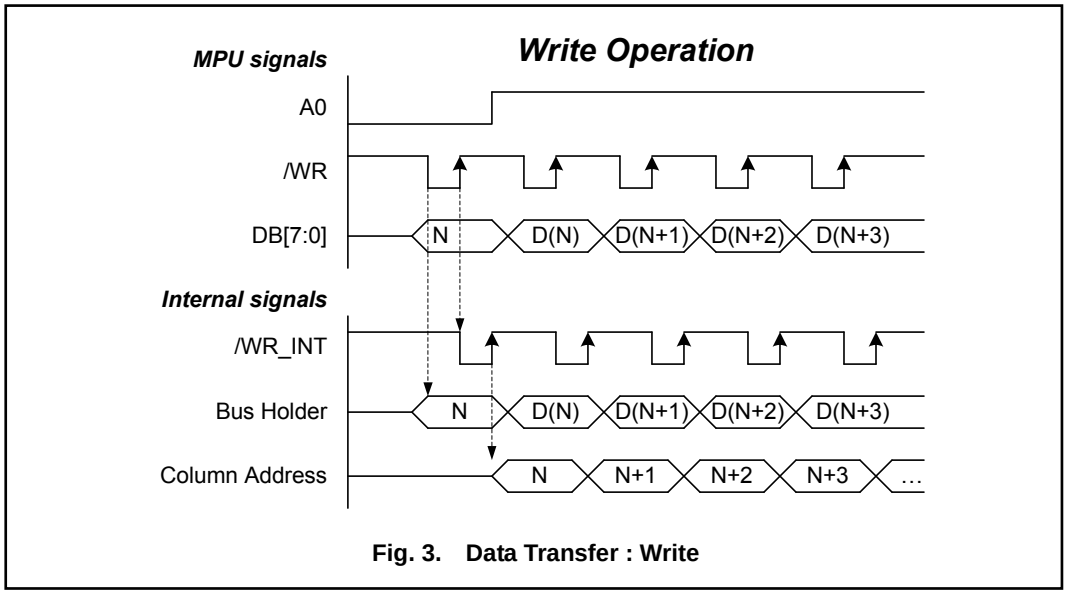


Fig. 3. Data Transfer : Write

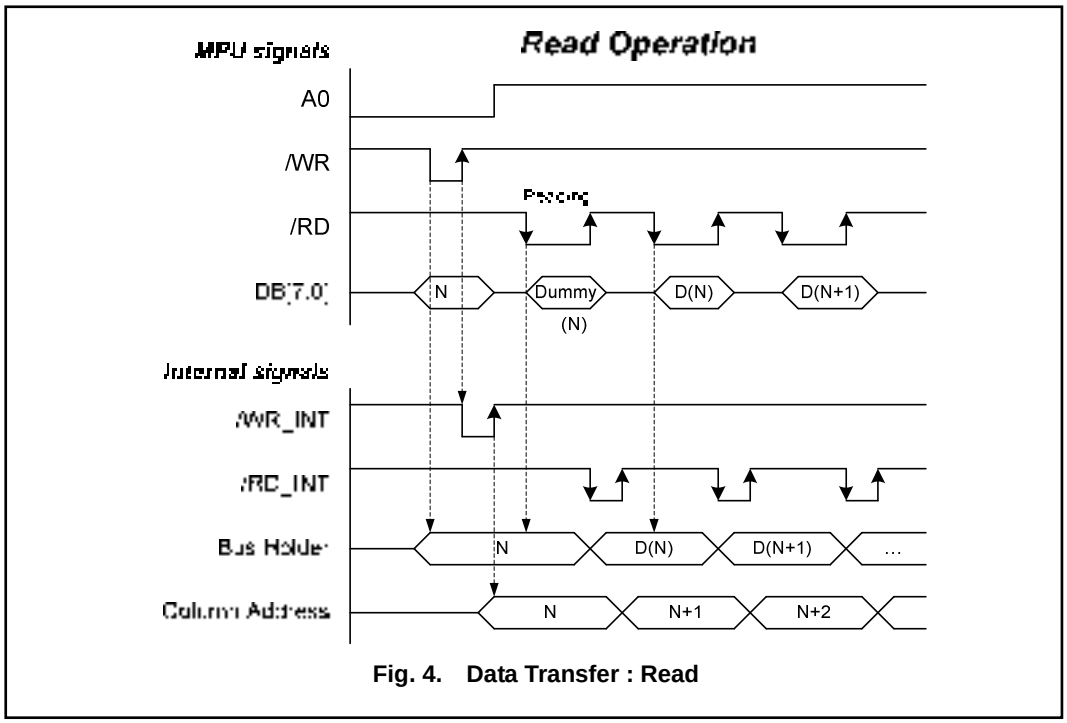


Fig. 4. Data Transfer : Read

Display Data RAM (DDRAM)

When the data bit in DDRAM is “1”, the segment driver will output ON voltage. If it is “0”, the segment driver will output OFF voltage. It is an addressable array with 160 columns by 132 rows (16-page with 8-bit and 1-page with 4-bit only). The column address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (refer to Fig. 5 for detailed illustration). The rows are divided into: 16 pages (Page-0 ~ Page-15) with 8 lines (for COM0~127) per page and 1 page (Page-16) with 4 lines (for COM128~131). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on the top. Page 0~15 can be accessed through D[7:0] directly while Page-16 can be accessed through D[3:0] only (refer to Fig. 6 for detailed illustration). The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

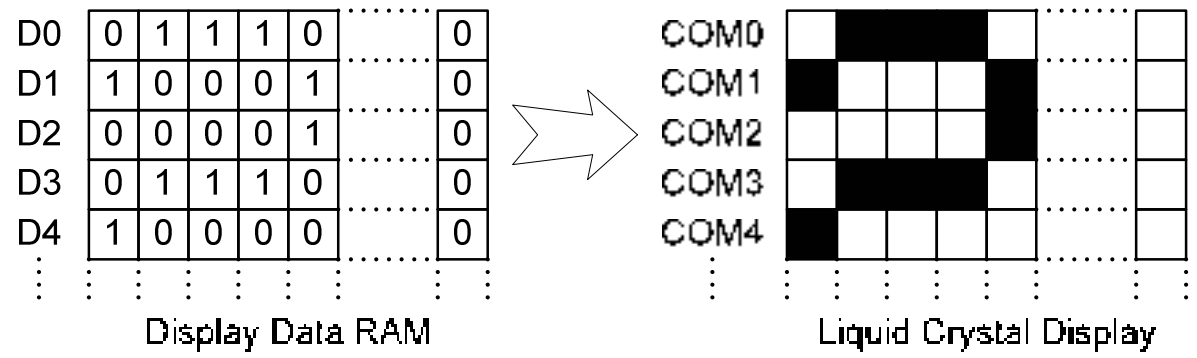


Fig. 5. DDRAM Mapping Mode (Default Setting)

Fig. 6. DDRAM Format

Display Data Latch Circuit

The display data larch circuit is a latch to temporarily latch the display, data output from then display data RAM to the liquid crystal drive circuit. Display normal/reverse, display ON/OFF, and display all lighting ON/OFF commands control the data in this latch, without the data in the display data RAM being controlled.

Addressing

Data is downloaded into the Display Data RAM matrix in ST7591 as byte-format. The Display Data RAM has a matrix of 160 x 132 bits. The address ranges are: X=0~159 (column address), Y=0~16 (page address). Addresses outside these ranges are not allowed.

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Set Page Address” instruction only. The Page Address must be set before accessing DDRAM content.

Column Address Circuit

The column address of DDRAM can be specified by “Set Column Address” instruction. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “9Fh”) because the address out of range is invalid. That means: both Page Address and Column Address should be assigned again if user wants to change the address pointers from the end of Page-0 to the beginning of Page-1 (from Page-0, Column-9Fh to Page-1, Column-0h).

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG) pads. It is necessary to rewrite the display data into DDRAM after changing MX setting.

Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the “Set Start Line” instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, it can realize the screen scrolling without changing the contents of DDRAM.

The relation between DDRAM and outputs with different MX or MY setting is shown below.

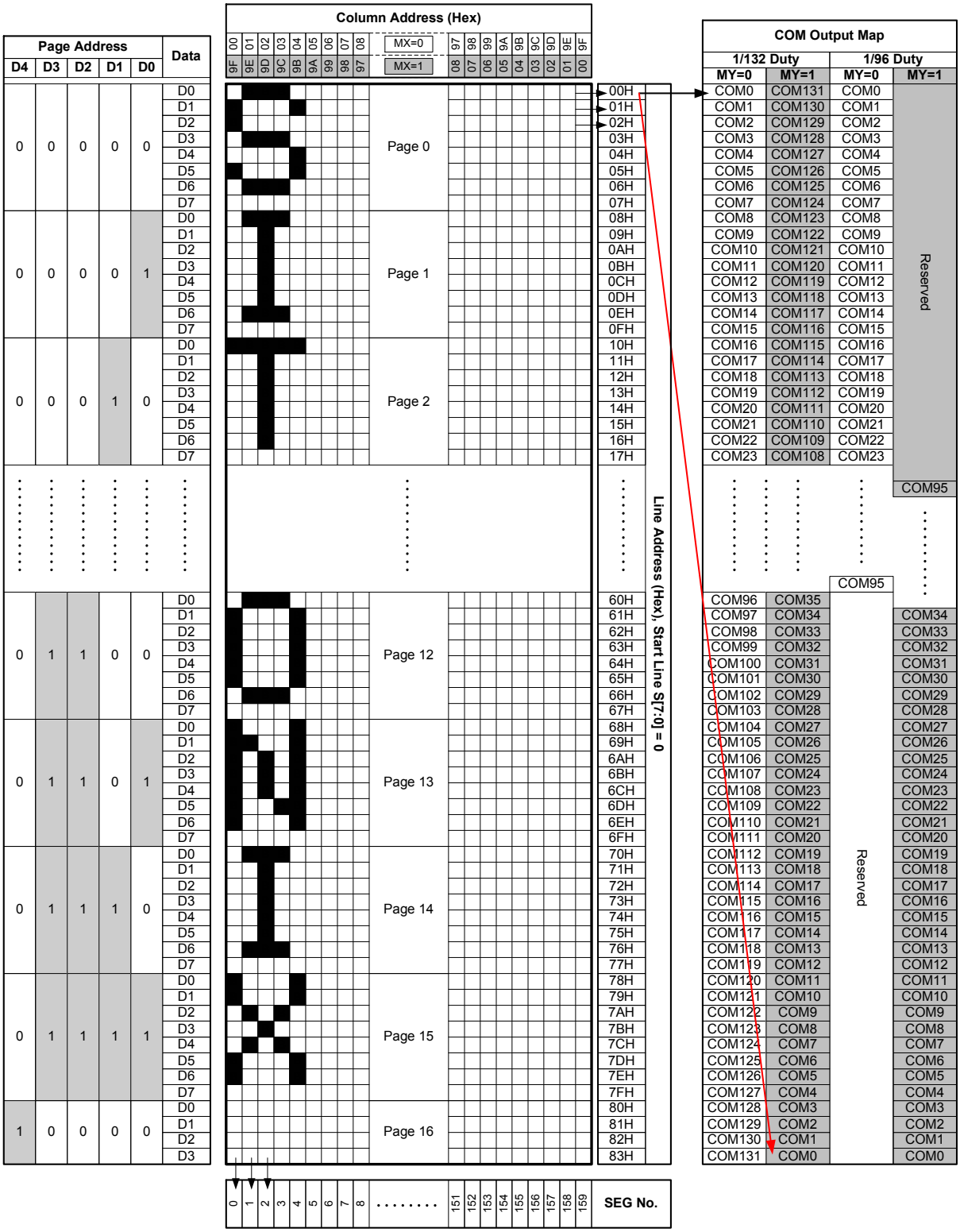


Fig. 7. DDRAM and Output Map (COM/SEG)

Oscillation Circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, connect CLS to VDD1; when the external oscillator is used, connect CLS to VSS1 and input external clock to CL pin. This oscillator signal is used by the voltage booster and display timing generation circuit.

Power System

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external components. The built-in power system has negative-power generator, voltage booster, voltage regulator and voltage follower circuits. Before turning power OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

External Components of Power Circuit

The external power components are shown below. The optimized value depends on the panel size and loading.

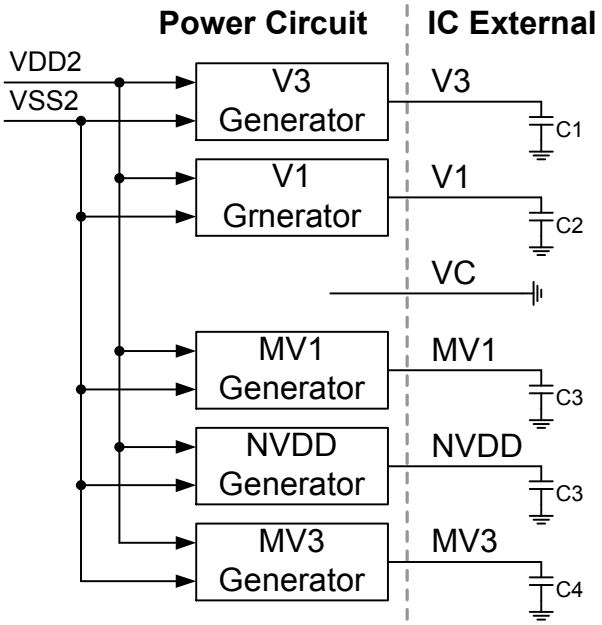


Fig. 8. LCD Power Circuits

Regulator Circuit

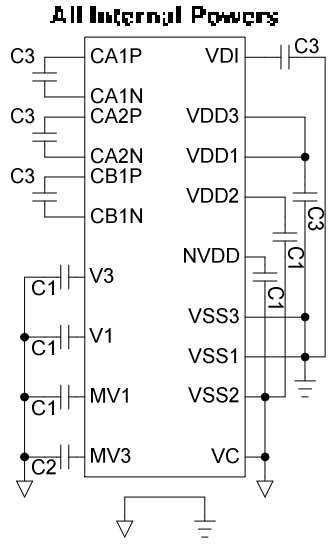
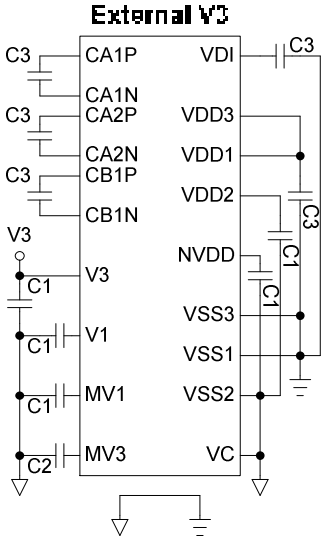
The built-in high accuracy regulator is used for Vop voltage adjustment. Its accuracy can be calibrated by built-in PROM. The detailed information for Vop setting is in “Set Vop” (Page 32) of Section 9. INSTRUCTION DESCRIPTION. With the help of the built-in temperature sensor, its temperature compensation can be customized. The output voltage can also be changed by instructions such as “Set Vop”, “Set TC Curve”, “Set TC Flag” and “Set FR TC Hysteresis”…

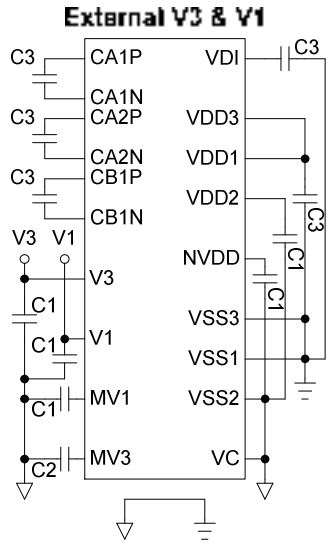
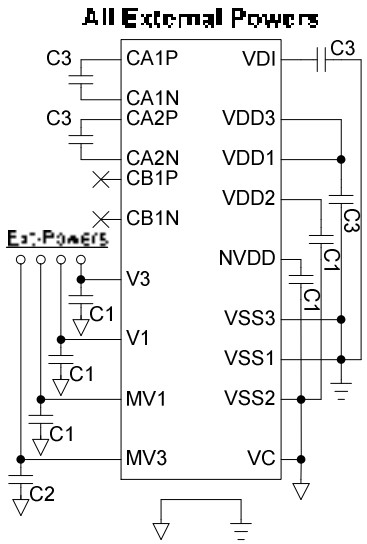
Power Application

Application Condition	Power Control Setting	Note
Use internal power circuits	(VN,VB,VR,VF)=(1,1,1,1)	NVDD, V3, V1, MV1 & MV3 are generated by IC.
Use external regulator	(VN,VB,VR,VF)=(1,0,1,1)	Apply external Vop to V3. NVDD, V1, MV1 & MV3 are generated by IC.
Use external V3, V1, MV3 & MV1	(VN,VB,VR,VF)=(1,0,0,0)	Apply external power to V3, V1, MV3 & MV1

Power Circuits Configuration

The hardware connections and their software settings are listed below (including Power ON Control Flow). Be sure the hardware connection and the software setting should be both correct.

<table>
<tr><th>Case 1 [All Internal Power Circuits]</th><th>Case 2 [External Regulator]</th></tr>
<tr><td>[Hardware Connection]
 
</td><td>[Hardware Connection]
 
</td></tr>
<tr><td>[Software Setting]
Power Control: VN=VB=VR=VF=1
Power Control Flow
Power Control: VN=1, VR=VR=VF=0
Delay_20ms
Power Control: VN=VB=1 VR=VF=0
Delay_50ms
Power Control: VN=VB=VR=1 VF=0
Delay_20ms
Power Control: VN=VB=VR=VF=1
Delay_40ms</td><td>[Software Setting]
Power Control: VN=1, VB=0, VR=VF=1
Power Control Flow
Power Control: VN=1, VR=VR=VF=0
Delay_20ms
External Booster ON
Delay (wait external Booster rising)
External Regulator ON
Delay (wait external V3 stable)
Power Control: VN=1, VB=0, VR=VF=1
Delay_40ms</td></tr>
<tr><td>[Related Features]
Contrast Control: Software Control
Vop Adjustment: Adjust by Internal PROM
Bias Control: Software Control
Vop Temperature Compensation: Software Defined
fFR Temperature Compensation: Software Defined</td><td>[Related Features]
Contrast Control: External Circuit
Vop Adjustment: External Circuit
Bias Control: Software Control
Vop Temperature Compensation: External Circuit
fFR Temperature Compensation: Software Defined</td></tr>
</table>

Case 3 [External Regulator & Follower]	*Case 4 [All External Power Circuits]*
[Hardware Connection] 	**[Hardware Connection]** 
[Software Setting] Power Control: VN=1, VB=VR=0, VF=1 Power Control Flow Power Control: VN=1, VB=VR=VF=0 Delay_20ms External Booster ON Delay (wait external Booster rising) External Regulator ON Delay (wait external V3 stable) Power Control: VN=1, VB=VR=0, VF=1 Delay_40ms	**[Software Setting]** Power Control: VN=1, VB=VR=0VF=0 Power Control Flow Power Control: VN=1, VB=VR=VF=0 Delay_20ms External Booster & Regulator ON Delay (wait external V3 stable) External Negative Regulator ON Delay (wait external MV3 stable) External Negative Follower ON Delay (wait MV1 stable)
[Related Features] Contrast Control: External Circuit Vop Adjustment: External Circuit Bias Control: External Circuit (fixed) Vop Temperature Compensation: External Circuit fFR Temperature Compensation: Software Defined **This case uses positive powers**.	**[Related Features]** Contrast Control: External Circuit Vop Adjustment: External Circuit Bias Control: External Circuit (fixed) Vop Temperature Compensation: External Circuit fFR Temperature Compensation: Software Defined **This case uses negative powers**.

For different kind of power applications, the external power should be applied after hardware reset. And the power should be stable before turning the display ON.

[External Capacitor Parameter]

Cap.	Typical Value	Capacitor Range	Voltage Rating
C1	4.7uF	1uF ~ 4.7uF	16V
C2	2.2uF	1uF ~ 2.2uF	16V
C3	1uF	0.47uF ~ 1uF	16V (for simple selection, all C3 capacitors use 16V)

Note: C3 of VDI can use 1uF/6.3V and C3 of VDDI (VDD1 & VDD3) can use 1uF/10V.

7. RESET CIRCUIT

Setting RSTB to “L” or SRESET instruction can initialize internal function.
When RSTB becomes “L”, following procedure is occurred.
Page address: 0
Column address: 0
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Display Line: 132 lines
Reverse display ON / OFF: OFF (normal)
N-line inversion register: 0 (disable)
Power control register (VN=0, VB=0, VR=0, VF=0)
Booster Level = (2*VDD2) x2
TC Control: OFF
Contrast Level: 00h
LCD bias ratio: 1/3
COM Scan Direction: 0
SEG Scan Direction: 0
Oscillator: OFF
Power Save Mode: Release
Read-modify-Write mode: Exit
Test Mode: Exit (TE=0, T[1:0]=0)

When SRESET instruction is issued, following procedure is occurred.
Page address: 0
Column address: 0
Initial display line: 0 (First)
Contrast Level: 00h
Read-modify-Write mode: Exit
Test Mode: Exit (TE=0, T[1:0]=0)

After power-on, DDRAM data are undefined and the display status is “Display OFF”. It’s recommended to initialize the whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. After the power is stable, a hardware reset is required to initialize internal registers. After the system power ON, the internal status can NOT be determined before a valid hardware reset.

8. INSTRUCTION TABLE

Basic Instruction (TE=0, T[1:0]= don't care)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Read Data	1	1	Data Read								Read display data from DDRAM
Write Data	1	0	Data Write								Write display data to DDRAM
Read Status	0	1	BSY	MX	D	RST	VN	VB	VF	Disv	Read IC Status
Set Page Address	0	0	0	1	1	1	1	1	0	0	Set page address
	0	0	0	0	0	Y4	Y3	Y2	Y1	Y0	
Set X Address (LSB)	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
Set X Address (MSB)	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
Power Control	0	0	1	0	0	1	VN	VB	VR	VF	Set built-in power blocks ON/OFF
Oscillator ON/OFF	0	0	1	0	1	0	1	0	1	OSC	The built-in oscillator ON/OFF
Set Start Line	0	0	1	1	0	1	0	0	0	0	Double command!! Set display start line of DDRAM
	0	0	S7	S6	S5	S4	S3	S2	S1	S0	
Set COM0	0	0	1	1	0	1	0	0	1	1	Double command!! Select COM0 output pad
	0	0	C7	C6	C5	C4	C3	C2	C1	C0	
Set Display Line	0	0	1	1	0	1	1	1	0	0	Double command!! Set display lines
	0	0	P7	P6	P5	P4	P3	P2	P1	P0	
Bias Select	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Set Booster	0	0	0	1	1	0	0	1	BL1	BL0	Set booster level
Set Vop	0	0	1	0	0	0	0	0	0	1	Double command!! Set Vop level
	0	0	V7	V6	V5	V4	V3	V2	V1	V0	
SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse; MX=0, normal
All Pixels ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixels ON AP=0, normal display
Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
Display ON/OFF	0	0	1	0	1	0	0	0	1	D	D=1, display ON D=0, display OFF
Set Power Save	0	0	0	1	0	1	1	0	0	PD	Set power save mode: PD=1: Standby; PD=0: Normal
Discharge ON/OFF	0	0	0	0	1	1	0	1	1	Disv	Discharge Power supply circuit
COM Direction	0	0	1	1	0	0	MY	0	0	0	Set output direction of COM MY=1, reverse; MY=0, normal
Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
SRESET	0	0	1	1	1	0	0	0	0	1	Software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
Set Frame Rate 1	0	0	0	0	1	1	0	0	0	0	Frame Freq. in Temp range A and B
	0	0	FB[3:0]				FA[3:0]				
Set Frame Rate 2	0	0	0	0	1	1	0	0	0	1	Frame Freq. in Temp range C and D
	0	0	FD[3:0]				FC[3:0]				
Set N-Line	0	0	0	1	0	0	1	1	-	-	Set N-Line inversion counter
			-	-	N5	N4	N3	N2	N1	N0	
LED[1:3] ON/OFF	0	0	0	0	1	1	1	L1	L2	L3	LED[1:3] control
Test	0	0	1	1	1	1	1	T1	T0	TE	TE=0, exit test mode; TE=1, enter test mode. T[1:0]: test mode.

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
TC Sensor Speed	0	0	1	1	1	1	1	1	0	1	Speed up TC function FTC=0: normal mode FTC=1: fast mode
	0	0	0	1	1	1	0	0	0	0	
	0	0	0	0	1	0	FTC	0	0	1	
	0	0	1	1	1	1	1	0	0	0	
Drive Mode Selection	0	0	1	1	1	1	1	1	0	1	Sets LCD drive mode DMP=0: dummy period ON DMP=1: dummy period OFF MLM=0: dispersion mode MLM=1: non- dispersion mode
	0	0	0	1	1	1	0	0	0	1	
	0	0	0	1	1	DMP	1	0	0	1	
	0	0	0	1	1	1	0	1	1	1	
	0	0	0	DSP	1	0	0	0	1	0	
	0	0	1	1	1	1	1	0	0	0	

Extended Instruction 1 (TE=1 & T[1:0]=0,0)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
TC Control	0	0	0	1	1	0	1	0	0	TC	Set temperature compensation function, TC=1: ON/TC=0: OFF
Set TC Curve 01	0	0	0	0	1	1	0	0	0	0	Set gradient of TC curves T0: -40 ~ -32℃; T1: -32 ~ -24℃
			MT1[3:0]				MT0[3:0]				
Set TC Curve 23	0	0	0	0	1	1	0	0	0	1	Set gradient of TC curves T2: -24 ~ -16℃; T3: -16 ~ - 8℃
			MT3[3:0]				MT2[3:0]				
Set TC Curve 45	0	0	0	0	1	1	0	0	1	0	Set gradient of TC curves T4: -8 ~ 0℃; T5: 0 ~ 8℃
			MT5[3:0]				MT4[3:0]				
Set TC Curve 67	0	0	0	0	1	1	0	0	1	1	Set gradient of TC curves T6: 8 ~ 16℃; T7: 16 ~ 24℃
			MT7[3:0]				MT6[3:0]				
Set TC Curve 89	0	0	0	0	1	1	0	1	0	0	Set gradient of TC curves T8: 24 ~ 32℃; T9: 32 ~ 40℃
			MT9[3:0]				MT8[3:0]				
Set TC Curve AB	0	0	0	0	1	1	0	1	0	1	Set gradient of TC curves TA: 40 ~ 48℃; TB: 48 ~ 56℃
			MTB[3:0]				MTA[3:0]				
Set TC Curve CD	0	0	0	0	1	1	0	1	1	0	Set gradient of TC curves TC: 56 ~ 64℃; TD: 64 ~ 72℃
			MTD[3:0]				MTC[3:0]				
Set TC Curve EF	0	0	0	0	1	1	0	1	1	1	Set gradient of TC curves TE: 72 ~ 80℃; TF: 80 ~ 88℃
			MTF[3:0]				MTE[3:0]				
Set TC Flag	0	0	0	0	1	1	1	1	1	0	Set +/- flag of MT[7:0] 0: positive flag, 1: negative flag
			FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
			0	0	1	1	1	1	1	1	Set +/- flag of MT[F:8] 0: positive flag, 1: negative flag
			FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
TMPARNG	0	0	1	0	1	0	0	0	0	0	Temp range A
	0	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
TMPBRNG	0	0	1	0	1	0	0	0	0	1	Temp range B
	0	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
TMPCRNG	0	0	1	0	1	0	0	0	1	0	Temp range C
	0	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
Set fFR TC Hysteresis	0	0	1	1	0	0	1	1	0	0	THF[3:0]: TC hysteresis for frequency
			0	0	0	0	THF3	THF2	THF1	THF0	
Set Vop TC Hysteresis	0	0	1	1	0	0	1	1	1	0	THV[5:0]: TC hysteresis for Vop
			0	0	THV5	THV4	THV3	THV2	THV1	THV0	

Extended Instruction 2 (TE=1 & T[1:0]=0,1)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
EPCTIN	0	0	1	0	0	1	0	0	0	1	Control PROM WR/RD EWR=1: PROM write mode EWR=0: PROM read mode
	0	0	0	0	EWR	0	0	0	0	0	
EPCTOUT	0	0	1	0	0	1	0	0	1	0	Exit PROM control mode
EPMWR	0	0	1	0	0	1	0	0	1	1	Write to PROM
EPMRD	0	0	1	0	0	1	0	1	0	0	Read from PROM
AutoLoadSet	0	0	1	0	0	1	0	1	1	0	PROM data auto re-load control
	0	0	0	0	0	ARD	0	0	0	0	
Vop Up	0	0	1	1	0	1	1	1	1	0	Increase Vop by 1 step
Vop Down	0	0	1	1	0	1	1	1	1	1	Decrease Vop by 1 step

Note:
1. Symbol “-” means this bit can be “H” or “L”.
2. Please don’t use instructions which are not defined in this specification.

9. INSTRUCTION DESCRIPTION

Basic Instruction (TE=0, T[1:0]=Don't Care)

Read Data

8-bit data of the Display Data RAM specified by the column address and page address can be read to the microprocessor by this instruction. The column address will be increased by 1 automatically after each byte of data read (till the end of a page). With this feature, the MPU can continuously read data from the addressed page. A dummy read is required after specifying the page and column address. The read function is not available in serial interface mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Data Read							

Write Data

8-bit display data from the microprocessor can be written into the Display Data RAM at the location specified by the column and page address. The column address will be increased by 1 automatically after each byte of data write (till the end of a page). With this feature, the MPU can continuously write data to the addressed page.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Data Write							

Read Status

Read the internal status of ST7591. The read function is not available in serial interface mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BSY	MX	D	RST	0	0	0	0

Flag	Description
BSY	BSY=0: Ready (ST7591 always returns 0 after hardware reset is finished) BSY=1: Busy
MX	MX=0: Normal direction (SEG0->SEG159) MX=1: Reverse direction (SEG159->SEG0)
D	D=0: Display ON D=1: Display OFF
RST	RST=1: During reset (hardware or software reset) RST=0: Normal operation
VN, VB, VF & Disv	Power Status

Set Page Address

This is double-byte instruction. Y [4:0] specifies the page address of the built-in DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	1	0	0
0	0	-	-	-	Y4	Y3	Y2	Y1	Y0

Y4	Y3	Y2	Y1	Y0	Page Address	Valid Bit
0	0	0	0	0	Page0	D0 ~ D7
0	0	0	0	1	Page1	D0 ~ D7
0	0	0	1	0	Page2	D0 ~ D7
:	:	:	:	:	:	:
0	1	1	1	0	Page14	D0 ~ D7
0	1	1	1	1	Page15	D0 ~ D7
1	0	0	0	0	Page16	D0 ~ D3

Set X Address

The range of column address is 0…159. The address parameter is separated into 2 instructions. The column address will be increased by 1 after each byte of display data access (read/write). This auto-increment feature stops at the end of each page (Column Address “9Fh”). This feature allows MPU accessing DDRAM content continuously in the addressed page.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4
0	0	0	0	0	0	X3	X2	X1	X0

X7	X6	X5	X4	X3	X2	X1	X0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1	157
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

Power Control

This instruction controls the built-in power circuits. Typically, these flags are turned ON at the same time.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	VN	VB	VR	VF

Flag	Description
VN	VN=0: NVDD Generator OFF VN=1: NVDD Generator ON
VB	VB=0: V3 Generator OFF VB=1: V3 Generator ON
VR	VR=0: MV3 Generator OFF VR=1: MV3 Generator ON
VF	VF=0: V1 Generator OFF VF=1: V1 Generator ON

* Please refer to the “Power System” section for the power application notes.

Oscillator ON/OFF

This instruction controls the built-in oscillator circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	0	1	OSC

Flag	Description
OSC	OSC=0: Set built-in oscillator OFF OSC=1: Set built-in oscillator ON

Set Start Line

This is double-byte instruction. This instruction sets the line address of DDRAM which determines the first scan line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	0	0	0
0	0	S7	S6	S5	S4	S3	S2	S1	S0

S7	S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131
1	0	0	0	0	1	0	0	Invalid Address No Operation
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

Set COM0

This is double-byte instruction. This instruction selects the COM pad to output the COM0 signal. This instruction moves the display area (display window) without updating DDRAM data. The instruction must execute under Display OFF condition.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	0	1	1
0	0	C7	C6	C5	C4	C3	C2	C1	C0

C7	C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	0	1	COM1
0	0	0	0	0	0	1	0	COM2
0	0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	COM129
1	0	0	0	0	0	1	0	COM130
1	0	0	0	0	0	1	1	COM131
1	0	0	0	0	1	0	0	Invalid Address No Operation
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

Set Display Line

This is double-byte instruction. This instruction selects the display line.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	1	0	0
0	0	P7	P6	P5	P4	P3	P2	P1	P0

P7	P6	P5	P4	P3	P2	P1	P0	Display Line	Display Duty
0	0	0	0	0	0	0	0	132 (default)	1/176
0	0	0	0	1	0	0	1	9	1/12
0	0	0	0	1	0	1	0	10	1/16
0	0	0	0	1	0	1	1	11	1/16
:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130	1/176
1	0	0	0	0	0	1	1	131	1/176
Settings not listed above								No Operation	

Note:

1. The display area changes in different Display Line. Please refer to the output map in “COM Direction” Section.
2. For the LCM which is not full Display Line, the display area for MY=1 is not the same as MY=0. Please refer to the output map and set correct COM0.

Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	Bias
0	0	0	1/3
0	0	1	
0	1	0	1/4
0	1	1	1/5
1	0	0	1/6
1	0	1	1/7
1	1	0	Reserved
1	1	1	

Symbol	Bias Setting				
	1/3	1/4	1/5	1/6	1/7
V3	V3	V3	V3	V3	V3
V1	V3/3	V3/4	V3/5	V3/6	V3/7
VC	0	0	0	0	0
MV1	-V3/3	-V3/4	-V3/5	-V3/6	-V3/7
MV3	-V3	-V3	-V3	-V3	-V3

Note:

- V1 range: 1.0V ≤ V1 < 2.3V.
- Optimized Bias: $2 / [(M * 4/3)^{1/2}]$ ……. M=Display Lines

Set Booster

This instruction controls the built-in booster circuit to provide the power source of the built-in regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1	BL1	BL0

Flag	Description		
BL[1:0]	BL1	BL0	Booster Level
	0	0	Booster Level = (2xVDD2) x 2
	0	1	Booster Level = (2xVDD2) x 3
	1	0	Booster Level = (2xVDD2) x 4
	1	1	Reserved

Set Vop

This is double-byte instruction. This instruction controls the Vop output voltage which is generated by the built-in Vop generator. Customers select the default Vop voltage and set the contrast by this instruction, while the voltage adjustment to match LCD characteristics is achieved by PROM feature.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	V7	V6	V5	V4	V3	V2	V1	V0

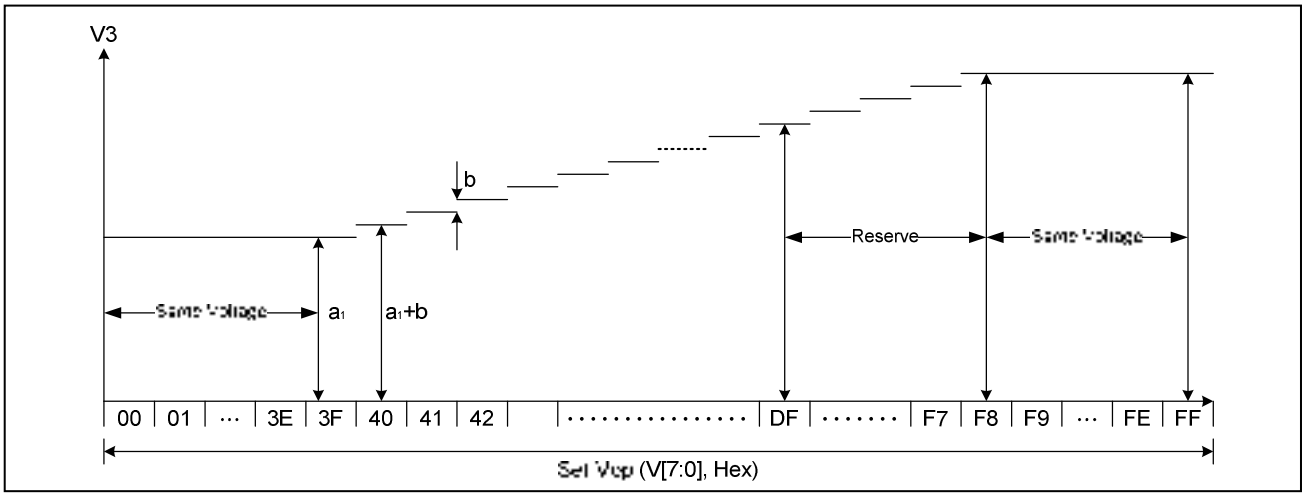
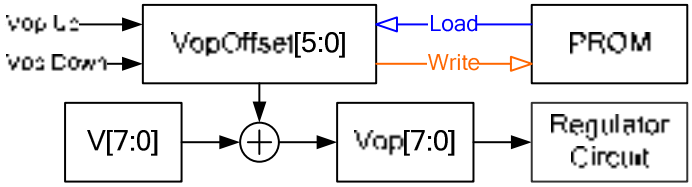


Fig. 9. Setting V3 Voltage

ST7591 has PROM for adjustment Vop. The relation can be illustrated as shown below:



The operation voltage (Vop) calculation formula is shown below:

Vop = V3 = a1 + b x (V[7:0] + VopOffset[5:0] – 64) .....(where the valid V[7:0] is 40h~DFh)

Symbol	Value	Unit
a1	2.64	V
b	0.04	V

Note:

1. The maximum voltage that can be generated is dependent on VDD2 voltage and the loading of LCD module. The first 64 values (00h~3Fh) generate the same voltage, the 25 values (DFh~F7h) are reserved for test, and the last 8 values (F8h~FFh) generate the same voltage.
2. It is not recommended to set Vop over 9V. Besides, it is recommended to reserve some range for Vop adjustment or temperature compensation. Therefore, for example, if we reserved 0.2V for customer to adjust contrast, 0.3V for TC function and 0.08V to fine tune Vop voltage… Then, the V[7:0] value should be less than “D2h” :
   [9V – 0.2V – 0.3V – 0.08] / 0.04V = (D2h).
3. Please note that: VopOffset[5:0] is ***2’s complement***, so that VopOffset[5:0] can increase or decrease Vop. If customer adjusts Vop by too many “Vop Up” (or “Vop Down”) instructions, the purpose to increase Vop (or decrease Vop) will become: “lower Vop” (or “higher Vop”). ***A software overflow prevention procedure*** should be used when using “Vop Up”/“Vop Down”. So that the overflow problem can be prevented.
4. If VDD is higher than 3.8V, the lowest Vop will higher than 2.64V.

SEG Direction

This instruction changes the DDRAM addressing mode which let the data write to DDRAM in the opposite direction. After changing the MX setting and re-writing the display data into DDRAM again, the display will be mirrored horizontally.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: Normal direction (SEG0->SEG159) MX=1: Reverse direction (SEG159->SEG0)

Note: It is necessary to write the display data again after the MX setting is altered.

All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP=0: Normal display AP=1: All pixels ON

Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (White -> Black, Black -> White) while the display data in DDRAM is never changed.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV=1: Inverse display

Display ON/OFF

This instruction turns the display ON/OFF.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	D

Flag	Description
D	D=1: Display ON. D=0: Display OFF. All SEGs/COMs output with VC.

Set Power Save

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	0	0	PD

Flag	Description
PD	Set Power-Save mode: PD=0: Normal mode PD=1: Standby mode

The Power Save mode starts the following procedure:

1. Stops the LCD driving circuits and keeps the common and segment outputs at VC;
2. Stops internal oscillation circuit;
3. PD=1: Stops internal oscillation circuit;
   PD=0: Internal oscillation circuit is still ON;
4. The display data and register settings are still kept except D-Flag and AP-Flag.

Discharge ON/OFF

This command is used to discharge the capacitors connected to the power supply circuits. This command is necessary when turning OFF the system power supply (VDD-VSS).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	1	Disv

Flag	Description
Disv	Disv=0: Disable Discharge Disv=1: Enable Discharge

Note:

1. In case of huge leakage current, do NOT discharge before related power is OFF.
2. In case of huge leakage current, do NOT discharge if external power is not OFF.

COM Direction

This instruction controls the common output sequence and the display direction changes vertically. Please refer to Fig. 7.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	0	0	0

Flag	Description
MY	MY=0: Normal direction (COM0->COM131) MY=1: Reverse direction (COM131->COM0)

COM output mode can be changed by hardware ITR pin and software MY flag. ITR pin controls the interlace mode ON/OFF and MY flag control the scan direction. The combination result is listed below:

ITR Pin	MY Flag	COM Output Function
0	0	Setting 1: Normal scan, in Normal direction
0	1	Setting 2: Normal scan, in Reverse direction
1	0	Setting 3: Interlace scan, in Normal direction
1	1	Setting 4: Interlace scan, in Reverse direction

The complete output mapping is shown below:

ITR	MY	Item	Description	1			2			3			4		
0	0	Setting 1	Normal	0	1	2	3	4	5	6	7	8	9	10	11
0	1	Setting 2	Normal Inverse	131	130	129	128	127	126	125	124	123	122	121	120
1	0	Setting 3	Interlace	0	1	2	66	67	68	3	4	5	69	70	71
1	1	Setting 4	Interlace Inverse	131	130	129	65	64	63	128	127	126	62	61	60

5			6			7			8			9			10			11			12		
12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
6	7	8	72	73	74	9	10	11	75	76	77	12	13	14	78	79	80	15	16	17	81	82	83
125	124	123	59	58	57	122	121	120	56	55	54	119	118	117	53	52	51	116	115	114	50	49	48

13			14			15			16			17			18			19			20		
36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72
18	19	20	84	85	86	21	22	23	87	88	89	24	25	26	90	91	92	27	28	29	93	94	95
113	112	111	47	46	45	110	109	108	44	43	42	107	106	105	41	40	39	104	103	102	38	37	36

21			22			23			24			25			26			27			28		
60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83
71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
30	31	32	96	97	98	33	34	35	99	100	101	36	37	38	102	103	104	39	40	41	105	106	107
101	100	99	35	34	33	98	97	96	32	31	30	95	94	93	29	28	27	92	91	90	26	25	24

29			30			31			32			33			34			35			36		
84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
42	43	44	108	109	110	45	46	47	111	112	113	48	49	50	114	115	116	51	52	53	117	118	119
89	88	87	23	22	21	86	85	84	20	19	18	83	82	81	17	16	15	80	79	78	14	13	12

37			38			39			40			41			42			43			44		
108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
54	55	56	120	121	122	57	58	59	123	124	125	60	61	62	126	127	128	63	64	65	129	130	131
77	76	75	11	10	9	74	73	72	8	7	6	71	70	69	5	4	3	68	67	66	2	1	0

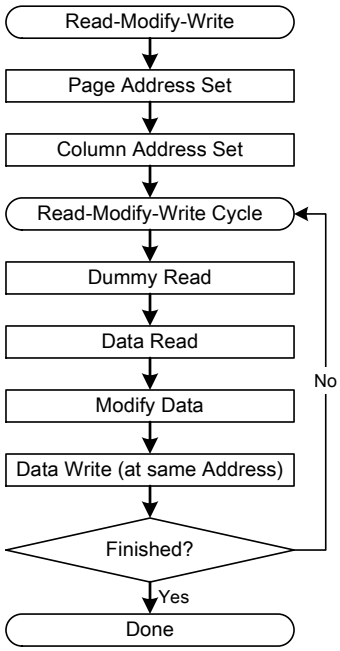
After a valid hardware reset, the COM output state is reset to normal.

Read-modify-Write

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

* Other instructions aside from data read/write can also be used in this mode.



RESET

This instruction resets some registers to their default (refer to the “Section 7. RESET CIRCUIT” for detailed information). Please note this instruction (software reset) is not same as the hardware reset (RSTB=L). For example, the built-in power circuit is initialized by the hardware reset (RSTB=L) but cannot be initialized by this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	1

NOP

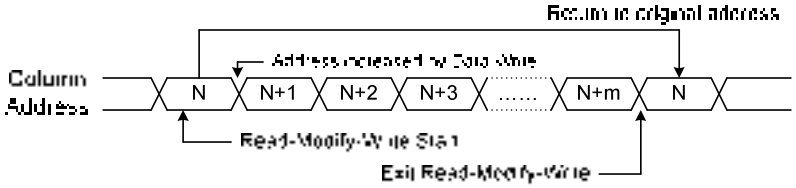
“No Operation” instruction. ST7591 will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

END

It exits Read-modify-Write. The column address returns to the address it was before entering Read-modify-Write mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0



Set Frame Rate 1 & 2

These two instructions set the dividing ratio of the built-in oscillation frequency (fOSC) and the internal operation clock (fCL) in each operation temperature range. This feature is enabled only when the built-in oscillation circuit is turned ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	0
0	0	FB[3:0]				FA[3:0]			

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1
0	0	FD[3:0]				FC[3:0]			

Parameter	Description
FA[3:0]	Set frame frequency in temperature range -40℃ to TA.
FB[3:0]	Set frame frequency in temperature range TA to TB.
FC[3:0]	Set frame frequency in temperature range TB to TC.
FD[3:0]	Set frame frequency in temperature range TC to 88℃.

Note:

1. TA, TB & TC are defined by Extended Instructions: TMPARNG, TMPBRNG & TMPCRNG.
2. By setting all temperature ranges with the same parameter, the temperature compensation for frequency is disabled.

[Definition of Symbols]

Symbol	Description
fOSC	Oscillation frequency of the built-in oscillation circuit.
fCL	Internal operation clock. It is the basic clock used by the synchronous circuit of IC. This clock is obtained by dividing fOSC.
fOCL	It is the external clock provided from CL pin externally when the built-in oscillation circuit is turned OFF. In this case, internal oscillation clock (fOSC) is the same as external operation clock (fOCL). Please set external clock close to 1630KHz.
fDCLK	Display operation clock. It is used to specify a single duration in the sequential drive of liquid crystal. It constantly meets the relation of fCL/15 independent of the value of the operation clock frequency select command. The relationship will not change even when the external clock is used.

When the built-in oscillation circuit is turned OFF, the external clock applied on CL pin (fOCL) is used as the internal oscillation clock (fOSC). In this case, the fOCL uses the same dividing ratio as the internal oscillation clock. The accuracy and the temperature effect should be considered by customer. Please note the Master/Slave function cannot support external clock input to Master.

The following table shows fCL (internal operation clock) and fDCLK (display operation clock) set by different parameters. It also shows the frame frequency (fFR) in different display lines.

FA3 FA2 FA1 FA0 FB3 FB2 FB1 FB0 FC3 FC2 FC1 FC0 FD3 FD2 FD1 FD0	fCL [kHz]	fDCLK [kHz]	Frame Frequency vs. Display Lines fFR [Hz]			
			132 lines	128 lines	112 lines	96 lines
0 0 0 0	408	27.2	151	154	174	206
0 0 0 1	326	21.7	121	123	139	165
0 0 1 0	272	18.1	101	103	116	137
0 0 1 1	233	15.5	86	88	100	118
0 1 0 0	204	13.6	75	77	87	103
0 1 0 1	181	12.1	67	69	77	91
0 1 1 0	163	10.9	60	62	70	82
0 1 1 1	136	9.1	50	51	58	69
1 0 0 0	116	7.8	43	44	50	59
1 0 0 1	109	7.2	40	41	46	55
1 0 1 0	102	6.8	38	39	44	51
1 0 1 1	91	6.0	34	34	39	46
1 1 0 0	82	5.4	30	31	35	41
1 1 0 1	78	5.2	29	29	33	39
1 1 1 0	68	4.5	25	26	29	34
1 1 1 1	65	4.3	24	25	28	33

Set N-Line

This is double-byte instruction. This instruction selects the inverted line number which alters the driving signal phase to improve the display quality.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	-	-
0	0	-	-	N5	N4	N3	N2	N1	N0

Flag	Description
N[5:0]	This command is used to set the inverted line number to improve display quality. If N[5:0]=0, N-line inversion function is disable. Line inversion number = (N[5:0] +1) * 3, if N[5:0]=7, inversion occurs per 24 line (except N=0).

LED[1:3] ON/OFF

The command can control LED[1:3] ON/OFF.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	L3	L2	L1

Flag	Description
L[3:1]	Value: 0 — LED Control: LED OFF Value: 1 — LED Control: LED ON

Test

The test mode is reserved for IC testing and IC calibration. The temperature compensation related instructions are in Test Mode 0. Always remember to exit test mode by setting TE=0. If the test mode is enabled accidentally, it can be cleared by: issuing an “L” pulse on RSTB pin, issuing RESET instruction or issuing NOP instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	T1	T0	TE

Flag	Description
T[1:0] TE	<table><tr><th>T1</th><th>T0</th><th>TE</th><th>Description</th></tr><tr><td>-</td><td>-</td><td>0</td><td>Normal operation (when TE=0, T[1:0] are ignored)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Extended Instruction 1 (Thermal)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Extended Instruction 2 (PROM)</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Reserved for IC testing only.</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Do NOT use!!</td></tr></table>

TC Sensor Speed

This instruction set the TC (Temperature Compensation) related circuits into Fast Mode. When the fast mode is enabled (FTC=1), the thermal detection frequency is increased and the display response time is decreased. It is only used in initialization procedure, so that the LCD can be turned ON under extremely temperature. It should be turned OFF before the display is turned ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	0	0	0	0
0	0	0	0	1	0	FTC	0	0	1
0	0	1	1	1	1	1	0	0	0

Flag	Description
FTC	FTC=0: Normal mode FTC=1: Fast mode

Drive Mode Selection

This instruction sets the LCD drive mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	0	0	0	1
0	0	0	1	1	DMP	1	0	0	1
0	0	0	1	1	1	0	1	1	1
0	0	0	DSP	1	0	0	0	1	0
0	0	1	1	1	1	1	0	0	0

Flag	Description
DMP	DMP=“1”: dummy period OFF (default) DMP=“0”: dummy period ON (recommend)
DSP	DSP=“1”: non-dispersion drive mode. DSP=“0”: dispersion drive mode.

Extended Instruction 1 (TE=1, T[1:0]=0,0)

TC Control

This instruction controls the temperature compensation function ON/OFF.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	1	0	0	TC

Flag	Description
TC	TC=0: Set Temperature Compensation OFF TC=1: Set Temperature Compensation ON

Set TC Curve

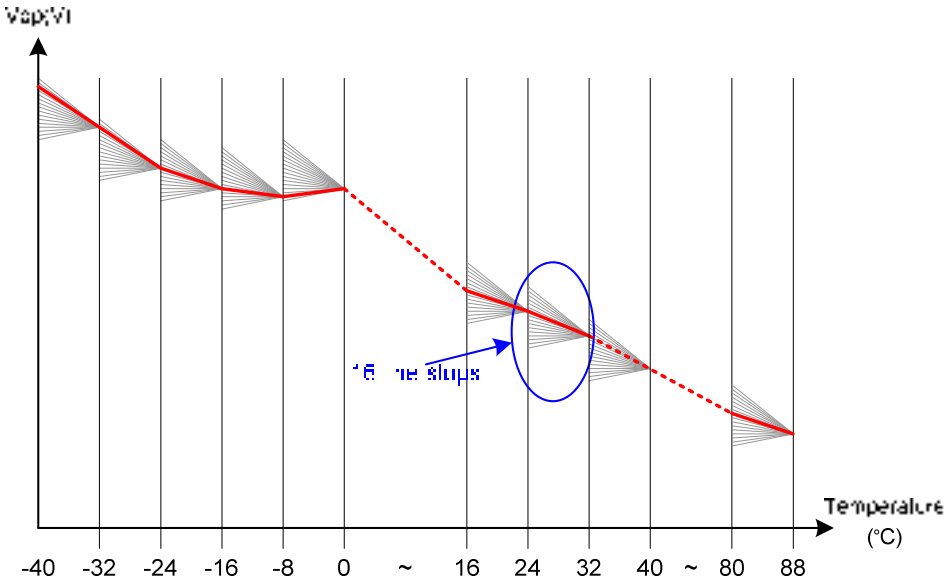
These instructions set the TC curve for Vop in each temperature range.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Temperature
0	0	0	0	1	1	0	0	0	0	-40 ~ -32℃
0	0	MT1[3:0]				MT0[3:0]				-32 ~ -24℃
0	0	0	0	1	1	0	0	0	1	-24 ~ -16℃
0	0	MT3[3:0]				MT2[3:0]				-16 ~ - 8℃
0	0	0	0	1	1	0	0	1	0	-8 ~ 0℃
0	0	MT5[3:0]				MT4[3:0]				0 ~ 8℃
0	0	0	0	1	1	0	0	1	1	8 ~ 16℃
0	0	MT7[3:0]				MT6[3:0]				16 ~ 24℃
0	0	0	0	1	1	0	1	0	0	24 ~ 32℃
0	0	MT9[3:0]				MT8[3:0]				32 ~ 40℃
0	0	0	0	1	1	0	1	0	1	40 ~ 48℃
0	0	MTB[3:0]				MTA[3:0]				48 ~ 56℃
0	0	0	0	1	1	0	1	1	0	56 ~ 64℃
0	0	MTD[3:0]				MTC[3:0]				64 ~ 72℃
0	0	0	0	1	1	0	1	1	1	72 ~ 80℃
0	0	MTF[3:0]				MTE[3:0]				80 ~ 88℃

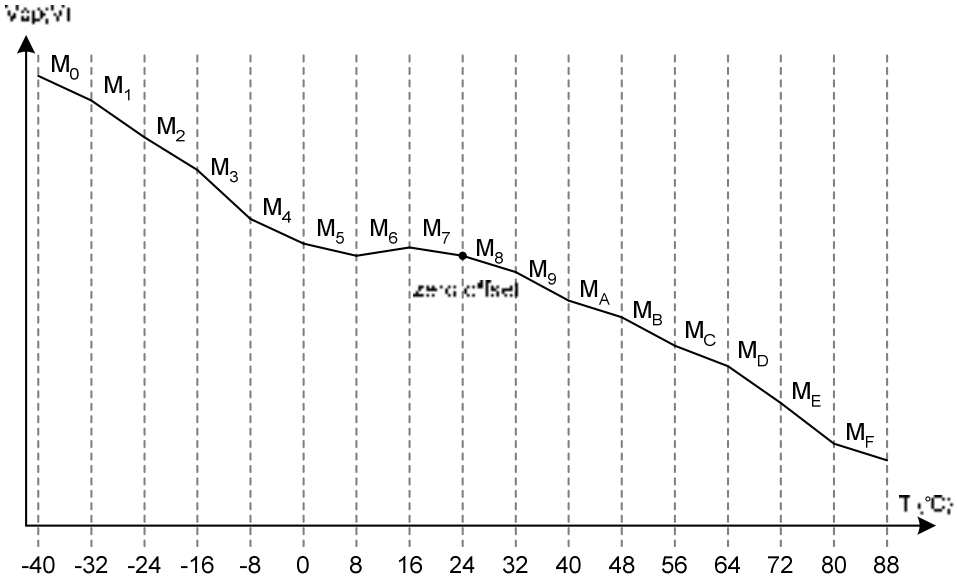
Flag	Description
MTn[3:0]	These commands define temperature gradient compensation coefficient.

TC Flag	MTn Value (Decimal)	MTn[3:0]				Slope of TC Curve (mV/℃)
		Bit-3	Bit-2	Bit-1	Bit-0	
0	0	0	0	0	0	0
	1	0	0	0	1	-5
	2	0	0	1	0	-10
	3	0	0	1	1	-15
	:	:	:	:	:	:
	14	1	1	1	0	-70
	15	1	1	1	1	-75
1	0	--	--	0	0	0
	1	--	--	0	1	5
	2	--	--	1	0	10
	3	--	--	1	1	15

* Gradient tolerance: +/- 3mV/℃.



For example, the TC curve can be programmed as shown below:



Set TC Flag

Set flag of TC curves.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1	1	0
0	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0
0	0	0	0	1	1	1	1	1	1
0	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8

Flag	Description
FMT[F:0]	<table><tr><th>FMTn</th><th>Description</th></tr><tr><td>0</td><td>Negative flag</td></tr><tr><td>1</td><td>Positive flag</td></tr></table>

TMPARNG

Temperature range A value set for Frame Freq. Adj.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	0
0	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0

Flag	Description
TA[6:0]	Temperature range set for automatic frame freq. adj. operation according the current temperature value. **TA Temperature(℃) + 40 = TA [6:0]** Example: If TA wants to be set at 24℃, TA[6:0]=24+40=64(40h)

TMPBRNG

Temperature range B value set for Frame Freq. Adj.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	1
0	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Flag	Description
TB[6:0]	Temperature range set for automatic frame freq. adj. operation according the current temperature value. **TB Temperature(℃) + 40 = TB [6:0]** Example: If TB wants to be set at 24℃, TB[6:0]=24+40=64(40h)

TMPCRNG

Temperature range C value set for Frame Freq. Adj.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	0
0	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0

Flag	Description
TC[6:0]	Temperature range set for automatic frame freq. adj. operation according the current temperature value. **TC Temperature(℃) + 40 = TC [6:0]** Example: If TC wants to be set at 24℃, TC[6:0]=24+40=64(40h)

ST7591 will auto-switch frame rate on different temperature such as Fig. 10. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPARNG, TMPBRNG and TMPCRNG. The frame rate FA, FB, FC and FD are defined by customer with command Set Frame Rate.

When the temperature is decreasing, the frame rate changes at the temperature specified by TA/TB/TC. When the temperature is increasing, the frame rate changes at the higher temperature: TA/TB/TC+TH (℃). The “TH” is specified by the “Set FR TC Hysteresis” command.

For example: TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please refer to Fig. 10.

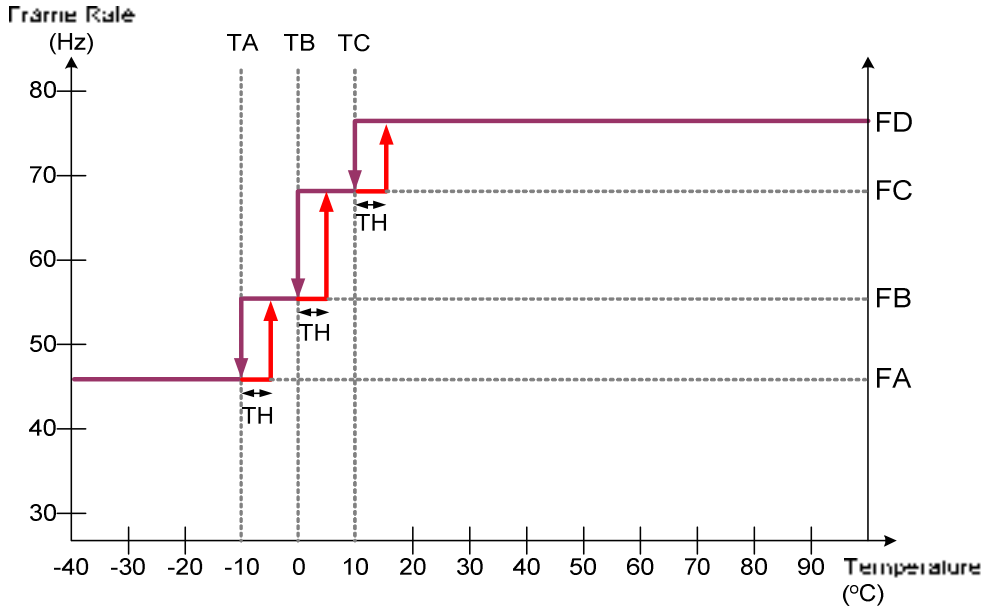


Fig. 10. Frame Rate vs. Temperature

Set FR TC Hysteresis

When the temperature changes around at the junction between 2 different frame rate slopes, this instruction controls the hysteresis. The TC circuit will use the parameter of the next slope only when the temperature difference is larger than the hysteresis.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	1	1	0	0
0	0	0	0	0	0	THF3	THF2	THF1	THF0

Set Vop TC Hysteresis

When the temperature changes around at the junction between 2 different Vop slopes, this instruction controls the hysteresis. The TC circuit will use the parameter of the next slope only when the temperature difference is larger than the hysteresis.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	1	1	1	0
0	0	0	0	THV5	THV4	THV3	THV2	THV1	THV0

Extended Instruction 2 (TE=1, T[1:0]=0,1)

EPCTIN

This instruction loads the registers' default value from PROM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	0	1
0	0	0	0	EWR	0	0	0	0	0

Flag	Description
EWR	EWR="1": The Write Enable of PROM will be opened. EWR="0": The Read Enable of PROM will be opened.

EPCTOUT

IC exits the PROM control circuit when executing this command.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	1	0

EPMWR

IC actives trigger to start PROM programming when executing this command.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	1	1

EPMRD

IC actives trigger to start PROM programming when executing this command.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0

AutoLoadSet

Mask PROM data auto re-load control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	1	0
0	0	0	0	0	ARD	0	0	0	0

Flag	Description
ARD	PROM auto-recovery control ARD=1: Disable PROM auto recovery ARD=0: Enable PROM auto recovery

Vop Up

This instruction increases the VopOffset by 1.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	1	1	0

Vop Down

This instruction decreases the VopOffset by 1.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	1	1	1

10. OPERATION FLOW

(1) Initial Flow (with built-in Power Circuits)

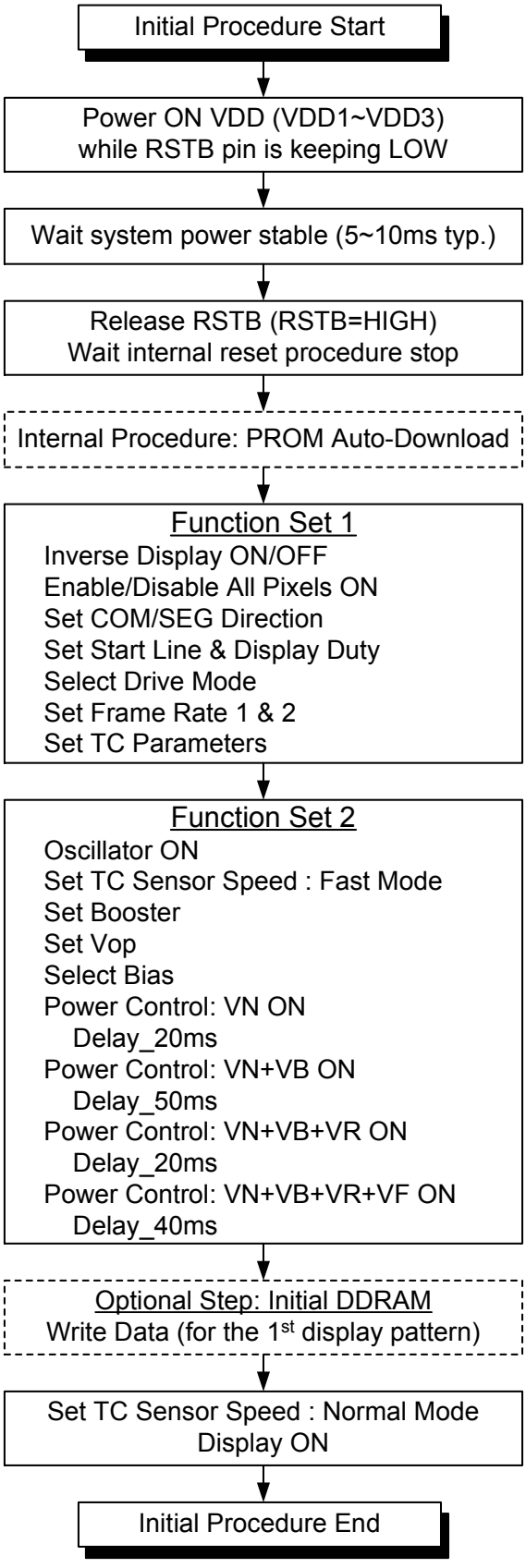


Fig. 11. Initial Flow (with built-in Power Circuits)

Power ON and Initial Flow Notes:

1. To prevent power ON noise, please hold RSTB LOW until the system power is stable (generally, 5~10 ms).
2. After releasing RSTB signal (RSTB=HIGH), do NOT issue instruction immediately. An internal reset time (tR) should be maintained for finishing internal reset procedure.
3. After internal reset procedure is finished, internal PROM Auto-Download procedure starts. This procedure takes around 120ms.
   This Initial Flow doesn't use PROM related instruction. Please refer to PROM operation flow if PROM related operation is required.
4. The delay time for Power Control flow depends on LCD module. The delay time should be increased if the ITO resistance or capacitor value increases.
5. The build-in DDRAM content is undetermined after power ON. The content cannot be reset by hardware or software reset. It is recommended to add a DDRAM initial flow to prevent showing unexpected display pattern after turning ON the display.

(2) Release Standby Flow (built-in Power Circuits)

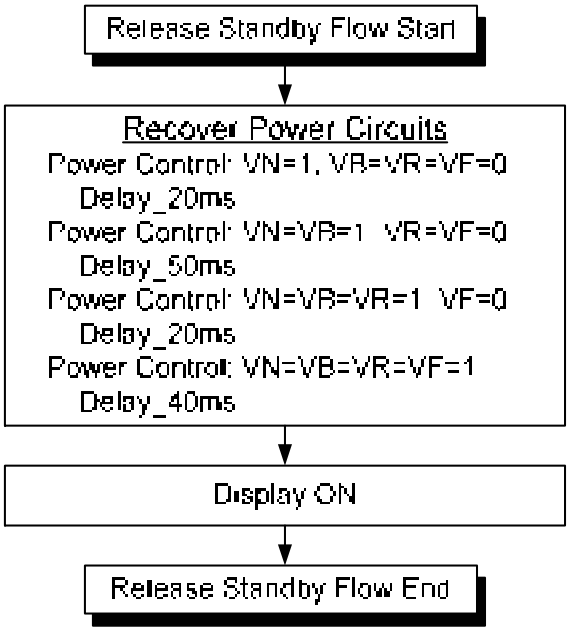


Fig. 12. Release standby mode Flow

Release Standby Flow Notes:

1. The delay time for Power Control flow depends on LCD module. The delay time should be increased if the ITO resistance or capacitor value increases.
2. For external power applications, be sure all the LCD driver powers are ready before display ON.

(3) Enter Standby Flow (built-in Power Circuits)

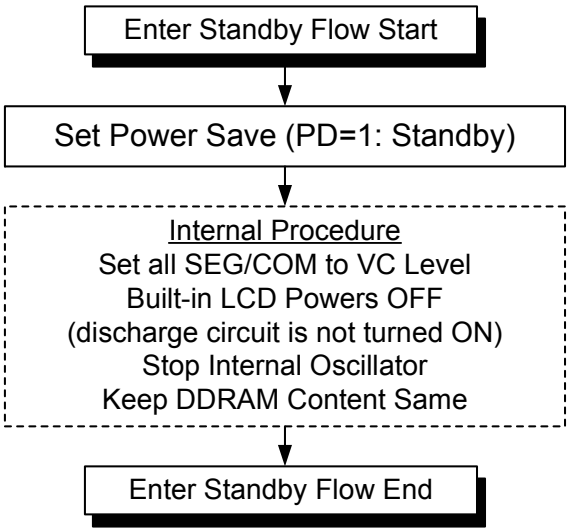


Fig. 13. Enter standby mode Flow

Enter Standby Flow Notes:

1. This flow doesn't include "Discharge". Before all analog related powers (V3~V1, MV1~MV3) being discharged, there will have small leakage current.
2. If customer wants to add Discharge instruction into this flow, be sure all external power(s) (if used) must be turned OFF before discharging.

(4) Power OFF Flow

Please execute the Power OFF flow before turning VDDI/VDDA OFF. Otherwise, unexpected abnormal display maybe occurred on the LCD module.

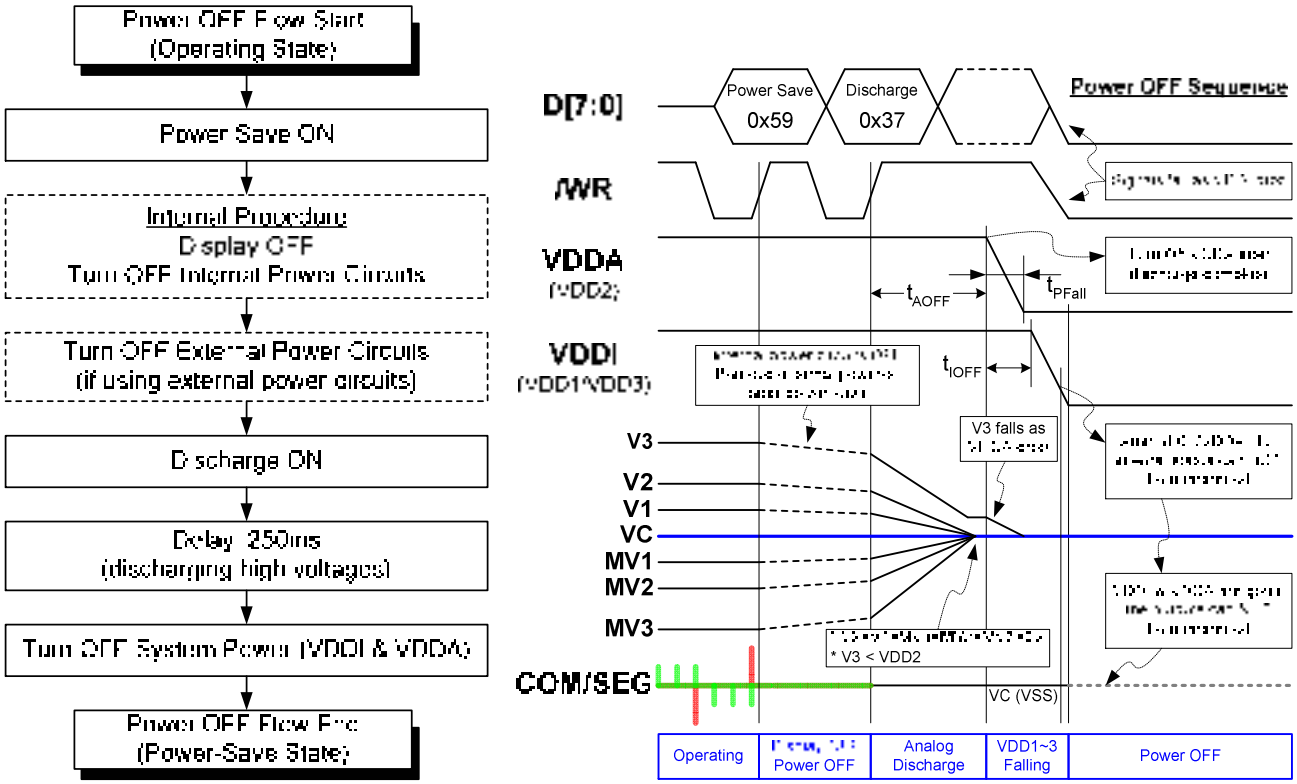


Fig. 14. Power OFF Flow and Power OFF Sequence

Timing Requirement:

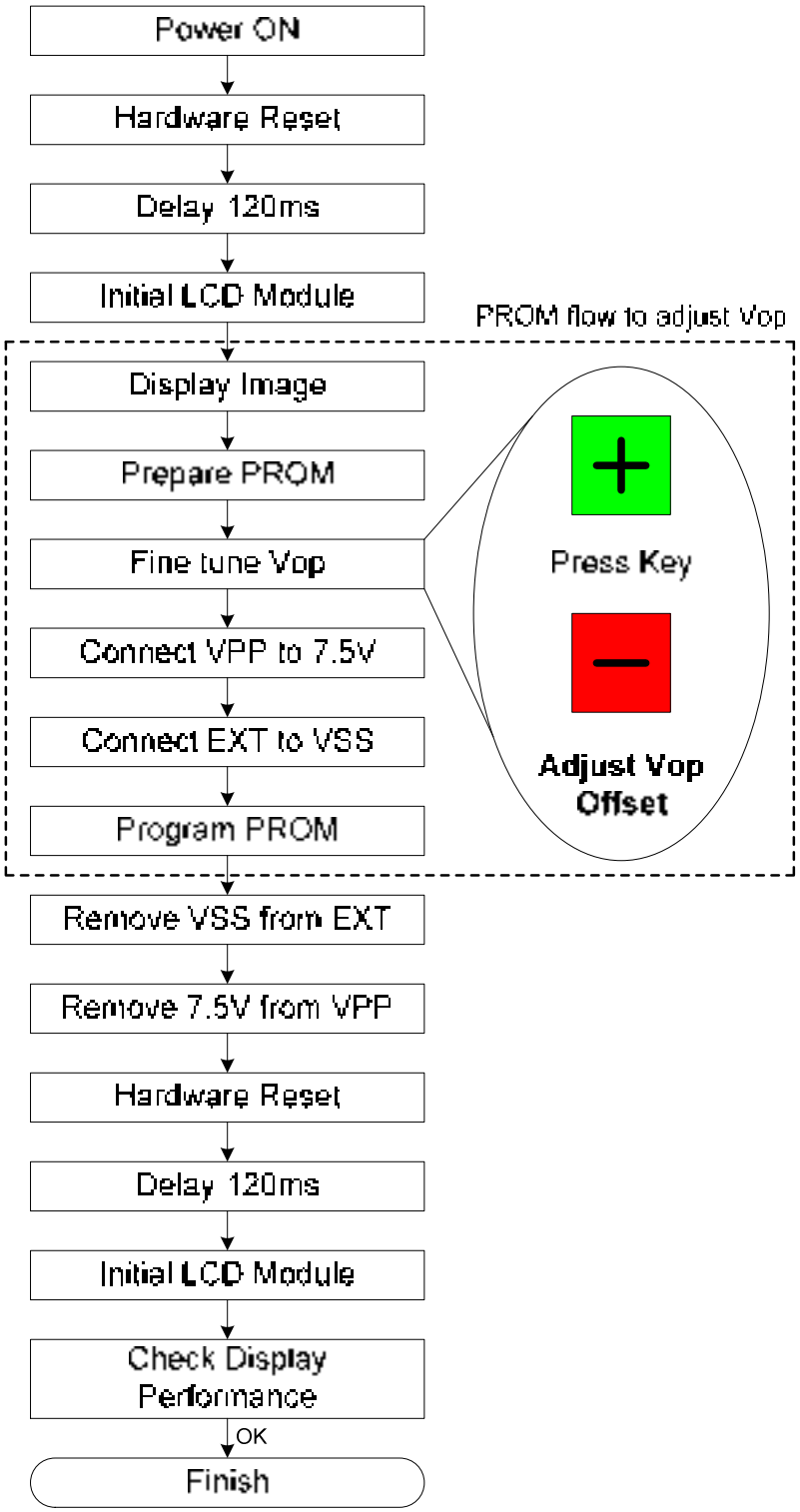
Item	Symbol	Requirement	Note
VDDA OFF delay	t_{AOFF}	250ms ≤ t_{AOFF}	● Turn VDDA OFF after discharge-procedure is finished.
VDDA Falling Time	t_{PFall}	Recommend t_{PFall} ≤ 10sec	● t_{PFall} depends on the LCD module and power circuit on the application system. ● It is recommended to keep t_{PFall} less than 10 seconds.
VDDI OFF delay	t_{IOFF}	0 ≤ t_{IOFF}	● If VDDI and VDDA are separated, turn VDDI OFF after VDDA, is lower than 0.2V.

Note:

- Be sure to turn external power circuits OFF and discharge them before the system power (VDDI/VDDA) is gone.
- For external power application, please issue discharge instruction after turning external power circuit OFF.

(5) MTP Program Flow

The reference PROM programming flow to adjust Vop is shown below:



Reference Code:

```
void Prepare_PROM ()
{   //----------------------Disable Auto-read + Manual read once ----------------------
    Write(COMMAND,0xFB);          // Enter PROM Control Mode
    Write(COMMAND,0x96);          // Auto Load Set
    Write(COMMAND,0x10);          // Auto Load Disable
    Write(COMMAND,0x95);          // PROM writing setup
    Write(COMMAND,0x08);
    Write(COMMAND,0x91);          // Read/write mode setting
    Write(COMMAND,0x00);          // Set read mode
    delayms(10);                  // Delay 10ms
    Write(COMMAND, 0x94);         // Read active
    delayms(10);                  // Delay 10ms
    Write(COMMAND, 0x92);         // Cancel control
    Write(COMMAND, 0xF8);         //Exit PROM Control Mode
    delayms(20);                  // Delay 20ms
}
void Fine_tune_Vop ()
{   //--------------------------------Fine tune Vop offset-----------------------------------
    Write(COMMAND,0xFB);          // Enter PROM Control Mode
    Write( COMMAND, 0xDE);        // Fine tuning Vop here by command.
    or                            // 0xDE=VopOffset+1; 0xDF=VopOffset-1
    Write( COMMAND, 0xDF);        Note #2
    Write(COMMAND, 0xF8 );        //Exit PROM Control Mode
}
void Program_PROM ()
{
    Write(COMMAND,0xFB);          // Enter PROM Control Mode
    Write(COMMAND,0x91);          // Read/write mode setting
    Write(COMMAND,0x20);          // Set Write mode
    delayms(10);                  // Delay 10ms
    Write(COMMAND,0x93);          // Write active
    delayms(50);                  // Delay 50ms
    Write(COMMAND,0x92);          // Cancel control
    Write(COMMAND,0xF8);          //Exit PROM Control Mode
}
```

Note:

1. If Vop is incorrect and display performance is not accepted after PROM programmed, please redo this flow again to fine tune Vop again.
2. In this section, for “+” & “-” key button, please execute Write(COMMAND,0xDE) to increase one step at Vop and execute Write(COMMAND,0xDF) to decrease one step at Vop, if necessary.
3. Do not have the backlight closed to IC, because the temperature compensation is be turned ON during the burning process. The backlight may heat IC and influence the altitude of Vop.
4. This setting flow (Burning Flow) is used for LCM assembler.
5. PROM can be written 3 times.

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	–0.3 ~ 6.0	V
Internal Digital Operating Voltage	VDI	–0.3 ~ 3.0	V
Analog Power supply voltage	VDD2	–0.3 ~ 6.0	V
Power Supply Voltage (OSC & Vref)	VDD3	–0.3 ~ 6.0	V
LCD Power supply voltage	V3-MV3	–0.3 ~ 18	V
LCD Power supply voltage	V1	–0.3 ~ VDD2+0.3	V
LCD Power supply voltage	MV1	–(VDD2+0.3) ~ 0.3	V
MPU Interface Input Voltage	Vi	–0.3 ~ VDD1+0.3	V
Operating temperature	TOPR	–40 to +85	℃
Storage temperature	TSTR (COF) TSTR (Dice)	–55 to +100 –55 to +120	℃

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels always match the correct relation:
   V3 ≥ V1 ≥ VC ≥ MV1 ≥ MV3

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

13. DC CHARACTERISTICS

VSS=0V; Tamp = -40℃ to +85℃; unless otherwise specif ied.

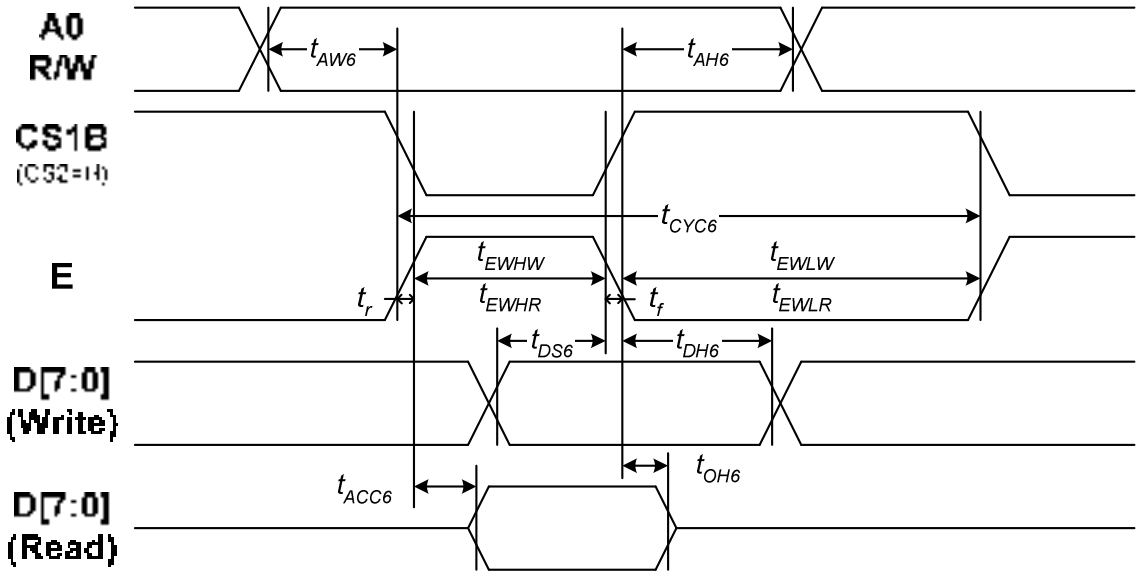
Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		2.7	–	5.5	V	VDD1
Operating Voltage (2)	VDD2		2.7	–	5.5	V	VDD2
Operating Voltage (3)	VDI		1.7	–	2.8	V	VDD3
Operating Voltage (4)	V3		VDD2–0.3V	–	9	V	V3
Operating Voltage (5)	V1		1	–	2.4	V	V1
MTP Operating Voltage	VPP		7.2	7.5	7.8	V	VPP
Input High-level Voltage	V_{IH}		0.7 x VDD1	–	VDD1	V	MPU Interface
Input Low-level Voltage	V_{IL}		VSS1	–	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OH}	I_{OUT}=1mA, VDD1=2.7V	0.8 x VDD1	–	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OL}	I_{OUT}=-1mA, VDD1=2.7V	VSS1	–	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		−1.0	–	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}		−3.0	–	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25℃ V3=9V ΔV=0.9V	–	–	–	KΩ	COMx
		Ta=25℃ V1=1.5V ΔV=0.15V	–	–	–	KΩ	SEGx
Frame Frequency	fFR	Display Line=132, FR=0x4, N-Line= 0x00, Ta = 25℃	–	75	–	Hz	

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=3.0V, 9V Ta=25℃	–	500	–	μA	
Power Down	ISS	VDD1=VDD2=3.0V, Ta=25℃	–	25	50	μA	

14. TIMING CHARACTERISTICS

System Bus Timing for 6800 Series MPU



(VDD1 = 3V~5V , Ta =25℃)

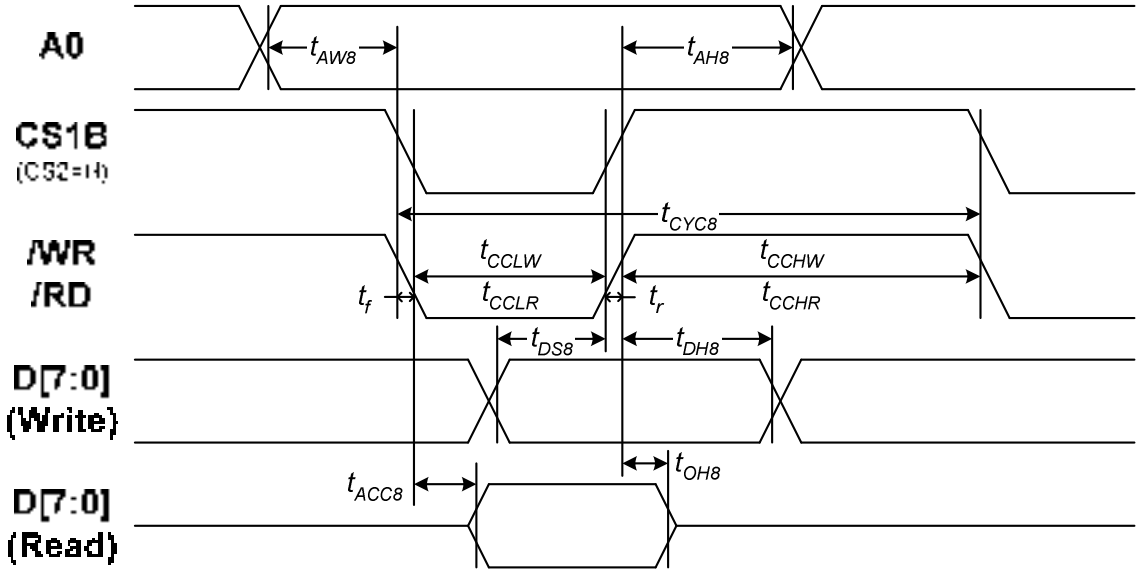
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	-	ns
Address hold time	R/W	tAH6		0	-	
System cycle time	E	tCYC6		300	-	
Enable L pulse width (Write)		tEWLW		95	-	
Enable H pulse width (Write)		tEWHW		30	-	
Enable L pulse width (Read)		tEWLR		30	-	
Enable H pulse width (Read)		tEWHR		100	-	
Write data setup time	D[7:0]	tDS6		40	-	
Write data hold time		tDH6		15	-	
Read data access time		tACC6	CL=100pF	-	140	
Read data output disable time		tOH6		10	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤ (tCYC6 - tEWLR - tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

System Bus Timing for 8080 Series MPU



(VDD1 = 3V~5V , Ta =25℃)

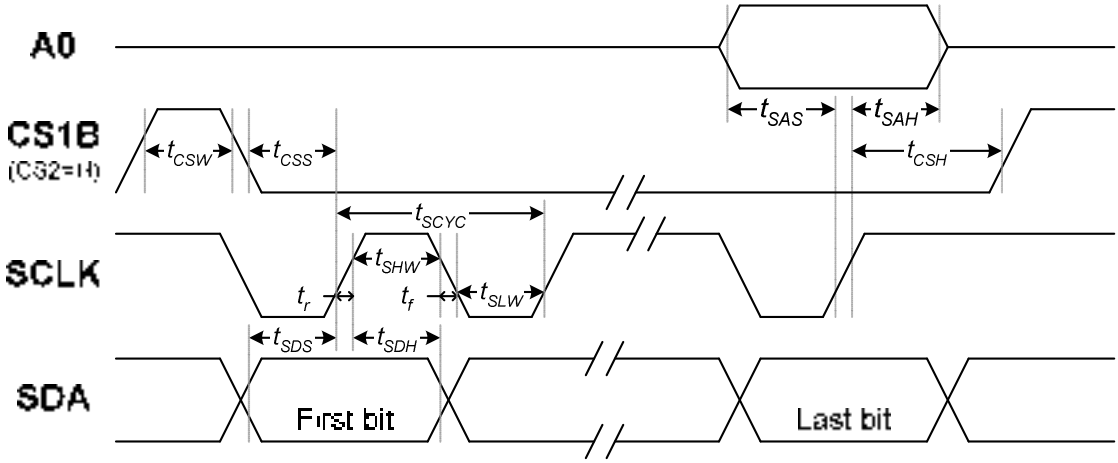
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	-	Ns
Address hold time		tAH8		0	-	
System cycle time	/WR	tCYC8		300	-	
/WR L pulse width		tCCLW		45	-	
/WR H pulse width		tCCHW		95	-	
/RD L pulse width	/RD	tCCLR		95	-	
/RD H pulse width		tCCHR		50	-	
Write Data setup time	D[7:0]	tDS8		40	-	
Write Data hold time		tDH8		15	-	
Read access time		tACC8	CL=100pF	-	140	
Read Output disable time		tOH8		10	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 - tCCLW - tCCHW) for (tr + tf) ≤ (tCYC8 - tCCLR - tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Timing for 4-Line Serial Interface



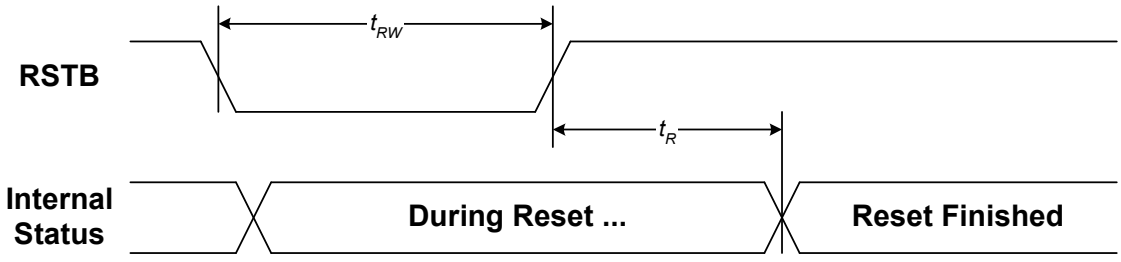
(VDD1 = 3V~5V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		250	-	ns
SCLK “H” pulse width		tSHW		100	-	
SCLK “L” pulse width		tSLW		100	-	
Address setup time	A0	tSAS		150	-	
Address hold time		tSAH		150	-	
Data setup time	SDA	tSDS		100	-	
Data hold time		tSDH		100	-	
Chip-select setup time	CS1B (CS2)	tCSS		150	-	
Chip-select hold time		tCSH		150	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

Hardware Reset Timing

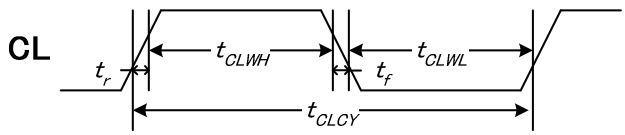


(VDD1 = 3V~5V , Ta =25℃)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR			3.5 *	us
Reset “L” pulse width	tRW		3.5		

* After a valid hardware reset, internal PROM will download its parameters to control registers automatically. Please don’t access the PROM related registers until 120ms after a valid hardware reset (i.e. tR=120ms in PROM related flow).

External Clock Timing



(VDD1 = 3V~5V, Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR Delay Time	FR	tDFR		-0.65	–	0.65	us
Clock High Pulse Width	CL	tCLWH	Default fCL=1630KHz	276.1	306.7	337.4	ns
Clock Low Pulse Width		tCLWL	ΔfFR=+/-10%	276.1	306.7	337.4	
Clock Cycle Time		tCLCY	*2, *3	552.1	613.5	674.8	
Clock Duty Ratio		tCLWH / tCLCY	*4	40	50	60	%
Clock Input Rising Time		tr		0	–	20	ns
Clock Input Falling Time		tf		0	–	20	

Note:

1. All timings are specified by 20% and 80% of VDD1 as the reference.
2. Be sure the real cycle time of CL includes tr and tf, so that : tCLCY = (tCLWH + tCLWL + tr + tf) are specified.
3. It is necessary to secure tCLCY, tCLWH & tCLWL even if the external CL is out of this specification.
   Ex, tCLCY = (tCLWH + tCLWL + β)..... , where “$\beta > tr_{(max)} + tf_{(max)}$” but tCLCY must be in specification.
4. tCLCY is still in specification.
5. AC timing of CL pin controls the accuracy of operation clock. This definition includes 10% tolerance already.
6. This specification defines the default speed of internal clock system. If the timing is over specification, all related speed should be re-calculated (such as, fFR and clock based operations).

APPLICATION NOTE

Application Circuits

6800 series 8-bit Interface:

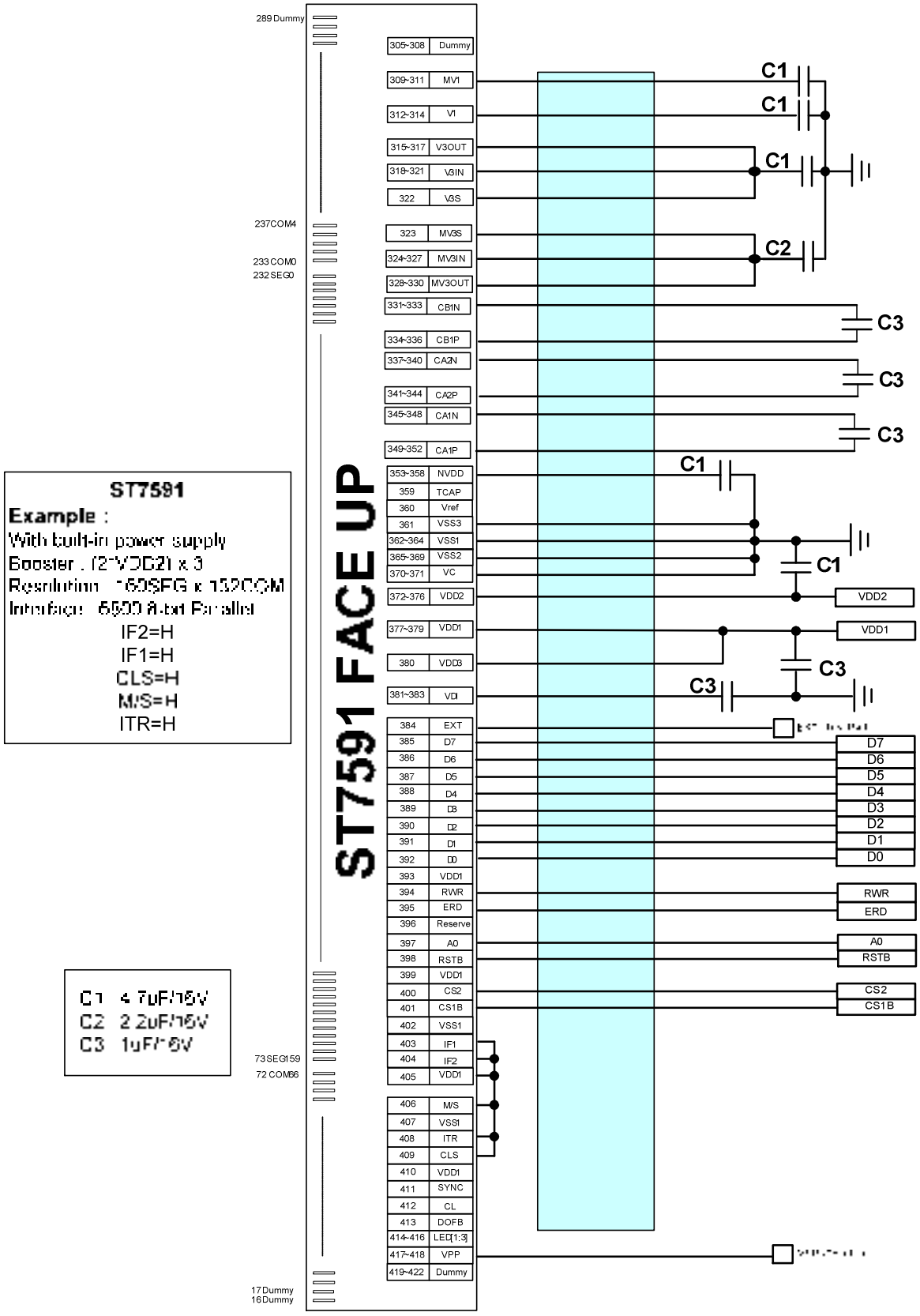


Fig. 15. Reference Application Circuit: Parallel 6800 Interface

8080 series 8-bit Interface:

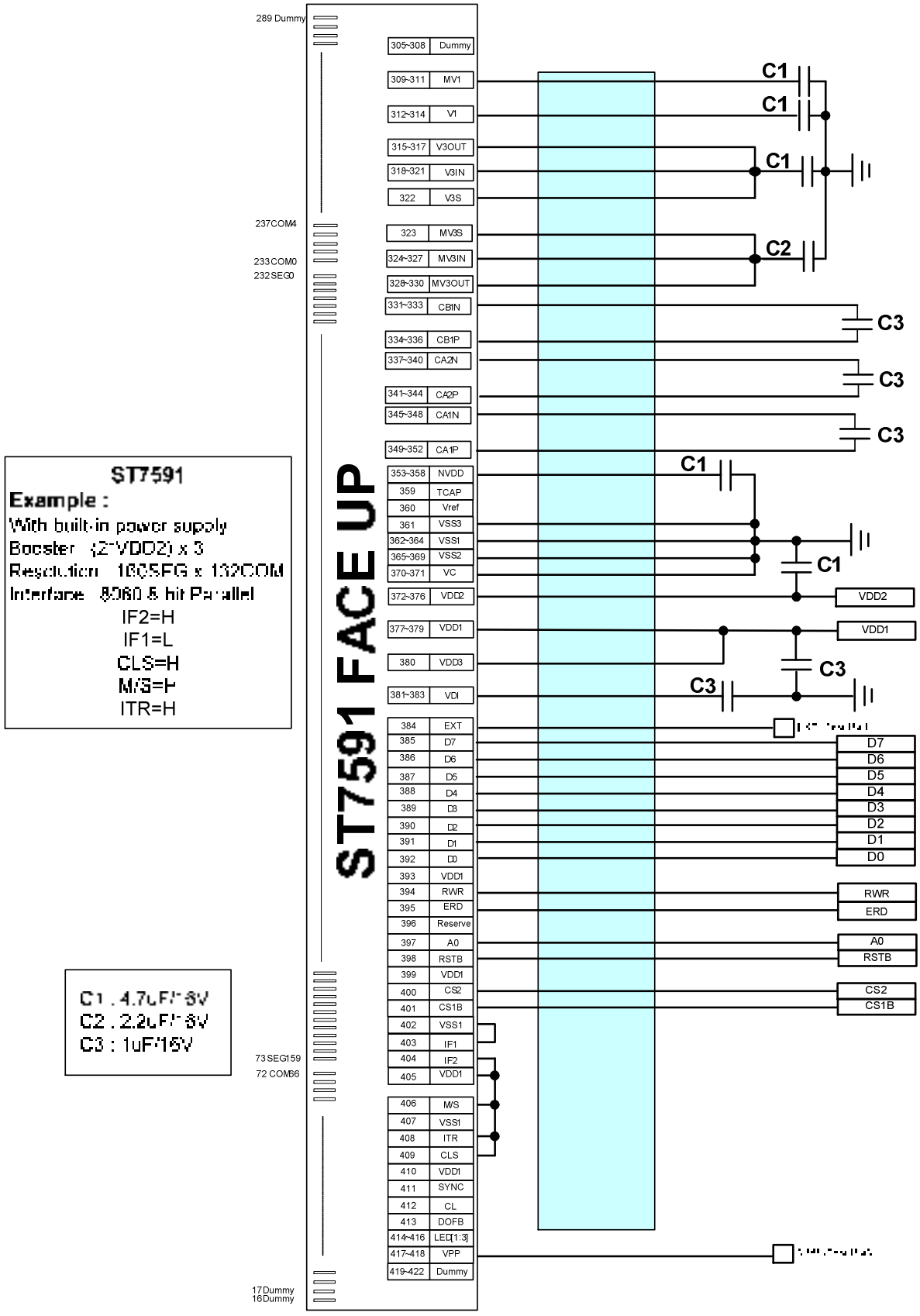


Fig. 16. Reference Application Circuit: Parallel 8080 Interface

4-Line series Interface:

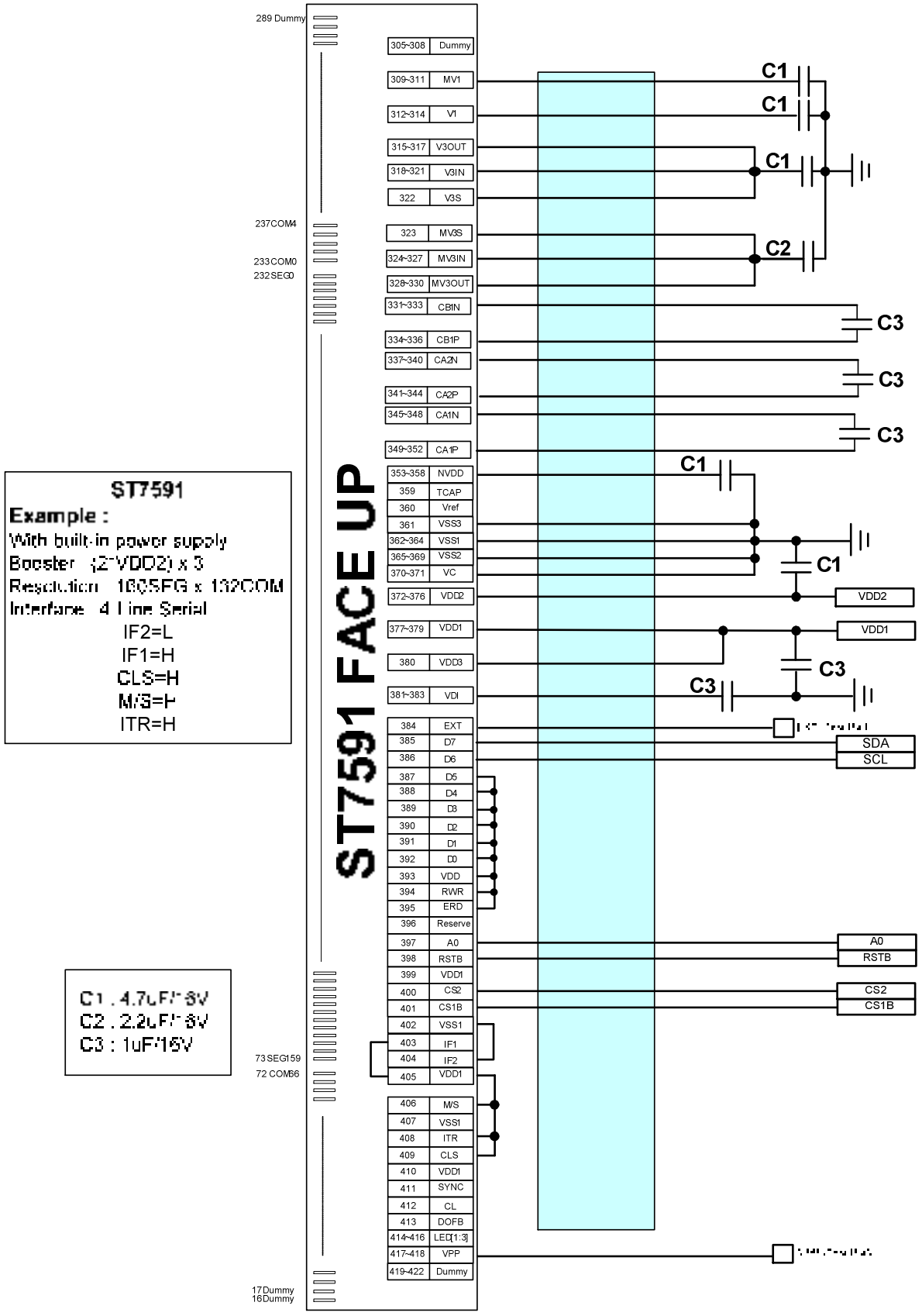


Fig. 17. Reference Application Circuit: Serial 4-Line Interface

Master/Slave Mode Connection with Internal Power (only for TCP/COF Applications)

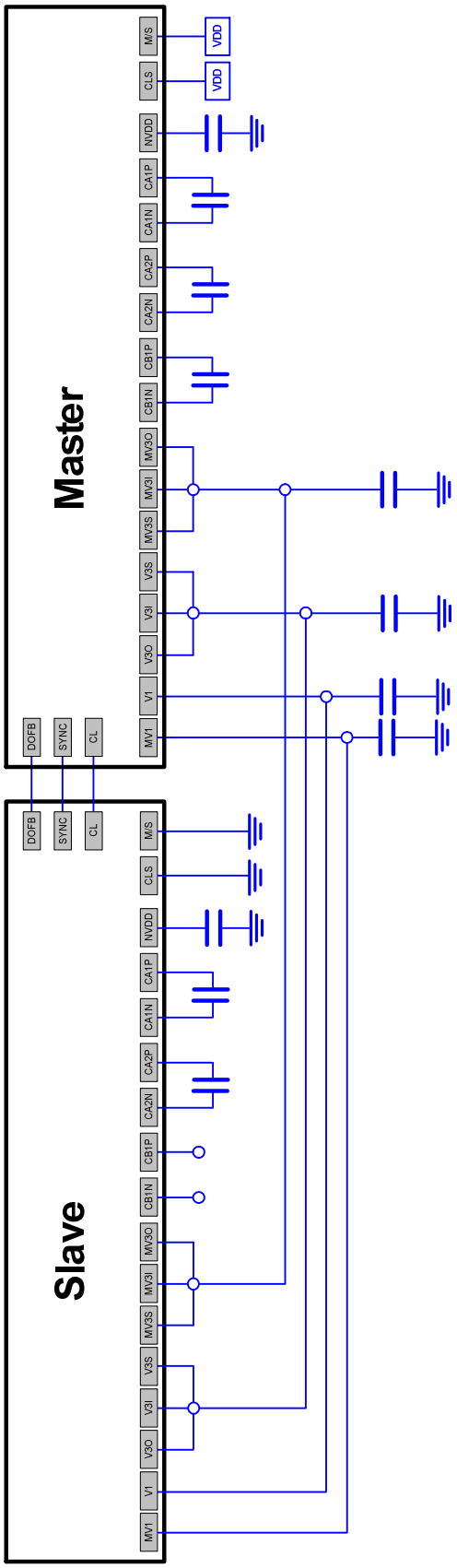


Fig. 18. Reference Application Circuit: Master/Slave Connection with Internal Power

Master/Slave Mode Connection with External Power (only for TCP/COF Applications)

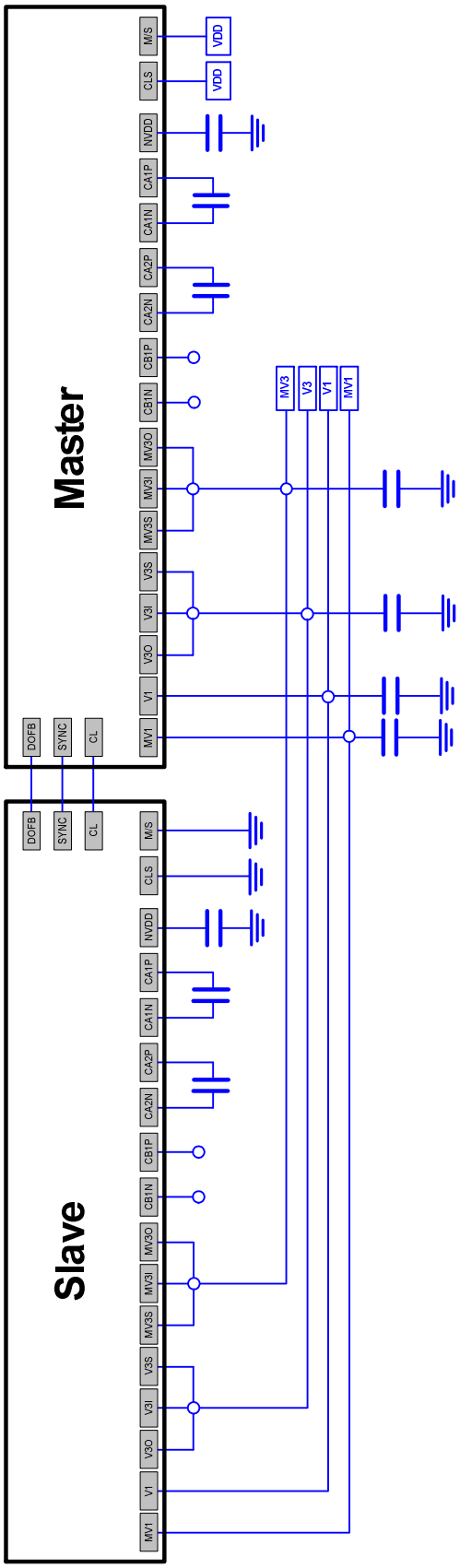


Fig. 19. Reference Application Circuit: Master/Slave Connection with External Power

REVERSION HISTORY

Version	Date	Description
1.1	2010/07	● Add Power OFF Flow ● Add LED[1:3] control singles description
1.2	2010/07/19	● Modify parameter description of Set Display Duty
1.2a	2010/07/20	● Fix typing mistake of Set Display Duty
1.3	2010/11/01	● Add display duty options to Page 1. ● Modify description of “Set COM0”. ● Rename “Set Partial Duty” to be “Set Display Duty”. ● Add notes to “Set Display Duty” & “Set Bias”. ● Fix typing mistake in “Set Booster” description. ● Rewrite “Set Frame Rate 1 & 2” description. ● Add frequency for 112 display lines in “Set Frame Rate 1 & 2” description. ● Fix “Test” instruction description. ● Add date to each page.
1.4	2011/3/24	● Release COF package and Master/Slave function is for COF products. ● Add N-Line function. ● Fix description mistakes about TC (Temperature Compensation) function. ● Redraw IC outline for better resolution. ● Shift the Origin point (0,0) to the center of the left alignment mark for ITO layout. ● Rearrange pin group in Pin Description and rename pin group: Power System Pins -> Power Supply Pins System Control Pins -> LCD Power System Pins ● Add missing pins (TCAP, NVDD, LED[1:3]) into “Recommend ITO Resistance”. ● Add more detailed description into “ITO Layout Notes”. ● Renumber figures. ● Fix Booster Level description : x2, x3, x4 -> (VDD2 * 2) x2, (VDD2 * 2) x3, (VDD2 * 2) x4. ● External fOCL: 1630KHz. ● Fix instruction mismatch : EPCTIN, Drive Mode Selection. ● Rearrange instruction order in Instruction Description and match this order with Instruction Table. ● Fix general typing mistakes. ● Add more detailed information into Instruction Flow. ● Decrease wait time for Power Control related flows. ● Fix typing mistakes of pin name in application circuits. ● Remove reversion history before V1.0.
1.5	2011/5/6	● Release all duty setting. ● Conditionally release Master/Slave feature for COG application. ● Add power application circuits and modify Power OFF Flow (and redraw figure) for external power applications. ● In order to prevent confusing with N-Line, the symbol in optimize bias formula changes from N to M. ● Fix N-Line description mistake. ● Add external clock timing specification.