1. INTRODUCTION

ST7580A is a single-chip LSI for graphic dot-matrix LCD systems. It incorporates LCD controller, LCD drivers and LCD power system. It can be connected directly to a microprocessor which supports 8-bit parallel interface or 4-line serial interface (SPI-4). Display data is stored in the internal Display Data RAM (DDRAM, 160x84 bits). The display data bits in DDRAM are directly related to the pixels on LCD panel. With built-in oscillation circuit and low power consumption power circuits, ST7580A can drive an LCD panel without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

2. FEATURES

Single-Chip LCD Controller & Driver

ML (Multi-Line) Driving Method

On-chip Display Data RAM (DDRAM)

- Capacity: 160 x 84 = 13,440 bits

LCD Driver Outputs

- 160 segment outputs x 84 common outputs

Microprocessor Interface

- Bidirectional 8-bit parallel interface supports: 8080-series and 6800-series MPU
- Serial interface (SPI-4, write only)

External Hardware Reset Pin (RSTB)

Built-in Oscillation Circuit

- No external component required

Built-in Low Power Consumption Analog Circuit

- Programmable Voltage Booster
- High-accuracy Voltage Regulator for LCD Vop (with programmable Temperature Gradient)
- Voltage Follower for LCD bias voltage

Wide Operation Voltage Range

- VDD1-VSS1=3V~5V (Typical)
- VDD2-VSS2=3V~5V (Typical)

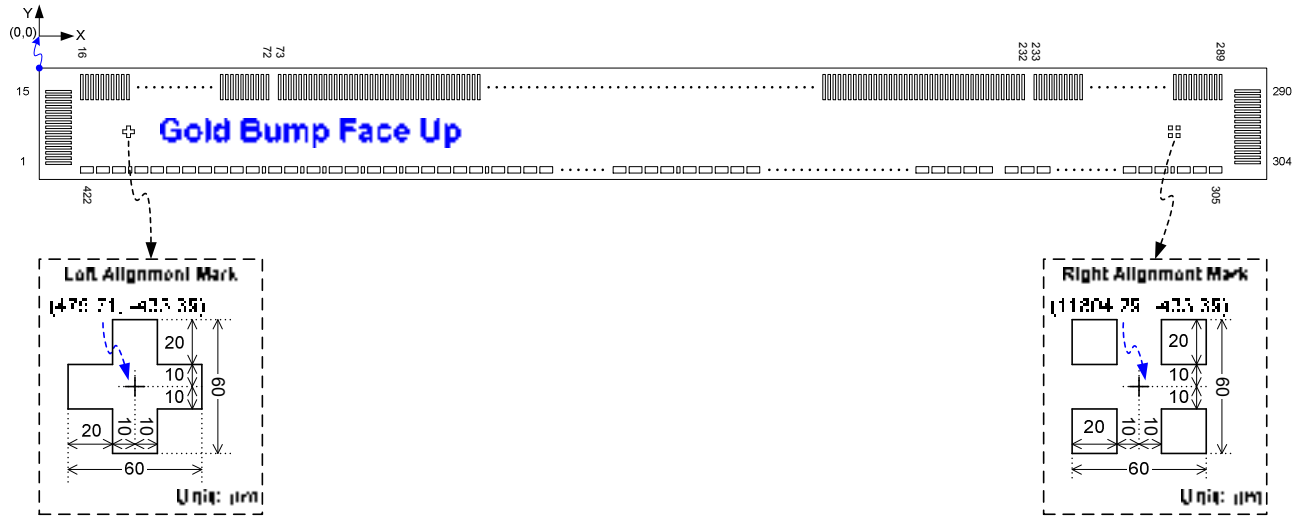
LCD Operation Voltage Range

- Maximum LCD Vop: 18V (V3: 9V, MV3: -9V)
- Typical Operation Range: 6V~17V (V3=3V~8.5V)

Temperature Range: -40~85℃

Package Type: COG

3-1. BARE CHIP OUTLINE



Unit: um

Part Number	Chip Size	Chip Thickness	Bump Height
ST7580A	12700 x 780	480	15
Pad Number	**Pad Pitch (Minimum)**	**Pad Number**	**Bump Size**
1~15, 16~72, 73~232, 233~289, 290~304	43	1~15, 290~304	96 x 26
72~73, 232~233	100	16~289	26 x 96
330~331	157.5	308, 360, 393, 399, 402, 405, 407, 410, 419	30 x 45
309~330, 331~359, 361~392, 394~398, 400~401, 403~404, 408~409, 411~418	105	305~307, 309~359, 361~392, 394~398, 400~401, 403~404, 406, 408~409, 411~418, 420~422	80 x 45
307~309, 359~361, 392~394, 398~400, 401~403, 404~408, 409~411, 418~420	78.75		
305~307, 420~422	103.75		
*** Refer to section "PAD CENTER COORDINATES" for ITO layout.**			

3-2. PAD CENTER COORDINATES

PAD NO.	PAD NAME	X	Y
1	Reserved	261.5	-691
2	Reserved	261.5	-648
3	Reserved	261.5	-605
4	Reserved	261.5	-562
5	Reserved	261.5	-519
6	Reserved	261.5	-476
7	Reserved	261.5	-433
8	Reserved	261.5	-390
9	Reserved	261.5	-347
10	Reserved	261.5	-304
11	Reserved	261.5	-261
12	Reserved	261.5	-218
13	Reserved	261.5	-175
14	Reserved	261.5	-132
15	Reserved	261.5	-89
16	Dummy	423.5	-71.5
17	Dummy	466.5	-71.5
18	Dummy	509.5	-71.5
19	Dummy	552.5	-71.5
20	Dummy	595.5	-71.5
21	Dummy	638.5	-71.5
22	Reserved	681.5	-71.5
23	Reserved	724.5	-71.5
24	Reserved	767.5	-71.5
25	Reserved	810.5	-71.5
26	Reserved	853.5	-71.5
27	Reserved	896.5	-71.5
28	Reserved	939.5	-71.5
29	Reserved	982.5	-71.5
30	Reserved	1025.5	-71.5
31	COM83	1068.5	-71.5
32	COM82	1111.5	-71.5
33	COM81	1154.5	-71.5
34	COM77	1197.5	-71.5
35	COM76	1240.5	-71.5
36	COM75	1283.5	-71.5
37	COM71	1326.5	-71.5
38	COM70	1369.5	-71.5
39	COM69	1412.5	-71.5
40	COM65	1455.5	-71.5
41	COM64	1498.5	-71.5
42	COM63	1541.5	-71.5
43	COM59	1584.5	-71.5
44	COM58	1627.5	-71.5
45	COM57	1670.5	-71.5
46	COM53	1713.5	-71.5

PAD NO.	PAD NAME	X	Y
47	COM52	1756.5	-71.5
48	COM51	1799.5	-71.5
49	COM47	1842.5	-71.5
50	COM46	1885.5	-71.5
51	COM45	1928.5	-71.5
52	COM41	1971.5	-71.5
53	COM40	2014.5	-71.5
54	COM39	2057.5	-71.5
55	COM35	2100.5	-71.5
56	COM34	2143.5	-71.5
57	COM33	2186.5	-71.5
58	COM29	2229.5	-71.5
59	COM28	2272.5	-71.5
60	COM27	2315.5	-71.5
61	COM23	2358.5	-71.5
62	COM22	2401.5	-71.5
63	COM21	2444.5	-71.5
64	COM17	2487.5	-71.5
65	COM16	2530.5	-71.5
66	COM15	2573.5	-71.5
67	COM11	2616.5	-71.5
68	COM10	2659.5	-71.5
69	COM9	2702.5	-71.5
70	COM5	2745.5	-71.5
71	COM4	2788.5	-71.5
72	COM3	2831.5	-71.5
73	SEG159	2931.5	-71.5
74	SEG158	2974.5	-71.5
75	SEG157	3017.5	-71.5
76	SEG156	3060.5	-71.5
77	SEG155	3103.5	-71.5
78	SEG154	3146.5	-71.5
79	SEG153	3189.5	-71.5
80	SEG152	3232.5	-71.5
81	SEG151	3275.5	-71.5
82	SEG150	3318.5	-71.5
83	SEG149	3361.5	-71.5
84	SEG148	3404.5	-71.5
85	SEG147	3447.5	-71.5
86	SEG146	3490.5	-71.5
87	SEG145	3533.5	-71.5
88	SEG144	3576.5	-71.5
89	SEG143	3619.5	-71.5
90	SEG142	3662.5	-71.5
91	SEG141	3705.5	-71.5
92	SEG140	3748.5	-71.5

PAD NO.	PAD NAME	X	Y
93	SEG139	3791.5	-71.5
94	SEG138	3834.5	-71.5
95	SEG137	3877.5	-71.5
96	SEG136	3920.5	-71.5
97	SEG135	3963.5	-71.5
98	SEG134	4006.5	-71.5
99	SEG133	4049.5	-71.5
100	SEG132	4092.5	-71.5
101	SEG131	4135.5	-71.5
102	SEG130	4178.5	-71.5
103	SEG129	4221.5	-71.5
104	SEG128	4264.5	-71.5
105	SEG127	4307.5	-71.5
106	SEG126	4350.5	-71.5
107	SEG125	4393.5	-71.5
108	SEG124	4436.5	-71.5
109	SEG123	4479.5	-71.5
110	SEG122	4522.5	-71.5
111	SEG121	4565.5	-71.5
112	SEG120	4608.5	-71.5
113	SEG119	4651.5	-71.5
114	SEG118	4694.5	-71.5
115	SEG117	4737.5	-71.5
116	SEG116	4780.5	-71.5
117	SEG115	4823.5	-71.5
118	SEG114	4866.5	-71.5
119	SEG113	4909.5	-71.5
120	SEG112	4952.5	-71.5
121	SEG111	4995.5	-71.5
122	SEG110	5038.5	-71.5
123	SEG109	5081.5	-71.5
124	SEG108	5124.5	-71.5
125	SEG107	5167.5	-71.5
126	SEG106	5210.5	-71.5
127	SEG105	5253.5	-71.5
128	SEG104	5296.5	-71.5
129	SEG103	5339.5	-71.5
130	SEG102	5382.5	-71.5
131	SEG101	5425.5	-71.5
132	SEG100	5468.5	-71.5
133	SEG99	5511.5	-71.5
134	SEG98	5554.5	-71.5
135	SEG97	5597.5	-71.5
136	SEG96	5640.5	-71.5
137	SEG95	5683.5	-71.5
138	SEG94	5726.5	-71.5
139	SEG93	5769.5	-71.5
140	SEG92	5812.5	-71.5

PAD NO.	PAD NAME	X	Y
141	SEG91	5855.5	-71.5
142	SEG90	5898.5	-71.5
143	SEG89	5941.5	-71.5
144	SEG88	5984.5	-71.5
145	SEG87	6027.5	-71.5
146	SEG86	6070.5	-71.5
147	SEG85	6113.5	-71.5
148	SEG84	6156.5	-71.5
149	SEG83	6199.5	-71.5
150	SEG82	6242.5	-71.5
151	SEG81	6285.5	-71.5
152	SEG80	6328.5	-71.5
153	SEG79	6371.5	-71.5
154	SEG78	6414.5	-71.5
155	SEG77	6457.5	-71.5
156	SEG76	6500.5	-71.5
157	SEG75	6543.5	-71.5
158	SEG74	6586.5	-71.5
159	SEG73	6629.5	-71.5
160	SEG72	6672.5	-71.5
161	SEG71	6715.5	-71.5
162	SEG70	6758.5	-71.5
163	SEG69	6801.5	-71.5
164	SEG68	6844.5	-71.5
165	SEG67	6887.5	-71.5
166	SEG66	6930.5	-71.5
167	SEG65	6973.5	-71.5
168	SEG64	7016.5	-71.5
169	SEG63	7059.5	-71.5
170	SEG62	7102.5	-71.5
171	SEG61	7145.5	-71.5
172	SEG60	7188.5	-71.5
173	SEG59	7231.5	-71.5
174	SEG58	7274.5	-71.5
175	SEG57	7317.5	-71.5
176	SEG56	7360.5	-71.5
177	SEG55	7403.5	-71.5
178	SEG54	7446.5	-71.5
179	SEG53	7489.5	-71.5
180	SEG52	7532.5	-71.5
181	SEG51	7575.5	-71.5
182	SEG50	7618.5	-71.5
183	SEG49	7661.5	-71.5
184	SEG48	7704.5	-71.5
185	SEG47	7747.5	-71.5
186	SEG46	7790.5	-71.5
187	SEG45	7833.5	-71.5
188	SEG44	7876.5	-71.5

PAD NO.	PAD NAME	X	Y
189	SEG43	7919.5	-71.5
190	SEG42	7962.5	-71.5
191	SEG41	8005.5	-71.5
192	SEG40	8048.5	-71.5
193	SEG39	8091.5	-71.5
194	SEG38	8134.5	-71.5
195	SEG37	8177.5	-71.5
196	SEG36	8220.5	-71.5
197	SEG35	8263.5	-71.5
198	SEG34	8306.5	-71.5
199	SEG33	8349.5	-71.5
200	SEG32	8392.5	-71.5
201	SEG31	8435.5	-71.5
202	SEG30	8478.5	-71.5
203	SEG29	8521.5	-71.5
204	SEG28	8564.5	-71.5
205	SEG27	8607.5	-71.5
206	SEG26	8650.5	-71.5
207	SEG25	8693.5	-71.5
208	SEG24	8736.5	-71.5
209	SEG23	8779.5	-71.5
210	SEG22	8822.5	-71.5
211	SEG21	8865.5	-71.5
212	SEG20	8908.5	-71.5
213	SEG19	8951.5	-71.5
214	SEG18	8994.5	-71.5
215	SEG17	9037.5	-71.5
216	SEG16	9080.5	-71.5
217	SEG15	9123.5	-71.5
218	SEG14	9166.5	-71.5
219	SEG13	9209.5	-71.5
220	SEG12	9252.5	-71.5
221	SEG11	9295.5	-71.5
222	SEG10	9338.5	-71.5
223	SEG9	9381.5	-71.5
224	SEG8	9424.5	-71.5
225	SEG7	9467.5	-71.5
226	SEG6	9510.5	-71.5
227	SEG5	9553.5	-71.5
228	SEG4	9596.5	-71.5
229	SEG3	9639.5	-71.5
230	SEG2	9682.5	-71.5
231	SEG1	9725.5	-71.5
232	SEG0	9768.5	-71.5
233	COM0	9868.5	-71.5
234	COM1	9911.5	-71.5
235	COM2	9954.5	-71.5
236	COM6	9997.5	-71.5

PAD NO.	PAD NAME	X	Y
237	COM7	10040.5	-71.5
238	COM8	10083.5	-71.5
239	COM12	10126.5	-71.5
240	COM13	10169.5	-71.5
241	COM14	10212.5	-71.5
242	COM18	10255.5	-71.5
243	COM19	10298.5	-71.5
244	COM20	10341.5	-71.5
245	COM24	10384.5	-71.5
246	COM25	10427.5	-71.5
247	COM26	10470.5	-71.5
248	COM30	10513.5	-71.5
249	COM31	10556.5	-71.5
250	COM32	10599.5	-71.5
251	COM36	10642.5	-71.5
252	COM37	10685.5	-71.5
253	COM38	10728.5	-71.5
254	COM42	10771.5	-71.5
255	COM43	10814.5	-71.5
256	COM44	10857.5	-71.5
257	COM48	10900.5	-71.5
258	COM49	10943.5	-71.5
259	COM50	10986.5	-71.5
260	COM54	11029.5	-71.5
261	COM55	11072.5	-71.5
262	COM56	11115.5	-71.5
263	COM60	11158.5	-71.5
264	COM61	11201.5	-71.5
265	COM62	11244.5	-71.5
266	COM66	11287.5	-71.5
267	COM67	11330.5	-71.5
268	COM68	11373.5	-71.5
269	COM72	11416.5	-71.5
270	COM73	11459.5	-71.5
271	COM74	11502.5	-71.5
272	COM78	11545.5	-71.5
273	COM79	11588.5	-71.5
274	COM80	11631.5	-71.5
275	Reserved	11674.5	-71.5
276	Reserved	11717.5	-71.5
277	Reserved	11760.5	-71.5
278	Reserved	11803.5	-71.5
279	Reserved	11846.5	-71.5
280	Reserved	11889.5	-71.5
281	Reserved	11932.5	-71.5
282	Reserved	11975.5	-71.5
283	Reserved	12018.5	-71.5
284	Dummy	12061.5	-71.5

PAD NO.	PAD NAME	X	Y
285	Dummy	12104.5	-71.5
286	Dummy	12147.5	-71.5
287	Dummy	12190.5	-71.5
288	Dummy	12233.5	-71.5
289	Dummy	12276.5	-71.5
290	Reserved	12438.5	-89
291	Reserved	12438.5	-132
292	Reserved	12438.5	-175
293	Reserved	12438.5	-218
294	Reserved	12438.5	-261
295	Reserved	12438.5	-304
296	Reserved	12438.5	-347
297	Reserved	12438.5	-390
298	Reserved	12438.5	-433
299	Reserved	12438.5	-476
300	Reserved	12438.5	-519
301	Reserved	12438.5	-562
302	Reserved	12438.5	-605
303	Reserved	12438.5	-648
304	Reserved	12438.5	-691
305	Dummy	12280	-734
306	Dummy	12176.25	-734
307	Dummy	12072.5	-734
308	Dummy	11993.75	-734
309	MV1	11915	-734
310	MV1	11810	-734
311	MV1	11705	-734
312	V1	11600	-734
313	V1	11495	-734
314	V1	11390	-734
315	V3O	11285	-734
316	V3O	11180	-734
317	V3O	11075	-734
318	V3I	10970	-734
319	V3I	10865	-734
320	V3I	10760	-734
321	V3I	10655	-734
322	V3S	10550	-734
323	MV3S	10445	-734
324	MV3I	10340	-734
325	MV3I	10235	-734
326	MV3I	10130	-734
327	MV3I	10025	-734
328	MV3O	9920	-734
329	MV3O	9815	-734
330	MV3O	9710	-734
331	CB1N	9552.5	-734
332	CB1N	9447.5	-734

PAD NO.	PAD NAME	X	Y
333	CB1N	9342.5	-734
334	CB1P	9237.5	-734
335	CB1P	9132.5	-734
336	CB1P	9027.5	-734
337	CA2N	8922.5	-734
338	CA2N	8817.5	-734
339	CA2N	8712.5	-734
340	CA2N	8607.5	-734
341	CA2P	8502.5	-734
342	CA2P	8397.5	-734
343	CA2P	8292.5	-734
344	CA2P	8187.5	-734
345	CA1N	8082.5	-734
346	CA1N	7977.5	-734
347	CA1N	7872.5	-734
348	CA1N	7767.5	-734
349	CA1P	7662.5	-734
350	CA1P	7557.5	-734
351	CA1P	7452.5	-734
352	CA1P	7347.5	-734
353	NVDD	7242.5	-734
354	NVDD	7137.5	-734
355	NVDD	7032.5	-734
356	NVDD	6927.5	-734
357	NVDD	6822.5	-734
358	NVDD	6717.5	-734
359	TCAP	6612.5	-734
360	Vref	6533.75	-734
361	VSS3	6455	-734
362	VSS1	6350	-734
363	VSS1	6245	-734
364	VSS1	6140	-734
365	VSS2	6035	-734
366	VSS2	5930	-734
367	VSS2	5825	-734
368	VSS2	5720	-734
369	VSS2	5615	-734
370	VC	5510	-734
371	VC	5405	-734
372	VDD2	5300	-734
373	VDD2	5195	-734
374	VDD2	5090	-734
375	VDD2	4985	-734
376	VDD2	4880	-734
377	VDD1	4775	-734
378	VDD1	4670	-734
379	VDD1	4565	-734
380	VDD3	4460	-734

PAD NO.	PAD NAME	X	Y
381	VDI	4355	-734
382	VDI	4250	-734
383	VDI	4145	-734
384	EXTB	4040	-734
385	D7	3935	-734
386	D6	3830	-734
387	D5	3725	-734
388	D4	3620	-734
389	D3	3515	-734
390	D2	3410	-734
391	D1	3305	-734
392	D0	3200	-734
393	VDD1	3121.25	-734
394	RWR	3042.5	-734
395	ERD	2937.5	-734
396	Reserved	2832.5	-734
397	A0	2727.5	-734
398	RSTB	2622.5	-734
399	VDD1	2543.75	-734
400	CS2	2465	-734
401	CS1B	2360	-734
402	VSS1	2281.25	-734
403	IF1	2202.5	-734
404	IF2	2097.5	-734
405	VDD1	2018.75	-734
406	M/S	1940	-734
407	VSS1	1861.25	-734
408	TP3	1782.5	-734
409	CLS	1677.5	-734
410	VDD1	1598.75	-734
411	SYNC	1520	-734
412	CL	1415	-734
413	DOFB	1310	-734
414	TP2	1205	-734
415	TP1	1100	-734
416	TP0	995	-734
417	VPP	890	-734
418	VPP	785	-734
419	Dummy	706.25	-734
420	Dummy	627.5	-734
421	Dummy	523.75	-734
422	Dummy	420	-734

* Unit: um

4. BLOCK DIAGRAM

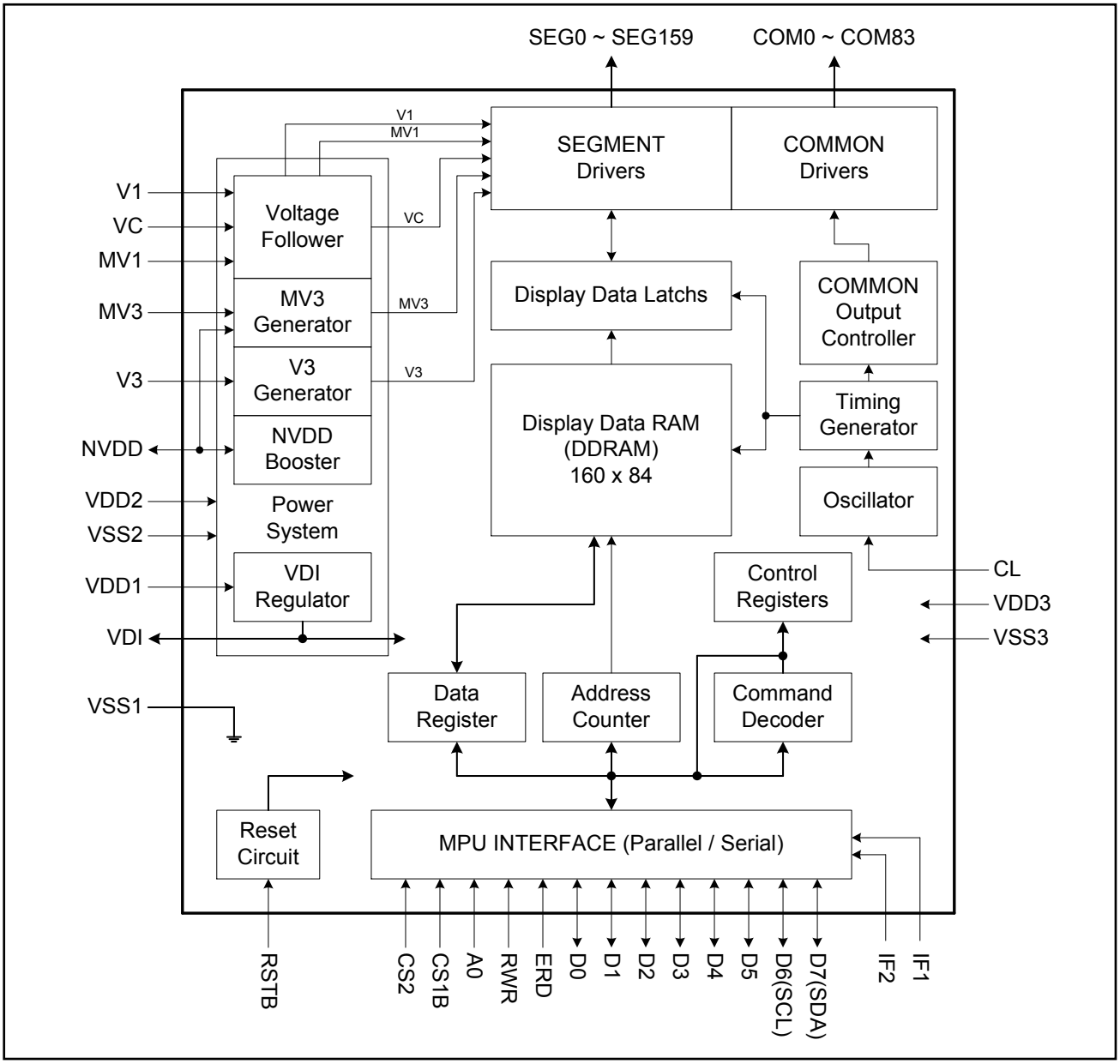


Fig. 1. Block Diagram

5. PIN DESCRIPTION

Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>IF[2:1]</td><td>I</td><td>IF2 selects the interface mode (Serial or Parallel), while IF1 selects the microprocessor type in parallel interface mode (8080-series or 6800-series).
<table>
<tr><th>IF2</th><th>IF1</th><th>Selected Interface</th></tr>
<tr><td>“H”</td><td>“H”</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>Serial 4-Line SPI Interface</td></tr>
<tr><td>“L”</td><td>“L”</td><td>Reserved (do NOT use)</td></tr>
</table>
Please refer to “APPLICATION NOTES” and “Microprocessor Interface” (Section 6) for detailed connection of the selected interface.</td></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin, when RSTB is “L”, initialization is executed.</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select pins. Interface is enabled when both CS1B is “L” and CS2 is “H”. If chip select pins are not active (CS1B=“H” or CS2=“L”), D[7:0] become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H”: Indicates that signals on D[7:0] are display data.
A0=“L”: Indicates that signals on D[7:0] are command.</td></tr>
<tr><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When chip select pins are not active (CS1B=“H” & CS2=“L”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I</td><td>When using serial interface: 4-Line
D7=SDA : Serial data input.
D6=SCL : Serial clock input.
D[5:0] are not used and should connect to “H” by VDD1.
When chip select pins are not active (CS1B=“H” & CS2=“L”), D[7:0] pins are high impedance.</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin.
<table>
<tr><th>IF2</th><th>IF1</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>H</td><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is not used in serial interface and should fix to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin.
<table>
<tr><th>IF2</th><th>IF1</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>H</td><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is not used in serial interface and should fix to “H” by VDD1.</td></tr>
</table>

Note: After VDD1 is turned ON, any MPU interface pins cannot be left floating.

LCD Driver Output Pins

Pin Name	Type	Description
SEG0 ~ 159	**O**	LCD segment driver outputs. One of the V1, VC and MV1 levels is selected by a combination of the DDRAM data, frame signal and field.
COM0 ~ 83	**O**	LCD common driver outputs. One of the V3, VC and MV3 levels is selected by a combination of the scan signal, frame signal and field.

Power Supply Pins

Pin Name	Type	Description
VDD1	**Power**	Power supply for digital I/O circuits (MPU Interface and Configuration pins). It is the same voltage level as VDD3. Connect with VDD3 by FPC externally.
VDD2	**Power**	Power supply for analog circuit.
VDD3	**Power**	Power supply for internal oscillator and Vref circuits. It is the same voltage level as VDD1. Connect with VDD1 by FPC externally.
VSS1	**Power**	Ground of digital I/O circuits (MPU Interface and Configuration pins). Connect with VSS3 by FPC externally.
VSS2	**Power**	Ground of analog circuit. All ground systems should be connected together by FPC or system circuit.
VSS3	**Power**	Ground of internal oscillator and Vref circuits. Connect with VSS1 by FPC externally.
VDI	**Power**	This pin is used to monitor internal logic power status.
VPP	**Power**	When programming PROM, provide an external power (7.5V, >4mA) to VPP. The EXTB pin should be “L” to enable PROM operation.
NVDD	**Power**	The negative power for analog circuit.
V3O V3I V3S	**Power**	LCD driver supply power. V3O is the output voltage of the built-in V3 generator. V3I is the input pin of LCD driver circuit. V3S is the input pin of the built-in V3 generator. It senses V3 voltage. V3O, V3I & V3S should be connected together at FPC side.
MV3O MV3I MV3S	**Power**	LCD driver supply power. MV3O is the output voltage of the built-in MV3 generator. MV3I is the input pin of LCD driver circuit. MV3S is the input pin of the built-in MV3 generator. It senses MV3 voltage. MV3O, MV3I & MV3S should be connected together at FPC side.
V1, MV1	**Power**	These pins are LCD driver supply powers for different output levels. These powers should have the following relationship: V3 ≥ V1 ≥ VC (VSS2) ≥ MV1 ≥ MV3
VC	**Power**	LCD driver supply power for center level. Connect to VSS2 by system circuit externally.
CA1P, CA1N CA2P, CA2N	**Power**	Positive and negative sides of the booster capacitor. These are the booster capacitors for NVDD.
CB1P, CB1N	**Power**	Positive and negative sides of the booster capacitor. This is the booster capacitor for MV3.

Configuration Pins

Pin Name	Type	Description
CLS	**I**	Clock source selection pin. CLS="H" (VDD1): enable internal clock. CLS="L" (VSS1): disable internal clock and use external clock.
CL	**I/O**	If CLS="H", the internal clock will be outputted to this pin. If CLS="L", this pin should apply the external clock (typical 1630KHz).

Test Pins

Pin Name	Type	Description
EXTB	**I**	The operation of the internal PROM will be enabled only when EXTB="L" (VSS1). This is used to prevent unexpected operate to PROM. Note: It is pulled-up internally (by resistor). Left it OPEN (default) when not operating.
Vref	**Test**	Internal reference voltage output. Any kind of connection to this pin is not recommended. Left this pin floating.
TP0~TP2	**Test**	Test pins. Left them floating.
TP3	**I**	It is reserved for testing, set it to "H".
TCAP	**Test**	Test pins. Left this pin floating.
Reserved	**-**	These pins are reserved only. Please don't connect these pins.
Dummy	**-**	These pins are no connection into internal IC. They are floating.
M/S	**I**	This pin is reserved for test. Please fix M/S="H" (VDD1).
SYNC	**I/O**	This pin is reserved for test. Please leave this pin floating.
DOFB	**I/O**	This pin is reserved for test. Please leave this pin floating.

Note:

1. The option setting to be "H" should connect to VDD1, and the option setting to be "L" should connect to VSS1.
2. The single VDD1/VSS1 pads in interface pins are used for ITO option. They don't have ESD protection circuit inside. Please don't connect them to FPC output side.

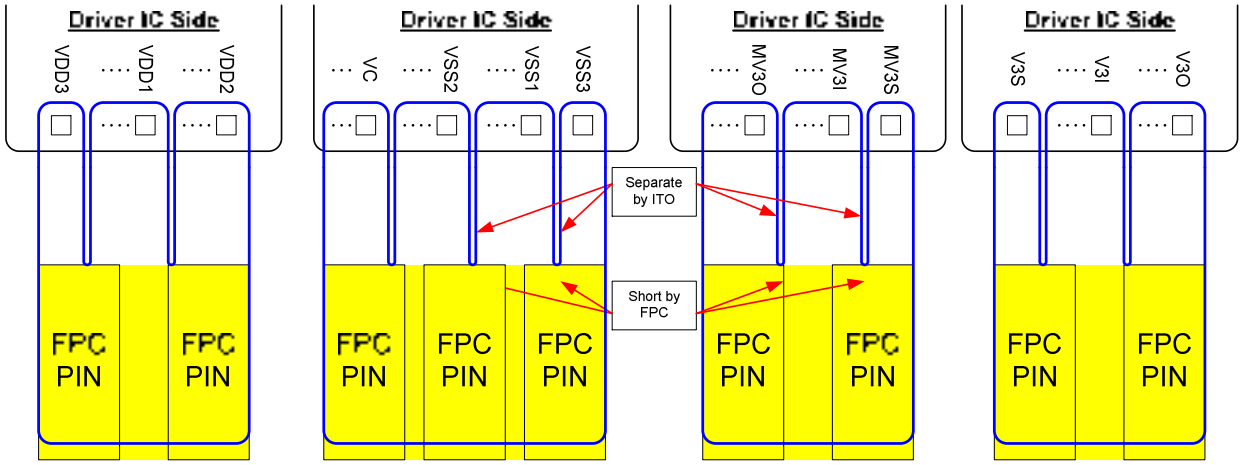
Recommend ITO Resistance (for COG applications)

Pin Name	ITO Resistance
Vref, TP[2:0], TCAP, Reserved Pins	Floating
VDD1, VDD2, VDD3, VDI, VSS1, VSS2, VSS3, VPP, VC, NVDD	< 100Ω
CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, V3, V1, MV1, MV3	< 300Ω
A0, RWR, ERD, CS1B, CS2, D[7:0]	< 1KΩ
SYNC, DOFB, EXTB, CL	< 3KΩ
M/S, IF[2:1], CLS, TP3, RSTB *	< 5KΩ

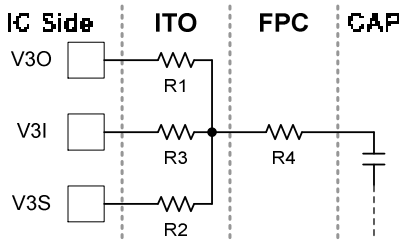
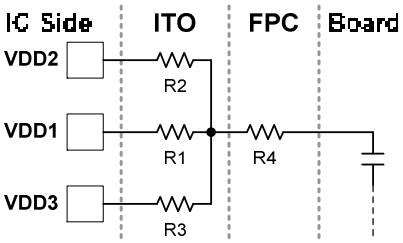
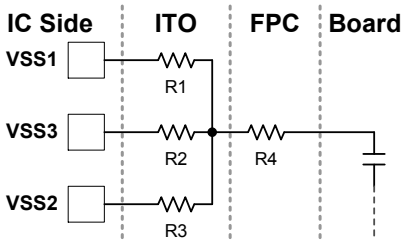
Note: It is recommended to keep the resistance of RSTB pin larger than 2KΩ(and less than 5KΩ).

ITO Layout Notes:

1. The Limitations include the bottleneck of ITO layout.
2. Make sure that the ITO resistance of COM0 ~ COM83 is equal, and so is it of SEG0 ~ SEG159.
3. To avoid the noise in different power systems affect other power system, please separate them on ITO layout.
4. The V3 and MV3 power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.



5. Exception condition: if ITO resistance is too large, traces should be connected by ITO to reduce the resistance (refer to the equivalent circuit below).

V3 & MV3	*VDD*	*VSS*
		
Ideal Layout: (short at FPC)	**Ideal Layout: (short at FPC)**	**Ideal Layout: (short at FPC)**
=> R4=0 Ohm. R2>>R1>R3.	=> R4=0 Ohm. R3>>R1>R2.	=> R4=0 Ohm. R2>>R1>R3.
Acceptable Layout: (short at ITO end)	**Acceptable Layout: (short at ITO end)**	**Acceptable Layout: (short at ITO end)**
=> R4≠0. R2>>R1>R3>R4.	=> R4≠0. R3>>R1>R2>R4.	=> R4≠0. R2>>R1>R3>R4.
Not Recommend: (no ITO separation)	**Not Recommend: (no ITO separation)**	**Not Recommend: (no ITO separation)**
=> R4 ≥ (R1 or R2 or R3).	=> R4 ≥ (R1 or R2 or R3).	=> R4 ≥ (R1 or R2 or R3).

6. FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

ST7580A has 2 chip select pins: CS1B (“Low” Active) & CS2 (“High” Active). When both of them are acted (CS1B=“L” & CS2=“H”), ST7580A is selected and the MPU interface is enabled. When this IC is NOT selected (CS1B=“H” or CS2=“L”), the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance.

Interface Selection

ST7580A has 3 types of interface with an MPU. This interface selection is shown in Table 1.

Table 1. Parallel/Serial Interface Mode

IF2	IF1	CS1B	CS2	A0	ERD	RWR	D[7:0]	MPU Interface
“H”	“H”	CS1B	CS2	A0	E	R/W	D[7:0]	6800-series parallel interface
“H”	“L”				/RD	/WR		8080-series parallel interface
“L”	“H”				---	---	Refer to serial interface.	4-Line SPI interface

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Parallel Interface

When IF2= “H”, the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by “IF1” pin as shown in Table 2. The data transfer type in parallel interface is determined by signals on A0, ERD and RWR as shown in Table 3.

Table 2. Microprocessor Selection for Parallel Interface

IF2	IF1	CS1B	CS2	A0	ERD	RWR	D[7:0]	MPU Interface
“H”	“H”	CS1B	CS2	A0	E	R/W	D[7:0]	6800-series parallel interface
“H”	“L”				/RD	/WR		8080-series parallel interface

Table 3. Parallel Data Transfer Type

Common Pins			6800-Series		8080-Series		Description
CS1B	CS2	A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
“L”	“H”	“H”	“H”	“H”	“L”	“H”	Display data read out
		“H”	“H”	“L”	“H”	“L”	Display data write
		“L”	“H”	“H”	“L”	“H”	Internal status read
		“L”	“H”	“L”	“H”	“L”	Writes to internal register (instruction)

Setting Serial Interface

Serial Mode	IF2	IF1	CS1B	CS2	A0	ERD	RWR	D7	D6	D[5:0]
4-Line SPI interface	“L”	“H”	CS1B	CS2	A0	---	---	SDA	SCL	---

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Note:

1. The option setting to be “H” should connect to VDD1, and the option setting to be “L” should connect to VSS1.
2. Some MPU will set interface pins to be Hi-Z (high impedance) mode during power-save mode or after hardware reset. This is not allowed when the VDD1of ST7580A is turned ON. Because the floating input (especially for those control pins such as CS1B, CS2, RSTB, RWR or ERD…) maybe cause abnormal latch and cause abnormal display.

4-Line SPI interface (IF[2:1]="L,H")

When ST7580A is selected (CS1B="L" & CS2="H"), serial data (SDA) and serial clock (SCL) inputs are enabled. When ST7580A is not selected (CS1B="H" or CS2="L"), the internal 8-bit shift register and 3-bit serial counter are reset (the MPU interface is disabled as well). Serial data on SDA is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the received 8-bit parallel data is display data or instruction. A0="H" indicates the received 8-bit parallel data is display data, while A0="L" indicates it is instruction. The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected data/instruction latch.

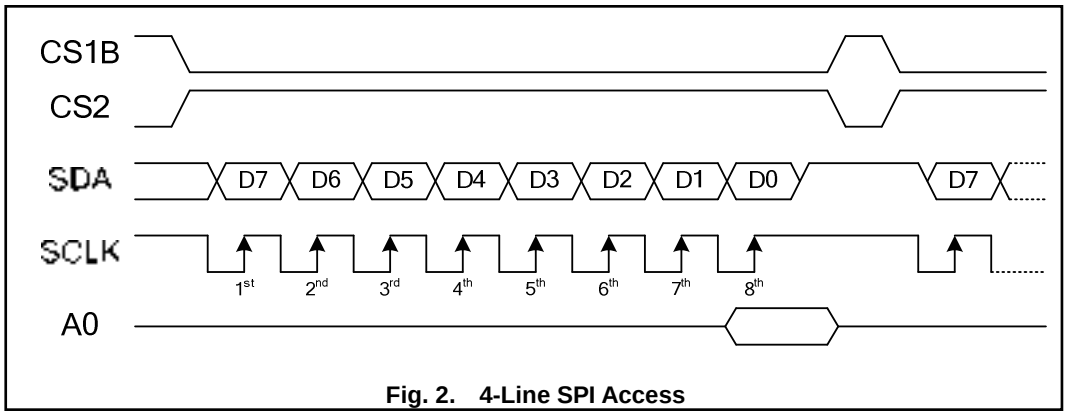


Fig. 2. 4-Line SPI Access

Data Transfer

ST7580A uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig. 3. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig. 4. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

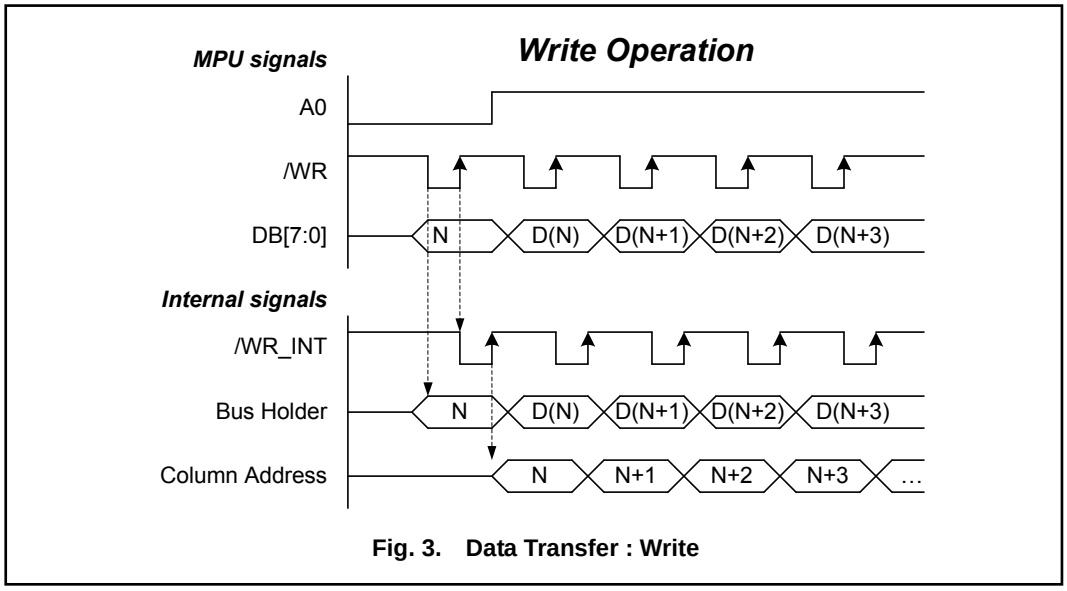


Fig. 3. Data Transfer : Write

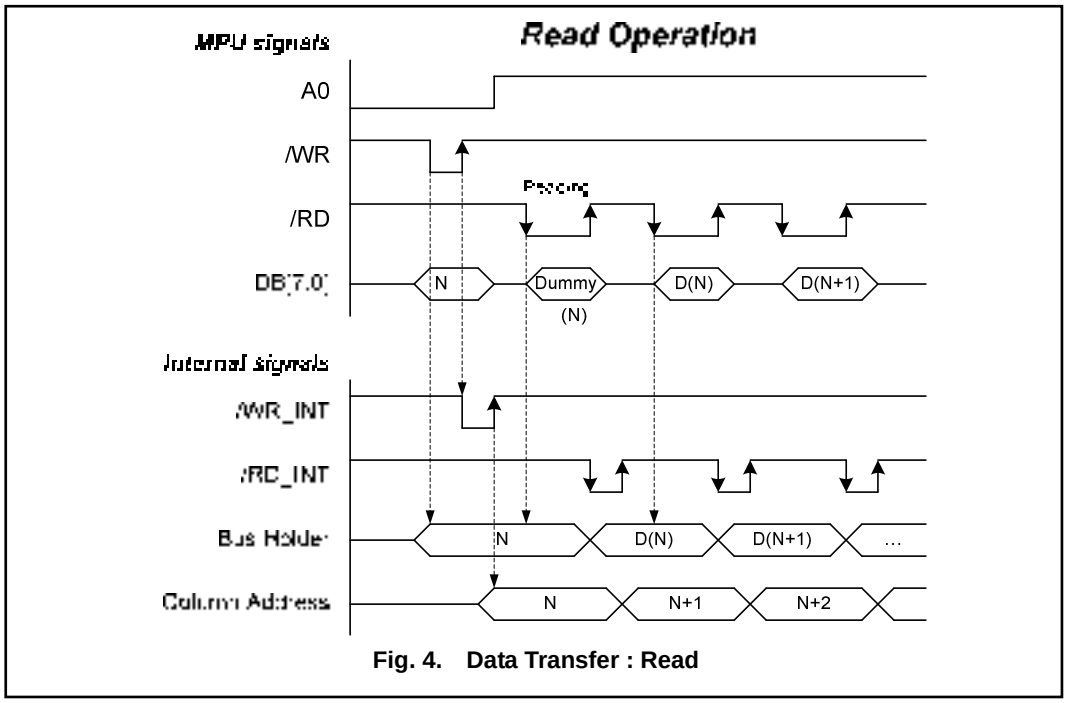


Fig. 4. Data Transfer : Read

Display Data RAM (DDRAM)

When the data bit in DDRAM is “1”, the segment driver will output ON voltage. If it is “0”, the segment driver will output OFF voltage. The DDRAM data bits (D[7:0]) corresponds to the common-line direction of LCD with D0 on the top (refer to the figure below).

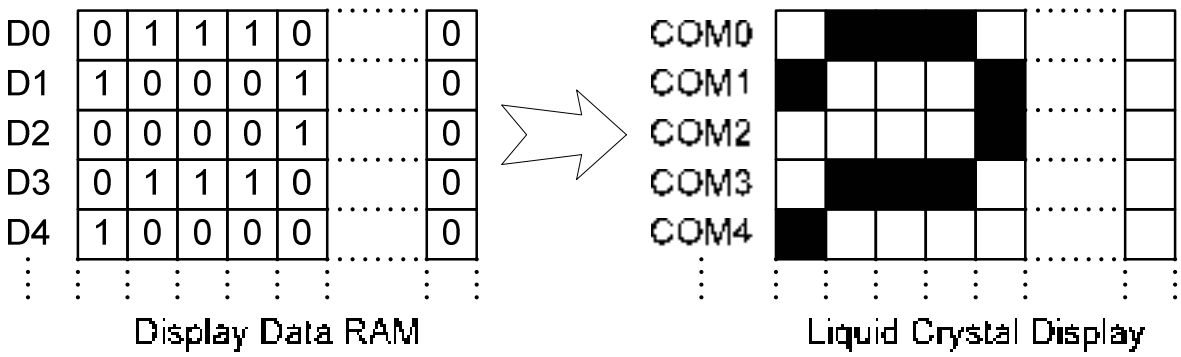


Fig. 5. DDRAM Mapping Mode (Default Setting)

DDRAM is an addressable array with 160 columns by 84 rows (10-page with 8-bit and 1-page with 4-bit only). The column address is related to the column output number directly. Each pixel can be selected when the page and column addresses are specified (refer to Fig. 5 for detailed illustration). The rows are divided into: 10 pages (Page-0 ~ Page-9) with 8 lines per page (COM0~79) and 1 page (Page-10) with 4 lines (COM81~83). As shown in Fig. 6, COM 0~79 (in Page 0~9) can be accessed through D[0:7] directly while COM80~83 (in Page-10) can be accessed through D[0:3].

Fig. 6. DDRAM Format

Display Data Latch Circuit

The display data larch circuit is a latch which temporarily holds the display data output from DDRAM and then transfer the latched data to the liquid crystal drive circuits. By controlling the contents in this latch, the display functions (such as Display ON/OFF, Inverse Display ON/OFF and All Pixels ON/OFF) can be achieved without changing the data in DDRAM.

Addressing

Data is downloaded into the Display Data RAM matrix in ST7580A as byte-format. The Display Data RAM has a matrix of 160 x 84 bits. The address ranges are: X=0~159 (column address), Y=0~10 (page address). Addresses outside these ranges are not allowed.

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Set Page Address” instruction. The Page Address must be set before accessing DDRAM content.

Column Address Circuit

The column address of DDRAM can be specified by “Set Column Address” instruction. The column address is increased by 1 automatically after each byte of DDRAM data access (read/write). This feature allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “9Fh”) because the address out of range is invalid. That means: both Page Address and Column Address should be assigned again if user wants to change the address pointers from the end of Page-0 to the beginning of Page-1 (from Page-0, Column-9Fh to Page-1, Column-0h).

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG) pads. It is necessary to rewrite the display data into DDRAM after changing MX setting.

The relation between DDRAM and outputs with different MX or MY setting is shown below.

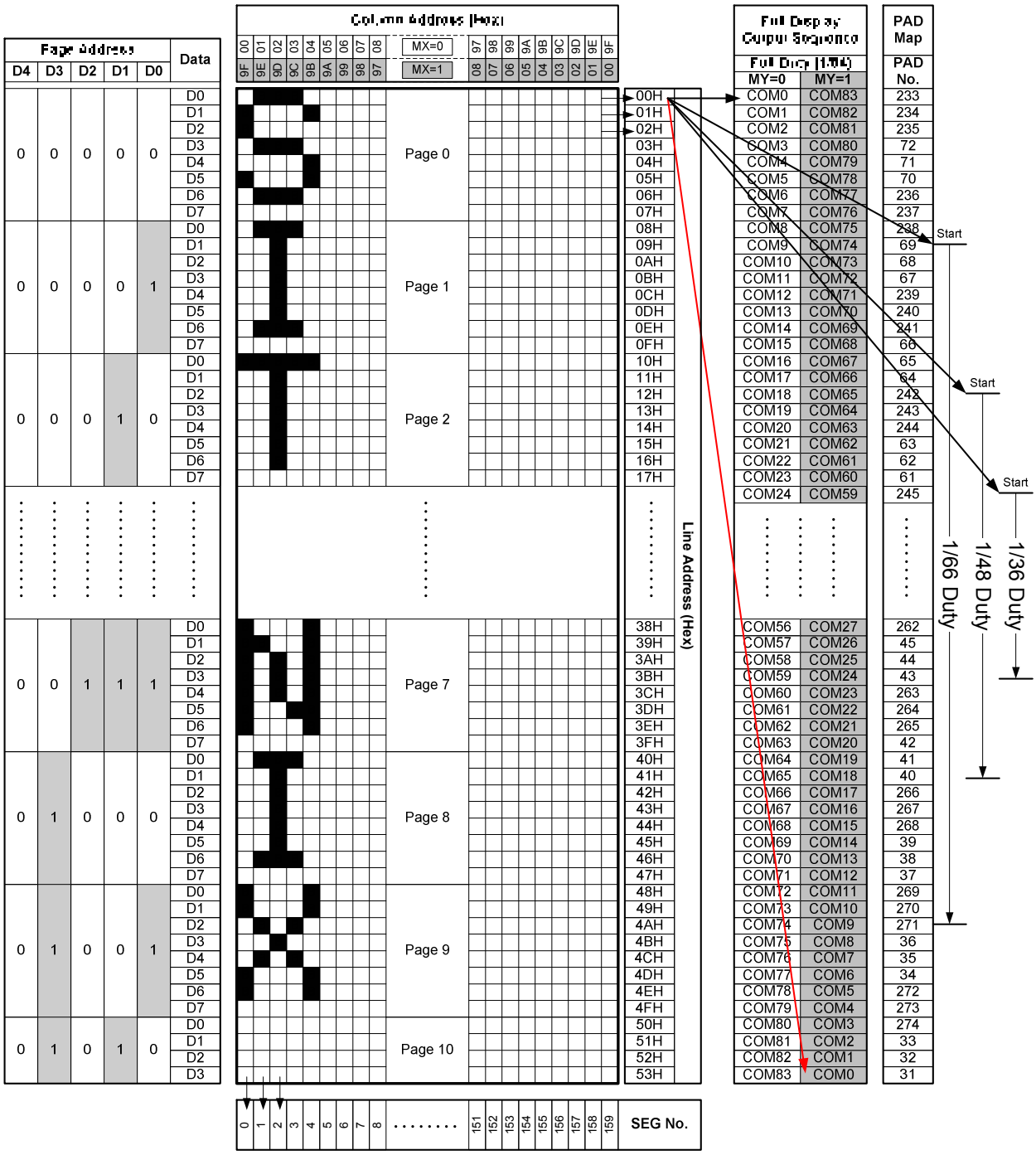


Fig. 7. DDRAM and Output Map (COM/SEG)

* Please refer to appendix for DDRAM mapping example.

Oscillation Circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, connect CLS to VDD1; when the external oscillator is used, connect CLS to VSS1 and input external clock to CL pin. This oscillator signal is used by the voltage booster and display timing generation circuit.

Power System

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external components. The built-in power system has negative-power generator, voltage booster, voltage regulator and voltage follower circuits. Before turning power OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

External Components of Power Circuit

The external power components are shown below. The optimized value depends on the panel size and loading.

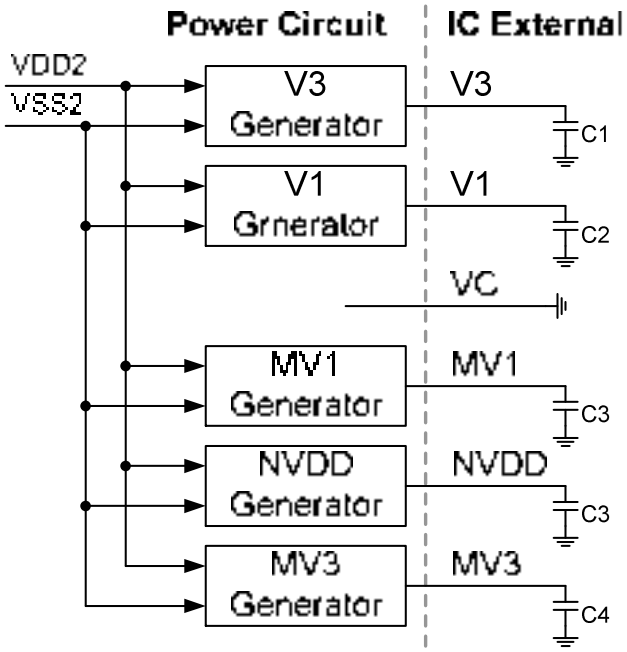


Fig. 8. LCD Power Circuit

Regulator Circuit

The built-in high accuracy regulator is used for Vop voltage adjustment. The detailed information for Vop setting is in “Set Vop” (Page 29) of Section 9. INSTRUCTION DESCRIPTION. With the help of the built-in temperature sensor, its temperature compensation can be customized. The output voltage can also be changed by instructions such as “Set Vop”, “Set Vop TC-Curve”, “Set TC Flag” and “Set FR TC Hysteresis”…

Power Application

Application Condition	Power Control Setting	Note
Use internal power circuits	(VN,VB,VR,VF)=(1,1,1,1)	NVDD, V3, V1, MV1 & MV3 are generated by IC.
Use external regulator	(VN,VB,VR,VF)=(1,0,1,1)	Apply external power to V3. NVDD, V1, MV1 & MV3 are generated by IC.
Use external V3, V1, MV3 & MV1	(VN,VB,VR,VF)=(1,0,0,0)	Apply external power to V3, V1, MV3 & MV1

7. RESET CIRCUIT

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s recommended to initialize the whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. After the power is stable, a hardware reset is required to initialize internal registers.

Setting RSTB to “L” will start the internal initial procedure. The control registers will return to their default value:
Page Address: 0
Column Address: 0
Display ON/OFF: OFF
Inverse Display ON/OFF: OFF (normal)
All Pixels ON: Normal
Power Control: All OFF (VN=0, VB=0, VR=0, VF=0)
Booster Control: BL = (2xVDD2) x 2
TC Control: OFF
TC Sensor Speed: Normal
Contrast Level: 00h
Bias Select: 1/3 bias
COM Scan Direction: 0 (normal)
SEG Scan Direction: 0 (normal)
Oscillator: OFF
Standby Mode: Exit (released)
Discharge ON/OFF: OFF
Read-modify-Write mode: Exit
ML Drive Mode: Normal
Test Mode: Exit (TE=0, T[1:0]=0)

The software reset function is also available in ST7580A. It is different from the hardware reset. When SRESET instruction is issued, the following procedure is occurred.
Page address: 0
Column address: 0
Contrast Level: 00h
Read-modify-Write mode: Exit
Test Mode: Exit (TE=0, T[1:0]=0)

8. INSTRUCTION TABLE

Basic Instruction (TE=0, T[1:0]= don't care)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Read Data	1	1	Data Read								Read display data from DDRAM
Write Data	1	0	Data Write								Write display data to DDRAM
Read Status	0	1	BSY	MX	D	RST	0	0	0	0	Read IC Status
Set Page Address	0	0	0	1	1	1	1	1	0	0	Set page address
	0	0	-	-	-	Y4	Y3	Y2	Y1	Y0	
Set X Address (LSB)	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
Set X Address (MSB)	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse; MX=0, normal
OSC ON	0	0	0	1	0	0	1	1	1	0	Set internal oscillator ON
	0	0	0	0	0	0	0	0	0	0	
	0	0	1	0	1	0	1	0	1	1	
Display ON/OFF	0	0	1	0	1	0	0	0	1	D	D=1, display ON D=0, display OFF
All Pixels ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixels ON AP=0, normal display
Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
Set Display Part	0	0	1	1	0	1	1	1	0	0	Set Display Part and COM output direction. Please refer to instruction description for detailed information. Full (1/84 Duty): MY=0: DP2,DP1,DP0=54h, D3h, 00h MY=1: DP2,DP1,DP0=54h, D3h, 30h
			DP27	DP26	DP25	DP24	DP23	DP22	DP21	DP20	
			DP17	DP16	DP15	DP14	DP13	DP12	DP11	DP10	
			DP07	DP06	DP05	DP04	DP03	DP02	DP01	DP00	
			1	1	0	0	MY	0	0	0	
Power Control	0	0	1	0	0	1	VN	VB	VR	VF	Set built-in power blocks ON/OFF
Discharge ON/OFF	0	0	0	0	1	1	0	1	1	Disv	Discharge Power supply circuit
Set Booster	0	0	0	1	1	0	0	1	BL1	BL0	Set booster level
Set Vop	0	0	1	0	0	0	0	0	0	1	Double command!! Set V3/MV3 level
	0	0	V7	V6	V5	V4	V3	V2	V1	V0	
Bias Select	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Standby ON/OFF	0	0	0	1	0	1	1	0	0	PSD	Enable standby mode
SRESET	0	0	1	1	1	0	0	0	0	1	Software reset
	0	0	1	1	0	1	0	0	0	0	
	0	0	0	0	0	0	0	0	0	0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Frame Rate 1	0	0	0	0	1	1	0	0	0	0	Frame frequency in Temp range A & B
	0	0	FB[3:0]				FA[3:0]				
Set Frame Rate 2	0	0	0	0	1	1	0	0	0	1	Frame frequency in Temp range C & D
	0	0	FD[3:0]				FC[3:0]				
Test	0	0	1	1	1	1	1	T1	T0	TE	T[1:0]: test mode. TE=0, exit test mode; TE=1, enter test mode.
ML Drive Mode	0	0	1	1	1	1	1	1	0	1	Select ML drive mode MLM=0, enhanced mode MLM=1, normal mode
	0	0	0	1	1	1	0	0	0	1	
	0	0	0	1	1	MLM	1	0	0	1	
	0	0	1	1	1	1	1	0	0	0	
TC Sensor Speed	0	0	1	1	1	1	1	1	0	1	Speed up internal thermal sensor F0=1 => Fast Speed F0=0 => Normal Speed
	0	0	0	1	1	1	0	0	0	0	
	0	0	0	0	1	0	F0	0	0	1	
	0	0	1	1	1	1	1	0	0	0	

Extended Instruction 1 (TE=1 & T[1:0]=0,0)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
TC Control	0	0	0	1	1	0	1	0	0	TC	Set temperature compensation function, TC=1: ON; TC=0: OFF
Set TC Curve 01	0	0	0	0	1	1	0	0	0	0	Set TC curves for: T0 (-40 ~ -32℃) & T1 (-32 ~ -24℃)
			MT1[3:0]				MT0[3:0]				
Set TC Curve 23	0	0	0	0	1	1	0	0	0	1	Set TC curves for: T2 (-24 ~ -16℃) & T3 (-16 ~ - 8℃)
			MT3[3:0]				MT2[3:0]				
Set TC Curve 45	0	0	0	0	1	1	0	0	1	0	Set TC curves for: T4 (-8 ~ 0℃) & T5 (0 ~ 8℃)
			MT5[3:0]				MT4[3:0]				
Set TC Curve 67	0	0	0	0	1	1	0	0	1	1	Set TC curves for: T6 (8 ~ 16℃) & T7 (16 ~ 24℃)
			MT7[3:0]				MT6[3:0]				
Set TC Curve 89	0	0	0	0	1	1	0	1	0	0	Set TC curves for: T8 (24 ~ 32℃) & T9 (32 ~ 40℃)
			MT9[3:0]				MT8[3:0]				
Set TC Curve AB	0	0	0	0	1	1	0	1	0	1	Set TC curves for: TA (40 ~ 48℃) & TB (48 ~ 56℃)
			MTB[3:0]				MTA[3:0]				
Set TC Curve CD	0	0	0	0	1	1	0	1	1	0	Set TC curves for: TC (56 ~ 64℃) & TD (64 ~ 72℃)
			MTD[3:0]				MTC[3:0]				
Set TC Curve EF	0	0	0	0	1	1	0	1	1	1	Set TC curves for: TE (72 ~ 80℃) & TF (80 ~ 88℃)
			MTF[3:0]				MTE[3:0]				
Set TC Flag	0	0	0	0	1	1	1	1	1	0	Set TC flag for MT7~0
			FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
			0	0	1	1	1	1	1	1	Set TC flag for MTF~8
			FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
TMPARNG	0	0	1	0	1	0	0	0	0	0	Temp range A
	0	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
TMPBRNG	0	0	1	0	1	0	0	0	0	1	Temp range B
	0	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
TMPCRNG	0	0	1	0	1	0	0	0	1	0	Temp range C
	0	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
Set FR TC Hysteresis	0	0	1	1	0	0	1	1	0	0	Set TC hysteresis for frame frequency
			0	0	0	0	THF3	THF2	THF1	THF0	
Set Vop TC Hysteresis	0	0	1	1	0	0	1	1	1	0	Set TC hysteresis for V3/MV3
			0	0	THV5	THV4	THV3	THV2	THV1	THV0	

Extended Instruction 2 (TE=1 & T[1:0]=0,1)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
EPCTIN	0	0	1	0	0	1	0	0	0	1	Control PROM WR/RD EWR=1: PROM write mode EWR=0: PROM read mode
	0	0	0	0	EWR	0	0	0	0	0	
EPCTOUT	0	0	1	0	0	1	0	0	1	0	Exit PROM control mode
EPMWR	0	0	1	0	0	1	0	0	1	1	Write to PROM
EPMRD	0	0	1	0	0	1	0	1	0	0	Read from PROM
AutoLoadSet	0	0	1	0	0	1	0	1	1	0	PROM data auto re-load control
	0	0	0	0	0	ARD	0	0	0	0	
Vop Up	0	0	1	1	0	1	1	1	1	0	Increase V3/MV3 by 1 step
Vop Down	0	0	1	1	0	1	1	1	1	1	Decrease V3/MV3 by 1 step

Note:
1. Symbol “-” means this bit can be “H” or “L”.
2. Please don’t use instructions which are not defined in this specification.

9. INSTRUCTION DESCRIPTION

Basic Instruction (T[1:0]=Don't Care & TE=0)

Read Data

8-bit data of the Display Data RAM specified by the column address and page address can be read to the microprocessor by this instruction. The column address will be increased by 1 automatically after each byte of data read (till the end of a page). With this feature, the MPU can continuously read data from the addressed page. A dummy read is required after specifying the page and column address. The read function is not available in serial interface mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Data Read							

Write Data

8-bit display data from the microprocessor can be written into the Display Data RAM at the location specified by the column and page address. The column address will be increased by 1 automatically after each byte of data write (till the end of a page). With this feature, the MPU can continuously write data to the addressed page.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Data Write							

Read Status

Read the internal status of ST7580A. The read function is not available in serial interface mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BSY	MX	D	RST	0	0	0	0

Flag	Description
BSY	BSY=0: Ready (ST7580A always returns 0 after hardware reset is finished) BSY=1: Busy
MX	MX=0: Normal direction (SEG0->SEG159) MX=1: Reverse direction (SEG159->SEG0)
D	D=0: Display ON (it's the inverse value of control register) D=1: Display OFF (it's the inverse value of control register)
RST	RST=1: During reset (hardware or software reset) RST=0: Normal operation

Set Page Address

This is double-byte instruction. Y[4:0] specifies the page address of the built-in DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	1	0	0
0	0	-	-	-	Y4	Y3	Y2	Y1	Y0

Y4	Y3	Y2	Y1	Y0	Page Address	Valid Bit
0	0	0	0	0	Page0	D0 ~ D7
0	0	0	0	1	Page1	D0 ~ D7
:	:	:	:	:	:	:
0	1	0	0	1	Page9	D0 ~ D7
0	1	0	1	0	Page10	D0 ~ D3

Set X Address

The range of column address is 0…159. The address parameter is separated into 2 instructions. The column address will be increased by 1 after each byte of display data access (read/write). This auto-increment feature stops at the end of each page (Column Address “9Fh”). This feature allows MPU accessing DDRAM content continuously in the addressed page.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4
0	0	0	0	0	0	X3	X2	X1	X0

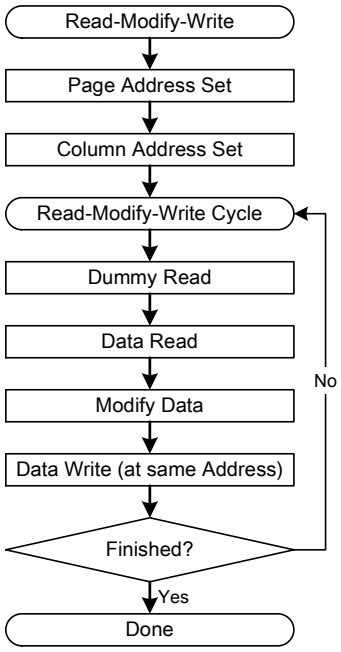
X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1	157
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

Read-modify-Write

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

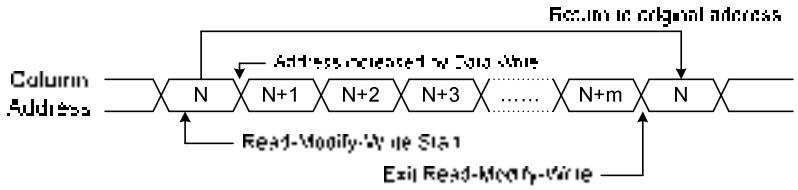
* Other instructions aside from data read/write can also be used in this mode.



END

This instruction releases the Read-modify-Write mode, and the column address returns to the address it was when the Read-modify-Write instruction was entered.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0



SEG Direction

This instruction changes the DDRAM addressing mode which let the data write to DDRAM in the opposite direction. After changing the MX setting and re-writing the display data into DDRAM again, the display will be mirrored horizontally.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: Normal direction (SEG0->SEG159) MX=1: Reverse direction (SEG159->SEG0)

Note: It is necessary to write the display data again after the MX setting is altered.

Oscillator ON

This instruction controls the built-in oscillator circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	1	0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	1	1

Display ON/OFF

This instruction selects the display mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	D

Flag	Description
D	D=1: Normal Display Mode. D=0: Display OFF. All SEGs/COMs output at VC level.

All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP=0: Normal display AP=1: All pixels ON

Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (white -> Black, Black -> White) while the display data in the Display Data RAM is never changed.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV=1: Inverse display

Set Display Part

This compounded instruction selects the display part of entire display area.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	1	0	0
		DP27	DP26	DP25	DP24	DP23	DP22	DP21	DP20
		DP17	DP16	DP15	DP14	DP13	DP12	DP11	DP10
		DP07	DP06	DP05	DP04	DP03	DP02	DP01	DP00
		1	1	0	0	MY	0	0	0

Display Duty	Instruction	DP2[7:0]	DP1[7:0]	DP0[7:0]	MY	Display Part (Pad name in 1/84 Duty)
1/84	DCh	54h	D3h	00h	MY=0 (C0h)	COM0~83 (Full)
				30h	MY=1 (C8h)	COM83~0 (Full)
1/66		42h		09h	MY=0 (C0h)	COM9~74
				39h	MY=1 (C8h)	COM74~9
1/48		30h		12h	MY=0 (C0h)	COM18~65
				42h	MY=1 (C8h)	COM65~18
1/36		24h		18h	MY=0 (C0h)	COM24~59
				48h	MY=1 (C8h)	COM59~24

For example,

1. 1/48 Duty display with MY=0: Set “DCh, 30h, D3h, 12h & C0h”
2. 1/48 Duty display with MY=1: Set “DCh, 30h, D3h, 42h & C8h”

Power Control

This instruction controls the built-in power circuits. Refer to the “Power System” section for the application notes.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	VN	VB	VR	VF

Flag	Description
VN	VN=0: NVDD Generator OFF VN=1: NVDD Generator ON
VB	VB=0: V3 Generator OFF VB=1: V3 Generator ON
VR	VR=0: MV3 Generator OFF VR=1: MV3 Generator ON
VF	VF=0: V1 Generator OFF VF=1: V1 Generator ON

Discharge ON/OFF

This command is used to discharge the capacitors connected to the power supply circuits. This command becomes necessary when: **Turning OFF the system power supply (VDD-VSS)**.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	1	Disv

Flag	Description
Disv	Disv=0: Disable Discharge Disv=1: Enable Discharge

Note: To prevent large current, do NOT discharge before the related power supplies (internal/external) are OFF.

Set Booster

This instruction controls the built-in booster circuit to provide the power source of the built-in regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1	BL1	BL0

Flag	Description
BL[1:0]	BL1 / BL0 / Booster Level 0 / 0 / Booster Level = (2xVDD2) x 2 0 / 1 / Booster Level = (2xVDD2) x 3 1 / 0 / Booster Level = (2xVDD2) x 4 1 / 1 / Reserved

Set Vop

This is double-byte instruction. This instruction controls the Vop output voltage which is generated by the built-in V3/MV3 generators. Customers select the target V3 voltage and set the contrast by this instruction. The MV3 will be generated by the built-in MV3 generator automatically.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	V7	V6	V5	V4	V3	V2	V1	V0

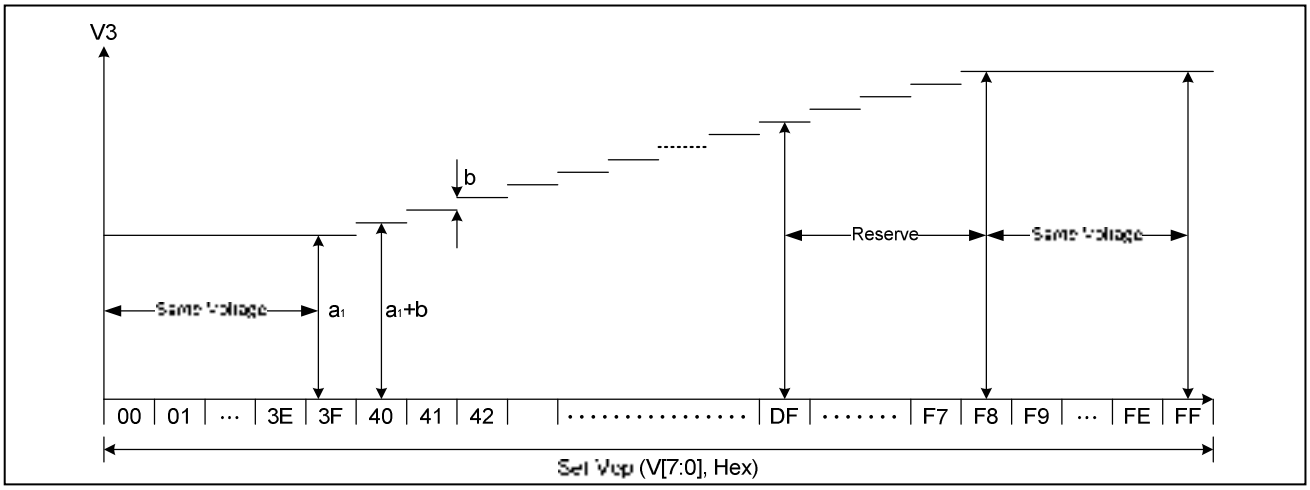
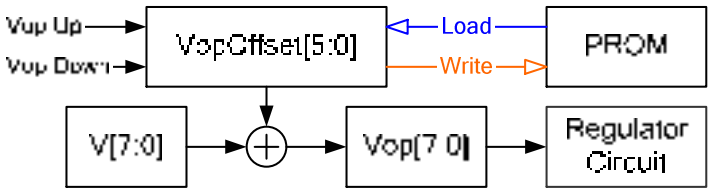


Fig. 9. Setting V3 Voltage

An internal PROM can be used to adjust Vop to get the best display performance on LCD module. The default offset is 0.



The operation voltage (Vop) calculation formula is shown below:

Vop = V3 – MV3… Since V3 = |MV3| => Vop = 2*V3

V3 = a1 + b x (V[7:0] + VopOffset[5:0] – 64)

…… (where the valid V[7:0] is 40h~DFh)

Symbol	Value	Unit
a1	2.64	V
b	0.04	V

Note:

1. The maximum voltage that can be generated depends on VDD2 and the loading of LCD module. The first 64 values (00h~3Fh) and the last 8 steps (F8h~FFh) generate the same voltage. DFh~F7h (25 steps) are reserved for test.
2. It is not recommended to set Vop over 9V. Besides, it is recommended to reserve some range for Vop adjustment or temperature compensation. Therefore, for example, if we reserved 0.2V for customer to adjust contrast, 0.32V for TC function and 0.08V to fine tune Vop voltage… We reserved 10-step (5+8+2) and the V[7:0] should be less than “D1h”.
3. If VDD2≥3.8V, the minimal V3 will be higher than 2.64V (an internal pre-charge diode connects from VDD2 to V3).
4. Please note that: VopOffset[5:0] is 2’s complement, so that VopOffset[5:0] can increase or decrease Vop. If customer adjusts Vop by too many “Vop Up” (or “Vop Down”) instructions, the purpose to increase Vop (or decrease Vop) will become: “lower Vop” (or “higher Vop”).
5. A software overflow prevention procedure should be used when using “Vop Up”/“Vop Down”. So that the overflow problem can be prevented.

Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	B2	B1	B0

Bias Selection			
B2	B1	B0	Bias
0	0	0	1/3
0	0	1	
0	1	0	1/4
0	1	1	1/5
1	0	0	1/6
1	0	1	1/7
1	1	0	Reserved
1	1	1	

LCD driving voltage relation:

Symbol	Bias Setting				
	1/3	1/4	1/5	1/6	1/7
V3	V3	V3	V3	V3	V3
V1	V3/3	V3/4	V3/5	V3/6	V3/7
VC	0	0	0	0	0
MV1	-V3/3	-V3/4	-V3/5	-V3/6	-V3/7
MV3	-V3	-V3	-V3	-V3	-V3

- V1 range: 1.0V ≤ V1 < 2.3V
- Optimized Bias = 2 / [(Duty * 4/3) 1/2]

Standby ON/OFF

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	0	0	PSD

When PSD=1, internal Standby procedure starts. The procedure of the Standby Mode is shown below:
(all display data is still kept in DDRAM)

- Stops the LCD driving circuits and keeps the common and segment outputs at VC.
- Stops internal oscillation circuit;
- The display data and register settings are still kept, except D-Flag and AP-Flag (they are masked temporarily).

SRESET

This instruction resets some registers to their default (refer to the “Section 7. RESET CIRCUIT” for detailed information). Please note this instruction (software reset) is not same as the hardware reset (RSTB=L). For example, the built-in power circuit is initialized by the hardware reset (RSTB=L) but cannot be initialized by this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0

NOP

“No Operation” instruction. ST7580A will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

Set Frame Rate 1 & 2

These commands set the display frame frequency for each temperature area.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	0
0	0	FB[3:0]				FA[3:0]			

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1
0	0	FD[3:0]				FC[3:0]			

Parameter	Description
FA[3:0]	Set frame frequency in temperature range -40℃ to TA.
FB[3:0]	Set frame frequency in temperature range TA to TB.
FC[3:0]	Set frame frequency in temperature range TB to TC.
FD[3:0]	Set frame frequency in temperature range TC to 88℃.

Note:

1. TA, TB & TC are defined by Extended Instructions: TMPARNG, TMPBRNG & TMPCRNG.
2. By setting all temperature ranges with the same parameter, the temperature compensation for frequency is disabled.

The clock system related symbol is defined as below:

Symbol	Description
fOSC	Oscillation frequency of the built-in oscillation circuit.
fCL	Internal operation clock. It is the basic clock used by the synchronous circuit of IC. This clock is obtained by dividing fOSC.
fOCL	It is the external clock provided from CL pin externally when the built-in oscillation circuit is turned OFF. In this case, internal oscillation clock (fOSC) is the same as external operation clock (fOCL). Please set external clock close to 1630KHz.
fDCLK	Display operation clock. It is used to specify a single duration in the sequential drive of liquid crystal. It constantly meets the relation of fCL/15 independent of the value of the operation clock frequency select command. The relationship will not change even when the external clock is used.

When the built-in oscillation circuit is turned OFF, the external clock applied on CL pin (fOCL) is used as the internal oscillation clock (fOSC). In this case, the fOCL uses the same dividing ratio as the internal oscillation clock. The accuracy and the temperature effect should be considered by customer.

The following tables show the relation between the control register and the frequency of the clock outputs.

FR[3:0] FA[3:0], FB[3:0], FC[3:0], FD[3:0]	fCL (kHz)	fDCLK (kHz)	Frame frequency fFR (Hz)		fCL (kHz)	fDCLK (kHz)	Frame frequency fFR (Hz)	
			1/84 Duty	1/66 Duty			1/48 Duty	1/36 Duty
0 0 0 0	408	27.2	234	295	116	7.8	114	149
0 0 0 1	326	21.7	187	236	102	6.8	100	131
0 0 1 0	272	18.1	156	197	91	6.0	89	116
0 0 1 1	233	15.5	134	169	82	5.4	80	104
0 1 0 0	204	13.6	117	148	78	5.2	76	100
0 1 0 1	181	12.1	104	131	68	4.5	67	87
0 1 1 0	163	10.9	94	118	65	4.3	64	84
0 1 1 1	136	9.1	78	98	58	3.9	57	75
1 0 0 0	116	7.8	67	84	51	3.4	50	65
1 0 0 1	109	7.2	62	79	45	3.0	44	58
1 0 1 0	102	6.8	59	74	34	2.3	33	44
1 0 1 1	91	6.0	52	66	29	1.9	29	37
1 1 0 0	82	5.4	47	59	27	1.8	27	35
1 1 0 1	78	5.2	45	56	20	1.4	20	26
1 1 1 0	68	4.5	39	49	18	1.2	18	23
1 1 1 1	65	4.3	37	47	15	1.0	15	19

Note:

1. The default clock speed is: fOSC=1630KHz (internal clock) or fOCL=1630KHz (external clock).
2. For customers use different clock speed, the new frame frequency will be: $\boldsymbol{fFR_{NEW} = (fOCL_{NEW} / 1630KHz) * fFR}$.
3. Please refer to “External Clock Timing” for the external clock specification.

Test

The test mode is reserved for IC testing and IC calibration. The temperature compensation related instructions are in Test Mode 0. Always remember to exit test mode by setting TE=0. If the test mode is enabled accidentally, it can be cleared by: setting TE=0, issuing an “L” pulse on RSTB pin or issuing SRESET instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	T1	T0	TE

Flag	Description

T1	T0	TE	Description
-	-	0	Normal operation (TE=0, T[1:0] are ignored)
0	0	1	Extended Instruction 1 (Thermal related)
0	1	1	Extended Instruction 2 (PROM related)
1	0	1	Reserved for IC testing only.
1	1	1	Do NOT use!!

T[1:0]
TE

ML Drive Mode

Sets the ML drive method

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	0	0	0	1
0	0	0	1	1	MLM	1	0	0	1
0	0	1	1	1	1	1	0	0	0

Flag	Description
MLM	MLM=1: Default ML driving mode (default). MLM=0: Enhanced ML driving mode (recommend).

TC Sensor Speed

Use this compounded instruction to speed up the temperature sensor circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	0	0	0	0
0	0	0	0	1	0	F0	0	0	1
0	0	1	1	1	1	1	0	0	0

Flag	Description
F0	F0=0: Normal speed. F0=1: Fast speed.

Extended Instruction 1 (T[1:0]=(0,0) & TE=1)

TC Control

This instruction controls the temperature compensation function ON/OFF.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	1	0	0	TC

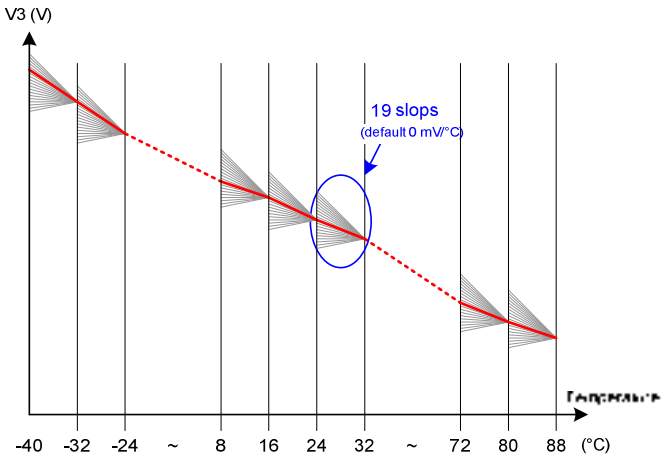
Flag	Description

TC	Temperature Compensation
0	OFF
1	ON

Set Vop TC-Curves

These instructions set the V3/MV3 temperature compensation (TC) gradient in each temperature range.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	0	0	0	MT0[3:0] : -40 ~ -32℃
0	0	MT1[3:0]				MT0[3:0]				MT1[3:0] : -32 ~ -24℃
0	0	0	0	1	1	0	0	0	1	MT2[3:0] : -24 ~ -16℃
0	0	MT3[3:0]				MT2[3:0]				MT3[3:0] : -16 ~ - 8℃
0	0	0	0	1	1	0	0	1	0	MT4[3:0] : -8 ~ 0℃
0	0	MT5[3:0]				MT4[3:0]				MT5[3:0] : 0 ~ 8℃
0	0	0	0	1	1	0	0	1	1	MT6[3:0] : 8 ~ 16℃
0	0	MT7[3:0]				MT6[3:0]				MT7[3:0] : 16 ~ 24℃
0	0	0	0	1	1	0	1	0	0	MT8[3:0] : 24 ~ 32℃
0	0	MT9[3:0]				MT8[3:0]				MT9[3:0] : 32 ~ 40℃
0	0	0	0	1	1	0	1	0	1	MTA[3:0] : 40 ~ 48℃
0	0	MTB[3:0]				MTA[3:0]				MTB[3:0] : 48 ~ 56℃
0	0	0	0	1	1	0	1	1	0	MTC[3:0] : 56 ~ 64℃
0	0	MTD[3:0]				MTC[3:0]				MTD[3:0] : 64 ~ 72℃
0	0	0	0	1	1	0	1	1	1	MTE[3:0] : 72 ~ 80℃
0	0	MTF[3:0]				MTE[3:0]				MTF[3:0] : 80 ~ 88℃



Set TC Flag

Set TC flag of MT[F~0]. The positive flag defines increasing gradient, while the negative flag defines decreasing gradient.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1	1	0
0	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0
0	0	0	0	1	1	1	1	1	1
0	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8

Flag	Description
FMT[F:0]	FMTn: 0 = Negative flag; 1 = Positive flag

In brief, the relationship of the parameters FMTn/MTn[3:0] and the voltage gradients of V3/MV3/Vop are shown below:

TC Flag	MTn[3:0] Parameter				TC Curve Gradient: Mx (mV/℃)		
FMTn	MTn3	MTn2	MTn1	MTn0	V3	MV3	Vop
0	0	0	0	0	0	0	0
	0	0	0	1	-5	5	-10
	0	0	1	0	-10	10	-20
	0	0	1	1	-15	15	-30
	:	:	:	:	:	:	:
	1	1	0	0	-60	60	-120
	1	1	0	1	-65	65	-130
	1	1	1	0	-70	70	-140
	1	1	1	1	-75	75	-150
1	-	-	0	0	0	0	0
	-	-	0	1	5	-5	10
	-	-	1	0	10	-10	20
	-	-	1	1	15	-15	30

Note: There are only 4 gradients (including 0mV/℃) for positive TC flag of V3/MV3.

For example, the TC curve can be programmed as shown below:

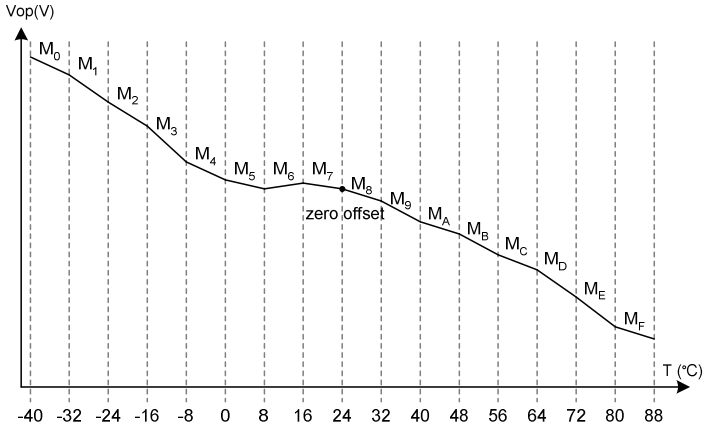


Fig. 10. Programmable Vop Temperature Compensation

TMPARNG

Temperature range A value set for Frame Freq. Adj.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	0
0	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0

Flag	Description
TA[6:0]	Temperature range set for automatic frame freq. adj. operation according the current temperature value. **TA Temperature (℃) + 40 = TA [6:0]** Example: If TA wants to be set at 24℃, TA[6:0]=24+40=64 (40h)

TMPBRNG

Temperature range B value set for Frame Freq. Adj.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	1
0	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Flag	Description
TB[6:0]	Temperature range set for automatic frame freq. adj. operation according the current temperature value. **TB Temperature (℃) + 40 = TB [6:0]** Example: If TB wants to be set at 24℃, TB[6:0]=24+40=64 (40h) ,

TMPCRNG

Temperature range C value set for Frame Freq. Adj.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	0
0	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0

Flag	Description
TC[6:0]	Temperature range set for automatic frame freq. adj. operation according the current temperature value. **TC Temperature(℃) + 40 = TC [6:0]** Example: If TC wants to be set at 24℃, TC[6:0]=24+40=64 (40 h)

ST7580A will auto-switch frame rate on different temperature such as **Fig. 11**. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPARNG, TMPBRNG and TMPCRNG. The frame rate FA, FB, FC and FD are defined by customer with command Set Frame Rate.

When the temperature is decreasing, the frame rate changes at the temperature specified by TA/TB/TC. When the temperature is increasing, the frame rate changes at the higher temperature: TA/TB/TC+TH (℃). The “TH” is specified by the “Set FR TC Hysteresis” command.

For example: TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please refer to **Fig. 11**.

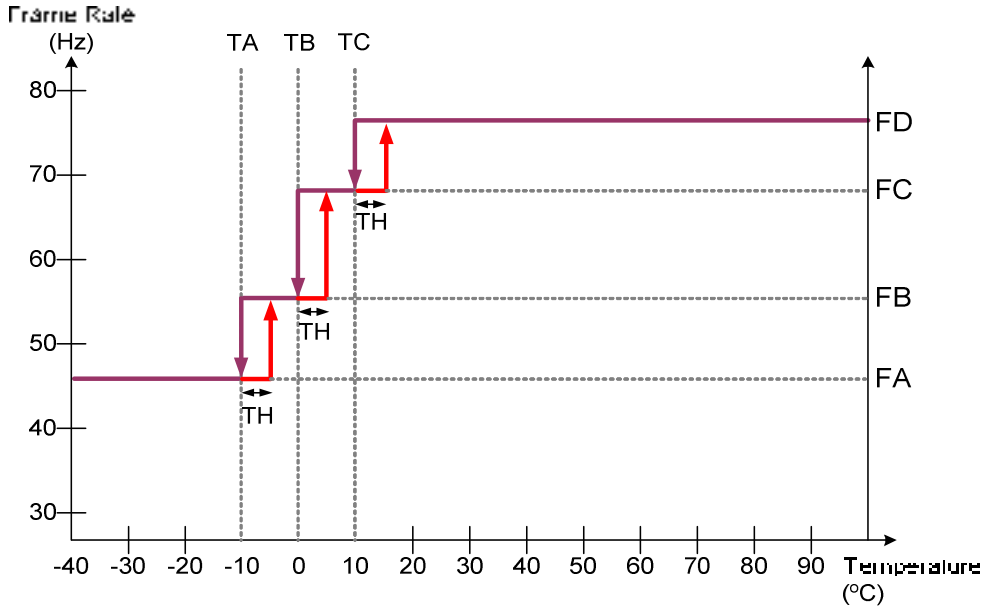


Fig. 11. Frame Rate vs. Temperature

Set FR TC Hysteresis

When the temperature changes around the junction between 2 different frame rate slopes, this instruction controls the threshold of temperature (only for increasing, as the red lines in Fig. 11). The TC function of FR will not change to the next slope unless the temperature exceeds this threshold. When the temperature is decreasing, it changes to another slope at the junction temperature (TA, TB & TC). This avoids the frame frequency switched in between and the display maybe flickers. As the result, it works like a “Hysteresis” of Frequency Temperature Compensation.

In brief, the frame frequency changes when:

1. The temperature increases above “TH” of the junction temperature (ex, TA+TH ℃).
2. The temperature decreases below the junction temperature.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	1	1	0	0
0	0	0	0	0	0	THF3	THF2	THF1	THF0

Set Vop TC Hysteresis

When the temperature changes around the junction between 2 different Vop slopes, this instruction controls the threshold of temperature (only for increasing). The TC function of Vop will not change to the next slope until the temperature exceeds this threshold. When the temperature is decreasing, it changes to another slope at the junction temperature (every 8℃ a junction). As the result, it works like a “Hysteresis” of Voltage Temperature Compensation.

In brief, the voltage changes when:

1. The temperature increases above “TH” of the junction temperature (ex, 32+TH ℃).
2. The temperature decreases below the junction temperature (ex, -8℃).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	1	1	1	0
0	0	0	0	THV5	THV4	THV3	THV2	THV1	THV0

Extended Instruction 2 (T[1:0]=(0,1) & TE=1)

EPCTIN

This instruction loads the registers' default value from PROM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	0	1
0	0	0	0	EWR	0	0	0	0	0

Flag	Description
EWR	EWR=1: The Write Enable of PROM will be opened. EWR=0: The Read Enable of PROM will be opened.

EPCTOUT

IC exits the PROM control circuit when executing this command.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	1	0

EPMWR

IC actives trigger to start PROM programming when executing this command.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	0	1	1

EPMRD

IC actives trigger to start PROM programming when executing this command.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0

AutoLoadSet

PROM data auto re-load control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	1	0
0	0	0	0	0	ARD	0	0	0	0

Flag	Description
ARD	ARD=1: Disable PROM auto recovery, ARD=0: Enable PROM auto recovery

Vop Up

This instruction increases the VopOffset by 1.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	1	1	0

Vop Down

This instruction decreases the VopOffset by 1.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	1	1	1

10. OPERATION FLOW

(1) Power ON Sequence

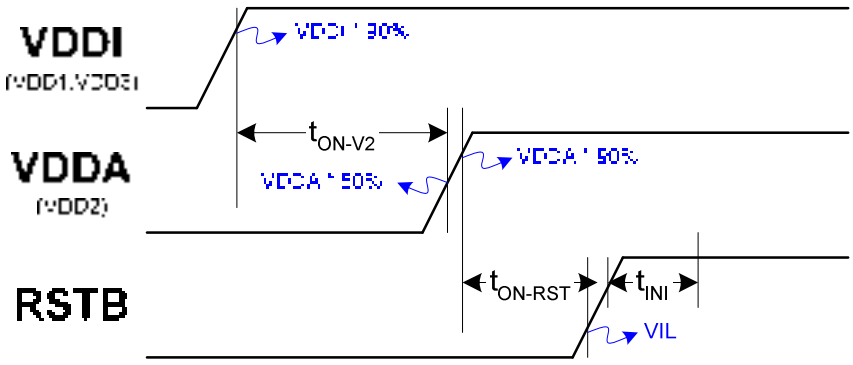


Fig. 12. Power ON Sequence

Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● If VDDI and VDDA are separated, turn ON VDDI first and then VDDA. It must keep a hardware reset until the last power is stable (higher than 90% of rated value). ● Applying VDDI and VDDA in any order will not damage IC.
RSTB wait time	t_{ON-RST}	$0 \le t_{ON-RST}$	● Keep "$t_{ON-V2} + t_{ON-RST}$" ≥ t_{RW} . ● Increasing t_{ON-RST} can cover the power stable time tolerance in customer's system.
Initial wait time	t_{INI}	$t_R \le t_{INI}$	● The initial procedure starts after t_{INI}.

Note:

1. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
   The specification listed below just wants to prevent abnormal display on LCD module.
2. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. The power stable time depends on system and the time is not included in this specification (customer should consider this factor).

(2) Initialization

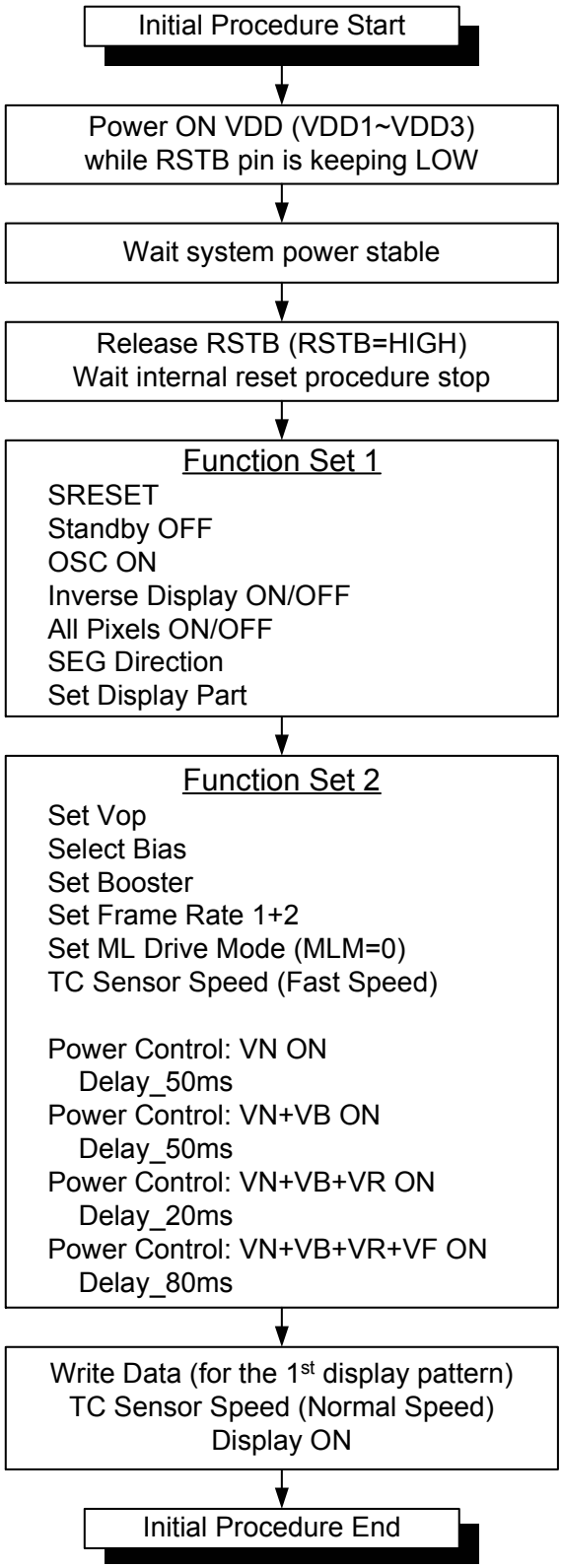


Fig. 13. Initialization Flow with Internal Power Circuits

(3) Standby ON

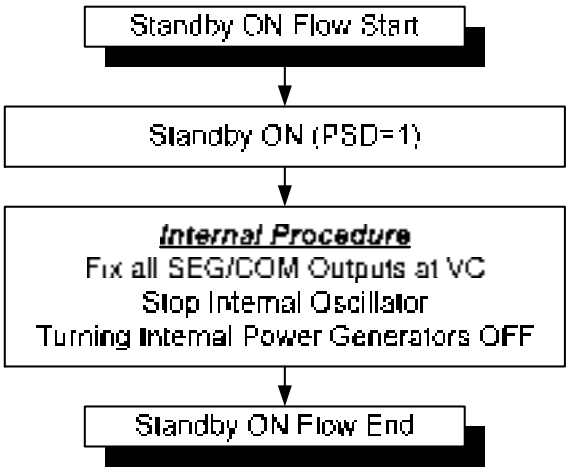


Fig. 14. Standby ON Flow

(4) Standby OFF

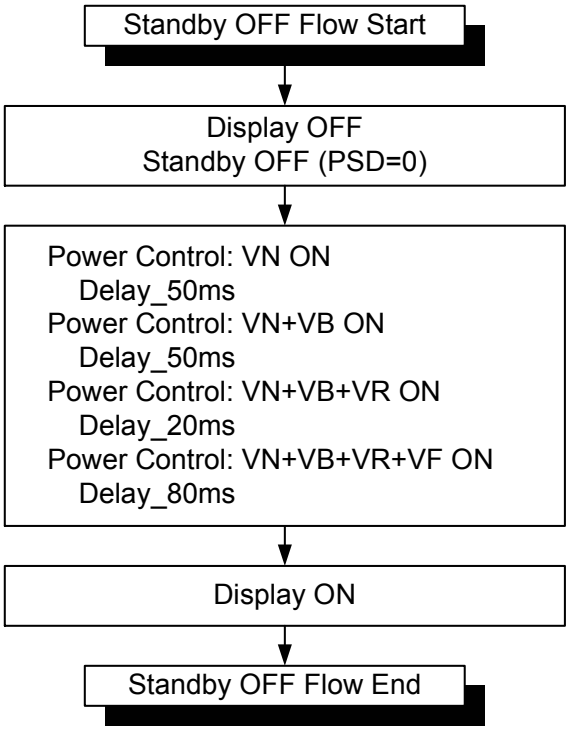


Fig. 15. Standby OFF Flow

(5) Power OFF Sequence

Please execute the Power OFF flow before turning VDDI/VDDA OFF. Otherwise, unexpected abnormal display maybe occurred on the LCD module.

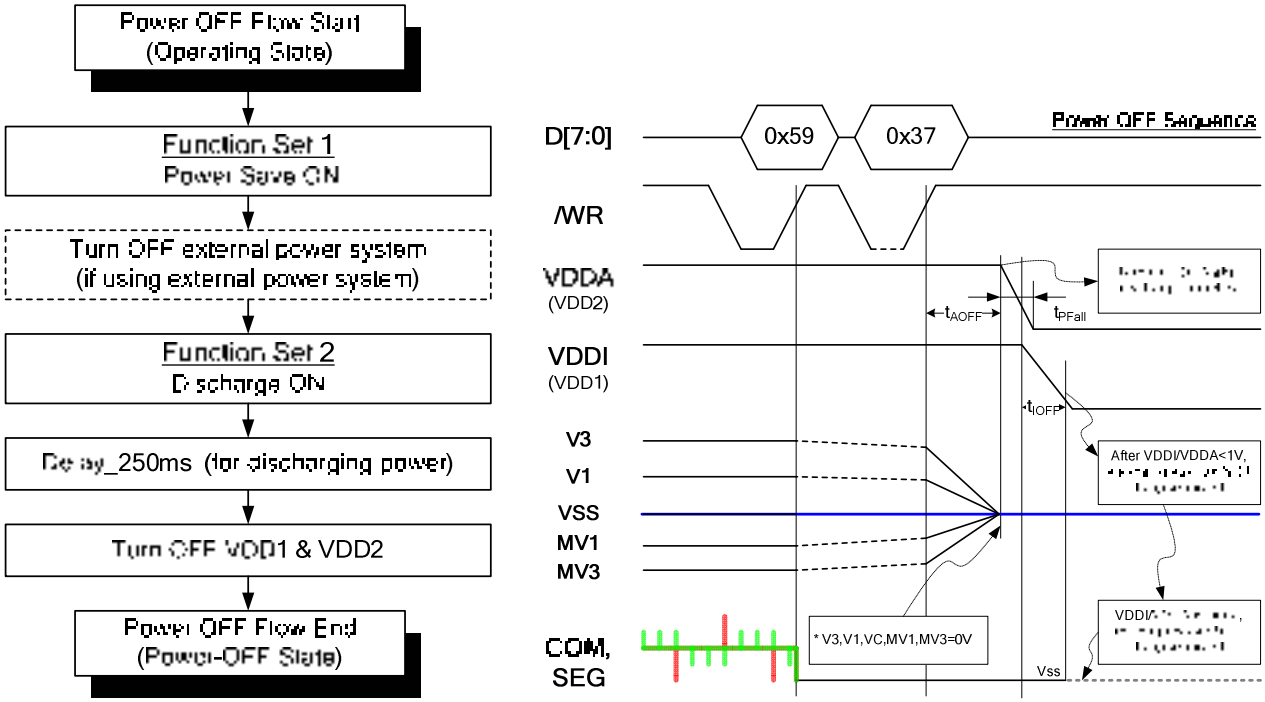


Fig. 16. Power OFF Flow and Power OFF Sequence

Timing Requirement:

Item	Symbol	Requirement	Note
VDDA OFF delay	t_{AOFF}	250ms ≤ t_{AOFF}	● Turn VDDA OFF after discharge-procedure is finished.
VDDA Falling Time	t_{PFall}	Recommend t_{Pfall} ≤ 5sec	● t_{Pfall} depends on the LCD module and power circuit on the application system. ● It is recommended to keep t_{Pfall} less than 10 seconds.
VDDI OFF delay	t_{IOFF}	0 ≤ t_{IOFF}	● If VDDI and VDDA are separated, turn VDDI OFF after VDDA, is lower than 0.2V.

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	–0.3 ~ 6.0	V
Internal Digital Operating Voltage	VDI	–0.3 ~ 3.0	V
Analog Power supply voltage	VDD2	–0.3 ~ 6.0	V
Power Supply Voltage (OSC & Vref)	VDD3	–0.3 ~ 6.0	V
LCD Power supply voltage	V3-MV3	–0.3 ~ 20	V
LCD Power supply voltage	V1	–0.3 ~ VDD2+0.3	V
LCD Power supply voltage	MV1	–(VDD2+0.3) ~ 0.3	V
MPU interface Input Voltage	Vi	–0.3 ~ VDD1+0.3	V
Operating temperature	TOPR	–40 to +85	℃
Storage temperature	TSTR (TCP) TSTR (Dice)	–55 to +100 –55 to +120	℃

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

13. DC CHARACTERISTICS

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		2.7	–	5.5	V	VDD1
Operating Voltage (2)	VDD2		2.7	–	5.5	V	VDD2
Operating Voltage (3)	VDI		1.7	–	2.8	V	VDD3
Operating Voltage (4)	V3		3	–	9	V	V3
	MV3		-9	–	-3	V	MV3
Operating Voltage (5)	V1		1	–	2.4	V	V1
	MV1		-2.4	–	-1	V	MV3
Input High-level Voltage	V_{IH}		0.7 x VDD1	–	VDD1	V	MPU Interface
Input Low-level Voltage	V_{IL}		VSS1	–	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OH}	I_{OUT}=1mA, VDD1=2.7V	0.8 x VDD1	–	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OL}	I_{OUT}=-1mA, VDD1=2.7V	VSS1	–	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		-1.0	–	1.0	uA	MPU Interface
Output Leakage Current	I_{LO}		-3.0	–	3.0	uA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25℃ 1/5 bias, V3=9V ΔV=0.9V	–	2	–	KΩ	COMx
		Ta=25℃ 1/5 bias, V1=1.8V ΔV=0.18V	–	2	–	KΩ	SEGx
Frame Frequency	fFR	Duty=1/84; FR[3:0]=0,1,1,1; VDDI=VDDA=3.0V; Ta = 25℃	–	78	–	Hz	

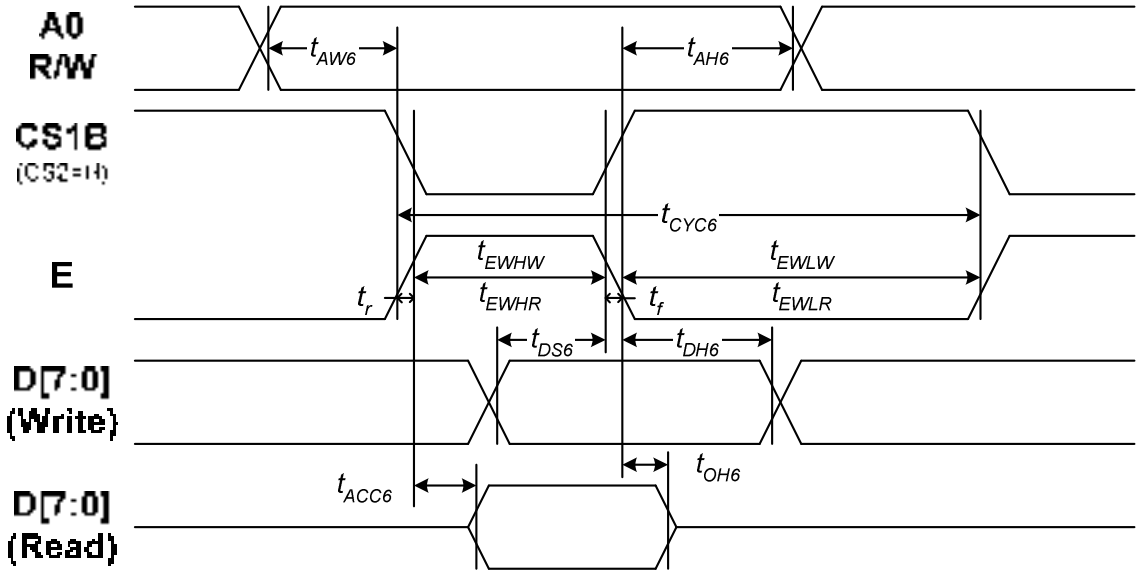
Note: VSS=VSS1=VSS2=VSS3=0V

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=3.0V, 9V 1/5 bias, Ta=25℃	—	500	—	uA	
Power Down	ISS	VDD1=VDD2=3.0V, Ta=25℃	—	25	50	uA	

14. TIMING CHARACTERISTICS

System Bus Timing for 6800 Series MPU

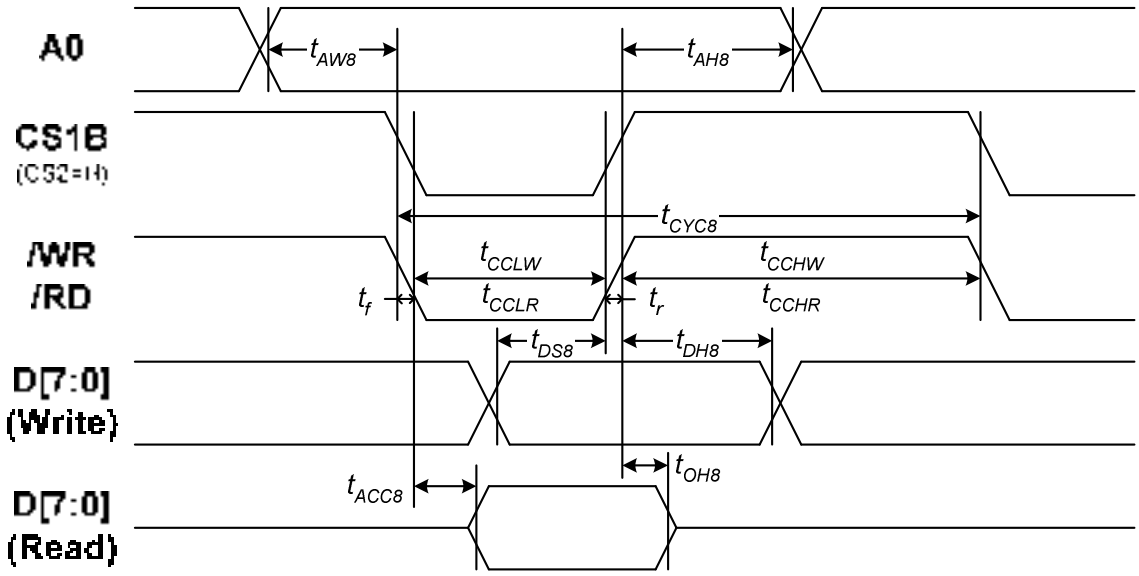


(VDD1 = 3V~5V, Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	-	ns
Address hold time	R/W	tAH6		0	-	
System cycle time	E	tCYC6		300	-	
Enable L pulse width (WRITE)		tEWLW		95	-	
Enable H pulse width (WRITE)		tEWHW		30	-	
Enable L pulse width (READ)		tEWLR		30	-	
Enable H pulse width (READ)		tEWHR		100	-	
Data setup time (Write)	D[7:0]	tDS6		40	-	
Data hold time (Write)		tDH6		15	-	
Data access time (Read)		tACC6	CL=100pF	-	140	
Data output disable time (Read)		tOH6		10	100	

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤ (tCYC6 - tEWLR - tEWHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tEWLW and tEWLR are specified as the overlap between CS1B/CS2 being “L” and E.

System Bus Timing for 8080 Series MPU

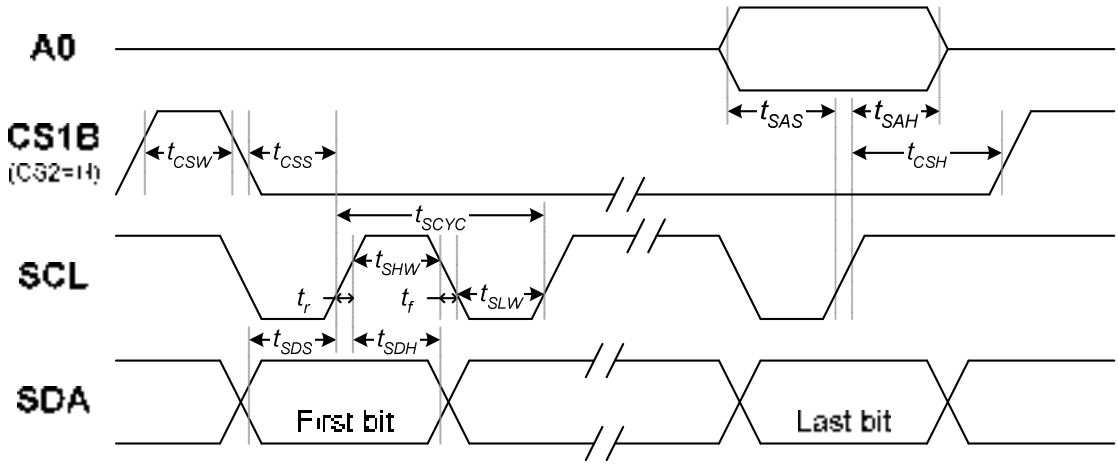


(VDD1 = 3V~5V, Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	-	Ns
Address hold time		tAH8		0	-	
System cycle time	/WR	tCYC8		300	-	
/WR L pulse width		tCCLW		45	-	
/WR H pulse width		tCCHW		95	-	
/RD L pulse width	/RD	tCCLR		95	-	
/RD H pulse width		tCCHR		50	-	
Data setup time (Write)	D[7:0]	tDS8		40	-	
Data hold time (Write)		tDH8		15	-	
Data access time (Read)		tACC8	CL=100pF	-	140	
Data output disable time (Read)		tOH8		10	100	

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 - tCCLW - tCCHW) for (tr + tf) ≤ (tCYC8 - tCCLR - tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CS1B/CS2 being “L” and WR and RD being at the “L” level.

System Bus Timing for 4-Line Serial Interface

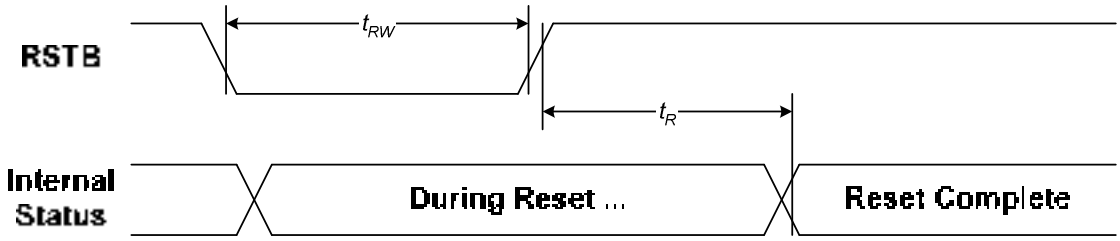


(VDD1 = 3V~5V, Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		250	-	ns
SCL “H” pulse width		tSHW		100	-	
SCL “L” pulse width		tSLW		100	-	
Address setup time	A0	tSAS		150	-	
Address hold time		tSAH		150	-	
Data setup time	SDA	tSDS		100	-	
Data hold time		tSDH		100	-	
CSB setup time	CS1B	tCSS		150	-	
CSB hold time		tCSH		150	-	
CSB wait time		tCSW		20	-	

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.
3. The specification of CS2 timing is the same as CS1B.

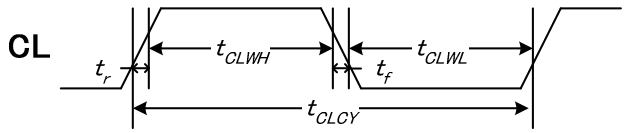
Hardware Reset Timing



(VDD1 = 3V~5V, Ta =25℃)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR			3.5	us
Reset “L” pulse width	tRW		3.5		

External Clock Timing



(VDD1 = 3V~5V, Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR Delay Time	FR	tDFR		-0.65	–	0.65	us
Clock High Pulse Width	CL	tCLWH	Default fCL=1630KHz	276.1	306.7	337.4	ns
Clock Low Pulse Width		tCLWL	ΔfFR=+/-10%	276.1	306.7	337.4	
Clock Cycle Time		tCLCY	*2, *3	552.1	613.5	674.8	
Clock Duty Ratio		tCLWH / tCLCY	*4	40	50	60	%
Clock Input Rising Time		tr		0	–	20	ns
Clock Input Falling Time		tf		0	–	20	

Note:

1. All timings are specified by 20% and 80% of VDD1 as the reference.
2. Be sure the real cycle time of CL includes tr and tf, so that : tCLCY = (tCLWH + tCLWL + tr + tf) are specified.
3. It is necessary to secure tCLCY, tCLWH & tCLWL even if the external CL is out of this specification.
   Ex, tCLCY = (tCLWH + tCLWL + β)……, where "β > $tr_{(max)}$ + $tf_{(max)}$" but tCLCY must be in specification.
4. tCLCY is still in specification.
5. AC timing of CL pin controls the accuracy of operation clock. This definition includes 10% tolerance already.
6. This specification defines the default speed of internal clock system. If the timing is over specification, all related speed should be re-calculated (such as, fFR and clock based operations).

APPLICATION NOTE

Application Circuits

6800 series 8-bit Interface:

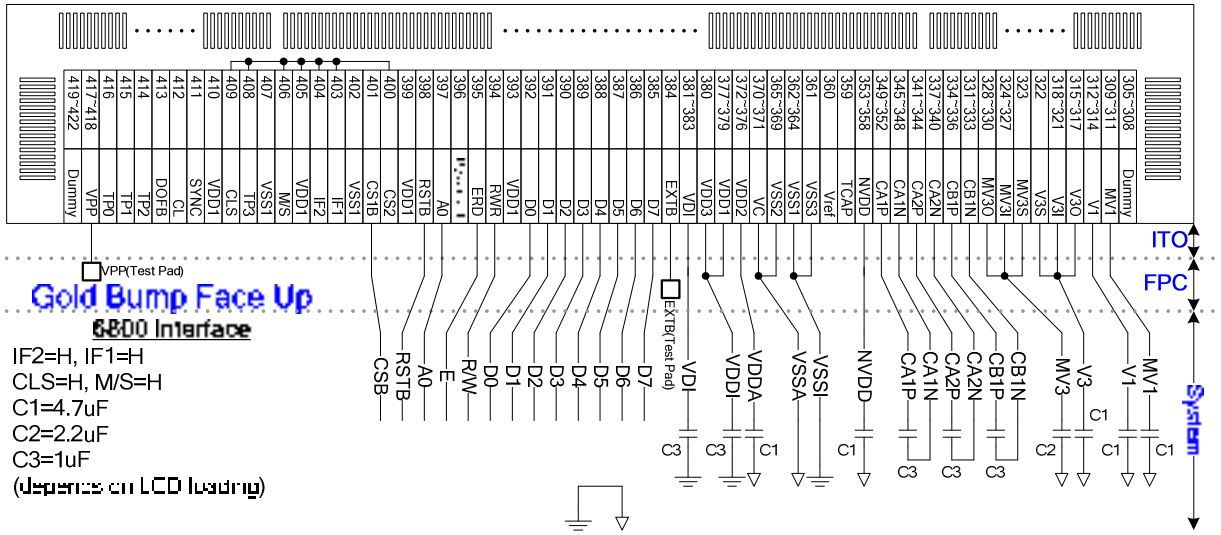


Fig. 17. Reference Application Circuit: Parallel 6800 Interface

8080 series 8-bit Interface:

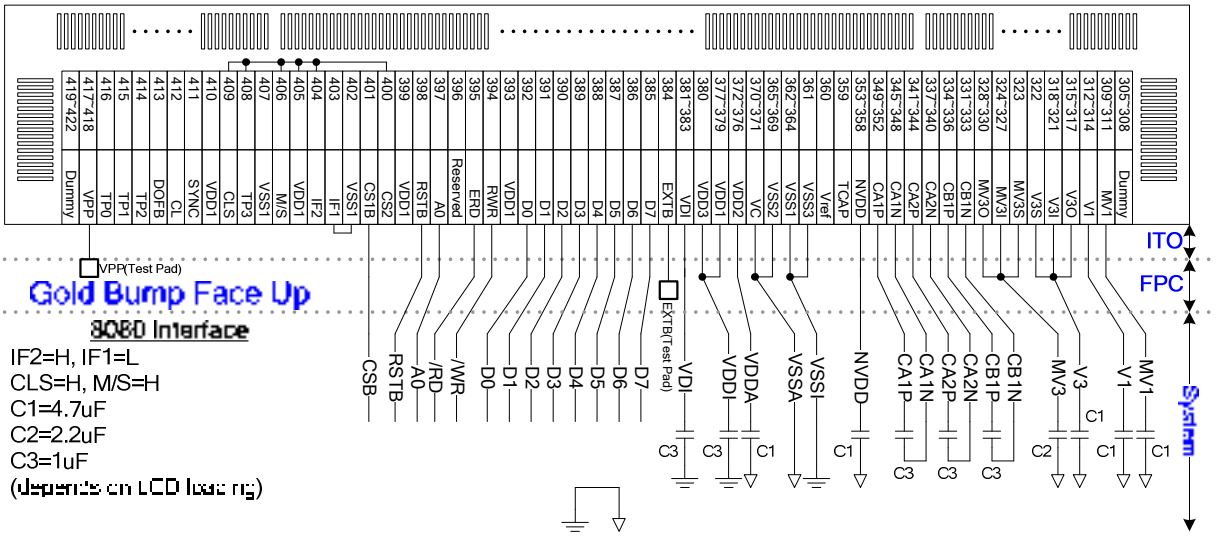


Fig. 18. Reference Application Circuit: Parallel 8080 Interface

4-Line series Interface:

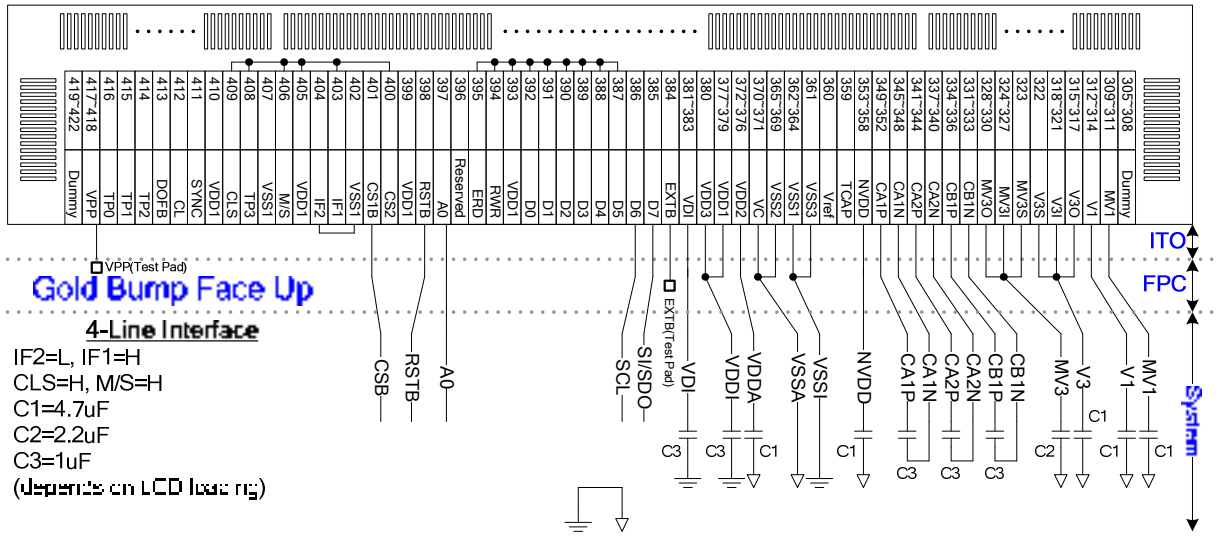
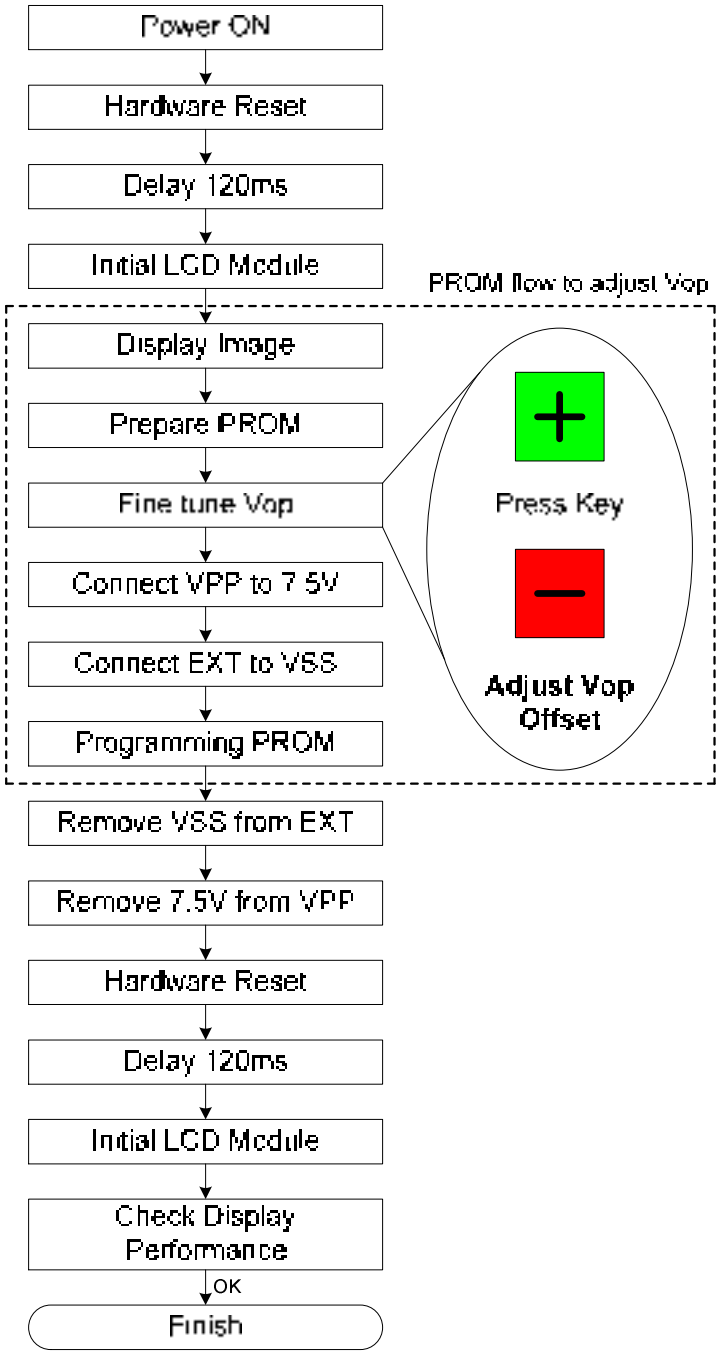


Fig. 19. Reference Application Circuit: Series 4-Line Interface

PROM Burning Flow:

The reference PROM programming flow to adjust Vop is shown below:



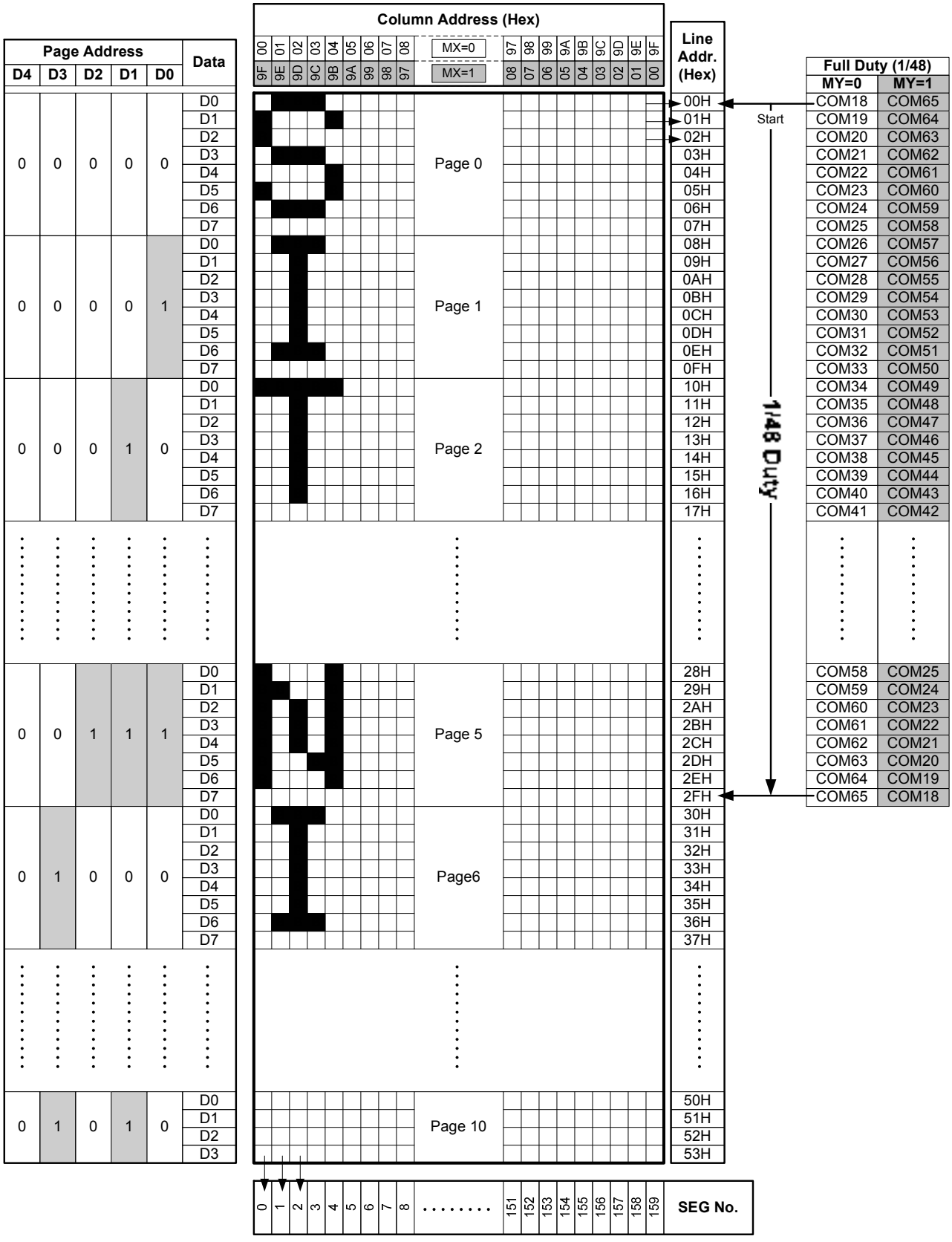
void Prepare_PROM (void)			
{			
//----------Disable Auto-read + Manual read once ----------			
	Write(COMMAND,0xFB);		// Enter PROM Control Mode
	Write(COMMAND,0x96);		// Auto Load Set
	Write(COMMAND,0x10);		// Auto Load Disable
	Write(COMMAND,0x95);		// PROM writing setup
	Write(COMMAND,0x08);		
	Write(COMMAND,0x91);		// Read/write mode setting
	Write(COMMAND,0x00);		// Set read mode
	delayms(10);		// Delay 10ms
	Write(COMMAND,0x94);		// Read active
	delayms(10);		// Delay 10ms
	Write(COMMAND,0x92);		// Cancel control
	Write(COMMAND,0xF8);		//Exit PROM Control Mode
	delayms(20);		// Delay 20ms
}			
//----------Fine tune vop offset----------			
void Fine_tune_Vop (void)			
{			
	Write(COMMAND,0xFB);		// Enter PROM Control Mode
	Write(COMMAND,0xDE); or Write(COMMAND,0xDF);		// Fine tuning Vop here by command. ***Note #2***
	Write(COMMAND,0xF8);		// Exit PROM Control Mode
}			
void Progeam_PROM (void)			
{			
	Write(COMMAND,0xFB);		// Enter PROM Control Mode
	Write(COMMAND,0x91);		// Read/write mode setting
	Write(COMMAND,0x20);		// Set Write mode
	delayms(10);		// Delay 10ms
	Write(COMMAND,0x93);		// Write active
	delayms(50);		// Delay 50ms
	Write(COMMAND,0x92);		// Cancel control
	Write(COMMAND,0xF8);		//Exit PROM Control Mode
}			

Note:

1. If the Vop and display performance is not suitable after burning PROM, the Vop has to re-fine tune.
2. In this section"+" & "-" key button, please execute Write(COMMAND,0xDE) to increase one step at Vop and execute Write(COMMAND,0xDF) to decrease one step at Vop, if necessary.
3. The TC is enabled in burning flow. If the LCD backlight is too close to IC, its temperature will confuse IC sensor.
4. This flow (Burning Flow) is used for LCM assembler.
5. PROM can be written FOUR times

DDRAM Output Example

For example, a DDRAM map in 1/48 Duty with original pin name (1/84 Duty) is shown below:



REVERSION HISTORY

Version	Date	Description
1.0	2010/06/29	● Remove “Preliminary”.
1.1	2010/8/26	● Correct Pad Location.
1.2	2010/9/2	● Add Reference Application Circuit: 4-Line interface. ● Add PROM programming flow and description of VPP/EXTB. ● Add the commands to read/write PROM.
1.3	2010/10/12	● Correct “Set Page Address” command typo.
1.4	2010/10/15	● Correct “Set Display Part” command typo.
1.5	2010/11/5	● Redraw DDRAM output mapping figure. And add example into appendix. ● Update parameter for “Set Display Part” and combine “Set COM Direction” to prevent misunderstanding. ● Add notes for optimized setting in “Set Bias”. ● Fix typing mistake in “Set Booster” description. ● Rewrite “Set Frame Rate 1 & 2” description. ● Fix “Test” instruction description. ● Remove Master/Slave feature (this is for COF/TCP applications). ● Add Display OFF instruction to the “Standby OFF” flow.
1.6	2011/2/11	● Fix typing mistakes. ● Use the same pin name in pin description and application. ● Add CL signal description and timing specification. ● Add pin note (Page 11). ● ITO pin list add: TCAP, NVDD. ● Add detail description to ITO layout note. ● Modify command description of “Set Frame Rate 1 & 2” &“Set Vop TC-Curves”. ● Fix PROM command mistake: EPCTIN. ● Fix parameter mistake in Set Display Part example: MY=1: DCh, 30h, D3h, “4”2h, C8h ● Release PROM description in Set Vop description. ● Fix Optimized Bias formula. ● Rewrite description of FR Hysteresis and Vop Hysteresis. ● Remove Chinese symbols. ● Add CS2 state into timing charts. ● Add tCSW timing specification into 4-Line serial interface. ● Modify PROM flow to prevent manually operation mistake.