Sitronix

ST7038

Dot Matrix LCD Controller/Driver

FEATURES

- **5 x 8 dot matrix possible**
- **Support low voltage single power operation:**
  - VDD, VDD2: 1.8 to 3.3V
- **LCD Voltage Operation Range (V0/Vout)**
  - Programmable V0: 3 to 7V(V0)
  - External power applied: Max. 12V(Vout)
- **Interface**
  - 6800-4bit / 8bit interface
  - 8080-4bit / 8bit interface
  - 3-line serial interface
  - 4-line serial interface
  - I^2C interface
- **Support display mode:**
  - 8-COM x 100-SEG and 80 ICON
  - 16-COM x 100-SEG and 80 ICON
  - 24-COM x 80-SEG and 80 ICON
- **10,240-bit Character Generator ROM (CGROM) stores 256 character fonts**
- **64 x 8-bit Character Generator RAM (CGRAM)**
- **80 x 8-bit Display RAM (80 characters max.)**
- **16 x 5 bit ICON RAM**
- **Variable instruction functions:** clear display, return home, display ON/OFF, cursor ON/OFF, character blink, cursor shift, display shift, double height font, ICON control and character generation RAM
- **Reset circuit through an external reset pin**
- **Internal oscillator or external clock**
- **Built-in low power consumption voltage booster, regulator and follower circuit**
- **Built-in high-accuracy voltage regulator:**
  - Programmable output range: 3~7V
- **COM/SEG direction selectable by instruction**
- **Selectable CGRAM/CGROM size**
- **Package Type: COG**

GENERAL DESCRIPTION

ST7038 dot-matrix liquid crystal display controller can display alphanumeric, Japanese kana characters and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a microprocessor with 4/8-bit 6800-series or 8080-series, 3/4-line serial or fast I^2C interface. Since all the functions (such as display RAM, character generator ROM/RAM and liquid crystal driver) required for driving a dot-matrix liquid crystal display are internally embedded in this chip, a minimal system can be used with this controller/driver.

The Character Generator ROM of ST7038 has 256 5x8dot cells and stores 256 different character fonts (5x8dot).

ST7038 is suitable for low voltage supply (1.8V to 3.3V) and is perfectly suitable for any portable product which is driven by the battery and requires low power consumption.

The display resolution of ST7038 dot-matrix LCD driver can be either 1-line x 20 characters, 2-line x 20 characters or 3-line x 16 characters with 80-bit ICON.

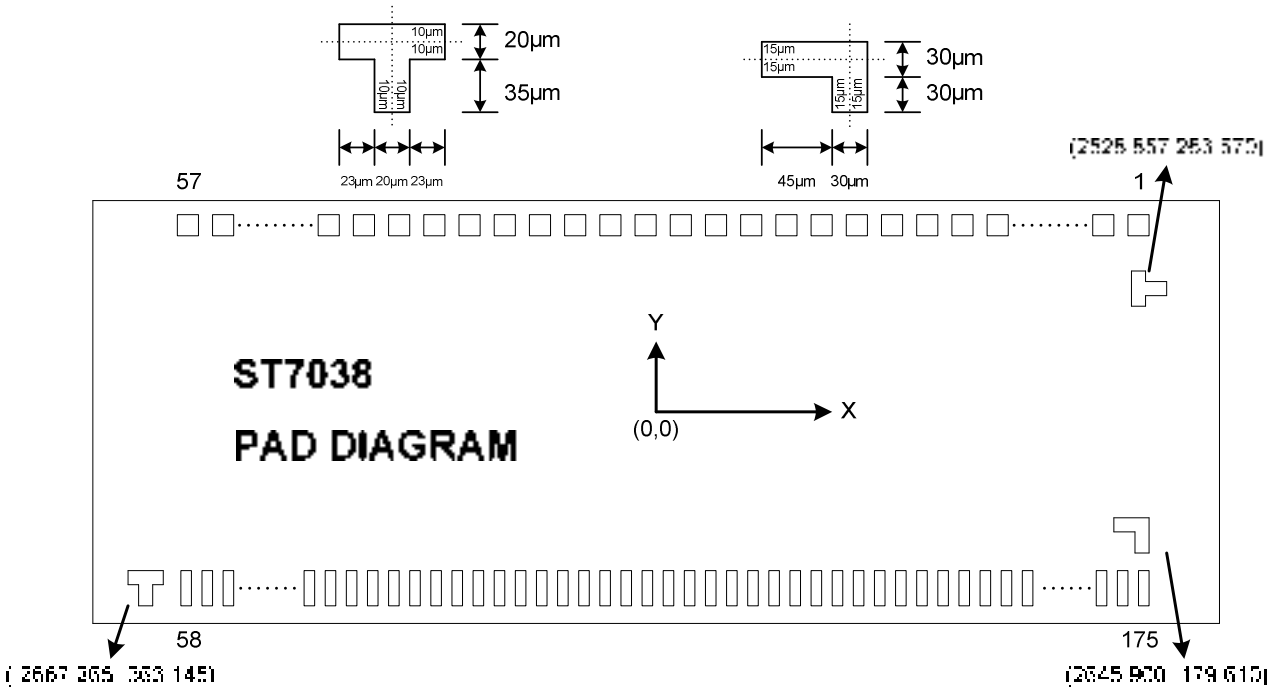
ST7038 works alone without extra cascaded drivers.

Product Name	Character generator ROM Size	Support Character
ST7038-0B	256	English / Europe / Japan

ST7038	**6800-4bit / 8bit interface 8080-4bit / 8bit interface 3-line/4-line serial interface (without I^2C interface)**	
ST7038i	**I^2C interface**	

PAD ARRANGEMENT

- Chip Size: 5476.2um X 906.2 um
- Bump Pitch:
  I/O PAD: 73um
  COM/SEG PAD: 45um
- Bump size:
  PAD No. 001 ~ 057: 55um X 60um
  PAD No. 058 ~ 175: 30um X 80um
- Bump Height: 17um
- Chip Thickness: 480um



PAD CENTER COORDINATES (3-line & 2-line with double height)

Unit: um

PAD No.	PIN Name	X	Y
1	XRESET	2543.915	379
2	OSC	2424.915	379
3	VDD	2350.675	379
4	A0(RS)	2276.575	379
5	CSB	2157.575	379
6	/WR(RW)	2084.575	379
7	/RD(E)	1965.575	379
8	DB[0]	1892.575	379
9	DB[1]	1773.575	379
10	DB[2]	1700.575	379
11	DB[3]	1581.575	379
12	DB[4]	1508.575	379
13	DB[5]	1389.575	379
14	DB[6]	1316.575	379
15	DB[7]	1197.575	379
16	VSS	1124.575	379
17	VSS	1051.575	379
18	VSS	978.575	379
19	VSS	905.575	379
20	PS0	830.945	379
21	PS1	711.945	379
22	PS2	638.945	379
23	CLS	519.945	379
24	TEST[0]	447.945	379
25	TEST[1]	298.945	379
26	TEST[2]	223.945	379
27	TEST[3]	48.945	379
28	TEST[4]	-26.055	379
29	TEST[5]	-201.055	379
30	VDD	-276.94	379
31	VDD	-349.94	379
32	VDD	-422.94	379
33	VDD2	-495.94	379
34	VDD2	-568.94	379
35	VDD2	-641.94	379
36	VOUT	-714.94	379
37	VOUT	-787.94	379
38	VOUT	-860.94	379
39	CAP3P	-933.94	379
40	CAP3P	-1006.94	379
41	CAP1P	-1079.94	379
42	CAP1P	-1152.94	379
43	CAP1N	-1225.94	379
44	CAP1N	-1298.94	379
45	CAP1N	-1371.94	379
46	CAP2P	-1444.94	379
47	CAP2P	-1517.94	379
48	CAP2N	-1590.94	379
49	CAP2N	-1663.94	379
50	CAP4P	-1736.71	379
51	CAP4P	-1809.94	379
52	VRS	-1892.1	379
53	V0	-1965.26	379
54	V1	-2053.56	379

PAD No.	PIN Name	X	Y
55	V2	-2126.56	379
56	V3	-2199.56	379
57	V4	-2272.56	379
58	COM[12]	-2611.93	-369
59	COM[11]	-2566.93	-369
60	COM[10]	-2521.93	-369
61	COM[9]	-2476.93	-369
62	COM[8]	-2431.93	-369
63	COM[7]	-2386.93	-369
64	COM[6]	-2341.93	-369
65	COM[5]	-2296.93	-369
66	NC	-2251.93	-369
67	COM[4]	-2206.93	-369
68	COM[3]	-2161.93	-369
69	COM[2]	-2116.93	-369
70	COM[1]	-2071.93	-369
71	NC	-2026.93	-369
72	NC	-1981.93	-369
73	NC	-1936.93	-369
74	NC	-1891.93	-369
75	NC	-1846.93	-369
76	NC	-1801.93	-369
77	SEG[1]	-1756.93	-369
78	SEG[2]	-1711.93	-369
79	SEG[3]	-1666.93	-369
80	SEG[4]	-1621.93	-369
81	SEG[5]	-1576.93	-369
82	SEG[6]	-1531.93	-369
83	SEG[7]	-1486.93	-369
84	SEG[8]	-1441.93	-369
85	SEG[9]	-1396.93	-369
86	SEG[10]	-1351.93	-369
87	SEG[11]	-1306.93	-369
88	SEG[12]	-1261.93	-369
89	SEG[13]	-1216.93	-369
90	SEG[14]	-1171.93	-369
91	SEG[15]	-1126.93	-369
92	SEG[16]	-1081.93	-369
93	SEG[17]	-1036.93	-369
94	SEG[18]	-991.93	-369
95	SEG[19]	-946.93	-369
96	SEG[20]	-901.93	-369
97	SEG[21]	-856.93	-369
98	SEG[22]	-811.93	-369
99	SEG[23]	-766.93	-369
100	SEG[24]	-721.93	-369
101	SEG[25]	-676.93	-369
102	SEG[26]	-631.93	-369
103	SEG[27]	-586.93	-369
104	SEG[28]	-541.93	-369
105	SEG[29]	-496.93	-369
106	SEG[30]	-451.93	-369
107	SEG[31]	-406.93	-369
108	SEG[32]	-361.93	-369

PAD No.	PIN Name	X	Y
109	SEG[33]	-316.93	-369
110	SEG[34]	-271.93	-369
111	SEG[35]	-226.93	-369
112	SEG[36]	-181.93	-369
113	SEG[37]	-136.93	-369
114	SEG[38]	-91.93	-369
115	SEG[39]	-46.93	-369
116	SEG[40]	-1.93	-369
117	SEG[41]	43.07	-369
118	SEG[42]	88.07	-369
119	SEG[43]	133.07	-369
120	SEG[44]	178.07	-369
121	SEG[45]	223.07	-369
122	SEG[46]	268.07	-369
123	SEG[47]	313.07	-369
124	SEG[48]	358.07	-369
125	SEG[49]	403.07	-369
126	SEG[50]	448.07	-369
127	SEG[51]	493.07	-369
128	SEG[52]	538.07	-369
129	SEG[53]	583.07	-369
130	SEG[54]	628.07	-369
131	SEG[55]	673.07	-369
132	SEG[56]	718.07	-369
133	SEG[57]	763.07	-369
134	SEG[58]	808.07	-369
135	SEG[59]	853.07	-369
136	SEG[60]	898.07	-369
137	SEG[61]	943.07	-369
138	SEG[62]	988.07	-369
139	SEG[63]	1033.07	-369
140	SEG[64]	1078.07	-369
141	SEG[65]	1123.07	-369
142	SEG[66]	1168.07	-369
143	SEG[67]	1213.07	-369
144	SEG[68]	1258.07	-369
145	SEG[69]	1303.07	-369
146	SEG[70]	1348.07	-369
147	SEG[71]	1393.07	-369
148	SEG[72]	1438.07	-369
149	SEG[73]	1483.07	-369
150	SEG[74]	1528.07	-369
151	SEG[75]	1573.07	-369
152	SEG[76]	1618.07	-369
153	SEG[77]	1663.07	-369
154	SEG[78]	1708.07	-369
155	SEG[79]	1753.07	-369
156	SEG[80]	1798.07	-369
157	NC	1843.07	-369
158	NC	1888.07	-369
159	NC	1933.07	-369
160	NC	1978.07	-369
161	NC	2023.07	-369
162	NC	2068.07	-369
163	COM[13]	2113.07	-369

PAD No.	PIN Name	X	Y
164	COM[14]	2158.07	-369
165	COM[15]	2203.07	-369
166	COM[16]	2248.07	-369
167	COM[17]	2293.07	-369
168	COM[18]	2338.07	-369
169	COM[19]	2383.07	-369
170	COM[20]	2428.07	-369
171	COM[21]	2473.07	-369
172	COM[22]	2518.07	-369
173	COM[23]	2563.07	-369
174	COM[24]	2608.07	-369
175	COMI2	2653.07	-369

PAD CENTER COORDINATES (2-line & 1-line with double height)

Unit: um

PAD No.	PIN Name	X	Y
1	XRESET	2543.915	379
2	OSC	2424.915	379
3	VDD	2350.675	379
4	A0(RS)	2276.575	379
5	CSB	2157.575	379
6	/WR(RW)	2084.575	379
7	/RD(E)	1965.575	379
8	DB[0]	1892.575	379
9	DB[1]	1773.575	379
10	DB[2]	1700.575	379
11	DB[3]	1581.575	379
12	DB[4]	1508.575	379
13	DB[5]	1389.575	379
14	DB[6]	1316.575	379
15	DB[7]	1197.575	379
16	VSS	1124.575	379
17	VSS	1051.575	379
18	VSS	978.575	379
19	VSS	905.575	379
20	PS0	830.945	379
21	PS1	711.945	379
22	PS2	638.945	379
23	CLS	519.945	379
24	TEST[0]	447.945	379
25	TEST[1]	298.945	379
26	TEST[2]	223.945	379
27	TEST[3]	48.945	379
28	TEST[4]	-26.055	379
29	TEST[5]	-201.055	379
30	VDD	-276.94	379
31	VDD	-349.94	379
32	VDD	-422.94	379
33	VDD2	-495.94	379
34	VDD2	-568.94	379
35	VDD2	-641.94	379
36	VOUT	-714.94	379
37	VOUT	-787.94	379
38	VOUT	-860.94	379
39	CPA3P	-933.94	379
40	CAP3P	-1006.94	379
41	CAP1P	-1079.94	379
42	CAP1P	-1152.94	379
43	CAP1N	-1225.94	379
44	CAP1N	-1298.94	379
45	CAP1N	-1371.94	379
46	CAP2P	-1444.94	379
47	CAP2P	-1517.94	379
48	CAP2N	-1590.94	379
49	CAP2N	-1663.94	379
50	CAP4P	-1736.71	379
51	CAP4P	-1809.94	379
52	VRS	-1892.1	379
53	V0	-1965.26	379
54	V1	-2053.56	379

PAD No.	PIN Name	X	Y
55	V2	-2126.56	379
56	V3	-2199.56	379
57	V4	-2272.56	379
58	COM[8]	-2611.93	-369
59	COM[7]	-2566.93	-369
60	COM[6]	-2521.93	-369
61	COM[5]	-2476.93	-369
62	COM[4]	-2431.93	-369
63	COM[3]	-2386.93	-369
64	COM[2]	-2341.93	-369
65	COM[1]	-2296.93	-369
66	COMI1	-2251.93	-369
67	SEG[1]	-2206.93	-369
68	SEG[2]	-2161.93	-369
69	SEG[3]	-2116.93	-369
70	SEG[4]	-2071.93	-369
71	SEG[5]	-2026.93	-369
72	SEG[6]	-1981.93	-369
73	SEG[7]	-1936.93	-369
74	SEG[8]	-1891.93	-369
75	SEG[9]	-1846.93	-369
76	SEG[10]	-1801.93	-369
77	SEG[11]	-1756.93	-369
78	SEG[12]	-1711.93	-369
79	SEG[13]	-1666.93	-369
80	SEG[14]	-1621.93	-369
81	SEG[15]	-1576.93	-369
82	SEG[16]	-1531.93	-369
83	SEG[17]	-1486.93	-369
84	SEG[18]	-1441.93	-369
85	SEG[19]	-1396.93	-369
86	SEG[20]	-1351.93	-369
87	SEG[21]	-1306.93	-369
88	SEG[22]	-1261.93	-369
89	SEG[23]	-1216.93	-369
90	SEG[24]	-1171.93	-369
91	SEG[25]	-1126.93	-369
92	SEG[26]	-1081.93	-369
93	SEG[27]	-1036.93	-369
94	SEG[28]	-991.93	-369
95	SEG[29]	-946.93	-369
96	SEG[30]	-901.93	-369
97	SEG[31]	-856.93	-369
98	SEG[32]	-811.93	-369
99	SEG[33]	-766.93	-369
100	SEG[34]	-721.93	-369
101	SEG[35]	-676.93	-369
102	SEG[36]	-631.93	-369
103	SEG[37]	-586.93	-369
104	SEG[38]	-541.93	-369
105	SEG[39]	-496.93	-369
106	SEG[40]	-451.93	-369
107	SEG[41]	-406.93	-369
108	SEG[42]	-361.93	-369

PAD No.	PIN Name	X	Y
109	SEG[43]	-316.93	-369
110	SEG[44]	-271.93	-369
111	SEG[45]	-226.93	-369
112	SEG[46]	-181.93	-369
113	SEG[47]	-136.93	-369
114	SEG[48]	-91.93	-369
115	SEG[49]	-46.93	-369
116	SEG[50]	-1.93	-369
117	SEG[51]	43.07	-369
118	SEG[52]	88.07	-369
119	SEG[53]	133.07	-369
120	SEG[54]	178.07	-369
121	SEG[55]	223.07	-369
122	SEG[56]	268.07	-369
123	SEG[57]	313.07	-369
124	SEG[58]	358.07	-369
125	SEG[59]	403.07	-369
126	SEG[60]	448.07	-369
127	SEG[61]	493.07	-369
128	SEG[62]	538.07	-369
129	SEG[63]	583.07	-369
130	SEG[64]	628.07	-369
131	SEG[65]	673.07	-369
132	SEG[66]	718.07	-369
133	SEG[67]	763.07	-369
134	SEG[68]	808.07	-369
135	SEG[69]	853.07	-369
136	SEG[70]	898.07	-369
137	SEG[71]	943.07	-369
138	SEG[72]	988.07	-369
139	SEG[73]	1033.07	-369
140	SEG[74]	1078.07	-369
141	SEG[75]	1123.07	-369
142	SEG[76]	1168.07	-369
143	SEG[77]	1213.07	-369
144	SEG[78]	1258.07	-369
145	SEG[79]	1303.07	-369
146	SEG[80]	1348.07	-369
147	SEG[81]	1393.07	-369
148	SEG[82]	1438.07	-369
149	SEG[83]	1483.07	-369
150	SEG[84]	1528.07	-369
151	SEG[85]	1573.07	-369
152	SEG[86]	1618.07	-369
153	SEG[87]	1663.07	-369
154	SEG[88]	1708.07	-369
155	SEG[89]	1753.07	-369
156	SEG[90]	1798.07	-369
157	SEG[91]	1843.07	-369
158	SEG[92]	1888.07	-369
159	SEG[93]	1933.07	-369
160	SEG[94]	1978.07	-369
161	SEG[95]	2023.07	-369
162	SEG[96]	2068.07	-369
163	SEG[97]	2113.07	-369

PAD No.	PIN Name	X	Y
164	SEG[98]	2158.07	-369
165	SEG[99]	2203.07	-369
166	SEG[100]	2248.07	-369
167	COM[9]	2293.07	-369
168	COM[10]	2338.07	-369
169	COM[11]	2383.07	-369
170	COM[12]	2428.07	-369
171	COM[13]	2473.07	-369
172	COM[14]	2518.07	-369
173	COM[15]	2563.07	-369
174	COM[16]	2608.07	-369
175	COMI2	2653.07	-369

PAD CENTER COORDINATES (1-line, SHLC="H")

Unit: um

PAD No.	PIN Name	X	Y
1	XRESET	2543.915	379
2	OSC	2424.915	379
3	VDD	2350.675	379
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11	DB[3]	1581.575	379
12	DB[4]	1508.575	379
13	DB[5]	1389.575	379
14	DB[6]	1316.575	379
15	DB[7]	1197.575	379
16	VSS	1124.575	379
17	VSS	1051.575	379
18	VSS	978.575	379
19	VSS	905.575	379
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22	PS2	638.945	379
23	CLS	519.945	379
24	TEST[0]	447.945	379
25	TEST[1]	298.945	379
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31	VDD	-349.94	379
32	VDD	-422.94	379
33	VDD2	-495.94	379
34	VDD2	-568.94	379
35	VDD2	-641.94	379
36	VOUT	-714.94	379
37	VOUT	-787.94	379
38	VOUT	-860.94	379
39	CAP3P	-933.94	379
40	CAP3P	-1006.94	379
41	CAP1P	-1079.94	379
42	CAP1P	-1152.94	379
43	CAP1N	-1225.94	379
44	CAP1N	-1298.94	379
45	CAP1N	-1371.94	379
46	CAP2P	-1444.94	379
47	CAP2P	-1517.94	379
48	CAP2N	-1590.94	379
49	CAP2N	-1663.94	379
50	CAP4P	-1736.71	379
51	CAP4P	-1809.94	379
52	VRS	-1892.1	379
53	V0	-1965.26	379
54	V1	-2053.56	379

PAD No.	PIN Name	X	Y
55	V2	-2126.56	379
56	V3	-2199.56	379
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58	COM[8]	-2611.93	-369
59	COM[7]	-2566.93	-369
60	COM[6]	-2521.93	-369
61	COM[5]	-2476.93	-369
62	COM[4]	-2431.93	-369
63	COM[3]	-2386.93	-369
64	COM[2]	-2341.93	-369
65	COM[1]	-2296.93	-369
66	COMI1	-2251.93	-369
67	SEG[1]	-2206.93	-369
68	SEG[2]	-2161.93	-369
69	SEG[3]	-2116.93	-369
70	SEG[4]	-2071.93	-369
71	SEG[5]	-2026.93	-369
72	SEG[6]	-1981.93	-369
73	SEG[7]	-1936.93	-369
74	SEG[8]	-1891.93	-369
75	SEG[9]	-1846.93	-369
76	SEG[10]	-1801.93	-369
77	SEG[11]	-1756.93	-369
78	SEG[12]	-1711.93	-369
79	SEG[13]	-1666.93	-369
80	SEG[14]	-1621.93	-369
81	SEG[15]	-1576.93	-369
82	SEG[16]	-1531.93	-369
83	SEG[17]	-1486.93	-369
84	SEG[18]	-1441.93	-369
85	SEG[19]	-1396.93	-369
86	SEG[20]	-1351.93	-369
87	SEG[21]	-1306.93	-369
88	SEG[22]	-1261.93	-369
89	SEG[23]	-1216.93	-369
90	SEG[24]	-1171.93	-369
91	SEG[25]	-1126.93	-369
92	SEG[26]	-1081.93	-369
93	SEG[27]	-1036.93	-369
94	SEG[28]	-991.93	-369
95	SEG[29]	-946.93	-369
96	SEG[30]	-901.93	-369
97	SEG[31]	-856.93	-369
98	SEG[32]	-811.93	-369
99	SEG[33]	-766.93	-369
100	SEG[34]	-721.93	-369
101	SEG[35]	-676.93	-369
102	SEG[36]	-631.93	-369
103	SEG[37]	-586.93	-369
104	SEG[38]	-541.93	-369
105	SEG[39]	-496.93	-369
106	SEG[40]	-451.93	-369
107	SEG[41]	-406.93	-369
108	SEG[42]	-361.93	-369

PAD No.	PIN Name	X	Y
109	SEG[43]	-316.93	-369
110	SEG[44]	-271.93	-369
111	SEG[45]	-226.93	-369
112	SEG[46]	-181.93	-369
113	SEG[47]	-136.93	-369
114	SEG[48]	-91.93	-369
115	SEG[49]	-46.93	-369
116	SEG[50]	-1.93	-369
117	SEG[51]	43.07	-369
118	SEG[52]	88.07	-369
119	SEG[53]	133.07	-369
120	SEG[54]	178.07	-369
121	SEG[55]	223.07	-369
122	SEG[56]	268.07	-369
123	SEG[57]	313.07	-369
124	SEG[58]	358.07	-369
125	SEG[59]	403.07	-369
126	SEG[60]	448.07	-369
127	SEG[61]	493.07	-369
128	SEG[62]	538.07	-369
129	SEG[63]	583.07	-369
130	SEG[64]	628.07	-369
131	SEG[65]	673.07	-369
132	SEG[66]	718.07	-369
133	SEG[67]	763.07	-369
134	SEG[68]	808.07	-369
135	SEG[69]	853.07	-369
136	SEG[70]	898.07	-369
137	SEG[71]	943.07	-369
138	SEG[72]	988.07	-369
139	SEG[73]	1033.07	-369
140	SEG[74]	1078.07	-369
141	SEG[75]	1123.07	-369
142	SEG[76]	1168.07	-369
143	SEG[77]	1213.07	-369
144	SEG[78]	1258.07	-369
145	SEG[79]	1303.07	-369
146	SEG[80]	1348.07	-369
147	SEG[81]	1393.07	-369
148	SEG[82]	1438.07	-369
149	SEG[83]	1483.07	-369
150	SEG[84]	1528.07	-369
151	SEG[85]	1573.07	-369
152	SEG[86]	1618.07	-369
153	SEG[87]	1663.07	-369
154	SEG[88]	1708.07	-369
155	SEG[89]	1753.07	-369
156	SEG[90]	1798.07	-369
157	SEG[91]	1843.07	-369
158	SEG[92]	1888.07	-369
159	SEG[93]	1933.07	-369
160	SEG[94]	1978.07	-369
161	SEG[95]	2023.07	-369
162	SEG[96]	2068.07	-369
163	SEG[97]	2113.07	-369

PAD No.	PIN Name	X	Y
164	SEG[98]	2158.07	-369
165	SEG[99]	2203.07	-369
166	SEG[100]	2248.07	-369
167	NC	2293.07	-369
168	NC	2338.07	-369
169	NC	2383.07	-369
170	NC	2428.07	-369
171	NC	2473.07	-369
172	NC	2518.07	-369
173	NC	2563.07	-369
174	NC	2608.07	-369
175	COMI2	2653.07	-369

PAD CENTER COORDINATES (1-line, SHLC="L")

Unit: um

PAD No.	PIN Name	X	Y
1	XRESET	2543.915	379
2	OSC	2424.915	379
3	VDD	2350.675	379
4	A0(RS)	2276.575	379
5	CSB	2157.575	379
6	/WR(RW)	2084.575	379
7	/RD(E)	1965.575	379
8	DB[0]	1892.575	379
9	DB[1]	1773.575	379
10	DB[2]	1700.575	379
11	DB[3]	1581.575	379
12	DB[4]	1508.575	379
13	DB[5]	1389.575	379
14	DB[6]	1316.575	379
15	DB[7]	1197.575	379
16	VSS	1124.575	379
17	VSS	1051.575	379
18	VSS	978.575	379
19	VSS	905.575	379
20	PS0	830.945	379
21	PS1	711.945	379
22	PS2	638.945	379
23	CLS	519.945	379
24	TEST[0]	447.945	379
25	TEST[1]	298.945	379
26	TEST[2]	223.945	379
27	TEST[3]	48.945	379
28	TEST[4]	-26.055	379
29	TEST[5]	-201.055	379
30	VDD	-276.94	379
31	VDD	-349.94	379
32	VDD	-422.94	379
33	VDD2	-495.94	379
34	VDD2	-568.94	379
35	VDD2	-641.94	379
36	VOUT	-714.94	379
37	VOUT	-787.94	379
38	VOUT	-860.94	379
39	CAP3P	-933.94	379
40	CAP3P	-1006.94	379
41	CAP1P	-1079.94	379
42	CAP1P	-1152.94	379
43	CAP1N	-1225.94	379
44	CAP1N	-1298.94	379
45	CAP1N	-1371.94	379
46	CAP2P	-1444.94	379
47	CAP2P	-1517.94	379
48	CAP2N	-1590.94	379
49	CAP2N	-1663.94	379
50	CAP4P	-1736.71	379
51	CAP4P	-1809.94	379
52	VRS	-1892.1	379
53	V0	-1965.26	379
54	V1	-2053.56	379

PAD No.	PIN Name	X	Y
55	V2	-2126.56	379
56	V3	-2199.56	379
57	V4	-2272.56	379
58	NC	-2611.93	-369
59	NC	-2566.93	-369
60	NC	-2521.93	-369
61	NC	-2476.93	-369
62	NC	-2431.93	-369
63	NC	-2386.93	-369
64	NC	-2341.93	-369
65	NC	-2296.93	-369
66	COMI1	-2251.93	-369
67	SEG[1]	-2206.93	-369
68	SEG[2]	-2161.93	-369
69	SEG[3]	-2116.93	-369
70	SEG[4]	-2071.93	-369
71	SEG[5]	-2026.93	-369
72	SEG[6]	-1981.93	-369
73	SEG[7]	-1936.93	-369
74	SEG[8]	-1891.93	-369
75	SEG[9]	-1846.93	-369
76	SEG[10]	-1801.93	-369
77	SEG[11]	-1756.93	-369
78	SEG[12]	-1711.93	-369
79	SEG[13]	-1666.93	-369
80	SEG[14]	-1621.93	-369
81	SEG[15]	-1576.93	-369
82	SEG[16]	-1531.93	-369
83	SEG[17]	-1486.93	-369
84	SEG[18]	-1441.93	-369
85	SEG[19]	-1396.93	-369
86	SEG[20]	-1351.93	-369
87	SEG[21]	-1306.93	-369
88	SEG[22]	-1261.93	-369
89	SEG[23]	-1216.93	-369
90	SEG[24]	-1171.93	-369
91	SEG[25]	-1126.93	-369
92	SEG[26]	-1081.93	-369
93	SEG[27]	-1036.93	-369
94	SEG[28]	-991.93	-369
95	SEG[29]	-946.93	-369
96	SEG[30]	-901.93	-369
97	SEG[31]	-856.93	-369
98	SEG[32]	-811.93	-369
99	SEG[33]	-766.93	-369
100	SEG[34]	-721.93	-369
101	SEG[35]	-676.93	-369
102	SEG[36]	-631.93	-369
103	SEG[37]	-586.93	-369
104	SEG[38]	-541.93	-369
105	SEG[39]	-496.93	-369
106	SEG[40]	-451.93	-369
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PAD No.	PIN Name	X	Y
109	SEG[43]	-316.93	-369
110	SEG[44]	-271.93	-369
111	SEG[45]	-226.93	-369
112	SEG[46]	-181.93	-369
113	SEG[47]	-136.93	-369
114	SEG[48]	-91.93	-369
115	SEG[49]	-46.93	-369
116	SEG[50]	-1.93	-369
117	SEG[51]	43.07	-369
118	SEG[52]	88.07	-369
119	SEG[53]	133.07	-369
120	SEG[54]	178.07	-369
121	SEG[55]	223.07	-369
122	SEG[56]	268.07	-369
123	SEG[57]	313.07	-369
124	SEG[58]	358.07	-369
125	SEG[59]	403.07	-369
126	SEG[60]	448.07	-369
127	SEG[61]	493.07	-369
128	SEG[62]	538.07	-369
129	SEG[63]	583.07	-369
130	SEG[64]	628.07	-369
131	SEG[65]	673.07	-369
132	SEG[66]	718.07	-369
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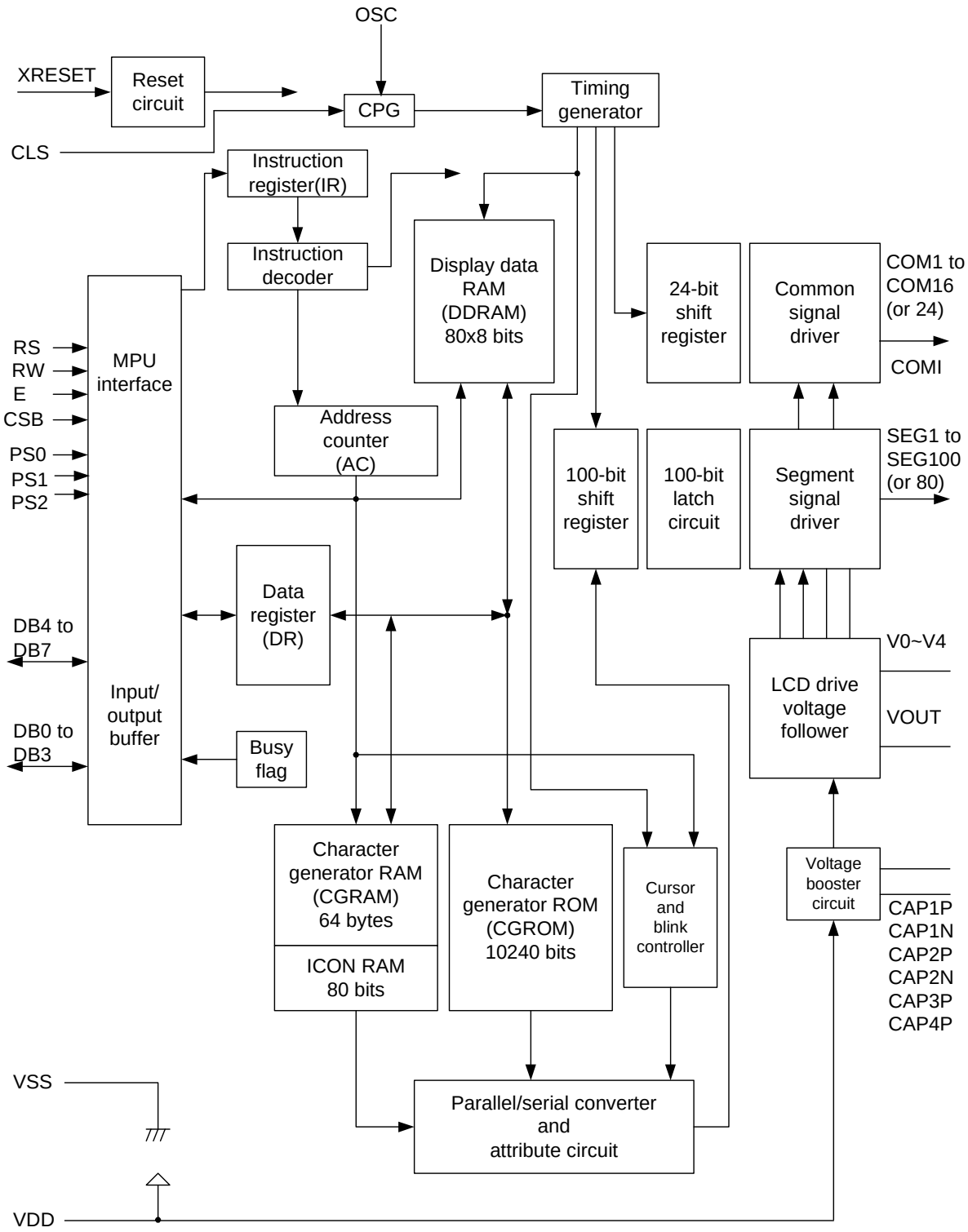
136	SEG[70]	898.07	-369
137	SEG[71]	943.07	-369
138	SEG[72]	988.07	-369
139	SEG[73]	1033.07	-369
140	SEG[74]	1078.07	-369
141	SEG[75]	1123.07	-369
142	SEG[76]	1168.07	-369
143	SEG[77]	1213.07	-369
144	SEG[78]	1258.07	-369
145	SEG[79]	1303.07	-369
146	SEG[80]	1348.07	-369
147	SEG[81]	1393.07	-369
148	SEG[82]	1438.07	-369
149	SEG[83]	1483.07	-369
150	SEG[84]	1528.07	-369
151	SEG[85]	1573.07	-369
152	SEG[86]	1618.07	-369
153	SEG[87]	1663.07	-369
154	SEG[88]	1708.07	-369
155	SEG[89]	1753.07	-369
156	SEG[90]	1798.07	-369
157	SEG[91]	1843.07	-369
158	SEG[92]	1888.07	-369
159	SEG[93]	1933.07	-369
160	SEG[94]	1978.07	-369
161	SEG[95]	2023.07	-369
162	SEG[96]	2068.07	-369
163	SEG[97]	2113.07	-369

PAD No.	PIN Name	X	Y
164	SEG[98]	2158.07	-369
165	SEG[99]	2203.07	-369
166	SEG[100]	2248.07	-369
167	COM[8]	2293.07	-369
168	COM[7]	2338.07	-369
169	COM[6]	2383.07	-369
170	COM[5]	2428.07	-369
171	COM[4]	2473.07	-369
172	COM[3]	2518.07	-369
173	COM[2]	2563.07	-369
174	COM[1]	2608.07	-369
175	COMI2	2653.07	-369

BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Name</th><th>I/O</th><th>Interfaced with</th><th>Function</th></tr>
<tr><td>XRESET</td><td>I</td><td>MPU</td><td>External reset pin.
Low active.</td></tr>
<tr><td>A0(RS)</td><td>I</td><td>MPU</td><td>Register select.
0: Instruction register (for writing)
Busy flag & address counter (for reading)
1: Data register (for write and read)
This Pin must connect to “VDD” when it is not used</td></tr>
<tr><td>/WR(R/W)</td><td>I</td><td>MPU</td><td>8080-series interface (/WR):
Write enable signal input pin (low active).
6800-series interface (R/W):
Select read or write
R/W=0: Write
R/W=1: Read
This Pin must connect to “VDD” when serial mode is selected.</td></tr>
<tr><td>/RD(E)</td><td>I</td><td>MPU</td><td>8080-series interface (/RD):
Read enable signal input pin (low active).
6800-series interface (E):
Data strobe signal input. It starts data read/write (high active).
This Pin must connect to “VDD” when serial mode is selected.</td></tr>
<tr><td>CSB</td><td>I</td><td>MPU</td><td>Chip select in parallel/serial interface (low active). In serial interface, the falling edge of CSB will reset the internal shift register and counter.
This Pin must connect to “VSS” when I^2C mode is selected.</td></tr>
<tr><td rowspan="4">DB7~DB0</td><td rowspan="4">I/O</td><td rowspan="4">MPU</td><td>For parallel 8-bit parallel interface:
DB7~DB0 are 8-bit bi-directional data bus and should be connected to 8-bit data bus of the microprocessor.
When the chip select is not active (CSB=H), DB7~DB0 are high impedance.</td></tr>
<tr><td>For parallel 4-bit parallel interface:
DB7~DB4 are used for data transfer between MPU and ST7038;
DB3~DB0 are not used and must be left OPEN or connected to VDD.</td></tr>
<tr><td>For serial interface (3-line and 4-line):
DB7: serial data input (SI);
DB6: serial clock input (SCL).
DB5~DB0 are not used and must be left OPEN or connected to VDD.</td></tr>
<tr><td>For I^2C interface:
DB7~DB6: slave addresses (SA1~SA0) and must be fixed to “H” or “L”;
DB5~DB3: serial data output (SDA-out);
DB2~DB1: serial data input (SDA-in);
DB0: serial clock input (SCL).
DB1~DB5 must be connected together (SDA).
The ITO resistance on SDA/SCL will form a voltage divider with the pull-up resistor on system. To keep the signal quality better, customers should keep the ITO resistance as low as possible.</td></tr>
<tr><td>PS2~PS0</td><td>I</td><td>MPU</td><td>Parallel / Serial access mode selection
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>Access mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4-line serial MPU interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3-line serial MPU interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>I^2C serial MPU interface</td></tr>
</table></td></tr>
</table>

Name	I/O	Interfaced with	Function
COM1~COM16 (COM1~COM24)	O	LCD	Common driver outputs. Signals that are not used will output the non-selection waveform. For example, COM9 to COM16 output the non-selection waveform in 1-line display mode.
COMI1, COMI2	O	LCD	Common driver outputs for ICON.
SEG1~SEG100 (SEG1~SEG80)	O	LCD	Segment driver outputs. The output map is different from display modes (3-line, 2-line and 1-line) please refer to Table 9 for detailed output map.
CAP1P, CAP2P, CAP3P, CAP4P, CAP1N, CAP2N	Power	Power	For voltage booster circuit (VDD-VSS). External capacitor about 0.1uF~4.7uF.
VOUT	Power	Power	Built-in Voltage Booster output. If using external booster circuit, this pin is used as the power input.
V0~V4	Power	Power	Power supply for LCD drive V0: built-in Voltage Regulator output. If using external regulator circuit, this pin is used as the power input. Internal regulator programmable range: V0 - VSS = 7V (Max); External power endurance: V0 - VSS = 12V (Max). V1~V4: built-in voltage follower outputs. If using external follower circuit, connect the external power to these pins. Please always keep the voltage relation between these pins to be: VOUT > V0 > V1 > V2 > V3 > V4 > VSS
VDD	Power	Power	Power for digital circuits. Connect to 1.8V~3.3V power source.
VDD2	Power	Power	Power for analog circuit. Connect to 1.8V~3.3V power source.
VSS	Power	Power	Ground.
VRS	Power	Power	Reserved to monitor the internal Voltage Regulator reference level. Must be left open.
CLS	I	Option	Select to use internal/external oscillation system. 0: External clock will be input through OSC pin; 1: Using internal clock and the OSC pin must be fixed to VDD.
OSC	I	Oscillation	External clock input pin. If using external clock, connect this pin to the clock source. If using internal clock, connect this pin to VDD.
TEST0~TEST5	-	Test Only	Reserved for testing only. Must be left open.

Notes:

1. Please connect all unused input pins to VDD.
2. The microprocessor interface pins (CSB, /WR, /RD, A0 and D7~D0) should not be left floating in any operation mode.

Recommended ITO Resistance Limitation

PIN Name	ITO Resistance (VDD2 ≥ 2.4V)	ITO Resistance (VDD2 < 2.4V)
PS2~PS0, CLS, OSC[*1]	**No Limitation**	**No Limitation**
TEST0~TEST5, VRS	**Floating**	**Floating**
VDD, VDD2, VSS, VOUT	**<100Ω**	**<80Ω**
A0, /WR(R/W), /RD(E), CSB, DB0~DB7[*2],	**<1KΩ**	**<800Ω**
V0~V4, CAP1P, CAP1N, CAP2P, CAP2N, CAP3P, CAP4P	**<500Ω[*3]**	**<200Ω[*3]**
XRESET	**<10KΩ[*4]**	**<8KΩ[*4]**

Notes:

1. If using internal clock, OSC is connect to VDD and there will be “No Limitation” on its ITO resistance.
   If using external clock, the ITO resistance of OSC should be kept lower than 500Ω to control the clock signal quality.
2. If using I^2C interface mode, the resistance of SDA signal should be lower than 300Ω.
3. To get a better power system efficiency, the recommended ITO resistance value should be lower than 300Ω.

FUNCTION DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

The CSB pin is used for chip selection. ST7038 can interface with an MPU when CSB is "L". When CSB is set to “H”, the control signal inputs, A0, /RD(E) and /WR(R/W), are disabled and DB0 to DB7 are set to be high impedance. When using 3-line or 4-line serial interface, the internal shift register and counter are reset right after the falling edge of CSB.

Parallel / Serial Interface

ST7038 has five interface modes to interface with an MPU, which are three serial interfaces and two parallel interfaces. These interface modes are selected by PS2~PS0 pins as shown below.

Table 1 Parallel / Serial Interface Modes

Parallel / Serial	PS2	PS1	PS0	CSB	Interface Mode
Parallel	L	L	L	CSB	8000-series parallel MPU interface mode
	L	L	H	CSB	6880-series parallel MPU interface mode
Serial	L	H	L	CSB	4-line SPI (Serial Peripheral Interface) mode
	L	H	H	CSB	3-line SPI (Serial Peripheral Interface) mode
	H	L	L	--	I^2C interface mode

Parallel Interface (PS[2:0] = "0, 0, X")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS0 as shown in Table 2. The access type is determined by signals on A0, /RD(E) and /WR(R/W) as shown in Table 3.

Table 2 Microprocessor Selection in Parallel Interface

PS0	CSB	A0	/RD(E)	/WR(R/W)	DB0 to DB7	MPU Type
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series MPU
H	CSB	A0	E	R/W	DB0 to DB7	6800-series MPU

Table 3 Parallel Access

Common	6800-series MPU		8080-series MPU		Description
A0	E	R/W	/RD	/WR	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read status
L	H	L	H	L	Write register (instruction)

Note: By fixing the /RD(E) pin to “H” in 6800-series interface, the CSB pin can be used as the “Enable” signal. In this way, the data is latched at the rising edge of CSB and the access type is determined by the signals A0 and /WR(R/W).

Serial Interface (3-Line / 4-Line / I^2C)

The serial interface mode can be selected by PS2~PS0 as listed below:

Serial mode	PS2	PS1	PS0	CSB	A0
4-Line SPI mode	L	H	L	CSB	A0
3-Line SPI mode	L	H	H	CSB	Not used
I^2C SPI mode	H	L	L	Not Used	Not Used

Note: Please connect the pins which are not used to “H”.

3-Line/4-Line SPI (PS[2:0] = "0, 1, X")

When CSB=”L”, ST7038 is active and the SDA and SCL inputs are enabled. When CSB=”H”, ST7038 is inactive and the internal 8-bit shift register and 3-bit counter are reset. The data/command indication is controlled via the software A0 bit (for 3-Line SPI) or the A0 Pin (for 4-Line SPI). For 4-Line SPI, A0=”H” indicates signal on data bus is display data while A0=”L” indicates signal on data bus is instruction. For 3-Line SPI, the first bit is A0 which indicates the following bits belong to display data or instruction. Serial data will be latched on the rising edge of serial clock. The shift register will collect the serial bits and reformat them to be an 8-bit parallel data at the 8th (4-Line SPI) or 9th (3-Line SPI) serial clock. The DDRAM column address pointer will be increased by one automatically after the 8-bit data is transferred into the DDRAM. The read of data or status (BF and AC) is not allowed in serial interface (neither 3-Line SPI nor 4-Line SPI).

Figure 1 The 4-Line SPI Mode access timing

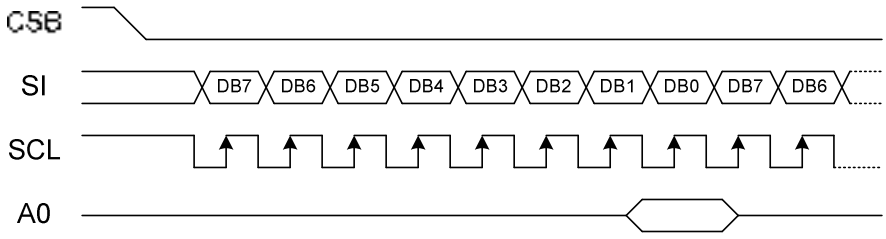
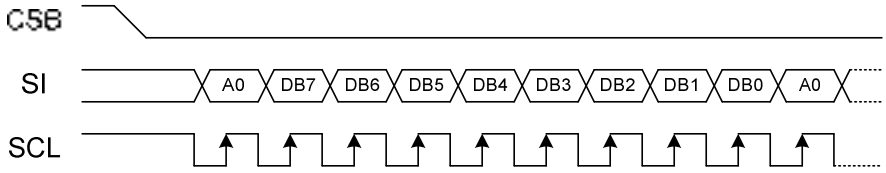


Figure 2 The 3-Line SPI Mode access timing



I²C Interface (PS[2:0] = "1, 0, 0")

The I²C Interface uses two-signal to communicate between different ICs or modules. The two signals are SDA (Serial Data) and SCL (Serial Clock). Both lines must be connected to a pull-up resistor to provide the "H" voltage level. Data transfer may be initiated only when the bus is not busy.

ST7038i support I²C interface with only write function. **Status read or data read is impossible** (except reading the Acknowledge signal). The related signals are listed below:

- SCL: serial clock input
- SDA_IN: serial data input
- SDA_OUT: acknowledge response output
- SA1~SA0: select the slave address and the **available slave addresses are: "0111100" to "0111111".**

- BIT TRANSFER
  One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 3.
- START AND STOP CONDITIONS
  Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition on SDA while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 4.
- SYSTEM CONFIGURATION
  The system configuration of I²C interface is illustrated in Figure 5. The related glossaries are listed below:
  - Transmitter: the device sends the data to the bus
  - Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
  - Slave: the device addressed by a master
  - Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
  - Arbitration: a procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted
  - Synchronization: a procedure to synchronize the clock signals of two or more devices.

- ACKNOWLEDGEMENT

  Acknowledge signal (ACK) is not identical with the Busy Flag (BF) signal in parallel interface. Since internal status cannot be read out, a certain delay is needed before writing the next instructions/data.

  Each byte of 8-bit is followed by an acknowledge bit. To check the acknowledge bit, the transmitter must release SDA to HIGH first and then the master generates an extra acknowledge related clock pulse for the acknowledge bit. A slave receiver which is addressed must generate an acknowledge bit after the reception of each byte. A master receiver must also generate an acknowledge bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the LOW period of the acknowledge clock, so that the SDA is stable LOW during the HIGH period of the acknowledge clock (setup time and hold times must be taken into consideration). Acknowledgement on the I^2C Interface is illustrated in Figure 6.

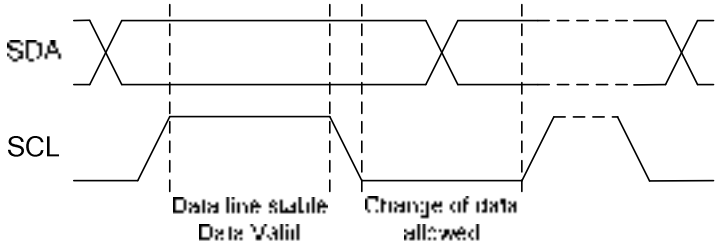


Figure 3 Bit Transfer

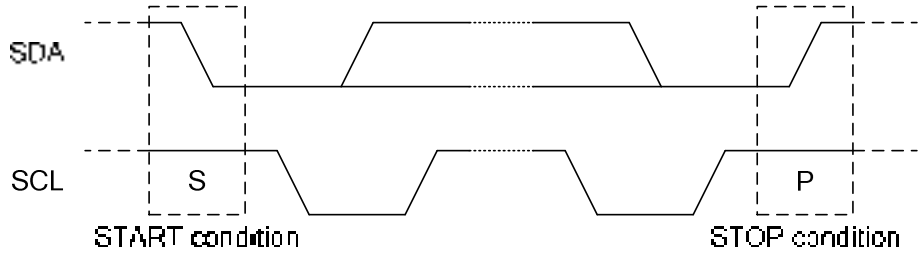


Figure 4 Definition of START and STOP conditions

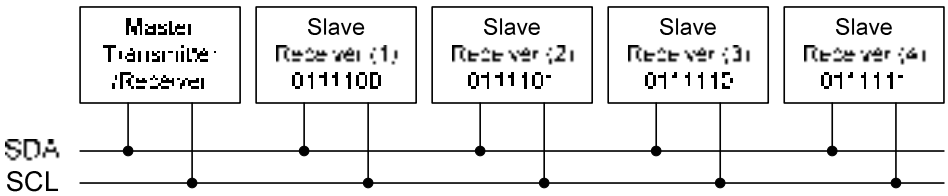


Figure 5 System Configuration

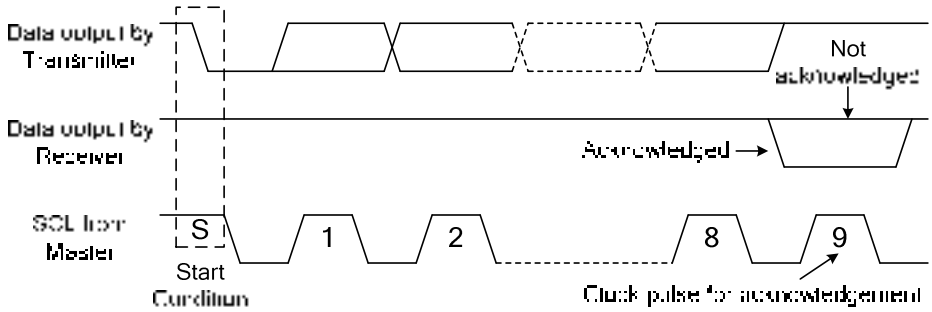


Figure 6 Acknowledgement on the I^2C Interface

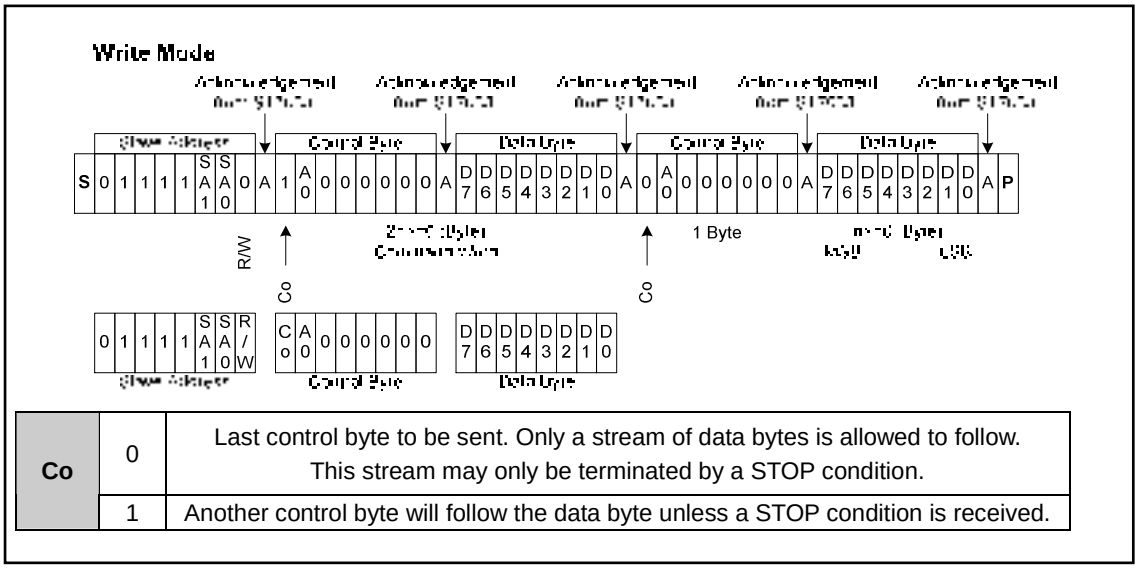
- I²C Interface protocol

  ST7038 receives command/data issued by MPU with correct slave address. Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four kinds of 7-bit slave address (01111**00** to 01111**11**) are reserved for ST7038. The R/W bit is assigned to 0 for write only. The I²C Interface protocol is illustrated in Figure 7.

  The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

  A command word consists of a control byte, which defines Co and A0, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7038i device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I²C INTERFACE-bus master issues a STOP condition (P).

Figure 7 I²C Interface Protocol



Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.

- Data Register and Instruction Register

  During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR).

  The data register (DR) is used as temporary data storage place for being written into internal RAM blocks (DDRAM, CGRAM and ICON RAM). The RAM block is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. That means: after MPU writes data into DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

  The instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot read instruction data back via this register (IR).

  Use the A0 bit in control byte to select the correct register (DR or IR):

Table 4 Operations according to A0 and R/W bits.

A0	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
H	L	Data Write operation (MPU writes data into DR)

Busy Flag (BF)

When BF is "High" (Busy), it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read in parallel interface mode. By issuing A0="Low" and R/W="High" (Read Status operation), BF (Busy Flag) can be checked on DB7. Before executing the next instruction, be sure that BF is not "High".

Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM/ICON RAM address which is transferred from IR. After writing into (reading from) DDRAM/CGRAM/ICON RAM, AC is automatically increased (decreased) by 1. By issuing A0="Low" and R/W="High" (Read Status Operation), AC can be read on DB6 ~ DB0.

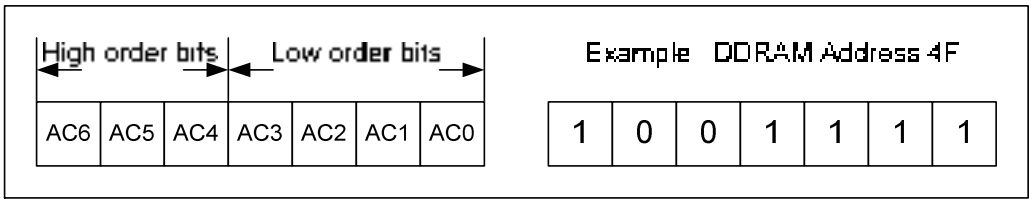


Figure 8 DDRAM Address

Display Data RAM (DDRAM)

Display Data RAM (DDRAM) stores display data represented in 8-bit character codes. Each character code has a unique font stored in the Character Generator ROM (CGROM). The Display Data RAM (DDRAM) capacity is 80 x 8 bits, or 80 characters. The unused area in Display Data RAM (DDRAM) can be used as general data RAM. Please refer to the following sections for the relationships between DDRAM address and display position on the LCD module under different display operation. Please note that: In following demonstration, the DDRAM address in the address counter (AC) is hexadecimal format while the character position is decimal format.

1-LINE DISPLAY (N2=0, N1=0)

In this mode, each line can use 80 RAM-cells to store the display data. The relation between DDRAM address and display position is illustrated in Figure 9. For example, 20 characters are displayed (with 100 segments); the default relation between DDRAM Address and display position is illustrated on the top of Figure 10. When the display shift operation is performed, the relation is changed, just as shown in Figure 10.

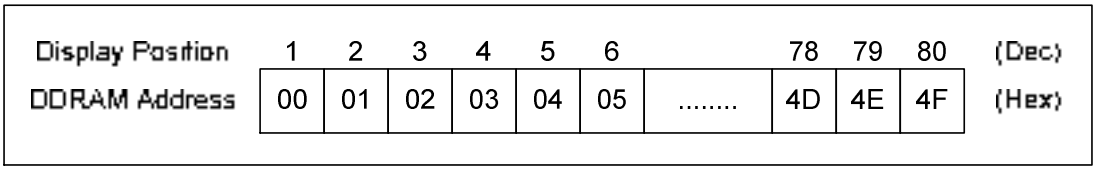


Figure 9 1-Line Display Mode

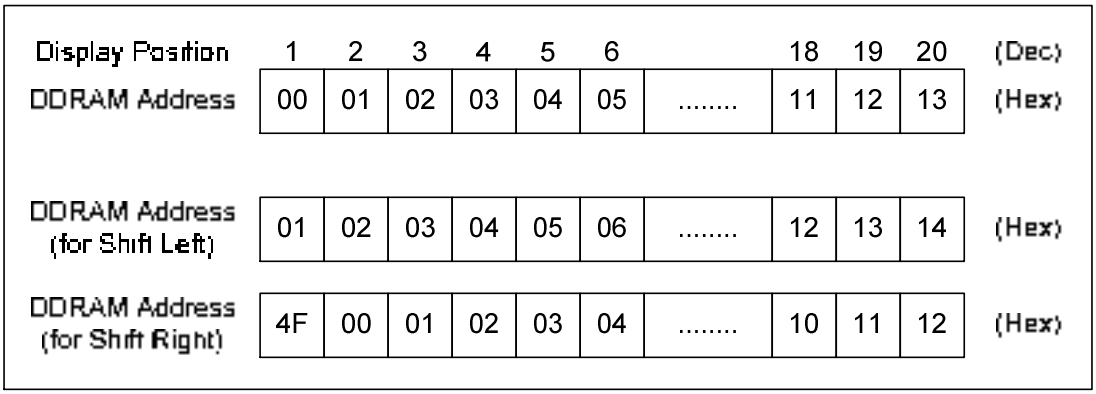


Figure 10 1-Line Display Mode with 20-Character Display

2-LINE DISPLAY (N2=0, N1=1)

In this mode, each line can use 40 RAM-cells to store the display data. The relation between DDRAM address and display position is illustrated in Figure 11 (NOTE: The end address of the first line and the start address of the second line are not consecutive). For example, 20 characters by 2 lines are displayed (with 100 segments); the default relation between DDRAM Address and display position is illustrated on the top of Figure 12. When display shift operation is performed, the relation is changed, just as shown in Figure 12.

Display Position	1	2	3	4	5	6		38	39	40	(Dec)
DDRAM Address	00	01	02	03	04	05	.....	25	26	27	(Hex)
	40	41	42	43	44	45	.....	65	66	67	

Figure 11 2-Line Display Mode

Display Position	1	2	3	4	5	6		18	19	20	(Dec)
DDRAM Address	00	01	02	03	04	05	.....	11	12	13	(Hex)
	40	41	42	43	44	45	.....	51	52	53	
DDRAM Address (FOR Shift Left)	01	02	03	04	05	06	.....	12	13	14	(Hex)
	41	42	43	44	45	46	.....	52	53	54	
DDRAM Address (for Shift Right)	27	00	01	02	03	04	.....	10	11	12	(Hex)
	67	40	41	42	43	44	.....	50	51	52	

Figure 12 2-Line Display Mode with 20-Character Display

3-LINE DISPLAY (N2=1, N1=X)

In this mode, each line can use 16 RAM-cells to store the display data. The relation between DDRAM address and display position is illustrated in Figure 13. For example, 16 characters by 3 lines are displayed (with 80 segments); the default relation between DDRAM Address and display position is illustrated on the top of Figure 14. When display shift operation is performed, the relation is changed, just as shown in Figure 14.

Display Position	1	2	3	4	5	6		14	15	16	(Dec)
DDRAM Address	00	01	02	03	04	05	.....	0D	0E	0F	
	10	11	12	13	14	15	.....	1D	1E	1F	(Hex)
	20	21	22	23	24	25	.....	2D	2E	2F	

Figure 13 3-Line Display Mode

Display Position	1	2	3	4	5	6		14	15	16	(Dec)
DDRAM Address	00	01	02	03	04	05	.....	0D	0E	0F	
	10	11	12	13	14	15	.....	1D	1E	1F	(Hex)
	20	21	22	23	24	25	.....	2D	2E	2F	
DDRAM Address (for Shift Left)	01	02	03	04	05	06	.....	0E	0F	00	
	11	12	13	14	15	16	.....	1E	1F	10	(Hex)
	21	22	23	24	25	26	.....	2E	2F	20	
DDRAM Address (for Shift Right)	0F	00	01	02	03	04	.....	0C	0D	0E	
	1F	10	11	12	13	14	.....	1C	1D	1E	(Hex)
	2F	20	21	22	23	24	.....	2C	2D	2E	

Figure 14 3-Line Display Mode with 16-Character Display

Character Generator ROM (CGROM)

The Character Generator ROM stores 5x8-dot character patterns for 8-bit character codes. It stores 256 5x8-dot character patterns which can be selected by 8-bit character code (Table 5). The first 16 patterns are multiplexed with the Character Generator RAM (CGRAM). By using instruction to set OPR2 & OPR1, customer can use the patterns stored in CGRAM to replace these 16 default patterns. The detailed setting is illustrated in Table 7. User-defined character patterns are also supported by changing the content in mask-programmed ROM. Table 5 illustrated the relation between Character Codes and Character Patterns.

ST7038-0B

Table 5 ROM Table (ROM Code ID: 0B)

Character Generator RAM (CGRAM)

The Character Generator RAM is reserved for customers to rewrite character patterns by program. Total 8 character patterns (each one is 5x8-dot) can be stored in CGRAM. Each byte of CGRAM has 5 bits and a character pattern (5x8-bit) uses 8 bytes to store its pattern. Refer to Table 6 for the relationship among DDRAM data, CGRAM addresses and CGRAM data. Areas that are not used for display can be used as general data RAM (* only 5-bit per byte).

To display the CGRAM Data (customized Character Pattern), write the Character Code (light green part in Table 6) into DDRAM (be sure the OPR2 & OPR1 settings are correct… refer to Table 7).

Display CGRAM Pattern — Generate CGRAM Pattern

Character Code (DDRAM Data)								CGRAM Address (Instruction)						Character Pattern (CGRAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	-*4	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
											0	0	1				0	0	1	0	0
											0	1	0				0	0	1	0	0
											0	1	1				0	0	1	0	0
											1	0	0				0	0	1	0	0
											1	0	1				0	0	1	0	0
											1	1	0				0	0	1	0	0
											1	1	1				0	0	0	0	0
0	0	0	0	-*4	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
											0	0	1				1	0	0	0	1
											0	1	0				1	0	0	0	1
											0	1	1				1	1	1	1	0
											1	0	0				1	0	1	0	0
											1	0	1				1	0	0	1	0
											1	1	0				1	0	0	0	1
											1	1	1				0	0	0	0	0

Table 6 Relationship among CGRAM Address, Character Code (DDRAM Data) & Character Pattern (CGRAM Data)

Notes:

1. Character code bits 2 to 0 are identical with CGRAM address bits 5 to 3 (the red block and red arrow). These 3 bits indicate there are maximum 8 character patterns can be generated by CGRAM.
2. CGRAM address bits 2 to 0 point to the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Try to keep the 8th line data at 0. Otherwise, those pixels with 1 in the 8th line will be turned ON no matter the cursor is ON or OFF.
3. Character pattern row positions correspond to CGRAM data bits 4 to 0 (bit 4 is on the left side).
4. As shown in Table 6, character patterns in CGRAM are selected when character code bits 7 to 4 are all 0 (assume OPR2 & OPR1 setting are correct). However, since character code bit 3 is not used, the “R” pattern in Table 6 can be selected by either character code 01H or 09H.
5. In CGRAM data, “1” corresponds to display selection, “0” to non-selection while “-” indicates no effect.
6. Different CGRAM size can be selected by instruction (OPR2 & OPR1). Please refer to Table 7 and instruction description.

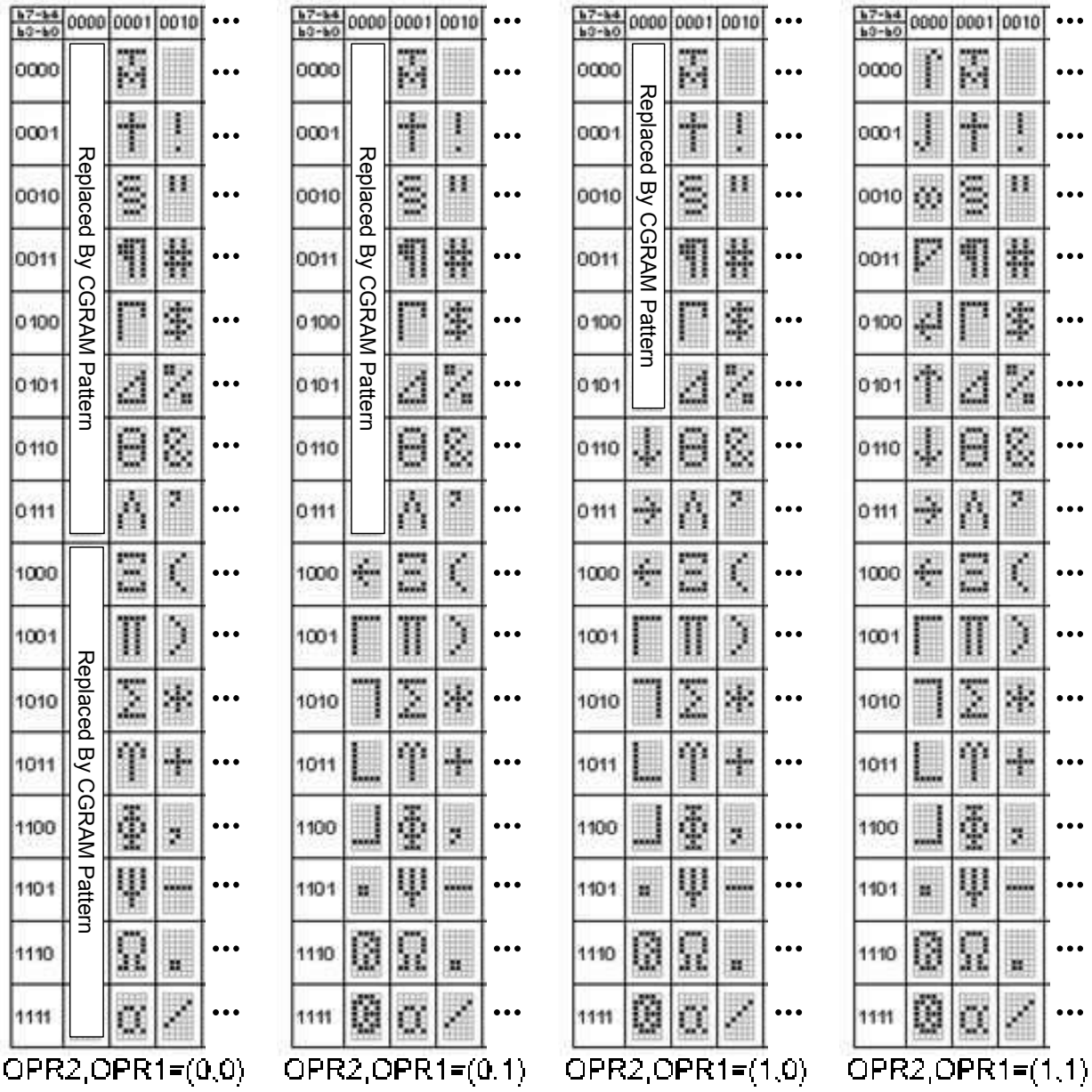


Table 7 Use OPR2 & OPR1 to configure the mapping between CGRAM and CGROM

ICON RAM

There are 80 bits ICON RAM embedded in ST7038. Each bit is mapped to an ICON pixel. Write “1”/”0” into the ICON RAM to control the ICON ON/OFF. Refer to Table 8 for the relationship between ICON RAM address and ICON mapping.

ICON RAM Mapping when SHLS=1:

ICON Address	ICON RAM bits							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	-	-	-	ICON1	ICON2	ICON3	ICON4	ICON5
01H	-	-	-	ICON6	ICON7	ICON8	ICON9	ICON10
02H	-	-	-	ICON11	ICON12	ICON13	ICON14	ICON15
03H	-	-	-	ICON16	ICON17	ICON18	ICON19	ICON20
04H	-	-	-	ICON21	ICON22	ICON23	ICON24	ICON25
05H	-	-	-	ICON26	ICON27	ICON28	ICON29	ICON30
06H	-	-	-	ICON31	ICON32	ICON33	ICON34	ICON35
07H	-	-	-	ICON36	ICON37	ICON38	ICON39	ICON40
08H	-	-	-	ICON41	ICON42	ICON43	ICON44	ICON45
09H	-	-	-	ICON46	ICON47	ICON48	ICON49	ICON50
0AH	-	-	-	ICON51	ICON52	ICON53	ICON54	ICON55
0BH	-	-	-	ICON56	ICON57	ICON58	ICON59	ICON60
0CH	-	-	-	ICON61	ICON62	ICON63	ICON64	ICON65
0DH	-	-	-	ICON66	ICON67	ICON68	ICON69	ICON70
0EH	-	-	-	ICON71	ICON72	ICON73	ICON74	ICON75
0FH	-	-	-	ICON76	ICON77	ICON78	ICON79	ICON80

ICON RAM Mapping when SHLS=0:

ICON Address	ICON RAM bits							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	-	-	-	ICON80	ICON79	ICON78	ICON77	ICON76
01H	-	-	-	ICON75	ICON74	ICON73	ICON72	ICON71
02H	-	-	-	ICON70	ICON69	ICON68	ICON67	ICON66
03H	-	-	-	ICON65	ICON64	ICON63	ICON62	ICON61
04H	-	-	-	ICON60	ICON59	ICON58	ICON57	ICON56
05H	-	-	-	ICON55	ICON54	ICON53	ICON52	ICON51
06H	-	-	-	ICON50	ICON49	ICON48	ICON47	ICON46
07H	-	-	-	ICON45	ICON44	ICON43	ICON42	ICON41
08H	-	-	-	ICON40	ICON39	ICON38	ICON37	ICON36
09H	-	-	-	ICON35	ICON34	ICON33	ICON32	ICON31
0AH	-	-	-	ICON30	ICON29	ICON28	ICON27	ICON26
0BH	-	-	-	ICON25	ICON24	ICON23	ICON22	ICON21
0CH	-	-	-	ICON20	ICON19	ICON18	ICON17	ICON16
0DH	-	-	-	ICON15	ICON14	ICON13	ICON12	ICON11
0EH	-	-	-	ICON10	ICON9	ICON8	ICON7	ICON6
0FH	-	-	-	ICON5	ICON4	ICON3	ICON2	ICON1

Table 8 ICON RAM Address and ICON Mapping

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as: DDRAM, CGROM and CGRAM. RAM read timing for display and RAM access timing for MPU are generated separately so that the interfering with each other can be avoided. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in the whole display area.

LCD Driver Circuit

ST7038 LCD Driver Circuit has 3 kinds of output mode: 8+1 common outputs, 16+1 common outputs and 24+1 common outputs. Besides, ST7038 also support horizontal and vertical mirror feature. Please refer to for the relationship of Pin Number and Pin Function.

Table 9 Pin Number vs. Pin Function in different display mode

Display setting			COM	PAD	PAD	PAD	PAD	PAD	PAD	PAD	PAD	PAD	PAD
Line	DH	SHLC	Rows	66	65~58	67~71	72~76	77~156	157~162	163~166	167~174	175	No.
1	0	1	8+1	COMI1	COM [1:8]	SEG [1:5]	SEG [6:10]	SEG [11:90]	SEG [91:96]	SEG [97:100]	**NC**	COMI2	Output (Pin Function)
		0			**NC**						COM [8:1]		
1	1	1	16+1		COM [1:8]						COM [9:16]		
2	0	0			COM [16:9]						COM [8:1]		
2	1	1	24+1	**NC**	COM [5:12]	COM[4:1] + COMI1	**NC**	SEG [1:80]	**NC**	COM [13:16]	COM [17:24]		
		0			COM [20:13]	COM[21:24] + COMI1				COM [12:9]	COM [8:1]		
3	0	1			COM [5:12]	COM[4:1] + COMI1				COM [13:16]	COM [17:24]		
		0			COM [20:13]	COM[21:24] + COMI1				COM [12:9]	COM [8:1]		

Note:

1. SHLC=1: COM scan direction is normal;
   SHLC=0: COM scan direction is reversed.
   * Pin definition of COM is changed when SHLC=0.
2. ICON COM (COMI1/COMI2) scan direction will never be changed (always the last).
3. SHLS=1: SEG scan direction is normal (SEG1~SEG100 or SEG1~SEG80);
   SHLS=0: SEG scan direction is reversed (SEG100~SEG1 or SEG80~SEG1).
   * Pin definition of SEG is NOT changed when SHLS=0

Cursor and Blink Control Circuit

ST7038 can generate the cursor and blink effects with built-in cursor/blink control circuit. The cursor or blink effect will appear at the current DDRAM display position which is kept in the AC (Address Counter).

INSTRUCTIONS

Instruction	Instruction Code										Description	Execution Time		
	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 260.4K Hz	OSC= 284.1K Hz	OSC= 531.1K Hz
Default Instruction Table (IS[1:0]: Don't Care)														
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to clear DDRAM and set AC to "00H".	1.8 ms	1,6 ms	1ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set AC to "00H". It will return cursor to the original position if shifted. The contents in DDRAM are not changed.	93 us	85 us	70 us
Set Entry Mode	0	0	0	0	0	0	0	1	I/D	S	Set cursor move direction and display shift direction. The effects are performed after each data access (write or read).	93 us	85 us	70 us
Display Control	0	0	0	0	0	0	1	D	C	B	D=1: Entire display on; C=1: Cursor on; B=1: Cursor position on.	93 us	85 us	70 us
Function Set	0	0	0	0	1	DL	X	X	IS1	IS0	DL: Interface data is 8/4 bits; IS[1:0]: select instruction table.	93 us	85 us	70 us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address into AC (address counter).	93 us	85 us	70 us
Read Status	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Before next access, Check BF will know if the internal operation is finished or not. The contents of AC (address counter) can also be read.	0	0	0
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	93 us	85 us	70 us
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	93 us	85 us	70 us
Instruction table 0: IS[1:0]=(0,0)														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C and R/L: Immediately move cursor or shift display by 1.	93 us	85 us	70 us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address into AC (address counter)	93 us	85 us	70us

Instruction table 1: IS[1:0]=(0,1)														
Follower Control	0	0	0	0	0	1	BS2	BS1	OPF2	OPF1	BS2~1: Bias select; OPF2~1: Select built-in voltage follower circuit.	93 us	85 us	70us
Set ICON RAM Address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address into AC (address counter).	93 us	85 us	70 us
V0 Control 1	0	0	0	1	0	1	PD	VC6	VC5	VC4	PD: Power down; VC6~4: Set V0 (High-nibble).	93us	85us	70us
ICON/Power Control	0	0	0	1	1	0	Ion	Bon	Ron	Fon	Ion: ICON display on/off; Bon: Set booster circuit on/off; Ron: Set regulator circuit on/off; Fon: Set follower circuit on/off.	93 us	85 us	70 us
V0 Control 2	0	0	0	1	1	1	VC3	VC2	VC1	VC0	Set V0 (Low-nibble).	93 us	85 us	70 us
Instruction table 2: IS[1:0]=(1,0)														
Set Display Mode	0	0	0	0	0	1	UD	DH	N2	N1	UD: Double Height Position (DHu or DHd); DH: Double Height; N2, N1: Display line number.	93 us	85 us	70 us
Select CGRAM & COM/SEG direction	0	0	0	1	0	0	OPR2	OPR1	SHLS	SHLC	OPR2~1: CGRAM mapping select SHLS: Set SEG scan direction SHLC: Set COM scan direction	93 us	85 us	70 us
Set Frame Rate	0	0	0	1	0	1	0	FR2	FR1	FR0	FRC2~0: Select Frame Rate	93 us	85 us	70 us

INSTRUCTION DESCRIPTION

IS[1:0]: Don't Care

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address. Then set DDRAM address "00H" into AC (address counter). This (AC=00H) will return cursor to the original position, namely, bring the cursor to the left edge on first line of the display. Besides, this instruction also reset the entry mode to be "increment" (I/D = "1").

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

By setting DDRAM address "00H" into AC (address counter), this instruction returns the cursor back to its "Home" position (original position or the left edge on the first line). This instruction not only returns cursor to its original position but also returns the display to its original setting, if it is shifted. Contents in DDRAM are not changed.

Set Entry Mode

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display. After each data access, the cursor and display will be moved or shifted according to I/D-bit and S-bit.

- I/D: Increment / decrement of DDRAM address (cursor/blink) after each byte data access.
  I/D = "1", cursor/blink moves to right and DDRAM address is increased by 1.
  I/D = "0", cursor/blink moves to left and DDRAM address is decreased by 1.
  * CGRAM operation is the same as DDRAM. CGRAM address is automatically adjusted according I/D bit after each byte access.
- S: Shift of entire display.
  When writes to DDRAM and the S bit is "H", the "Screen" (entire display) shifts instead of the cursor moves. The shift direction is controlled by the I/D-bit after each byte wrote:
  I/D = "1", display shift left;
  I/D = "0", display shift right.
  When reads from DDRAM (CGRAM: read/write) or the S bit is "L", the shift of entire display is not performed.
  * CGRAM operation is not affected by this feature.
  Refer to Figure 10, Figure 12, Figure 14 and the following table for detailed information.

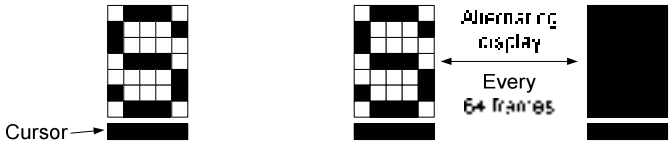
S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

Display Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Set Display and Cursor mode.

- D: Display ON/OFF control bit.
  D = "1", the display is turned on.
  D = "0", the display is turned off, but display data is remained in DDRAM.
- C: Cursor ON/OFF control bit.
  C = "1", cursor is turned on.
  C = "0", cursor is disappeared from current display, but I/D register remains its data.
- B: Cursor Blink ON/OFF control bit.
  B = "1", cursor blink is on. The display on the cursor position will alternate between all-black and the character.
  B = "0", blink is off.



Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	X	X	IS1	IS0

- DL: Interface data length control bit. It selects parallel 8-bit or 4-bit interface mode.
  When DL = "1", use parallel 8-bit bus to communicate with MPU.
  When DL = "0", use parallel 4-bit bus to communicate with MPU.
  When using parallel 4-bit bus mode, each instruction needs to be transfer twice, including this instruction.
- IS[1:0]: Selects instruction table.
  When IS[1:0]=(0,0): Normal instruction is selected(refer instruction table 0).
  When IS[1:0]=(0,1): Extension instruction is selected(refer instruction table 1).
  When IS[1:0]=(1,0): Extension instruction is selected(refer instruction table 2).
  When IS[1:0]=(1,1): Do not use !!

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction sets DDRAM address into AC. This instruction makes DDRAM data available for MPU access.

- N2=0, N1=0: 1-Line display mode, the valid DDRAM address is from "00H" to "4FH".
- N2=0, N1=1: 2-Line display mode, the valid DDRAM address will be:
  1st Line: "00H" to "27H";
  2nd Line: “40H" to "67H".
- N2=1, N1=don’t care: 3-Line display mode, the valid DDRAM address will be:
  1st Line: “00H” to “0FH”;
  2nd Line: “10H” to “1FH”;
  3rd Line: “20H” to “2FH”.

Read Status

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

BF: Busy Flag

When BF is "H", it indicates that the internal operation is processing. So the next instruction(s) cannot be accepted until BF="L". Be sure to check BF bit before issuing next instruction. In serial interface mode (including I^2C mode), please use delay to avoid the next instruction conflict with the internal operation.

AC: Address Counter

In parallel interface modes the Address Counter (AC) can be read by MPU on DB6~DB0. The AC stores DDRAM/CGRAM address which is transferred from IR. After each byte access (read/write) with DDRAM/CGRAM, AC is adjusted by 1 automatically (increase or decrease is controlled by the setting of Entry Mode).

Write Data to CGRAM, DDRAM or ICON RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

This operation writes binary 8-bit data to CGRAM, DDRAM or ICON RAM. The selection of RAM (DDRAM, CGRAM or ICON RAM) is controlled by the previous "Set xxxxx Address" instruction (Set DDRAM Address, Set CGRAM Address, Set ICON RAM Address).

RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is adjusted by 1 automatically (increase or decrease is controlled by the setting of Entry Mode).

Read Data from DDRAM, CGRAM or ICON RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

This operation reads binary 8-bit data from DDRAM, CGRAM or ICON RAM. The selection of RAM (DDRAM, CGRAM or ICON RAM) is controlled by the previous "Set xxxxx Address" instruction. Make sure the selected RAM (DDRAM, CGRAM or ICON RAM) is correct before read data operation.

Instruction Table 0, IS[1:0]=(0,0)

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

This instruction is different from the "Entry Mode Set" instruction. The shift is performed immediately right after receiving this instruction. The data search or data correction in applications can be easily achieved by using screen and cursor shift.

S/C	R/L	Description	AC Value
L	L	Shift cursor left.	AC=AC-1
L	H	Shift cursor right.	AC=AC+1
H	L	Shift Screen (current display) left. Cursor follows the screen to shift left.	AC=AC
H	H	Shift Screen (current display) right. Cursor follows the screen to shift right.	AC=AC

- S/C: Selects Cursor or Screen to perform the shift function.
  S/C="H": The Screen (current display) is selected to shift. The direction is controlled by R/L bit;
  S/C="L": The Cursor is selected to shift. The direction is controlled by R/L bit.
- R/L: Selects the shift direction.
  R/L="H": The shift direction is toward Right;
  R/L="L": The shift direction is toward Left.

Cursor Shift

When display line mode is more than 1-Line, the cursor will move to the first position on the next line if AC reaches the last valid address. If the line address is at the last line, the cursor will shift to the first position on the first line.

Screen Shift

The screen shift is performed simultaneously on each line in all kinds of display line mode. Each line is shifted individually. The content kept in AC is not changed when performing Screen Shift operation.

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

This instruction sets CGRAM address into AC. This instruction makes CGRAM data available for MPU access.

Instruction Table 1, IS[1:0]=(0,1)

Follower Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	BS2	BS1	OPF2	OPF1

BS[2:1]	Bias level selection
(0,0)	Select 1/4 Bias
(0,1)	Select 1/5 Bias
(1,0)	Select 1/6 Bias
(1,1)	Select 1/7 Bias
OPF[2:1]	Follower circuit selection
(0,0)	Select built-in Follower
(0,1)	Select built-in bias resistor (9.9K)
(1,0)	Select built-in bias resistor (3.3K)
(1,1)	Select external bias circuit (built-in Follower is OFF)

Set ICON RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	AC3	AC2	AC1	AC0

This instruction sets ICON RAM address into AC. This instruction makes ICON data available for MPU access. The valid ICON RAM address is from "00H" to "0FH", when IS[1:0]=(0,1).

V0 Control 1 & 2

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	0	1	PD	VC6	VC5	VC4	V0 Control 1
0	0	0	1	1	1	VC3	VC2	VC1	VC0	V0 Control 2

- PD: Set Power Down Mode ON/OFF.
  PD="H": Enter Power Down Mode;
  PD="L": Exit Power Down Mode.
- VC[6:0]: Set V0 voltage. Please refer to "POWER SUPPLY FOR LCD " section for more detailed information.

VC6	VC5	VC4	VC3	VC2	VC1	VC0	V0 (V)
0	0	0	0	0	0	0	2.940
0	0	0	0	0	0	1	2.975
0	0	0	0	0	1	0	3.010
0	0	0	0	0	1	1	3.045
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	7.280
1	1	1	1	1	0	1	7.315
1	1	1	1	1	1	0	7.350
1	1	1	1	1	1	1	7.385

ICON/Power Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	I_{ON}	B_{ON}	R_{ON}	F_{ON}

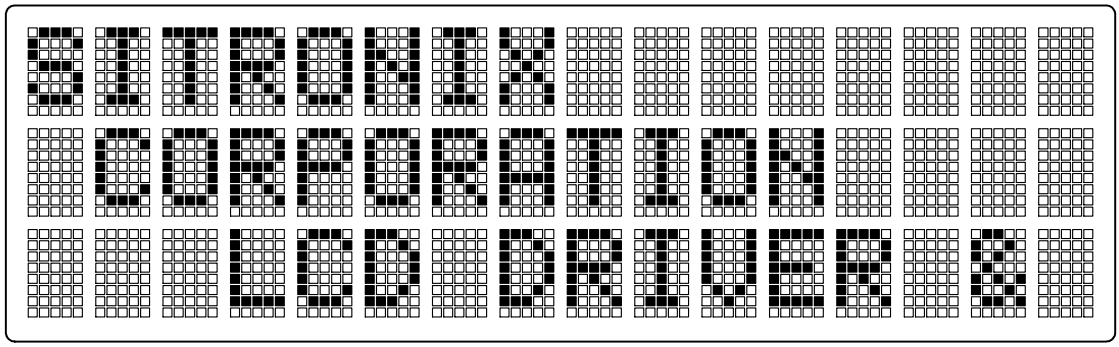
Setting	I_{ON}	B_{ON}	R_{ON}	F_{ON}
H	ICON display: ON	Built-in Booster: ON	Built -in Regulator: ON	Built -in Follower: ON
L	ICON display: OFF	Built -in Booster: OFF	Built -in Regulator: OFF	Built -in Follower: OFF

Instruction Table 2, IS[1:0]=(1,0)

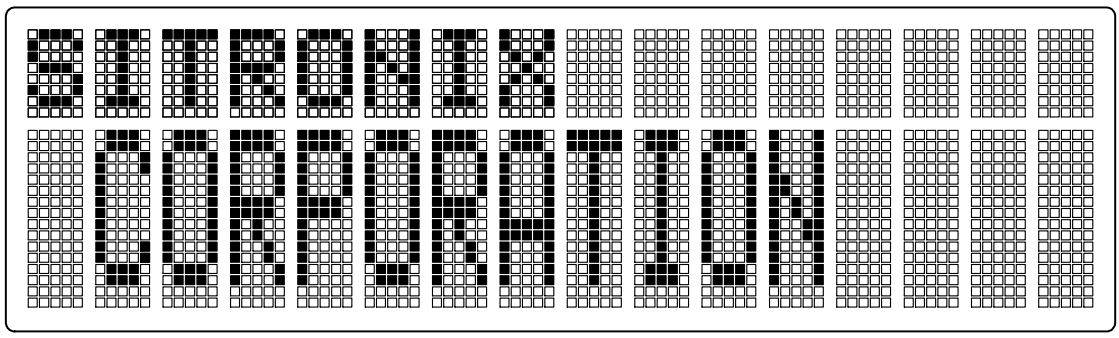
Set Display Mode

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	UD	DH	N2	N1

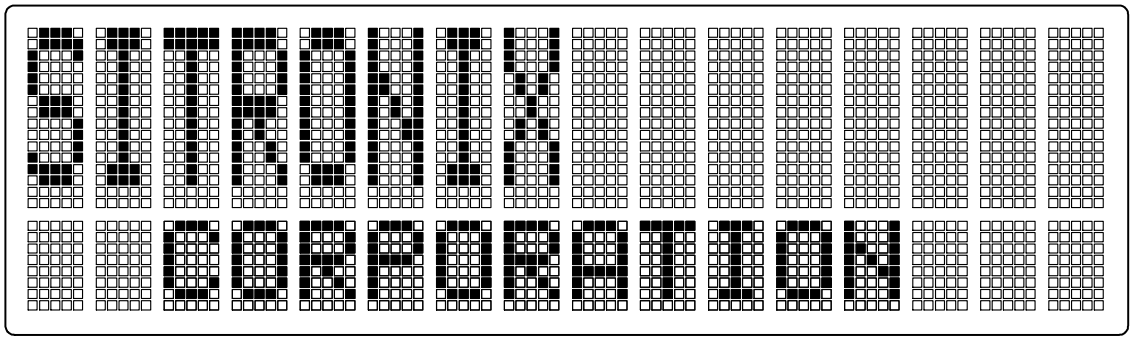
- UD: Select double height font display position on screen. This bit is only valid when N2=0, N1=1 and DH=1.
  UD="H": Double height font is displayed on COM1~COM16;
  UD="L": Double height font is displayed on COM9~COM24.



DH=0, N2=1 & UD=X (don`t care): 3-Line normal display mode



DH=1, N2=0, N1=1 & UD=0: COM1~8 is normal, COM9~24 is double height

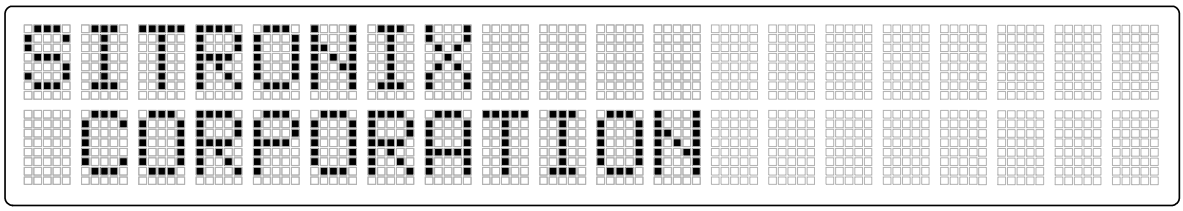


DH=1, N2=0, N1=1 & UD=1: COM17~24 is normal,COM1~16 is double height

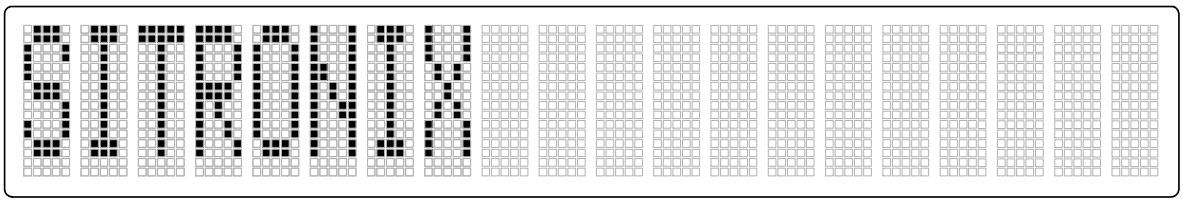
- DH: Display double height font (5X16 dot-matrix) control bit.
  Please refer to the following table for detailed setting and description.

DH	UD	N2=0, N1=0 (1-Line)	N2=0, N1=1 (2-Line)	N2=1, N1=X (3-Line)
L	X	Normal Display DDRAM: 00H~4FH	Normal Display DDRAM: 00H~27H	Normal Display DDDRAM: 00H~0FH
H	H	Double Height (COM1~16) DDRAM: 00H~27H	COM1~16: Double Height COM17~24: Normal Display DDDRAM: 00H~0FH	Do NOT use
H	L		COM1~8: Normal Display COM9~24: Double Height DDDRAM: 00H~0FH	

For example, the normal height font and the doubled height font are shown as below.



2 line mode normal display (DH=0, N2=0, N1=1)



1 line mode with double height font (DH=1, N2=0, N1=0)

- N[2,1]: Control the “Display Line Number”.

  ST7038 has 17-common and 100-segment LCD driving signals as default. If operated in 1-Line Display mode, the used common pads are COM1~COM8 and COMI (for ICON). If operated in 3-Line Display mode, some segments will be used as commons. Please refer to Table 9 or the “Pad Location Coordinates” section for more detailed information.

N2	N1	Display Mode
0	0	1-Line Display mode
0	1	2-Line Display mode
1	X	3-Line Display mode

Table 10 N[2,1] vs. Display Line Number

- Complete Display Modes:

UD	DH	N2	N1	Display Mode Description	Duty
X	0	0	0	1-Line Display mode	1/(8+1)
X	1	0	0	1-Line Display mode, double height	1/(16+1)
X	0	0	1	2-Line Display mode	1/(16+1)
1	1	0	1	2-Line Display mode, double height (UP)	1/(24+1)
0	1	0	1	2-Line Display mode, double height (DOWN)	1/(24+1)
X	X	1	X	3-Line Display mode	1/(24+1)

Select CGRAM & COM/SEG direction

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	OPR2	OPR1	SHLS	SHLC

- OPR2, OPR1:

  Select CGROM size. The CGROM stores 256 characters. The first 16 characters can be replaced by CGRAM data (customized pattern). By setting OPR2 and OPR1, the CGROM pattern will be changed as shown in Table 7. The used character numbers are shown below:

OPR2	OPR1	CGROM	CGRAM
0	0	240	8
0	1	248	8
1	0	250	6
1	1	256	0

- SHLS: (Pin definition is NOT changed when SHLS=0)
  SHLS=1: SEG1~100 ←Column address 0~99 (Normal)
  SHLS=0: SEG100~1 ←Column address 99~0 (Invert)
  * Pin definition of SEG is NOT changed when SHLS=0
  * 3-Line Display Mode uses only 80 segments.
- SHLC: (Pin definition is changed when SHLC=0)
  SHLC=1: COM1~24 ←Row address 0~23 (Normal)
  SHLC=0: COM1~24 ←Row address 23~0 (Invert)
  * Pin definition of COM is changed when SHLC=0
  * Please refer to Table 9 for the detailed output map.

Set Frame Rate

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	FR2	FR1	FR0

FR[2:0]: Set Frame Rate according the table below:

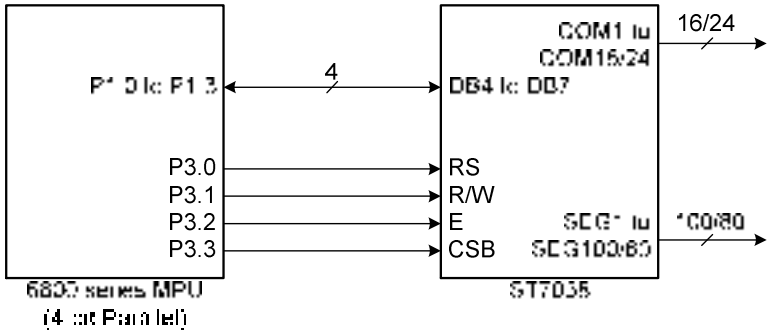
FR2	FR1	FR0	Frame Rate (Hz)
0	0	0	65.35±15%
0	0	1	68.03±15%
0	1	0	70.92±15% (Default)
0	1	1	74.07±15%
1	0	0	77.52±15%
1	0	1	111.1±15%
1	1	0	120.5±15%
1	1	1	131.6±15%

MPU INTERFACE

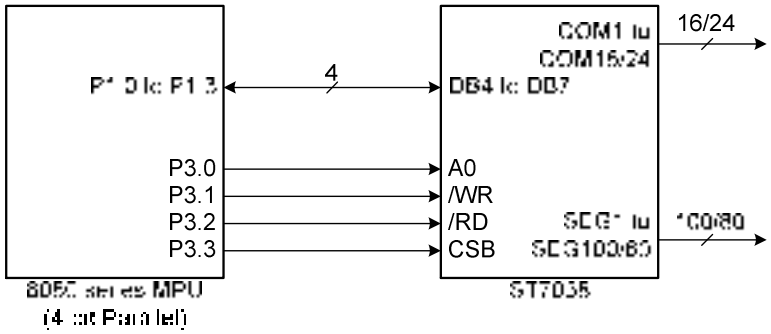
The ST7038 supports various kinds of MPU interface to communicate with MPU: Parallel 4-bit 6800/8080-series, Parallel 8-bit 6800/8080-series, Serial 3/4-Line SPI and I^2C operation. The following figures are referential circuits connected with different kinds of MPU.

The microprocessor interface pins (CSB, /WR, /RD, A0 and D7~D0) should not be left floating in any operation mode.

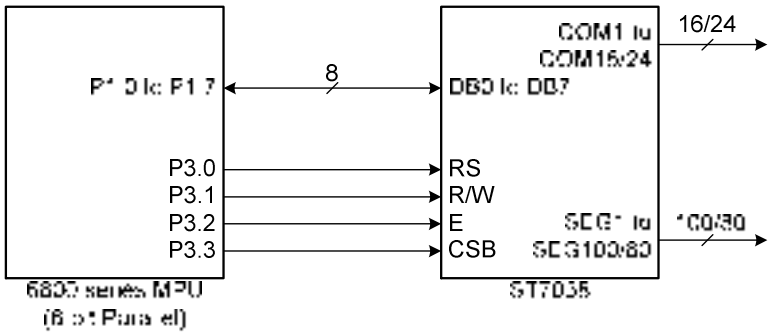
- Intel 8051 interface: 4-Bit parallel (6800-series)



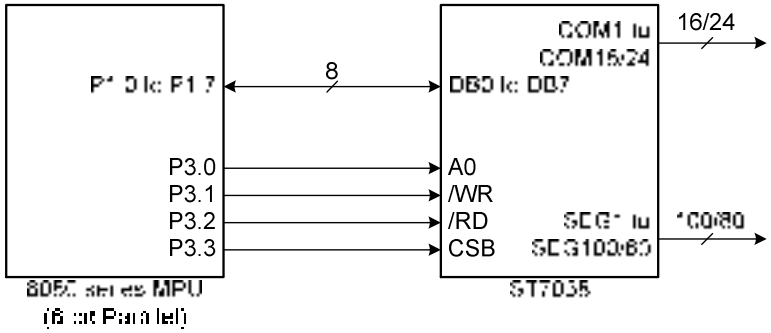
- Intel 8051 interface: 4 Bit parallel (8080-series)



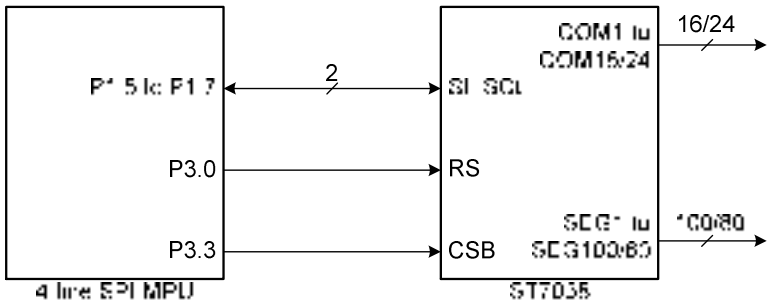
- Intel 8051 interface: 8 Bit parallel (6800-series)



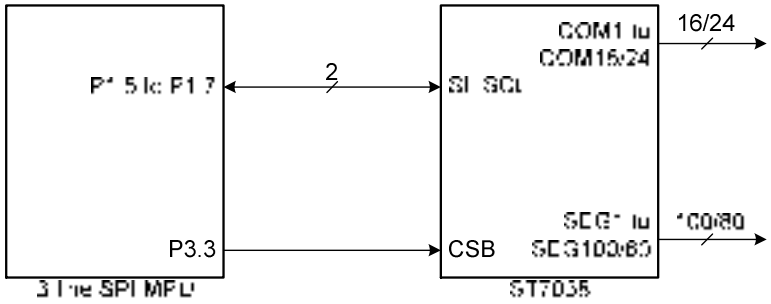
- Intel 8051 interface: 8 Bit parallel (8080-series)



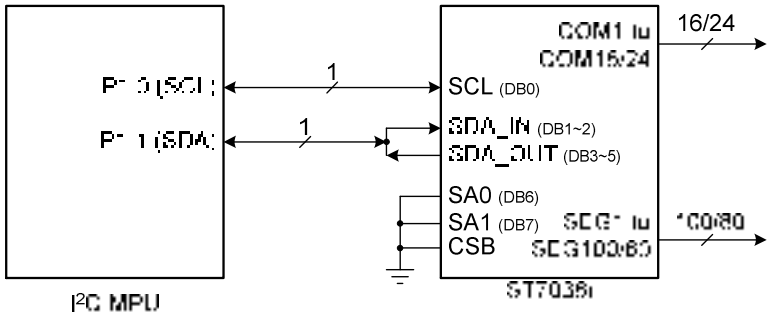
- Intel 8051 interface: Serial 4-line SPI



- Intel 8051 interface: Serial 3-line SPI

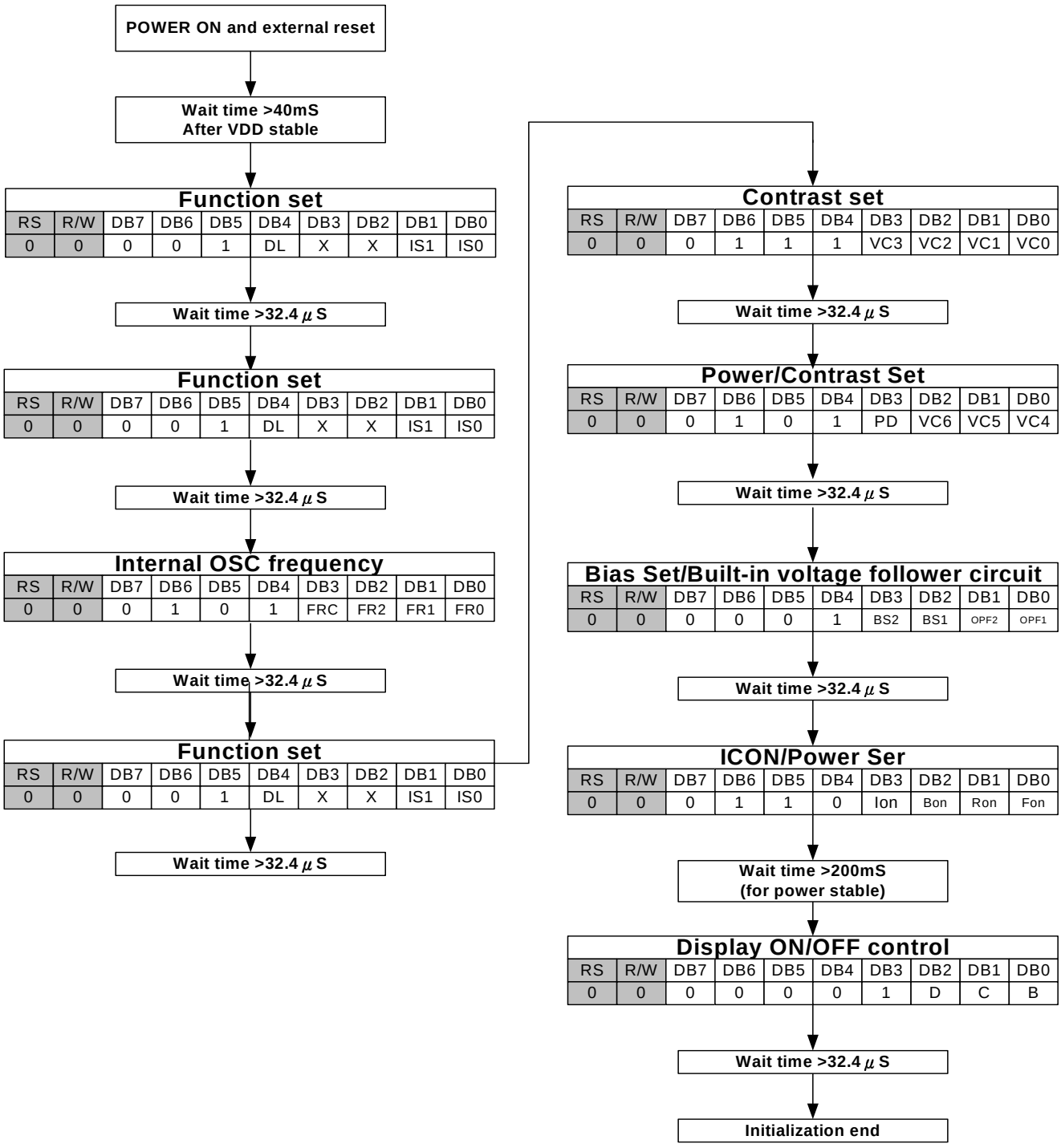


- Intel 8051 interface: Serial I^2C



INITIALIZATION

Initial Flow



Initial Code (8051 MPU, Parallel 8-bit Interface)

```
;-------------------------------------------------------------------------------
INITIAL_START:
CALL    HARDWARE_RESET
CALL    DELAY40mS
MOV     A,#32H                  ;FUNCTION SET
CALL    WRINS_NOCHK     ;8 bit,
CALL    DELAY40uS
MOV     A,#32H                  ;FUNCTION SET
CALL    WRINS_NOCHK     ;8 bit,
CALL    DELAY40uS
MOV     A,#54H                  ;Internal  OSC  frequency
adjustment
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#31H                  ;FUNCTION SET
CALL    WRINS_CHK       ;8 bit,
CALL    DELAY40uS
MOV     A,#7FH                  ;Contrast set
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#53H                  ;Power down/Contrast set
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#14H                  ; Bias/Follwer set
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#67H                  ; ICON/Power(B,R,F) set
CALL    WRINS_CHK

CALL    DELAY200mS      ;for power stable
MOV     A,#0CH                  ;DISPLAY ON
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#01H                  ;CLEAR DISPLAY
CALL    WRINS_CHK
CALL    DELAY2mS
;-------------------------------------------------------------------------------
MAIN_START:
XXXX
XXXX
XXXX
;-------------------------------------------------------------------------------
WRINS_CHK:
CALL    CHK_BUSY
WRINS_NOCHK:
CLR     RS                      ;EX:Port 3.0
CLR     RW                      ;EX:Port 3.1
SETB    E               ;EX:Port 3.2
MOV     P1,A                    ;EX:Port 1=Data Bus
CLR     E
MOV     P1,#FFH         ;For Check Busy Flag
RET
;-------------------------------------------------------------------------------
CHK_BUSY:                       ;Check Busy Flag
CLR     RS
SETB    RW
SETB    E
JB      P1.7,$
CLR     E
RET
```

Initial Code (8051 MPU, Serial 4-line SPI Interface)

```
;---------------------------------------------------------------------
INITIAL_START:
INITIAL_START:
CALL    HARDWARE_RESET
CALL    DELAY40mS
MOV     A,#22H                  ;FUNCTION SET
CALL    WRINS_NOCHK             ;8 bit,
CALL    DELAY40uS
MOV     A,#22H                  ;FUNCTION SET
CALL    WRINS_NOCHK     ;8 bit,
CALL    DELAY40uS
MOV     A,#54H                      ;Internal  OSC  frequency
adjustment
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#21H                  ;FUNCTION SET
CALL    WRINS_CHK           ;8 bit,
CALL    DELAY40uS
MOV     A,#7FH                  ;Contrast set
CALL    WRINS_CHK
CALL    DELAY40uS
MOV      A,#53H             ;Power down/Contrast set
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#14H                  ; Bias/Follwer set
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#67H                  ; ICON/Power(B,R,F) set
CALL    WRINS_CHK
CALL    DELAY200mS      ;for power stable
MOV     A,#0CH                  ;DISPLAY ON
CALL    WRINS_CHK
CALL    DELAY40uS
MOV     A,#01H                  ;CLEAR DISPLAY
CALL    WRINS_CHK
CALL    DELAY2mS
;---------------------------------------------------------------------
MAIN_START:
XXXX
XXXX
XXXX
.
.
.
.
.
;---------------------------------------------------------------------
WRINS_CHK:
CALL    CHK_BUSY
WRINS_NOCHK:
PUSH    A
ANL     A,#F0H
CLR     RS          ;EX:Port 3.0
CLR     RW              ;EX:Port 3.1
SETB    E           ;EX:Port 3.2
MOV     P1,A            ;EX:Port1=Data Bus
CLR     E
POP     A
SWAP    A
WRINS_ONCE:
ANL     A,#F0H
CLR     RS
CLR     RW
SETB    E
MOV     P1,A
CLR     E
MOV     P1,#FFH ;For Check Bus Flag
RET
;---------------------------------------------------------------------
CHK_BUSY:               ;Check Busy Flag
PUSH    A
MOV     P1,#FFH
$1
CLR     RS
SETB    RW
SETB    E
MOV     A,P1
CLR     E
MOV     P1,#FFH
CLR     RS
SETB    RW
SETB    E
NOP
CLR     E
JB       A.7,$1
POP     A
RET
```

Initial Code (8051 MPU, Parallel 4-bit Interface)

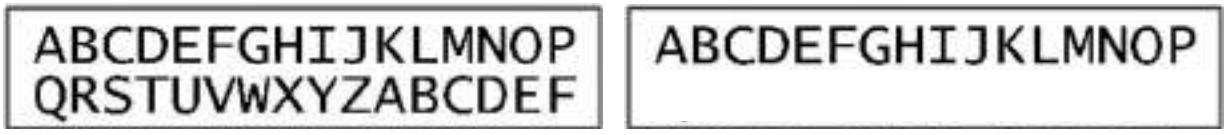
```
;-------------------------------------------------------------------------------
INITIAL_START:
CALL    HARDWARE_RESET
CALL    DELAY40mS
MOV     A,#32H                  ;FUNCTION SET
CALL    WRINS_NOCHK     ;8 bit,
CALL    DELAY40uS
MOV     A,#32H                  ;FUNCTION SET
CALL    WRINS_NOCHK     ;8 bit,
CALL    DELAY40uS
MOV     A,#54H                  ;Internal  OSC  frequency
adjustment
CALL    WRINS_NOCHK
CALL    DELAY40uS
MOV     A,#31H                  ;FUNCTION SET
CALL    WRINS_NOCHK     ;8 bit,
CALL    DELAY40uS
MOV     A,#7FH                  ;Contrast set
CALL    WRINS_NOCHK
CALL    DELAY40uS
MOV     A,#53H                  ;Power down/Contrast set
CALL    WRINS_NOCHK
CALL    DELAY40uS
MOV     A,#14H                  ; Bias/Follwer set
CALL    WRINS_NOCHK
CALL    DELAY40uS
MOV     A,#67H                  ; ICON/Power(B,R,F) set
CALL    WRINS_NOCHK

CALL    DELAY200mS      ;for power stable
MOV     A,#0CH                  ;DISPLAY ON
CALL    WRINS_NOCHK
CALL    DELAY40uS
MOV     A,#01H                  ;CLEAR DISPLAY
CALL    WRINS_NOCHK
CALL    DELAY2mS
;-------------------------------------------------------------------------------
MAIN_START:
XXXX
XXXX
XXXX
XXXX
    .
    .
;-------------------------------------------------------------------------------
WRINS_NOCHK:
PUSH    1
MOV  R1,#8
CLR      RS
$1
RLC      A
MOV      SI,C
SET      SCL
NOP
CLR      SCL
DJNZ     R1,$1
POP      1

CALL     DLY1.5mS
RET
```

LCD & ST7038 CONNECTION

SHLC/SHLS bits can select different scan direction for LCD panel.

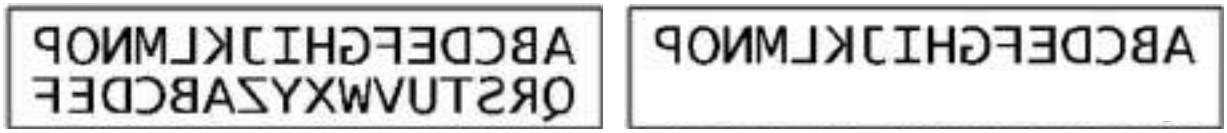
1 & 2-Line Display Mode

- COM normal direction, SEG normal direction (SHLC=1, SHLS=1)



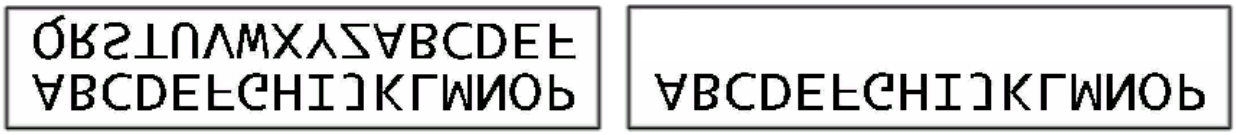
2-Line X 16 Characters, SHLC=1, SHLS=1 | 1-Line X 16 Characters, SHLC=1, SHLS=1

- COM normal direction, SEG reverse direction (SHLC=1, SHLS=0)



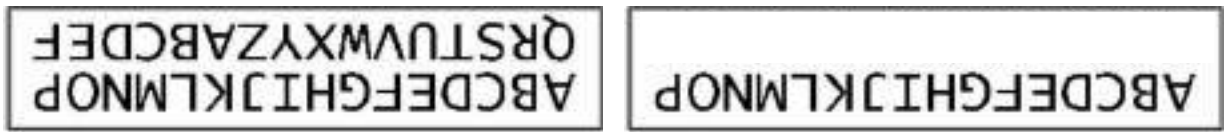
2-Line X 16 Characters, SHLC=1, SHLS=0 | 1-Line X 16 Characters, SHLC=1, SHLS=0

- COM reverse direction, SEG normal direction (SHLC=0, SHLS=1)



2-Line X 16 Characters, SHLC=0, SHLS=1 | 1-Line X 16 Characters, SHLC=0, SHLS=1

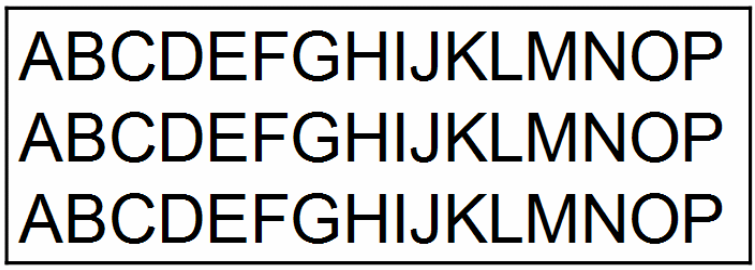
- COM reverse direction, SEG reverse direction (SHLC=0, SHLS=0)



2-Line X 16 Characters, SHLC=0, SHLS=0 | 1-Line X 16 Characters, SHLC=0, SHLS=0

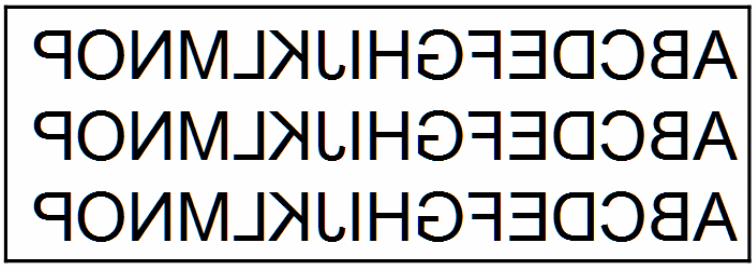
3-Line Display Mode

- COM normal direction, SEG normal direction (SHLC=1, SHLS=1)



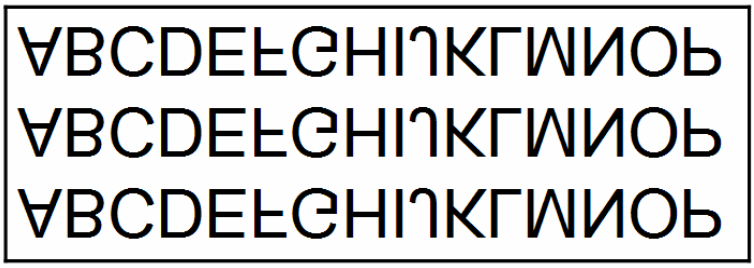
3 line x 16 characters, SHLC=1 SHLS=1

- COM normal direction, SEG reverse direction (SHLC=1, SHLS=0)



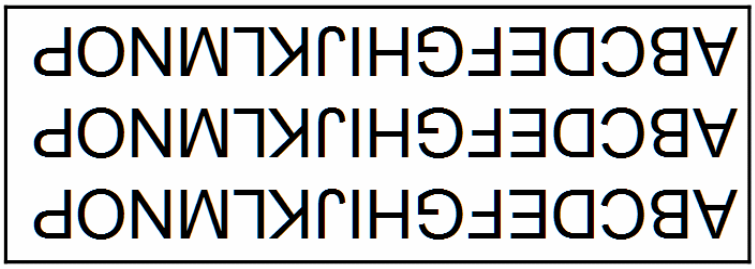
3 line x 16 characters, SHLC=1, SHLS=0

- COM reverse direction, SEG normal direction (SHLC=0, SHLS=1)



3 line x 16 characters, SHLC=0, SHLS=1

- COM reverse direction, SEG reverse direction (SHLC=0, SHLS=0)

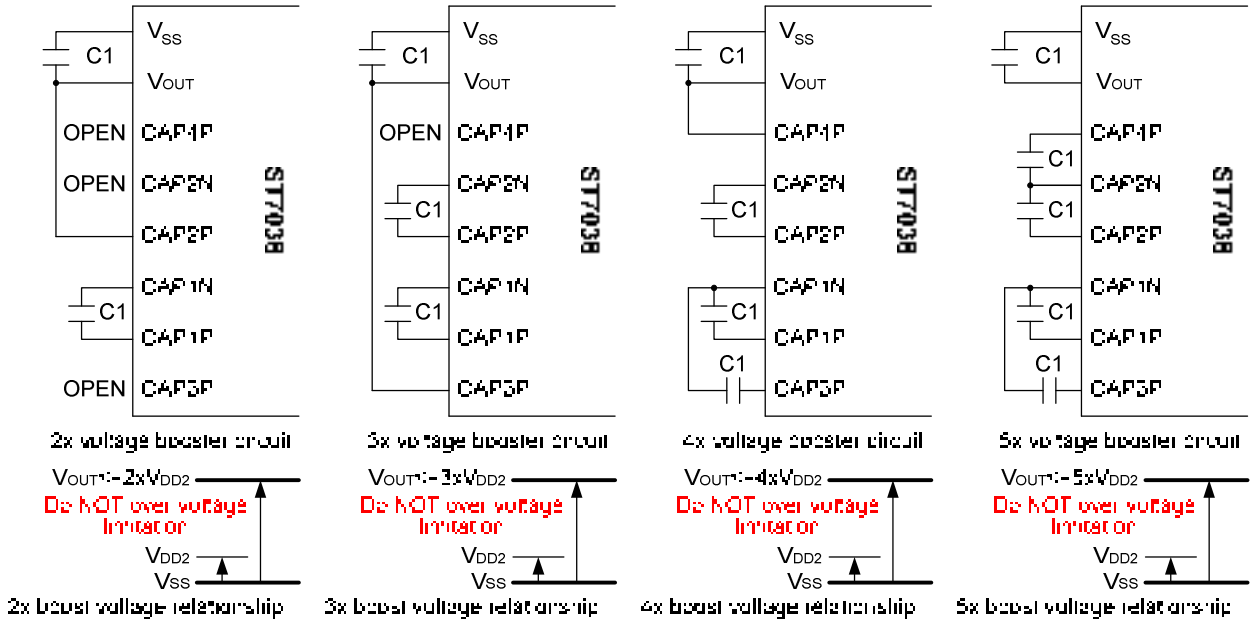


3 line x 16 characters, SHLC=0, SHLS=0

POWER SUPPLY FOR LCD DRIVER

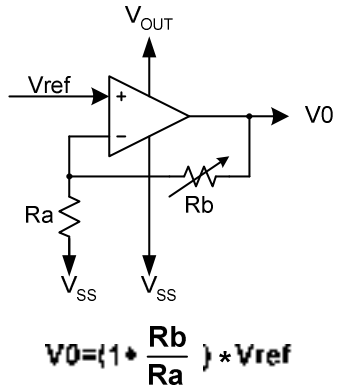
Built-in Booster circuit:

The voltage booster uses analog power (V_{DD2}) to generate boosted voltage. The boost stage is controlled by hardware connection. Please refer to the following figure for the detailed booster circuit connection.



Built-in Regulator circuit:

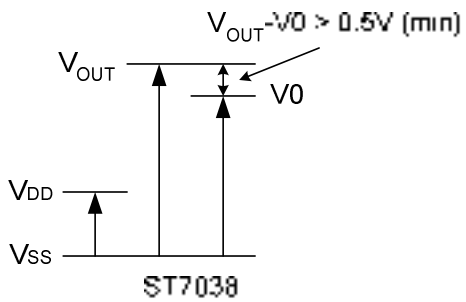
The built-in Regulator circuit is shown below, where the Vref = 1.47V.



VC6	VC5	VC4	VC3	VC2	VC1	VC0	V0 (V)
0	0	0	0	0	0	0	2.940
0	0	0	0	0	0	1	2.975
0	0	0	0	0	1	0	3.010
0	0	0	0	0	1	1	3.045
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	7.280
1	1	1	1	1	0	1	7.315
1	1	1	1	1	1	0	7.350
1	1	1	1	1	1	1	7.385

Notes:

- $V_{OUT} \geqq V0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq Vss$ must be maintained.
- If the calculation value of V0 is higher than V_{OUT}, the real V0 value will saturate to V_{OUT}.
- Internal built-in booster can only be used when OPF1=0,OPF2=0.
- To keep V0 level stable, be sure the voltage level of V_{OUT} is higher than V0 by at least 0.5V (even displaying the heaviest-loading pattern).
  If the panel size is larger than 3", the recommend V_{OUT} should be higher than V0 by at least 0.8V (even displaying the heaviest-loading pattern).



Built-in Follower circuit:

There are 3 kinds of built-in Follower circuits. By instruction, the follower can be configured to be:

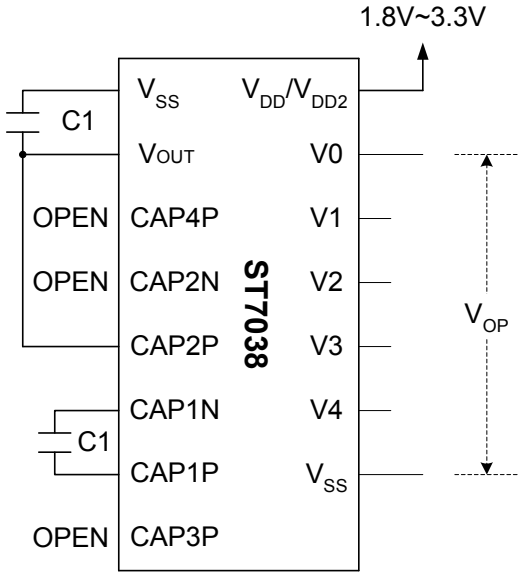
OPF[2:1]	Description
(0,0)	Select built-in Follower
(0,1)	Select built-in bias resistor (9.9K)
(1,0)	Select built-in bias resistor (3.3K)
(1,1)	Select external bias circuit (built-in Follower is OFF)

Note:

- When using built-in bias resistors (9.9K or 3.3K), the current consumption maybe larger than using built-in Follower. Furthermore, the loading of built-in Booster is increasing too. That will cause the Booster efficiency drop and V0 maybe affected.

Referential Power Connection:

When using internal Booster, Regulator and Follower, the referential connection is shown below.



2X Booster, Regulator & Follower

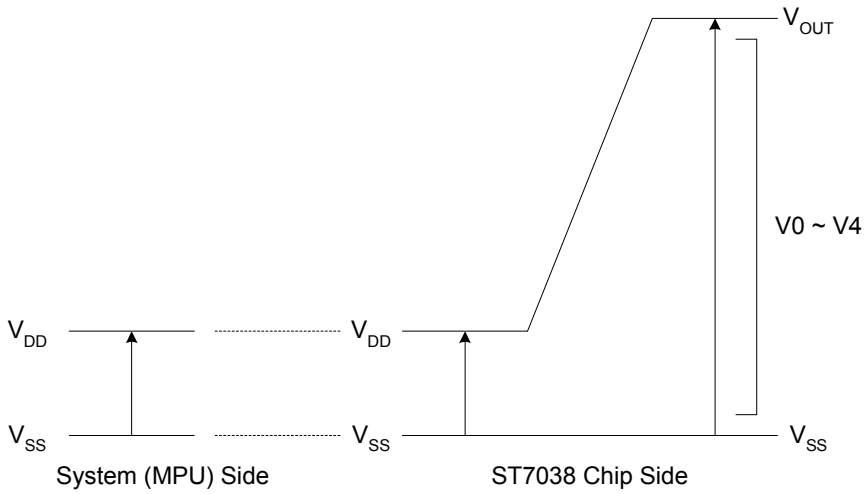
Note:

- If LCD panel size is larger than 2”, a V0 capacitor is recommended.
  If LCD panel size is larger than 3”, 4 Follower capacitors (V1~V4) are recommended.
- When V_{DD2}<2.4V, the Booster efficiency maybe lower and the ITO resistance should be lower to solve this problem.

ABSOLUTE LIMITING VALUES

V_{SS} is 0V unless otherwise specified.

Characteristics	Symbol	Value	Unit
Digital Power Supply Voltage	V_{DD}	−0.3 ~ 3.6	V
Analog Power Supply Voltage	V_{DD2}	−0.3 ~ 3.6	V
Interface Input Voltage Apply on : CSB, RESB, A0, /WR, /RD, D7~D0	V_{IN}	−0.3 ~ V_{DD}+0.5	V
LCD Driver Voltage (Booster & Regulator)	V_{OUT}, V0	−0.3 ~12	V
LCD Driver Voltage (Follower)	V1, V2, V3 & V4	−0.3 ~ 12	V
Operating Temperature	T_{OPR}	−30 ~ +85	°C
Storage Temperature	T_{STO}	−65 ~ +150	°C



Notes:

1. Stresses over the Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are relative to V_{SS} unless otherwise noted.
3. Ensure that the voltage levels of V1, V2, V3 and V4 always follow the rule below:
   $V_{OUT} \geqq V0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V_{SS}$

DC CHARACTERISTICS

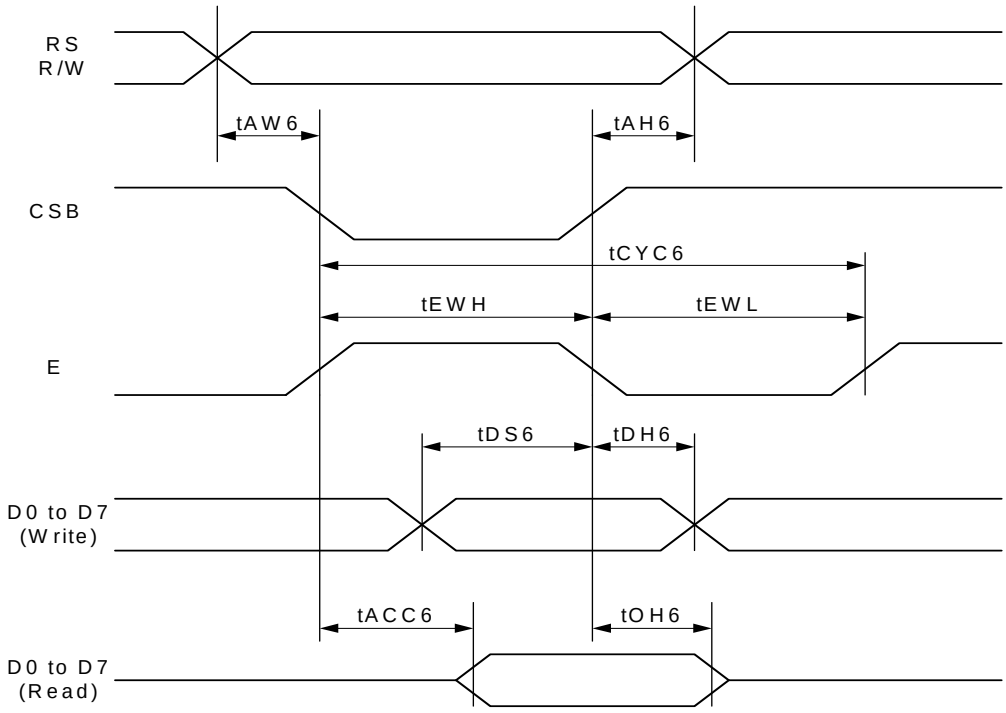
V_{SS} is 0V unless otherwise specified.

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-	1.8	-	3.3	V
LCD Voltage	V0	V0-Vss	3.0	-	12.0	V
Power Supply Current	I_{DD}	V_{DD}=3.0V *[1] (use internal power circuit)	-	160	230	uA
Sleep Mode	I_{DD}	V_{DD}=3.0V (use internal power circuit)	-	-	10	uA
Input High Voltage (Except OSC1)	V_{IH1}	-	0.8 V_{DD}	-	VDD	V
Input Low Voltage (Except OSC1)	V_{IL1}	-	- 0.3	-	0.2 V_{DD}	V
Input High Voltage (OSC1)	V_{IH2}	-	0.8 V_{DD}	-	V_{DD}	V
Input Low Voltage (OSC1)	V_{IL2}	-	-	-	0.2 V_{DD}	V
Output High Voltage (DB0 - DB7)	V_{OH1}	I_{OH} = -1.5mA	1.4	-	-	V
Output Low Voltage (DB0 - DB7)	V_{OL1}	I_{OL} = 2.0mA	-	-	0.66	V
Common Resistance	R_{COM}	V0 = 4V, Id = 0.05mA	-	2	20	K
Segment Resistance	R_{SEG}	V0 = 4V, Id = 0.05mA	-	2	30	K
Input Leakage Current	I_{LEAK}	V_{DD} = 0V to V_{DD}	-1	-	1	A
Pull Up MOS Current	I_{PUP}	V_{DD} = 3V	150	-	-	uA
Internal OSC	f_{OSC}	V_{DD} = 3V, 1/25duty	-	370.5	407.6	kHz
Frame frequency	FR	FRC=0, Ta=25°C	-	70.92	78.01	Hz

Notes: When the XRESET Pin is “L”, there is a temporary current over (5mA).

AC CHARACTERISTICS

6800 Interface

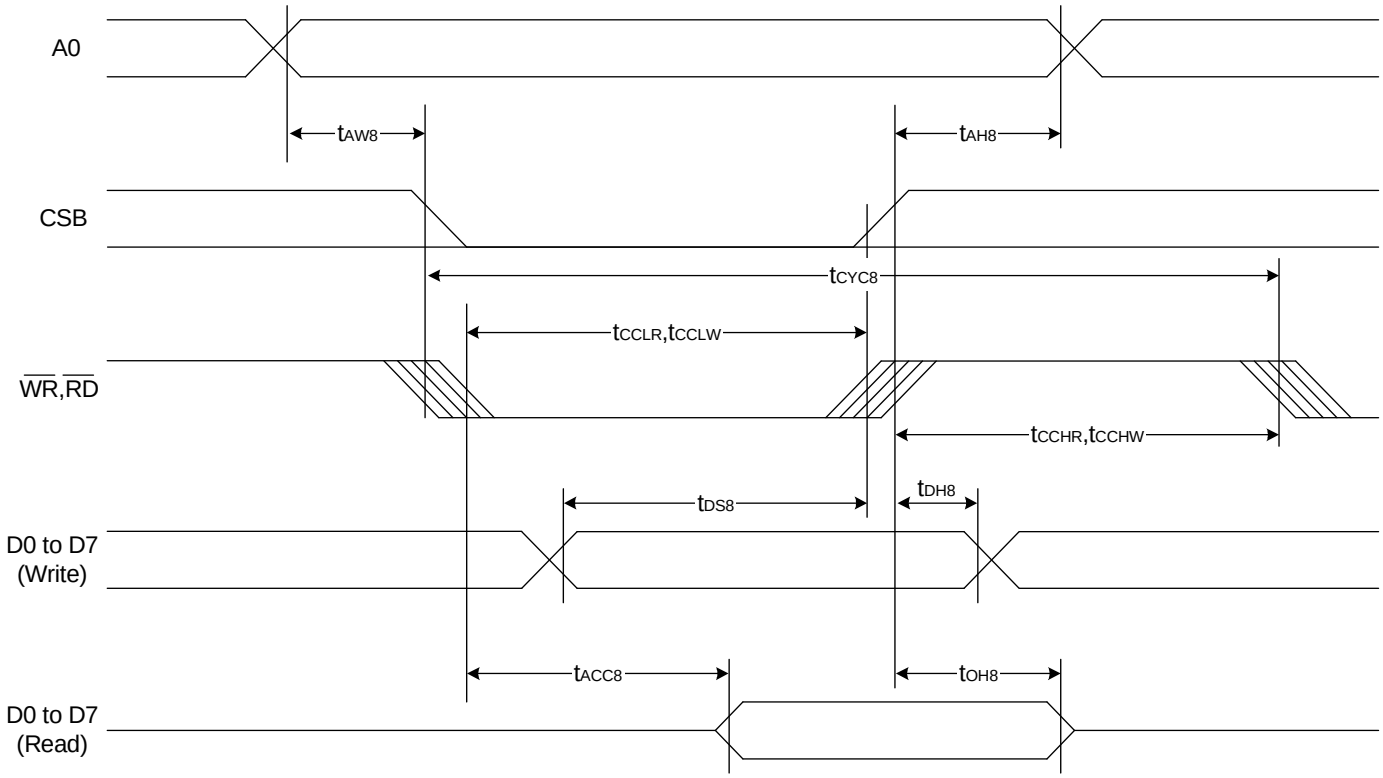


Ta = -30 ~ 85 °C

Item	Signal	Symbol	VDD=1.8V		VDD=2.5V		VDD=3.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Address hold time	RS	tAH6	20	-	15	-	15	-	ns
Address setup time	RS	tAW6	20	-	15	-	15	-	
System cycle time	RS	tCYC6	240	-	150	-	120	-	ns
Data setup time	D0 to D7	tDS6	150	-	80	-	60	-	ns
Data hold time	D0 to D7	tDH6	20	-	15	-	15	-	
Access time	D0 to D7	tACC6	-	320	-	260	-	240	ns
Output disable time	D0 to D7	tOH6	200	-	130	-	100	-	
Enable Rise/Fall time	E	tr,tf		20	-	20	-	20	ns
Enable H pulse time	E	tEWH	210	-	120	-	90	-	ns
Enable L pulse time	E	tEWL	30	-	30	-	30	-	ns

Note: All timing is specified using 20% and 80% of VDD as the reference.

8080 Interface

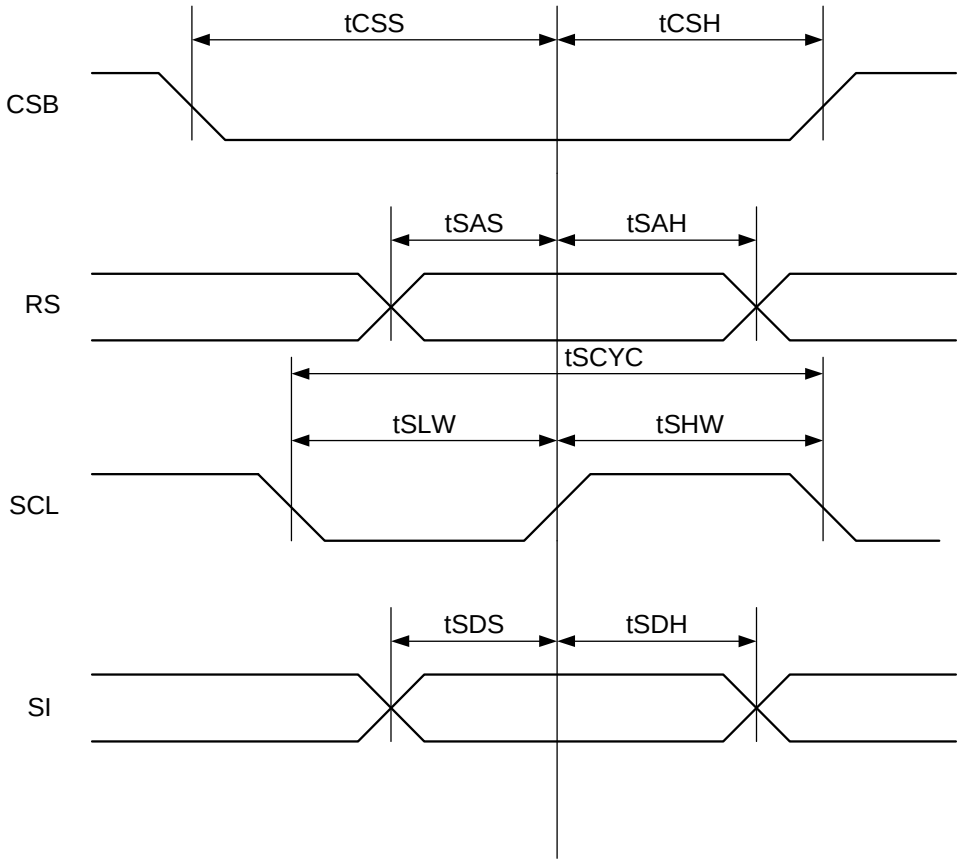


Ta = −30 ~ 85 °C

Item	Signal	Symbol	VDD=1.8V		VDD=2.5V		VDD=3.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Address hold time	RS	t_{AH8}	80	-	30	-	30	-	ns
*Address setup time	RS	t_{AW8}	0	-	0	-	0	-	
System cycle time	RS	t_{CYC8}	240	-	190	-	150	-	ns
Enable L pulse width (WRITE)	D0 to D7	t_{CCLW}	180	-	140	-	110	-	ns
Enable H pulse width (WRITE)	D0 to D7	t_{CCHW}	20	-	20	-	20	-	
Enable L pulse width (READ)	D0 to D7	t_{CCLR}	180	-	140	-	110	-	ns
Enable H pulse width (READ)	D0 to D7	t_{CCHR}	20	-	20	-	20	-	
WRITE Data setup time	Write	t_{DS8}	120	-	80	-	70	-	ns
WRITE Data hold time	Write	t_{DH8}	80	-	50	-	50	-	ns
READ access time, C_L= 100 pF	Read	t_{ACC8}	-	240	-	220	-	180	ns
READ Output disable time, C_L = 100 pF	Read	t_{OH8}	120	-	-	100	-	80	ns

Note: All timing is specified using 20% and 80% of VDD as the reference.

Serial 4-Line Interface

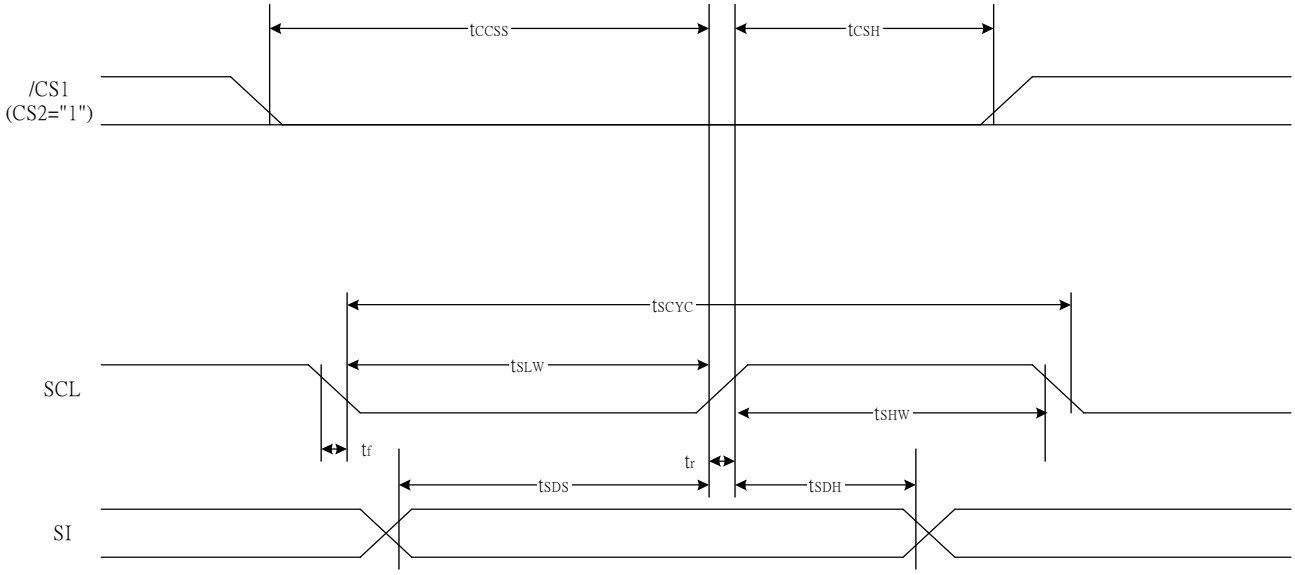


Ta = −30 ~ 85 °C

Item	Signal	Symbol	VDD=1.8V		VDD=2.5V		VDD=3.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	tSCYC	180	-	110	-	80	-	ns
SCL “H” pulse width		tSHW	70	-	40	-	40	-	
SCL “L” pulse width		tSLW	80	-	50	-	40	-	
Address setup time	RS	tSAS	10	-	10	-	10	-	ns
Address hold time		tSAH	60	-	40	-	30	-	
Data setup time	SI	tSDS	20	-	20	-	20	-	ns
Data hold time		tSDH	10	-	10	-	10	-	
CS-SCL time	CS	tCSS	20	-	20	-	20	-	ns
		tCSH	210	-	120	-	90	-	

Note: All timing is specified using 20% and 80% of VDD as the reference.

Serial 3-Line Interface

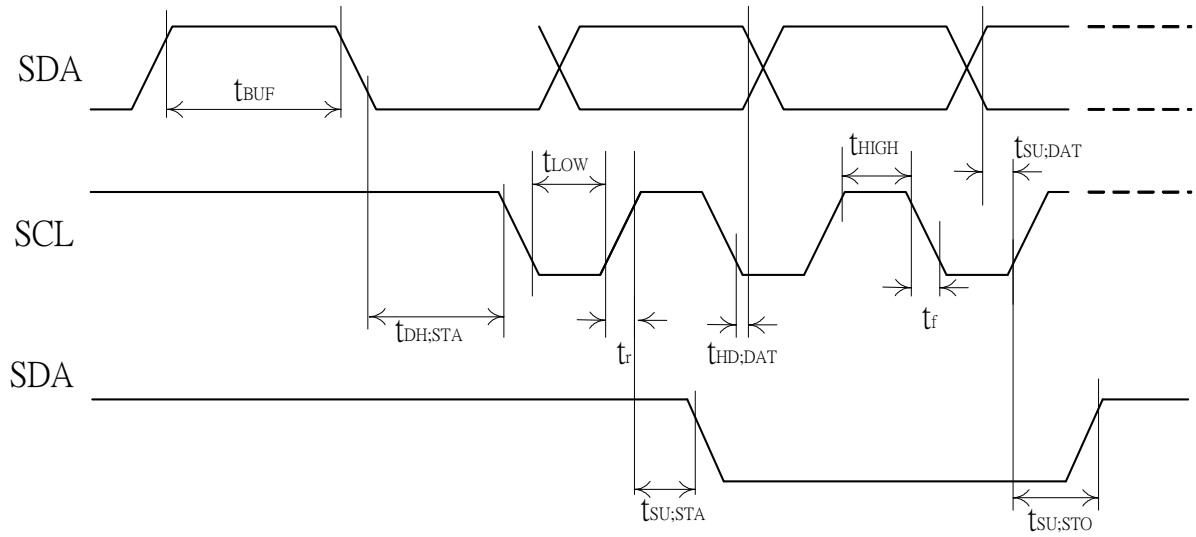


Ta = −30 ~ 85 °C

Item	Signal	Symbol	VDD=1.8V		VDD=2.5V		VDD=3.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	tSCYC	200	-	100	-	80	-	ns
SCL “H” pulse width		tSHW	70	-	40	-	30	-	
SCL “L” pulse width		tSLW	100	-	50	-	40	-	
Address setup time	RS	tSAS	10	-	10	-	10	-	ns
Address hold time		tSAH	60	-	40	-	30	-	
Data setup time	SI	tSDS	20	-	20	-	20	-	ns
Data hold time		tSDH	10	-	10	-	10	-	
CS-SCL time	CS	tCSS	70	-	40	-	20	-	ns
		tCSH	200	-	100	-	80	-	

Note: All timing is specified using 20% and 80% of VDD as the reference.

Serial I²C Interface

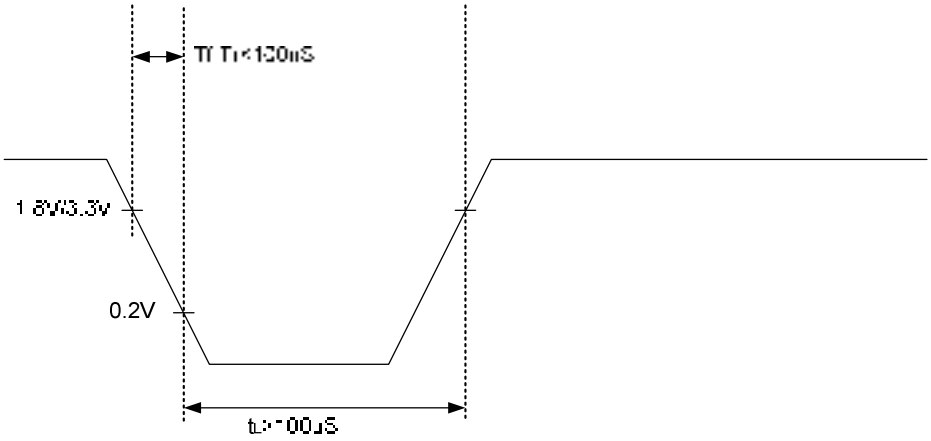


Ta = −30 ~ 85°C

Item	Signal	Symbol	Condition	VDD=1.8V Rating		VDD=2.5V Rating		VDD=3.3V Rating		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	0.6	–	
Data set-up time	SI	$t_{SU;DAT}$	—	300	–	200	–	100	–	ns
Data hold time		$t_{HD:DAT}$		0	0.9	0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	—	300	—	300	—	300	ns
SCL,SDA fall time		t_f		—	300	—	300	—	300	
Capacitive load represent by each bus line	—	C_b	—	–	400	–	400	–	400	pf
Setup time for a repeated START condition	SI	$t_{SU;STA}$	—	0.7	–	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	0.6	–	us
Setup time for STOP condition	—	$t_{SU;STO}$	—	0.6	–	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	1.3	–	us

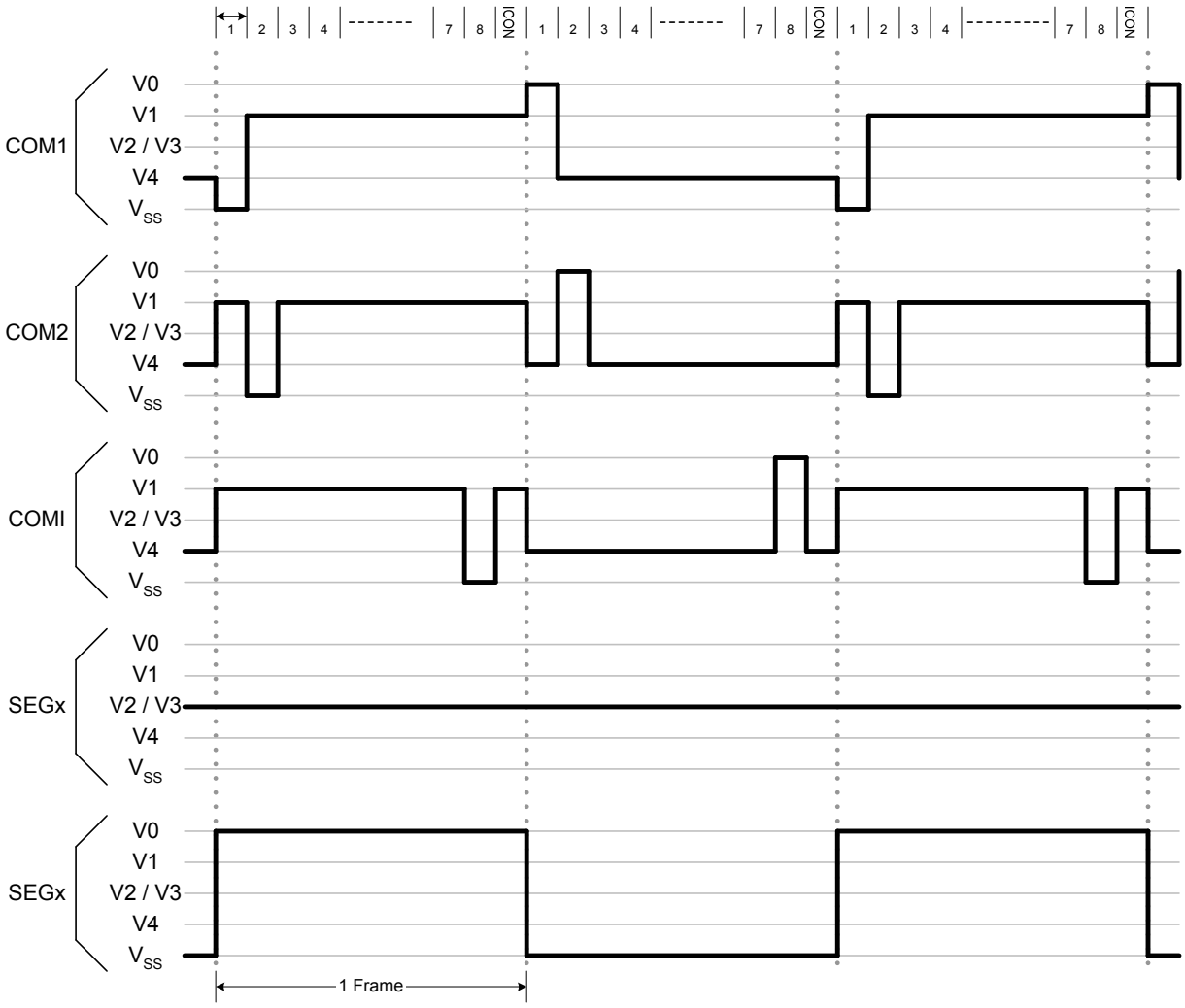
Note: All timing is specified using 20% and 80% of VDD as the reference.

Hardware Reset (XRESET)

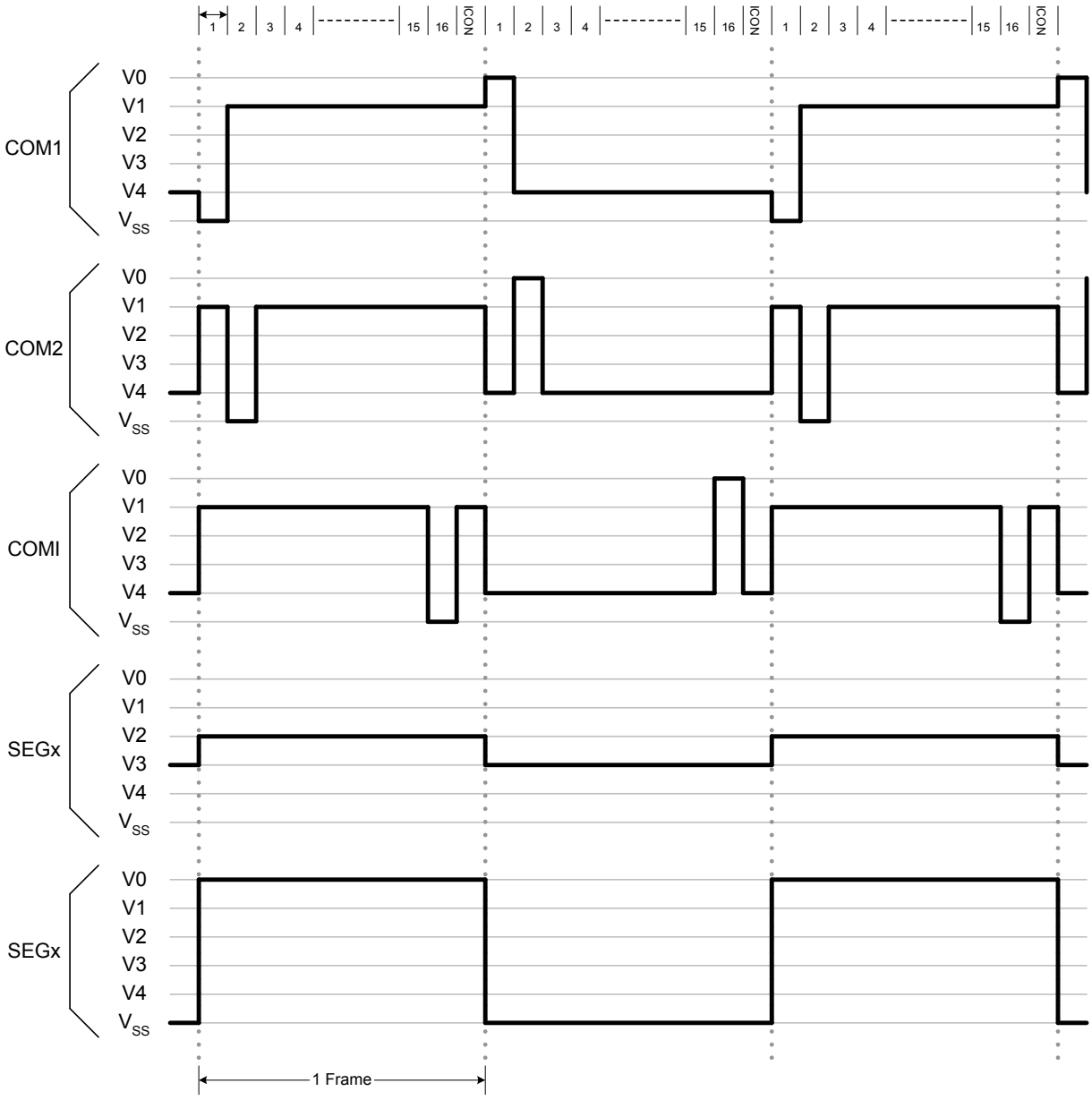


LCD FRAME RATE

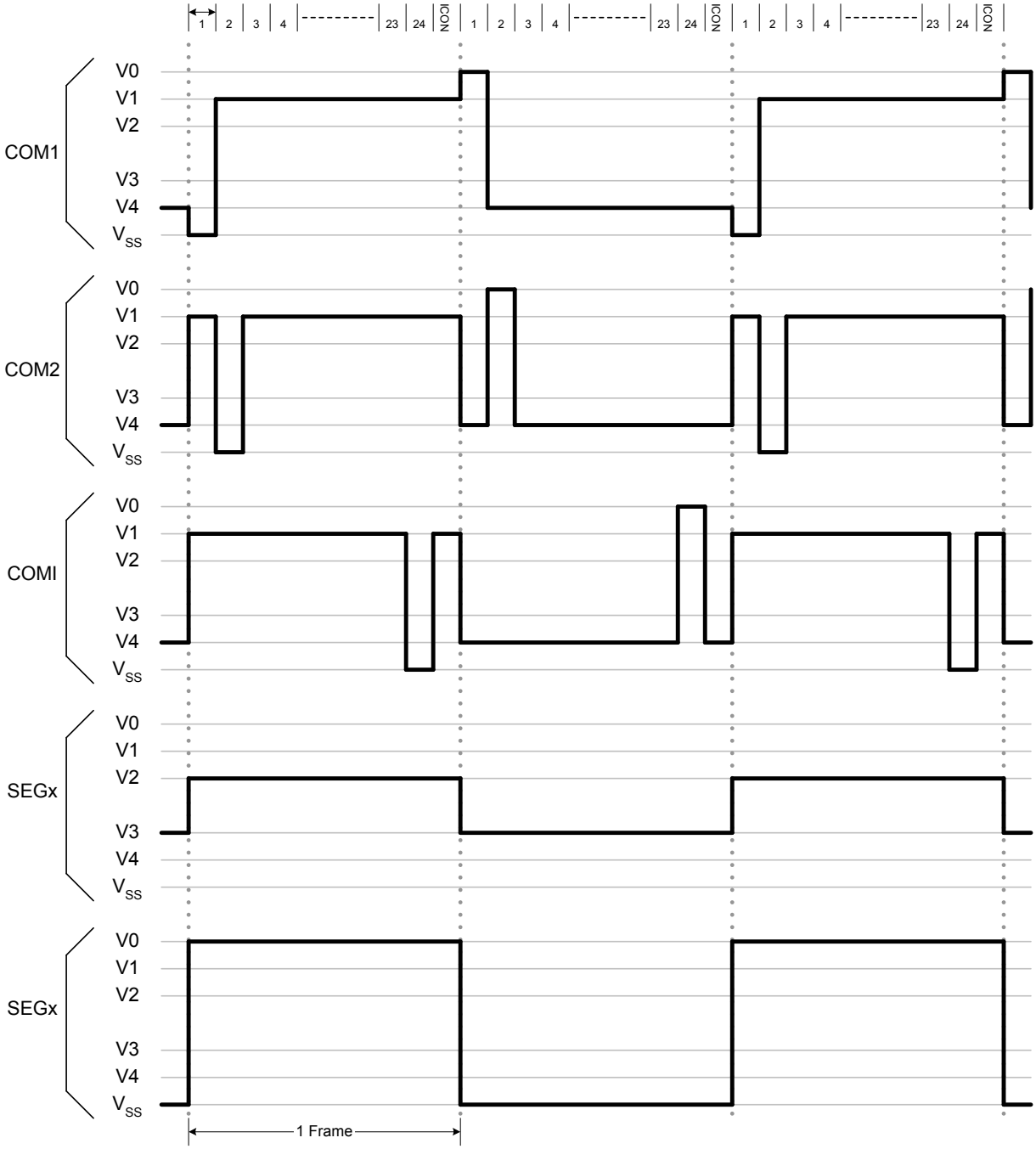
1. 1-Line Display Mode:
   Assume the oscillation frequency is 284KHz (1 clock cycle time = 3.52us), 1/4 bias,
   1/9 duty, 1 frame = 14.08ms = 71Hz (SHLC=1, SHLS=1).



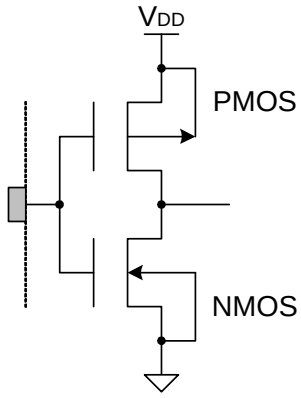
2. 2-Line or 1-Line Double Height Display Mode:
   Assume the oscillation frequency is 249.7KHz (1 clock cycle time = 4us), 1/5 bias, 1/17 duty, 1 frame = 14.42ms = 69.36Hz (SHLC=1, SHLS=1).



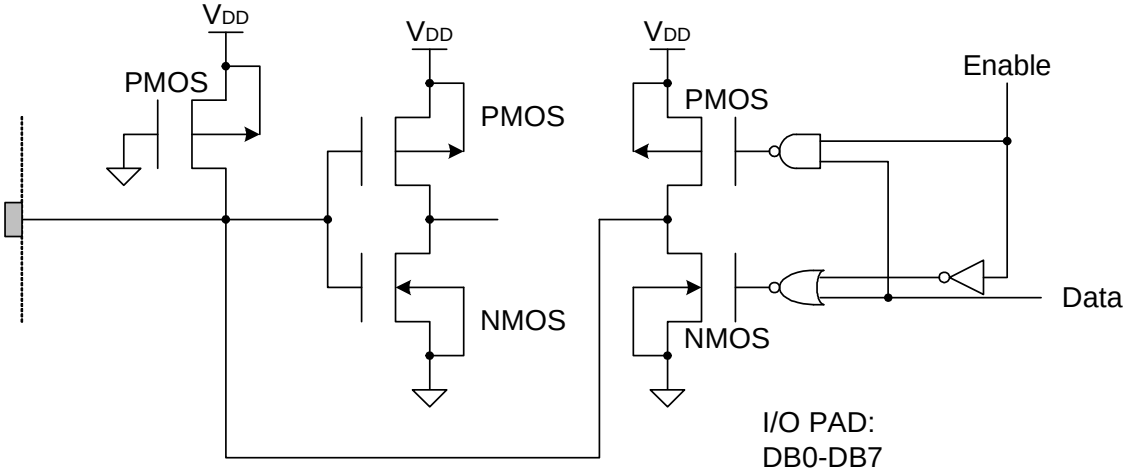
3. 3-Line or 2-Line Double Height Display Mode:
   Assume the oscillation frequency is 370.5KHz (1 clock cycle time = 2.70us), 1/6 bias, 1/25 duty, 1 frame = 14.04ms = 71.25Hz (SHLC=1, SHLS=1).



I/O PAD CONFIGURATION



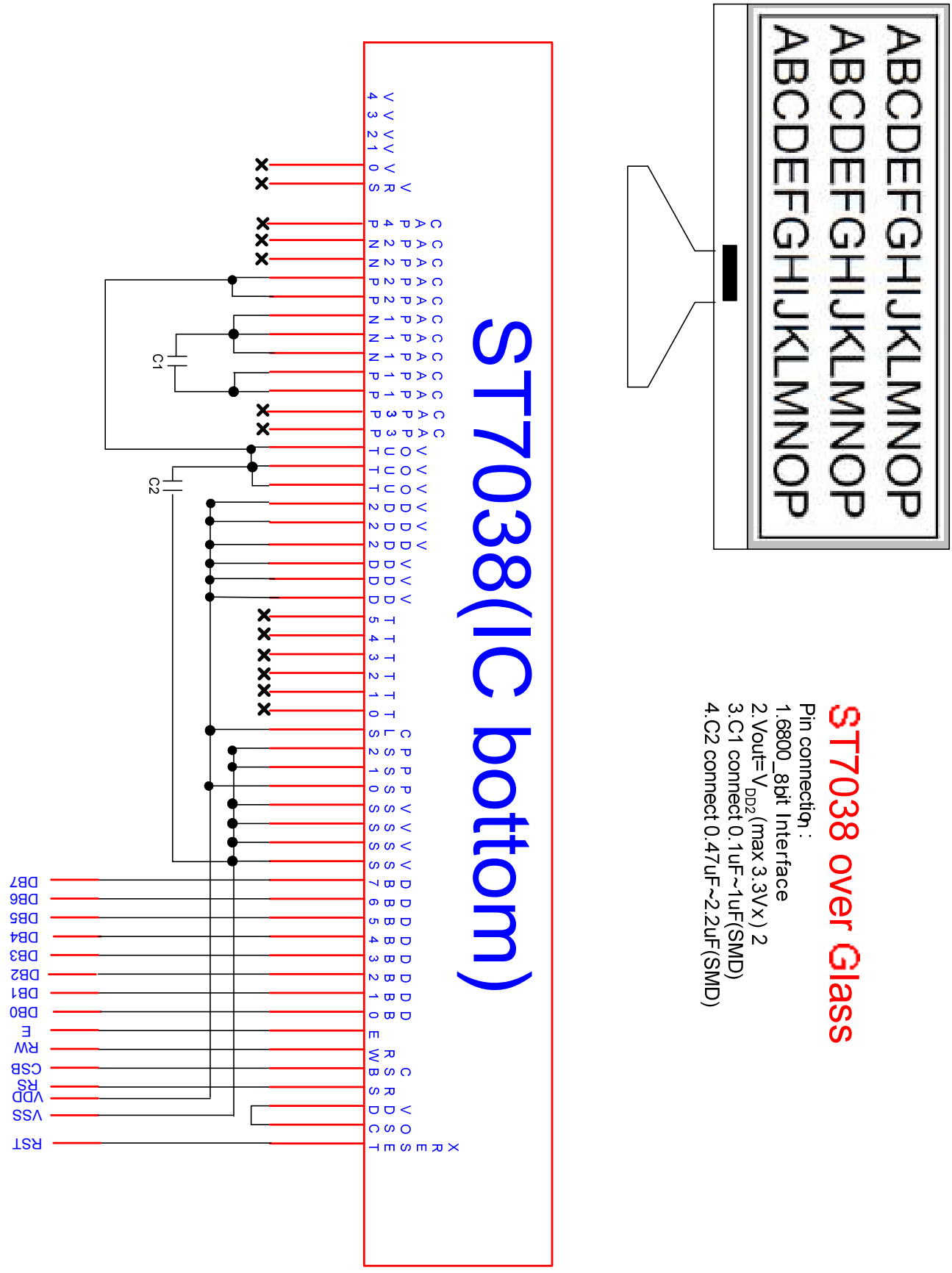
Input PAD (No Pull up):
RS, R/W, XRESET, CSB,
CLS



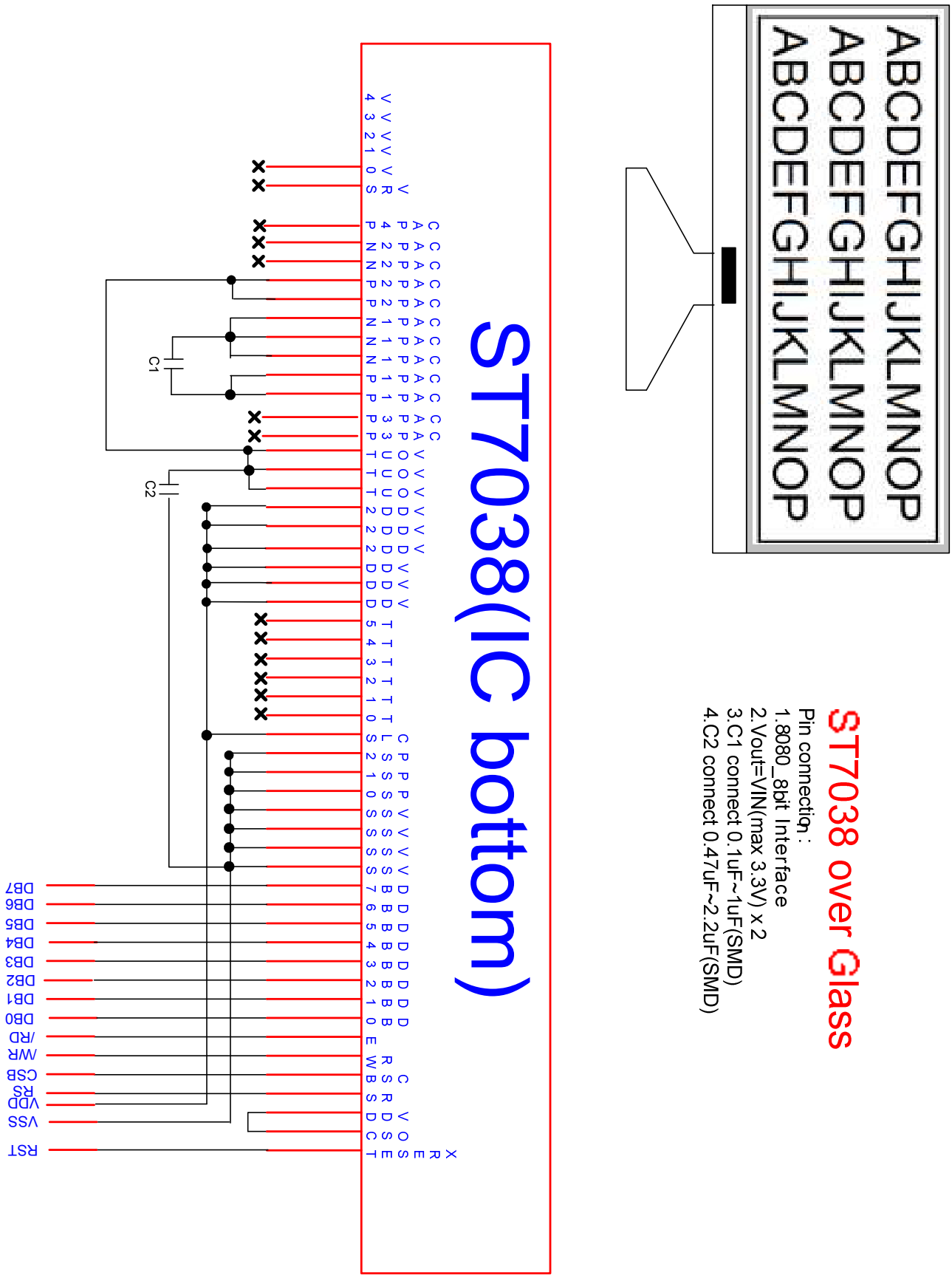
I/O PAD:
DB0-DB7

APPLICATION CIRCUIT

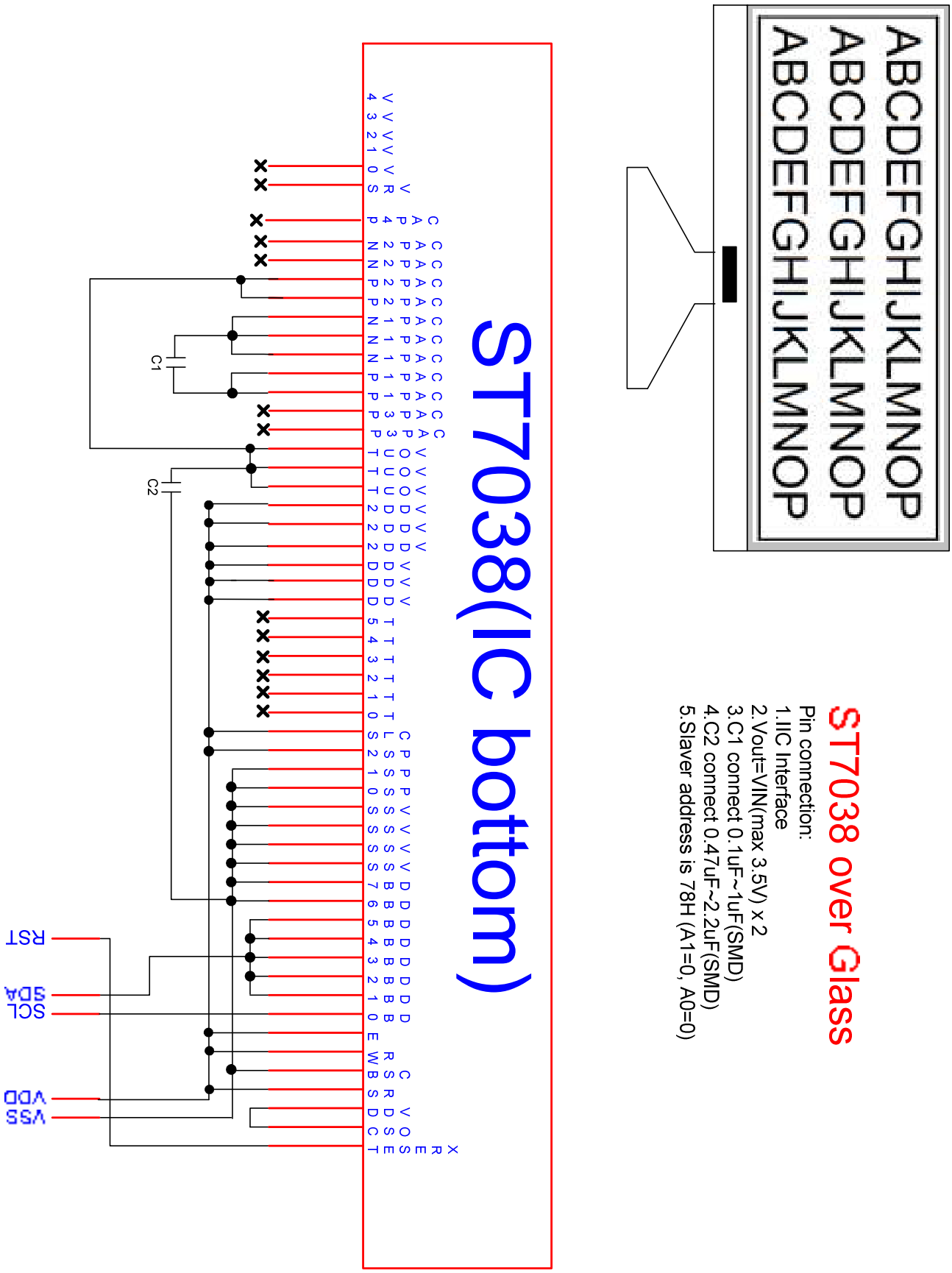
- 6800 series 8-bit Interface:



- 8080 series 8-bit Interface:



- I²C Interface:



ST7038 over Glass

Pin connection:

1.IIC Interface

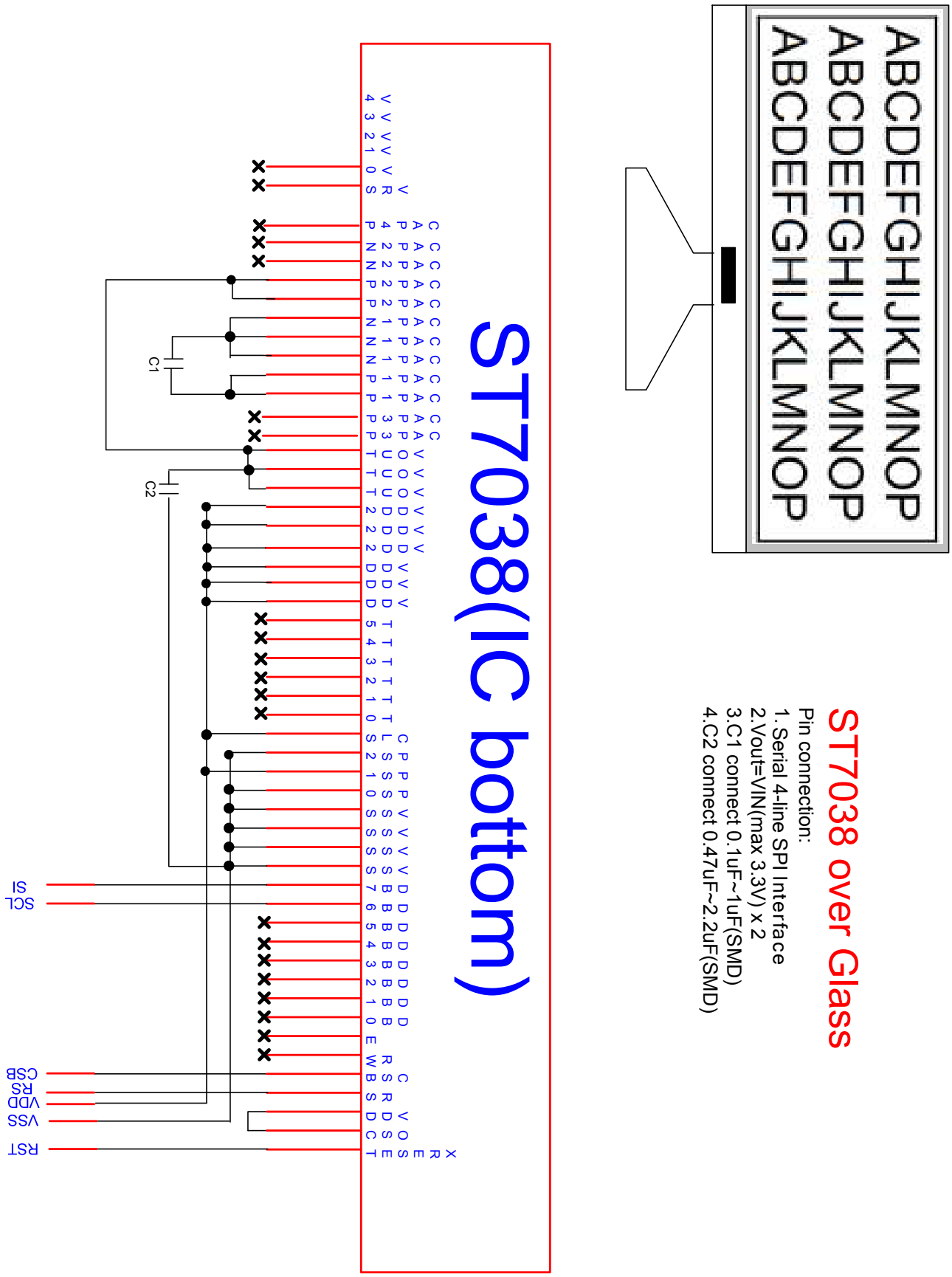
2.Vout=VIN(max 3.5V) x 2

3.C1 connect 0.1uF~1uF(SMD)

4.C2 connect 0.47uF~2.2uF(SMD)

5.Slaver address is 78H (A1=0, A0=0)

- Serial 4 line SPI :

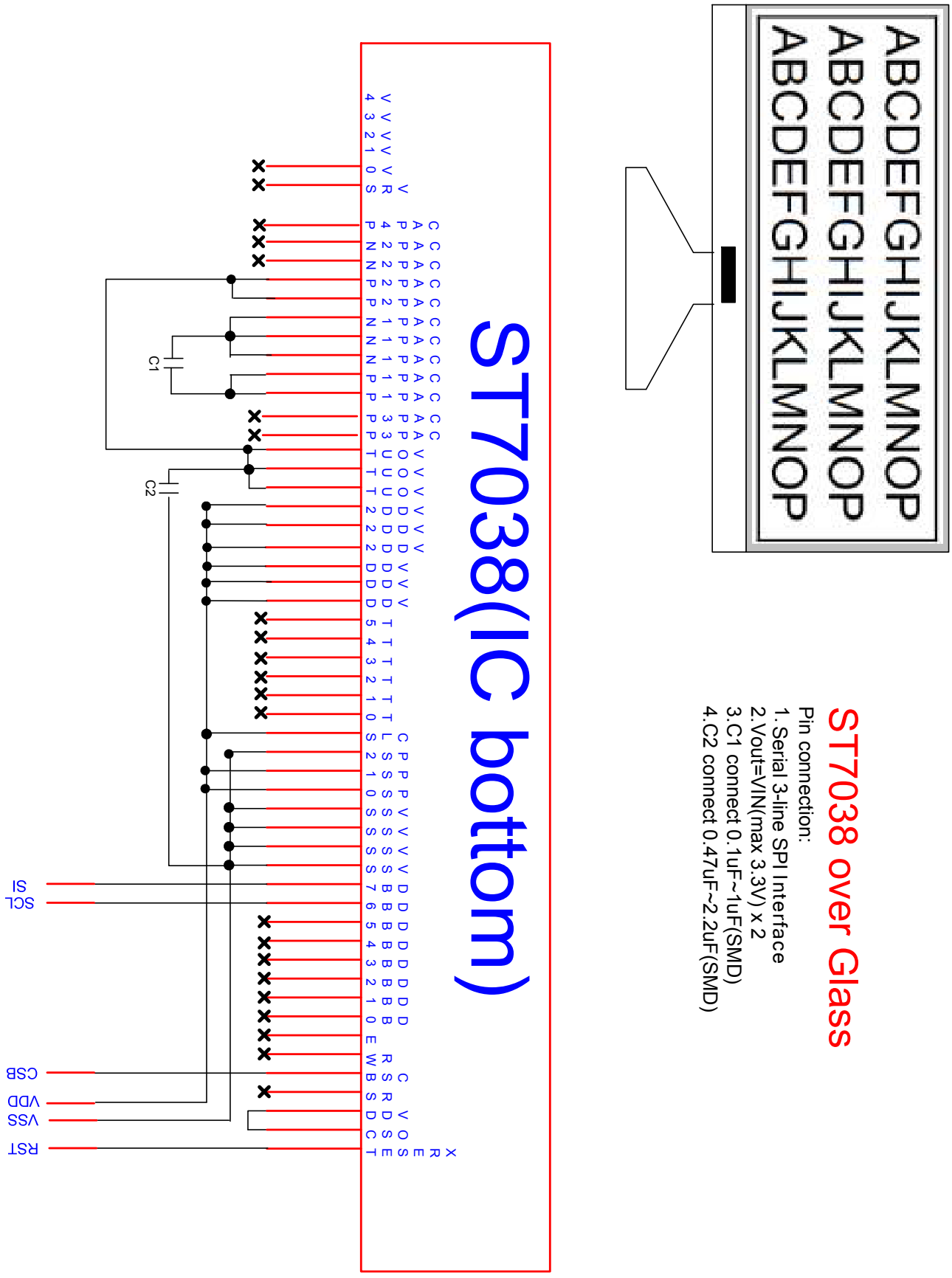


ST7038 over Glass

Pin connection:

1. Serial 4-line SPI Interface
2. Vout=VIN(max 3.3V) x 2
3. C1 connect 0.1uF~1uF(SMD)
4. C2 connect 0.47uF~2.2uF(SMD)

- Serial 3 line SPI :



ST7038 over Glass

Pin connection:

1. Serial 3-line SPI Interface
2. Vout=VIN(max 3.3V) x 2
3. C1 connect 0.1uF~1uF(SMD)
4. C2 connect 0.47uF~2.2uF(SMD)

Reversion History

Version	Date	Description
0.6	2005/11/10	Modify 2x,3x booster circuit.
0.7	2005/11/22	Modify the COM output map when SHLC=0.
0.8	2005/12/16	● Update the COM output map. ● Update the characteristics. ● Update the initial flow.
0.8_0B	2006/01/23	Added I/O PIN ITO Resister Limitation Modified Character Codes and Character Patterns page 20
0.9_0B	2006/02/09	Modified Chip Size
1.0	2006/08/03	All unused input pin must be connect to VDD. Rewrite function description and reorganize document format.
1.1	2006/08/22	Modified V0 voltage range page 32, page 44
1.2	2007/03/01	Modified CSB pin must connect to “VSS” when I2C mode is selected.
1.3	2008/5/21	Added Serial 3-line 4-line interface Application Circuit