



ST2601B

PRELIMINARY

8 BIT Integrated Microcontroller with 128K Bytes ROM

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1. FEATURES

■ Totally static 8-bit CPU

■ ROM: 128k x 8-bit ■ RAM: 1.5K x 8-bit

Stack: Up to 128-level deepOperation voltage: 2.4V ~ 3.6V

Operation frequency:

-3.0Mhz@2.4V(Min.)

- 4.0Mhz@2.7V(Min.)

LCD Drives

- COM: 36 outputs. Eight shared with one output port

 SEG: 56 outputs. Shared with 3 I/O ports and memory bus signals.

One 8x8 Signed Multiplier

■ Low Voltage Reset (LVR)

- Two levels by code option

Low Voltage Detector (LVD)

- Programmable 4 levels

- System power or external battery level can be detected.

■ Programmable Watchdog Timer (WDT)

Memory interface to ROM, RAM, Flash

■ Memory configuration

- Three kinds of banks for program, data and interrupt

- 12-bit bank registers support up to 44M bytes

- Six programmable chip-selects with 4 modes

- Maximum single device of 16M bytes

■ General-Purpose I/O (GPIO) ports

- Up to 39 bit programmable I/Os

8 dedicated CMOS I/Os

23 shared with LCD SEGs

8 open drain output pins shared with LCD COMs

- Bit programmable pull-up for input pins

Pull-up/down and open-drain/CMOS control for Port-C

■ Timer/Counter

- Four 12-bit timers.

- One 8-bit base timer

- Seven fixed base timers

■ Three clocking outputs

- Clock sources including Timer0/1, baud rate generator

Eleven prioritized interrupts with dedicated exception vectors

- External interrupt (edge triggered)

- LCD buffer interrupt

- Base timer interrupt

- Timer0~3 interrupts (x4)

- SPI interrupts (x2)

- UART interrupts (x2)

Dual clock sources with warm-up timer

- Low frequency crystal oscillator (OSCX)...32768 Hz

- High frequency resistor or crystal/resonator oscillator

(OSC) selected by pin option455K~4M Hz

■ Direct Memory Access (DMA)

- Block-to-Block transfer

- Block to Single port

LCD Power Management

- DC-DC converter with 8-level output control
- LC driving voltage regulator with 16-level control
- 1/4, 1/5, 1/6 bias options with 4 voltage followers

LCD Driver

- 32x28~56x36 resolution, maximum 2016 dots
- Clock source from OSC/OSCX.
- Internal bias resistors(1/4, 1/5, 1/6 bias).

LCD Controller (LCDC)

- Software programmable display size up to 80X120
- B/W, Hardware 4/16 gray levels with 5-bit palette
- Support 1-/4-/8-bit LCD data bus
- Share system memory with display buffer and with no loss of the CPU time
- LCD buffer extension function to combine both internal and external RAM for larger display
- Diverse functions including virtual screen, panning, scrolling, contrast control and alternating signal generator

Programmable Sound Generator (PSG)

- Four channels with three playing modes:
 9-bit ADPCM, 8-bit PCM and 8-bit melody
- One 16-byte buffer and 6-bit volume control per channel
- Wavetable melody support
- Two dedicated PWM outputs for direct driving
- One 12-bit current DAC

Universal Asynchronous Receiver/Transmitter (UART)

- Full-duplex operation
- Baud rate generator with one digital PLL
- Standard baud rates of 600 bps to 115.2 kbps
- Both transmitter and receiver buffers supported
- Direct glueless support of IrDA physical layer protocol
 Two sets of I/Os (TX,RX) for two independent devices

■ Serial Peripheral Interface (SPI)

- Master and slave modes
- Five serial signals including enable and data-ready
- Both transmitter and receiver buffers supported
- Programmable data length from 7-bit to 16-bit

■ VIcd/LVD trimming fuse function:

- Vlcd default voltage variation trimming.
- 4-level LVD voltage variation trimming.

Three power down modes

- WAI0 mode
- WAI1 mode
- STP mode

2. BLOCK DIAGRAM

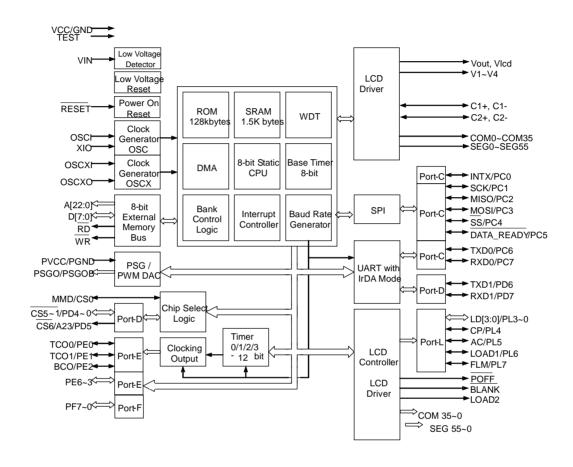


FIGURE 1-1 ST2601B Block Diagram



3. GENERAL DESCRIPTION

The ST2601B is a 8-bit integrated microcontroller designed with CMOS silicon gate technology. The true static CPU core, power down modes and dual oscillators design makes the ST2601B suitable for power saving and long battery life designs. The ST2601B integrates various logic to support functions on-chip which are needed by system designers.

The ST2601B features the capacity of memory access of maximum 44M bytes and DMA function for fast memory transfer. Six chip-select pins are equipped for direct connection to external ROM, SRAM, Flash memory or other devices. The maximum size for a single external memory device can be 16M bytes.

The ST2601B has 39 I/Os grouped into 5 ports. They are Port-C, Port-D, Port-E (7 pins), Port-F and Port-L, where the Port-F consists of 8 open-drain output pins shared with LCD COMs. Each I/O pins can be programmed to input or output individually. Port-C input pins provide both pull-up and pull-down options. The other input pins only support the pull-up option. In the case of output mode, Port-C output pins have open-drain type and CMOS type options; while the other ports are fixed at CMOS type. The Port-C/D/E/F/L are shared with other system functions. All the properties of the I/O pins are still programmable when they are configured as other special functional signals. This enlarges the flexibility of the usage of the functional signals.

The ability of driving large LCD panels, up to 80x120 in BW mode, and hardware gray-level support may enrich the display information and the diversify the display contents as well. By the patented sharing mechanism design of internal memory, the LCD display function can be done without the need of external display RAM. The variable LCD buffer design also makes it feasible to use small internal display RAM as the buffer of large-sized display. User may free major internal RAM for computing or temporary access while keeping the display content. The clock of LCD (LCDCK) is not only sourced from main-frequency (OSC), it can also be sourced by OSCX (32KHz crystal) to make current consumption to be minimum. Besides, Vlcd has excellent voltage variation when Vdd changes from 2.4V to 3.6V. Further more, ST2601B has inside trimming fuse function for Vlcd and LVD.So every ST2601B real-chip will have almost the same default Vlcd and LVD voltage.

The ST2601B equips 2 serial communication ports, one UART port and one SPI port, to perform different communications, ex.: RS-232 and IrDA, with system components or other products

such as PC, Notebook, and popular PDA. Three clocking outputs can produce synthesized PWM signals or high frequency carrier for IR remote control. This helps products become more useful in our daily life.

The built-in four-channel PSG are designed to generate key tone, melody, voice, and speech. Two dedicated pins with large driving capacity can drive a buzzer/speaker directly.

The ST2601B has a Low Voltage Detector (LVD) for power management usage. The status of internal or external power can be detected and reported to the management software.

Power bouncing during power-on is a major problem when designing a reliable system. The ST2601B equips a Low Voltage Reset function to keep the whole system in reset status when power is low. After the power returns to normal level, the system may recover its original states and keeps working correctly.

With these integrated functions inside, the ST2601B single chip microcontroller is a right solution for PDA, translator, databank and other consumer products.

The block diagram of ST2601B is shown in the above figure.

4. SIGNAL DESCRIPTIONS

Signal Function Groups

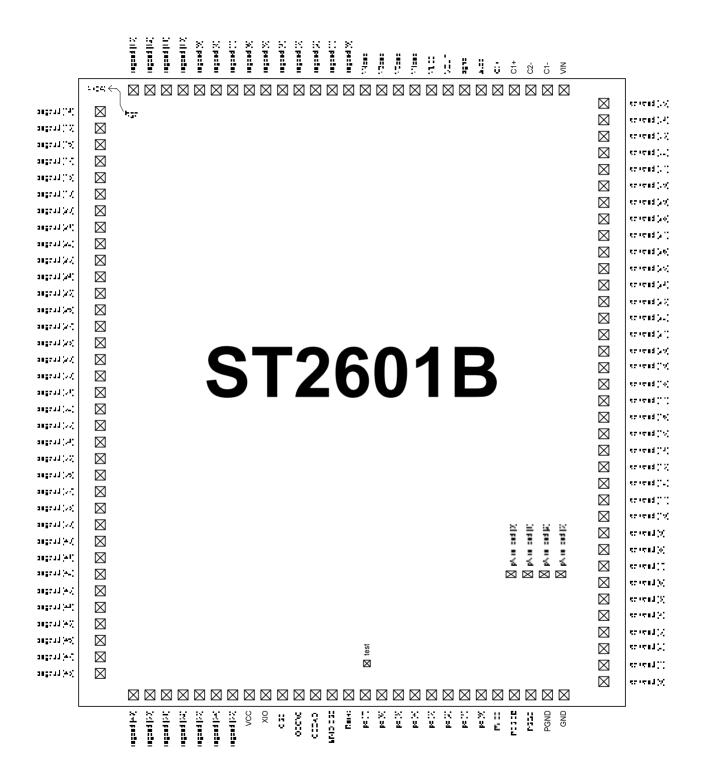
Signal Function Groups						
Function Group	Pad No.	Designation	Description			
			VCC: Power supply for system			
Power		VCC , PVCC, AVCC	AVCC: Power supply for LCD function			
			PVCC: Power supply for PSGO and PSGOB			
			GND: System power ground			
Ground		GND , PGND, AGND	AGND: Power ground for LCD function			
			PGND: Power ground for PSGO and PSGOB			
			RESET: Active low system reset signal input			
			TEST: Leave this pin open when normal operation			
			MMD/ $\overline{\mathrm{CS0}}$: Memory modes selection pin			
		RESET,	Normal mode: Enable internal ROM.			
System control		TEST,	MMD/CS0 is connected to GND.			
		MMD/CS0	Emulation mode: Disable internal ROM.			
			MMD/CS0 is connected to the chip-select pin of external ROM. During reset period, the MMD/CS0 is an internally pulled-up input pin. After reset cycles, MMD/CS0 is changed to be an output pin. It will output signal CS0.			
			High frequency oscillator (OSC) mode selected by code-option			
		XIO,OSCI	Crystal mode: One crystal or resonator should be connected between OSCI and XIO			
Clock		OSCXO,OSCXI, ,	Resistor oscillator mode: One resistor should be connected between OSCI and VCC			
			OSCXI, OSCXO: Connect one 32768Hz crystal between these two pins when using low frequency oscillator			
		WR / SEG9,	External memory R/W control signals / LCD Segment drivers			
External memory bus signals		RD / SEG8				
/ LCD drivers		A[22:0]/SEG32~SEG10	External memory address bus / LCD Segment drivers			
		D[7:0]/SEG7~SEG0	External memory data bus / LCD Segment drivers			
PSG/PWM DAC		PSGO, PSGOB	PSG outputs. Connect to one buzzer or speaker			
Chip selects / LCD		CS5 ~ 1/PD4~0 / SEG33~SEG37,	I/O port D and chip-select outputs / LCD Segment drivers			
drivers		CS6 /A23/PD5 /SEG38				
UART		RXD0/PC7,TXD0/PC6, RXD1/PD7/SEG40,TXD1/ PD6/SEG39	UART signals and I/Os / LCD Segment drivers			
SPI		DATA_READY /PC5 , SS/PC4 , SDO/PC3 , SDI/PC2 , SCK/PC1	SPI signals and I/Os			



Signal Function Groups (continued)

Signal Function Groups (continued)								
Function Group	Pad No.	Designation	Description					
External clock/signal interrupt		INTX/PC0	External interrupt inputs					
Clocking output		BCO/PE2/SEG43 , TCO1/PE1/SEG42 , TCO0/PE0/SEG41	Clocking outputs / LCD Segment drivers					
GPIO / LCD drivers		PE6~3/SEG47~SEG44	I/O port E/ LCD Segment drivers					
LCD control signals (for controller mode)		BLANK/COM0, POFF/COM1, FLM/COM2, LOAD1/COM3, LOAD2/COM4, AC/COM5,CP/COM6, EIO/COM7, LD7~LD0/COM15/COM8	LCD control signals					
LCD voltage source		Vout, Vlcd, V1, V2, V3, V4	LCD voltage sources					
LCD voltage booster		C1+, C1-, C2+, C2-	Connect a 0.1 uF between C1+ and C1-, C2+ and C2-repectively.					
Low Voltage Detector		VIN	Analog input pin of Low Voltage Dector module					

5. PAD DIAGRAM



6. ELECTRICAL CHARACTERISTICS

Absolute Maximum Rations

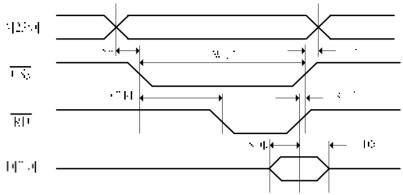
 *Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

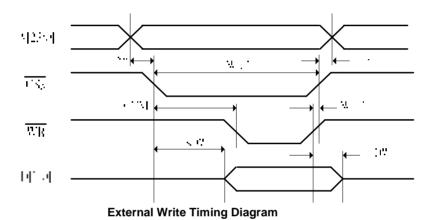
Standard operation conditions: VCC = 3.0V, GND = 0V, T_A = 25°C, OSC = 4M Hz, unless otherwise specified

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
Operating Voltage	V/00	2.4	3.0	3.6	V	Fosc = 3MHz	
Operating voltage	VCC	2.7	3.0	3.6	V	Fosc = 4MHz	
Operating Frequency	F ₁	-	-	3	MHz	VCC = 2.4V ~ 3.6V	
Operating Frequency	F ₂	-	-	4	MHz	VCC = 2.7 ~ 3.6V	
Operating Current	I _{OP}		2.5	3	mA	All I/O port are input and pull-up, execute NOP instruction, LCDC on	
Standby Current	I _{SB0}		450	550	μΑ	All I/O port are input and pull-up, OSCX on, LCDC off (WAIT0 mode)	
Standby Current	I _{SB1}		3.5	5	μΑ	All I/O port are input and pull-up, OSCX on, LCDC off (WAIT1 mode)	
Standby Current	I _{SB2}		0.5	1	μА	All I/O port are input and pull-up, OSCX off, LCDC off (WAIT1 mode)	
Standby Current	I _{SB3}		100	130	υΑ	LCD on, LCDCK=32Kz, Wait0, no panel	
Input High Voltage	V _{IH}	0.7Vcc		Vcc+0.3	V	Port-C/D/E/L	
		0.85Vcc			V	RESET	
Input Low Voltage	V _{IL}	GND-0.3		0.3Vcc	V	Port-C/D/E/L	
				0.15Vccc	V	RESET	
Pull-up resistance	R _{IH}		150		ΚΩ	Port-C/D/E/L (input Voltage=0.7VCC)	
Output high voltage	V _{OH1}	0.7Vcc			V	Port-C/D/L (I _{OH} =-6mA)	
Output low voltage	V_{OL1}			0.3Vcc	V	Port-C/D/E/L (I _{OL} =9mA)	
Output high voltage	V_{OH2}	0.7Vcc			V	PSG, I _{OH} = -35mA.	
Output low voltage	V_{OL2}			0.3Vcc	V	PSG, I _{OL} = 65mA.	
DAC current						Maximum of I = 3mA	
Low Voltage Detector current	ILVR		30	60	μΑ	Total LVD current consumption	
Vlcd variation		-3%		+3%			
INT LVD variation		-4%		+4%			
EXT LVD variation		-4%		+4%			

AC Electrical Characteristics



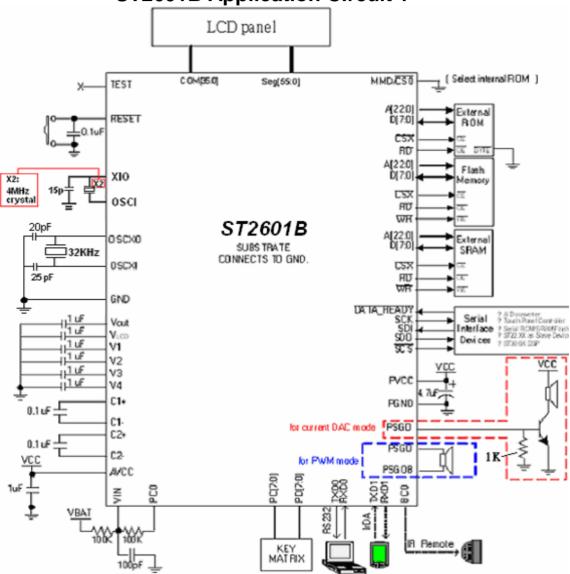
External Read Timing Diagram



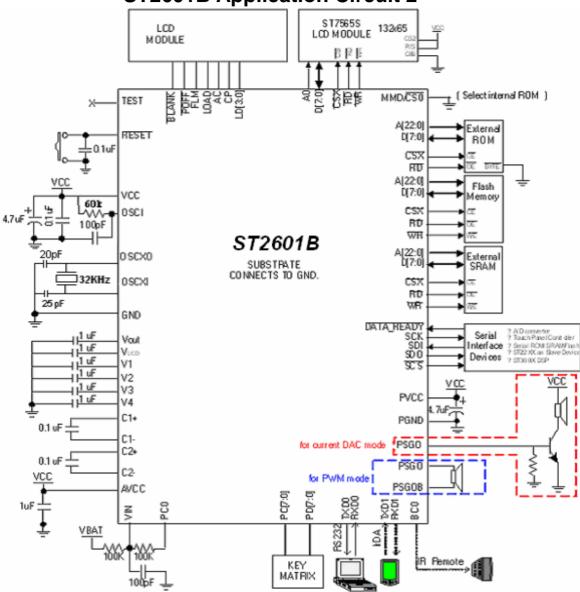
Symbol	Characteristic		Unit		
Cyllibol	Ondidoteriotic	Min.	Тур.	Max.	Oilit
tSA	Address setup time	_	1	10	ns
tHA	Address hold time	0		—	ns
tWLC	CS "L" pulse width	166		—	ns
tCLWL	CS asserted to WR asserted	_	1/2 tWLC	_	ns
tWHCH	CS negated after WR is negated	10	_	_	ns
tSDW	CS asserted to data-out is valid	_	1/2 tWLC	_	ns
tHDW	Data-out hold time after $\overline{\mathrm{WR}}$ is negated	20			ns
tCLRL	CS asserted to RD asserted		1/2 tWLC	_	ns
tRHCH	CS negated after RD is negated	10	1	_	ns
tSDR	Data-in valid before \overline{RD} is negated	30	1	_	ns
tHDR	Data-in hold time after RD is negated	10	1	_	ns
tR	Signal rise time	_	20	_	ns
tF	Signal fall time	_	10	_	ns

7. APPLICATION CIRCUITS

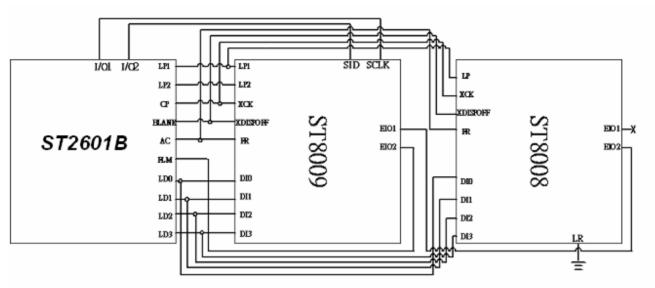








ST2601B+ST8008+ST8009 Application Circuit



Note:

LR pin of ST8008 is connected to GND.

L/R bit of ST8009 is configured as low by "interface control selection" instruction

8. FEATURE COMPARISON OF ST2600 SERIES

Part Number	ST2608B	ST2604B	ST2602B	ST2601B			
ROM	1M Byte	Byte 512K Byte 256K Byte		128K Byte			
RAM	5K Byte 3.5K Byte 2.5K Byte			1.5K Byte			
Built-in LCD Driver	36 COMs X 72 SEGs	36 COMs X 64 SEGs	36 COMs X 56 SEGs	36 COMs X 56 SEGs			
Driving LCD with	~9000 dots (16 gray)	~6000 dots (16 gray)	~4000 dots (16 gray)	~2500 dots (16 gray)			
ext. driver	~36000 dots (mono)	~24000 dots (mono)	~16000 dots (mono)	~10000 dots (mono)			
Dedicated I/O	24 (PA, PC, PL)	16 (PA, PC)	8 (PC)	8 (PC)			
LCD-Shared I/O	32 (PB, PD, PE, PF)	39 (PB[6:0], PD, PE, PL, PF) 31 (PD, PE[6:0], PL, PF)		31 (PD, PE[6:0], PL, PF)			
LCD gray level	Up to 16 gray levels						
PSG /	4-channel wavetable / 64 levels						
volume-control	4-criainei wavetable / 64 levels						
DAC	9-bit PWM, 12-bit current DAC						
Low voltage	Internal / External 4 levels						
detector	internal / External 4 levels						
Low voltage reset	Yes						
Watchdog timer	Yes						
Serieal interface	UART, SPI, IrDA						
LCDCK= 32KHz	YES						
Trimming Fuse	YES						

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