ST2204B

PRELIMINARY

8 BIT Integrated Microcontroller with 512K Bytes ROM

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1. FEATURES

- **Totally static 8-bit CPU**
- **ROM: 512K x 8-bit**
- **RAM: 10K x 8-bit**
- **Stack: Up to 128-level deep**
- **Operation voltage: 2.4V ~ 3.6V**
- **Operation frequency:**
  - 6.0Mhz@2.4V(Min.)
  - 8.0Mhz@3.1V(Min.)
- **Low Voltage Detector (LVD)**
- **Low Voltage Reset (LVR)**
- **Memory interface to ROM, RAM, Flash**
- **Memory configuration**
  - Three kinds of bank for program, data and interrupts
  - 12-bit bank register supports up to 44M bytes
  - 6 programmable chip-selects with 4 modes
  - Maximum single device of 16M bytes at $\overline{CS5}$
- **General-Purpose I/O (GPIO) ports**
  - 48 multiplexed CMOS bidirectional bit programmable I/Os
  - Hardware de-bounce option for Port-A
  - Bit programmable pull-up for input pins
  - Bit programmable pull-up/down and open-drain/CMOS for Port-C
- **Programmable Watchdog Timer (WDT)**
- **Timer/Counter**
  - Two 8-bit timer, one can be a 16-bit event counter
  - One 8-bit Base timer with 5 coexistent interrupt time settings
- **Three clocking outputs**
  - Clock sources including Timer0/1, baud rate generator
- **11 prioritized interrupts with dedicated exception vectors**
  - External interrupt (edge triggered)
  - TIMER0 interrupt
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA interrupt (transition triggered)
  - DAC reload interrupt
  - LCD buffer interrupt
  - SPI interrupt (x2)
  - UART interrupts (x2)
- **Dual clock sources with warm-up timer**
  - Low frequency crystal oscillator (OSCX) ..... 32768 Hz
  - RC oscillator (OSC) ..... 500K ~ 4M Hz
  - High frequency crystal/resonator oscillator (Bonding option)..... 455K~4M Hz
- **Direct Memory Access (DMA)**
  - Block-to-Block transfer
  - Block to Single port
- **LCD Controller (LCDC)**
  - Software programmable screen size up to 320X240
  - Support 1-, 4-bit LCD data bus
  - Share system memory with display memory
  - Large display area with small internal RAM buffer is possible to free more internal RAM for temporary access
  - Unique internal bus for memory sharing with no loss of the CPU time
  - Diverse functions including virtual screen, panning, scrolling, contrast control and alternating signal generator
  - Gray level support: Hardware 4 levels/Software 31 levels
- **Universal Asynchronous Receiver/Transmitter (UART)**
  - Full-duplex operation
  - Baud rate generator with one digital PLL
  - Standard baud rates of 600 bps to 115.2 kbps
  - Direct glueless support of IrDA physical layer protocol
  - Two sets of I/Os (TX,RX) for two independent devices
- **Serial Peripheral Interface (SPI)**
  - Master and slave modes
  - 5 serial signals including enable and data-ready
  - One stage buffer for transmitter and receiver for continuous data exchange
  - Programmable data length from 7-bit to 16-bit
- **Programmable Sound Generator (PSG)**
  - Two channels with three playing modes
  - Tone/noise generator
  - 16-level volume control
  - 8-bit PWM DAC for speech/voice
  - Two dedicated outputs for directly driving and large current
- **Three power down modes**
  - WAI0 mode
  - WAI1 mode
  - STP mode

2. GENERAL DESCRIPTION

The ST2204B is a 8-bit integrated microcontroller designed with CMOS silicon gate technology. The true static CPU core, power down modes and dual oscillators design makes the ST2204B suitable for power saving and long battery life designs. The ST2204B integrates various logic to support functions on-chip which are needed by system designers. This is also important for lower system complexity, small board size and, of course, shorter time to market and less cost.

The ST2204B features the capacity of memory access of maximum 44M bytes which is needed by products with large data bases, and also DMA function for fast memory transfer. Six chip selects are equipped for direct connection to external ROM, SRAM, Flash memory or other devices. Maximum one single device of 16M bytes is possible.

The ST2204B has 48 I/Os grouped into 6 ports, Port-A ~ Port-E and Port-L. Each pin can be programmed to input or output. There are two options: pull-up/down for inputs of Port-C and only pull-up for inputs of the other ports. In case of output, there are open-drain/CMOS options for outputs of PortC and only CMOS for the other ports. Port-A/B is designed for keyboard scan with de-bounce and transition triggered interrupt at Port-A, while Port-C/D/E/L are shared with other system functions. All the properties of I/O pins are still programmable when they are assigned to another function. This enlarges the flexibility of the usage of function signals.

The ability of driving large LCD panels, up to 320x240, and hardware/software gray-level support may rich the display information and the diversity of contents as well. This is done with no need of external display RAM because of the internal memory sharing design. The variable LCD buffer design also make large panel size with little internal RAM possible. User may free major internal RAM for computing or temporary access while keeping the display content.

The ST2204B equips serial communication ports of one UART and one SPI to perform different communications, ex.: RS-232 and IrDA, with system components or other products such as PC, Notebook, and popular PDA. Three clocking outputs can produce synthesized PWM signals or high frequency carrier for IR remote control. This helps products become more useful in our daily life.

The built-in two channel PSG/one channel PWM DAC are for the production of key tone, melody, voice, and speech. Two dedicated pins with large driving capacity can drive a buzzer/speaker directly for minimum cost.

The ST2204B has one Low Voltage Detector (LVD) for power management. The status of internal or external power can be detected and reported to the management software.

Power bouncing during power on is a major problem when designing a reliable system. The ST2204B equips Low Voltage Reset function to keep whole system in reset status when power is low. After the power backs to normal, the system may recover its original states and keeps working correctly.

With these integrated functions inside, the ST2204B single chip microcontroller is a right solution for PDA, translator, databank and other consumer products.

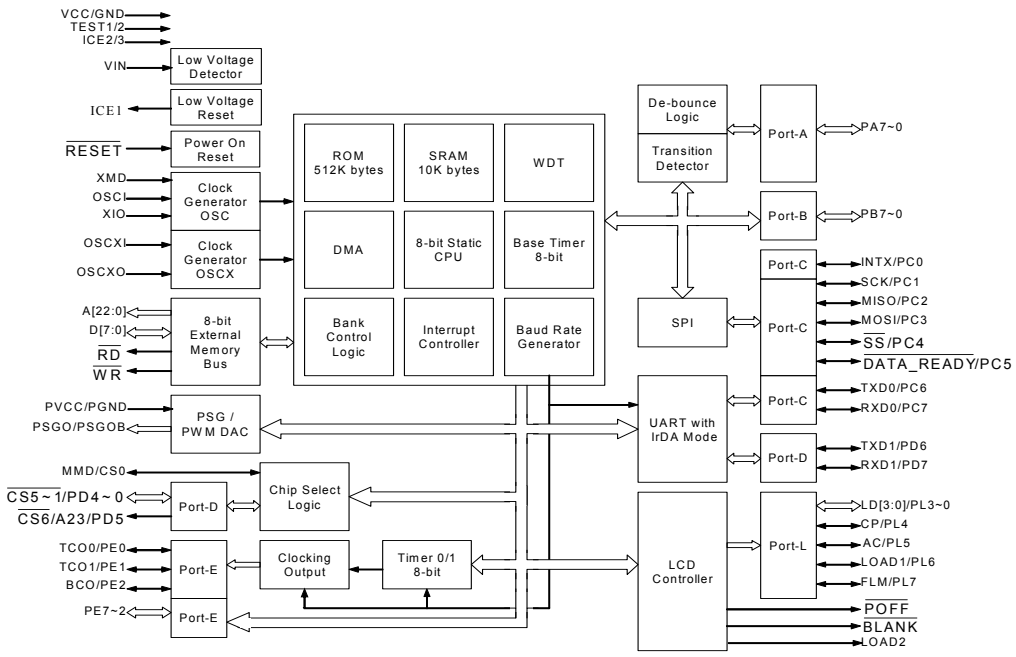


FIGURE 2-1 ST2204B Block Diagram

3. SIGNAL DESCRIPTIONS

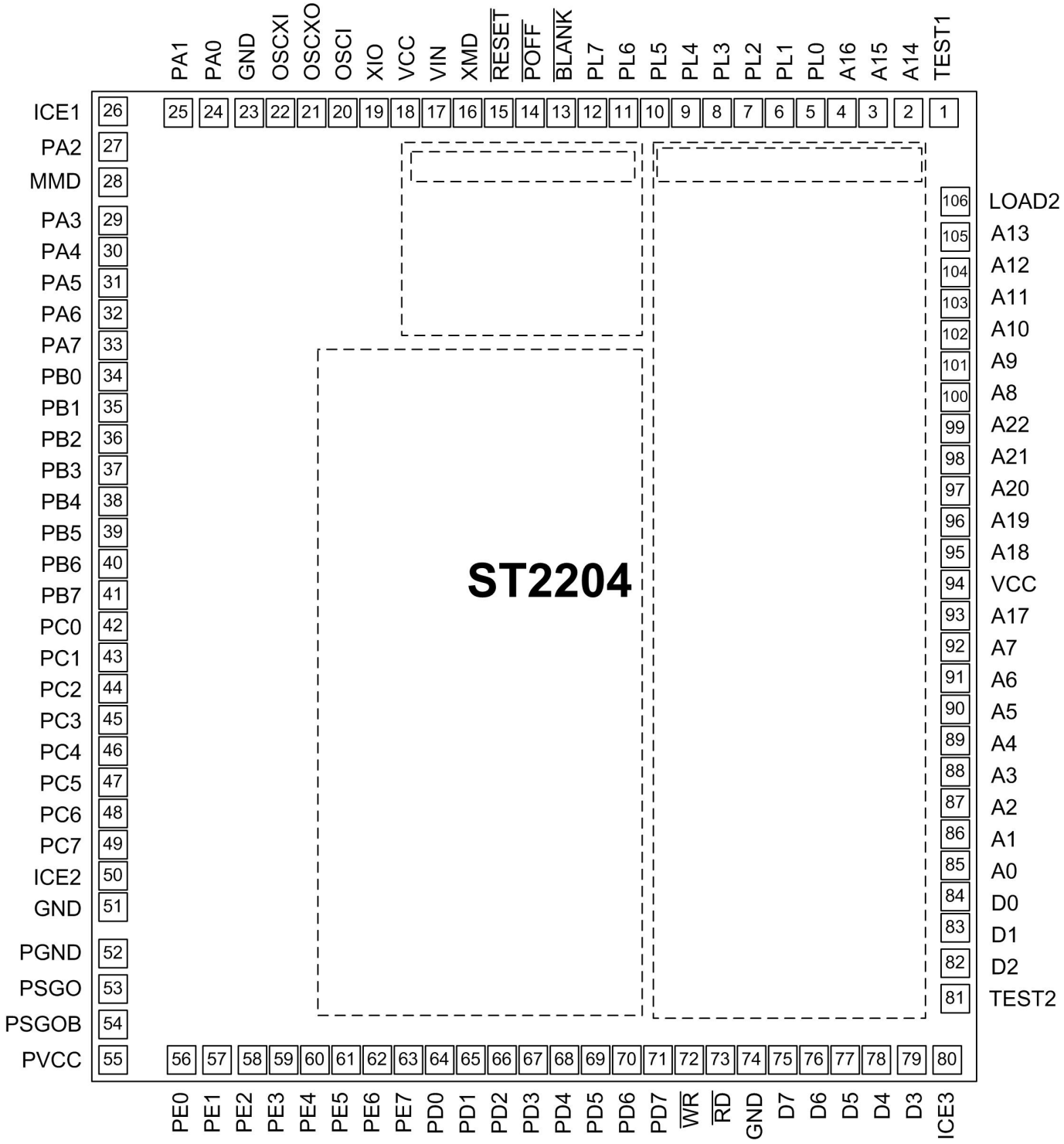
TABLE 3-1 Signal Function Groups

Function Group	Pad No.	Designation	Description
Power	18, 55, 94	VCC , PVCC	**VCC:** Power supply for system **PVCC:** Power supply for PSGO and PSGOB
Ground	23, 51, 52, 74	GND , PGND	**GND:** System power ground **PGND:** Power ground for PSGO and PSGOB
System control	15, 26,50,80 1,81 28	$\overline{\text{RESET}}$, ICE1/2/3, TEST1/2, MMD/$\overline{\text{CS0}}$	$\overline{\textbf{RESET}}$ **:** Active low system reset signal input **TEST1/2, ICE1/2/3:** Leave them open when normal operation **MMD/CS0:** Memory modes selection pin **Normal mode:** Enable internal ROM. MMD/$\overline{\text{CS0}}$ connects to GND. **Emulation mode:** Disable internal ROM. MMD/$\overline{\text{CS0}}$ connects to chip-select pin of external ROM. One resistor should be added between VCC and this pin. After reset cycles, MMD/$\overline{\text{CS0}}$ changes to be an output, and outputs signal $\overline{\text{CS0}}$.
Clock	16, 19~22	XMD, XIO,OSCI OSCXO,OSCXI, ,	**XMD:** High frequency oscillator (OSC) mode selection input **Low:** Crystal mode. One crystal or resonator should be connected between OSCI and XIO **High:** Resistor oscillator mode. One resistor should be connected between OSCI and VCC **OSCXI, OSCXO:** Connect one 32768Hz crystal between these two pins when using low frequency oscillator
External memory bus signals	72, 73	$\overline{\text{WR}}$, $\overline{\text{RD}}$	External memory R/W control signals
	2~4, 85~93, 95~105	A[22:0]	External memory address bus
	75~79, 82~84	D[7:0]	External memory data bus
PSG/PWM DAC	53, 54	PSGO, PSGOB	PSG outputs. Connect to one buzzer or speaker
Keyboard scan signal (return line)	24~25, 27,29~33	PA7~0	I/O port A
GPIO	34~41	PB7~0	I/O port B
Chip selects	64~69	$\overline{\text{CS5 ~ 1}}$/PD4~0, $\overline{\text{CS6}}$ /A23/PD5	I/O port D and chip-select outputs
UART	48, 49, 70, 71	RXD0/PC7,TXD0/PC6, RXD1/PD7,TXD1/PD6	UART signals and I/Os
SPI	43~47	$\overline{\text{DATA\_READY}}$ /PC5 , $\overline{\text{SS}}$ /PC4 , MOSI/PC3 , MISO/PC2 , SCK/PC1	SPI signals and I/Os

TABLE 3-2 Signal Function Groups (continued)

Function Group	Pad No.	Designation	Description
External clock/signal interrupt	42	INTX/PC0	External interrupt inputs
Clocking output	56~58	BCO/PE2 , TCO1/PE1 , TCO0/PE0	Clocking outputs
GPIO	59~63	PE7~3	I/O port E
LCD control signals	5~14, 106	FLM/PL7, LOAD1/PL6, AC/PL5 , CP/PL4, $\overline{LD[3:0]}$/PL3~0, $\overline{POFF}$, $\overline{BLANK}$,LOAD2	LCD control signals

4. PAD DIAGRAM



5. DEVICE INFORMATION

1. **Pad size: 90um x 90um**
2. **Substrate: GND**
3. **Chip size: 3120um x 3560um**

PAD No.	Symbol	X	Y
1	TEST1	1445.0	1704.3
2	A14	1320.0	1704.3
3	A15	1195.0	1704.3
4	A16	1085.0	1704.3
5	PL0	975.0	1704.3
6	PL1	865.0	1704.3
7	PL2	755.0	1704.3
8	PL3	645.0	1704.3
9	PL4	535.0	1704.3
10	PL5	425.0	1704.3
11	PL6	315.0	1704.3
12	PL7	205.0	1704.3
13	$\overline{\text{BLANK}}$	95.0	1704.3
14	$\overline{\text{POFF}}$	-15.0	1704.3
15	$\overline{\text{RESET}}$	-125.0	1704.3
16	XMD	-235.0	1704.3
17	VIN	-345.0	1704.3
18	VCC	-455.0	1704.3
19	XIO	-565.0	1704.3
20	OSCI	-675.0	1704.3
21	OSCXO	-785.0	1704.3
22	OSCXI	-895.0	1704.3
23	GND	-1005.0	1704.3
24	PA0	-1130.0	1704.3
25	PA1	-1255.0	1704.3
26	$\overline{\text{LVR}}$ \ICE1	-1485.0	1704.3
27	PA2	-1485.0	1579.3
28	MMD	-1485.0	1459.8
29	PA3	-1485.0	1320.8
30	PA4	-1485.0	1207.8
31	PA5	-1485.0	1094.8
32	PA6	-1485.0	981.8
33	PA7	-1485.0	868.8
34	PB0	-1485.0	755.8
35	PB1	-1485.0	642.8

PAD No.	Symbol	X	Y
36	PB2	-1485.0	529.8
37	PB3	-1485.0	416.8
38	PB4	-1485.0	303.8
39	PB5	-1485.0	190.8
40	PB6	-1485.0	77.8
41	PB7	-1485.0	-35.3
42	PC0	-1485.0	-148.3
43	PC1	-1485.0	-261.3
44	PC2	-1485.0	-374.3
45	PC3	-1485.0	-487.3
46	PC4	-1485.0	-600.3
47	PC5	-1485.0	-713.3
48	PC6	-1485.0	-826.3
49	PC7	-1485.0	-939.3
50	ICE2	-1485.0	-1052.5
51	GND	-1485.0	-1165.3
52	PGND	-1485.0	-1329.3
53	PSGO	-1485.0	-1454.3
54	PSGOB	-1485.0	-1579.3
55	PVCC	-1485.0	-1704.3
56	PE0	-1243.4	-1704.3
57	PE1	-1118.4	-1704.3
58	PE2	-993.4	-1704.3
59	PE3	-883.4	-1704.3
60	PE4	-773.4	-1704.3
61	PE5	-663.4	-1704.3
62	PE6	-553.4	-1704.3
63	PE7	-443.4	-1704.3
64	PD0	-333.4	-1704.3
65	PD1	-223.4	-1704.3
66	PD2	-113.4	-1704.3
67	PD3	-3.4	-1704.3
68	PD4	106.6	-1704.3
69	PD5	216.6	-1704.3
70	PD6	326.6	-1704.3

PAD No.	Symbol	X	Y
71	PD7	436.6	-1704.3
72	$\overline{\text{WR}}$	546.6	-1704.3
73	$\overline{\text{RD}}$	656.6	-1704.3
74	GND	766.6	-1704.3
75	D7	876.6	-1704.3
76	D6	986.6	-1704.3
77	D5	1096.6	-1704.3
78	D4	1206.6	-1704.3
79	D3	1331.6	-1704.3
80	ICE3	1456.6	-1704.3
81	TEST2	1485.0	-1488.3
82	D2	1485.0	-1363.3
83	D1	1485.0	-1238.3
84	D0	1485.0	-1125.3
85	A0	1485.0	-1012.3
86	A1	1485.0	-899.3
87	A2	1485.0	-786.3
88	A3	1485.0	-673.3
89	A4	1485.0	-560.3
90	A5	1485.0	-447.3
91	A6	1485.0	-334.3
92	A7	1485.0	-221.3
93	A17	1485.0	-108.3
94	VCC	1485.0	4.8
95	A18	1485.0	117.8
96	A19	1485.0	230.8
97	A20	1485.0	343.8
98	A21	1485.0	456.8
99	A22	1485.0	569.8
100	A8	1485.0	682.8
101	A9	1485.0	795.8
102	A10	1485.0	908.8
103	A11	1485.0	1021.8
104	A12	1485.0	1134.8
105	A13	1485.0	1261.8
106	LOAD2	1485.0	1391.8

6. INTERRUPT CONTROLLER

The ST2204B supports 11 hardware internal/external interrupts as well as one software interrupt Brk. There are 12 exception vectors for these interrupts and another one for reset. All interrupts are controlled by interrupt disable flag "**I**" (bit2 of status register **P**), and initiate if "**I**" equals "0". Hardware interrupts are further controlled by interrupt enable register **IENA**. Setting bits of **IENA** enables respective interrupts.

The interrupt controller owns one priority arbitrator. When more than one interrupts happen at the same time, the one with lower priority number will be executed first. Refer to TABLE 6-1 for priorities of interrupts.

Once an interrupt event was enabled and then happens, the CPU wakes up (if in either wait mode), and associated bit of interrupt request register (**IREQ**) will be set. If "**I**" flag is cleared, the related vector will be fetched and then the interrupt service routine (ISR) will be executed. Interrupt request flag can be cleared by two methods. One is to write "0" to **IREQ**, the other is to initiate related interrupt service routine. Hardware will automatically clear the Interrupt request flag. All interrupt vectors are listed in TABLE 6-1.

TABLE 6-1 Interrupt Vectors

Name	Signal Source	Vector Address	Priority	Description
BRK	Internal	$7FFF,$7FFE	1	Software BRK operation vector
RESET	External	$7FFD,$7FFC	0	Reset vector
-	-	$7FFB,$7FFA	-	Reserved
INTX	External	$7FF9,$7FF8	6	PC0 edge interrupt
DAC	Internal	$7FF7,$7FF6	7	Reload DAC data interrupt
T0	Internal/External	$7FF5,$7FF4	8	Timer0 interrupt
T1	Internal/External	$7FF3,$7FF2	9	Timer1 interrupt
PT	External	$7FF1,$7FF0	10	Port-A transition interrupt
BT	Internal	$7FEF,$7FEE	11	Base Timer interrupt
LCD	Internal	$7FED,$7FEC	12	LCD Frame interrupt
-	-	$7FEB,$7FEA	-	Reserved
STX	External	$7FE9,$7FE8	2	SPI transmit buffer empty interrupt
SRX	External	$7FE7,$7FE6	3	SPI receive buffer ready interrupt
UTX	External	$7FE5,$7FE4	4	UART receiver interrupt
URX	External	$7FE3,$7FE2	5	UART transmitter interrupt

7. GPIO

The ST2204B consists of 48 general-purpose I/O (GPIO) which are divided into six I/O ports: Port-A/B/C/D/E and Port-L.

Each single pin can be programmed to be input or output. This is controlled by port direction control registers **PCx**. Setting bit of **PCx** makes respective pin to output, and clearing this bit for input. There are two options: pull-up/down for inputs of Port-C but only pull-up for inputs of the other ports. In case of output, there are open-drain/CMOS options for outputs of PortC but only CMOS for the other ports. Refer to TABLE 7-1.

TABLE 7-1 I/O Types Of GPIO Ports

I/O Mode	I/O Types	
	Port-A/B/D/E/L	Port-C
Input	Pull-up/Pure	Pull-up/Pull-down/Pure
Output	CMOS	Open-drain/CMOS

■ Input Mode

In case of input function, port data registers **Px** reflect the values on associated pins. Besides read instruction for data of signals input, writing to register **Px** selects I/O types of pins, pull-up or pull-down. Setting bits of all port data register **Px** to select pull-up type. Clearing bits of only **PC** to select pull-down type for pins of Port-C. There are no pull-down resistors for Port-A/B/D/E and Port-L, thereby no pull-down resistors will be enabled if clearing bits of **PA**, **PB**, **PD**, **PE** and **PL**. Pull-up resistors of Port-A/B/D/E/L are also controlled by PULL bit (bit7 of port miscellaneous register **PMCR**), “0” is to disable, while “1” is to enable them. The pull-up/pull-down resistors of Port-C are further controlled by bits of port type select registers **PSC**. They work in the same way with PULL bit of **PMCR** but only on single pin, “0” is to disable, while “1” is to enable.

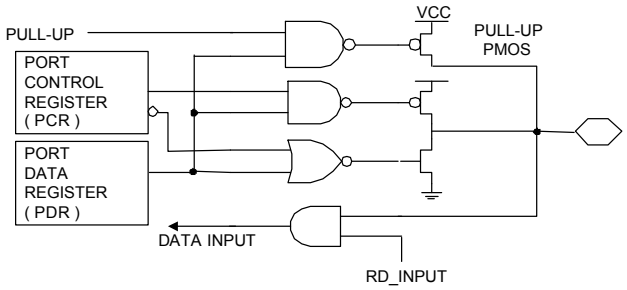


FIGURE 7-1 Configuration Of Port-A/B/D/E/L

■ Output Mode

In case of output function, Write to port data registers **Px** makes pins to output desired value. This value can also be read back by read instruction. Besides Port-C, the output pins are CMOS type. Port-C have two options of output types: open-drain and CMOS, and is controlled by port type select registers **PSC**. Clearing bits of registers **PSC** is for that disable PMOS of output stage and left only NMOS, while setting bits is for CMOS.

Port-A is designed for keyboard scan with de-bounce and transition triggered interrupt, while Port-C/D/E are multiplexed with other system functions, and are controlled by **PFC**, **PFD**, and **PMCR[2:0]**. Port-L is shared with LCD specific signals of LCDC. Turning off LCDC by setting **LPWR** (**LCTR[7]**) reserves Port-L for GPIO.

Selecting respective pins to be GPIO or signals of system function will not affect original settings of I/O directions and types. This entends the flexibility of the usage of function signals.

Note: All the properties of pins are still programmable and must be ascertained before they are assigned to system functions, especially the direction of pins.

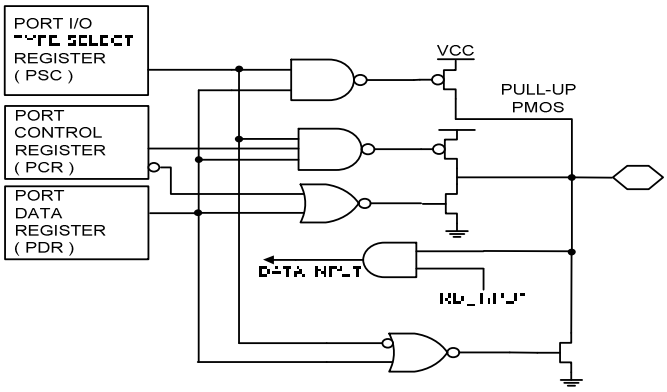


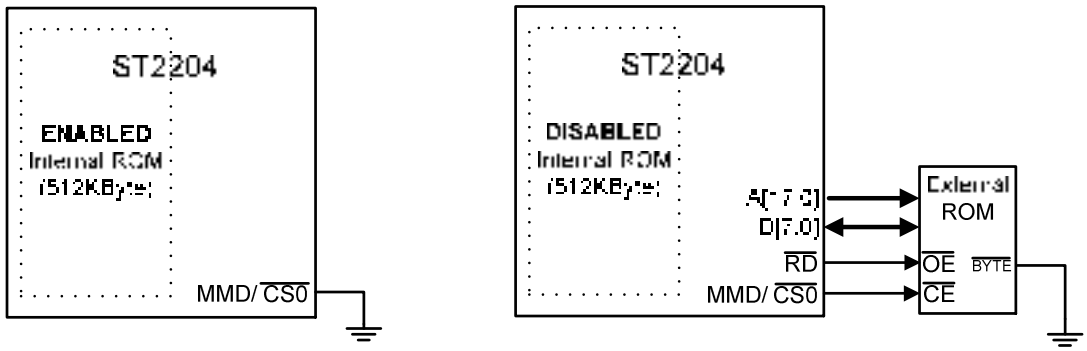
FIGURE 7-2 Configuration Of Port-C

8. CHIP-SELECT LOGIC (CSL)

The ST2204B builds in one chip-select signal ($\overline{CS0}$) for embedded 512K bytes mask ROM and six chip-select signals multiplexed with PD5~0 of Port-D which are used to select external devices on the address and data bus. There are two options for the first 512K bytes memory which are controlled by MMD pin. Tie MMD to ground to select normal mode and enable internal ROM for the first 512K bytes memory. Connect MMD to chip-select of an external device to select emulation mode and disable internal ROM. After reset cycles, MMD changes to an output and outputs chip-select signal $\overline{CS0}$. Refer to FIGURE 8-1 for two connections of different modes.

Two bits **CSM[1:0]** of port miscellaneous register (**PMCR**) select four modes of CSL which define the memory size of each external chip-select. If **CSM0** equals “1”, chip-select signal $\overline{CS6}$ changes to be address signal A23 to make one single device of 16M bytes at $\overline{CS5}$ possible. The address range of $\overline{CSx}$ of higher number follows the range of previous one of lower number.

Note: Write “1” to bit of port direction control register **PCD**, then to bit of port function-select register **PFD** to activate the designated chip-select signal.



A. Normal Mode **B. Emulation Mode**

FIGURE 8-1 Connections Of MMD/ $\overline{CS0}$

9. TIMER/EVENT COUNTER

The ST2204B has three timers, Base timer, Timer 0 and Timer 1, and two prescalers PRES and PREW. There are two clock sources, SYSCK and INTX, for PRES and one clock source, CLK32, for PREW. Refer to FIGURE 9-1

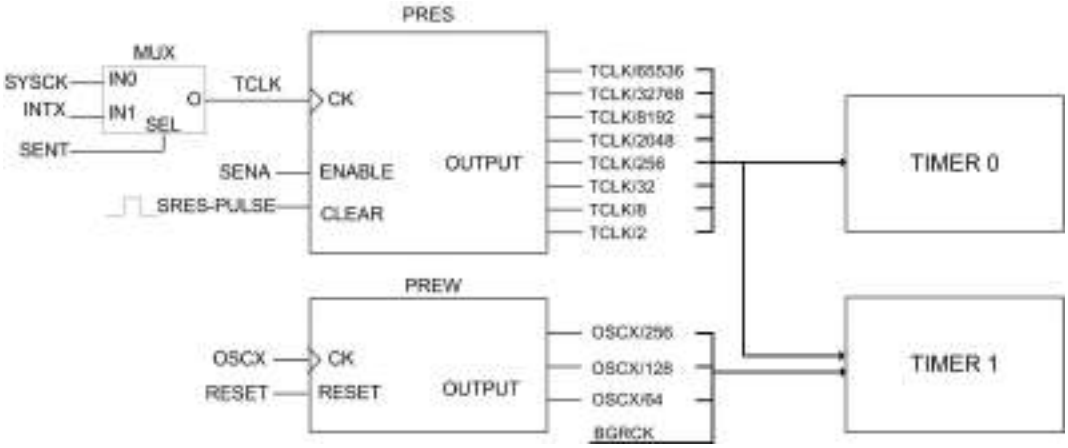


FIGURE 9-1 Structure Of Two Prescalers

■ **PRES**

The prescaler PRES is an 8-bits counter as shown in FIGURE 9-1. Which provides four clock sources for base timer and timer1, and it is controlled by register PRS. The instruction read toward PRS will bring out the content of PRES and the Instruction write toward PRS will reset, enable or select clock sources for PRES. When user set external interrupt as the input of PRES for event counter, combining PRES and Timer1 will get a 16bit-event counter.

■ **PREW**

The prescaler PREW is an 8-bits counter as shown in FIGURE 9-1. PREW provides four clocks source for base timer and timer1. It stops counting only if OSCX stops or hardware reset occurs.

9.1 Base Timer

The base timer supports one interrupt, which occurs at five different rates. Applications base on the base timer interrupt can chose an appropriate interrupt rate from five time bases for their specific needs. These real-time applications may include digitizer sampling, keyboard debouncing, or communication polling. Block diagram of base timer is shown in FIGURE 9-2.

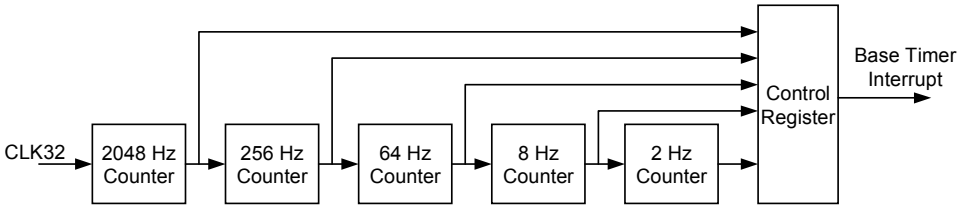


FIGURE 9-2 Base Timer Block Diagram

9.1.1 Base Timer Operations

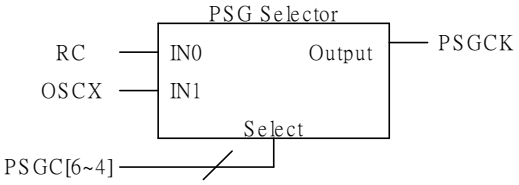
The base timer consists of five sub-counters to produce five predefined rates. The connections between overflow signals of these sub-counters and the base timer interrupt are controlled by respective bit fields of base timer enable register (**BTEN**). The enabled overflow signals are ORed to generate the base timer interrupt request. Related bits of base timer status register (**BTSR**) will show which rates of interrupts should be serviced. Write "1" to **BTCLR** (bit 7 of **BTSR)** may clear this register.

Note: Make sure **BTSR** is cleared after the interrupt was serviced, so that the request can be set next time

10. PSG

10.1 Function Description

The built-in dual channel Programmable Sound Generator (PSG) is controlled by register file directly. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms and tone signaling. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the CPU. The structure of PSG was shown in FIGURE 10-2 and the PSG clock source is shown in FIGURE 10-1. The ST2204B has three PSG playing type. One for channel0(C0) & channel1(C1) square type tone sound playing. Second for ch0 square tone sound and ch1 noise sound. The third sound playing type is DAC PCM playing.



PSGC			PSGCK
B6	B5	B4	
0	0	0	SYSCK/2
X	0	1	SYSCK/4
X	1	0	SYSCK/8
0	1	1	SYSCK/16
1	0	0	SYSCK
1	1	1	OSCX

FIGURE 10-1 PSG Clock Source Control

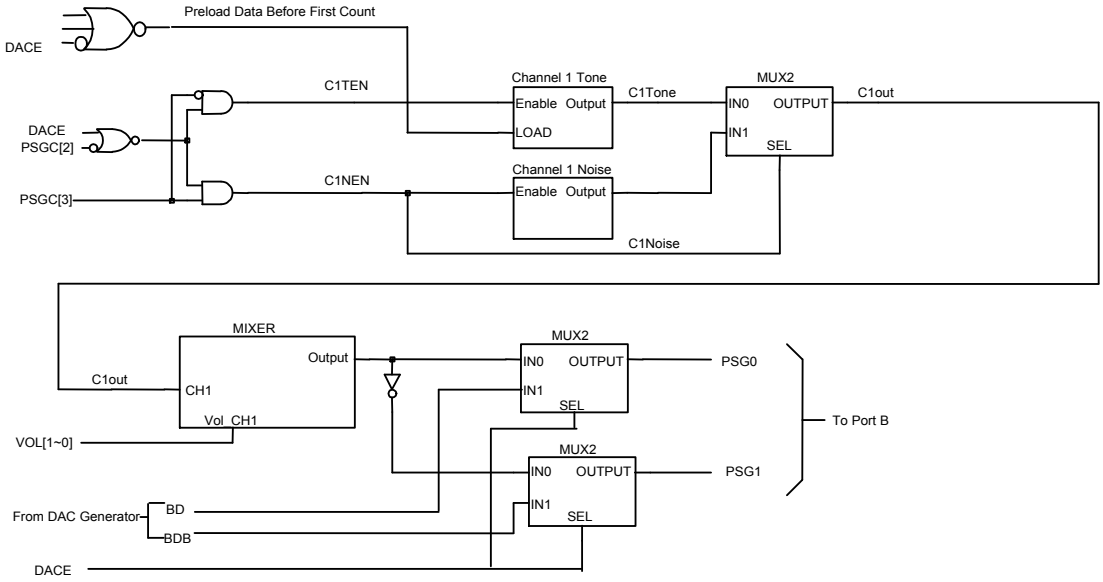


FIGURE 10-2 PSG Block Diagram

11. PWM DAC

A built-in PWM DAC is for analog sampling data or voice signals. There is an interrupt signal from DAC to CPU whenever DAC data update is needed and the same signal will decide the sampling rate of voice. In DAC mode, the frequency of RC oscillator can't less 2M Hz.

11.1 Sample Rate Control

PSG1L and PSG1H control the sample rate. PSG1[11~6] controls PWM repeat times (usually set=111100 for four times of DAC reload) and PSG1[5~0] usually set '1'. The input clock source is controlled by PCK[2~0]. The block diagram is shown as the following:

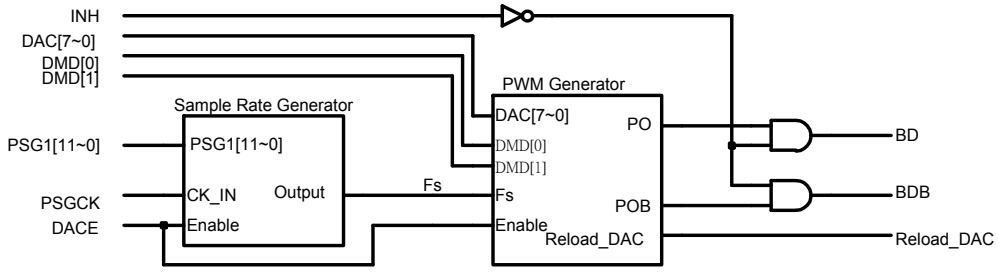
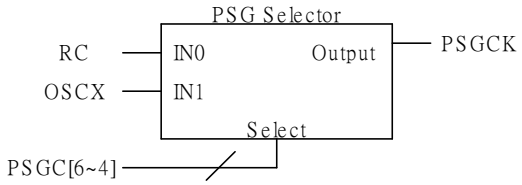


FIGURE 11-1 DAC Diagram



PSGC			PSGCK
B6	B5	B4	
0	0	0	SYSCK/2
X	0	1	SYSCK/4
X	1	0	SYSCK/8
0	1	1	SYSCK/16
1	0	0	SYSCK
1	1	1	OSCX

FIGURE 11-2 DAC Clock Source Control

12. LCD CONTROLLER (LCDC)

The LCD controller (LCDC) provides display data and specific signals for external LCD drivers to drive the STN LCD panels. The LCDC fetches display data directly from internal system memory through one unique memory bus. The special designed internal bus shares almost none of the CPU resources to make both fast display data process and high speed CPU operation possible. Both black-and-white and 4-gray-level are supported and is selected by **GL[0]** of control register **LCTR**.

The ST2204B builds in 10K bytes SRAM, so the maximum panel size can be 320x240 for B/W and 240x160 for 4-gray-level mode. The LCDC also supports software gray-level up to 31 levels for displaying pictures and photos.

The ST2204B supports 1- and 4-bit data bus for the compatibility of most popular LCD drivers. The LCD output signals are shared with Port-L., and are controlled by LCD power control bit **LPWR** (**LCTL[7]**) and data bus selection bit **LMOD** (**LCK[4]**). In case of 1-bit mode, PL3~1 of Port-L can still be used for general purpose.

Note: The LCD signals will be disconnected and Port-L will output values assigned by **PL** after clearing **LPWR**.

Various functions are also supported to rich the display information, including virtual screen, panning, scrolling, contrast control and an alternating signal generator. Control registers used by LCDC are listed below.

12.1 LCD Specific Signals

The following signals are generated by LCDC to connect the ST2204B and an LCD panel. Two of them are dedicated output pins, while the rest eight pins are multiplexed with Port-L.

■ FLM (PL7)

The LCD frame marker signal indicates the start of a new display frame. FLM becomes active after the last line pulse of the frame and remains active until the next line pulse, at which point it de-asserts and remains inactive until the next frame.

■ LOAD1 (PL6)

The LCD line pulse signal is used to latch a line of shifted data to the segment drivers' outputs and is also used to shift the line enable signal of common driver. All the driver outputs then control the liquid crystal to form the desired frame on panel.

■ AC (PL5)

The LCD alternate signal toggles the polarity of liquid crystal on the panel. This signal can be programmed to toggle for a period of 1 to 31 lines or one frame.

■ CP (PL4)

The LCD shift clock pulse signal is the clock output to which the output data to the LCD panel is synchronized. Data for segment drivers is shifted into the internal line buffer at each falling edge of CP.

■ LD3~0 (PL3~0)

The LCD data bus lines transfer pixel data to the LCD panel so that it can be displayed. Two kinds of data busses, 1- and 4-bit, are supported and are controlled by **LMOD** (**LCK[4]**). In case of 1-bit mode, **LMOD** should be cleared and the LCDC uses only LD0 to transfer data. LD3~1 can still be programmed to be normal inputs or outputs. The output pixel data can be inverted through programming. Setting **REV** (**LCTR**) will reverse the output data on data bus.

■ $\overline{\text{POFF}}$ (Power control)

The LCD power control signal is used to turn on/off the external DC-DC converter, which generates a high voltage for driving liquid crystal. $\overline{\text{POFF}}$ outputs "1" when clearing **LPWR** (**LCTR**), and outputs "0" by setting this bit, which is also the default value.

■ $\overline{\text{BLANK}}$ (Contrast control)

The LCD blank signal is used to control the contrast of display by setting contrast level in **LPWM[5:0]** with "00000" (default) represents a maximum level and "11111" is for minimum. The $\overline{\text{BLANK}}$ signal achieves this function by outputting a PWM signal according to the settings of contrast.

Besides contrast control, $\overline{\text{BLANK}}$ signal plays another role of turning display off. This is controlled by register bit **BLNK** (**LCTR**). Setting **BLNK** bit will make $\overline{\text{BLANK}}$ signal to output "0" to blank the display regardless of contrast control. Setting **BLNK** bit will enable the PWM contrast control and of course the $\overline{\text{BLANK}}$ signal. If **LPWMTR[5:0]** are all zeros, $\overline{\text{BLANK}}$ signal will stay at high level with no PWM modulation.

12.2 Mapping the Display Data

The screen width and height of the LCD panel are programmable through software. Although the maximum screen size can be up to 1024x512, the actual supported resolution is limited by the display buffer size, which is also the internal RAM size, and is 10K bytes. Instead of screen size specified by control registers, larger frame can also be displayed via the Virtual Page Width setting. FIGURE 12-1 illustrates the relationship between the portion of a large graphic to be displayed on the screen and the actual area that can be seen.

Each one or two bits in the display memory correspond to a pixel on the LCD panel. TABLE 12-2 shows the mapping of the display data to the LCD. When clear control bit **GL[0]** (**LCTR[2]**) and enable B/W mode, every bit of display buffer represents one pixel on the screen. In case of setting **GL[0]** and enable 4-gray-level mode, there will be two bits to present each pixel on the screen.

When in 4-gray-level mode, there are two kinds of light gray,1/2 and 1/3, can be selected by **GL[1]** (**LCTR[3]**). Refer to TABLE 12-2 for the relationship of data bits and the displayed pixel.

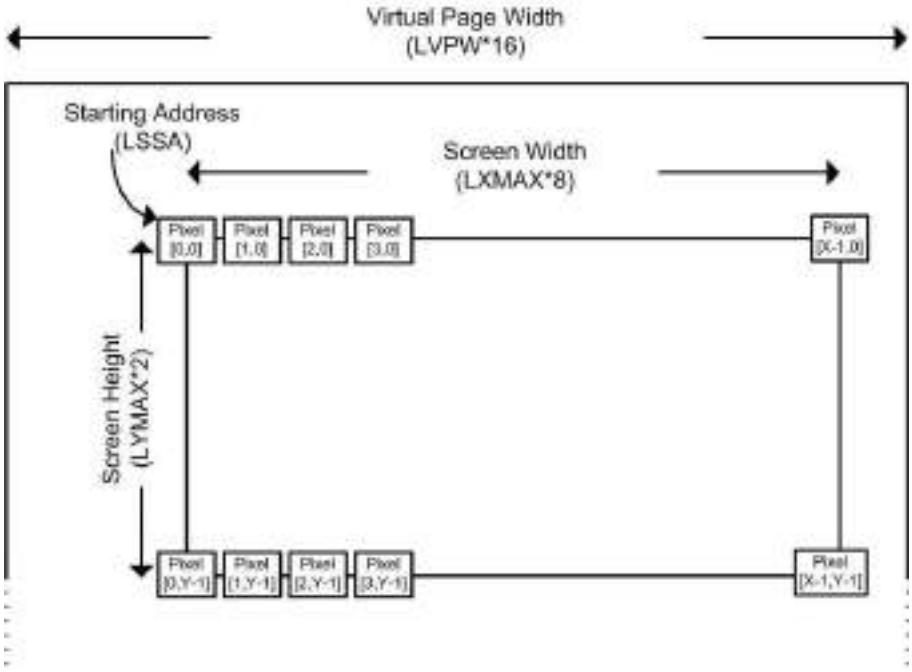


FIGURE 12-1 LCD Screen Format

TABLE 12-1 Mapping Memory Data on the Screen

A. 1-bit-per-pixel mode

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	…
Pixel [0,0]	Pixel [1,0]	Pixel [2,0]	Pixel [3,0]	Pixel [4,0]	Pixel [5,0]	Pixel [6,0]	Pixel [7,0]	Pixel 8,0]	Pixel [9,0]	…
:	:	:	:	:	:	:	:	:	:	…

B. 2-bit-per-pixel mode

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	…
Pixel [0,0]		Pixel [1,0]		Pixel [2,0]		Pixel [3,0]		Pixel [4,0]		…
:		:		:		:		:		…

TABLE 12-2 Mapping Memory Data to Screen Pixel

Display Mode	Data	Pixel
B/W	0	White
	1	Dark
4-Gray-Level	00	White
	01	1/2(1/3) gray
	10	2/3 gray
	11	Dark

for normal white panel

12.3 LCD Interface Timing

The LCD controller continuously pumps the pixel data into the LCD panel via the LCD data bus. The bus is timed by the CP, LOAD, and FLM signals. Two kinds of data width, 1- and 4-bit, are supported for most monochrome LCD panels. Refer to FIGURE 12-2 for both 1- and 4-bit interface timing.

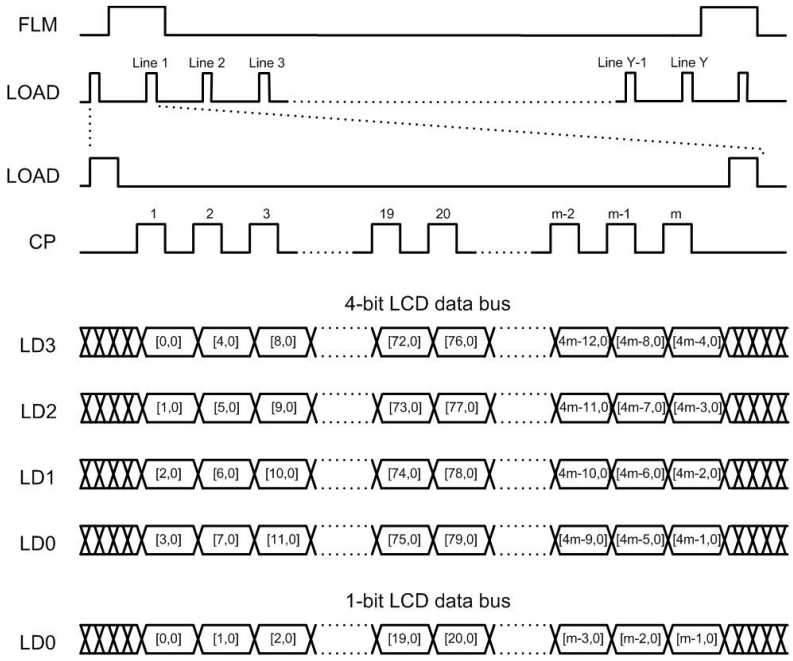


FIGURE 12-2 LCD Interface Timing for 1-/4-Bit Data

13. SERIAL PERIPHERAL INTERFACE

The ST2204B contains one serial peripheral interface (SPI) module to interface with external devices, such as Flash memory, analog-to-digital converter, and other peripherals, including another ST2204B. The SPI consists of a master- or slave-configurable interface so that connections of both master and slave devices are allowable. Five signals multiplexed with Port-C are used by SPI. With equipped $\overline{\text{DATA\_READY}}$ and $\overline{\text{SS}}$ (slave-select) control signals and transmit/receive buffers, faster data exchange with fewer software interrupts is easy to be made. Data length is widely supported from 7-bit up to 16-bit to satisfy various applications. One clock generator is provided for the synchronous communication clock SCK, which is sourced from OSCK. FIGURE 13-1 illustrates the block diagram of SPI.

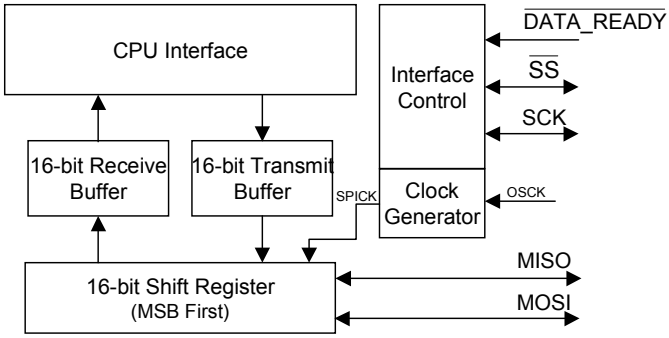


FIGURE 13-1 SPI Block Diagram

13.1 SPI Operations

The SPI contains one 16-bit shift register and two 16-bit buffers for transmission and receiving respectively. Data with variable length from 7-bit to 16-bit can be exchanged with external devices through two data lines. Data length is controlled by bit count register **BC[3:0]** (bit3~0 of SPI clock control register **SCKR)**. The current exchange will be over while the exchanged bit number reaches bit count setting.

The synchronous communication clock SCK is used to synchronize two devices and transfer data in and out of the shift register. Data is clocked by SCK with a programmable data rate, which is assigned by **SCK[2:0]** (bit6~4 of SPI clock control register **SCKR**).

The SPI block is controlled by **SPIEN** (**SCTR[7]**). Setting **SPIEN** will enable SPI function and the clock divider. Then the internal states of SPI will be reset to initial values. After that, write data to **SDATAL** will initiate an exchange. While exchanging, the busy flag will be set and is reported in **SBZ** (bit 4 of SPI status register **SSR**).

A slave select signal $\overline{\text{SS}}$ (multiplexed with PC4) is used to identify individual selection of a slave SPI device. Slave devices that are not selected do not interfere with SPI bus activities. For a master SPI device, $\overline{\text{SS}}$ can be used to indicate a multiple-master bus contention which can be reported in mode fault bit **MDERR** (bit3 of SPI status register **SSR**).

14. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

The ST2204B integrates one universal asynchronous receiver/transmitter (UART), which can be used to communicate with external serial devices. Serial data is transmitted and received at standard bit rates using the internal baud rate generator (BGR), which is controlled by BGR control register **BCTR**. FIGURE 14-1 shows the block diagram of UART.

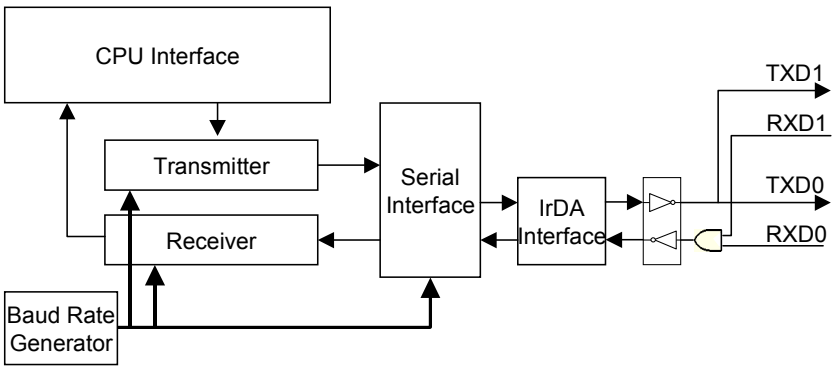


FIGURE 14-1 UART Block Diagram

14.2 UART Operations

The UART has two modes of operation, NRZ and IrDA, which represent data in different ways for serial communication protocols, RS-232 and IrDA.

14.2.1 NRZ mode

The non-return to zero (NRZ) mode is primarily associated with RS-232. Each character is transmitted as a frame delimited by a start bit at the beginning and a stop bit at the end. Data bits are transmitted least significant bit (LSB) first, and each bit occupies a period of time equal to 1 full bit. If parity is used, the parity bit is transmitted after the most significant bit. Data settings including data length, stop bit number and parity are controlled by bit fields in **UCTR**. FIGURE 14-2 illustrates a character “S” in NRZ mode.

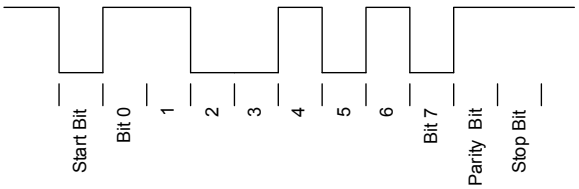


FIGURE 14-2 NRZ ASCII “S” with Odd Parity

14.2.2 IrDA mode

IrDA mode uses character frames as NRZ mode does, but, instead of driving ones and zeros for a full bit-time period, zeros are transmitted as three-sixteenth (or less) bit-time pulses (which is selected by **PW[1:0]** (**IRCTR[2:1]**), and ones remain low. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct connection can be made to external IrDA transceiver modules that use active low pulses. This is controlled by **RXINV** and **TXINV** (**IRCTR[7:6]**). IrDA mode is enabled by control bit **IREN** (**IRCTR[0]**). FIGURE 14-3 illustrates a character “S’ in IrDA mode.

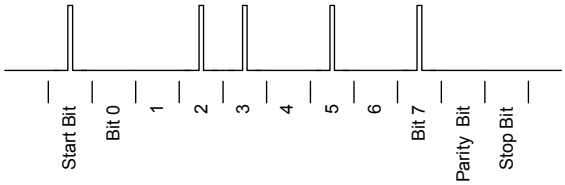


FIGURE 14-3 IrDA ASCII “S” with Odd Parity

15. DIRECT MEMORY ACCESS (DMA)

To speed up the memory access of this system, a sequential direct memory access (DMA) controller is designed-in. DMA can perform memory transfer function more efficient than CPU does. While DMA working, data ROM register (DRR) will disable and DMA use DMA memory bank register (DMR) to access ROM. After DMA complete, ROM bank control still return to DRR.
With the help of DMR can make DMS across bank boundary smoothly, but DMR is only valid for DMS. **The DMR can automatic increases when DMS across bank boundary.**

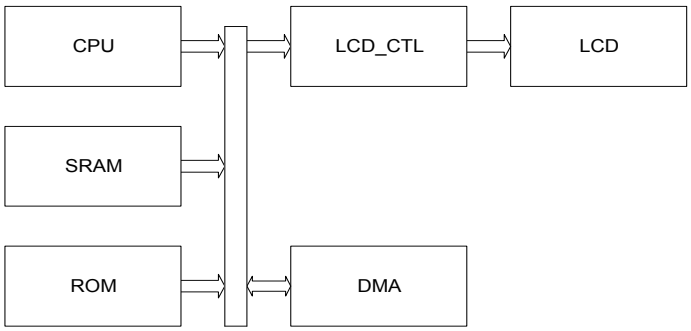


FIGURE 15-1 System Block Diagram

16. CLOCKING OUTPUTS

Three clocking outputs PE0, PE1 and PE2 are supported by the ST2204B. These signals are very useful for outputs of high frequency, such as PWM base signal or carrier of remote control. Timer0, Timer1 overflow signals are clock sources for PE0 and PE1, while BGRCK are for PE2.

■ Clocking Outputs: PE0 and PE1

Overflow states of Timers will be connected to toggle data of **PE[0:1]** when setting function selection bits **TCO0/TCO1** (**PMCR[0:1]**). Meanwhile PE0/PE1 output clocked data of half the frequency of Timers. After resetting **TCO0/TCO1**, the toggle operation ceases. Then PE0/PE1 return to the original logic level of **PE[0:1]**.

■ Clocking Output: PE2

BGRCK will output through PE2 when setting function selection bit **BCO** (**PMCR[2]**). If **BCO** is cleared, PE2 returns to the original logic level of **PE[2]**.

17. POWER DOWN MODES

ST2204B has three power down modes: WAI-0, WAI-1 and STP. The instruction WAI will enable either WAI-0 or WAI-1, which is controlled by **WAIT** (**SYS[2]**). And the instruction STP will enable **STP** mode in the same manner. WAI-0 and WAI-1 modes can be waked up by interrupt. However, **STP** mode can only be waked up by hardware reset.

17.1 WAI-0 Mode:

If **WAIT** is cleared, WAI instruction makes MCU enter WAI-0 mode. In the mean time, the oscillator, interrupts, timer/counter, and PSG are still working. On the other hand CPU and the related instruction execution stop. All registers, RAM, and I/O pins will retain the same states as those before the MCU entered power down mode. WAI-0 mode can be waked up by reset or interrupt request even If user sets interrupt disable flag **I**. In that case MCU will be waked up but not entering interrupt service routine. If interrupt disable flag is cleared (**I=**'0'), the corresponding interrupt vector will be fetched and the service routine will be executed. The sample program is shown below:

```
LDA     #$00
STA     <SYS
WAI                 ; WAI 0 mode
```

17.2 WAI-1 Mode:

If **WAIT** is set, WAI instruction makes MCU enter WAI-1 mode. In this mode, CPU stops, but the PSG, timer/counter keep running if their clock sources are from OSCX. The wake-up procedure is the same as for WAI-0. The difference is that the warm-up cycles occur when waking from WAI-1. Sample program is shown as following:

```
LDA     #$04
STA     <SYS
WAI                 ; WAI 1 mode
```

17.3 STP Mode:

STP instruction will force MCU to enter stop mode. In this mode, MCU stops, but PSG, timer/counter won't stop if the clock source is from OSCX. In power-down mode, MCU can only be waked up by hardware reset, and the warm-up cycles occur at the same time.

FIGURE 17-1 Status Under Power Down Modes

SYSCK source is OSC:

Mode	Timer0,1	SYSCK	LCD	OSC	OSCX	Base Timer	RAM	REG.	I/O	Wake-up condition
WAI-0	Retain									Reset, Any interrupt
WAI-1	Stop	Stop	Stop	Stop	Retain					Reset, Any interrupt
STP	Stop	Stop	Stop	Stop	Retain					Reset

SYSCK source is OSCX:

Mode	Timer0,1	SYSCK	OSC	OSCX	Base Timer	RAM	REG.	I/O	LCD	Wake-up condition
WAI-0	Retain								Wrong Frame	Reset, Any interrupt
WAI-1	Stop	Stop	Retain						Stop	Reset, Any interrupt
STP	Stop	Stop	Retain						Stop	Reset

18. WATCHDOG TIMER

The watchdog timer (WDT) is an added check that a program is running and sequencing properly. When the application software is running, it is responsible for keeping the 2- or 8-second watchdog timer from timing out. If the watchdog timer times out, it is an indication that the software is no longer being executed in the intended sequence. At this time the watchdog timer generates a reset signal to the system.

18.1 WDT Operations

The WDT is enabled by setting the WDT enable flag **WDTEN** (**MISC[3]**). Two time settings, 2 and 8 seconds, are selectable with selection bit **WDTPS** (**MISC[2]**).WDT is clocked by the 2Hz clock from the base timer and therefore has 0.5-second resolution. It is recommended that the watchdog timer be periodically cleared by software once it is enabled. Otherwise, software reset will be generated when the timer reached a binary value of 4 or 16.

Note:The WDT can be reset by writing any value to **MISC** register.

After a system reset, **WDTEN** is cleared. Then the WDT returns to be idle.

19. LOW VOLTAGE DETECTOR

ST2204B has a built-in low voltage detector for power management. Two voltage signals can be selected by the control bit **LVDS** (**MISC[4]**). First is the power applied to ST2204B and the typical detection level is 2.6V. Second is the signal applied to input pin VIN, and the typical detection level is 1.25V. When **LVDEN** (**SYS[0]**) is set, LVD is enabled and the detection result will be outputted at the same bit after 3 μs. Using read instruction twice can get this result: first read will enable initial stableness control. Second read equal '0' represents 'low voltage'. Once LVD is enabled, it keeps on consuming power. So it is important to write “0” to **LVDEN** and disable the detector after detection is completed. FIGURE 19-1 shows an application circuit for detecting low battery voltage of 2.5V. Note that the DC current of two external resistors can be cut off by setting PC0 to open. Also add one capacitor to VIN to minimize noise and narrow the low voltage detection range.

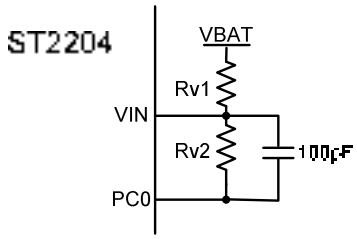


FIGURE 19-1 Application of LVD

The detection voltage for FIGURE 19-1 is:

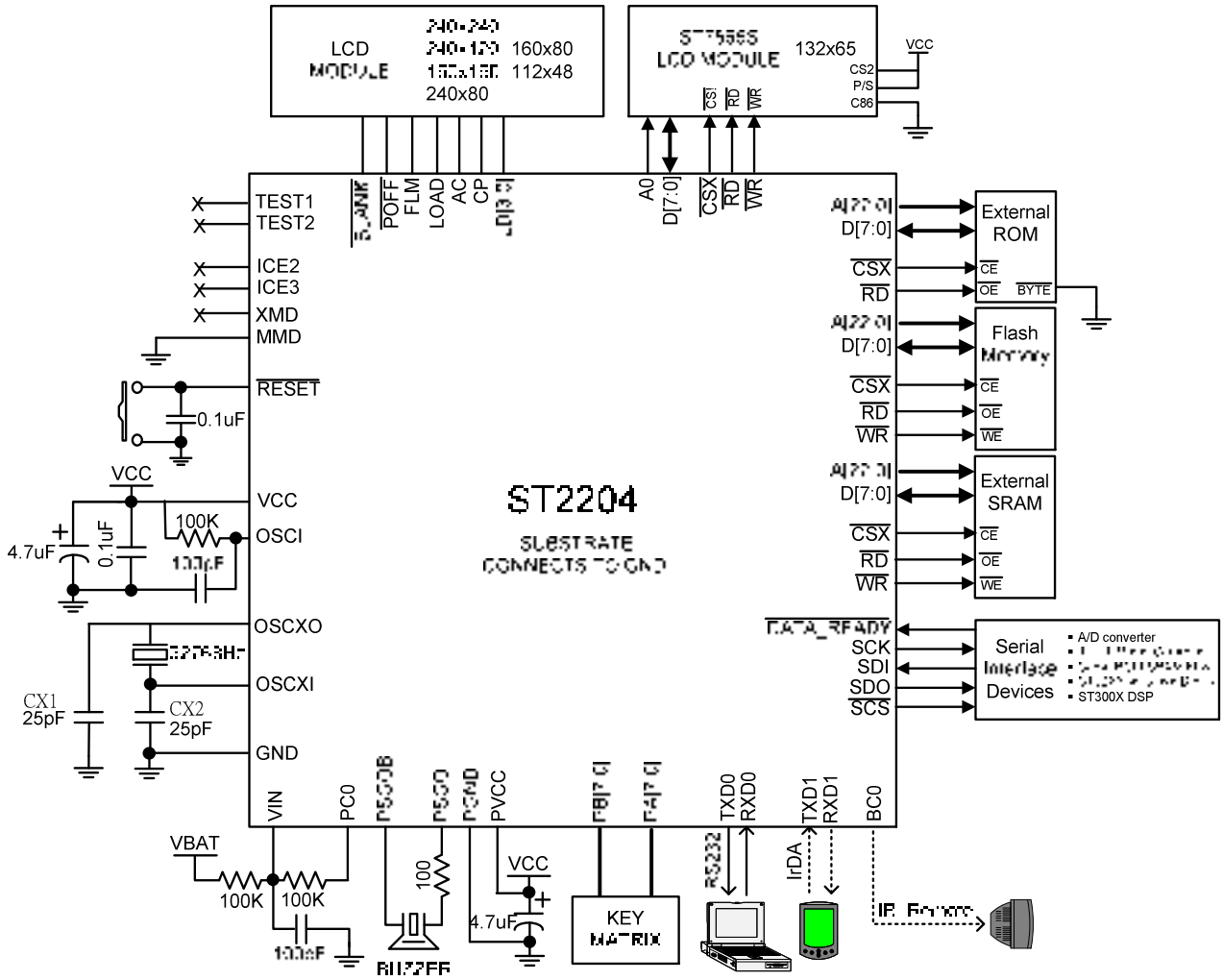
$$Detection\ Voltage = \frac{Rv1 + Rv2}{Rv2} * 1.25 \qquad \text{Equation22-1}$$

If Rv1=Rv2=100kΩ
Then the detection voltage is 2.5V

20. LOW VOLTAGE RESET (LVR)

Power bouncing during power on is a major problem when designing a reliable system. The ST2204B equips Low Voltage Reset function to keep whole system in reset status when power is not stable. Once low voltage status is detected, the system will reset automatically. After the power backs to normal, the system may recover its original states and keeps working correctly. The LVR circuit always works and it consumes very few current.

21. APPLICATION CIRCUITS



Note: 1. Keep the trace between oscillation resistor and the PCB pad as close as possible for a more stable clock.
2. The OSCX can still work if remove CX1 and increase CX2 to 47pF.

22. ELECTRICAL CHARACTERISTICS

22.1 Absolute Maximum Rations

DC Supply Voltage ---------- -0.3V to +4.5V
Operating Ambient Temperature ---------- -10°C to +60°C
Storage Temperature ---------- -55°C to +125°C

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

22.2 DC Electrical Characteristics

Standard operation conditions: VCC = 3.0V, GND = 0V, T_A = 25°C, OSC = 4M Hz, unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	VCC	2.4		3.6	V	
Operating Frequency	F_1			6.0	MHz	VCC = 2.4V ~ 3.6V
Operating Frequency	F_2			8.0	MHz	VCC = 3.3 ~ 3.6V
Operating Current	I_{OP}		3.0	4.0	mA	All I/O port are input and pull-up, execute NOP instruction, LCDC on
Standby Current	I_{SB0}		450	675	μA	All I/O port are input and pull-up, OSCX on, LCDC on (WAIT0 mode)
Standby Current	I_{SB1}		7	10.5	μA	All I/O port are input and pull-up, OSCX on, heavy load, LCDC off (WAIT1 mode)
Standby Current	I_{SB2}		3.5	5.3	μA	All I/O port are input and pull-up, OSCX on, normal load, LCDC off (WAIT1 mode)
Standby Current	I_{SB3}		1	1.5	μA	All I/O port are input and pull-up, OSCX off, LCDC off (WAIT1 mode)
Input High Voltage	V_{IH}	0.7Vcc 0.85Vcc		Vcc+0.3	V V	Port-A/B/C/D/E/L $\overline{\text{RESET}}$
Input Low Voltage	V_{IL}	GND-0.3		0.3Vcc 0.15Vccc	V V	Port-A/B/C/D/E/L $\overline{\text{RESET}}$
Pull-up resistance	R_{IH}		180		KΩ	Port-A/B/C/D/E/L (input Voltage=0.7VCC)
Output high voltage	V_{OH1}	0.7Vcc			V	Port-A/B/C/D/L (I_{OH} =-4mA)
Output low voltage	V_{OL1}			0.3Vcc	V	Port-A/B/C/D/E/L (I_{OL} =6mA)
Output high voltage	V_{OH2}	0.7Vcc			V	PSG/DAC, I_{OH} = -37mA.
Output low voltage	V_{OL2}			0.3Vcc	V	PSG/DAC, I_{OL} = 74mA.
Low Voltage Detect level (internal mode)	V_{LVD1}	2.4		2.8	V	
Low Voltage Detect level (external mode)	V_{LVD2}	1.2		1.4	V	
Low Voltage Reset level	V_{LVR}	2.0		2.2	V	
Low Voltage Reset current	I_{LVR}		1	1.5	μA	Total LVR circuit current consumption

22.3 AC Electrical Characteristics

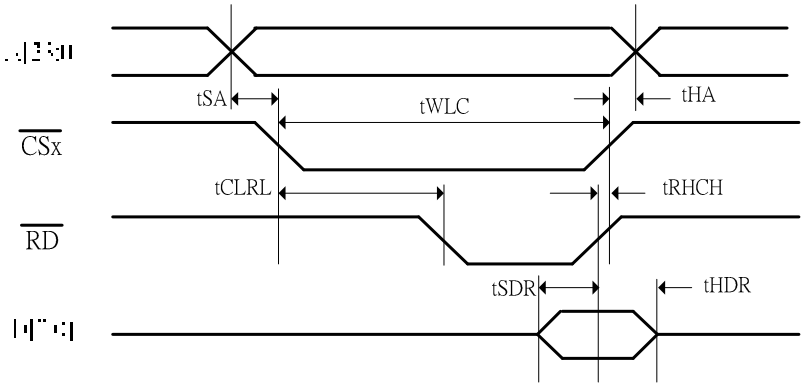


FIGURE 22-1 External Read Timing Diagram

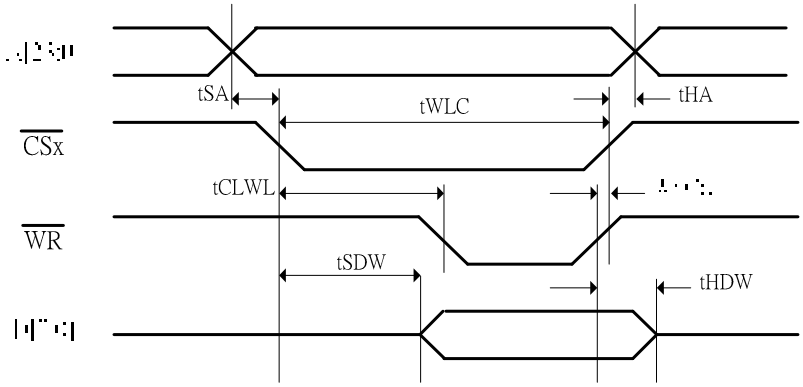


FIGURE 22-2 External Write Timing Diagram

TABLE 22-1 Timing parameters for FIGURE 22-1 and FIGURE 22-2

Standard operation conditions: VCC = 3.0V, GND = 0V, T_A = 25°C

Symbol	Characteristic	Rating			Unit
		Min.	Typ.	Max.	
tSA	Address setup time	—	—	10	ns
tHA	Address hold time	0	—	—	ns
tWLC	CS "L" pulse width	166	—	—	ns
tCLWL	CS asserted to $\overline{WR}$ asserted	—	1/2 tWLC	—	ns
tWHCH	CS negated after $\overline{WR}$ is negated	10	—	—	ns
tSDW	CS asserted to data-out is valid	—	1/2 tWLC	—	ns
tHDW	Data-out hold time after $\overline{WR}$ is negated	20	—		ns
tCLRL	CS asserted to $\overline{RD}$ asserted	—	1/2 tWLC	—	ns
tRHCH	CS negated after $\overline{RD}$ is negated	10	—	—	ns
tSDR	Data-in valid before $\overline{RD}$ is negated	30	—	—	ns
tHDR	Data-in hold time after $\overline{RD}$ is negated	10	—	—	ns
tR	Signal rise time	—	20	—	ns
tF	Signal fall time	—	10	—	ns

22.4 Characteristic Charts

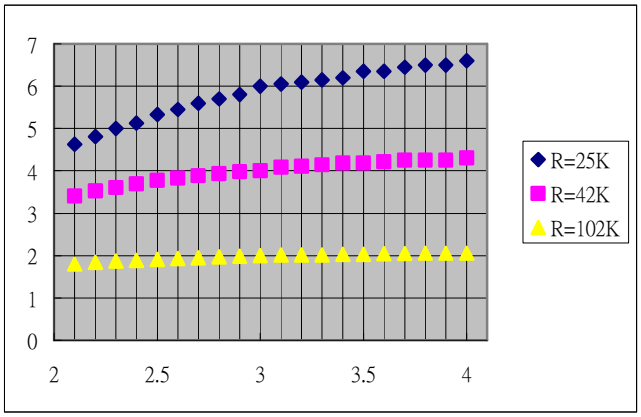


FIGURE 22-3 Frequency of R-OSC as a function of VCC

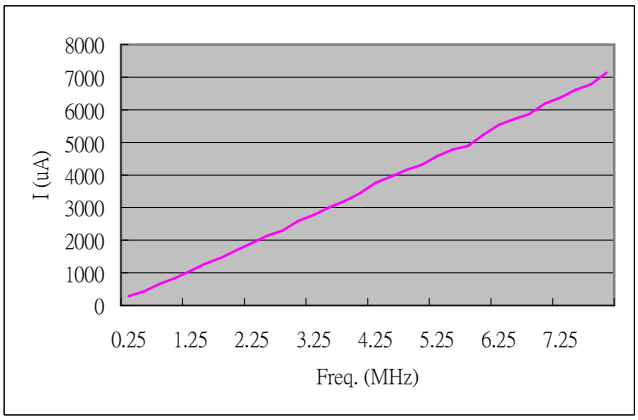


FIGURE 22-5 Operation Current as a function of OSCK

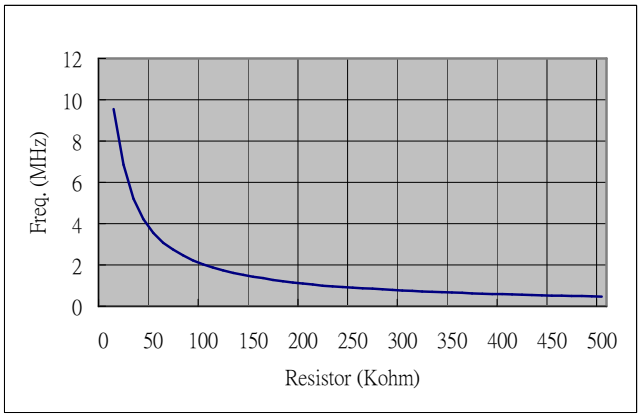


FIGURE 22-4 Frequency of R-OSC as a function of Resistor under VCC=3v

23. REVISIONS

REVISION	DESCRIPTION	PAGE	DATE
1.1	■ Modify section 5 “DEVICE INFORMATION”	**6**	2005/01/18
	■ Add section 22.1 “Absolute Maximum Rations”	**22**	
	■ Add section 22.2 “DC Electrical Characteristics”	**22**	
	■ Add section 22.3 “AC Electrical Characteristics”	**23**	
	■ Add section 22.4 “Characteristic Charts”	**24**	
1.0	First release		2004/9/16