



# ST20P16

## 16K 8-bit Single Chip Microcontroller

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### 1. FEATURES

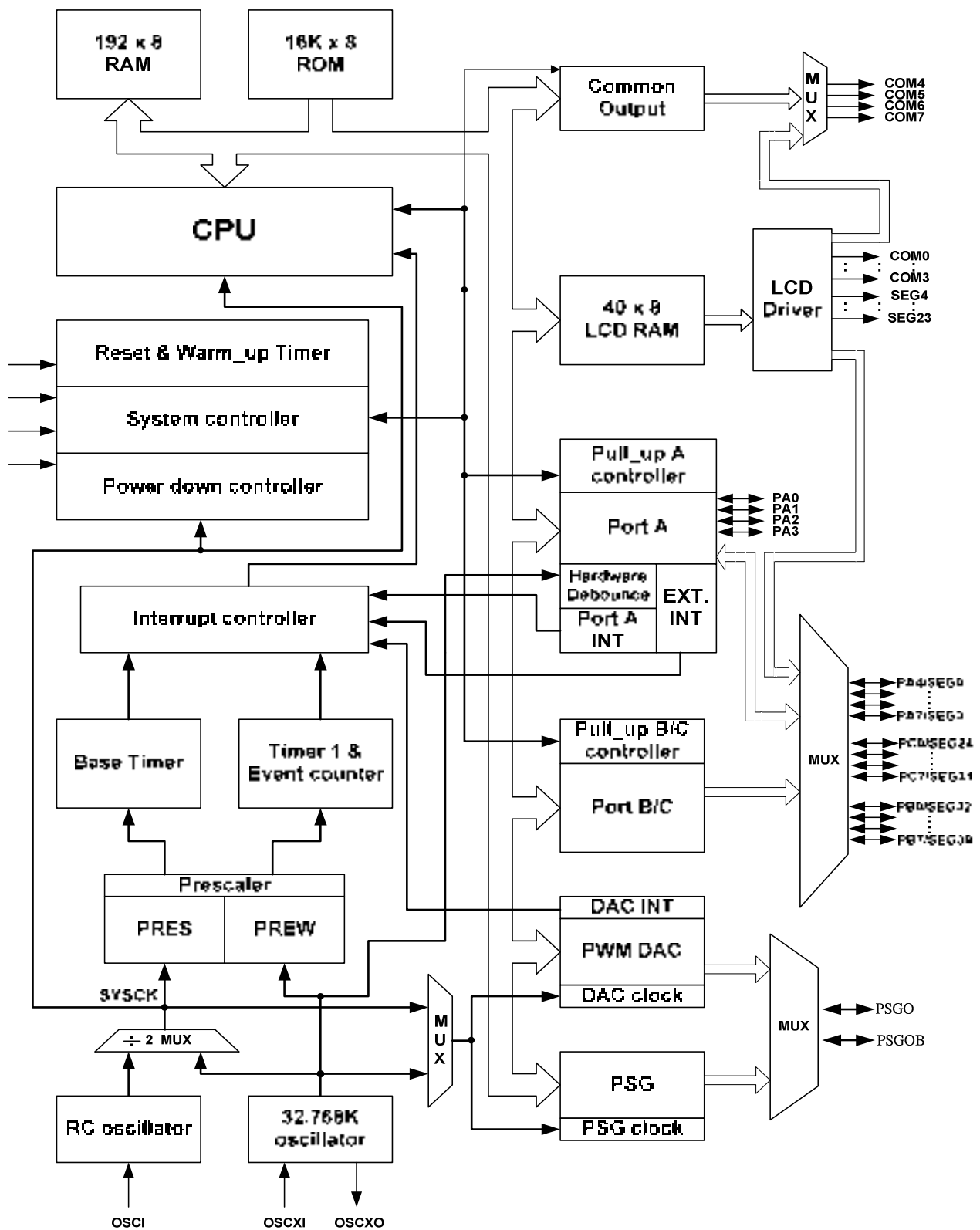
- 8-bit static pipeline CPU
- ROM: 16K x 8 bits
- RAM: 192 x 8 bits
- Operation voltage : 2.4V ~3.6V
- 24 CMOS Bi-directional bit programmable I/O pins
  - Twenty (Port-A high nibble & Port-B/C) are shared with LCD drives
- 6 Output pins (Four are shared with LCD common and two are shared with PSG)
- 2 Input pins (code option: Shared with OSCX)
- Hardware debounce option for input port
- Bit programmable PULL-UP for input port
- Timer/Counter :
  - One 8-bit timer / 16-bit event counter
  - One 8-bit BASE timer
- Five powerful interrupt sources :
  - External interrupt (edge trigger)
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
  - DAC reload interrupt
- 32-level deep stack
- Dual clock source :
  - OSCX: Crystal oscillator: 32768Hz
  - OSC: RC oscillator 500K ~ 4M Hz
  - CPU clock 250k ~ 2M Hz
- Build-in oscillator with warm-up timer
- LCD controller driver:
  - 16 level contrast control
  - 320 ( 8x40) dots ( 1/8 duty, 1/4 bias, programmable)
  - 160 ( 4x40) dots ( 1/4 duty, 1/3 bias, programmable)
  - Two clock source options: RC and resonator oscillator
  - Keyboard scan function supported on 20 shared segment drives
  - Internal bias resistors(1/4 bias & 1/3 bias) with 32 level driving strength control
- Programmable Sound Generator (PSG) includes :
  - Tone generator
  - Sound effect generator
  - 16 level volume control
  - Digital DAC for speech / tone
- Three power down modes :
  - WAI0 mode
  - WAI1 mode
  - STP mode

### 2. GENERAL DESCRIPTION

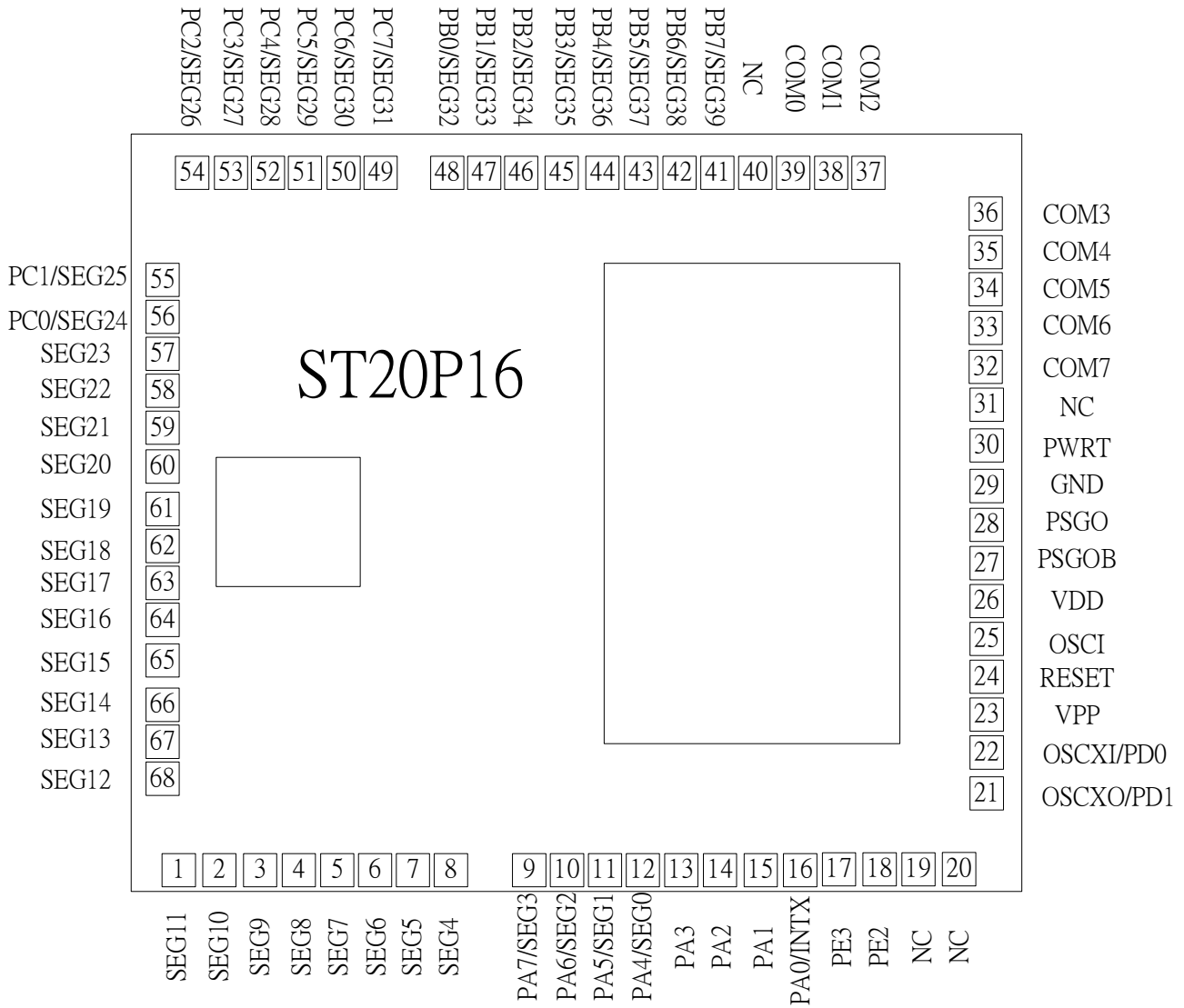
ST20P16 is a low-cost, high-performance, fully static, 8-bit microcontroller designed with CMOS silicon gate technology. It comes with 8-bit pipeline CPU core, SRAM, timer, LCD driver, I/O port, PSG and mask program ROM. A build-in dual oscillator

is specially integrated to enhance chip performance. For business equipment and consumer applications. Such as watch, calculator, and LCD game , ST20P16 is definitely a perfect solution for implementation.

### 3. BLOCK DIAGRAM



### 4. PAD DIAGRAM



## 5. PAD DESCRIPTION

Pin No.	Designation	Type	Description
12~9	SEG0/PA4 ~ SEG3/PA7	O I/O	LCD Segment output Port-A bit programmable I/O
8 ~ 1 68 ~ 57	SEG4 ~ SEG23	O	LCD Segment output
56~49	SEG24/PC0 ~ SEG31/PC7	O I/O	LCD Segment output Port-C bit programmable I/O
48~41	SEG32/PB0 ~ SEG39/PB7	O I/O	LCD Segment output Port-B bit programmable I/O
39~36	COM 0 - 3	O	LCD Common output
35~32	COM 4 - 7	O O	LCD Common output Output port
24	RESET	I	Pad reset input (HIGH Active)
29	GND	P	Ground Input and chip substrate
16	PA0/INTX	I/O I I I	Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source
15~9	PA 1-7	I/O I	Port-A bit programmable I/O Transition-trigger Interrupt
28~27	PSGO,PSGOB	O	PSG/DAC Output
26	VDD	P	Power supply
22	OSCXI/PD0	I I	OSC input pin. For 32768Hz crystal Port-D input
21	OSCXO/PD1	O I	OSC output pin. For 32768Hz crystal Port-D input
25	OSCI	I	OSC input pin. Toward to external resistor
17~18	PE2~PE3	P	OTP programming power
19,20,31,40	NC	-	-
23	VPP	P	OTP programming power
30	PWRT	I	Power on timer control pin. Suggest tie to GND to disable

Legend: I = input, O = output, I/O = input/output, P = power.

## 6. Application Circuits

### 6.1 APPLICATION CIRCUIT UNDER 3V OPERATING VOLTAGE

VDD : 3V  
 Clock : 32768Hz crystal and 4.0MHz RC oscillator  
 LCD : 1/8 duty  
 I/O : PORT A  
 ALARM : PSGO, PSGOB

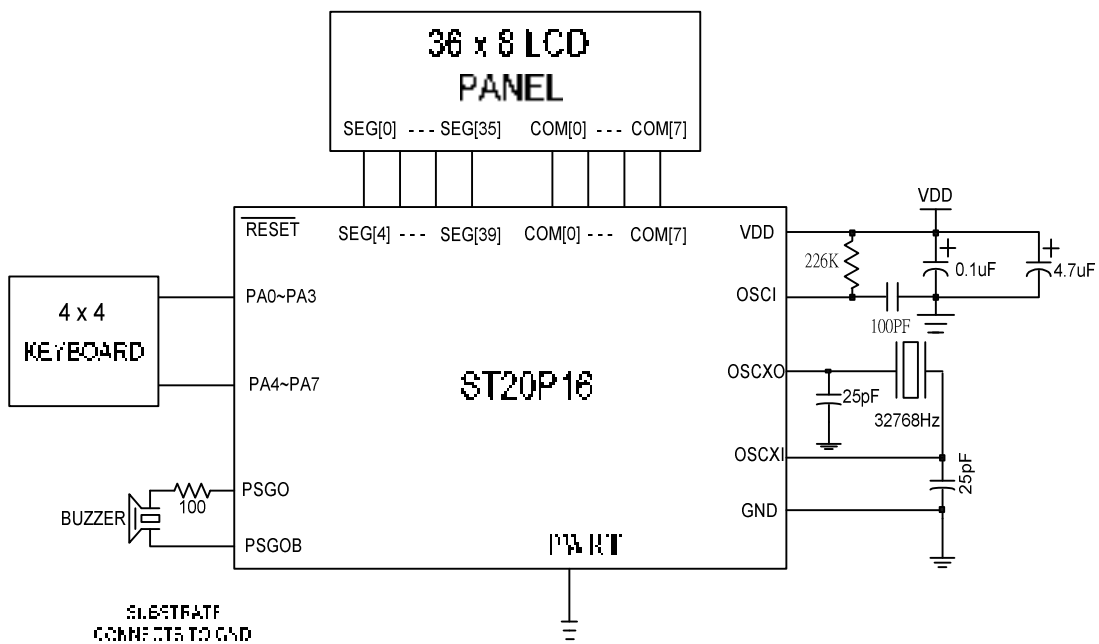


FIGURE 6-1: APPLICATION CIRCUIT WITHOUT LCD KEYBOARD AWAKING PULSE

Note: The functions of PWRT have been added in the ST20P18. When ST20P18 is used as ST20P16, please connect to GND.

VDD : 3V  
 Clock : 32768Hz crystal and 4.0MHz RC oscillator  
 LCD : 1/8 duty  
 I/O : PORT A  
 ALARM : PSG0, PSG1

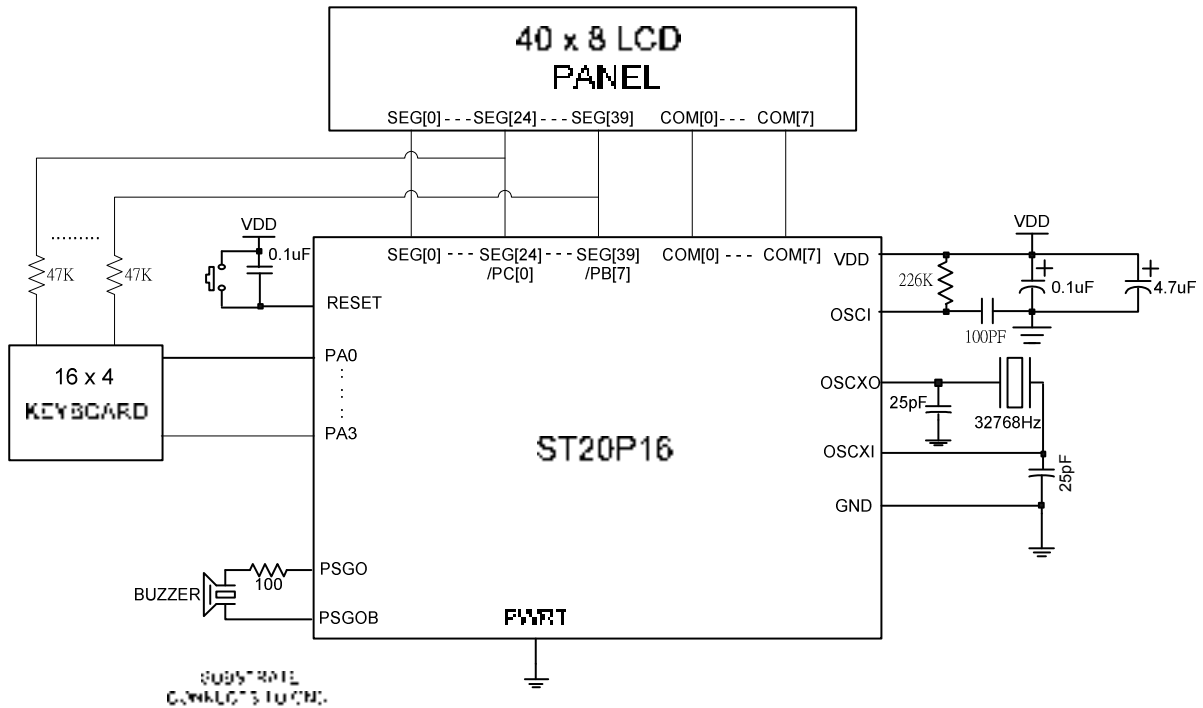


FIGURE 6-2: APPLICATION CIRCUIT WITH LCD KEYBOARD AWAKING PULSE

**Note:**

1. COMs and SEGs output GND level, while the LCD is turned off.
2. If LCD is turned off, Keyboard Awaking Pulses must be turned off at the same time.
3. Connect one capacitor of 100PF to OSCI stabilize oscillation frequency. This capacitor must be placed close to OSCI.
4. The functions of PWRT have been added in the ST20P18. When ST20P18 is used as ST20P16, please connect to GND.

## 7. OTP ROM Programming Interface

### 7.1 Interface Description

In order to program OTP ROM, several pins have to be reserved on the PCB which is bounding with ST20P18. These total are 8 pins that include following list TABLE 7-1: . It just be used to connect

writer to program OTP ROM. After programming and disconnecting from writer, they can be used as original purpose.

**TABLE 7-1: Pin assignment of interface**

ST20P16 Pad Name	(SPI Interface)	Pin Type	Description
VPP	VPP	Power	High Voltage Power Supply 1) OTP Program, Program Verify, VPP=> 12V 2) OTP Read:VPP=> Floating
GND	VSS	Power	Ground.
VCC	VDD	Power	Low Voltage (2.4V-5.4V) Power Supply.
PE3	SSB	Input	SPI signal
SEG4	MOSI	Input	SPI signal
SEG5	MISO	Output	SPI signal
PE2	SCK	Input	SPI signal
RESET	RESET	Input	SPI RESET

### 7.2 Programming Function Specification

There are reserved 5 option bits to select to apply or not the function we needed. It includes PD input and Code Protection.

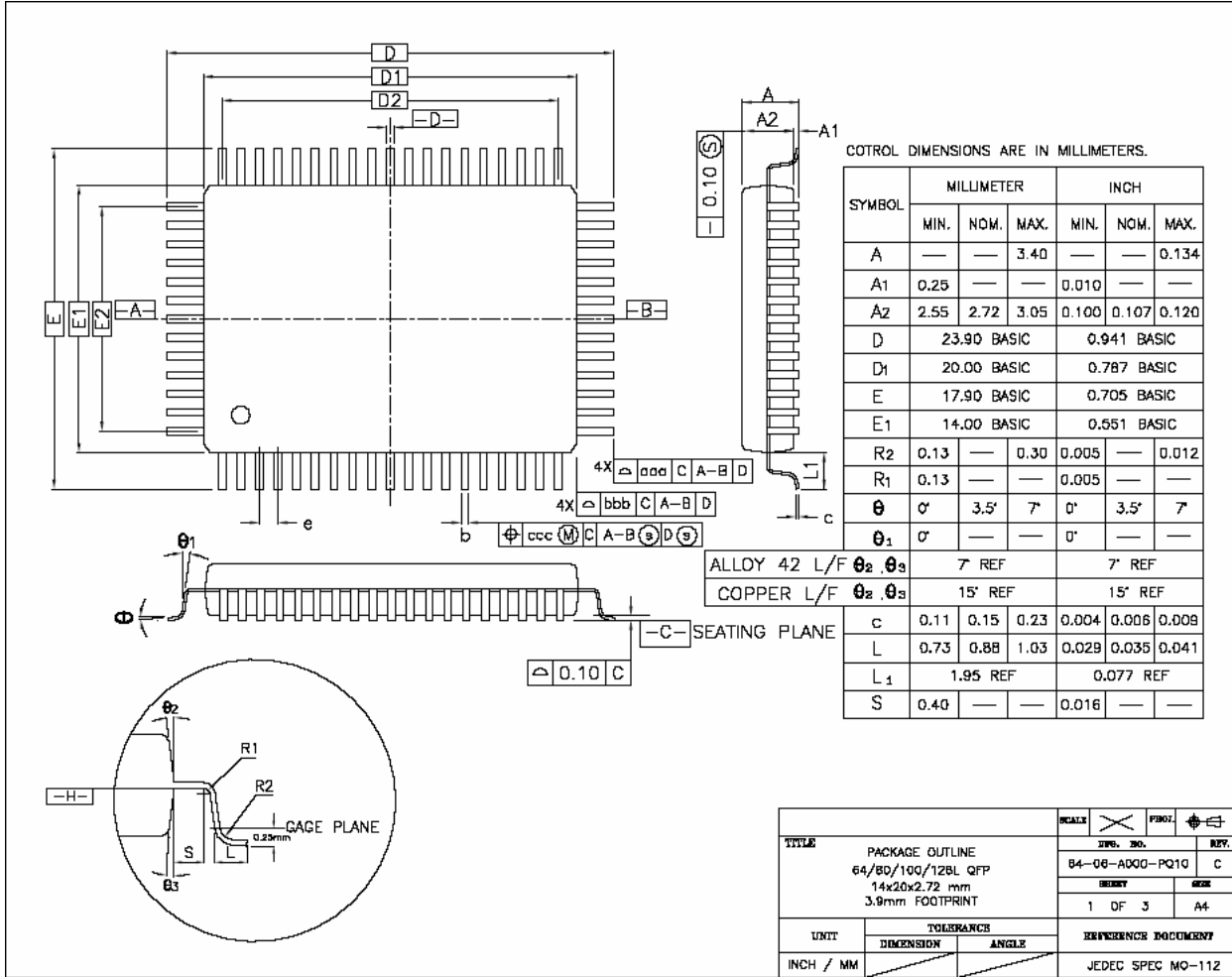
To setup the options should program the OTP ROM by OTP writer .

**TABLE 7-2: Option ward**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
CP	-	-	-	WDTSTP	WDTEN	-	PD	1--- 00-1
<p>Bit 7: <b>CP</b>: OTP ROM code protect. 0 =protect OTP data. 1 =Un-Protect OTP data.</p> <p>Bit 3: <b>WDTSTP</b>: WDT stop control bit. 0 = WDT stop at WAI-1 and STP mode.</p> <p>Bit 2: <b>WDTEN</b>: WDT enable. 0 = WDT disable.</p> <p>Bit 0: <b>PD</b>: Port function selection 0 = PD used as input port. 1 = OSC input pin for 32768Hz crystal.</p>								

Note :Watchdog timer (WDT) circuit has been added in the ST20P18. When ST20P18 is used as ST20P16, the option bits of WDTEN and WDTSTP have to be programmed to "0".(OTP firmware option select )

# 8. PACKAGE INFORMATION

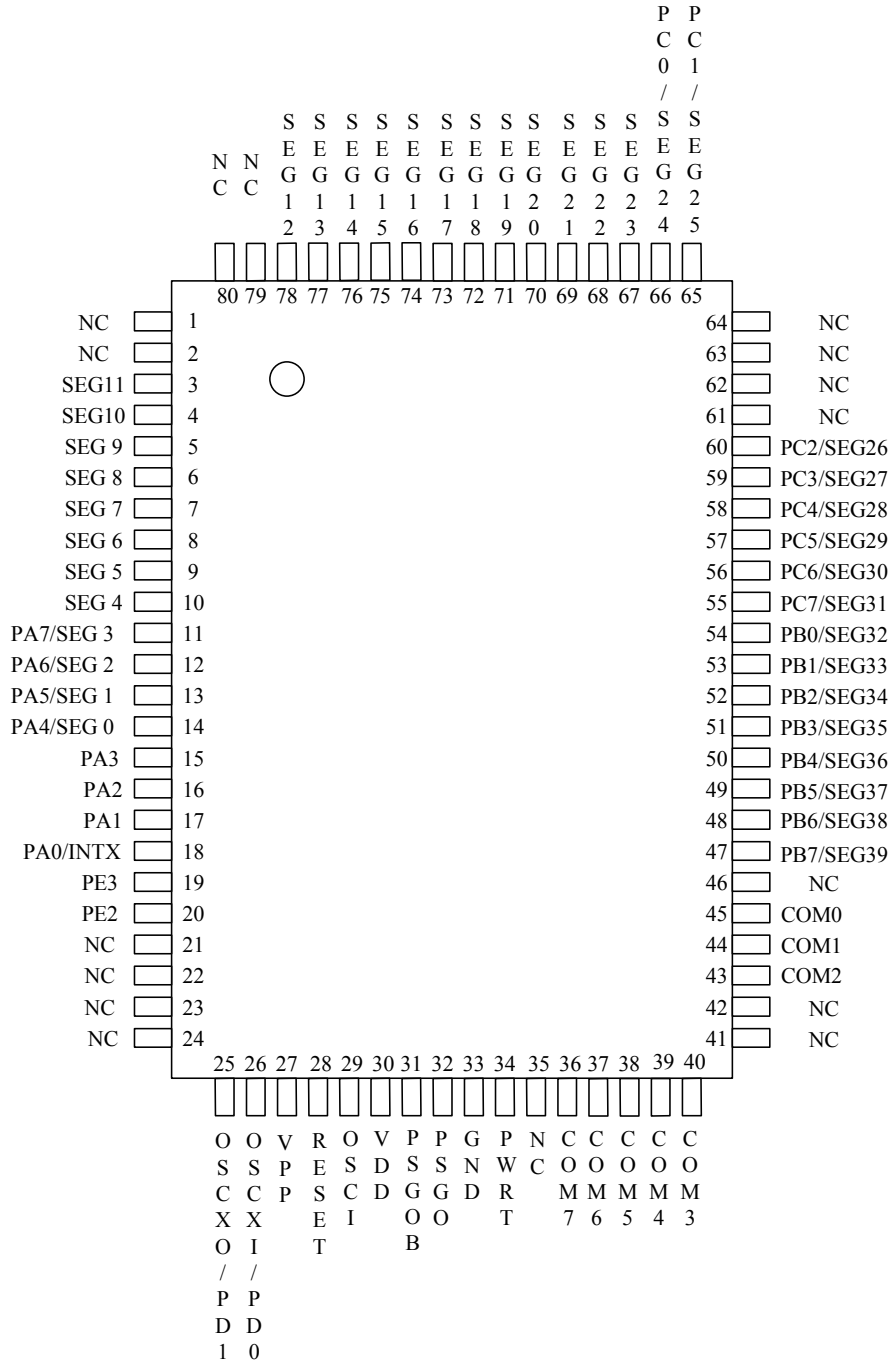


## Dimensions in Millimeters

SYMBOL	80L MILLIMETER		
	MIN.	NOM.	MAX.
b	0.30	0.35	0.45
e	0.80 BSC.		
D2	18.4 REF		
E2	12.0 REF		
TOLERANCE OF FORM AND POSITION			
aaa	0.25		
bbb	0.20		
ccc	0.20		



# 9. PIN CONFIGURATION(QFP80)



## Revisions

Version	Page	Description	Date
1.3	7,8	Modify Rosc 180k ohm to 226k ohm under 4Mhz condition.....	2006/3/1
1.4	1	Add CPU clock 250k ~ 2M Hz.....	2006/6/23
1.5	8,9	Move package information to page8,9.....	2006/8/8

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