ST1624

Capacitive Touch Screen Controller

Datasheet

Version 1.1

2014/10/22

Note: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

Sitronix Technology Corporation

1 INTRODUCTION

The ST1624 is a mutual capacitive sensing controller for small size projected capacitive touch screen. It is a RISC microcontroller with capacitor charge, capacitor sensing, slave I2C interface, general purpose I/O and embedded non-volatile memory.
Internal program and cooperating digital circuit convert finger / capacitor stylus physical touching into button pressing message or multiple coordination information for application. The maximum fingers identification ability is up to five.
The ST1624 uses low profile QFN package and support ITO electrode on glass or film substrate. Hence, slim and small touch panel module is realizable.
And more, low electromagnetic interference of ST1624 makes it suitable for modern touch screen application which contain a vivid and high density display, like smart phone, portable navigation device and touch-enabled media player, etc..

FEATURES

- **MCU based touch controller**
- **Operation voltage**
  - VDD = 2.7V ~ 3.6V
  - IOVDD = 1.6V ~ 3.6V
- **Operation Temperature: -20℃ ~ 80℃**
- **Storage Temperature: -40℃ ~ 125℃**
- **Interface**
  - I2C (slave)
- **Sensor:**
  - 15 TX, 9 RX
- **Single finger handwriting**
- **five fingers detection and tracking**
- **Capacitive Sensor**
  - Mutual-capacitance sensing
  - Max. loading: 30 kOhm/60pF
  - Report Rate : 100Hz
  - Hardware noise reduction
  - Waterproof circuit
- **Package**
  - QFN32

APPLICATIONS

- **Cell phones**
- **PDAs**
- **Portable instruments**
- **Touch screen monitors**
- **Electrical papers**
- **Gaming machines**
- **Pointing devices**
- **PC peripherals**

2 PACKAGE INFORMATION

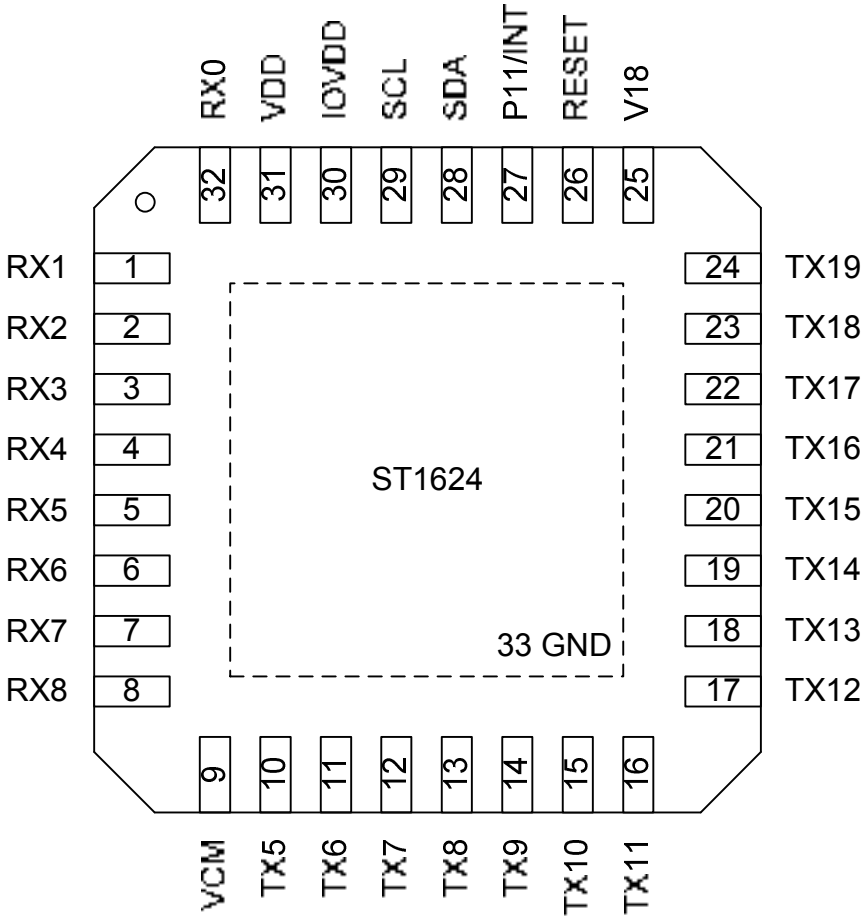


Figure 2-1 ST1624 Package Pin Configuration

Table 2-1 ST1624 Package Signal Descriptions

Pin #	Pin Name	I/O	Description
8~1	RX8~RX1	I	Receiver channel
9	VCM	P	Common mode voltage, connect to 1uF capacitor
24~10	TX19~TX5	O	Transmitter channel
25	V18	P	Digital power, connect to 1uF capacitor
26	RESET	I	System reset signal input, active low
27	INT/P11	I/O	INT : Indicate coordinate data ready P11 : General purpose I/O
28	SDA	I/O	I2C serial data
29	SCL	I/O	I2C serial clock
30	IOVDD	P	I/O power supply, connect to 1uF capacitor
31	VDD	P	Power supply, connect to 1uF capacitor
32	RX0	I	Receiver channel
33	GND	P	Ground

Note: I/O type: P=Power pin, I=Input pin, O=Output pin

3 SYSTEM MANAGEMENT

3.1 Power Down

In power down mode, all of the clocks of ST1624 are stopped. The way to exit power down mode is by a hardware reset or I2C.

3.2 Reset

Master can reset ST1624 through $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ pin is low active and needs hold low for 1us to take effect.

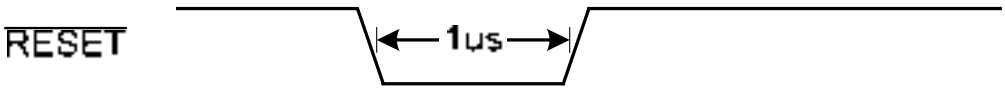


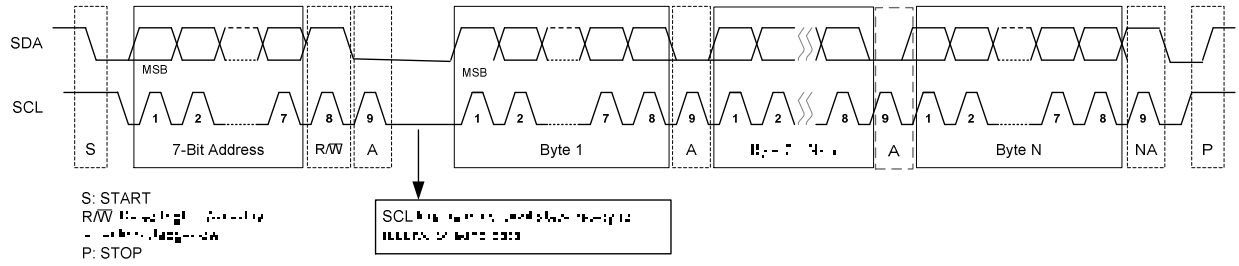
Figure 3-1 $\overline{\text{RESET}}$ Pin Low Pulse Width

4 DIGITAL INTERFACE

4.1 I2C Slave Interface

ST1624 equipped with I2C provides two wires, serial data (SDA) and serial clock (SCL), to carry transferring information at up to 400 kbit/s(Fast mode). ST1624 plays the slave role in I2C transfer. Both SDA and SCL are bidirectional lines, connected to IOVDD via pull-up resistors. All transactions begin with a START (S) and can be terminated by a STOP (P). 7-bits address follows START to recognize device. Each bye is 8-bits length and followed by an acknowledge bit. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Read



Write

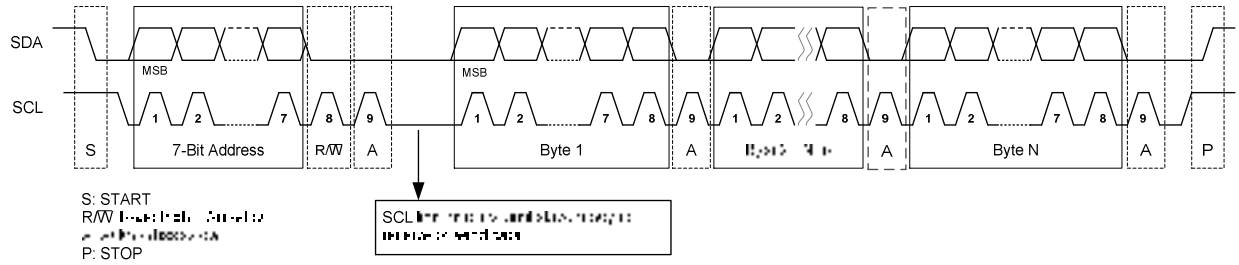


Figure 4-1 I2C Waveform

5 ELECTRICAL CHARACTERISTIC

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
VDD	V_{VDD}	-0.3	+6	V
IOVDD	V_{IOVDD}	-0.3	+6	V
Operating Ambient Temperature	T_A	-20	+80	℃
Storage Temperature	T_S	-40	+125	℃

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 DC Electrical Characteristics

Table 5-2 System DC Electrical Characteristics

Condition: VDD = IOVDD = 3.3V, T_A = 25°C, unless be specified individually.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD	V_{VDD}	2.7	-	3.6	V	
IOVDD	V_{IOVDD}	1.6	-	3.6	V	
Operating Current	I_{NML}	-	16	24	mA	15TX, 9RX
Idle Current	I_{IDLE}	-	5.9	8.9	mA	15TX, 9RX, scan rate=20Hz
Power Down Current	I_{PD}	-	-	20	uA	
Input High Voltage	V_{IH}	0.85*IOVDD	-	-	V	IOVDD=3.3V
Input Low Voltage	V_{IL}	-	-	0.15*IOVDD	V	IOVDD=3.3V
Input Pull Up Resistor	R_{PU}	50	-	60	KOhm	
Output Driving Current	I_{DRV}	30	-	-	mA	V_{OH} = IOVDD x 0.8
Output Sinking Current	I_{SINK}	80	-	-	mA	V_{OL} = IOVDD x 0.2
Low Voltage Reset	V_{LVR}	-	-	2.3	V	

5.3 AC Electrical Characteristics

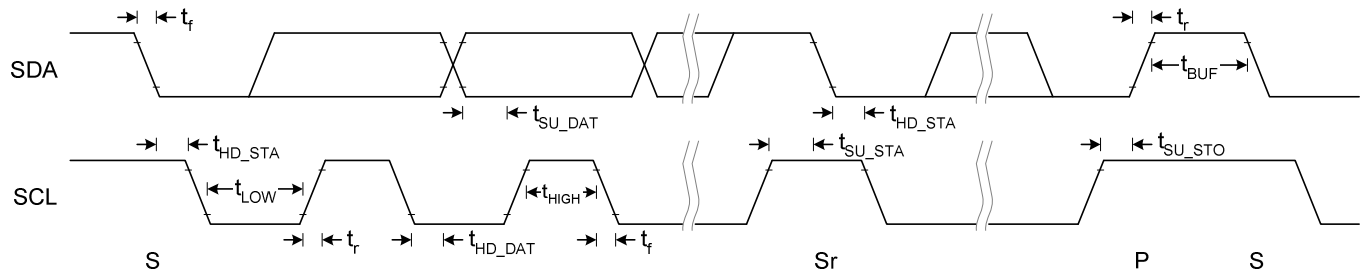


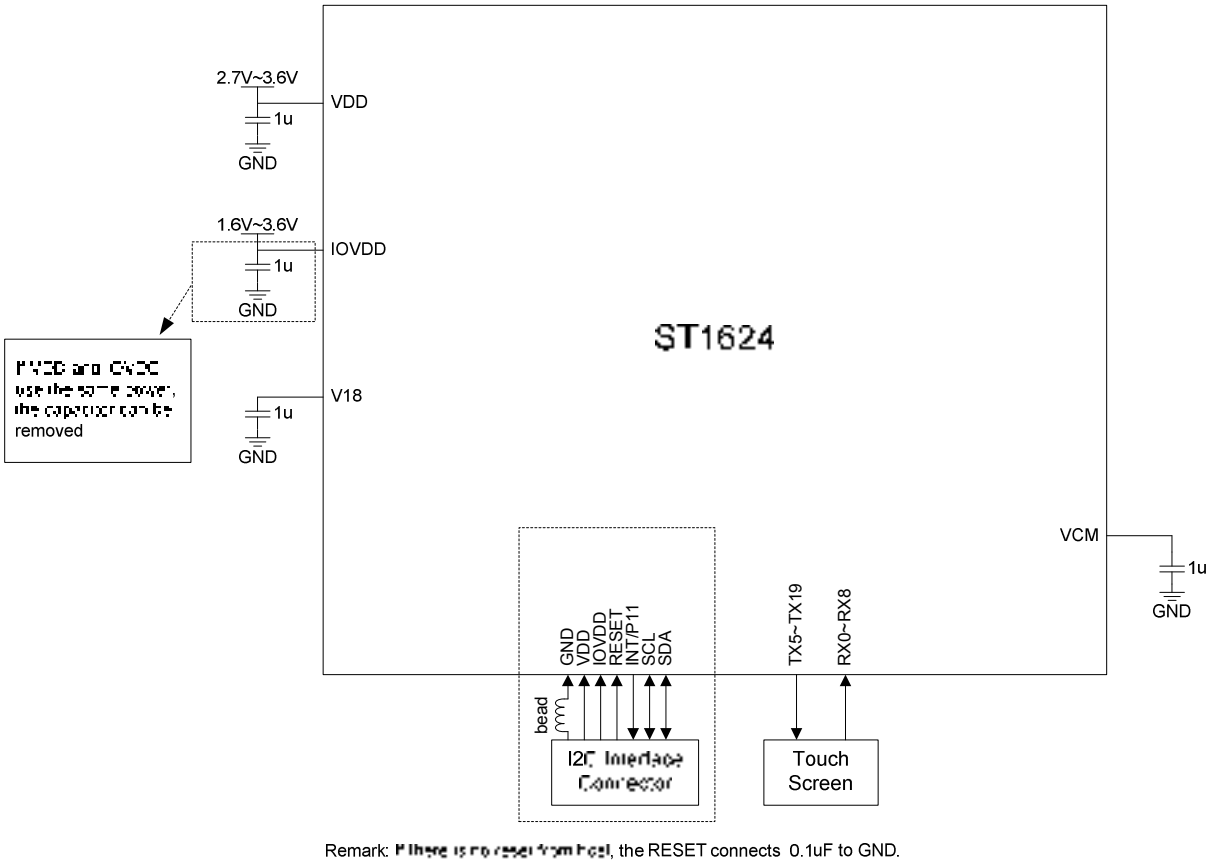
Figure 5-1 I2C Fast Mode Timing

Table 5-3 I2C Fast Mode Timing Characteristic

Conditions: VDD = 3.3V, GND = 0V, T_A = 25°C

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
f_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Low period of the SCL clock	1.3	-	-	us
t_{HIGH}	High period of the SCL clock	0.6	-	-	us
t_f	Signal falling time	-	-	300	ns
t_r	Signal rising time	-	-	300	ns
t_{SU_STA}	Set up time for a repeated START condition	0.6	-	-	us
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	us
t_{SU_DAT}	Data set up time	100	-	-	ns
t_{HD_DAT}	Data hold time	0	-	0.9	us
t_{SU_STO}	Set up time for STOP condition	0.6	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
C_b	Capacitive load for each bus line	-	-	400	pF

6 APPLICATION CIRCUITS



Remark: If there is no reset from host, the RESET connects 0.1uF to GND.

Figure 6-1 ST1624 Application Circuit

7 SCHEMATIC EXAMPLE

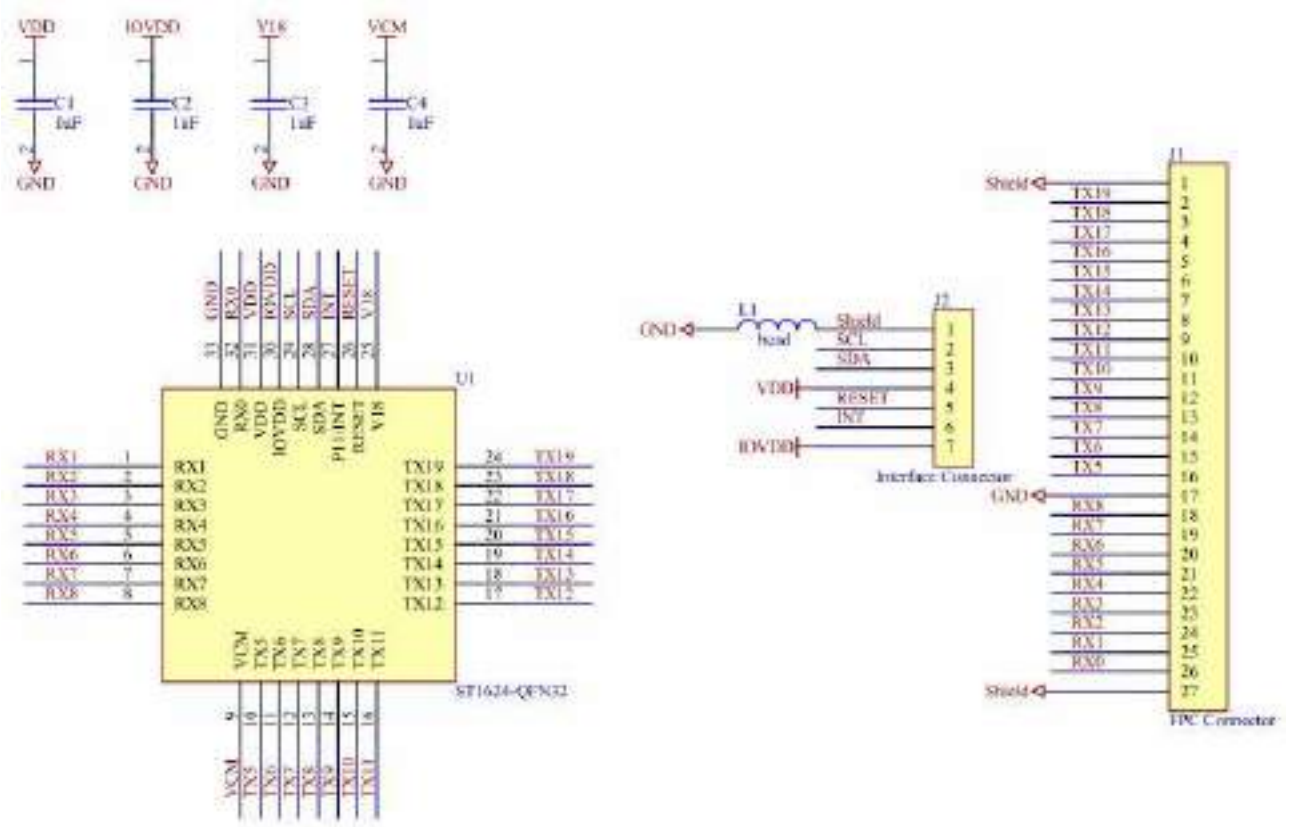
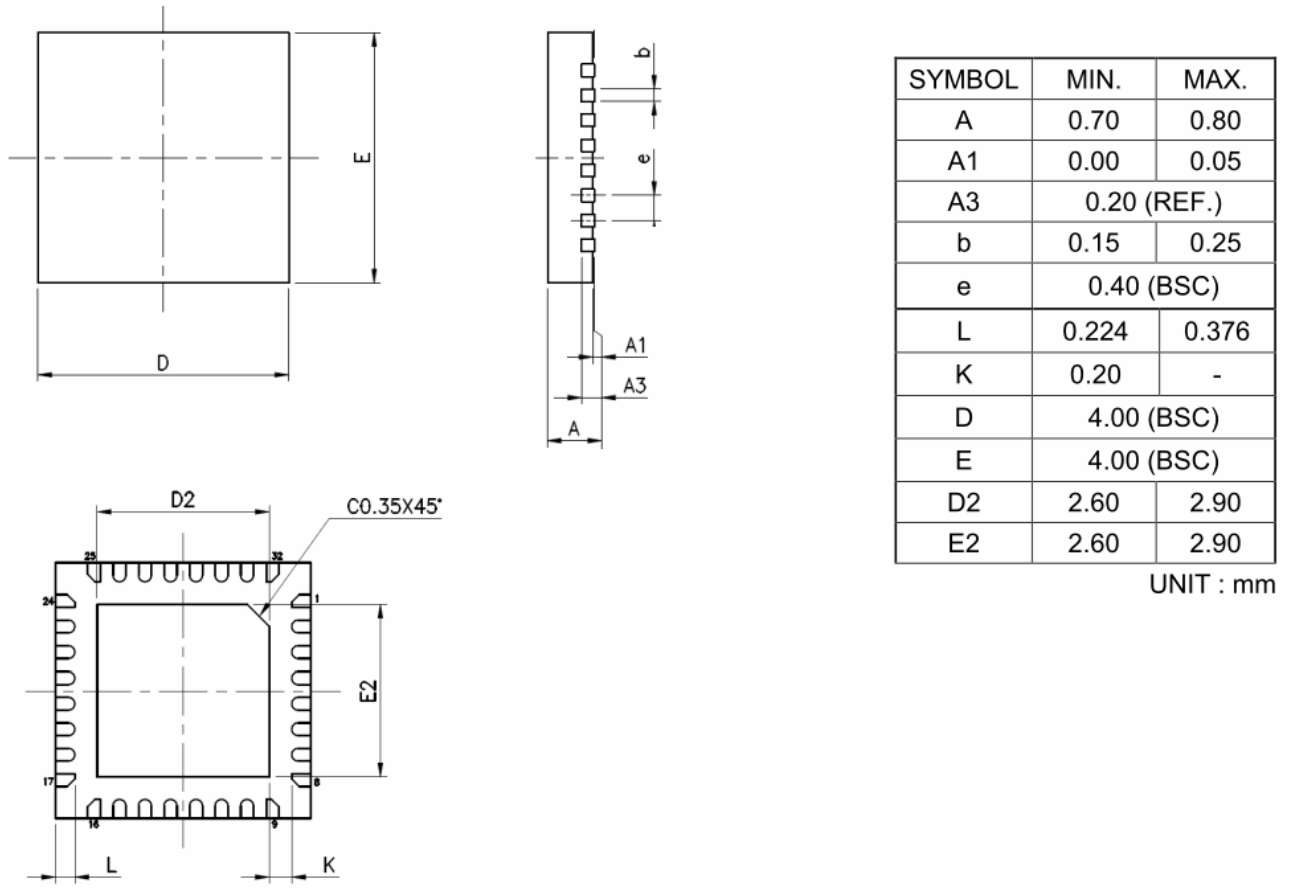


Figure 7-1 ST1624 Schematic Example

8 PACKAGE DIMENSION



SYMBOL	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 (REF.)	
b	0.15	0.25
e	0.40 (BSC)	
L	0.224	0.376
K	0.20	-
D	4.00 (BSC)	
E	4.00 (BSC)	
D2	2.60	2.90
E2	2.60	2.90

UNIT : mm

Figure 8-1 ST1624 Package Dimension

9 REVISION

REVISION	DESCRIPTION	PAGE	DATE
1.1	■ Add operating/idle current data	8	2014/10/22
1.0	■ Add package dimension	12	2014/09/09
0.1	■ First release		2014/09/05