SSD2118

Advance Information

320RGB x 240 a-Si TFT LCD Driver
Integrated Power Circuit, Gate and Source Driver

TABLE OF CONTENTS

TABLE OF TABLES

TABLE OF FIGURES

1 General Description

SSD2118 is an all in one a-Si TFT driver that integrated the power circuits, gate driver and source driver into single chip. It can drive a 16.7M / 262k / 8 color a-TFT panel with resolution of 320 RGB x 240. The interface follows 6/8 bit serial and 18/24 bit parallel RGB input signals and digital control timing signals.

It embeds DC-DC Converter and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. SSD2118 supports RGB Gamma settings. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

The driver can be operated down to 1.6V and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- 320RGBx240 single chip controller driver IC for 16.7M / 262k / 8 color amorphous silicon TFT LCD
- Power Supply
  - VDDEXT = VDDIO = 1.6V – 3.6V (I/O Interface)
  - VCI = 2.5V – 3.6V (power supply for internal analog circuit)
- Output Voltages
  - Gate Driver:
    - VGH-GND = 6V ~ 18V
    - VGL-GND = -6V ~ -15V
    - VGH-VGL = 30Vp-p
  - Source Driver:
    - V0 – V63 = AGND+0.1V ~ VCIX2-0.1V
    - Typical Source Output Voltage variation: ±15 mV
  - VCOM drive:
    - VCOMH = 2.5V ~ 6.0V
    - VCOML = 0V ~ -3.0V
    - VCOM amplitude = 6V (max)
- Operation frequency
  - 32MHz (max)
- System Interface
  - Serial Peripheral Interface (SPI), 3 wire, 4 wire and SPID interface
- Moving picture display interface
  - 18/24-bit RGB interface
  - 6/8-bit serial RGB interface
- Support low power consumption:
  - Low current sleep mode
  - 8-color display mode for power saving
  - Charge sharing function for switching circuits
  - Software settable for Shut and 8 color modes.
- Internal power supply circuit
  - Voltage generator
  - DC-DC converter up to 6x/-5x
- Support PWM backlight control
- Support stripe and delta pattern color filter.
- Support Frame and Line inversion AC drive
- Support Frame Rate Control (FRC)
- TFT storage capacitance: Cs on common
- Support source and gate scan direction control
- Built-in Non Volatile Memory (MTP) for VCOM calibration
- Auto sleep while VCI is lower than normal operation voltage

3 ORDERING INFORMATION

Ordering Part Number	Source	Gate	Package Form	Reference	Remark
SSD2118Z	320 x 3 (960)	240	Gold Bump Die		

Table 3-1 - Ordering Information

4 BLOCK DIAGRAM

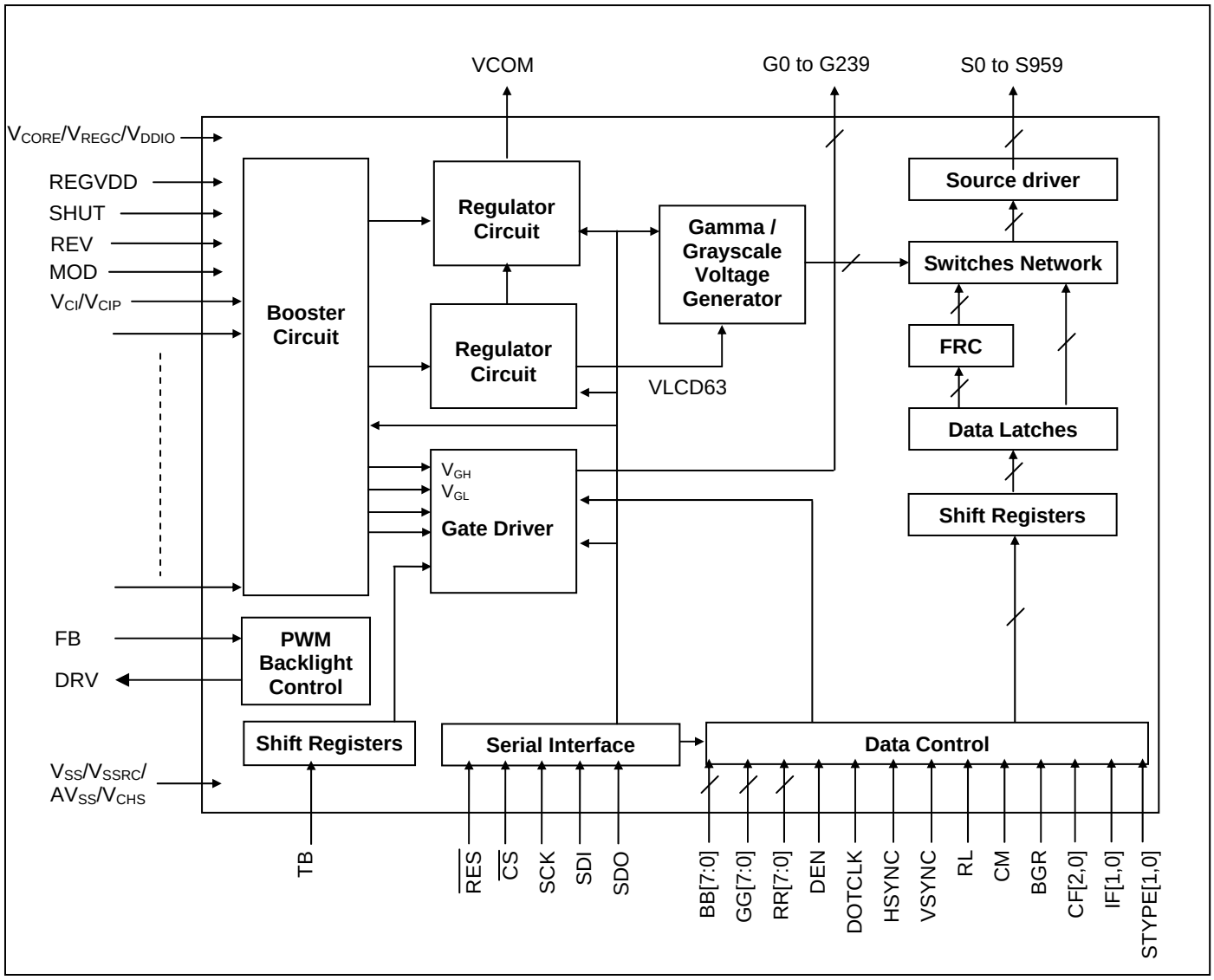
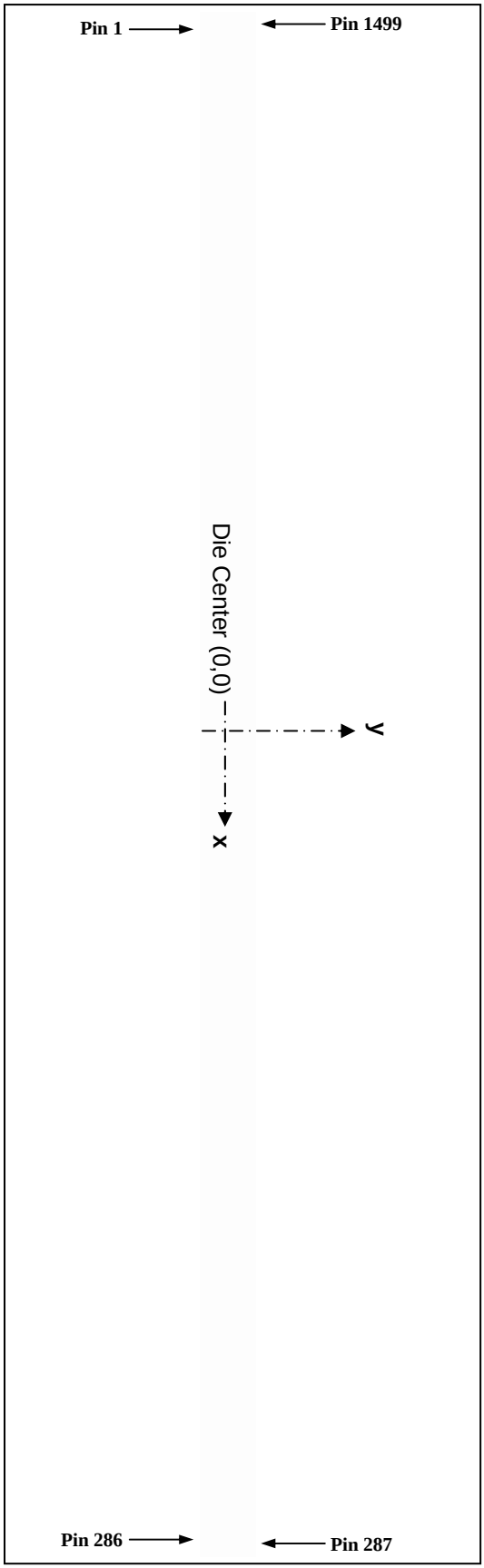


Figure 4-1 - SSD2118 Block Diagram Description

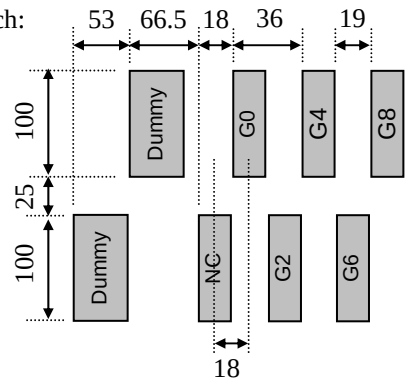
5 DIE PAD FLOOR PLAN



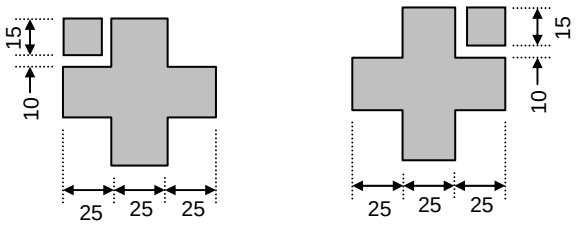
Die Information:

Die Size:	22170 x 809 μm^2
Die Thickness:	304 ± 25μm
Bump Height:	15 μm (Typ.)
Bump Co-planarity:	≤ 2 μm within die
Bump Size 1:	50 x 120 μm^2 (Pin 1 ~ 286)
Pad Pitch 1:	75 μm
Bump Size 2:	50 x 100 μm^2 (Pin 287, 288, 1498, 1499)
Pad Pitch 2:	53 μm
Bump Size 3:	17 x 100 μm^2 (Pin 289 ~ 1497)
Pad Pitch 3:	18 μm

Output Pad Pitch:



Alignment Marks:



Center:(-10945, -290)
Size: 75 x 75 μm^2

Center: (10945, -290)
Size: 75 x 75 μm^2

Figure 5-1 - SSD2118Z Die Floor Plan (Bump face up)

Drawings are not to scale

Table 5-1: SSD2118 Bump Die Pad Coordinates (Bump Centre)

Note: IC material temperature expansion factor is 2.6ppm, customer should take into account during panel design

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	DUMMY	-10800	-290	65	C3P	-5850	-290	129	CXP	-1050	-290	193	NC	3750	-290
2	VCOM	-10725	-290	66	C3P	-5775	-290	130	CXN	-975	-290	194	NC	3825	-290
3	VCOM	-10650	-290	67	C3P	-5700	-290	131	CXN	-900	-290	195	NC	3900	-290
4	NC	-10575	-290	68	C3P	-5625	-290	132	CXN	-825	-290	196	NC	3975	-290
5	NC	-10500	-290	69	IF1	-5550	-290	133	CXN	-750	-290	197	NC	4050	-290
6	VSS	-10425	-290	70	VCHS	-5475	-290	134	GAMAS1	-675	-290	198	NC	4125	-290
7	EXVR	-10350	-290	71	VCHS	-5400	-290	135	VSS	-600	-290	199	NC	4200	-290
8	EXVR	-10275	-290	72	VCHS	-5325	-290	136	NC	-525	-290	200	NC	4275	-290
9	VSS	-10200	-290	73	VCHS	-5250	-290	137	NC	-450	-290	201	NC	4350	-290
10	GPI3	-10050	-290	74	VCHS	-5175	-290	138	NC	-375	-290	202	NC	4425	-290
11	NC	-9975	-290	75	VCI	-5100	-290	139	NC	-300	-290	203	VSS	4500	-290
12	NC	-9900	-290	76	VCI	-5025	-290	140	NC	-225	-290	204	SDO	4575	-290
13	NC	-9825	-290	77	VCI	-4950	-290	141	NC	-150	-290	205	SDO	4650	-290
14	NC	-9750	-290	78	VCI	-4875	-290	142	VSS	-75	-290	206	SDC	4725	-290
15	NC	-9675	-290	79	VCI	-4800	-290	143	NC	0	-290	207	SDC	4800	-290
16	NC	-9600	-290	80	IF0	-4725	-290	144	NC	75	-290	208	CSB	4875	-290
17	NC	-9525	-290	81	VCIX2	-4650	-290	145	NC	150	-290	209	CSB	4950	-290
18	NC	-9450	-290	82	VCIX2	-4575	-290	146	NC	225	-290	210	SDI	5025	-290
19	NC	-9375	-290	83	VCIX2	-4500	-290	147	NC	300	-290	211	SDI	5100	-290
20	NC	-9300	-290	84	VCIX2	-4425	-290	148	VSS	375	-290	212	SCK	5175	-290
21	NC	-9225	-290	85	VCIX2J	-4350	-290	149	TESTA	450	-290	213	SCK	5250	-290
22	NC	-9150	-290	86	VCIX2J	-4275	-290	150	TESTB	525	-290	214	VCIP	5325	-290
23	NC	-9075	-290	87	VCIX2J	-4200	-290	151	VSS	600	-290	215	VCIP	5400	-290
24	NC	-9000	-290	88	VCIX2J	-4125	-290	152	NC	675	-290	216	VCI	5475	-290
25	NC	-8925	-290	89	VCIX2G	-4050	-290	153	GAMAS0	750	-290	217	VCI	5550	-290
26	NC	-8850	-290	90	VCIX2G	-3975	-290	154	BGR	825	-290	218	VCI	5625	-290
27	NC	-8775	-290	91	VCIX2G	-3900	-290	155	VDDIO	900	-290	219	VCI	5700	-290
28	NC	-8700	-290	92	VCIX2G	-3825	-290	156	NC	975	-290	220	VCI	5775	-290
29	NC	-8625	-290	93	NC	-3750	-290	157	VSS	1050	-290	221	DEN	5850	-290
30	NC	-8550	-290	94	CYP	-3675	-290	158	CM	1125	-290	222	VSS	5925	-290
31	GPI2	-8400	-290	95	CYP	-3600	-290	159	VDDIO	1200	-290	223	NC	6000	-290
32	VGH	-8325	-290	96	CYP	-3525	-290	160	RL	1275	-290	224	VDDIO	6075	-290
33	VGH	-8250	-290	97	CYP	-3450	-290	161	VSS	1350	-290	225	BB7	6150	-290
34	VGH	-8175	-290	98	CYN	-3375	-290	162	REGVDD	1425	-290	226	BB6	6225	-290
35	VGH	-8100	-290	99	CYN	-3300	-290	163	VDDIO	1500	-290	227	BB5	6300	-290
36	VGH	-8025	-290	100	CYN	-3225	-290	164	RESB	1575	-290	228	BB4	6375	-290
37	GPI1	-7950	-290	101	CYN	-3150	-290	165	VSS	1650	-290	229	BB3	6450	-290
38	C2P	-7875	-290	102	CF1	-3075	-290	166	REV	1725	-290	230	GG7	6525	-290
39	C2P	-7800	-290	103	CF0	-3000	-290	167	VDDIO	1800	-290	231	GG6	6600	-290
40	C2P	-7725	-290	104	VCI	-2925	-290	168	SPID	1875	-290	232	GG5	6675	-290
41	C2P	-7650	-290	105	VCI	-2850	-290	169	VSS	1950	-290	233	GG4	6750	-290
42	C2N	-7575	-290	106	VCI	-2775	-290	170	TB	2025	-290	234	GG3	6825	-290
43	C2N	-7500	-290	107	VCI	-2700	-290	171	VDDIO	2100	-290	235	RR7	6900	-290
44	C2N	-7425	-290	108	VCI	-2625	-290	172	GPIP	2175	-290	236	RR6	6975	-290
45	GPI0	-7350	-290	109	VCHS	-2550	-290	173	VSS	2250	-290	237	RR5	7050	-290
46	C1P	-7275	-290	110	VCHS	-2475	-290	174	STYPE1	2325	-290	238	RR4	7125	-290
47	C1P	-7200	-290	111	VCHS	-2400	-290	175	VDDIO	2400	-290	239	RR3	7200	-290
48	C1P	-7125	-290	112	VCHS	-2325	-290	176	STYPE0	2475	-290	240	RR2	7275	-290
49	C1P	-7050	-290	113	VCHS	-2250	-290	177	VSS	2550	-290	241	RR1	7350	-290
50	C1N	-6975	-290	114	HC	-2175	-290	178	VDDEXT	2625	-290	242	RR0	7425	-290
51	C1N	-6900	-290	115	HC	-2100	-290	179	VDDEXT	2700	-290	243	VDDIO	7500	-290
52	C1N	-6825	-290	116	HC	-2025	-290	180	VDDEXT	2775	-290	244	BB2	7575	-290
53	MOD	-6750	-290	117	HC	-1950	-290	181	VCORE	2850	-290	245	VSS	7650	-290
54	NC	-6675	-290	118	HC	-1875	-290	182	VCORE	2925	-290	246	HSYNC	7725	-290
55	VGL	-6600	-290	119	FB	-1800	-290	183	VCORE	3000	-290	247	VDDIO	7800	-290
56	VGL	-6525	-290	120	VCIM	-1725	-290	184	VREGC	3075	-290	248	VSYNC	7875	-290
57	VGL	-6450	-290	121	VCIM	-1650	-290	185	VREGC	3150	-290	249	VSS	7950	-290
58	VGL	-6375	-290	122	VCIM	-1575	-290	186	VREGC	3225	-290	250	DOTCLK	8025	-290
59	VGL	-6300	-290	123	VCIM	-1500	-290	187	VSS	3300	-290	251	DOTCLK	8100	-290
60	NC	-6225	-290	124	VCIM	-1425	-290	188	VSS	3375	-290	252	AVSS	8175	-290
61	C3N	-6150	-290	125	DRV	-1350	-290	189	VSS	3450	-290	253	AVSS	8250	-290
62	C3N	-6075	-290	126	CXP	-1275	-290	190	SHUT	3525	-290	254	AVSS	8325	-290
63	C3N	-6000	-290	127	CXP	-1200	-290	191	SHUT	3600	-290	255	VDDIO	8400	-290
64	C3N	-5925	-290	128	CXP	-1125	-290	192	VDDIO	3675	-290	256	VDDIO	8475	-290

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
257	VDDIO	8550	-290	321	G<63>	10296	175	385	G<191>	9144	175	449	S<923>	7992	175
258	VDDIO	8625	-290	322	G<65>	10278	300	386	G<193>	9126	300	450	S<922>	7974	300
259	TEST3	8700	-290	323	G<67>	10260	175	387	G<195>	9108	175	451	S<921>	7956	175
260	VLCD63	8775	-290	324	G<69>	10242	300	388	G<197>	9090	300	452	S<920>	7938	300
261	VCOMR	8850	-290	325	G<71>	10224	175	389	G<199>	9072	175	453	S<919>	7920	175
262	VCOMR	8925	-290	326	G<73>	10206	300	390	G<201>	9054	300	454	S<918>	7902	300
263	VCOMH	9000	-290	327	G<75>	10188	175	391	G<203>	9036	175	455	S<917>	7884	175
264	VCOMH	9075	-290	328	G<77>	10170	300	392	G<205>	9018	300	456	S<916>	7866	300
265	VCOMH	9150	-290	329	G<79>	10152	175	393	G<207>	9000	175	457	S<915>	7848	175
266	TEST4	9225	-290	330	G<81>	10134	300	394	G<209>	8982	300	458	S<914>	7830	300
267	VCOML	9300	-290	331	G<83>	10116	175	395	G<211>	8964	175	459	S<913>	7812	175
268	VCOML	9375	-290	332	G<85>	10098	300	396	G<213>	8946	300	460	S<912>	7794	300
269	VCOML	9450	-290	333	G<87>	10080	175	397	G<215>	8928	175	461	S<911>	7776	175
270	GG2	9525	-290	334	G<89>	10062	300	398	G<217>	8910	300	462	S<910>	7758	300
271	GG1	9600	-290	335	G<91>	10044	175	399	G<219>	8892	175	463	S<909>	7740	175
272	GG0	9750	-290	336	G<93>	10026	300	400	G<221>	8874	300	464	S<908>	7722	300
273	VSSRC	9825	-290	337	G<95>	10008	175	401	G<223>	8856	175	465	S<907>	7704	175
274	VSSRC	9900	-290	338	G<97>	9990	300	402	G<225>	8838	300	466	S<906>	7686	300
275	CDUM0	9975	-290	339	G<99>	9972	175	403	G<227>	8820	175	467	S<905>	7668	175
276	CDUM0	10050	-290	340	G<101>	9954	300	404	G<229>	8802	300	468	S<904>	7650	300
277	VSS	10125	-290	341	G<103>	9936	175	405	G<231>	8784	175	469	S<903>	7632	175
278	BB1	10200	-290	342	G<105>	9918	300	406	G<233>	8766	300	470	S<902>	7614	300
279	BB0	10275	-290	343	G<107>	9900	175	407	G<235>	8748	175	471	S<901>	7596	175
280	CSVCMP	10350	-290	344	G<109>	9882	300	408	G<237>	8730	300	472	S<900>	7578	300
281	CSVCMP	10425	-290	345	G<111>	9864	175	409	G<239>	8712	175	473	S<899>	7560	175
282	CSVCMN	10500	-290	346	G<113>	9846	300	410	NC	8694	300	474	S<898>	7542	300
283	CSVCMN	10575	-290	347	G<115>	9828	175	411	DUMMY	8676	175	475	S<897>	7524	175
284	VCOM	10650	-290	348	G<117>	9810	300	412	DUMMY	8658	300	476	S<896>	7506	300
285	VCOM	10725	-290	349	G<119>	9792	175	413	S<959>	8640	175	477	S<895>	7488	175
286	DUMMY	10800	-290	350	G<121>	9774	300	414	S<958>	8622	300	478	S<894>	7470	300
287	DUMMY	10975	175	351	G<123>	9756	175	415	S<957>	8604	175	479	S<893>	7452	175
288	DUMMY	10922	300	352	G<125>	9738	300	416	S<956>	8586	300	480	S<892>	7434	300
289	DUMMY	10872	175	353	G<127>	9720	175	417	S<955>	8568	175	481	S<891>	7416	175
290	G<1>	10854	300	354	G<129>	9702	300	418	S<954>	8550	300	482	S<890>	7398	300
291	G<3>	10836	175	355	G<131>	9684	175	419	S<953>	8532	175	483	S<889>	7380	175
292	G<5>	10818	300	356	G<133>	9666	300	420	S<952>	8514	300	484	S<888>	7362	300
293	G<7>	10800	175	357	G<135>	9648	175	421	S<951>	8496	175	485	S<887>	7344	175
294	G<9>	10782	300	358	G<137>	9630	300	422	S<950>	8478	300	486	S<886>	7326	300
295	G<11>	10764	175	359	G<139>	9612	175	423	S<949>	8460	175	487	S<885>	7308	175
296	G<13>	10746	300	360	G<141>	9594	300	424	S<948>	8442	300	488	S<884>	7290	300
297	G<15>	10728	175	361	G<143>	9576	175	425	S<947>	8424	175	489	S<883>	7272	175
298	G<17>	10710	300	362	G<145>	9558	300	426	S<946>	8406	300	490	S<882>	7254	300
299	G<19>	10692	175	363	G<147>	9540	175	427	S<945>	8388	175	491	S<881>	7236	175
300	G<21>	10674	300	364	G<149>	9522	300	428	S<944>	8370	300	492	S<880>	7218	300
301	G<23>	10656	175	365	G<151>	9504	175	429	S<943>	8352	175	493	S<879>	7200	175
302	G<25>	10638	300	366	G<153>	9486	300	430	S<942>	8334	300	494	S<878>	7182	300
303	G<27>	10620	175	367	G<155>	9468	175	431	S<941>	8316	175	495	S<877>	7164	175
304	G<29>	10602	300	368	G<157>	9450	300	432	S<940>	8298	300	496	S<876>	7146	300
305	G<31>	10584	175	369	G<159>	9432	175	433	S<939>	8280	175	497	S<875>	7128	175
306	G<33>	10566	300	370	G<161>	9414	300	434	S<938>	8262	300	498	S<874>	7110	300
307	G<35>	10548	175	371	G<163>	9396	175	435	S<937>	8244	175	499	S<873>	7092	175
308	G<37>	10530	300	372	G<165>	9378	300	436	S<936>	8226	300	500	S<872>	7074	300
309	G<39>	10512	175	373	G<167>	9360	175	437	S<935>	8208	175	501	S<871>	7056	175
310	G<41>	10494	300	374	G<169>	9342	300	438	S<934>	8190	300	502	S<870>	7038	300
311	G<43>	10476	175	375	G<171>	9324	175	439	S<933>	8172	175	503	S<869>	7020	175
312	G<45>	10458	300	376	G<173>	9306	300	440	S<932>	8154	300	504	S<868>	7002	300
313	G<47>	10440	175	377	G<175>	9288	175	441	S<931>	8136	175	505	S<867>	6984	175
314	G<49>	10422	300	378	G<177>	9270	300	442	S<930>	8118	300	506	S<866>	6966	300
315	G<51>	10404	175	379	G<179>	9252	175	443	S<929>	8100	175	507	S<865>	6948	175
316	G<53>	10386	300	380	G<181>	9234	300	444	S<928>	8082	300	508	S<864>	6930	300
317	G<55>	10368	175	381	G<183>	9216	175	445	S<927>	8064	175	509	S<863>	6912	175
318	G<57>	10350	300	382	G<185>	9198	300	446	S<926>	8046	300	510	S<862>	6894	300
319	G<59>	10332	175	383	G<187>	9180	175	447	S<925>	8028	175	511	S<861>	6876	175
320	G<61>	10314	300	384	G<189>	9162	300	448	S<924>	8010	300	512	S<860>	6858	300

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
513	S<859>	6840	175	577	S<795>	5688	175	641	S<731>	4536	175	705	S<667>	3384	175
514	S<858>	6822	300	578	S<794>	5670	300	642	S<730>	4518	300	706	S<666>	3366	300
515	S<857>	6804	175	579	S<793>	5652	175	643	S<729>	4500	175	707	S<665>	3348	175
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1052	S<321>	-2862	300	1116	S<257>	-4014	300	1180	S<193>	-5166	300	1244	S<129>	-6318	300
1053	S<320>	-2880	175	1117	S<256>	-4032	175	1181	S<192>	-5184	175	1245	S<128>	-6336	175
1054	S<319>	-2898	300	1118	S<255>	-4050	300	1182	S<191>	-5202	300	1246	S<127>	-6354	300
1055	S<318>	-2916	175	1119	S<254>	-4068	175	1183	S<190>	-5220	175	1247	S<126>	-6372	175
1056	S<317>	-2934	300	1120	S<253>	-4086	300	1184	S<189>	-5238	300	1248	S<125>	-6390	300
1057	S<316>	-2952	175	1121	S<252>	-4104	175	1185	S<188>	-5256	175	1249	S<124>	-6408	175
1058	S<315>	-2970	300	1122	S<251>	-4122	300	1186	S<187>	-5274	300	1250	S<123>	-6426	300
1059	S<314>	-2988	175	1123	S<250>	-4140	175	1187	S<186>	-5292	175	1251	S<122>	-6444	175
1060	S<313>	-3006	300	1124	S<249>	-4158	300	1188	S<185>	-5310	300	1252	S<121>	-6462	300
1061	S<312>	-3024	175	1125	S<248>	-4176	175	1189	S<184>	-5328	175	1253	S<120>	-6480	175
1062	S<311>	-3042	300	1126	S<247>	-4194	300	1190	S<183>	-5346	300	1254	S<119>	-6498	300
1063	S<310>	-3060	175	1127	S<246>	-4212	175	1191	S<182>	-5364	175	1255	S<118>	-6516	175
1064	S<309>	-3078	300	1128	S<245>	-4230	300	1192	S<181>	-5382	300	1256	S<117>	-6534	300
1065	S<308>	-3096	175	1129	S<244>	-4248	175	1193	S<180>	-5400	175	1257	S<116>	-6552	175
1066	S<307>	-3114	300	1130	S<243>	-4266	300	1194	S<179>	-5418	300	1258	S<115>	-6570	300
1067	S<306>	-3132	175	1131	S<242>	-4284	175	1195	S<178>	-5436	175	1259	S<114>	-6588	175
1068	S<305>	-3150	300	1132	S<241>	-4302	300	1196	S<177>	-5454	300	1260	S<113>	-6606	300
1069	S<304>	-3168	175	1133	S<240>	-4320	175	1197	S<176>	-5472	175	1261	S<112>	-6624	175
1070	S<303>	-3186	300	1134	S<239>	-4338	300	1198	S<175>	-5490	300	1262	S<111>	-6642	300
1071	S<302>	-3204	175	1135	S<238>	-4356	175	1199	S<174>	-5508	175	1263	S<110>	-6660	175
1072	S<301>	-3222	300	1136	S<237>	-4374	300	1200	S<173>	-5526	300	1264	S<109>	-6678	300
1073	S<300>	-3240	175	1137	S<236>	-4392	175	1201	S<172>	-5544	175	1265	S<108>	-6696	175
1074	S<299>	-3258	300	1138	S<235>	-4410	300	1202	S<171>	-5562	300	1266	S<107>	-6714	300
1075	S<298>	-3276	175	1139	S<234>	-4428	175	1203	S<170>	-5580	175	1267	S<106>	-6732	175
1076	S<297>	-3294	300	1140	S<233>	-4446	300	1204	S<169>	-5598	300	1268	S<105>	-6750	300
1077	S<296>	-3312	175	1141	S<232>	-4464	175	1205	S<168>	-5616	175	1269	S<104>	-6768	175
1078	S<295>	-3330	300	1142	S<231>	-4482	300	1206	S<167>	-5634	300	1270	S<103>	-6786	300
1079	S<294>	-3348	175	1143	S<230>	-4500	175	1207	S<166>	-5652	175	1271	S<102>	-6804	175
1080	S<293>	-3366	300	1144	S<229>	-4518	300	1208	S<165>	-5670	300	1272	S<101>	-6822	300
1081	S<292>	-3384	175	1145	S<228>	-4536	175	1209	S<164>	-5688	175	1273	S<100>	-6840	175
1082	S<291>	-3402	300	1146	S<227>	-4554	300	1210	S<163>	-5706	300	1274	S<99>	-6858	300
1083	S<290>	-3420	175	1147	S<226>	-4572	175	1211	S<162>	-5724	175	1275	S<98>	-6876	175
1084	S<289>	-3438	300	1148	S<225>	-4590	300	1212	S<161>	-5742	300	1276	S<97>	-6894	300
1085	S<288>	-3456	175	1149	S<224>	-4608	175	1213	S<160>	-5760	175	1277	S<96>	-6912	175
1086	S<287>	-3474	300	1150	S<223>	-4626	300	1214	S<159>	-5778	300	1278	S<95>	-6930	300
1087	S<286>	-3492	175	1151	S<222>	-4644	175	1215	S<158>	-5796	175	1279	S<94>	-6948	175
1088	S<285>	-3510	300	1152	S<221>	-4662	300	1216	S<157>	-5814	300	1280	S<93>	-6966	300

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1281	S<92>	-6984	175	1345	S<28>	-8136	175	1409	G<174>	-9288	175	1473	G<46>	-10440	175
1282	S<91>	-7002	300	1346	S<27>	-8154	300	1410	G<172>	-9306	300	1474	G<44>	-10458	300
1283	S<90>	-7020	175	1347	S<26>	-8172	175	1411	G<170>	-9324	175	1475	G<42>	-10476	175
1284	S<89>	-7038	300	1348	S<25>	-8190	300	1412	G<168>	-9342	300	1476	G<40>	-10494	300
1285	S<88>	-7056	175	1349	S<24>	-8208	175	1413	G<166>	-9360	175	1477	G<38>	-10512	175
1286	S<87>	-7074	300	1350	S<23>	-8226	300	1414	G<164>	-9378	300	1478	G<36>	-10530	300
1287	S<86>	-7092	175	1351	S<22>	-8244	175	1415	G<162>	-9396	175	1479	G<34>	-10548	175
1288	S<85>	-7110	300	1352	S<21>	-8262	300	1416	G<160>	-9414	300	1480	G<32>	-10566	300
1289	S<84>	-7128	175	1353	S<20>	-8280	175	1417	G<158>	-9432	175	1481	G<30>	-10584	175
1290	S<83>	-7146	300	1354	S<19>	-8298	300	1418	G<156>	-9450	300	1482	G<28>	-10602	300
1291	S<82>	-7164	175	1355	S<18>	-8316	175	1419	G<154>	-9468	175	1483	G<26>	-10620	175
1292	S<81>	-7182	300	1356	S<17>	-8334	300	1420	G<152>	-9486	300	1484	G<24>	-10638	300
1293	S<80>	-7200	175	1357	S<16>	-8352	175	1421	G<150>	-9504	175	1485	G<22>	-10656	175
1294	S<79>	-7218	300	1358	S<15>	-8370	300	1422	G<148>	-9522	300	1486	G<20>	-10674	300
1295	S<78>	-7236	175	1359	S<14>	-8388	175	1423	G<146>	-9540	175	1487	G<18>	-10692	175
1296	S<77>	-7254	300	1360	S<13>	-8406	300	1424	G<144>	-9558	300	1488	G<16>	-10710	300
1297	S<76>	-7272	175	1361	S<12>	-8424	175	1425	G<142>	-9576	175	1489	G<14>	-10728	175
1298	S<75>	-7290	300	1362	S<11>	-8442	300	1426	G<140>	-9594	300	1490	G<12>	-10746	300
1299	S<74>	-7308	175	1363	S<10>	-8460	175	1427	G<138>	-9612	175	1491	G<10>	-10764	175
1300	S<73>	-7326	300	1364	S<9>	-8478	300	1428	G<136>	-9630	300	1492	G<8>	-10782	300
1301	S<72>	-7344	175	1365	S<8>	-8496	175	1429	G<134>	-9648	175	1493	G<6>	-10800	175
1302	S<71>	-7362	300	1366	S<7>	-8514	300	1430	G<132>	-9666	300	1494	G<4>	-10818	300
1303	S<70>	-7380	175	1367	S<6>	-8532	175	1431	G<130>	-9684	175	1495	G<2>	-10836	175
1304	S<69>	-7398	300	1368	S<5>	-8550	300	1432	G<128>	-9702	300	1496	G<0>	-10854	300
1305	S<68>	-7416	175	1369	S<4>	-8568	175	1433	G<126>	-9720	175	1497	NC	-10872	175
1306	S<67>	-7434	300	1370	S<3>	-8586	300	1434	G<124>	-9738	300	1498	DUMMY	-10922	300
1307	S<66>	-7452	175	1371	S<2>	-8604	175	1435	G<122>	-9756	175	1499	DUMMY	-10975	175
1308	S<65>	-7470	300	1372	S<1>	-8622	300	1436	G<120>	-9774	300				
1309	S<64>	-7488	175	1373	S<0>	-8640	175	1437	G<118>	-9792	175				
1310	S<63>	-7506	300	1374	DUMMY	-8658	300	1438	G<116>	-9810	300				
1311	S<62>	-7524	175	1375	DUMMY	-8676	175	1439	G<114>	-9828	175				
1312	S<61>	-7542	300	1376	DUMMY	-8694	300	1440	G<112>	-9846	300				
1313	S<60>	-7560	175	1377	G<238>	-8712	175	1441	G<110>	-9864	175				
1314	S<59>	-7578	300	1378	G<236>	-8730	300	1442	G<108>	-9882	300				
1315	S<58>	-7596	175	1379	G<234>	-8748	175	1443	G<106>	-9900	175				
1316	S<57>	-7614	300	1380	G<232>	-8766	300	1444	G<104>	-9918	300				
1317	S<56>	-7632	175	1381	G<230>	-8784	175	1445	G<102>	-9936	175				
1318	S<55>	-7650	300	1382	G<228>	-8802	300	1446	G<100>	-9954	300				
1319	S<54>	-7668	175	1383	G<226>	-8820	175	1447	G<98>	-9972	175				
1320	S<53>	-7686	300	1384	G<224>	-8838	300	1448	G<96>	-9990	300				
1321	S<52>	-7704	175	1385	G<222>	-8856	175	1449	G<94>	-10008	175				
1322	S<51>	-7722	300	1386	G<220>	-8874	300	1450	G<92>	-10026	300				
1323	S<50>	-7740	175	1387	G<218>	-8892	175	1451	G<90>	-10044	175				
1324	S<49>	-7758	300	1388	G<216>	-8910	300	1452	G<88>	-10062	300				
1325	S<48>	-7776	175	1389	G<214>	-8928	175	1453	G<86>	-10080	175				
1326	S<47>	-7794	300	1390	G<212>	-8946	300	1454	G<84>	-10098	300				
1327	S<46>	-7812	175	1391	G<210>	-8964	175	1455	G<82>	-10116	175				
1328	S<45>	-7830	300	1392	G<208>	-8982	300	1456	G<80>	-10134	300				
1329	S<44>	-7848	175	1393	G<206>	-9000	175	1457	G<78>	-10152	175				
1330	S<43>	-7866	300	1394	G<204>	-9018	300	1458	G<76>	-10170	300				
1331	S<42>	-7884	175	1395	G<202>	-9036	175	1459	G<74>	-10188	175				
1332	S<41>	-7902	300	1396	G<200>	-9054	300	1460	G<72>	-10206	300				
1333	S<40>	-7920	175	1397	G<198>	-9072	175	1461	G<70>	-10224	175				
1334	S<39>	-7938	300	1398	G<196>	-9090	300	1462	G<68>	-10242	300				
1335	S<38>	-7956	175	1399	G<194>	-9108	175	1463	G<66>	-10260	175				
1336	S<37>	-7974	300	1400	G<192>	-9126	300	1464	G<64>	-10278	300				
1337	S<36>	-7992	175	1401	G<190>	-9144	175	1465	G<62>	-10296	175				
1338	S<35>	-8010	300	1402	G<188>	-9162	300	1466	G<60>	-10314	300				
1339	S<34>	-8028	175	1403	G<186>	-9180	175	1467	G<58>	-10332	175				
1340	S<33>	-8046	300	1404	G<184>	-9198	300	1468	G<56>	-10350	300				
1341	S<32>	-8064	175	1405	G<182>	-9216	175	1469	G<54>	-10368	175				
1342	S<31>	-8082	300	1406	G<180>	-9234	300	1470	G<52>	-10386	300				
1343	S<30>	-8100	175	1407	G<178>	-9252	175	1471	G<50>	-10404	175				
1344	S<29>	-8118	300	1408	G<176>	-9270	300	1472	G<48>	-10422	300				

Note: IC material Temperature expansion factor should take into account during panel design.

6 PIN DESCRIPTION

SSD2118Z Pin Function Description

Key:

I = Input
O =Output
I/O = Bi-directional (input/output)
P = Power pin
GND = System VSS

Table 6-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
V_{SS}	P	GND	Ground of Power Supply	System ground pin of the IC.	-
A_{VSS}		GND		Grounding for analog circuit.	-
V_{SSRC}		GND		Grounding for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages.	-
V_{CHS}		GND		Grounding for booster circuit.	-
V_{CORE}	P	V_{REGC}	Power for Core Logic	V_{DD} for core use - Connect a capacitor for stabilization	-
V_{DDEXT}		System V_{DD}	Power for Internal VCORE Regulator	Voltage input pin for internal logic. Connect to System V_{DD} (refer to power connection Figure 14-1)	-
V_{DDIO}		System V_{DD}	Power for Interface Logic Pins	Voltage input pin for logic I/O.	-
V_{CI}	P	Power supply	Power for Analog Circuits	Booster input voltage pin. - Connect to voltage source between 2.5V to 3.6V	-
V_{CIP}		V_{CI}		Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages.	-
HC		V_{SS}		Connect to V_{SS}	-
V_{CIM}	O	Stabilizing capacitor	Booster Output	Negative voltage of V_{CI}	-
V_{CIX2}	O	Stabilizing capacitor	Booster Voltages	Booster voltage and regulated between 5.1V to 6.3V. Controlled by command Power control 2 (R0Ch)	-
V_{CIX2J}		V_{CIX2} on FPC	Voltage for analog	power supply used by on chip analog blocks and V_{GH}/V_{GL} dcdc. Must connect V_{CIX2} together	-
V_{CIX2G}		V_{CIX2} on FPC	Voltage for analog	power supply used by on chip analog blocks and V_{GH}/V_{GL} dcdc. Must connect V_{CIX2} together	-
V_{COMH}	O	Stabilizing capacitor	Voltages for V_{COM} Signal	This pin indicates a HIGH level of V_{COM} generated in driving the V_{COM} alternation.	-
V_{COML}		Stabilizing capacitor		This pin indicates a LOW level of V_{COM} generated in driving the V_{COM} alternation.	-
V_{LCD63}	O	Stabilizing capacitor	LCD Driving Voltages	This pin is the maximum source driver voltage.	-
V_{GH}		Stabilizing capacitor		A positive power output pin for gate driver.	-
V_{GL}		Stabilizing capacitor		A negative power output pin for gate driver.	-
EXVR	I	V_{SS}	External	External reference of internal Gamma resistor.	-

V_{COMR}	I	External voltage source or Open	Reference	This pin provides voltage reference for internal voltage regulator when register VDV[4:0] of Power Control 4 is set to “01111”.	Open
V_{REGC}	P	Stabilizing capacitor	Regulator output for logic circuits	Regulator output for V_{CORE} use	-
CXP	P	Booster capacitor	Booster and Stabilization Capacitors	- Connect a capacitor to CXN	-
CXN				- Connect a capacitor to CXP	-
CYP		Booster capacitor		- Connect a capacitor to CYN	-
CYN				- Connect a capacitor to CYP	-
C1P		Booster capacitor		- Connect a capacitor to C1N	-
C1N				- Connect a capacitor to C1P	-
C2P		Booster capacitor		- Connect a capacitor to C2N	-
C2N				- Connect a capacitor to C2P	-
C3P		Booster capacitor		- Connect a capacitor to C3N	-
C3N				- Connect a capacitor to C3P	-
CDUM0		Charge Sharing		- Connect a capacitor to VSS	Open
CSVCMP		Charge Sharing		- Connect a capacitor to CSVCMN	Open
CSVCMN				- Connect a capacitor to CSVCMP	Open

Table 6-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
SPID	I	V_{DDIO} or V_{SS}	Serial Interface	ID selection pin for the SPI serial interface. When sending serial data, the "ID" bit must match with the logic stage of this pin. (Refer to Serial Interface block description on Page 21 for details)	-
CSB		MPU		Chip select pin of serial interface.	V_{DDIO}
SDI		MPU		Data input pin in serial mode.	V_{SS}
SDC		MPU		Data/Command pin of serial interface.	V_{SS}
SCK		MPU		Clock input pin in serial mode.	V_{SS}
SDO	O	MPU	Serial Interface	Data output pin in serial mode.	Open
SHUT	I	V_{DDIO} or V_{SS}	Logic Control	Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. - Connect to V_{DDIO} for sleep mode - Connect to V_{SS} for normal operating mode Note: Software can override the setting	V_{DDIO} or V_{SS}
VSYNC	I	MPU	RGB Interface	Frame synchronization signal. Fixed to V_{DDIO} or V_{SS} if not used.	-
HSYNC	I	MPU		Line synchronization signal. Fixed to V_{DDIO} or V_{SS} if not used	-
DOTCLK	I	MPU	Display Timing Signals	Dot-clock signal and oscillator source. External clock must be provided to that pin even at front or black porch non-display period.	-
DEN	I	MPU		Display enable pin from controller.	V_{DDIO}
RR[7:0]	I	MPU	Graphic Display Data	- RR[7:0] : Red Data –24bit parallel/8bit serial - GG[7:0] : Green Data –24bit parallel - BB[7:0] : Blue Data –24bit parallel - RR[7:2] : Red Data –18bit parallel/6bit serial - GG[7:2] : Green Data –18bit parallel - BB[7:2] : Blue Data –18bit parallel	V_{DDIO} or V_{SS}
GG[7:0]					
BB[7:0]					
RESB	I	MPU	System reset	System reset pin. Initialization occurs once this pin is pulled Low, the minimum pulse length is 1ms. A low pulse must be applied after power-on. Connect this pin to VDDIO when not used.	V_{DDIO}
GPI[3:0]	I	User define		General propose pins defined by user	Open (GPIP=V_{SS})
GPIP	I	V_{DDIO}	Logic Control	Enable pin for GPI [3:0]. - Connect to V_{DDIO} to activate GPI [3:0] - Connect to V_{SS} to disable GPI [3:0]	V_{ss}
IF[1:0]	I	V_{DDIO} or V_{SS}	Graphic Display Interface	IF[1:0] = 10 ; Serial IF[1:0] = 11 ; Parallel Note: Software can override the setting	-
GAMAS1	I	V_{DDIO} or V_{SS}	Logic Control	GAMAS[1:0] controls the default register values	V_{DDIO} or V_{SS}
GAMAS0	I				

Table 6-3: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
STYPE0	I	V_{DDIO} or V_{SS}	Serial Interface Selection	STYPE[1:0] = 0x ; SPID type 3 wires SPI STYPE[1:0] = 10 ; standard 3 wires SPI STYPE[1:0] = 11 ; standard 4 wires SPI	-
STYPE1	I	V_{DDIO} or V_{SS}			-
REGVDD	I	V_{DDIO}	Logic Control	Input pin to enable internal voltage regulation. - Connect to VDDIO	-
FB	I	PWM feedback voltage	Voltage reference	PWM controller feedback input. FB threshold	Vss
MOD	I	V_{DDIO} or V_{SS}	Panel Type Selection	MOD = 0 ; Stripe type MOD = 1 ; Delta type Note: Software can override the setting	V_{DDIO} or V_{SS}
CF[1:0]	I	V_{DDIO} or V_{SS}	Logic Control	Select the delta type color filter arrangement Note: Software can override the setting	V_{DDIO} or V_{SS}
BGR	I	V_{DDIO} or V_{SS}	Panel Mapping controls	Color mapping selection pin. Refer to S0-S959 pin description. Note: Software can override the setting	V_{DDIO} or V_{SS}
REV	I	V_{DDIO} or V_{SS}		Input pin to select the display reversion. - Connect to V_{DDIO} mapping data "0" to maximum pixel voltage for normal white panel - Connect to V_{SS} mapping data "0" to minimum pixel voltage for normal black panel Note: Software can override the setting	V_{DDIO} or V_{SS}
RL	I	V_{DDIO} or V_{SS}		Select the Source driver data shift direction. - Connect to V_{DDIO} for display first RGB data at S0-S2 - Connect to V_{SS} for display first RGB data at S959-S957 Note: Software can override the setting	V_{DDIO} or V_{SS}
TB	I	V_{DDIO} or V_{SS}		Select the Gate driver scan direction. Note: Software can override the setting	V_{DDIO} or V_{SS}
CM	I	V_{DDIO} or V_{SS}		Input pin to select 16.7M/262k-color or 8-color display mode. After entered 8-color display mode, the driver will switch to Frame-Inversion-Mode, and only MSB of the data Red, Green and Blue will be considered. - Connect to V_{DDIO} for 8-color display mode - Connect to V_{SS} for 16.7M/262k-color display mode Note: Software can override the setting	V_{DDIO} or V_{SS}

Table 6-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
VCOM	O	LCD	LCD Driving Signals	A power supply for the TFT-display common electrode.	Open
G0-G239		LCD		Gate driver output pins. These pins output VGH or VGL level.	Open
S0-S959		LCD		Source driver output pins. Color filter arrangement depends on BGR and MOD pins. For stripe type: S(3n): Display Red if BGR = Low, Blue if BGR = High. S(3n+1): Display Green. S(3n+2): Display Blue if BGR = Low, Red if BGR = High.	Open
DRV	O	PWM Booster	PWM Driving Signals	PWM output driver signal for the boost converter	Open

Table 6-5: Miscellaneous Pins

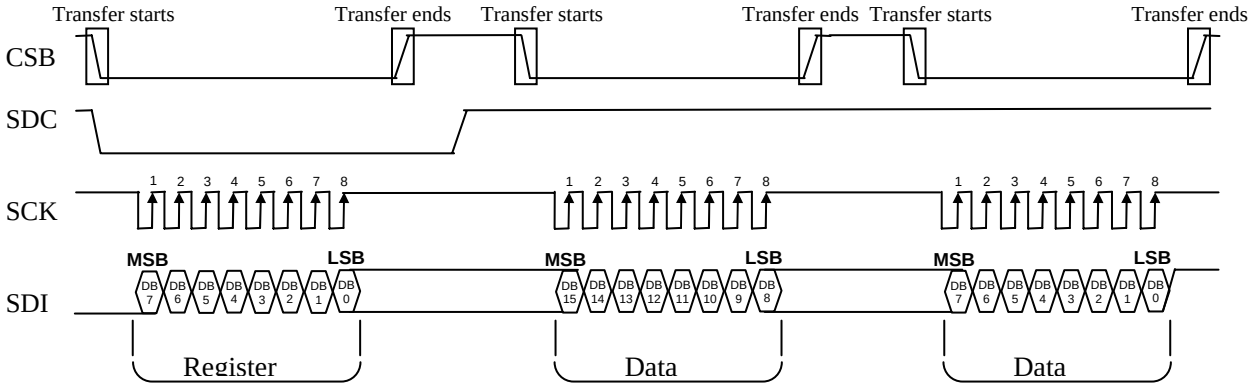
Name	Type	Connect to	Function	Description	When not in use
NC	-	-	-	These pins must be left open and cannot be connected together	Open
DUMMY	-	-	-	Floating pins and no connection inside the IC. These pins can be shorted together or connect to any signal.	Open
TESTA/B	I/O	FPC	IC Testing Signal	Test pin of the internal circuit. - Leave this pin open and optional to insert test point in FPC for evaluation.	Open
TEST3/4		FPC		Test pin of the internal circuit. - Leave this pin open and optional to insert test point in FPC for evaluation.	Open

7 Block Function Description

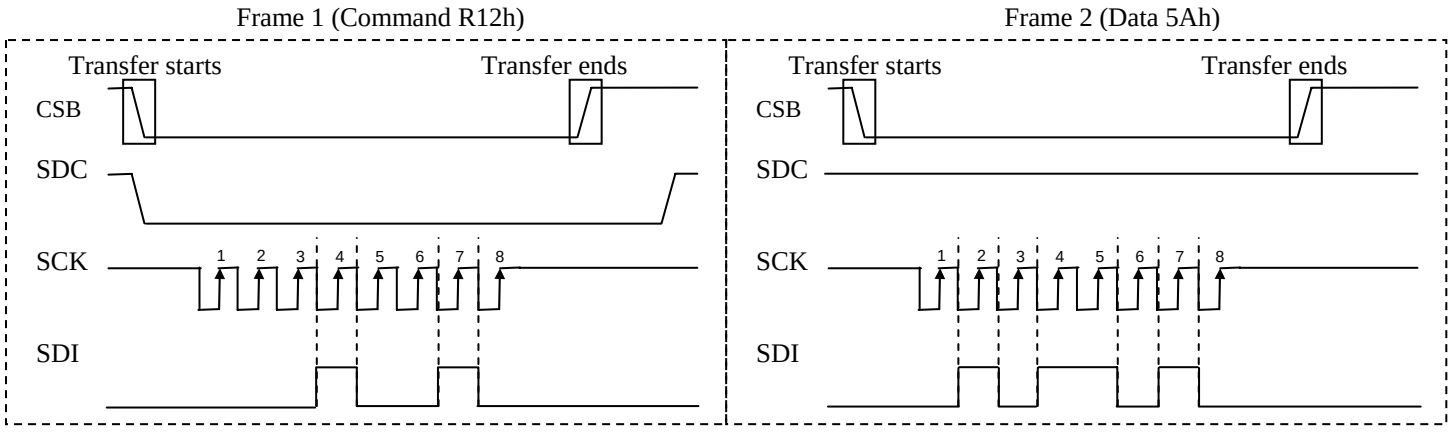
7.1 Serial Interface

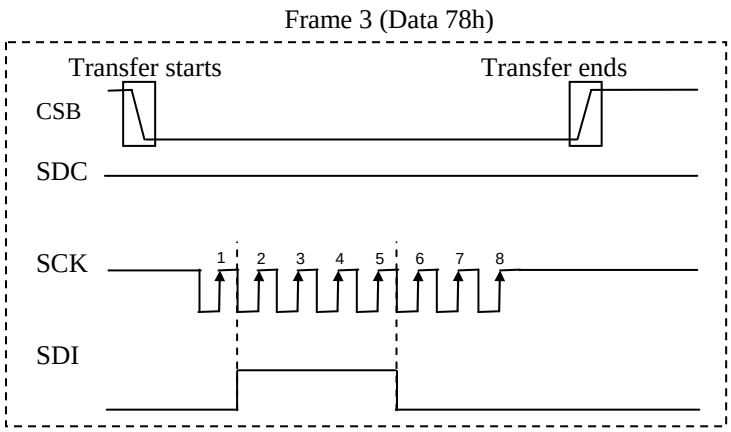
7.1.1 Serial Interface – 4-wires (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB.SDC determinate the data of SDI which is register or data.



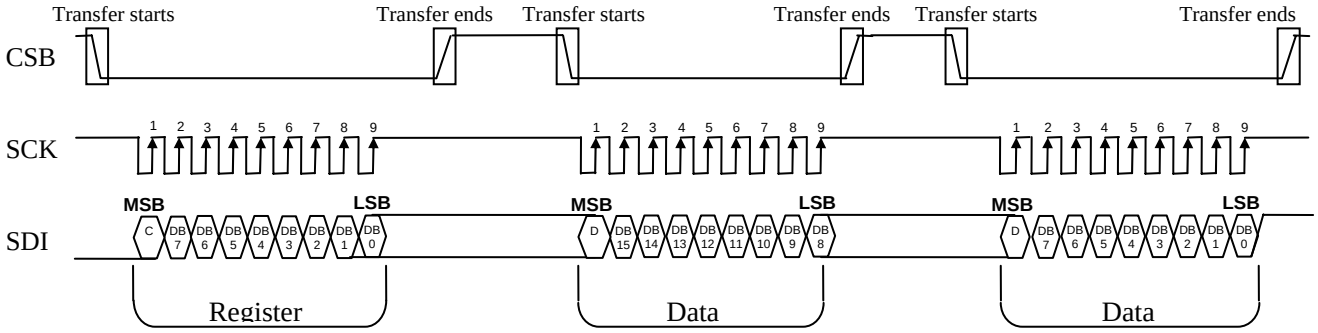
Example of 4-wires (8 bits) – R12h 5A78h



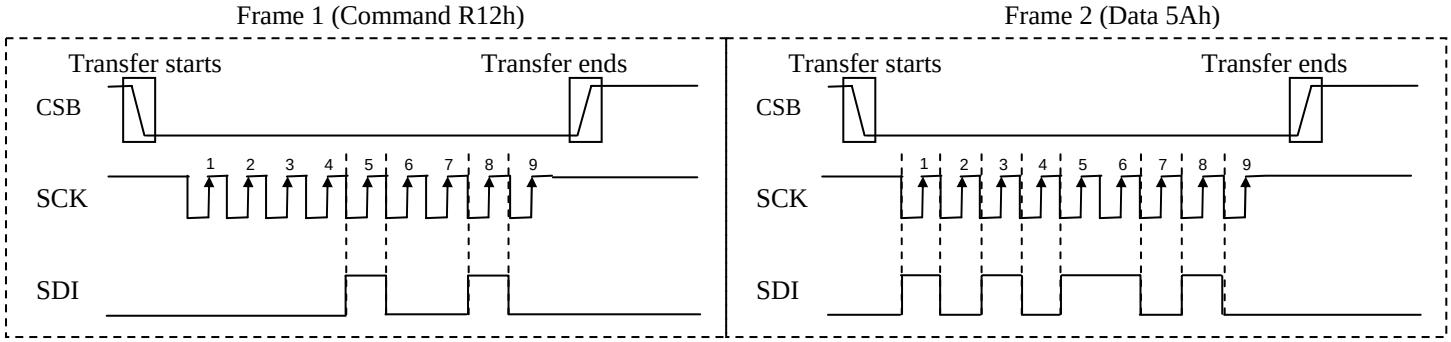


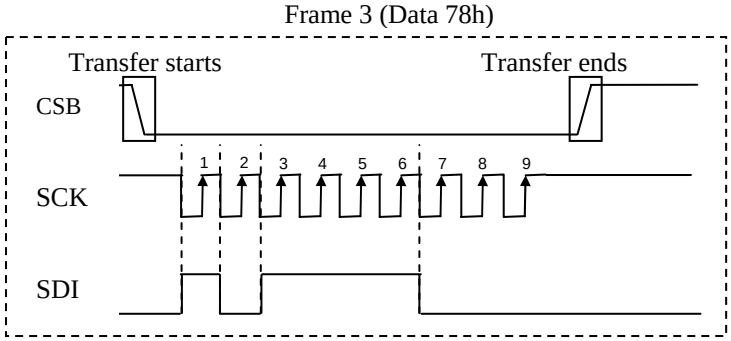
7.1.2 Serial Interface – 3-wires (9 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB. DC bit determinate the data of SDI which is register or data.



Example of 3-wires (9 bits) – R12h 5A78h

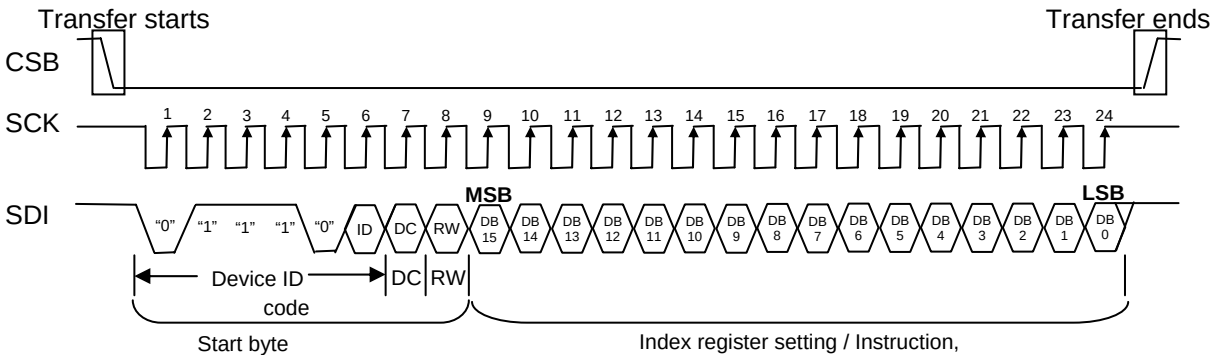




7.1.3 Serial Interface – 3-wires (24 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (CSB), serial transfer clock line (SCK), serial input data (SDI), and serial output data (SDO). The serial data transfer starts at the falling edge of CSB input and ends at the rising edge of CSB. DC bit determinate the data of SDI which is register or data. RW bit determinate the read / write operation.

Write

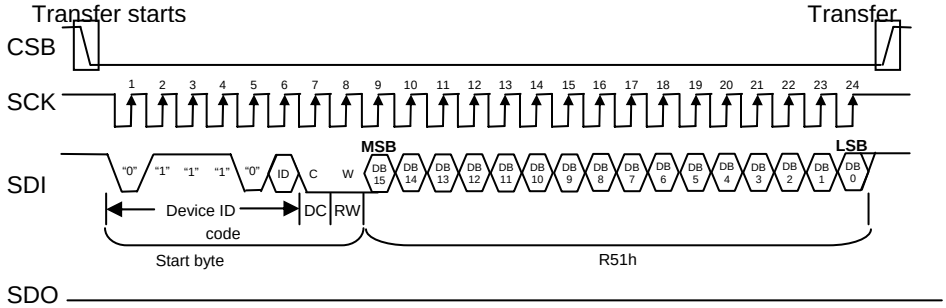


Read GPI

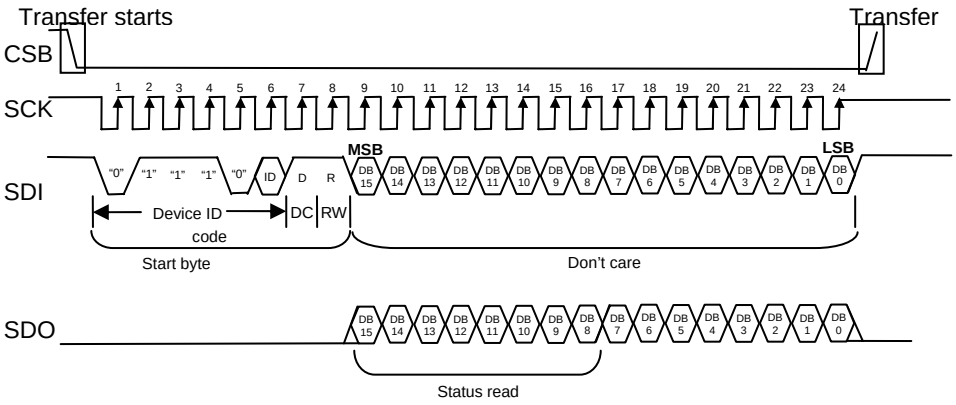
Command Code:

1. R28hx0006h – enable R2x command
2. R2Bhx8520h – enable SDO read

1st step read - Index register



2nd step read - Data at SDO



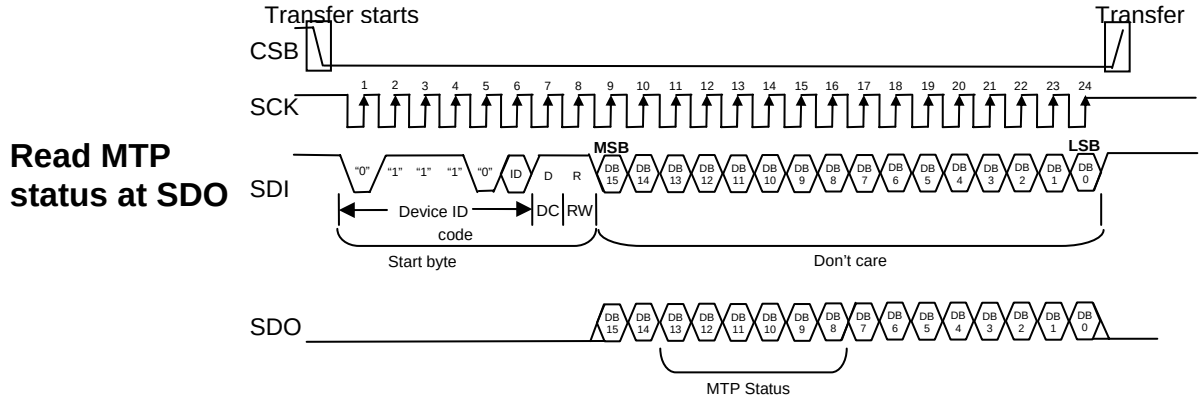
Read MTP

Command Code:

1. R28hx0006h – enable R2x command
2. R1Fhx0000h – ensure the SDO reading is MTP value
3. R2Bhx8520h – enable SDO read
4. R2EhxB941h – enable MTP read status

After that, D/C bit need to set to 1 and RW bit need to be set to 1 in the 24bits SPI interface, bit 8~13 at the SDO pin is the MTP status.

Note: More than 16 frames between leave sleep mode and Read MTP



7.2 Data Control

The display data and frame position information from the controller is synchronized with the Gate Drive circuit and shift registered for the Source Driver circuit.

7.3 Booster and Regulator Circuit

These two functional blocks generate the voltage of V_{GH}, V_{GL}, V_{COMH}, V_{COML} and V_{LCD63} which are necessary for operating a TFT LCD.

7.4 Shift Register

The shift registers control the direction of line scanning of source and gate.

7.5 Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the Source Driver to output the required voltage level.

7.6 Reset Circuit

This block is integrated into the Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given in Section 8 Command Table:

8 COMMAND TABLE

Table 8-1: Command Table and POR (Power On Reset) values

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output control	0	1	CF1	CF0	REV	MOD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
	(XXEFh)			X	X	X	X	X	0	X	X	1	1	1	0	1	1	1	1
R02h	LCD-Driving-Waveform Control	0	1	0	0	0	0	0	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0300h)			0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	(9490h)			1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	EQ2	0	0	0	0	0	0	0
	(D800h)			1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0005h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ch)			0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	VCOMAS
	(3000h)			0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Uniformity and low VCI detect	0	1	0	0	0	0	0	0	0	0	ENSVIN	1	0	1	ENVDET	1	0	0
	(005Ch)			0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0
R11h	Shut and 8 color	0	1	0	0	0	0	0	0	0	CM	0	0	0	0	0	0	0	SHUT
				0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	X
R12h	Entry Control	0	1	0	0	0	0	0	0	0	0	0	IF1	IF0	CMI	IFS1	IFS0	0	0
				0	0	0	0	0	0	0	0	0	X	X	1	0	1	0	0
R13h	PWM Control	0	1	0	0	0	0	FBR2	FBR1	FBR0	PWMEN	0	0	0	DRVCLK 1	DRVCLK 0	PWM2	PWM1	PWM0
	(0802h)			0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
R16h	Pixel per line	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0
R17h	Vertical Porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nMTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(0032h)			0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
R1Fh	Power control (6)	0	1	0	0	VCMT5	VCMT4	VCMT3	VCMT2	VCMT1	VCMT0	0	0	VCMR5	VCMR4	VCMR3	VCMR2	VCMR1	VCMR0
	(0632h)			0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	γ control (1)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
	(0301h)			0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1
R32h	γ control (1)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R33h	γ control (1)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
	(0207h)			0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1
R34h	γ control (1)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
	(0505h)			0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1
R35h	γ control (1)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R36h	γ control (1)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	γ control (1)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
	(0303h)			0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
R3Ah	γ control (2)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
	(0d0Fh)			0	0	0	0	1	1	0	1	0	0	0	0	1	1	1	1
R3Bh	γ control (2)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00
	(0E05h)			0	0	0	0	1	1	1	0	0	0	0	0	0	1	0	1

R28h	VCOM MTP	0	1	0	0	0	0	0	0	0	0	0	0	0	0	CCB3	CCB2	CCB1	CCB0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R29h	Turn on VCIX2	0	1	1	0	0	0	0	0	0	0	1	VCIX2	0	0	0	0	0	0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R2Bh	SDO Read and Pump/Burntime	0	1	ENSDO	0	0	0	PUMPT 1	PUMPT 0	BURNT 1	BURNT 0	0	MSENS E1	MSENS E0	0	0	0	0	0
	(0520h)			0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0
R2Ch	VCOM Charge sharing	0	1	1	0	VCOM SH	0	1	0	0	0	1	0	0	0	1	1	0	1
	(888Dh)			1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	1
R2Dh	Unregulated VCIX2	0	1	0	0	1	1	1	1	1	1	0	1	0	UNREG	0	0	0	0
	(3F40h)			0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0
R2Eh	Enable MTP Read and FRC	0	1	1	0	1	1	1	0	0	FFRC	0	1	ALTRE AD	0	0	0	0	LFRC
	(B941h)			1	0	1	1	1	0	0	1	0	1	0	0	0	0	0	1
R3Fh ~ R50h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
R51h	Read GPI	1	1	0	0	0	0	GPI3	GPI2	GPI1	GPI0	0	0	0	0	0	0	0	0
				0	0	0	0	X	X	X	X	0	0	0	0	0	0	0	0
R52h ~ R99h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Note: X means hardware defining default setting

Table 8-2 – Gamma Registers POR value

Command R30h-R3Bh	GAMAS[1:0] 00	GAMAS[1:0] 01	GAMAS[1:0] 10	GAMAS[1:0] 11
PKP0	000	000	000	000
PKP1	000	000	000	000
PKP2	001	001	111	010
PKP3	011	011	111	011
PKP4	010	100	011	100
PKP5	010	010	000	101
PRP0	111	110	001	010
PRP1	010	011	100	011
VRP0	1111	1111	1011	0000
VRP1	01101	01111	01101	10000
PKN0	101	101	111	001
PKN1	101	011	011	000
PKN2	011	011	000	010
PKN3	000	011	000	110
PKN4	111	111	111	111
PKN5	111	111	111	111
PRN0	011	011	100	011
PRN1	011	011	010	011
VRN0	0101	1010	1011	0101
VRN1	01110	10000	01101	01111

Table 8-3: Registers POR value at GAMAS[1:0] = 00

Reg#	Register	Hex code	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R03h	Power control (1)	9490	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0
R0Ch	Power control (2)	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R0Dh	Power control (3)	000C	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R0Eh	Power control (4)	3000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R1Eh	Power control (5)	0032	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
R1Fh	Power control (6)	0632	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0

Table 8-4: Registers POR value at GAMAS[1:0] = 01

Reg#	Register	Hex code	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R03h	Power control (1)	9496	1	0	0	1	0	1	0	0	1	0	0	1	0	1	1	0
R0Ch	Power control (2)	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R0Dh	Power control (3)	000C	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R0Eh	Power control (4)	3000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R1Eh	Power control (5)	002B	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1
R1Fh	Power control (6)	182B	0	0	0	1	1	0	0	0	0	0	1	0	1	0	1	1

Table 8-5: Registers POR value at GAMAS[1:0] = 10

Reg#	Register	Hex code	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R03h	Power control (1)	7A7E	0	1	1	1	1	0	1	0	0	1	1	1	1	1	1	0
R0Ch	Power control (2)	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R0Dh	Power control (3)	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R0Eh	Power control (4)	2B00	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0
R1Eh	Power control (5)	002D	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
R1Fh	Power control (6)	0D2D	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1

Table 8-6: Registers POR value at GAMAS[1:0] = 11

Reg#	Register	Hex code	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R03h	Power control (1)	9490	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0
R0Ch	Power control (2)	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R0Dh	Power control (3)	000C	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R0Eh	Power control (4)	3000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R1Eh	Power control (5)	0031	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1
R1Fh	Power control (6)	1031	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1

9 COMMAND DESCRIPTION

Index (IR)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to R7Fh). It sets the register number in the range of 0000000 to 1111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Driver Output Control (R01h) (POR = XXEFh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	CF1	CF0	REV	MOD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
POR		X	X	X	X	X	0	X	X	1	1	1	0	1	1	1	1

CF1-0: For MOD = "1", define the color filter arrangement of delta pattern.

MOD = 1	CF0 = 0	CF0 = 1
CF1 = 0	R G B R G B R G B B R G B R G B R G R G B R G B R G B B R G B R G B R G	R G B R G B R G B G B R G B R G B R R G B R G B R G B G B R G B R G B R
CF1 = 1	B G R B G R B G R R B G R B G R B G B G R B G R B G R R B G R B G R B G	B G R B G R B G R G R B G R B G R B B G R B G R B G R G R B G R B G R B

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data [7:2]	Source Output level	
		VCOM = "H"	VCOM = "L"
1	000000B : 111111B	V63 : V0	V0 : V63
0	000000B : 111111B	V0 : V63	V63 : V0

MOD: Selects the type of color filter. When MOD = "1", delta type color filter is selected. When MOD = "0", stripe type color filter is selected.

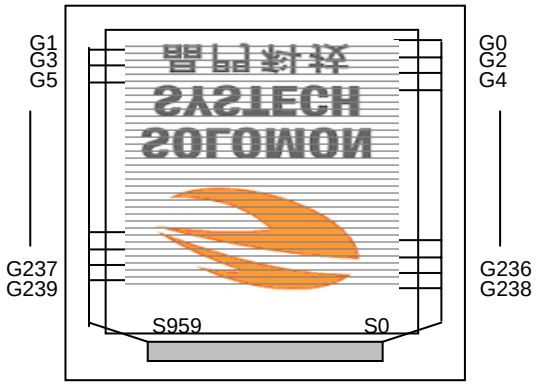
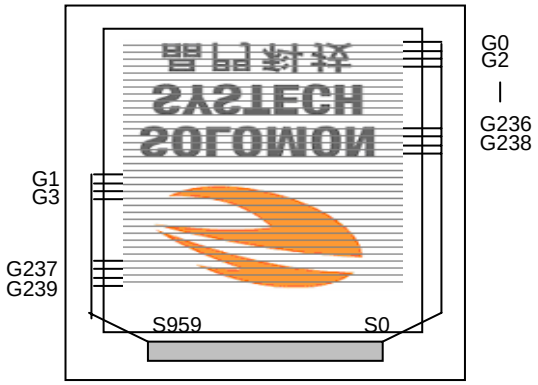
BGR: For MOD = "0", selects the <R><G><B> arrangement. When BGR = "0" <R><G><B> color is assigned from S0. When BGR = "1" <B><G><R> color is assigned from S0.

SM: For MOD = "0", change the division of gate driver. When SM = "0", odd/even division (interlace mode) is selected. When SM = "1", upper/lower division is selected. Select the division mode according to the mounting method.

TB: For MOD = "0", selects the output shift direction of the gate driver. When TB = "1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

RL: For MOD = “0”, selects the output shift direction of the source driver of stripe type. When RL = “1”, S0 shifts to S959 and <R><G><B> color is assigned from S1. When RL = “0”, S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits CF, REV, MOD, BGR, SM, TB and RL are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

MOD = 0	SM = 0	SM = 1
TB = 1 **RL = 0**		
TB = 0 **RL = 0**		
TB = 1 **RL = 1**		
TB = 0 **RL = 1**		

LCD-Driving-Waveform Control (R02h) (POR = 0300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
POR		0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

B/C: Select the liquid crystal drive waveform VCOM.

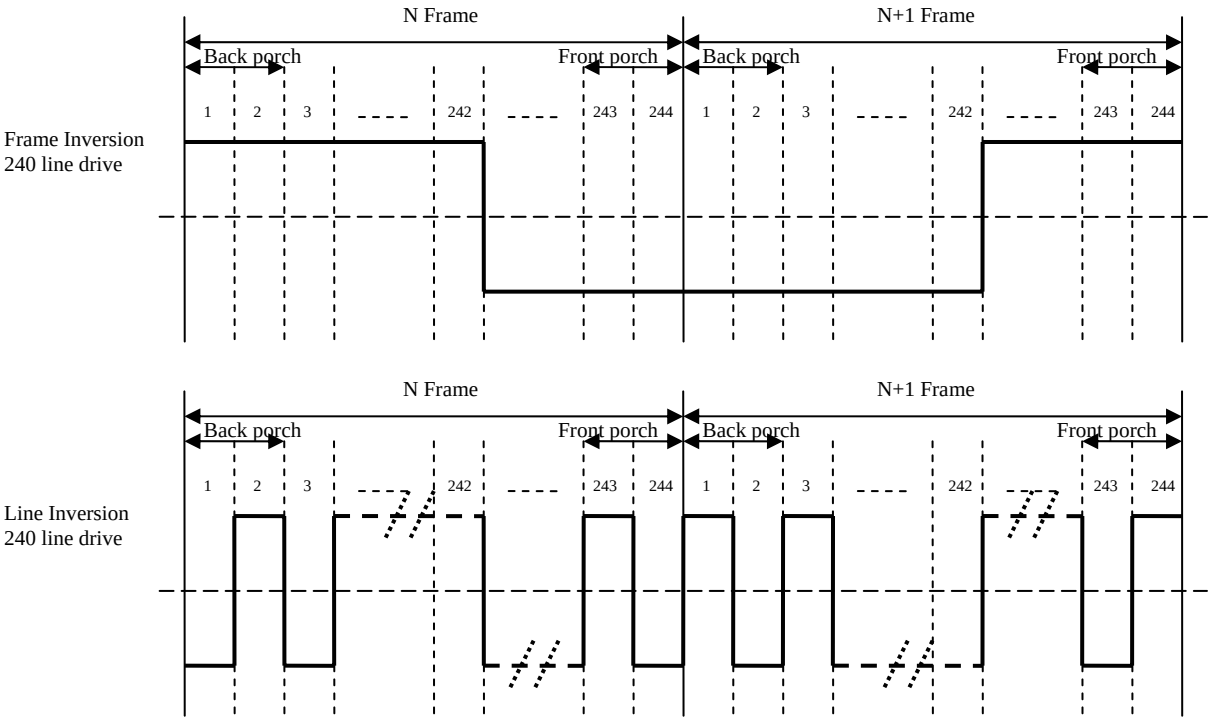
When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW6-0: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW6-0 alternate for every set value + 1 lines.

Figure 9-1: Line Inversion AC Driver



Power control 1 (R03h) (POR = 9490h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
POR		1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = V_{DDIO}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline × 14
0	0	0	1	Fline × 12
0	0	1	0	Fline × 8
0	0	1	1	Fline × 7
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 64
1	0	1	1	fosc / 80
1	1	0	0	fosc / 96
1	1	0	1	fosc / 128
1	1	1	0	fosc / 160
1	1	1	1	fosc / 256

Note: Fline = Horizontal frequency
fosc = Pixel clock frequency

BT2-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	VCIX2 x 3	-(VGH - VCI)	+6	-5
0	0	1	VCIX2 x 3	-(VGH - VCIX2)	+6	-4
0	1	0	VCIX2 x 3	-(VCIX2)	+6	-2
0	1	1	VCIX2 x 2 + VCI	-(VGH)	+5	-5
1	0	0	VCIX2 x 2 + VCI	-(VGH - VCI)	+5	-4
1	0	1	VCIX2 x 2 + VCI	-(VGH - VCIX2 x 2)	+5	-3
1	1	0	VCIX2 x 2	-(VGH)	+4	-4
1	1	1	VCIX2 x 2	-(VGH - VCI)	+4	-3

DC3-0: Set the step-up cycle of the step-up circuit for 16.7M/262k-color mode (CM = V_{SS}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline × 14
0	0	0	1	Fline × 12
0	0	1	0	Fline × 8
0	0	1	1	Fline × 7
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 64
1	0	1	1	fosc / 80
1	1	0	0	fosc / 96
1	1	0	1	fosc / 128
1	1	1	0	fosc / 160
1	1	1	1	fosc / 256

Note: Fline = Horizontal frequency
fosc = Pixel clock frequency

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. While there is no display, such as the system is in a sleep mode, AP2-0 can be set to (0,0,0) and shutting down the operational amplifier can reduce the power consumption.

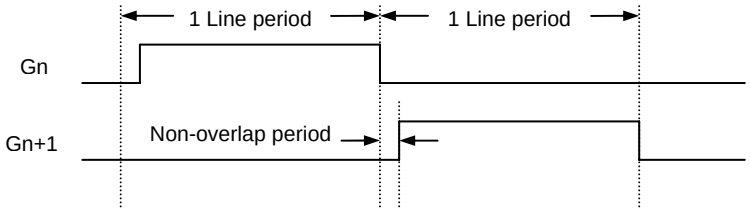
AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Frame Cycle Control (R0Bh) (POR = D800h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	EQ2	0	0	0	0	0	0	0
POR		1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	HSYNC_falling + 100 Pixel clock
0	1	HSYNC _falling + 60 Pixel clock
1	0	HSYNC _falling + 30 Pixel clock
1	1	9 Pixel clock after Source On

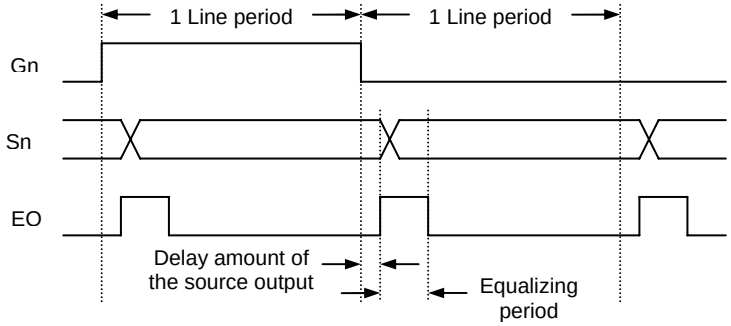


SDT1-0: Set delay amount from the gate output signal falling edge of the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	HSYNC_falling – 3 Pixel clock
0	1	HSYNC_falling – 7 Pixel clock
1	0	HSYNC_falling – 11 Pixel clock
1	1	HSYNC_falling – 15 Pixel clock

EQ2-0: Sets the equalizing period on source

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	28 Pixel clock cycle
0	1	0	42 Pixel clock cycle
0	1	1	After VCOM charge sharing + 12 Pixel clock cycle
1	0	0	64 Pixel clock cycle
1	0	1	80 Pixel clock cycle
1	1	0	96 Pixel clock cycle
1	1	1	106 Pixel clock cycle



Power Control 2 (R0Ch) (POR = 0005h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	VCIX2 voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserved
1	1	1	Reserved

Note: VCI=3.3V and without panel loading
Figures on the above table are target VCIX2 output, actual VCIX2 voltage depends on VCI, booster efficiency and panel loading

Power Control 3 (R0Dh) (POR = 000Ch)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
POR		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

VRH3-0: Set amplitude magnification of V_{LCD63}. These bits amplify the V_{LCD63} voltage 1.78 to 3.00 times the Vref voltage set by VRH3-0.

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.815
0	0	0	1	Vref x 2.905
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

Note: Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R0Eh) (POR = 3000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	VCOMAS
POR		0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

VCOMG: When VCOMG = "1", it is possible to set output voltage of V_{COML} to any level, and the instruction (VDV4-0) becomes available. When VCOMG = "0", V_{COML} output is fixed to Hi-z level, V_{CI2} output for V_{COML} power supply stops, and the instruction (VDV4-0) becomes unavailable. Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV4-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.23 times the V_{LCD63} voltage. When VCOMG = "0", the settings become invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOMA
0	0	0	0	0	V_{LCD63} x 0.60
0	0	0	0	1	V_{LCD63} x 0.63
0	0	0	1	0	V_{LCD63} x 0.66
:	:	:	:	:	: Step = 0.03 :
0	1	1	0	1	V_{LCD63} x 0.99
0	1	1	1	0	V_{LCD63} x 1.02
0	1	1	1	1	External Voltage Reference
1	0	0	0	0	V_{LCD63} x 1.05
1	0	0	0	1	V_{LCD63} x 1.08
:	:	:	:	:	: Step = 0.03 :
1	0	1	0	1	V_{LCD63} x 1.20
1	0	1	1	0	V_{LCD63} x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

Note1: VCOMA < 6.0V
Note2: VCOMH – VCOML < 6.0V
Note3: |VCOML| < VCI

VCOMAS: Set the equation of V_{COML}.

$$V_{COML} = \alpha \text{ x } V_{COMH} - V_{COMA}$$

VCOMAS	α
0	1
1	Reserved

Uniformity and low VCI detect (R10h) (POR = 005Ch)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	ENSVIN	1	0	1	ENVDET	1	0	0
POR		0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0

ENSVIN: When ENSVIN = 1, uniformity improvement scheme is enabled
When ENSVIN = 0, uniformity improvement scheme is disabled

ENVDET: When ENVDET = 1, low VCI detector is enabled. Enter sleep mode automatically while VCI is lower than 2.4V +/-0.1V.
When ENVDET = 0, low VCI detector is disabled.

Shut and 8 color (R11h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	CM	0	0	0	0	0	0	0	SHUT
POR		0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	X

CM: When CM = 1, 8-color mode is selected.
When CM = 0, 16.7M/262k color mode is selected.

SHUT: When SHUT = 1, the driver enters into the sleep mode. In the sleep mode, the internal display operations are halted.

Note: **The default setting of register bits CM and SHUT are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.**
Enter sleep mode automatically while VCI is lower than 2.4V +/-0.1V.

Entry Mode (R12h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	IF1	IF0	CMI	IFS1	IFS0	0	0
POR		0	0	0	0	0	0	0	0	0	X	X	1	0	1	0	0

IF1-0: Selection for serial and parallel interfaces.

CMI: Selection for 6/8-bit serial or 18/24-bit parallel RGB interfaces. Set CMI = 0 for current version.

IFS1-0: Selection for HV SYNC, DEN, with and without dummy modes.

IF1	IF0	CMI	IFS1	IFS0	Interface
1	0	0	0	0	6-bit serial RGB DEN Mode (Without dummy)
1	0	0	0	1	6-bit serial RGB DEN Mode (With dummy)
1	0	0	1	0	6-bit serial RGB HV SYNC Mode (Without dummy)
1	0	0	1	1	6-bit serial RGB HV SYNC Mode (With dummy)
1	0	1	0	0	8-bit serial RGB DEN Mode (Without dummy)
1	0	1	0	1	8-bit serial RGB DEN Mode (With dummy)
1	0	1	1	0	8-bit serial RGB HV SYNC Mode (Without dummy)
1	0	1	1	1	8-bit serial RGB HV SYNC Mode (With dummy)
1	1	0	0	0	18-bit digital RGB DEN Mode
1	1	0	0	1	18-bit digital RGB HV SYNC Mode
1	1	1	0	0	24-bit digital RGB DEN Mode
1	1	1	0	1	24-bit digital RGB HV SYNC Mode

R12h	6-bit serial	8-bit serial	18-bit parallel	24-bit parallel	DEN mode	SYNC mode	Dummy mode
0014h							
0034h							
0040h	✓				✓		
0044h	✓				✓		✓
0048h	✓					✓	
004Ch	✓					✓	✓
0050h		✓			✓		
0054h		✓			✓		✓
0058h		✓				✓	
005Ch		✓				✓	✓
0060h			✓		✓		
0064h			✓			✓	
0070h				✓	✓		
0074h				✓		✓	

Note: For DEN mode, minimum vertical porch = 2 and minimum horizontal porch = 4

PWM control (R13h) (POR = 0802h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FBR2	FBR1	FBR0	PWMEN	0	0	0	DRVCLK1	DRVCLK0	PWM2	PWM1	PWM0
POR		0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

PWMEN: When PWMEN = "1", back light power control will be activated
When PWMEN = "0", back light power control will not be activated.

DRVCLK1-0: Set the frequency of DRV.

DRVCLK1	DRVCLK0	PWM Frequency
0	0	Pixel Clock / 24
0	1	Pixel Clock / 32
1	0	Pixel Clock / 64
1	1	Pixel Clock / 128

PWM2-0: Set the PWM duty ratio.

PWM2	PWM1	PWM0	PWM Duty Ratio
0	0	0	10%
0	0	1	30%
0	1	0	50%
0	1	1	60%
1	0	0	65%
1	0	1	70%
1	1	0	80%
1	1	1	90%

FBR2-0: Set the reference voltage for FB.

FBR2	FBR1	FBR0	FB Refrence voltage
0	0	0	0.40
0	0	1	0.50
0	1	0	0.60
0	1	1	0.65
1	0	0	0.70
1	0	1	0.75
1	1	0	0.80
1	1	1	0.20

Pixel per line (R16h) (POR = 9F86h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

Note: **Number of Pixel Clock for hsync active low period must be smaller than that of HBP**
Only for 18/24-bit parallel and 6/8-bit serial interface.

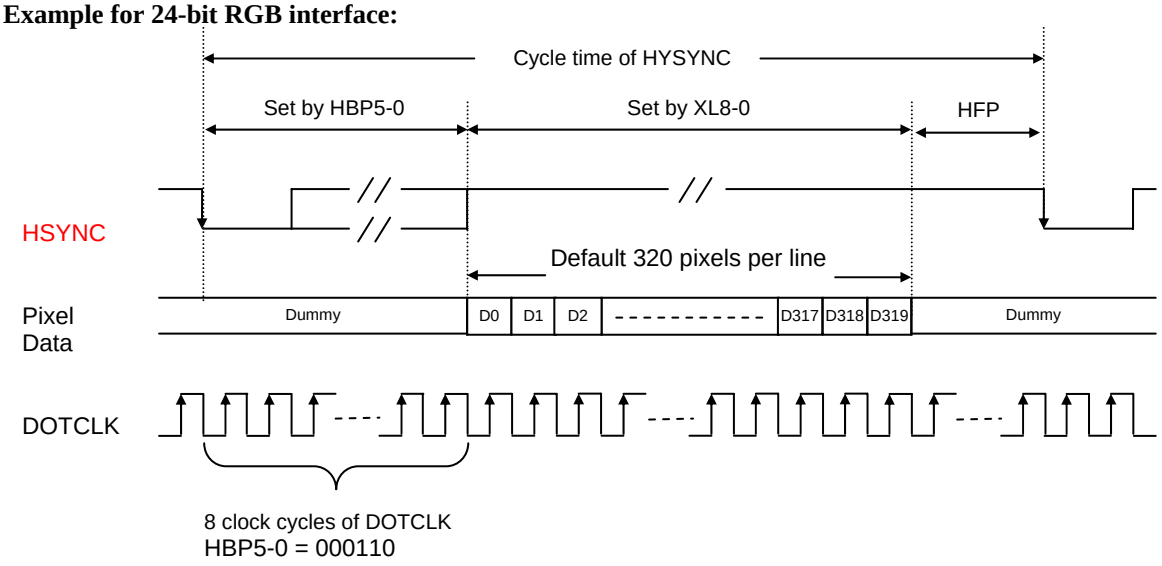
XL8-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

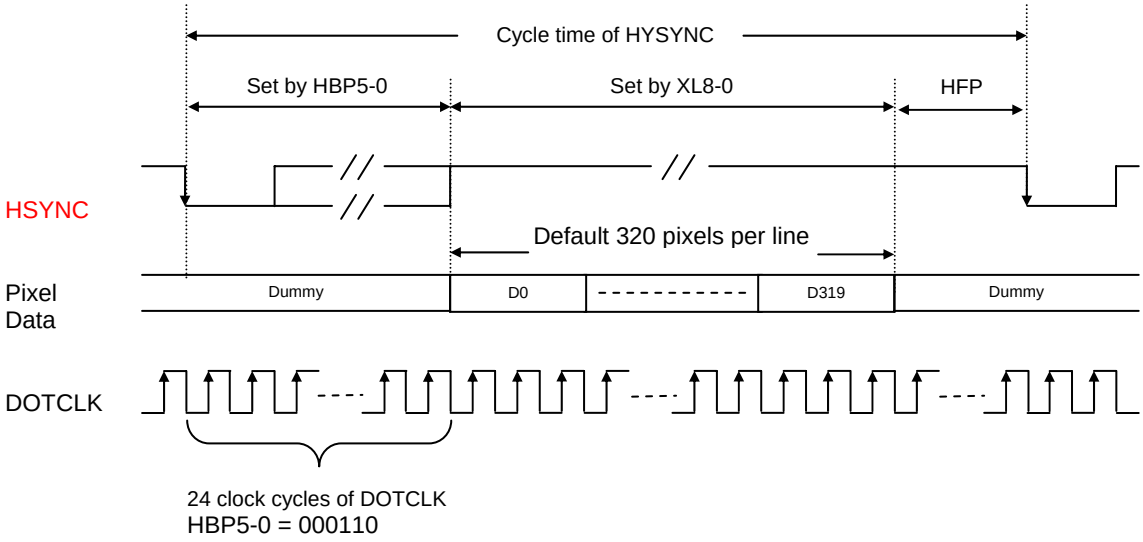
HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK		
						18/24-bit RGB	6/8-bit RGB (without dummy)	6/8-bit RGB (with dummy)
0	0	0	0	0	0	2	6	8
0	0	0	0	0	1	3	9	12
0	0	0	0	1	0	4	12	16
0	0	0	0	1	1	5	15	20
0	0	0	1	0	0	6	18	24
0	0	0	1	0	1	7	21	28
0	0	0	1	1	0	8	24	32
0	0	0	1	1	1	9	27	36
0	0	1	0	0	0	10	30	40
			:			: Step = 1 :	: Step = 3 :	: Step = 4 :
1	1	1	1	1	0	64	192	256
1	1	1	1	1	1	65	195	260

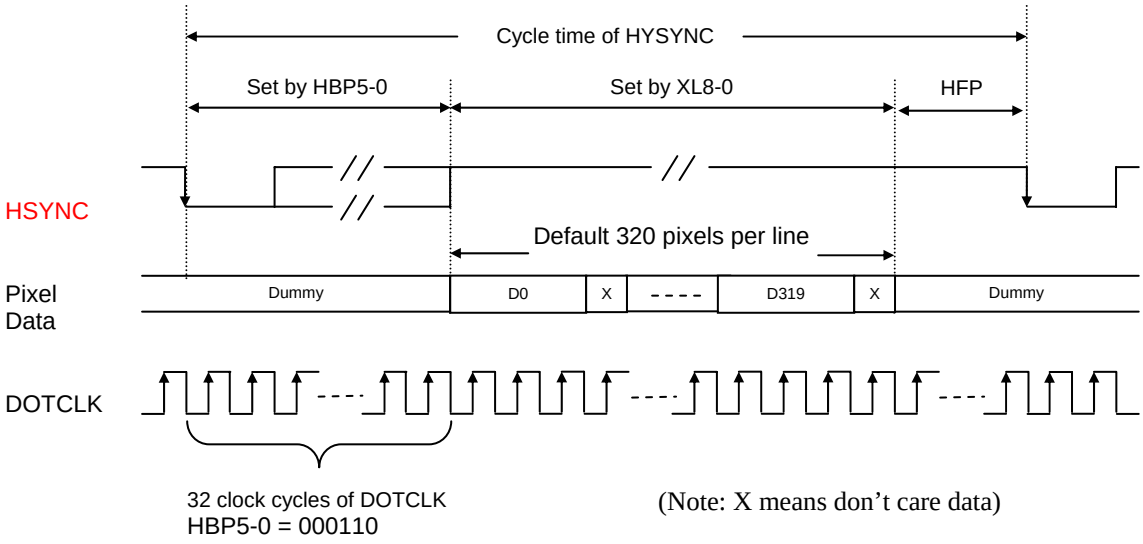
Example for 24-bit RGB interface:



Example for 8-bit RGB interface (without dummy):



Example for 8-bit RGB interface (with dummy):



(Note: X means don't care data)

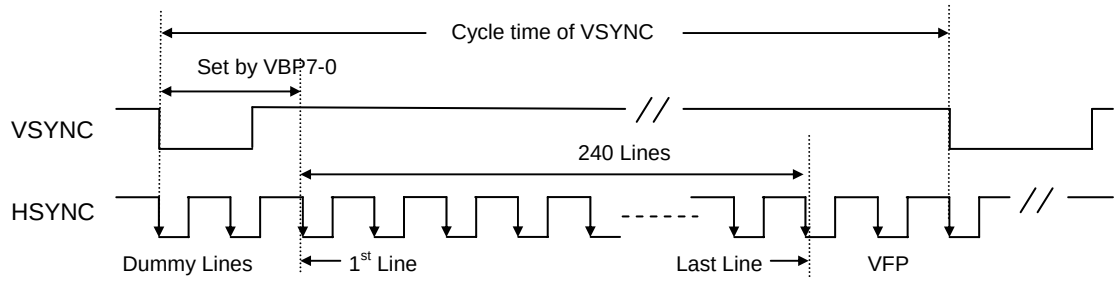
Vertical Porch (R17h) (POR = 0002h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
:	:	:	:	:	:	:	:	: Step = 1 :
1	1	1	0	1	1	1	1	239
1	1	1	1	0	0	0	0	240
1	1	1	1	*	*	*	*	Reserved

Example for 24-bit RGB interface:



Power Control 5 (R1Eh) (POR = 0032h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nMTP	0	VCM3	VCM4	VCM3	VCM2	VCM1	VCM0
POR		0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

nMTP: nMTP equals to "0" after power on reset and V_{COMH} voltage equals to programmed MTP value. When nMTP set to "1", setting of VCM5-0 becomes valid and voltage of V_{COMH} can be adjusted.

VCM5-0: Set the V_{COMH} voltage if nMTP = "1". These bits amplify the V_{COMH} voltage 0.36 to 0.99 times the V_{LCD63} voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	V_{COMH}
0	0	0	0	0	0	V_{LCD63} x 0.36
0	0	0	0	0	1	V_{LCD63} x 0.37
			:			: Step = 0.01 :
1	1	1	1	1	0	V_{LCD63} x 0.98
1	1	1	1	1	1	V_{LCD63} x 0.99

Note: VCI < V_{COMH} < V_{CIX2}

Power Control 6 (R1Fh) (POR = 0632h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCMT5	VCMT4	VCMT3	VCMT2	VCMT1	VCMT0	0	0	VCMR5	VCMR4	VCMR3	VCMR2	VCMR1	VCMR0
POR		0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0

Note: R1F command register will only be valid when nMTP = 0.

VCMR[5:0]: To set the VCM[5:0] when nMTP = "0" which is equal to programmed MTP register(MTPR) value XOR with VCMR. These bits amplify the V_{COMH} voltage 0.36 to 0.99 times the V_{LCD63} voltage.

VCM[5:0] = VCMR[5:0] xor MTPR[5:0]

VCMR5 xor MTPR5	VCMR4 xor MTPR4	VCMR3 xor MTPR3	VCMR2 xor MTPR2	VCMR1 xor MTPR1	VCMR0 xor MTPR0	V_{COMH}
0	0	0	0	0	0	VLCD63 x 0.36
0	0	0	0	0	1	VLCD63 x 0.37
			:			: Step = 0.01 :
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

VCMT[5:0]: in 8-color mode (CM=1), SSD2118 allows a negative offset to the final VCM[5:0] from the normal 16.7M/262k color mode (CM=0).

$$VCM[5:0]_{8\text{-}color} = (VCMR[5:0] \ xor \ MTPR[5:0]) - VCMT[5:0]$$

MTPR[5:0] are the MTP registers correspondingly

Please refer to MTP detail for further explanation.

Read GPI (R51h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	0	GPI3	GPI2	GPI1	GPI0	0	0	0	0	0	0	0	0
POR		0	0	0	0	User define				0	0	0	0	0	0	0	0

GPI3-0: When hardware pin GPIP is connected to VDDIO, GPI[3:0] pins are activated and able to be read by sending command R51h.

When hardware pin GPIP is connected to VSS, GPI[3:0] pins are deactivated and float.

10 EXTENDED COMMAND DESCRIPTION

Reminder – In order to activate extended command, user is required to send R28h-0006 prioir to the extended command in application. See below for further description on the R28h register.

VCOM MTP (R28h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	CCB3	CCB2	CCB1	CCB0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CCB3-0: Command Control Bit, the master control of the internal command decoder. This register provides function of software reset and MTP programming.

CCB3	CCB2	CCB1	CCB0	Usage
0	0	0	0	Release Reset or no action
0	1	0	1	Driver initialization
0	1	1	0	Enable extended test command/ Enable for MTP Programming (Refer to MTP programming on Page 46 for details)
1	0	1	0	Fire MTP (Refer to MTP programming on Page 46 for details)
1	1	1	0	Reset all command bits to default
All other setting				Reserved

Turn on VCIX2 (R29h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	1	0	0	0	0	0	0	0	1	VCIX2	0	0	0	0	0	0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R29h 0000h: All boosters are turned on.
R29h 80C0h: Only VCIX2 primary booster is turned on

SDO Read and Pump/Burntime (R2Bh) (POR = 0520h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	ENSDO	0	0	0	PUMPT1	PUMPT0	BURNT1	BURNT0	0	MSENSE1	MSENSE0	0	0	0	0	0
POR		0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0

ENSDO: Command to enable SDO output
When ENSDO = 0, disable SDO output
When ENSDO = 1, enable SDO output

MSENSE [1:0]: Sensing method of MTP
When MSENSE [1:0] = 10, Sense once only during the 3th frames
When MSENSE [1:0] = 01, Sense MTP value per 16 frames

PUMPT [1:0]: VGH pump up delay time for programming MTP

PUMPT1	PUMPT0	Number of pixel clock
0	0	8192
0	1	16384
1	0	24576
1	1	32768

BURNT [1:0]: Burn time for programming MTP

BURNT 1	BURNT 0	Number of pixel clock
0	0	262144
0	1	524288
1	0	786432
1	1	1048576

Total MTP Programming Time = 1/(Pixel Clock)*(Pumptime+Burntime)

e.g. Total MTP Programming Time = 1/(2MHz)*(32768+1048576) = 0.54s

VCOM charge sharing scheme (R2Ch) (POR = 888Dh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	1	0	VCOMSH	0	1	0	0	0	1	0	0	0	1	1	0	1
POR		1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	1

VCOMSH: Command to control VCOM charge sharing scheme.
When VCOMSH = 1, 2 phase charge sharing scheme is used
When VCOMSH = 0, 1 phase charge sharing scheme is used (POR)

Unregulated VCIX2 (R2Dh) (POR = 3F40h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	1	1	1	1	1	1	0	1	0	UNREG	0	0	0	0
POR		0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0

UNREG: When UNREG = “1”, VCIX2 primary booster is unregulated.
When UNREG = “0”, VCIX2 primary booster is regulated by **VRC[2:0]** register.

Enable MTP Read and FRC (R2Eh) (POR = B941h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	1	0	1	1	1	0	0	FFRC	0	1	ALTREAD	0	0	0	0	LFRC
POR		1	0	1	1	1	0	0	1	0	1	0	0	0	0	0	1

ALTREAD: Command to control SDO to output MTP status
Wen ALTREAD = 1, SDO will not output MTP status
When ALTREAD = 0, SDO will output MTP status

FFRC: When FFRC = 1, frame FRC is enabled
When FFRC = 0, frame FRC is disabled

LFRC: When LFRC = 1, line FRC is enabled
When LFRC = 0, line FRC is disabled

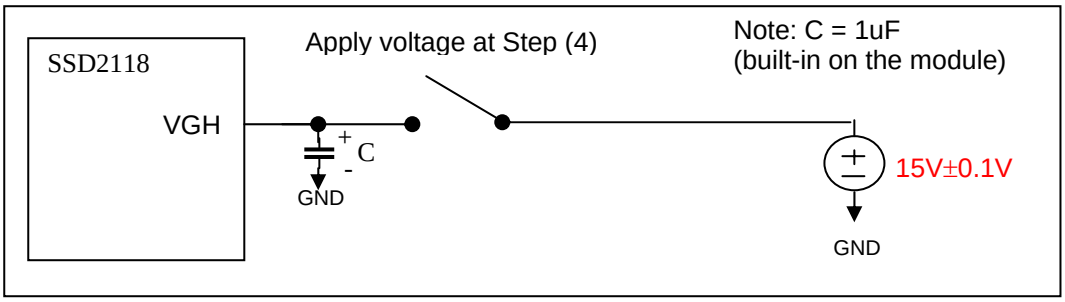
11 MTP PROGRAMMING

Remark: * The application setup should be synchronized.
Note1: nMTP must set to “0” to activate the MTP effect.
Note2: VCI is suggested to be larger than 3.3V during fire MTP.

Precaution:

1. All capacitors on MTP machine should be discharged completely before placing the LCD module.
2. The MTP programming voltage should not be applied when placing and removing the LCD module.
3. The MTP programming voltage should not be applied before VDDIO/VDDEXT/VCI.
4. After MTP is finished, the capacitors at VGH and VCIX2 must be discharged completely before removing the LCD module.
5. DOTCLK must be applied during MTP programming

Figure 11-1: MTP circuitry



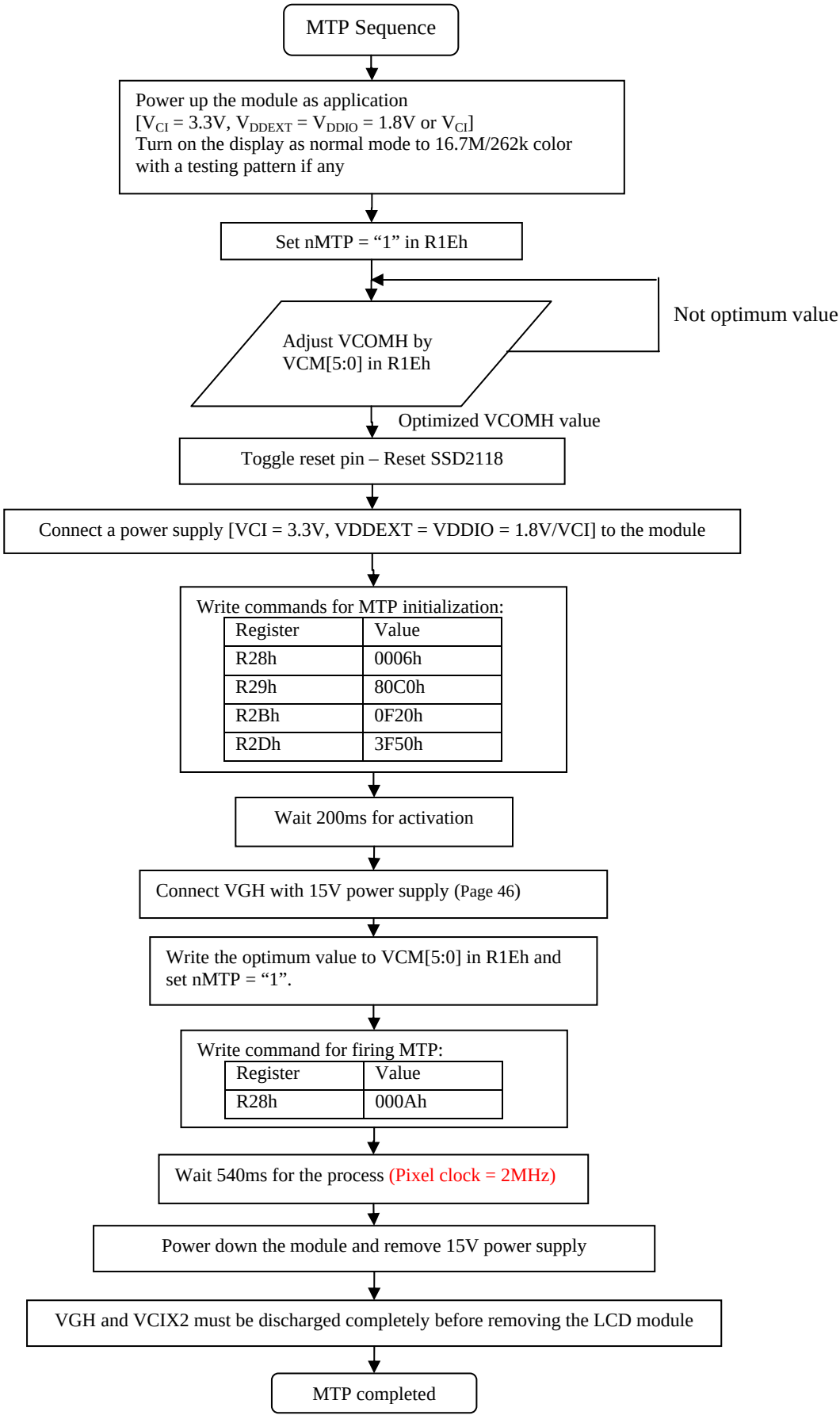
MTP Re-Write cycle

Table 11-1: MTP Re-write cycle

Characteristics	Symbol	Min	Typ	Max	Units
Re-write Cycle	N	-	-	5	Cycle
Power Supply voltage for programming	VGH	-	15	-	V
Power Supply voltage for erase	VGH	9	10	11	V
Program Pixel Clock	t_{PIXCLK}	1/(5MHz)	1/(2MHz)	1/(1MHz)	s
Program time	Tprog	0.22	0.54	1.08	s
Erase Pixel Clock	t_{PIXCLK}	-	1/(5MHz)	-	s
Erase time	Terase	-	1	-	s

Note: PUMPT [1:0] = 11 and BURNT [1:0] = 11

Figure 11-2: MTP Programming Flowchart



MTP Erase sequence

Remark: * The application setup should be synchronized.
Precaution:

1. All capacitors on MTP machine should be discharged completely before placing the LCD module.
2. The MTP erase voltage should not be applied when placing and removing the LCD module.
3. The MTP erase voltage should not be applied before $V_{DDIO}/V_{DDEXT}/V_{CI}$.
4. After Erasing MTP is finished, the capacitors at VGH and VCIX2 must be discharged completely before removing the LCD module.

Figure 11-3: MTP Erase circuitry

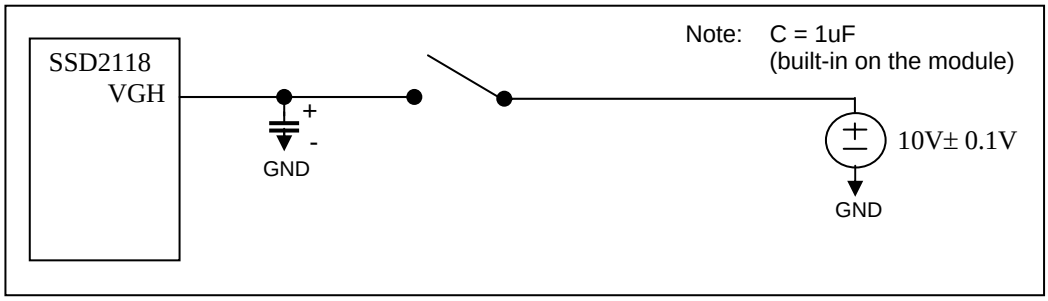
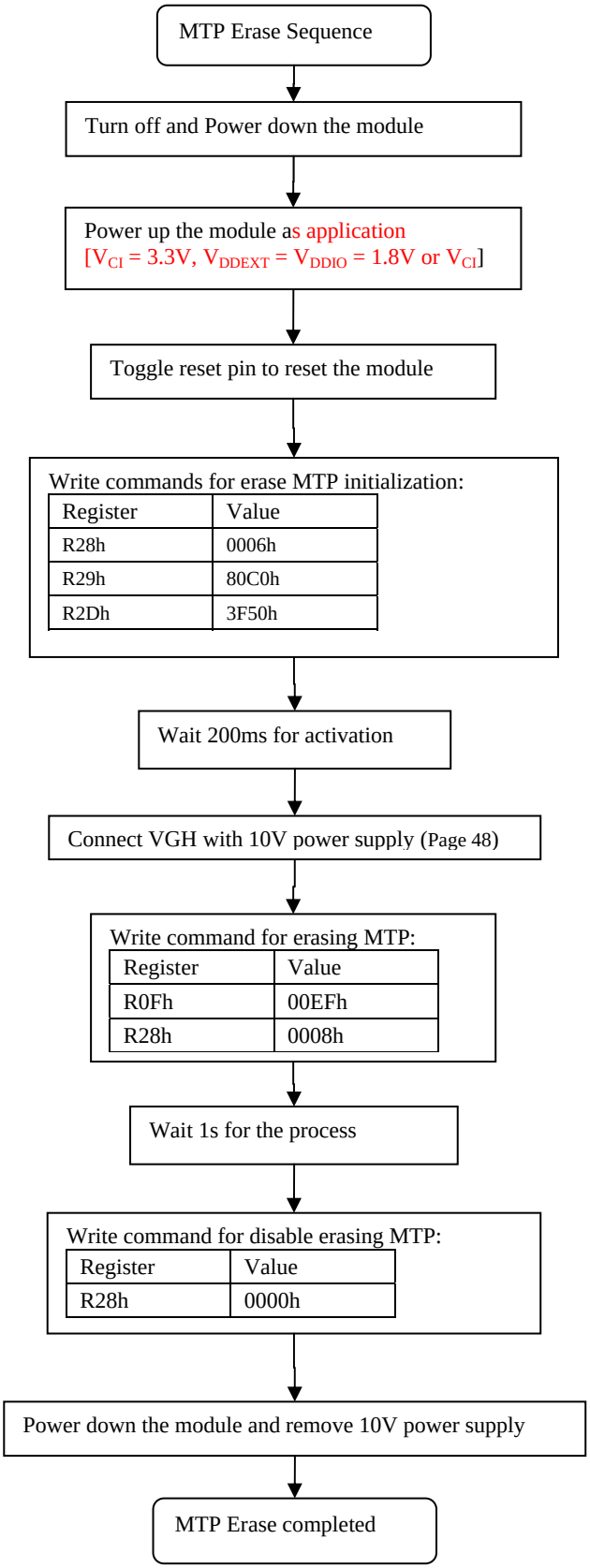


Figure 11-4: MTP Erase Flowchart



12 Gamma Adjustment Function

The SSD2118Z incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

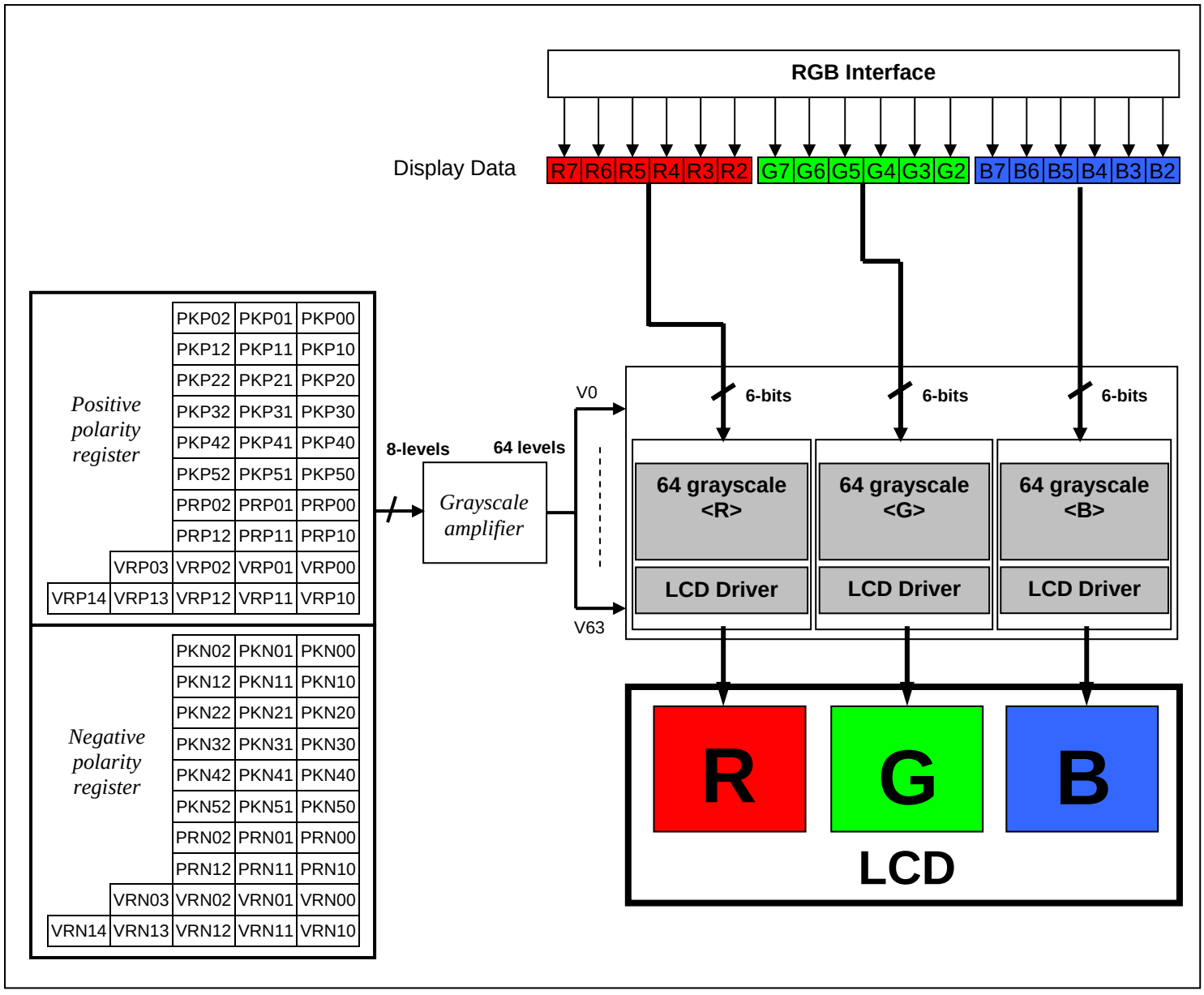


Figure 12-1 - Grayscale Control Block

12.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

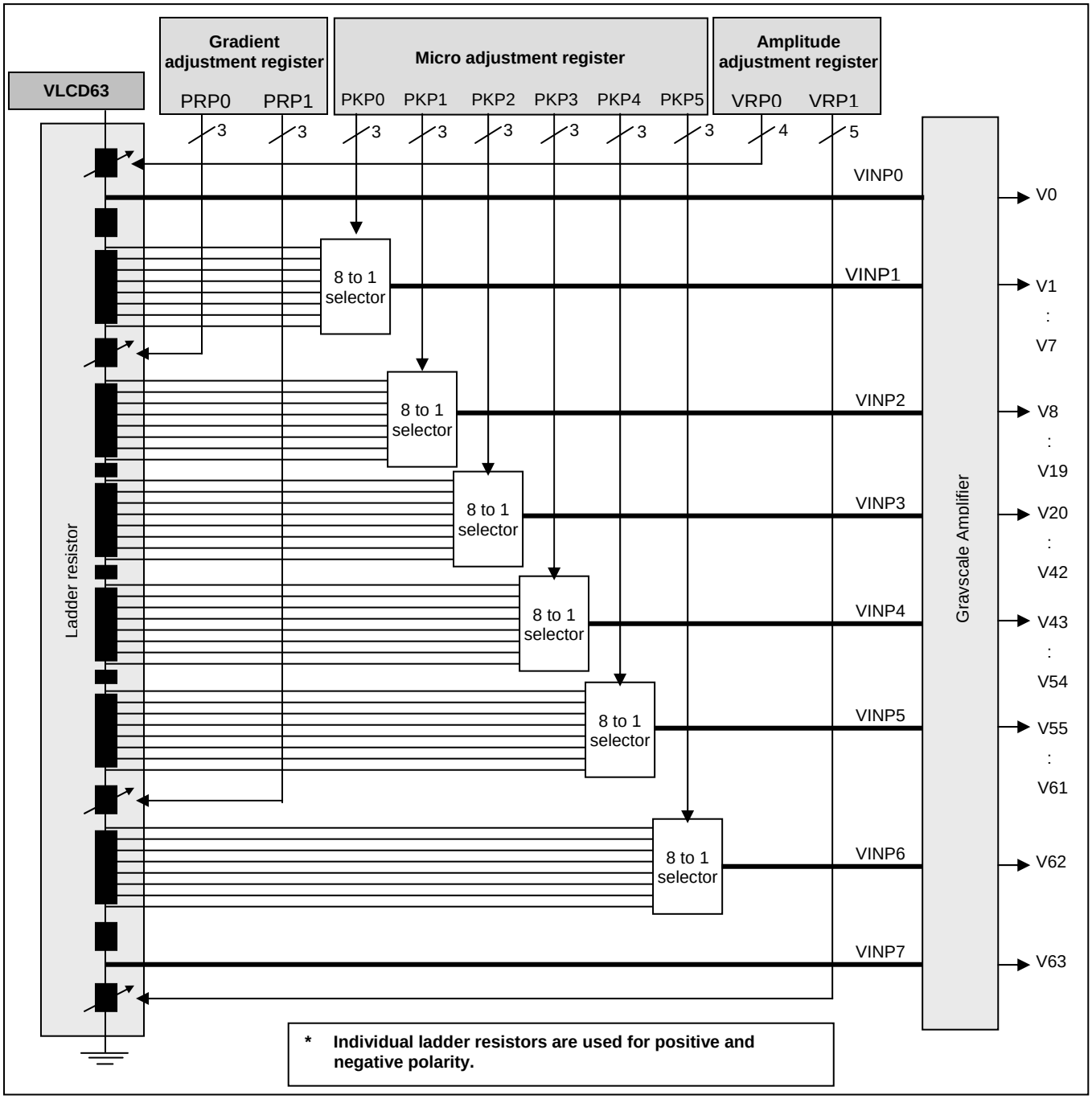


Figure 12-2 - Grayscale Amplifier

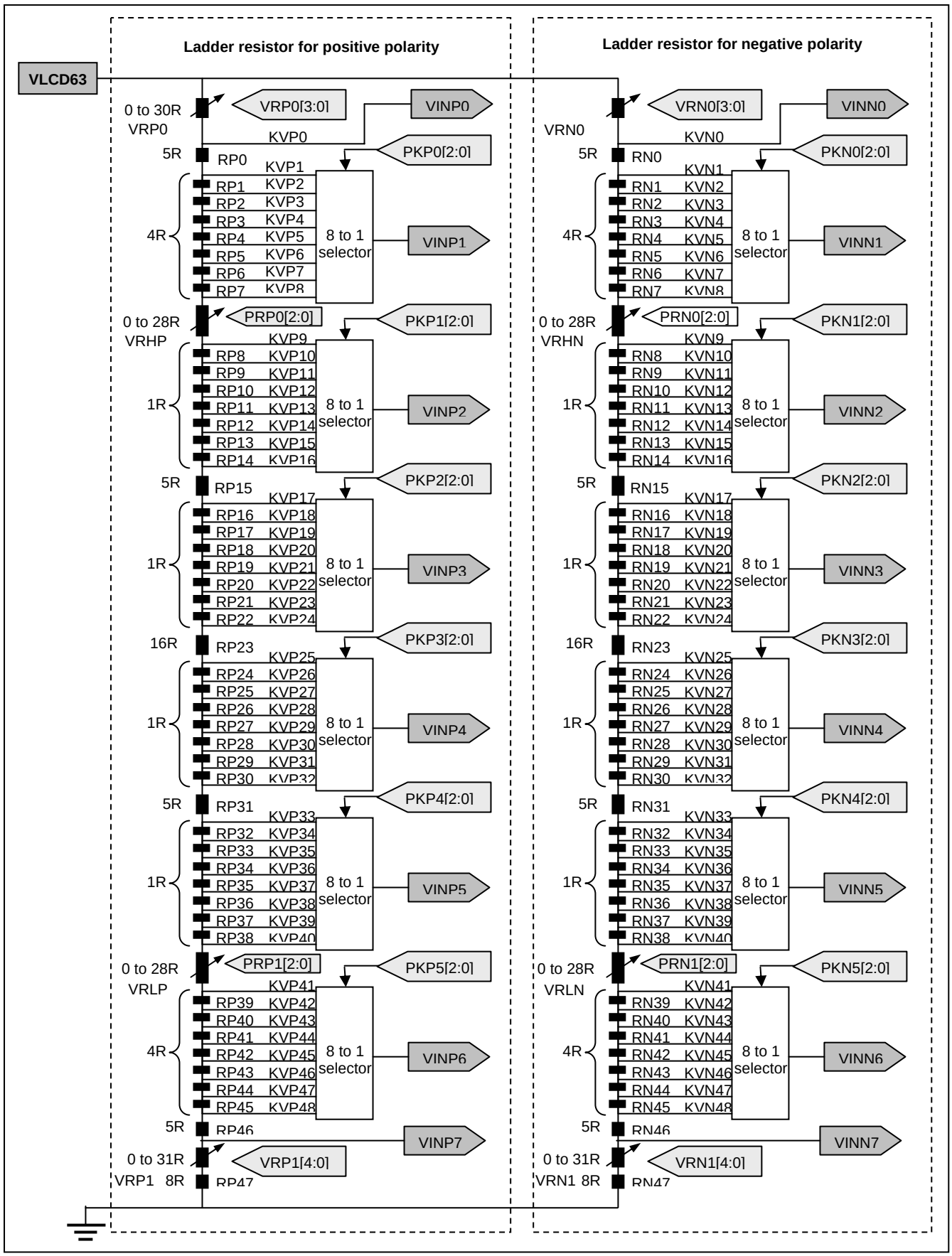


Figure 12-3- Resistor Ladder for Gamma Voltages Generation

12.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. R.G.B. grayscale voltage can be adjusted individually. Following graphics indicates the operation of each adjusting register.

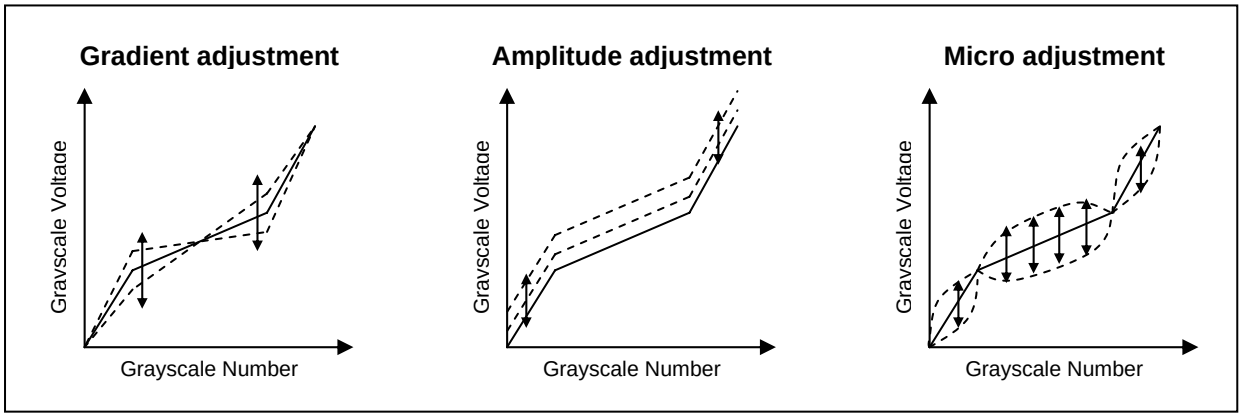


Figure 12-4 - Gamma Adjustment Function

1. Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

2. Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

3. Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

12.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step = 2R :	
1110	28R
1111	30R

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

8 to 1 selecter

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Positive polarity							Negative polarity						
Registor	Selected voltage						Registor	Selected voltage					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	PKN[2:0]	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table 12-1 - Grayscale Voltages Formulas

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V22	V43+(V20-V43)*(42/46)	V44	V55+(V43-V55)*(22/24)
V1	VINP(N)1	V23	V43+(V20-V43)*(40/46)	V45	V55+(V43-V55)*(20/24)
V2	V8+(V1-V8)*(30/48)	V24	V43+(V20-V43)*(38/46)	V46	V55+(V43-V55)*(18/24)
V3	V8+(V1-V8)*(23/48)	V25	V43+(V20-V43)*(36/46)	V47	V55+(V43-V55)*(16/24)
V4	V8+(V1-V8)*(16/48)	V26	V43+(V20-V43)*(34/46)	V48	V55+(V43-V55)*(14/24)
V5	V8+(V1-V8)*(12/48)	V27	V43+(V20-V43)*(32/46)	V49	V55+(V43-V55)*(12/24)
V6	V8+(V1-V8)*(8/48)	V28	V43+(V20-V43)*(30/46)	V50	V55+(V43-V55)*(10/24)
V7	V8+(V1-V8)*(4/48)	V29	V43+(V20-V43)*(28/46)	V51	V55+(V43-V55)*(8/24)
V8	VINP(N)2	V30	V43+(V20-V43)*(26/46)	V52	V55+(V43-V55)*(6/24)
V9	V20+(V8-V20)*(22/24)	V31	V43+(V20-V43)*(24/46)	V53	V55+(V43-V55)*(4/24)
V10	V20+(V8-V20)*(20/24)	V32	V43+(V20-V43)*(22/46)	V54	V55+(V43-V55)*(2/24)
V11	V20+(V8-V20)*(18/24)	V33	V43+(V20-V43)*(20/46)	V55	VINP(N)5
V12	V20+(V8-V20)*(16/24)	V34	V43+(V20-V43)*(18/46)	V56	V62+(V55-V62)*(44/48)
V13	V20+(V8-V20)*(14/24)	V35	V43+(V20-V43)*(16/46)	V57	V62+(V55-V62)*(40/48)
V14	V20+(V8-V20)*(12/24)	V36	V43+(V20-V43)*(14/46)	V58	V62+(V55-V62)*(36/48)
V15	V20+(V8-V20)*(10/24)	V37	V43+(V20-V43)*(12/46)	V59	V62+(V55-V62)*(32/48)
V16	V20+(V8-V20)*(8/24)	V38	V43+(V20-V43)*(10/46)	V60	V62+(V55-V62)*(25/48)
V17	V20+(V8-V20)*(6/24)	V39	V43+(V20-V43)*(8/46)	V61	V62+(V55-V62)*(18/48)
V18	V20+(V8-V20)*(4/24)	V40	V43+(V20-V43)*(6/46)	V62	VINP(N)6
V19	V20+(V8-V20)*(2/24)	V41	V43+(V20-V43)*(4/46)	V63	VINP(N)7
V20	VINP(N)3	V42	V43+(V20-V43)*(2/46)		
V21	V43+(V20-V43)*(44/46)	V43	VINP(N)4		

Table 12-2 - Reference Voltages of Positive Polarity

Reference	Formula	Micr0-adjusting register	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	--	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	VLCD63 - ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1

ΔV: Voltage difference between VLCD63 and of VSS.

Table 12-3 - Reference Voltages of Negative Polarity:

Reference	Formula	Micr0-adjusting register	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	--	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = “001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = “010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = “011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = “100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = “101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = “110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = “111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = “001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = “010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = “011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = “100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = “101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = “110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = “111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = “001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = “010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = “011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = “100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = “101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = “110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = “111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = “001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = “010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = “011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = “100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = “101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = “110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = “111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = “001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = “010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = “011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = “100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = “101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = “110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = “111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “001”	
KVN43	VLCD63 - (V x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “010”	
KVN44	VLCD63 - (V x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “011”	
KVN45	VLCD63 - (V x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “100”	
KVN46	VLCD63 - (V x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “101”	
KVN47	VLCD63 - (V x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “110”	
KVN48	VLCD63 - (V x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “111”	
KVN49	VLCD63 - (V x (VRN0 + 120R + VRHN + VRLN) / SUMRN	--	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1

ΔV: Voltage difference between VLCD63 and of VSS.

13 MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{CORE}	Supply voltage for logic	-0.3 to +2.0	V
V_{DDIO}	Supply Voltage for I/O	-0.3 to +4.0	V
V_{CI}	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{CORE} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that analog voltages should be constrained to the range $V_{GL} < V_{SS} < V_{DDIO} \leq V_{CI} < V_{GH}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

14 DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, T_A = -40 to 85°C)

V_{DDEXT}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.6	-	3.6	V
V_{DDIO}	Power supply pin of I/O pins	Recommend Operating Voltage Possible Operating Voltage	1.6	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	2.5 or V_{DDIO}	-	3.6	V
$I_{sleep}1$	Sleep mode current (VCI pin)	VDDEXT=VDDIO=1.8V, VCI=3.3V	-	2	50	uA
$I_{sleep}2$	Sleep mode current (VDDEXT+VDDIO)		-	1	50	uA
I_{dp}	Operating mode current	100pF loading at Source output VDDEXT=VDDIO=1.8V, VCI=3.3V $I_{DP} = I_{VDDIO} + I_{VDDEXT} + I_{VCI}$	-	6.5	13	mA
V_{CIM}	Negative V_{CI} Output Voltage	No panel loading	$-V_{CI}$	-	-	V
V_{CIX2}	V_{CIX2} primary booster efficiency[1]	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	90	95	-	%
			-	-	6.1	V
V_{GH}	Gate driver High Output Voltage Booster efficiency[2]	No panel loading; 4x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	84	89.5	-	%
		No panel loading; 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	80	88.5	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	72	80	-	%
V_{GL}	Gate driver Low Output Voltage		$-V_{GH}$	-	$-V_{CIx2}$	V
V_{COMH}	VCOM High Output Voltage		VCI	-	99% x VLCD63	V
V_{COML}	VCOM Low Output Voltage		V_{CIM}+0.5	-	-	V
V_{COMA}	VCOM Amplitude V_{COMH} - V_{COML}		-	-	6.0 or VCIX2-0.1	V
V_{LCD63}	V_{LCD63} Output Voltage[3]		-	-	6.0 or VCIX2-0.1	V
ΔV_{LCD63}	Max. Source Voltage Variation		-2	-	2	%
VOH1	Logic High Output Voltage	Iout=-100uA	0.9 * V_{DDIO}	-	V_{DDIO}	V
VOL1	Logic Low Output Voltage	Iout=100uA	0	-	0.1 * V_{DDIO}	V
VIH1	Logic High Input voltage		0.8 * V_{DDIO}	-	V_{DDIO}	V
VIL1	Logic Low Input voltage		0	-	0.2 * V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V_{OH} = V_{DDIO}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	V_{OL} = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
TC	Temperature Coefficient		-	0.015	-	%

Note1: **V_{CIX2} efficiency = V_{CIX2} /(2 x V_{CI}) x 100%**
Note2: **V_{GH} efficiency = V_{GH}/(V_{CI} x n) x 100%** **(where n = booster factor)**
Note3: **VCIX2 – VLCD63 ≥ 0.1V**

15 AC CHARACTERISTICS

AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 1.8V, T_A = -40 to 85°C)

15.1 Display General Information

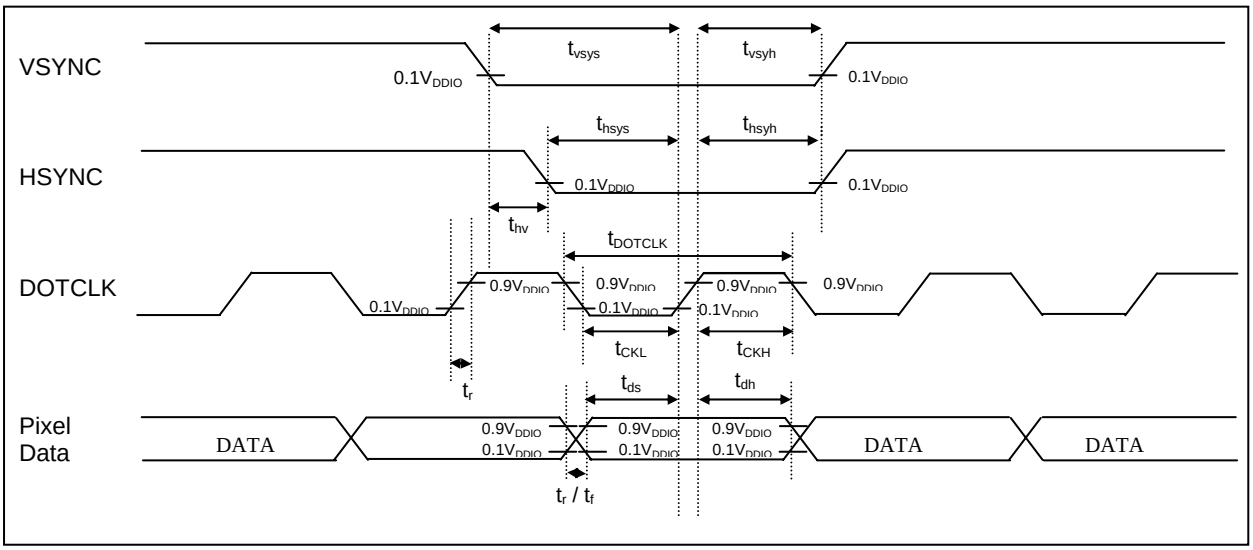


Figure 15-1- Pixel Clock Timing

Characteristics		Symbol	Target Min	Target Typ	Target Max	Units
DOTCLK Frequency	18/24 bits parallel	f_{DOTCLK}	-	5	8	MHz
	6/8 bits serial without dummy		-	15	24	
	6/8 bits serial with dummy		-	20	32	
DOTCLK Period	18/24 bits parallel	t_{DOTCLK}	125	200	-	nSec
	6/8 bits serial without dummy		42	67	-	
	6/8 bits serial with dummy		31	50	-	
Pixel Clock Period	18/24 bits parallel	t_{PIXCLK}	-	1	-	t_{DOTCLK}
	6/8 bits serial without dummy		-	3	-	
	6/8 bits serial with dummy		-	4	-	
Pixel Clock Freq.	18/24 bits parallel	f_{PIXCLK}	-	5	8	MHz
	6/8 bits serial without dummy					
	6/8 bits serial with dummy					
Vertical Sync Setup Time		t_{vsys}	5	-	-	nSec
Vertical Sync Hold Time		t_{vsyh}	5	-	-	nSec
Horizontal Sync Setup Time		t_{hsys}	5	-	-	nSec
Horizontal Sync Hold Time		t_{hsyh}	5	-	-	nSec
Phase difference of Sync Signal Falling Edge		t_{hv}	0	-	320	t_{DOTCLK}
DOTCLK Low Period		t_{CKL}	16	-	-	nSec
DOTCLK High Period		t_{CKH}	16	-	-	nSec
Data Setup Time		t_{ds}	10	-	-	nSec
Data hold Time		t_{dh}	10	-	-	nSec
Reset pulse width		t_{RES}	2.5	-	-	uSec
Rise / Fall time		t_r / t_f	5	-	25	nSec

Note: External clock source must be provided to DOTCLK pin of SSD2118Z. The driver will not operate if absent of the clocking signal.

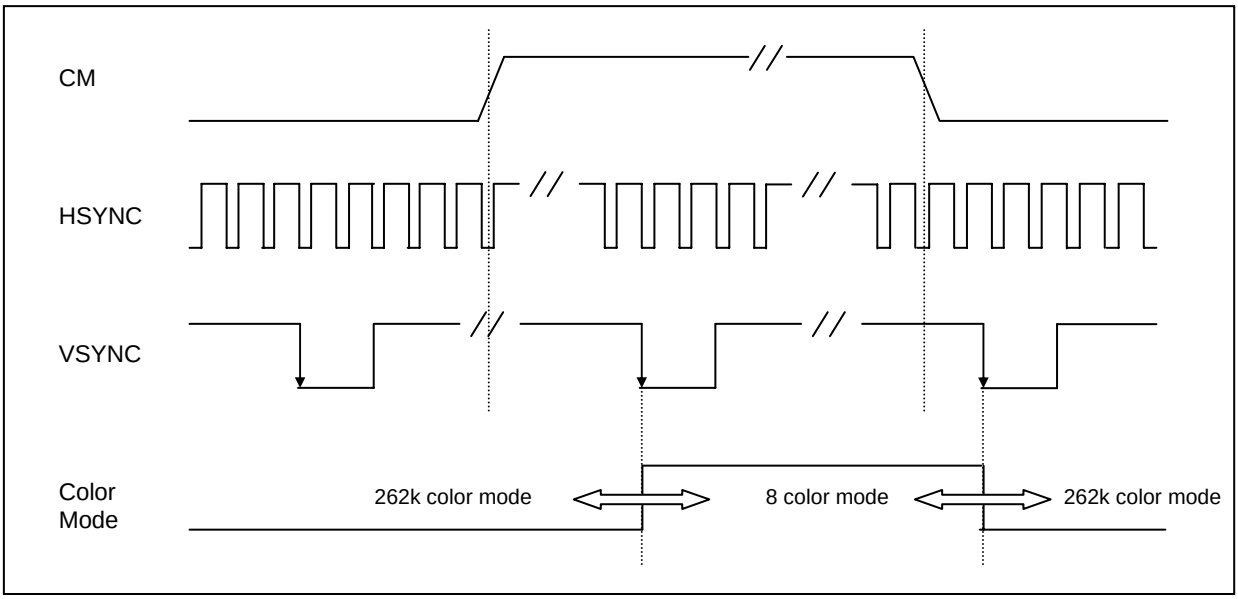


Figure 15-2 Color Mode Conversion Timing

Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

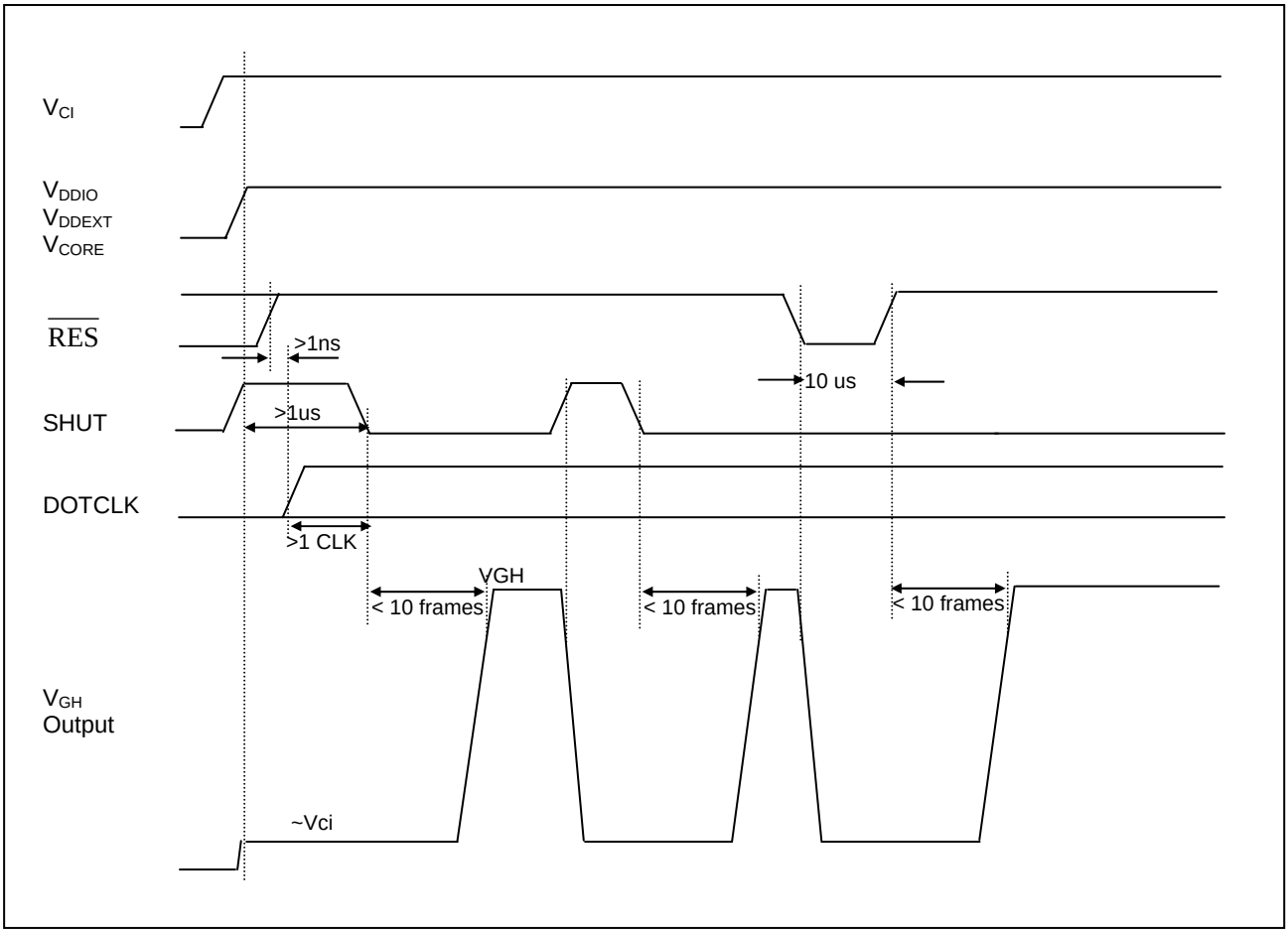


Figure 15-3 VGH Output against SHUT & RESB

Note1: **The minimum cycle time of SHUT is 10 + 2 frames.**

Note2: **DOTCLK must be provided for boosting of V_{GH}. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.**

Note3: **V_{GH} will be forced to V_{CI} at the low stage of $\overline{RES}$.**

Note4: **The minimum pulse width of RESET is 10us.**

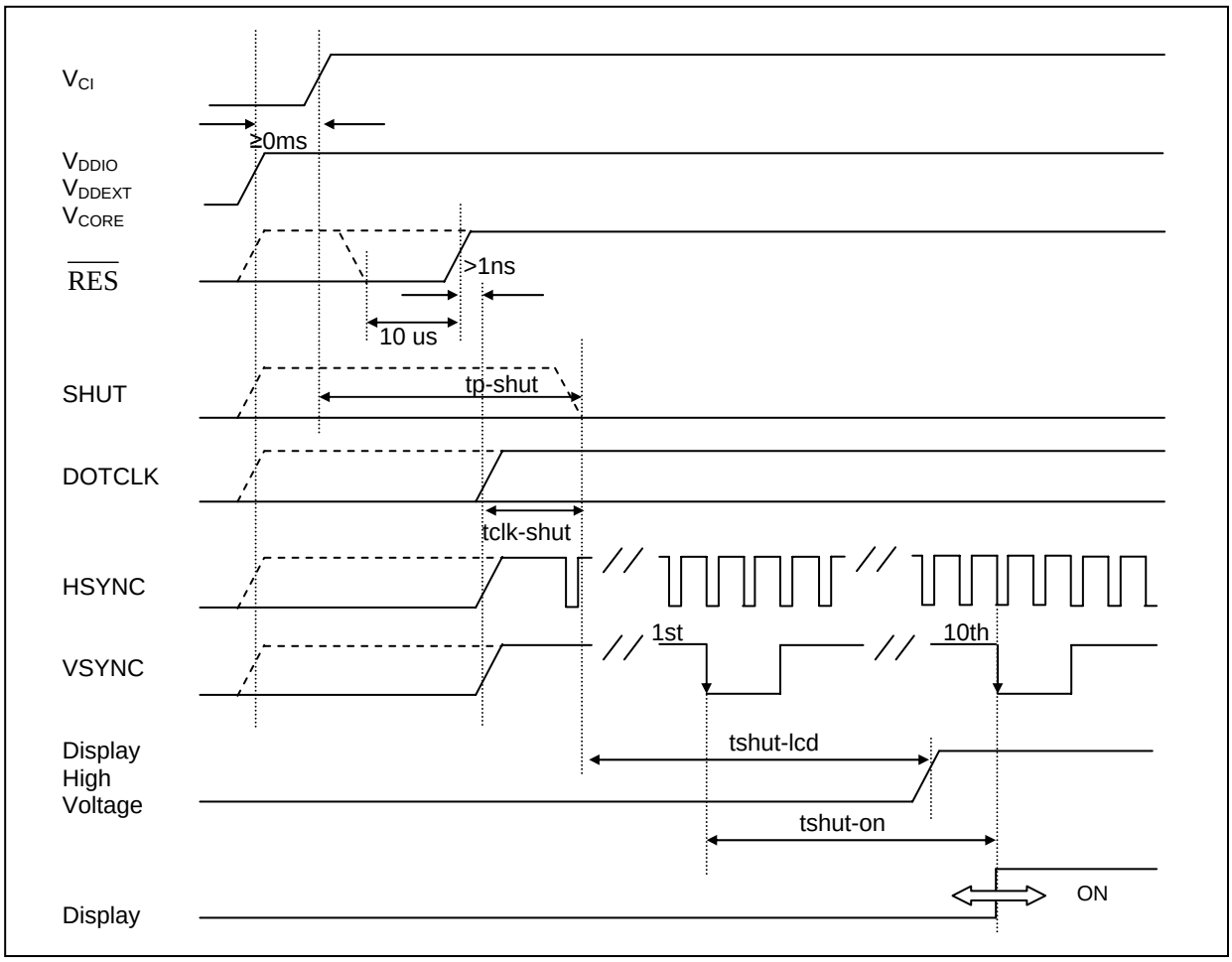


Figure 15-4 - Power Up Sequence

Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
V_{DDEXT} / V_{DDIO} on to falling edge of SHUT	tp-shut	1	-	-	µsec
Start of DOTCLK to SHUT low	tclk-shut	1	-	-	DOTCLK
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	164	msec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 336 clk -- 1 frame: 244 line -- PIXCLK = 5.0MHz		-	164	-	msec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

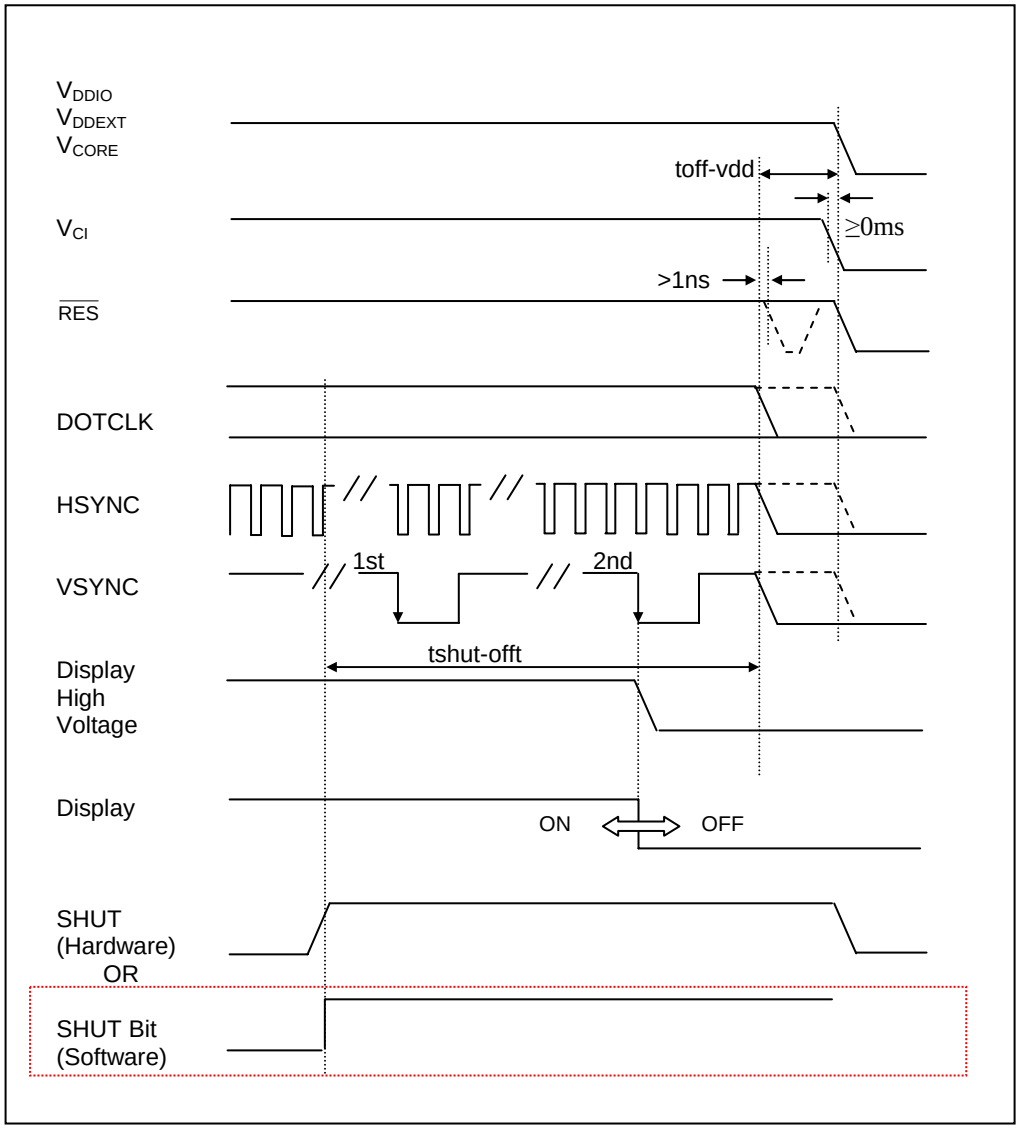


Figure 15-5 - Power Down Sequence

Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
Rising edge of SHUT to display off -- 1 line: 336 clk -- 1 frame: 244 line -- PIXCLK = 5.0 MHz	tshut-off	2	-	-	frame
		32.8	-	-	msec
Input-signal-off to V_{DDEXT} / V_{DDIO} off	toff-vdd	1	-	-	µsec

Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

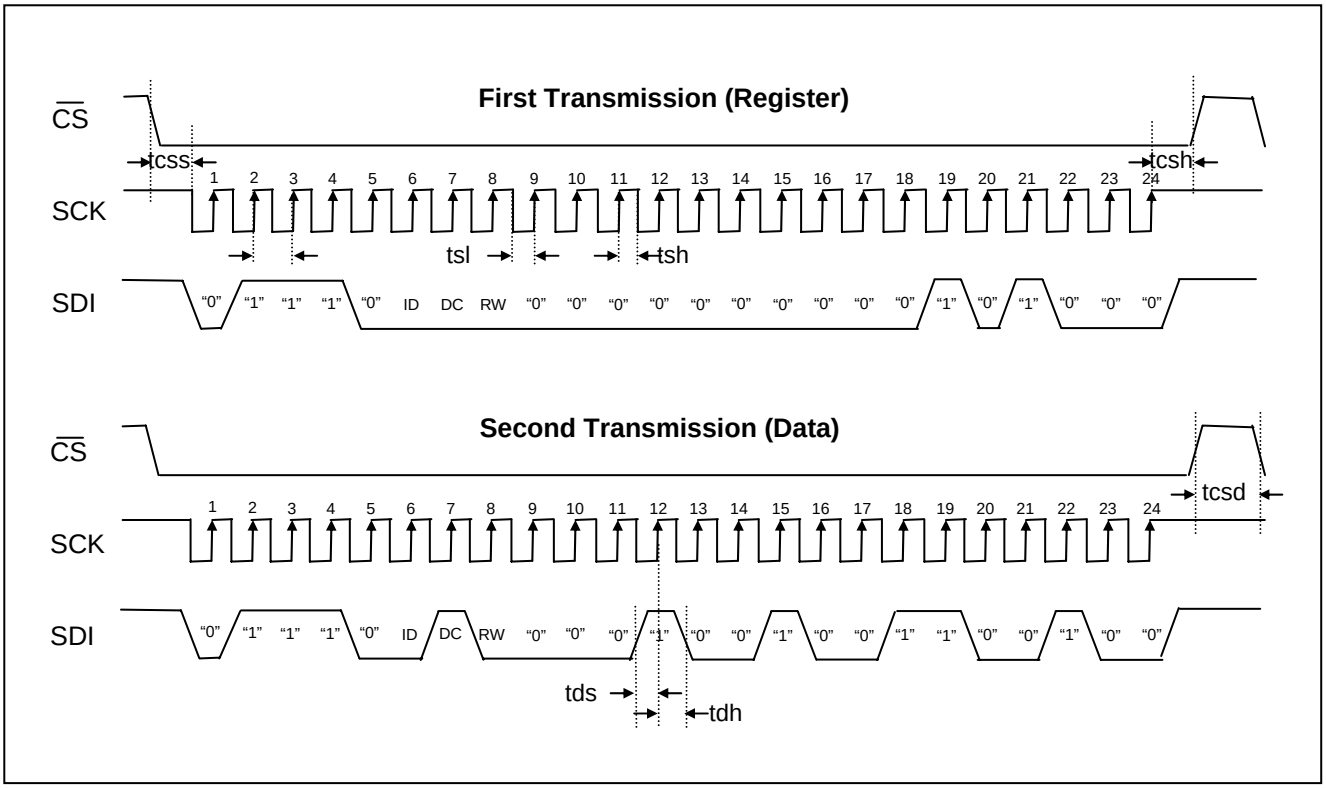


Figure 15-6 - SPI Interface Timing Diagram & Transaction Example

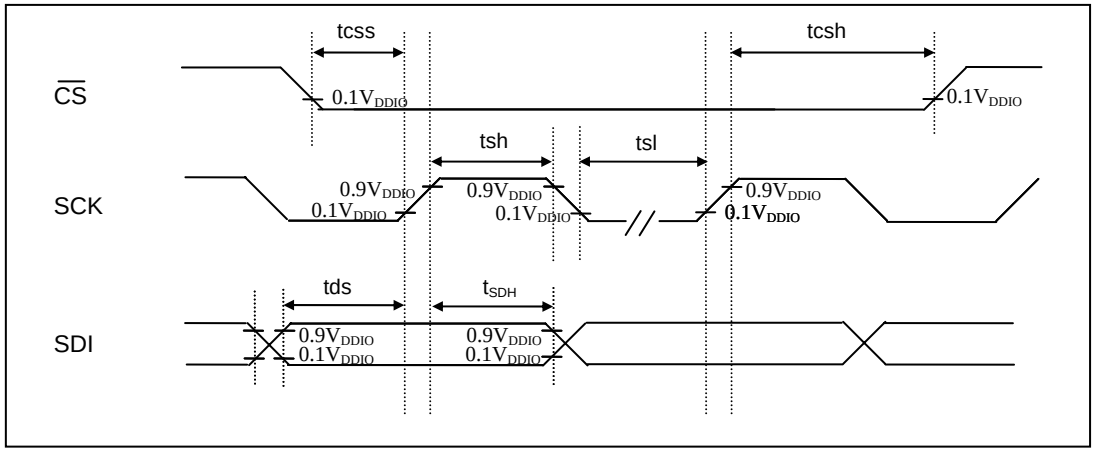


Figure 15-7 - SPI Interface Timing Diagram

Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock High Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	0	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	20	-	-	nsec
Data Setup Time	tds	5	-	-	nsec
Data Hold Time	tdh	10	-	-	nsec

Note1: SPID pin connected to VSS.

15.2 8-bit Serial Interface

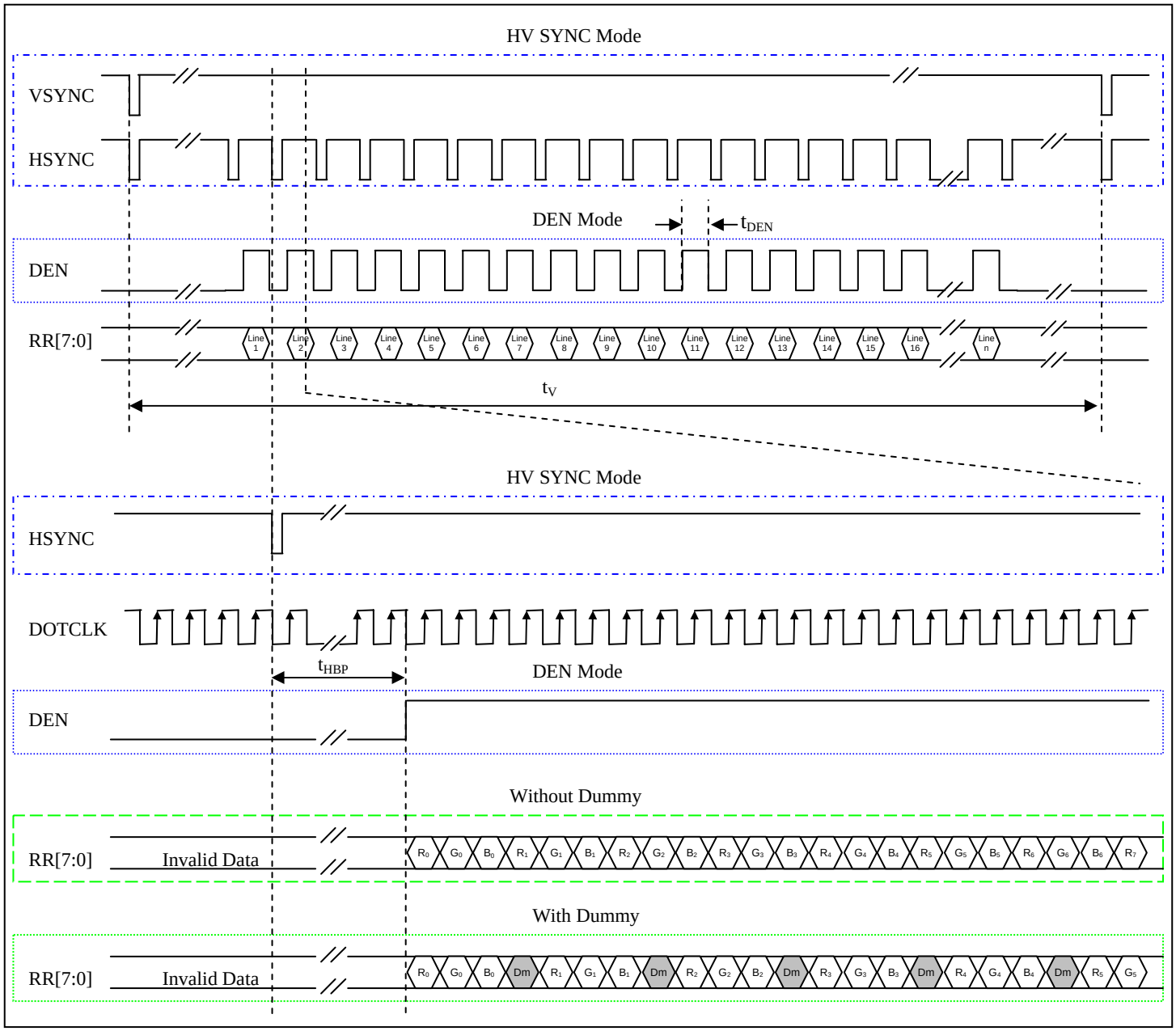


Figure 15-8 – 8-bit Serial Interface Timing Diagram & Transaction Example

Characteristics		Symbol	HV SYNC Mode Without Dummy	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	15.00	MHz
Horizontal	One Line Period	t_H	1008	t_{DOTCLK}
	Active Data Period	t_{data}	960	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	24	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	24	t_{DOTCLK}
Vertical	One Field Period	t_V	244	t_H
	Active Line period	t_{AL}	240	t_H
	Vertical Back Porch	t_{VBP}	2	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

Characteristics		Symbol	HV SYNC Mode With Dummy	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	20	MHz
Horizontal	One Line Period	t_H	1328	t_{DOTCLK}
	Active Data Period	t_{data}	1280	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	32	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	32	t_{DOTCLK}
Vertical	One Field Period	t_V	244	t_H
	Active Line period	t_{AL}	240	t_H
	Vertical Back Porch	t_{VBP}	2	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

Characteristics		Symbol	DEN Mode Without Dummy	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	15	MHz
Horizontal	One Line Period	t_H	1008	t_{DOTCLK}
	Active Data Period	t_{data}	960	t_{DOTCLK}
	Data Enable Period	t_{DEN}	960	t_{DOTCLK}
Vertical	One Field Period	t_V	244	t_H
	Active Line period	t_{AL}	240	t_H

Characteristics		Symbol	DEN Mode With Dummy	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	20	MHz
Horizontal	One Line Period	t_H	1328	t_{DOTCLK}
	Active Data Period	t_{data}	1280	t_{DOTCLK}
	Data Enable Period	t_{DEN}	1280	t_{DOTCLK}
Vertical	One Field Period	t_V	244	t_H
	Active Line period	t_{AL}	240	t_H

15.3 24-bit RGB Interface

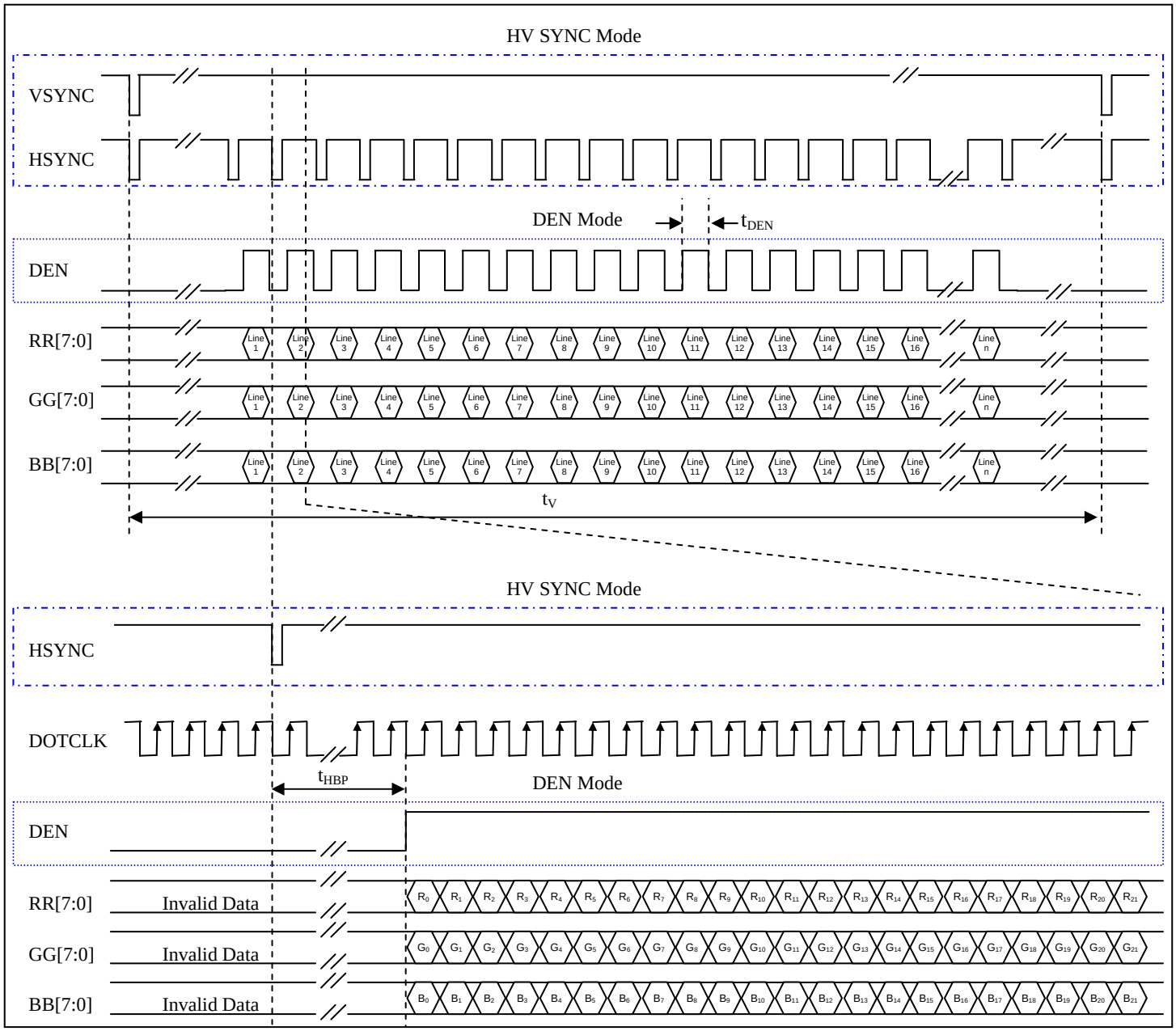


Figure 15-9 – 24-bit RGB Interface Timing Diagram & Transaction Example

Characteristics		Symbol	HV SYNC Mode	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	5	MHz
Horizontal	One Line Period	t_H	336	t_{DOTCLK}
	Active Data Period	t_{data}	320	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	8	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	8	t_{DOTCLK}
Vertical	One Field Period	t_V	244	t_H
	Active Line period	t_{AL}	240	t_H
	Vertical Back Porch	t_{VBP}	2	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

Characteristics		Symbol	DEN Mode	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	5	MHz
Horizontal	One Line Period	t_H	336	t_{DOTCLK}
	Active Data Period	t_{data}	320	t_{DOTCLK}
	Data Enable Period	t_{DEN}	320	t_{DOTCLK}
Vertical	One Field Period	t_V	244	t_H
	Active Line period	t_{AL}	240	t_H

16 ITO RESISTANCE REQUIREMENT

Pin	Suggested maximum resistance
V_{COM}, EXVR, V_{CHS}, CYP, CYN, V_{CIX2}, V_{CIX2J}, V_{CIX2G}, $V_{CI,}$ V_{CIP}, HC	10 ohm
V_{SS}, AV_{SS}, $V_{SSRC,}$	10 ohm
V_{CORE}, V_{REGC} , V_{DDEXT}, $V_{CIM,}$ V_{DDIO}	20 ohm
CDUM0, CSVCMP, CSVCMN	20 ohm
C1N, C1P, C2N, C2P, C3P, C3N, CXP, CXN, V_{GH}, $V_{GL,}$ $V_{LCD63,}$ $V_{COMR,}$ $V_{COMH,}$ V_{COML}	20 ohm
TESTA, TESTB, TEST3, TEST4	100 ohm
DOTCLK, RR[7:0], BB[7:0], GG[7:0], VSYNC, HSYNC	50 ohm
BGR, CM, RL, REGVDD, RESB, REV, SPID, TB, STYPE1, STYPE0, SHUT, GPI0, GPI1, GPI2, GPI3, MOD, CF0, CF1, FB, GPIP, IF0, IF1, GAMAS1, GAMAS0	100 ohm
SDO, SDC, CSB, SDI, SCK, DEN, DRV	100 ohm

Note: ITO resistance and capacitance of DOTCLK, RR[7:0], BB[7:0], GG[7:0], VSYNC, HSYNC is suggested to be the same to prevent mismatch

17 INTERFACE MAPPING

17.1 Mapping for Writing an Instruction

		Hardware pins																					
Interface	**Cycle**	**BB7**	**BB6**	**BB5**	**BB4**	**BB3**	**BB2**	**BB1**	**BB0**	**GG7**	**GG6**	**GG5**	**GG4**	**GG3**	**GG2**	**GG1**	**GG0**	**RR7**	**RR6**	**RR5**	**RR4**	**RR3**	**RR2**	**RR1**	**RR0**
24 bits		IB23	IB22	IB21	IB20	IB19	IB18	IB17	IB16	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
8 bits	1st																	IB23	IB22	IB21	IB20	IB19	IB18	IB17	IB16
	2nd																	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8
	3rd																	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

Remark : Not connected pins

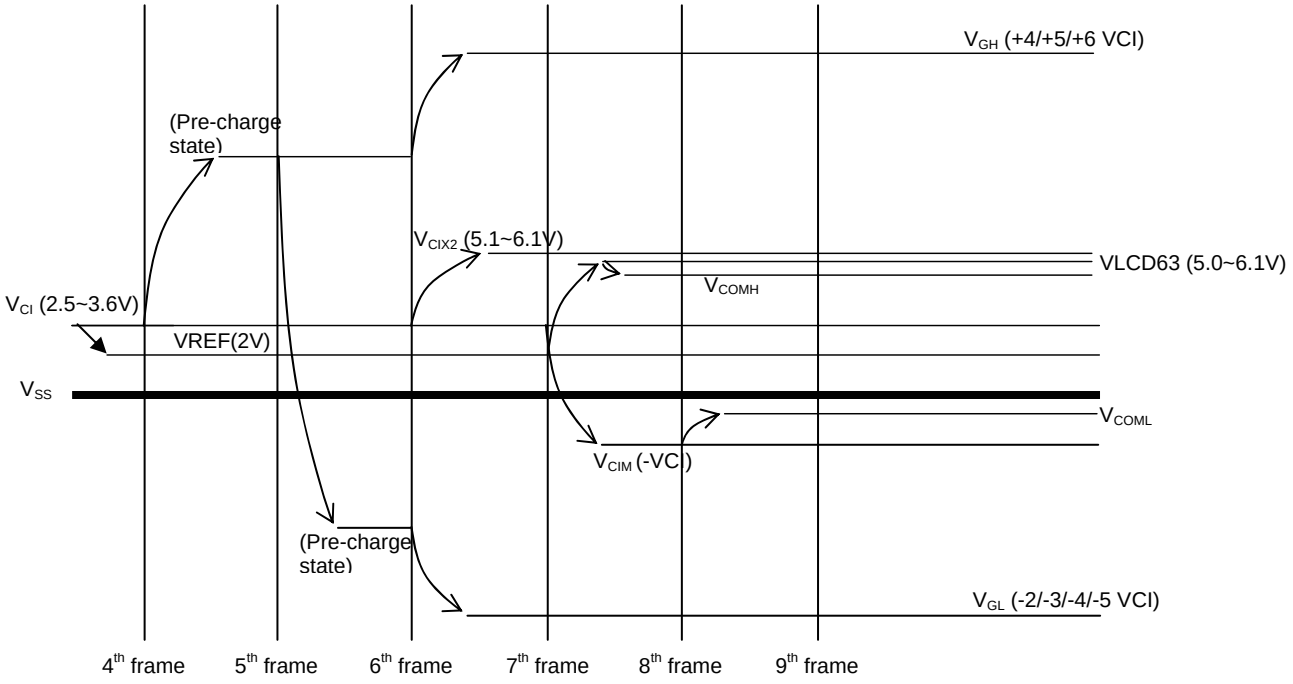
17.2 Mapping for Writing Pixel Data(s)

			Hardware pins																						
Interface	**Color mode**	**Cycle**	**BB7**	**BB6**	**BB5**	**BB4**	**BB3**	**BB2**	**BB1**	**BB0**	**GG7**	**GG6**	**GG5**	**GG4**	**GG3**	**GG2**	**GG1**	**GG0**	**RR7**	**RR6**	**RR5**	**RR4**	**RR3**	**RR2**	**RR1**	**RR0**
Parallel	16.7M		B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0
	262k		B7	B6	B5	B4	B3	B2	x	x	G7	G6	G5	G4	G3	G2	x	x	R7	R6	R5	R4	R3	R2	x	x
	8 color		B7	x	x	x	x	x	x	x	G7	x	x	x	x	x	x	x	R7	x	x	x	x	x	x	x
Serial	16.7M	1st																	R7	R6	R5	R4	R3	R2	R1	R0
		2nd																	G7	G6	G5	G4	G3	G2	G1	G0
		3rd																	B7	B6	B5	B4	B3	B2	B1	B0
	262k	1st																	R7	R6	R5	R4	R3	R2	x	x
		2nd																	G7	G6	G5	G4	G3	G2	x	x
		3rd																	B7	B6	B5	B4	B3	B2	x	x
	8 color	1st																	R7	x	x	x	x	x	x	x
		2nd																	G7	x	x	x	x	x	x	x
		3rd																	B7	x	x	x	x	x	x	x

Remark: Not connected pins
x Don't care

18 SSD2118Z OUTPUT VOLTAGE RELATIONSHIP

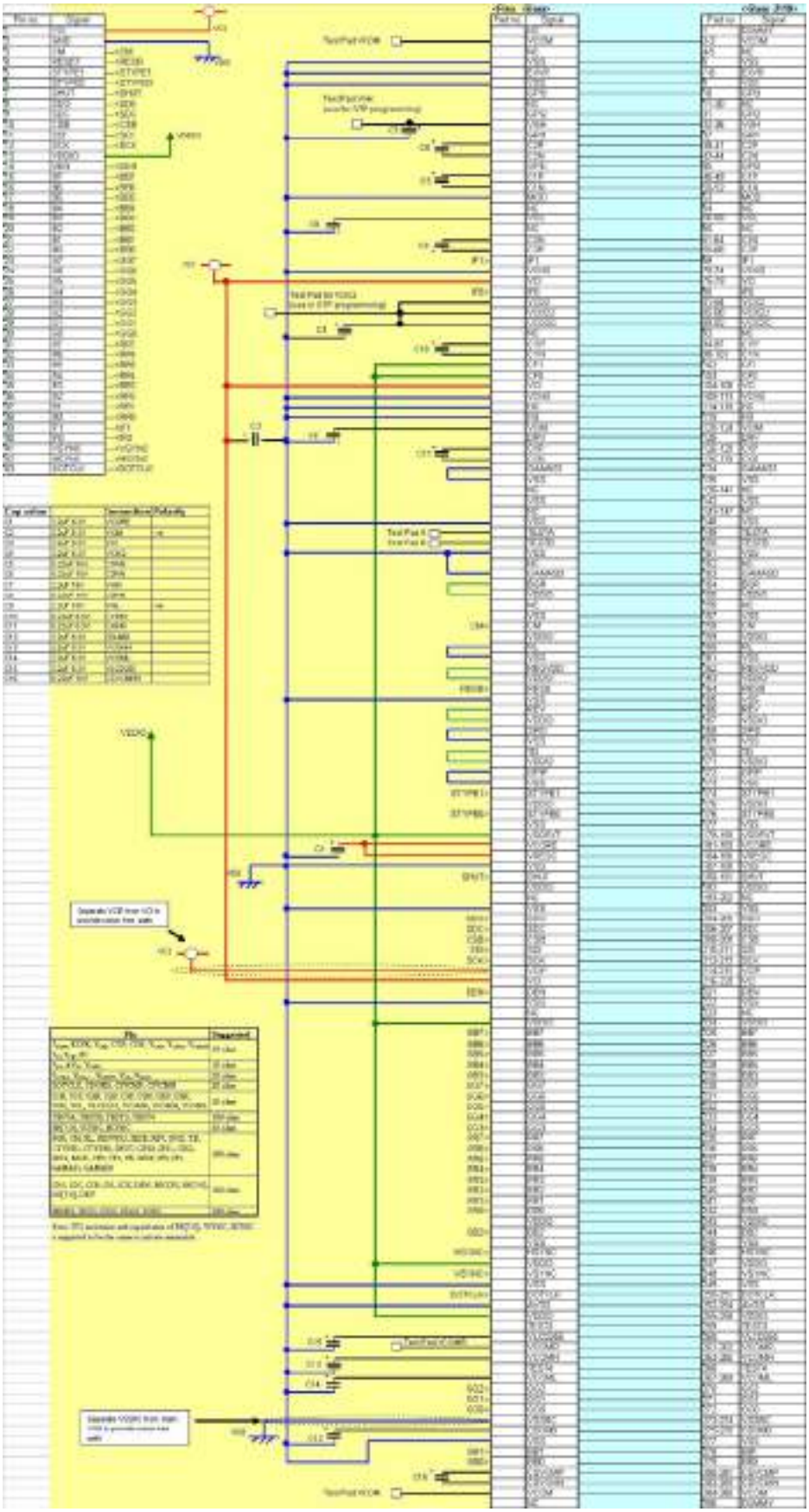
Figure 18-1- LCD Driving Voltage Relationship



Note: **The above voltages level assumed 100% efficiency of the internal booster. There has no voltage drop due to resistance from ITO trace of the panel.**

19 APPLICATION CIRCUIT

Figure 19-1 - Application Diagram



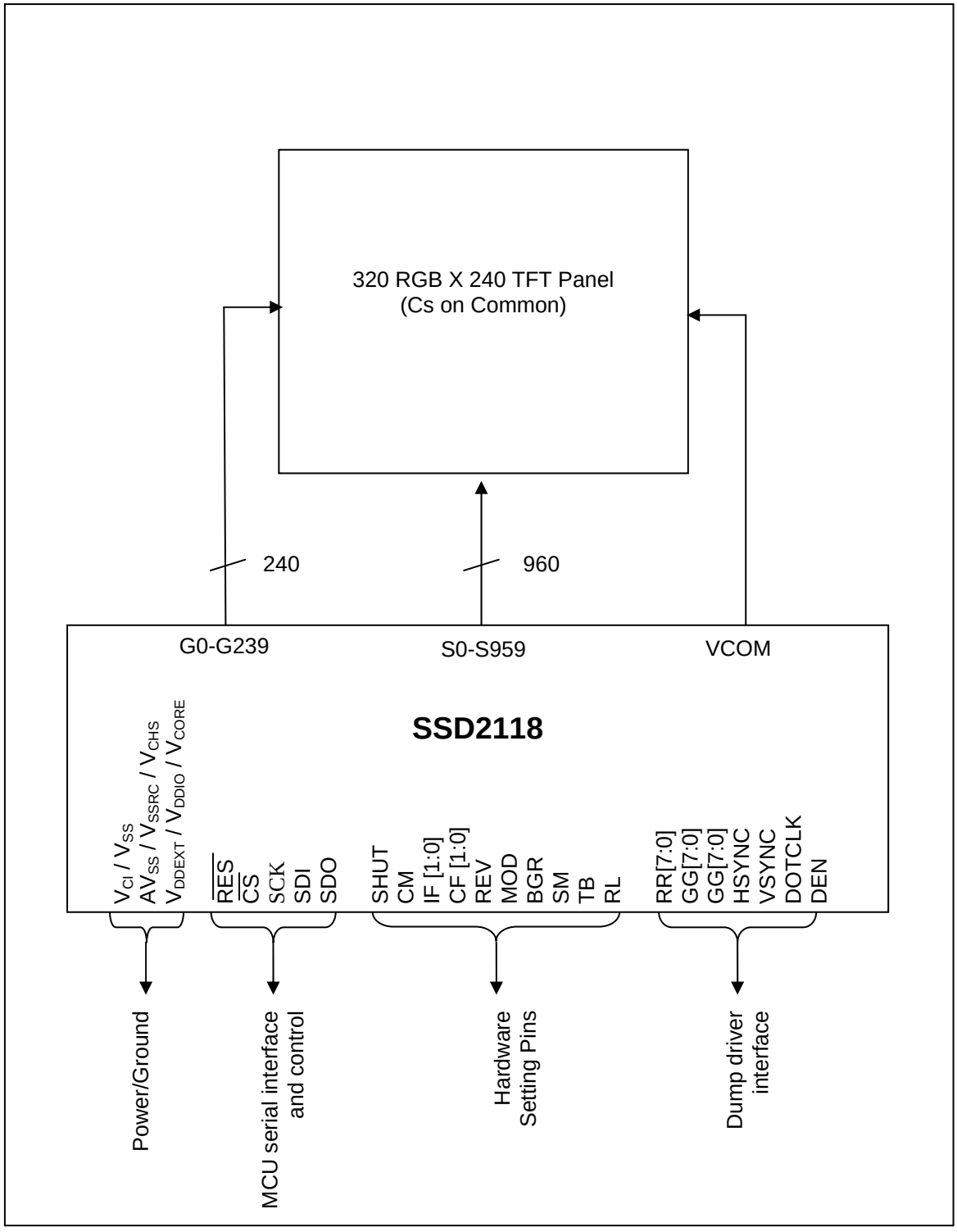
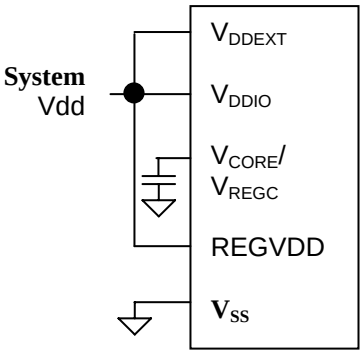


Figure 19-2 - Panel Connection Example

Figure 19-3 - Power Supply Pins Connections

3.6V ≥ System Vdd > 1.6V



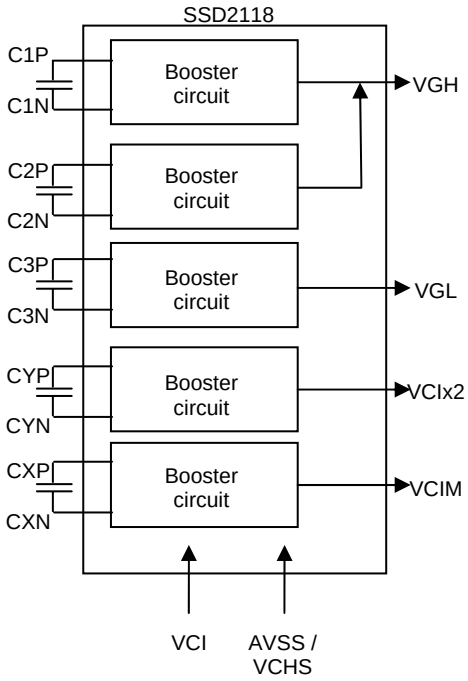
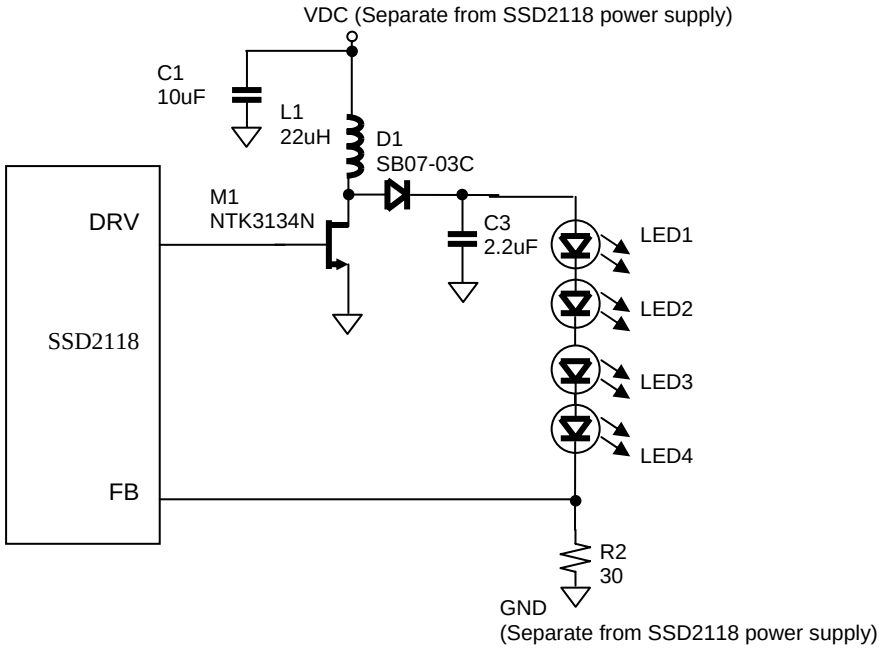


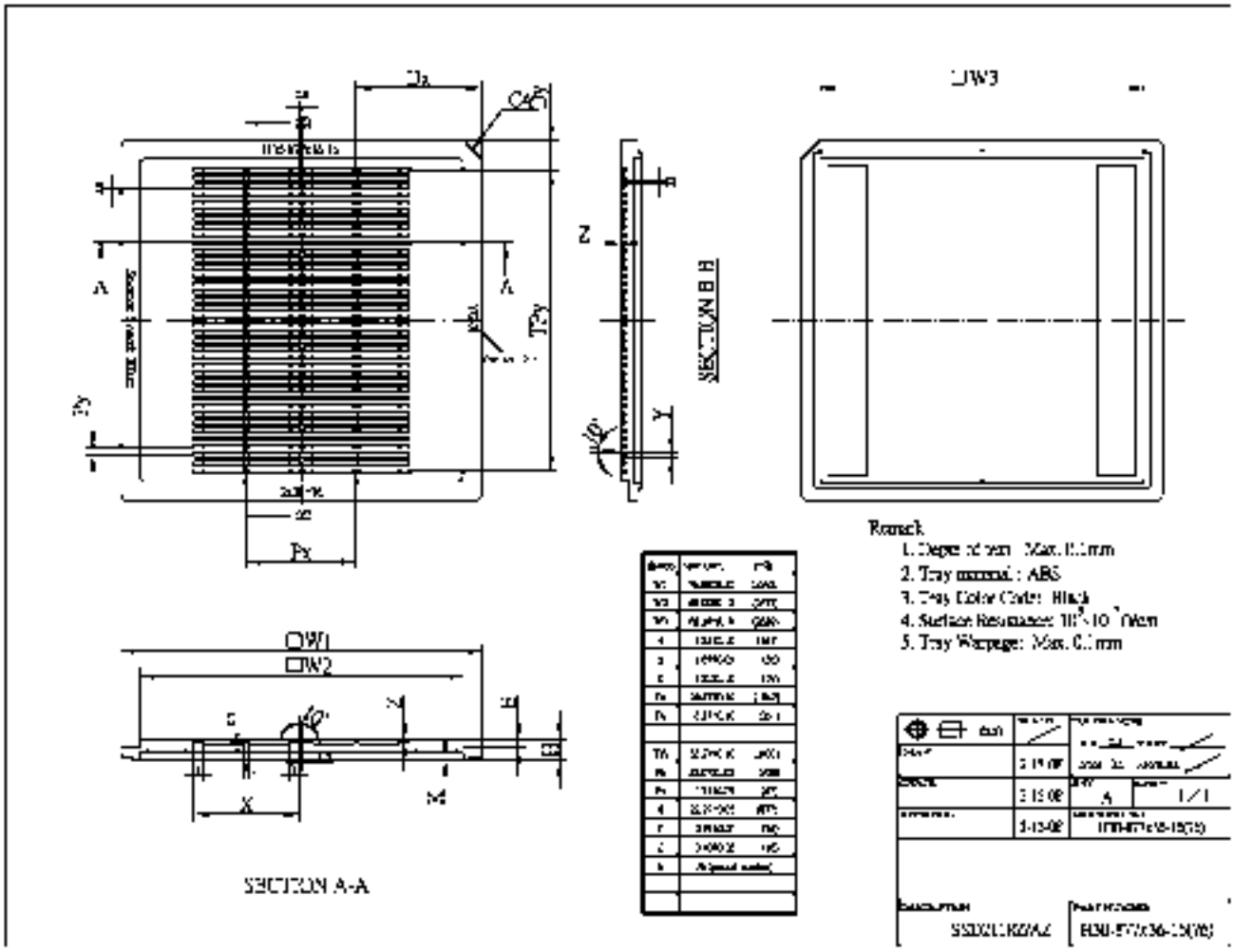
Figure 19-4 - PWM Reference Circuit

Switch is turned on and off by the PWM signal. The average LED current is increased proportionally to the duty-cycle of the PWM signal.



20 PACKAGE INFORMATION

20.1 Die Tray Dimension



21 MTP DETAIL

Fresh die

1) Example 1 - VCMR[5:0] is as default

A fresh SSD2118 will have the MTP register default value of MTPR[5:0]=0x00 and R1F default value of VCMR[5:0]=0x36, which corresponds to base values [110110] from the 6 least significant bits.

VCMR[5:0]	1	1	0	1	1	0
MTPR[5:0]	0	0	0	0	0	0
VCOMH = VCMR XOR MTPR	1	1	0	1	1	0

2) Example 2 - VCMR[5:0] is adjusted

VCMR[5:0] will exclusive or (XOR) with the MTPR default value (0x00) to form a new VCOMH default value, and it is recommended to set this command right after the power control commands when applicable.

For example, when VCMR[5:0]=0x0030 which corresponding to [110000], the resultant VCOMH will be as below.

VCMR[5:0]	1	1	0	0	0	0
MTPR[5:0]	0	0	0	0	0	0
VCOMH = VCMR xor MTPR	1	1	0	0	0	0

The new VCOMH default value will become, 0x30

(Please be noted that preceding 10’b is added to the result so as to have uniformity as R1E command is sent.)

3) Example 3 - VCM[5:0] is adjusted and nMTP=1

nMTP=1 will override the default VCOMH value and is used together with VCM[5:0] to find out the optimal value against flickering.

Purpose VCMR[5:0] and MTPR[5:0] is the same as example 2.

For example, when nMTP=1 and VCM[5:0]=0x36 which corresponding to [110110], the resultant VCOMH will equal VCM regardless the value of VCMR XOR MTPR.

VCM[5:0]	1	1	0	1	1	0
VCOMH = VCM	1	1	0	1	1	0

The new VCOMH value will become, 0x36

(Please be noted that preceding 10’b is added to the result so as to have uniformity as R1E command is sent.)

Program MTP

When nMTP=1, R1E command is mainly used to find out the optimal value against flickering. The MTPR will be programmed as below.
(The equivalent VCOMH value is simply VCM[5:0] if nMTP is 1)

1) Example 1 - VCMR[5:0] is as default, target VCOMH value is equivalent to VCM[5:0] = 0x30.

When R1E-0x00B0 is sent, VCM[5:0] will be [110000]. The MTPR will be the XOR result of VCM[5:0] and VCMR[5:0]. In this case, VCMR[5:0] is the default = 0x36.

VCM[5:0]	1	1	0	0	0	0
VCMR[5:0]	1	1	0	1	1	0
MTPR[5:0]	0	0	0	**1**	**1**	0

The result in MTPR means bit 2 and bit 1 in MTPR[5:0] are programmed.

2) Example 2 – VCMR[5:0]=0x30 is adjusted, target VCOMH value is equivalent to VCM[5:0] = 0x30.

For optimum performance against flickering with different panel characteristic, VCMR[5:0] can be adjusted to reduce the frequency on MTP execution.

For VCMR[5:0]=0x30 is adjusted, and VCOMH target is same as VCM[5:0]=0x30, the below result shows that MTP is not required if VCMR[5:0] is adjusted.

VCM[5:0]	1	1	0	0	0	0
VCMR[5:0]	1	1	0	0	0	0
Result MTPR[5:0]	**0**	**0**	**0**	**0**	**0**	**0**

However, SSD2118 requires VCMR[5:0]=0x30 to be updated when power up every time in order to produce the target VCOMH value of VCM[5:0]=0x30

VCMR[5:0]	1	1	0	0	0	0
MTPR	0	0	0	0	0	0
VCOMH = VCMR xor MTPR	1	1	0	0	0	0

Please be reminded that MTP registers can be fired once and cannot be recovered, it is recommended to finalize the optimal MTP value before firing.

3) Example 3 – VCMR[5:0]=0x30 is adjusted, target VCOMH value is equivalent to VCM[5:0] = 0x31.

Upon process variation, there may be a variation in the panel characteristic, MTP may be used to adapt this.

VCMR[5:0] is adjusted to 0x30 as example 2 to reduce the frequency on MTP execution.

For VCM[5:0]=0x31 is adjusted to adapt the process variation, and VCOMH target is same as VCM[5:0]=0x31, the below result shows that only bit 1 of MTPR is required for programming if VCMR[5:0] is adjusted.

VCM [5:0]	1	1	0	0	0	1
VCMR[5:0]	1	1	0	0	0	0
Result MTPR	**0**	**0**	**0**	**0**	**0**	**1**

However, SSD2118 requires VCMR[5:0]=0x30 to be updated when power up every time in order to produce the target VCOMH value of VCM[5:0]=0x31

VCMR[5:0]	1	1	0	0	0	0
MTPR	0	0	0	0	0	1
VCOMH = VCMR XOR MTPR	**1**	**1**	**0**	**0**	**0**	**1**

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http://www.solomon-systech.com

Appendix: IC Revision history of SSD2118 Specification

Version	Change Items	Effective Date
1.0	1. Modify R2Bh from 8540h to 8520h in page 23 and 24 2. Add one note in page 24 for MTP read. 3. Typo of HSYNC in page 40 and 41. 4. Modify “Serial” to “DOTCLK” in page 65 ~ 68 5. Add “(Pixel clock = 2MHz)” in page 47 6. Remove 16.7M color and FRC support 7. Change to Advance Information	24-Jun-08