SSD1829

Advance Information

96 x 32 + 1 STN /
96 x 64 + 1 STN /
96 x 65 + 1 STN /
96 x 68 STN
LCD Segment / Common Mono Driver with Controller

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TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1829 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. SSD1829 consists of 164 high voltage driving output pins for driving maximum 96 Segments and 68 Commons.

SSD1829 displays data directly from its internal 96x68 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through hardware selectable 6800-/8080-series compatible Parallel Interface or 4 wires Serial Peripheral Interface.

SSD1829 embeds a DC-DC Converter, a LCD Voltage Regulator, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die layout, SSD1829 is suitable for any portable battery-driven applications requiring a long operation period and a compact size.

2 FEATURES

- 96 x 68 Graphic Display with an optional Icon Line
- Programmable Multiplex ratio [16Mux - 68Mux]
- Pin selectable 68/65/64/32 multiplex ratio configuration
  Maximum display size:
  - 96 columns by 68 rows
  - 96 columns by 65 rows with dual icon lines
  - 96 columns by 64 rows with dual icon lines
  - 96 columns by 32 rows with dual icon lines
- Single Supply Operation, 1.8 V - 3.3V
- Maximum +12V LCD Driving Output Voltage
- Low Current Sleep Mode
- On-Chip 96 x 68 Graphic Display Data RAM
- On-Chip Voltage Generator / External Power Supply
- On-Chip Oscillator
- Software Selectable On-Chip Bias Dividers, with No External Capacitors required
- Hardware pin selectable for 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface or 4-wire Serial Peripheral Interface
- Maximum 17MHz SPI or 10MHz PPI operation
- Software selectable 2X / 3X / 4X / 5X/ 6X On-Chip DC-DC Converter
- Programmable 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 bias ratio
- Re-mapping of Row and Column Drivers
- Vertical Scrolling
- Display Offset Control
- 64 Levels Internal Contrast Control
- Selectable LCD Driving Voltage Temperature Coefficients (4 settings)
- Non-Volatile Memory (OTP) for calibration

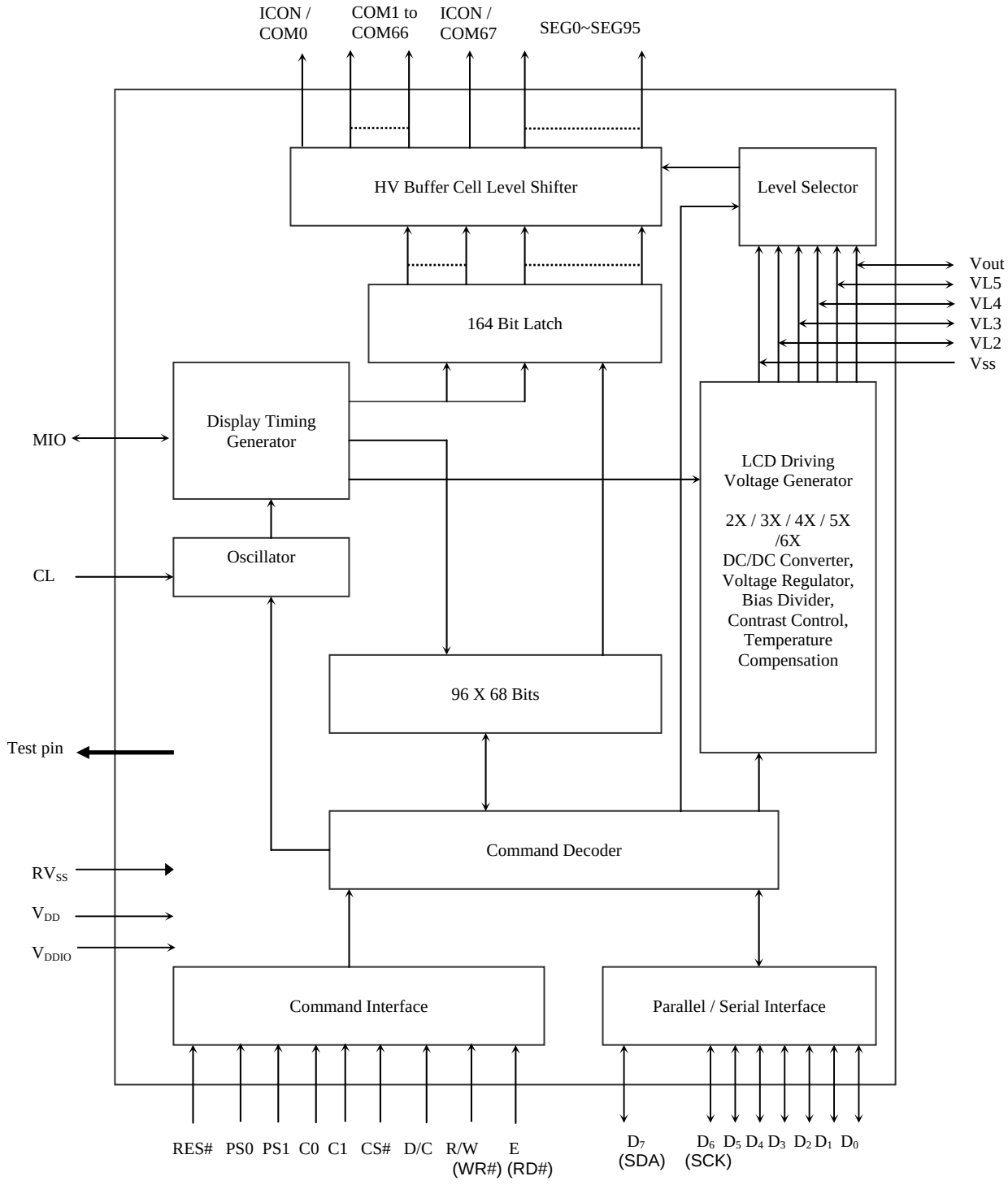
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Seg	Com	Package Form	Reference	Remark
SSD1829Z	96	68	Gold Bump die	Figure 5-1 on P. 8	

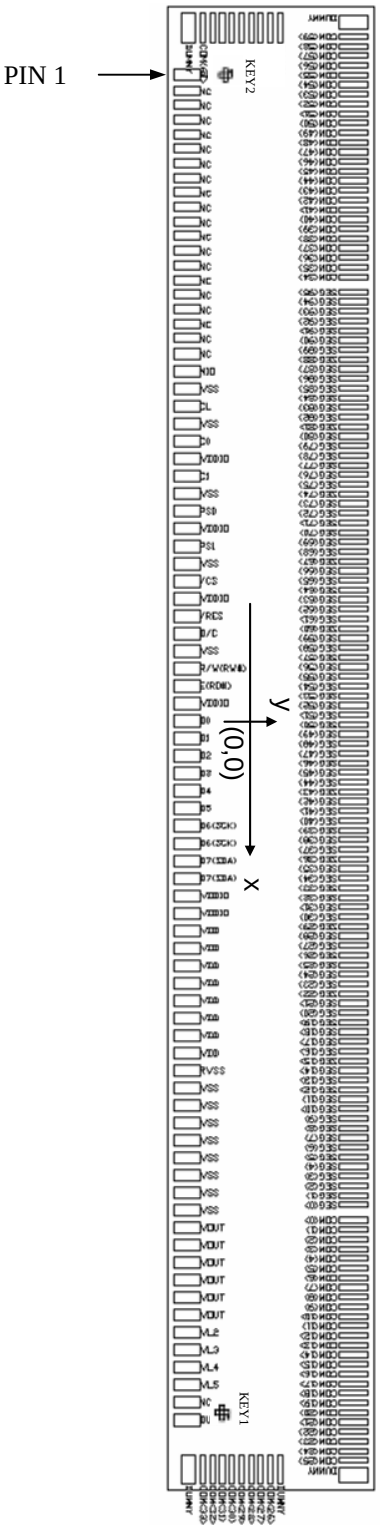
4 BLOCK DIAGRAM

Figure 4-1 : SSD1829 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1829 Die Pad Floor Plan



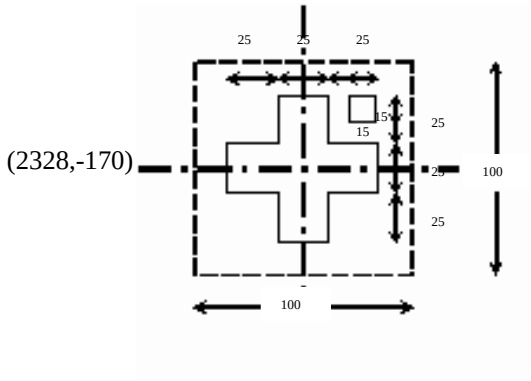
Note

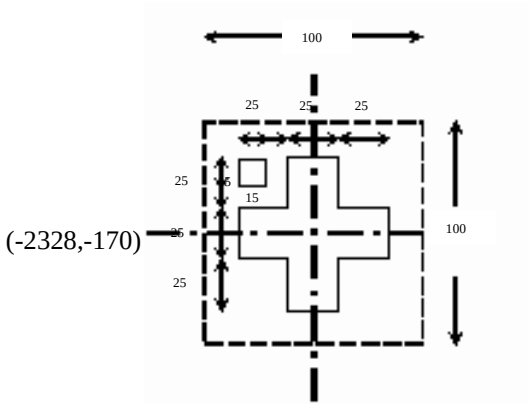
(1) Diagram showing the die face up.

(2) Coordinates are referenced to center of the chip.

(3) Coordinate units and size of all alignment marks are in um.

(4) All alignment keys do not contain gold





Die Size	5.103 X 0.72 = 3.67mm^2
Die Thickness	300 ± 25 um
Typical Bump Height	15 um
Bump Co-planarity (within die)	≤2 um

Note: IC material Temperature expansion factor should take into account during panel design.

Table 5-1 : SSD1829 Bump Die Pad Coordinates (Bump center)

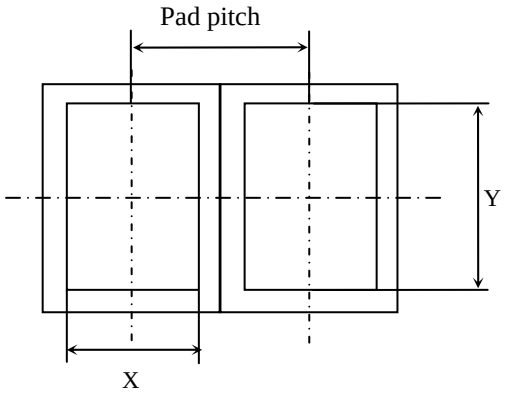
Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1	DUMMY	-2314.5	-287	49	D7(SDA)	385.5	-287	97	COM<21>	2312.5	282.5
2	NC	-2259.5	-287	50	D7(SDA)	445.5	-287	98	COM<20>	2279.5	282.5
3	NC	-2209.5	-287	51	VDDIO	505.5	-287	99	COM<19>	2246.5	282.5
4	NC	-2159.5	-287	52	VDDIO	565.5	-287	100	COM<18>	2213.5	282.5
5	NC	-2109.5	-287	53	VDD	625.5	-287	101	COM<17>	2180.5	282.5
6	NC	-2059.5	-287	54	VDD	685.5	-287	102	COM<16>	2147.5	282.5
7	NC	-2009.5	-287	55	VDD	745.5	-287	103	COM<15>	2114.5	282.5
8	NC	-1959.5	-287	56	VDD	805.5	-287	104	COM<14>	2081.5	282.5
9	NC	-1909.5	-287	57	VDD	865.5	-287	105	COM<13>	2048.5	282.5
10	NC	-1859.5	-287	58	VDD	925.5	-287	106	COM<12>	2015.5	282.5
11	NC	-1809.5	-287	59	VDD	985.5	-287	107	COM<11>	1982.5	282.5
12	NC	-1759.5	-287	60	VDD	1045.5	-287	108	COM<10>	1949.5	282.5
13	NC	-1709.5	-287	61	RVSS	1105.5	-287	109	COM<9>	1916.5	282.5
14	NC	-1659.5	-287	62	VSS	1165.5	-287	110	COM<8>	1883.5	282.5
15	NC	-1609.5	-287	63	VSS	1225.5	-287	111	COM<7>	1850.5	282.5
16	NC	-1559.5	-287	64	VSS	1285.5	-287	112	COM<6>	1817.5	282.5
17	NC	-1509.5	-287	65	VSS	1345.5	-287	113	COM<5>	1784.5	282.5
18	NC	-1459.5	-287	66	VSS	1405.5	-287	114	COM<4>	1751.5	282.5
19	NC	-1409.5	-287	67	VSS	1465.5	-287	115	COM<3>	1718.5	282.5
20	NC	-1354.5	-287	68	VSS	1525.5	-287	116	COM<2>	1685.5	282.5
21	MIO	-1294.5	-287	69	VSS	1585.5	-287	117	COM<1>	1652.5	282.5
22	VSS	-1234.5	-287	70	VOUT	1645.5	-287	118	COM<0>	1619.5	282.5
23	CL	-1174.5	-287	71	VOUT	1705.5	-287	119	SEG<0>	1567.5	282.5
24	VSS	-1114.5	-287	72	VOUT	1765.5	-287	120	SEG<1>	1534.5	282.5
25	C0	-1054.5	-287	73	VOUT	1825.5	-287	121	SEG<2>	1501.5	282.5
26	VDDIO	-994.5	-287	74	VOUT	1885.5	-287	122	SEG<3>	1468.5	282.5
27	C1	-934.5	-287	75	VOUT	1945.5	-287	123	SEG<4>	1435.5	282.5
28	VSS	-874.5	-287	76	VL2	2005.5	-287	124	SEG<5>	1402.5	282.5
29	PS0	-814.5	-287	77	VL3	2065.5	-287	125	SEG<6>	1369.5	282.5
30	VDDIO	-754.5	-287	78	VL4	2125.5	-287	126	SEG<7>	1336.5	282.5
31	PS1	-694.5	-287	79	VL5	2185.5	-287	127	SEG<8>	1303.5	282.5
32	VSS	-634.5	-287	80	NC	2245.5	-287	128	SEG<9>	1270.5	282.5
33	/CS	-574.5	-287	81	DUMMY	2305.5	-287	129	SEG<10>	1237.5	282.5
34	VDDIO	-514.5	-287	82	DUMMY	2474	-282	130	SEG<11>	1204.5	282.5
35	/RES	-454.5	-287	83	COM<33>	2474	-233	131	SEG<12>	1171.5	282.5
36	D/C	-394.5	-287	84	COM<32>	2474	-200	132	SEG<13>	1138.5	282.5
37	VSS	-334.5	-287	85	COM<31>	2474	-167	133	SEG<14>	1105.5	282.5
38	R/W(RW#)	-274.5	-287	86	COM<30>	2474	-134	134	SEG<15>	1072.5	282.5
39	E(RD#)	-214.5	-287	87	COM<29>	2474	-101	135	SEG<16>	1039.5	282.5
40	VDDIO	-154.5	-287	88	COM<28>	2474	-68	136	SEG<17>	1006.5	282.5
41	D0	-94.5	-287	89	COM<27>	2474	-35	137	SEG<18>	973.5	282.5
42	D1	-34.5	-287	90	COM<26>	2474	-2	138	SEG<19>	940.5	282.5
43	D2	25.5	-287	91	DUMMY	2474	31	139	SEG<20>	907.5	282.5
44	D3	85.5	-287	92	DUMMY	2493.5	282.5	140	SEG<21>	874.5	282.5
45	D4	145.5	-287	93	COM<25>	2444.5	282.5	141	SEG<22>	841.5	282.5
46	D5	205.5	-287	94	COM<24>	2411.5	282.5	142	SEG<23>	808.5	282.5
47	D6(SCK)	265.5	-287	95	COM<23>	2378.5	282.5	143	SEG<24>	775.5	282.5
48	D6(SCK)	325.5	-287	96	COM<22>	2345.5	282.5	144	SEG<25>	742.5	282.5

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
145	SEG<26>	709.5	282.5	193	SEG<74>	-874.5	282.5
146	SEG<27>	676.5	282.5	194	SEG<75>	-907.5	282.5
147	SEG<28>	643.5	282.5	195	SEG<76>	-940.5	282.5
148	SEG<29>	610.5	282.5	196	SEG<77>	-973.5	282.5
149	SEG<30>	577.5	282.5	197	SEG<78>	-1006.5	282.5
150	SEG<31>	544.5	282.5	198	SEG<79>	-1039.5	282.5
151	SEG<32>	511.5	282.5	199	SEG<80>	-1072.5	282.5
152	SEG<33>	478.5	282.5	200	SEG<81>	-1105.5	282.5
153	SEG<34>	445.5	282.5	201	SEG<82>	-1138.5	282.5
154	SEG<35>	412.5	282.5	202	SEG<83>	-1171.5	282.5
155	SEG<36>	379.5	282.5	203	SEG<84>	-1204.5	282.5
156	SEG<37>	346.5	282.5	204	SEG<85>	-1237.5	282.5
157	SEG<38>	313.5	282.5	205	SEG<86>	-1270.5	282.5
158	SEG<39>	280.5	282.5	206	SEG<87>	-1303.5	282.5
159	SEG<40>	247.5	282.5	207	SEG<88>	-1336.5	282.5
160	SEG<41>	214.5	282.5	208	SEG<89>	-1369.5	282.5
161	SEG<42>	181.5	282.5	209	SEG<90>	-1402.5	282.5
162	SEG<43>	148.5	282.5	210	SEG<91>	-1435.5	282.5
163	SEG<44>	115.5	282.5	211	SEG<92>	-1468.5	282.5
164	SEG<45>	82.5	282.5	212	SEG<93>	-1501.5	282.5
165	SEG<46>	49.5	282.5	213	SEG<94>	-1534.5	282.5
166	SEG<47>	16.5	282.5	214	SEG<95>	-1567.5	282.5
167	SEG<48>	-16.5	282.5	215	COM<34>	-1619.5	282.5
168	SEG<49>	-49.5	282.5	216	COM<35>	-1652.5	282.5
169	SEG<50>	-82.5	282.5	217	COM<36>	-1685.5	282.5
170	SEG<51>	-115.5	282.5	218	COM<37>	-1718.5	282.5
171	SEG<52>	-148.5	282.5	219	COM<38>	-1751.5	282.5
172	SEG<53>	-181.5	282.5	220	COM<39>	-1784.5	282.5
173	SEG<54>	-214.5	282.5	221	COM<40>	-1817.5	282.5
174	SEG<55>	-247.5	282.5	222	COM<41>	-1850.5	282.5
175	SEG<56>	-280.5	282.5	223	COM<42>	-1883.5	282.5
176	SEG<57>	-313.5	282.5	224	COM<43>	-1916.5	282.5
177	SEG<58>	-346.5	282.5	225	COM<44>	-1949.5	282.5
178	SEG<59>	-379.5	282.5	226	COM<45>	-1982.5	282.5
179	SEG<60>	-412.5	282.5	227	COM<46>	-2015.5	282.5
180	SEG<61>	-445.5	282.5	228	COM<47>	-2048.5	282.5
181	SEG<62>	-478.5	282.5	229	COM<48>	-2081.5	282.5
182	SEG<63>	-511.5	282.5	230	COM<49>	-2114.5	282.5
183	SEG<64>	-544.5	282.5	231	COM<50>	-2147.5	282.5
184	SEG<65>	-577.5	282.5	232	COM<51>	-2180.5	282.5
185	SEG<66>	-610.5	282.5	233	COM<52>	-2213.5	282.5
186	SEG<67>	-643.5	282.5	234	COM<53>	-2246.5	282.5
187	SEG<68>	-676.5	282.5	235	COM<54>	-2279.5	282.5
188	SEG<69>	-709.5	282.5	236	COM<55>	-2312.5	282.5
189	SEG<70>	-742.5	282.5	237	COM<56>	-2345.5	282.5
190	SEG<71>	-775.5	282.5	238	COM<57>	-2378.5	282.5
191	SEG<72>	-808.5	282.5	239	COM<58>	-2411.5	282.5
192	SEG<73>	-841.5	282.5	240	COM<59>	-2444.5	282.5

Pad #	Signal	X-pos	Y-pos
241	DUMMY	-2493.5	282.5
242	DUMMY	-2474	31
243	COM<60>	-2474	-2
244	COM<61>	-2474	-35
245	COM<62>	-2474	-68
246	COM<63>	-2474	-101
247	COM<64>	-2474	-134
248	COM<65>	-2474	-167
249	COM<66>	-2474	-200
250	COM<67>	-2474	-233
251	DUMMY	-2474	-282

Bump Size

Pad #	X [um]	Y [um]	Pad pitch [um] (Min)
1	40	89	55
2-19	30	89	50
20-81	40	89	60
82	100	50	49
83-91	100	18	33
92	50	100	49
93-240	18	100	33
241	50	100	49
242-250	100	18	33
251	100	50	49



6 PIN DESCRIPTIONS

6.1 RES#

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

6.2 PS0, PS1

These pins pair to determine the interface protocol between the driver and MCU, according to the following table.

Table 6-1 : PS0 & PS1 Interface

PS0	PS1	Interface
L	H	4-wire SPI (write only)
H	L	8080 parallel interface (read and write allowed)
H	H	6800 parallel interface (read and write allowed)

Note1: For serial applications, D0 – D5, R/W (WR), E(RD) pins are recommended to connect VDDIO.
Note2: Read back operation is only available in parallel mode

6.3 CS#

This pin is chip select input. The chip is enabled for display data/command transfer only when CS is low.

6.4 D/C

This input pin is to identify display data/command cycle. When the pin is high, the data written to the driver will be written into display RAM. When the pin is low, the data will be interpreted as command.

6.5 R/W(WR#)

This pin is microprocessor interface signal. When interfacing to a 6800-series microprocessor, the signal indicates read mode when high and write mode when low. When interfacing to an 8080-microprocessor, a data write operation is initiated when R/W(WR#) is low and the chip is selected.

6.6 E(RD#)

This pin is microprocessor interface signal. When interfacing to an 6800-series microprocessor, a data operation is initiated when E(RD#) is high and the chip is selected. When interfacing to an 8080-microprocessor, a data read operation is initiated when E(RD#) is low and the chip is selected.

6.7 D_0 -D_7

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 is the serial data input SDA and D_6 is the serial clock input SCK.

6.8 V_{DD}

Power supply pin

6.9 V_{DDIO}

This pin is the system power supply pin of bus IO buffer.

6.10 RV_{SS}

Ground reference of Vref.

6.11 V_{SS}

Ground reference of analog and logic circuitry.

6.12 Vout

These pins are the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal regulator. All Vout pins must be connected together for normal circumstances.

6.13 V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$V_{out} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$

Table 6-2 : Vout > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{ss} Relationship

	1 : a bias
V_{L5}	(a-1)/a * Vout
V_{L4}	(a-2)/a * Vout
V_{L3}	2/a * Vout
V_{L2}	1/a * Vout

where a is equals to 9 at POR.

6.14 C0, C1

These pins are the Chip Mode Selection input. The chip mode is determined by multiplex ratio. Altogether there are four chip modes. Please see the following list for reference.

C1	C0	Chip Mode
0	0	32 MUX + 1 icon Mode
0	1	64 MUX+ 1 icon Mode
1	0	65 MUX+ 1 icon Mode
1	1	68 MUX Mode

Please refer to Table 6-3 on P. 15 for detail description of common pins at different multiplex mode.

6.15 COM1 – COM66

These pins provide the row driving signal COM1 - COM66 to the LCD panel. See about the COM signal mapping in different multiplex ratio N.

6.16 COM 0 / COM 67 / ICONS

This pin is the special icon line COM signal output in 32 MUX + 1 icon Mode/ 64 MUX+ 1 icon Mode or 65 MUX+ 1 icon Mode and this is the pin provides the row driving signal COM0 / COM67 in 68 MUX Mode.

6.17 SEG0 – SEG95

These pins provide the LCD column driving signal. Their voltage level is V_{SS} during sleep mode.

6.18 CL

This pin is the external clock input for the device, which is enabled by using an extended command. Under normal operation, this pin should be left opened and internal oscillator will be used after power on reset.

6.19 MIO

This pin is used for test purpose only. Under normal operation, it should be left open.

6.20 TEST pins

These pins is used for internal only and should be left open, any connection is not allowed.

Table 6-3 : Arrangement of common at different multiplex modes

Command	C0 = 0; C1 = 0;	C0 = 1; C1 = 0;	C0 = 0; C1 = 1;	C0 = 1; C1 = 1;
Pin Name	**32Mux Mode**	**64Mux Mode**	**65Mux Mode**	**68Mux Mode**
ROW0	ICON	ICON	ICON	COM0
ROW1	COM0	Non-select	COM0	COM1
ROW2	COM1	COM0	COM1	COM2
ROW3	COM2	COM1	COM2	COM3
ROW4	COM3	COM2	COM3	COM4
ROW5	COM4	COM3	COM4	COM5
ROW6	COM5	COM4	COM5	COM6
ROW7	COM6	COM5	COM6	COM7
ROW8	COM7	COM6	COM7	COM8
ROW9	COM8	COM7	COM8	COM9
ROW10	COM9	COM8	COM9	COM10
ROW11	COM10	COM9	COM10	COM11
ROW12	COM11	COM10	COM11	COM12
ROW13	COM12	COM11	COM12	COM13
ROW14	COM13	COM12	COM13	COM14
ROW15	COM14	COM13	COM14	COM15
ROW16	COM15	COM14	COM15	COM16
ROW17	Non-select	COM15	COM16	COM17
ROW18	Non-select	COM16	COM17	COM18
ROW19	Non-select	COM17	COM18	COM19
ROW20	Non-select	COM18	COM19	COM20
ROW21	Non-select	COM19	COM20	COM21
ROW22	Non-select	COM20	COM21	COM22
ROW23	Non-select	COM21	COM22	COM23
ROW24	Non-select	COM22	COM23	COM24
ROW25	Non-select	COM23	COM24	COM25
ROW26	Non-select	COM24	COM25	COM26
ROW27	Non-select	COM25	COM26	COM27
ROW28	Non-select	COM26	COM27	COM28
ROW29	Non-select	COM27	COM28	COM29
ROW30	Non-select	COM28	COM29	COM30
ROW31	Non-select	COM29	COM30	COM31
ROW32	Non-select	COM30	COM31	COM32
ROW33	Non-select	COM31	COM32	COM33
ROW34	Non-select	Non-select	Non-select	COM34
ROW35	COM16	COM32	COM33	COM35
ROW36	COM17	COM33	COM34	COM36
ROW37	COM18	COM34	COM35	COM37
ROW38	COM19	COM35	COM36	COM38
ROW39	COM20	COM36	COM37	COM39
ROW40	COM21	COM37	COM38	COM40
ROW41	COM22	COM38	COM39	COM41
ROW42	COM23	COM39	COM40	COM42
ROW43	COM24	COM40	COM41	COM43
ROW44	COM25	COM41	COM42	COM44
ROW45	COM26	COM42	COM43	COM45
ROW46	COM27	COM43	COM44	COM46
ROW47	COM28	COM44	COM45	COM47
ROW48	COM29	COM45	COM46	COM48
ROW49	COM30	COM46	COM47	COM49
ROW50	COM31	COM47	COM48	COM50
ROW51	Non-select	COM48	COM49	COM51
ROW52	Non-select	COM49	COM50	COM52
ROW53	Non-select	COM50	COM51	COM53
ROW54	Non-select	COM51	COM52	COM54
ROW55	Non-select	COM52	COM53	COM55
ROW56	Non-select	COM53	COM54	COM56
ROW57	Non-select	COM54	COM55	COM57
ROW58	Non-select	COM55	COM56	COM58
ROW59	Non-select	COM56	COM57	COM59
ROW60	Non-select	COM57	COM58	COM60
ROW61	Non-select	COM58	COM59	COM61
ROW62	Non-select	COM59	COM60	COM62
ROW63	Non-select	COM60	COM61	COM63
ROW64	Non-select	COM61	COM62	COM64
ROW65	Non-select	COM62	COM63	COM65
ROW66	Non-select	COM63	COM64	COM66
ROW67	ICON	ICON	ICON	COM67

Remarks: “Non-select” means no common signal will be selected to support those output ROW pins.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Command Decoder and Command Interface

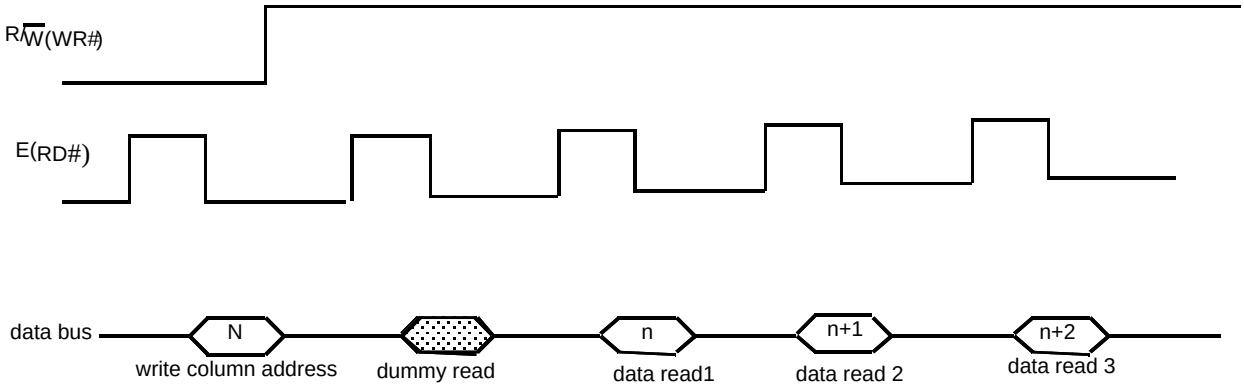
This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C is high, data is written to Graphic Display Data RAM (GDDRAM). If D/C is low, the input at D_0 -D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once RES# receives a negative reset pulse of about 1us, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

7.2 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/W(WR#), D/C, E(RD#) and CS#. R/W(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD#) and CS# input serves as data latch signal (clock) when they are high and low respectively. Refer to Figure 12-2 parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1 below.

Figure 7-1 : Display Data Read with the insertion of Dummy Read



MPU Parallel 8080-series Interface
The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/W(WR#), E(RD#), D/C and CS#. The CS# input serves as data latch signal (clock) when it is low. Whether it is display data or status register read is controlled by D/C. R/W(WR#) and E(RD#) input indicates a write or read cycle when CS is low. Refer to Figure 12-4 parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

7.3 MPU Serial 4-wire Interface

The serial interface consists of serial clock SCK, serial data SDA, D/C and CS#. SDA is shifted into a 8-bit shift register on every rising edge of SCK in the order of D_7, D_6, ... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock. No extra clock or command is required to end the transmission.

It should be noted that if there is a signal glitch at SCK that causing an out of synchronization in the serial communication, a hardware reset pulse at RES# pin is required to initialize the chip for re-synchronization.

Table 7-1 : Modes of Operation

	6800 Parallel	8080 Parallel	Serial
Data Read	Yes	Yes	No
Data Write	Yes	Yes	Yes
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

7.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 96 x 68 = 6,528bits for SSD1829. Please refer to the description of the GDDRAM address map.
For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.
For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data mapped to the display.
For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

7.5 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages.

It consists of:

1. 2X, 3X, 4X, 5X and 6X DC-DC voltage converter
2. Bias Divider
   If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (Vout) to give the LCD driving levels (V_{L2} - V_{L5}).
   The divider does not require external capacitors to reduce the external hardware and pin counts.
3. Contrast Control
   Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry
   Software control of 1/4 to 1/9 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.

7.6 164 Bit Latch

A register carries the display signal information. In 96 X 68 display-mode, data will be fed to the HV-buffer Cell and level-shifted to the required level.

7.7 Level selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

7.8 HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter, which translated the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

7.9 Default Value after hardware reset

Table 7-2: Default Value After Hardware Reset

When RES input is low, the chip is initialized to the following:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display ON/OFF	0	Display OFF
Display Start Line	0	GDDRAM page 0,D0
Display Offset	0	COM0 is mapped to ROW0
Mux Ratio	44H	68 Mux
Normal/Reverse Display	0	Normal Display
N-line Inversion	0	No N-line Inversion
Entire Display	0	Entire Display is OFF
DC-DC booster	6FH	6X booster is selected
Internal Resistor Ratio	0	Gain = 3.01 (IR0)
Contrast	20H	
LCD Bias Ratio	5	1/9 Bias Ratio
Scan direction of COM	0	Normal Scan direction
Segment Remap	0	Segment remap is disabled
Internal oscillator	0	Internal oscillator is OFF
Temperature coefficient	5	PTC5 (-0.05%/^{o}C)
Icon display	0	Icon display line is OFF
Frame frequency	2	Frame frequency = 75Hz
Power control	0,0,0	Booster, regulator & divider are both disabled

When RESET command is issued, the following parameters are initialized only:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 3.01 (IR0)
DC-DC booster	6FH	6X booster is selected
Contrast	20H	

7.10 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 96 x 68 = 6,528bits. Table 7-3 on P. 19 is a description of the GDDRAM address map in which the display start line register is set at 18H. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data mapped to the display. For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage. Please be noticed that the display offset cannot be greater than the default mux mode for any circumstance.

Table 7-3 - Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 18h

RAM Row	RAM Column	Normal	00h	01h	-----	42h	43h	32 Mux Mode Common Pins		64 Mux Mode Common Pins		65 Mux Mode Common Pins		68 Mux Mode Common Pins	
		Remapped	43h	42h	-----	01h	00h	Normal	Remapped	Normal	Remapped	Normal	Remapped	Normal	Remapped
00h	Page 0	DB0 (LSB)			-----			8	23	40	23	41	23	44	23
01h		DB1			-----			9	22	41	22	42	22	45	22
02h		DB2			-----			10	21	42	21	43	21	46	21
03h		DB3			-----			11	20	43	20	44	20	47	20
04h		DB4			-----			12	19	44	19	45	19	48	19
05h		DB5			-----			13	18	45	18	46	18	49	18
06h		DB6			-----			14	17	46	17	47	17	50	17
07h		DB7 (MSB)			-----			15	16	47	16	48	16	51	16
08h	Page 1	DB0 (LSB)			-----			16	15	48	15	49	15	52	15
09h		DB1			-----			17	14	49	14	50	14	53	14
0Ah		DB2			-----			18	13	50	13	51	13	54	13
0Bh		DB3			-----			19	12	51	12	52	12	55	12
0Ch		DB4			-----			20	11	52	11	53	11	56	11
0Dh		DB5			-----			21	10	53	10	54	10	57	10
0Eh		DB6			-----			22	9	54	9	55	9	58	9
0Fh		DB7 (MSB)			-----			23	8	55	8	56	8	59	8
10h	Page 2	DB0 (LSB)			-----			24	7	56	7	57	7	60	7
11h		DB1			-----			25	6	57	6	58	6	61	6
12h		DB2			-----			26	5	58	5	59	5	62	5
13h		DB3			-----			27	4	59	4	60	4	63	4
14h		DB4			-----			28	3	60	3	61	3	64	3
15h		DB5			-----			29	2	61	2	62	2	65	2
16h		DB6			-----			30	1	62	1	63	1	66	1
17h		DB7 (MSB)			-----			31	0	63	0	64	0	67	0
18h	Page 3	DB0 (LSB)			-----			0	31	0	63	0	64	0	67
19h		DB1			-----			1	30	1	62	1	63	1	66
1Ah		DB2			-----			2	29	2	61	2	62	2	65
1Bh		DB3			-----			3	28	3	60	3	61	3	64
1Ch		DB4			-----			4	27	4	59	4	60	4	63
1Dh		DB5			-----			5	26	5	58	5	59	5	62
1Eh		DB6			-----			6	25	6	57	6	58	6	61
1Fh		DB7 (MSB)			-----			7	24	7	56	7	57	7	60
20h	Page 4	DB0 (LSB)			-----			Non-select	Non-select	8	55	8	56	8	59
21h		DB1			-----			Non-select	Non-select	9	54	9	55	9	58
22h		DB2			-----			Non-select	Non-select	10	53	10	54	10	57
23h		DB3			-----			Non-select	Non-select	11	52	11	53	11	56
24h		DB4			-----			Non-select	Non-select	12	51	12	52	12	55
25h		DB5			-----			Non-select	Non-select	13	50	13	51	13	54
26h		DB6			-----			Non-select	Non-select	14	49	14	50	14	53
27h		DB7 (MSB)			-----			Non-select	Non-select	15	48	15	49	15	52
28h	Page 5	DB0 (LSB)			-----			Non-select	Non-select	16	47	16	48	16	51
29h		DB1			-----			Non-select	Non-select	17	46	17	47	17	50
2Ah		DB2			-----			Non-select	Non-select	18	45	18	46	18	49
2Bh		DB3			-----			Non-select	Non-select	19	44	19	45	19	48
2Ch		DB4			-----			Non-select	Non-select	20	43	20	44	20	47
2Dh		DB5			-----			Non-select	Non-select	21	42	21	43	21	46
2Eh		DB6			-----			Non-select	Non-select	22	41	22	42	22	45
2Fh		DB7 (MSB)			-----			Non-select	Non-select	23	40	23	41	23	44
30h	Page 6	DB0 (LSB)			-----			Non-select	Non-select	24	39	24	40	24	43
31h		DB1			-----			Non-select	Non-select	25	38	25	39	25	42
32h		DB2			-----			Non-select	Non-select	26	37	26	38	26	41
33h		DB3			-----			Non-select	Non-select	27	36	27	37	27	40
34h		DB4			-----			Non-select	Non-select	28	35	28	36	28	39
35h		DB5			-----			Non-select	Non-select	29	34	29	35	29	38
36h		DB6			-----			Non-select	Non-select	30	33	30	34	30	37
37h		DB7 (MSB)			-----			Non-select	Non-select	31	32	31	33	31	36
38h	Page 7	DB0 (LSB)			-----			Non-select	Non-select	32	31	32	32	32	35
39h		DB1			-----			Non-select	Non-select	33	30	33	31	33	34
3Ah		DB2			-----			Non-select	Non-select	34	29	34	30	34	33
3Bh		DB3			-----			Non-select	Non-select	35	28	35	29	35	32
3Ch		DB4			-----			Non-select	Non-select	36	27	36	28	36	31
3Dh		DB5			-----			Non-select	Non-select	37	26	37	27	37	30
3Eh		DB6			-----			Non-select	Non-select	38	25	38	26	38	29
3Fh		DB7 (MSB)			-----			Non-select	Non-select	39	24	39	25	39	28
40h	Page 8	DB0 (LSB)			-----			Non-select	Non-select	Non-select	Non-select	40	24	40	27
41h		DB1			-----			Non-select	Non-select	Non-select	Non-select	Non-select	Non-select	41	26
42h		DB2			-----			Non-select	Non-select	Non-select	Non-select	Non-select	Non-select	42	25
43h		DB3			-----			ICON	ICON	ICON	ICON	ICON	ICON	43	24

Segment Re-map =0	00	01	------	5E	5F
Segment Re-map =1	5F	5E	------	01	00
SEG Outputs	SEG0	SEG1	------	SEG94	SEG95

Remarks: DB0 – DB7 represent the data bit of the GDDRAM.
"Non-select" means corresponding ram content will support non-select common signal at ROW pins.

7.11 LCD Panel Driving Waveform

Figure 7-2 - LCD Display Example "0"

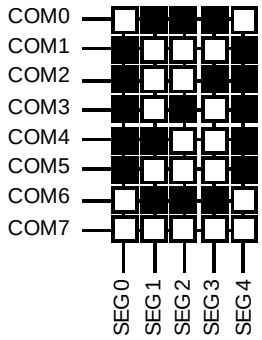
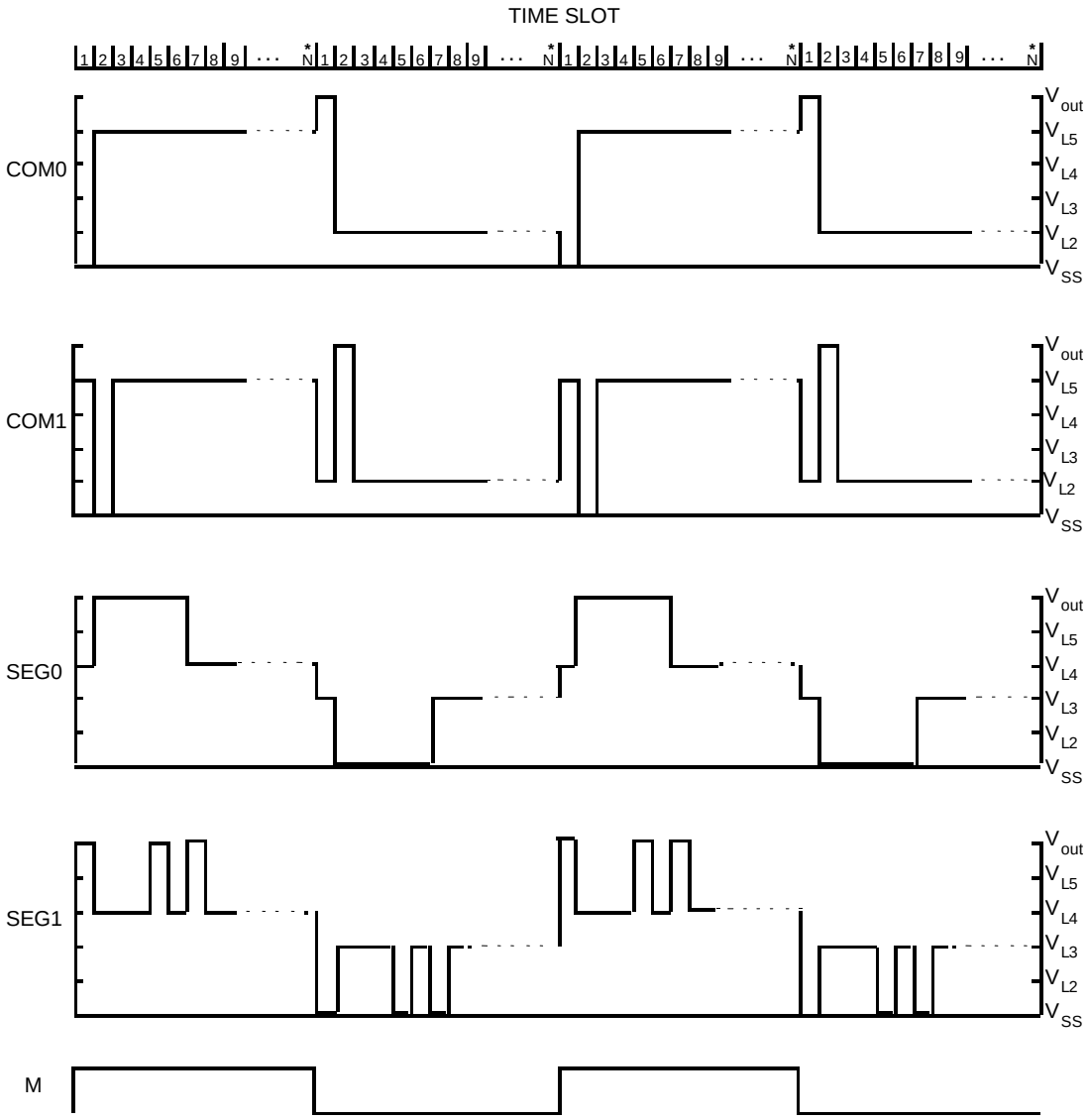


Figure 7-3 : LCD Driving Signal from SSD1829



* Note : N is the number of multiplex ratio including Icon line if it is enabled, N is equal to 64 on POR.

8 COMMAND TABLE

Table 8-1 : Command Table (R/W (WR#) = 0, E(RD#) = 1 unless specific setting is stated)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00 – 0F	0	0	0	0	C_3	C_2	C_1	C_0	Set Column LSB	Set the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0	10 – 17	0	0	0	1	0	C_6	C_5	C_4	Set Column MSB	Set the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0	20 – 27	0	0	1	0	0	R_2	R_1	R_0	Set Internal Resistor Ratio	The internal regulator gain ($1+R_2/R_1$) Vout increases as $R_2R_1R_0$ is increased from 000b to 111b. The factor, $1+R_2/R_1$, is given by: $R_2R_1R_0$ = 000: 3.01 (POR) $R_2R_1R_0$ = 001: 3.93 $R_2R_1R_0$ = 010: 4.84 $R_2R_1R_0$ = 011: 5.76 $R_2R_1R_0$ = 100: 6.67 $R_2R_1R_0$ = 101: 7.6 $R_2R_1R_0$ = 110: Reserved $R_2R_1R_0$ = 111: Reserved
0	28 – 2F	0	0	1	0	1	VC	VR	VF	Set Voltage Control Register	VC VR = 00: turn OFF the internal voltage booster & regulator (POR) VC VR = 01,10,11: turn ON the internal voltage booster & regulator VF=0: turn OFF the output op-amp buffer (POR) VF=1: turn ON the output op-amp buffer
0	38 – 3F	0	0	1	1	1	T_2	T_1	T_0	Set TC value	This command set the Temperature Coefficient $T_2T_1T_0$: 011: -0.01% 100: -0.03% 101: -0.05% (POR) 110: -0.08%
0 0	40 00 – 7F	0 *	1 L_6	0 L_5	0 L_4	0 L_3	0 L_2	* L_1	* L_0	Set Initial Display Line	The second command specifies the row address pointer (0-67) of the RAM data to be displayed in COM0. This command has no effect on ICONS. The pointer is set to 0 after reset.
0 0	44 00 – 3F	0 *	1 *	0 C_5	0 C_4	0 C_3	1 C_2	* C_1	* C_0	Set Initial COM0	The second command specifies the mapping of first display line (COM0) to one of ROW0~67. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	48 00 – 7F	0 *	1 D_6	0 D_5	0 D4	1 D_3	0 D_2	* D_1	* D_0	Set Multiplex Ratio (Partial display)	The second command specifies the number of lines, excluding ICONS, to be displayed. With Icon is disabled (POR), 16~64 mux could be selected. With Icon enabled, the available mux are 17~68. D6 – D0 Mux (Icon disable) Mux (Icon enable) 000000 invalid invalid … 0001111 invalid invalid 0010000 16 17 0010001 17 18 … 1000001 65 66 1000010 66 invalid 1000011 67 invalid 1000100 68 invalid … 1111111 invalid invalid
0 0	4C 00 – 1F	0 *	1 *	0 *	0 N_4	1 N_3	1 N_2	* N_1	* N_0	Set N-line Inversion	The second command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of Mux (including the icon line) should NOT be a multiple of the lines of inversion (n).
0	50 – 57	0	1	0	1	0	B_2	B_1	B_0	Set LCD Bias	Sets the LCD bias from 1/4 ~ 1/9 according to $B_2B_1B_0$: 000: 1/4 bias 001: 1/5 bias 010: 1/6 bias 011: 1/7 bias 100: 1/8 bias 101: 1/9 bias (POR) 110: 1/9 bias 111: 1/9 bias
0	64 – 6F	0	1	1	0	B2	1	B_1	B_0	Set Boost Level	Set the DC-DC multiplying factor from 2X to 6X $B_2B_1B_0$: 000: 3X 001: 4X 010: 5X 011: 2X 1XX:6X (POR)
0 0	81 00 – 3F	1 *	0 *	0 C_5	0 C_4	0 C_3	0 C_2	0 C_1	1 C_0	Set Contrast Level	The second command sets one of the 64 contrast levels. The darkness increase as the contrast level increase.
0	A0 – A1	1	0	1	0	0	0	0	S_0	Set Segment Re-map	S_0=0: column address 00H is mapped to SEG0 (POR) S_0=1: column address 5FH is mapped to SEG0
0	A2 – A3	1	0	1	0	0	0	1	C_0	Icon Control Register ON/OFF	C_0=0: Disable icon row (Mux = 16 to 68, POR) C_0=1: Enable icon row (Mux = 17 to 66)
0	A4 – A5	1	0	1	0	0	1	0	E_0	Entire Display Select	E_0=0: Normal display (display according to RAM contents, POR) E_0=1: All pixels are ON regardless of the RAM contents *Note: This command will override the effect of “Set Normal/Invert Display”

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A6 – A7	1	0	1	0	0	1	1	R_0	Invert Display Select	R_0=0: Normal display (display according to RAM contents, POR) R_0=1: Invert display (ON and OFF pixels are inverted) *Note: This command will not affect the display of the icon lines
0	A8	1	0	1	0	1	0	0	0	NOP	No Operation
0	AB	1	0	1	0	1	0	1	1	Start Internal Oscillator	This command starts the internal oscillator. Note that the oscillator is OFF after reset, so this instruction must be executed for initialization.
0	AE – AF	1	0	1	0	1	1	1	D_0	Display On/Off	Turn the display on and off without modifying the content of the RAM. (0: off, 1: on) This command has priority over Entire Display On/Off and Invert Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.
0	B0 – B8	1	0	1	1	P_3	P_2	P_1	P_0	Set Page Address	Set GDDRAM page address (0~8) using $P_3P_2P_1P_0$ for RAM access. The page address is sets to 0 after reset.
0	C0 – C8	1	1	0	0	S_3	*	*	*	Set COM Output Scan Direction	Set the COM (row) scanning direction. 32 mux mode 0: COM0 →COM31, 1: COM31 →COM0 64 mux mode 0: COM0 →COM63, 1: COM63 →COM0 65 mux mode 0: COM0 →COM64, 1: COM64 →COM0 68 mux mode 0: COM0 →COM67, 1: COM67 →COM0
0	D8 – DF	1	1	0	1	1	F_2	F_1	F_0	Set Frame Frequency	This command is used to set the frame frequency. $F_2F_1F_0$ Frame Frequency 000 57Hz 001 66Hz 010 75Hz(POR) 011 82Hz 100 88Hz 101 94Hz 110 100Hz 111 106Hz
0	E1	1	1	1	0	0	0	0	1	Exit Power-save Mode	DC-DC converter, regulator and divider status before entering the power-save mode is restored. At POR, Power-save Mode is released.
0	E2	1	1	1	0	0	0	1	0	Software Reset	Reset some functions of the driver/controller. See Reset Section below for more details.
0	E4	1	1	1	0	0	1	0	0	Release N-line Inversion Mode	Release the driver/controller from N-line inversion mode. The frame will be inverted once per frame.

Extended Command Table

Table 8-2 : Command Table (R/W (WR#) = 0, E(RD#) = 1 unless specific setting is stated)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	82	1 *	0 0	0 0	0 X_4	0 X_3	0 X_2	1 X_1	0 X_0	OTP Setting	$X_4X_3X_2X_1X_0$: OTP fuse value 00000 : original contrast 00001 : original contrast + 1 steps 00010 : original contrast + 2 steps 00011 : original contrast + 3 steps 00100 : original contrast + 4 steps 00101 : original contrast + 5 steps 00110 : original contrast + 6 steps 00111 : original contrast + 7 steps 01000 : original contrast + 8 steps 01001 : original contrast + 9 steps 01010 : original contrast + 10 steps 01011 : original contrast + 11 steps 01100 : original contrast + 12 steps 01101 : original contrast + 13 steps 01110 : original contrast + 14 steps 01111 : original contrast + 15 steps 10000 : original contrast - 16 steps 10001 : original contrast - 15 steps 10010 : original contrast - 14 steps 10011 : original contrast - 13 steps 10100 : original contrast - 12 steps 10101 : original contrast - 11 steps 10110 : original contrast - 10 steps 10111 : original contrast - 9 steps 11000 : original contrast - 8 steps 11001 : original contrast - 7 steps 11010 : original contrast - 6 steps 11011 : original contrast - 5 steps 11100 : original contrast - 4 steps 11101 : original contrast - 3 steps 11110 : original contrast - 2 steps 11111 : original contrast - 1 steps
0	83	1	0	0	0	0	0	1	1	OTP Programming	This command starts to program LCD driver with OTP offset value. Each bit can be programmed to 1 once. Detail of OTP programming procedure on P. 30.
0 0	FA 95/ 9D	1 1	1 0	1 0	1 1	1 A3	0 1	1 0	0 1	High Power Mode	This command enables driver to enter high power mode for heavy loading application. A3: 0: normal power 1: high power (por)
0 0 0 0	F6 A3 F5 06	1 1 1 0	1 0 1 0	1 1 1 0	1 0 1 0	0 0 0 0	1 0 1 1	1 1 0 1	0 1 1 0	High Regulator Driving mode	This command can be used to increase the driving power of regulator

8.1 Read Status Byte

A 8 bits status byte will be placed to the data bus if a read operation is performed if D/C is low. The status byte is defined as follow.

Table 8-3 : Read Status Byte

Bit Pattern	Command	Comment
BUSY ON RES 0 1000	Read Status	BUSY=0: Chip is idle BUSY=1: Chip is executing instruction ON=0: Display is OFF ON=1: Display is ON RES=0: Chip is idle RES=1: Chip is executing reset

8.2 Data Read / Write

To read data from the GDDRAM, input High to R/W(WR#) pin and D/C pin for 6800-series parallel mode. Low to E(RD#) pin and High to D/C pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. Also, a dummy read is required before the first data is read. See Figure 7-1 for Functional Description.

To write data to the GDDRAM, input Low to R/W(WR#) pin and High to D/C pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write. The address will be reset to 0 in next data read/write operation is executed when it is 95.

Table 8-4 : Address Increment Table

D/C	R/W (WR)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Address Increment is done automatically after data read/write. The column address pointer of GDDRAM is also affected. It will be reset to 0 in next data read/write operation is executed when it is 95.

Table 8-5 : Commands Required for R/W (WR#) Actions on RAM

R/W (WR) Actions on RAMs	Commands Required	
Read/write Data from/to GDDRAM	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	$(1011X_3X_2X_1X_0)$* $(0001X_3X_2X_1X_0)$* $(0000X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$

* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

9 COMMAND DESCRIPTIONS

9.1 Set Display On/Off

This command turns the display on/off, by the value of the LSB.

9.2 Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 67. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0.

9.3 Set Page Address

This command positions the page address to 0 to 8 possible positions in GDDRAM.

9.4 Set Higher Column Address

This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>95).

9.5 Set Lower Column Address

This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>95).

9.6 Set Temperature Coefficient (TC) Value

This command is to set 1 out of 4 different temperature coefficients in order to match various liquid crystal temperature grades.

9.7 Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly.

9.8 Set Normal/Reverse Display

This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an “ON” pixel while in reverse display; a RAM data of 0 indicates an “ON” pixel. The icon line is not affected by this command.

9.9 Set Entire Display On/Off

This command forces the entire display, including the icon row, to be “ON” regardless of the contents of the display data RAM. This command has priority over normal/reverse display.
To execute this command, Set Display On command must be sent in advance.

9.10 Set LCD Bias

This command selects a suitable bias ratio (1/4 to 1/9) required for driving the particular LCD panel in use. The POR is set to 1/9 bias.

9.11 Software Reset

This command causes some of the internal status of the chip to be initialized:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 3.01 (IR0)
Contrast	20H	

9.12 Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

9.13 Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three power relating sub-circuits could be turned on/off by this command.

Internal voltage booster is used to generate the highest positive voltage supply internally from the voltage input (V_{DD} -V_{SS}).

Internal regulator is used to generate the LCD driving voltage.

Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2}, V_{L3}, V_{L4}, V_{L5}) from the internal regulator output, Vout. External voltage sources should be fed into this driver if this circuit is turned off.

9.14 Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref} \qquad ,where\ Vref = 1.6V$$

9.15 Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing Vout of the LCD drive voltage provided by the On-Chip power circuits. Vout is set with 64 steps (6-bit) contrast control register. It is a compound commands:

Figure 9-1 : Contrast Control Flow Set Segment Re-map

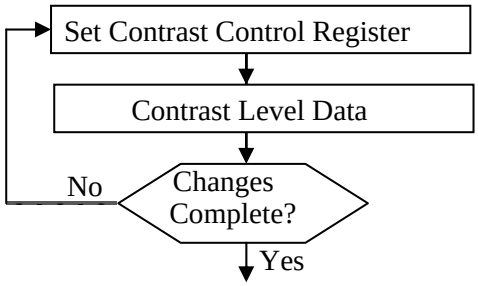
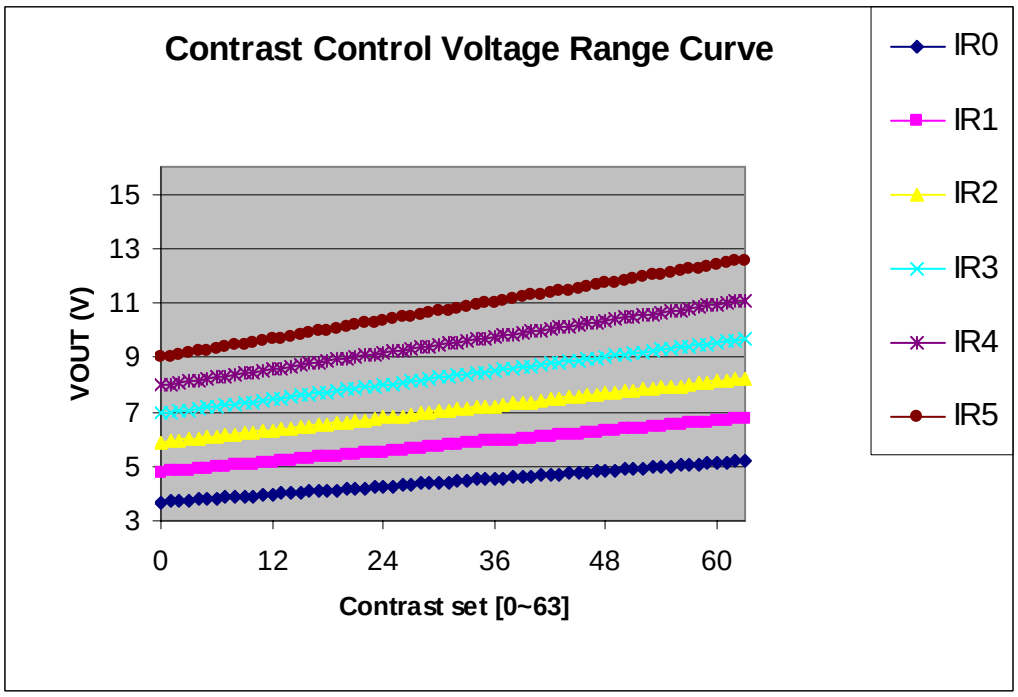


Figure 9-2 : Contrast Control Voltage Range Curve



9.16 Set Frame Frequency

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 75Hz at 68 mux after POR.

9.17 Set Multiplex Ratio

This command switches default 68 multiplex modes to any multiplex from 16 to 68, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped from 17 to 65. The chip pads ROW0-ROW67 will be switched to corresponding COM signal output as specified in Table 6-3.

9.18 Set Power Save Mode

Force the chip to enter Standby or Sleep Mode. LSB of the command will define which mode will be entered.

9.19 Exit Power Save Mode

This command releases the chip from Sleep Mode and return to normal operation.

9.20 Set N-line Inversion

Number of line inversion is set by this command for reducing crosstalk noise. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled.
It should be noted that the total number of MUX (including the icon line) should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change.

9.21 Exit N-line Inversion

This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

9.22 Set DC-DC Converter Factor

Internal DC-DC converter factor is set by this command. For SSD1829, 2X to 6X multiplying factors could be selected. 2X to 6X factors are selected using this command.

9.23 Set Icon Enable

This command enable/disable the Icon displays.

9.24 Start Internal Oscillator

After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

9.25 Set Test Mode

This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

9.26 Status Register Read

This command is issued by setting D/C Low during a data read (refer to Figure 12-2 and Figure 12-4 for the parallel interface waveforms). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

9.27 Enable external oscillator input.

This command enables the external clock input from CL pin and expected external square wave is 102kHz.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip.

9.28 OTP setting and programming

OTP (One Time Programming) is a method to adjust V_{OUT}. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules. OTP setting and programming should include two major steps. Find the OTP offset and OTP programming as following,

Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value 0x81, 0x00~0x3F until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1

Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x24
OTP offset value = 0x24 - 0x20 = +4
OTP setting command should be (0x82, 0x04)

Example 2:

Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x1B
OTP setting = 0x1B - 0x20 = -5
OTP setting command should be (0x82, 0x1B)

Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(7) Enable oscillator clk (0xAB)
(8) Connect an external V_{OUT} by closing SW1 (see diagram below)
(9) Send OTP setting commands that we find in step 1 (0x82, 0x00~0X0F)
(10) Send OTP programming command (0x83)
(11) Wait at least 2 seconds
(12) Disconnect the external Vout by opening SW1
(13) Discharge the capacitor C by closing the switch SW2 and wait for 1 second
(14) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(15) Verify the result by repeating step 1. (2) – (3)

Figure 9-3 : OTP programming circuitry

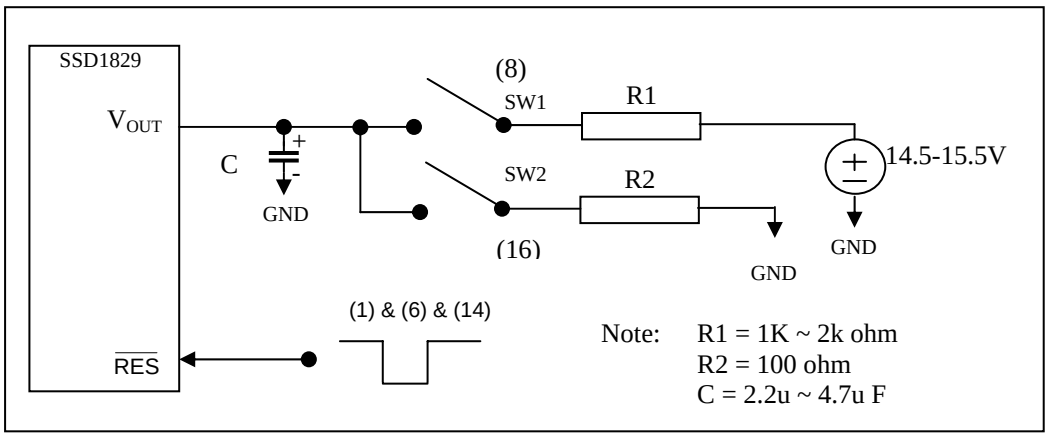
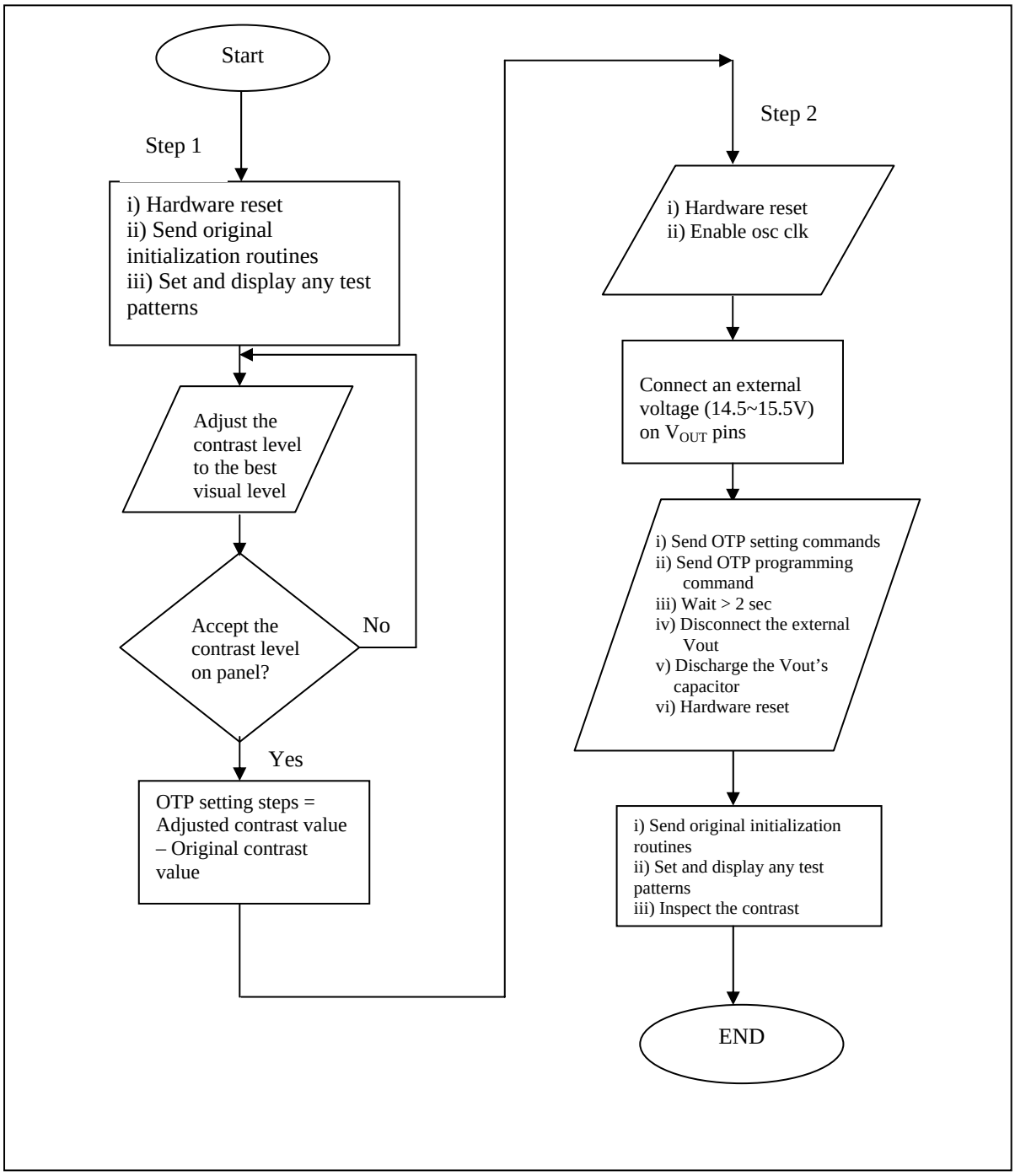


Figure 9-4 : Flow Chart of OTP Programming Procedure



OTP Example Program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. 0XAB \\ Enable internal oscillator
3. 0X55 \\ Set Biasing ratio, 1/9 for 68/64 MUX mode
   0X66 \\ Set Booster level, 5X for 68/64 MUX mode
4. 0X81 \\Set target gain and contrast.
   0X20 \\ contrast = 20 Hex.
   0X24 \\ IR4
5. \\ Set target display contents
   0x00 \\ set start column address at 0000 binary for lower nibble
   0X10 \\ set start column address at 0000 binary for upper nibble
   0XB0 \\ set page address at page 0
6. 0X2F \\ turn on the internal voltage booster & output op-amp buffer.
7. 0xAF \\ display on
8. OTP offset calculation… target OTP offset value is +6

OTP programming:

9. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
10. Enable oscillator clk (C: AB)
11. Connect a external V_{OUT} (14.5V~15.5V)
12. 0X82 \\ Set OTP offset value to +6 (0110)
    0X06 \\ 00110 $X_4X_3X_2X_1X_0$, where $X_4X_3X_2X_1X_0$ is the OTP offset value
    0X83 \\ Send the OTP programming command.
13. Wait at least 2 seconds for programming wait time.
14. Disconnect an external Vout
15. Discharge the Vout's capacitor
16. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

Verify the result:

17. After OTP programming, procedure 2 to 7 are repeated for inspection of the contrast on the panel.

Note: A proper power off sequence is reminded to avoid evitable miss-OTP, please refer P. 43- 44 for more details.

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 3.6	V
V_{DDIO}	I/O Input Voltage	-0.3 to 3.6	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{DD} , V_{DDIO} and Vout be constrained to range Vss < V_{DDIO} <= V_{DD} < Vout. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DDIO}). Unused outputs must be open. This device may be light sensitive. Caution should be taken to avoid exposure of this device any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Table 11-1 : DC Characteristics (Unless otherwise specified, Voltage Referenced to VSS, VDD = 1.8 to 3.3V, TA = -40 to 85˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Internal Circuit Voltage Supply Pin	(Absolute value referenced to V_{SS})	1.8	2.7	3.3	V
V_{DDIO}	I/O Supply Voltage Range	(Absolute value referenced to V_{SS})	1.7	-	VDD	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X DC-DC Converter Enabled, Write accessing, T_{cyc} =3.3MHz, Osc. Freq.=102kHz, Display On.	-	600	1000	uA
I_{DP1}	Display Mode Supply Current Drain (V_{DDIO} & V_{DD} Pins)	V_{DDIO} =V_{DD} = 2.7V, Voltage Generator off, external Vout Divider Enable. Read/Write Halt, Osc. Freq. = 102kHz, Display On, Vout = 10.0V.	-	40	60	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DDIO} &V_{DD} Pins)	V_{DDIO} = 1.8V, V_{DD} = 2.5V, Voltage Generator ON, 5x DC-DC Converter Enabled, Internal Vout Divider Enable. Read/Write Halt, Osc Freq. = 102kHz, Display On, Vout = 10.0V, no panel loading.	-	150	300	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, Read/Write halt and POR.	-	1	10	µA
Vout	LCD Driving Voltage Generator Output (Vout Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Regulator Enabled, Osc. Freq. = 102kHz,	4.0	-	12.0	V
	DC-DC Converter Efficiency (Without loading)	5X booster enabled	-	90	-	%
V_{LCD}	LCD Driving Voltage Input (Vout Pin)	Voltage Generator Disabled	4.0	-	12.0	V
V_{OH1}	Output High Voltage (D_0-D_7)	I_{out} = +500µA	0.8* V_{DDIO}	-	V_{DDIO}	V_{LCD}
V_{OL1}	Out Low Voltage (D_0-D_7)	I_{out} = -500µA	0	-	0.2* V_{DDIO}	V
Vout	LCD Driving Voltage Source (Vout Pin)	Regulator Enabled (Vout voltage depends on Internal contrast Control)	V_{DD}	-	12.0	V
Vout	LCD Driving Voltage Source (Vout Pin)	Regulator Disable	-	Floating	-	V
V_{IH1}	Input high voltage (/RES, PS0, PS1, /CS, D/C, R/W, D_0-D_7)		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Input low voltage (/RES, PS0, PS1, /CS, D/C, R/W, D_0-D_7)		0	-	0.2* V_{DDIO}	V
Vout	LCD Display Voltage Output	Bias Divider Enabled, 1:a bias ratio	-	V_{out}	-	V
V_{L5}	(Vout, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)		-	(a-1)/a*V_{out}	-	V
V_{L4}			-	(a-2)/a*V_{out}	-	V
V_{L3}			-	2/a*V_{out}	-	V
V_{L2}			-	1/a*V_{out}	-	V
Vout	LCD Display Voltage Input (Vout, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Voltage reference to V_{SS}, External Voltage Generator, Bias Diver Disabled	V_{L5}	-		V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{L5}			V_{L4}	-	Vout	V
V_{L4}			V_{L3}	-	V_{L5}	V
V_{L3}			V_{L2}	-	V_{L4}	V
V_{L2}			V_{SS}		V_{L3}	V
I_{OH}	Output High Current Source (D_0-D_7)	Output Voltage=V DDIO -0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D_0-D_7)	Output Voltage = 0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Source (D_0-D_7)		-1	-	1	µA
I_{IL} /I_{IH}	Input Current (RES , PS0, PS1, CS , E, D/C, R/W, D_0-D_7		-1	-	1	µA
C_{IN}	Input Capacitance (all logic pins)		-	5	7.5	PF
V_{ref}	Reference Voltage (T= 25ºC)		1.54	1.6	1.66	V
PTC3	Temperature Coefficient 3*	Voltage Regulator Enabled	0	-0.01	-0.02	%/ºC
PTC4	Temperature Coefficient 4*	Voltage Regulator Enabled	-0.02	-0.03	-0.04	%/ºC
PTC5	Temperature Coefficient 5*(POR)	Voltage Regulator Enabled	-0.04	-0.05	-0.06	%/ºC
PTC6	Temperature Coefficient 6*	Voltage Regulator Enabled	-0.07	-0.08	-0.09	%/ºC

* The formula for the temperature coefficient is:

$$TC(\%)= \frac{V_{out}\ 50ºC - V_{out}\ \text{at}\ 0ºC}{50ºC - 0ºC} \times \frac{1}{V_{out}\ \text{at}\ 25ºC} \times 100\%$$

12 AC CHARACTERISTICS

Table 12-1 : AC Characteristics (Unless otherwise specified, Voltage Referenced to VSS, VDD = 2.7V, TA = -40 to 85˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{osc}	Oscillator frequency	Display ON, Set 96 x 68 Graphic Display Mode, Icon Line Disabled	104	102	110	kHz
F_{FRM}	Frame Frequency	Display ON, Set 96 x 68 Graphic Display Mode, Icon Line Disabled	65	75	100	Hz

Table 12-2 : Parallel Timing Characteristics (TA = -40 to 85˚C, VDDIO = 1.8V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycl}	Clock Cycle Time (write cycle)	200	1000	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DS}	Write Data Setup Time	40	-	-	ns
t_{DH}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 100	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	200 200	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

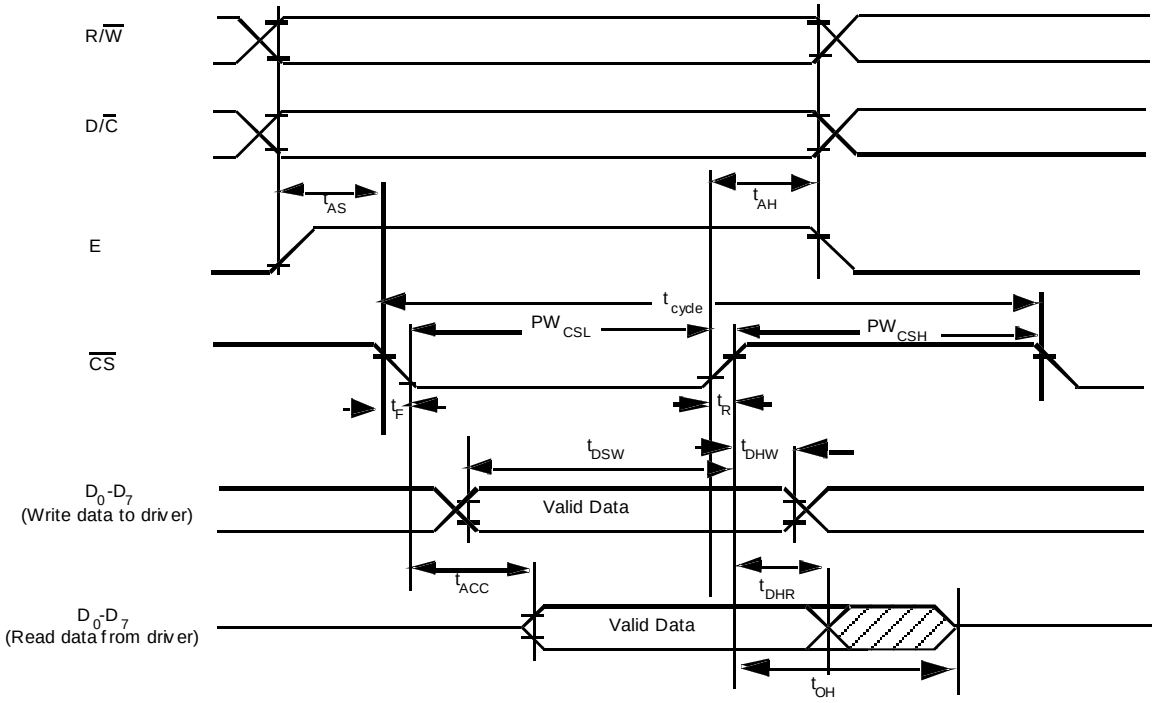


Figure 12-1 : Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 12-3 : Parallel Timing Characteristics (TA = -40 to 85˚C, VDDIO = 2.7, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycl}	Clock Cycle Time (write cycle)	100	500	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DS}	Write Data Setup Time	30	-	-	ns
t_{DH}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	100 100	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

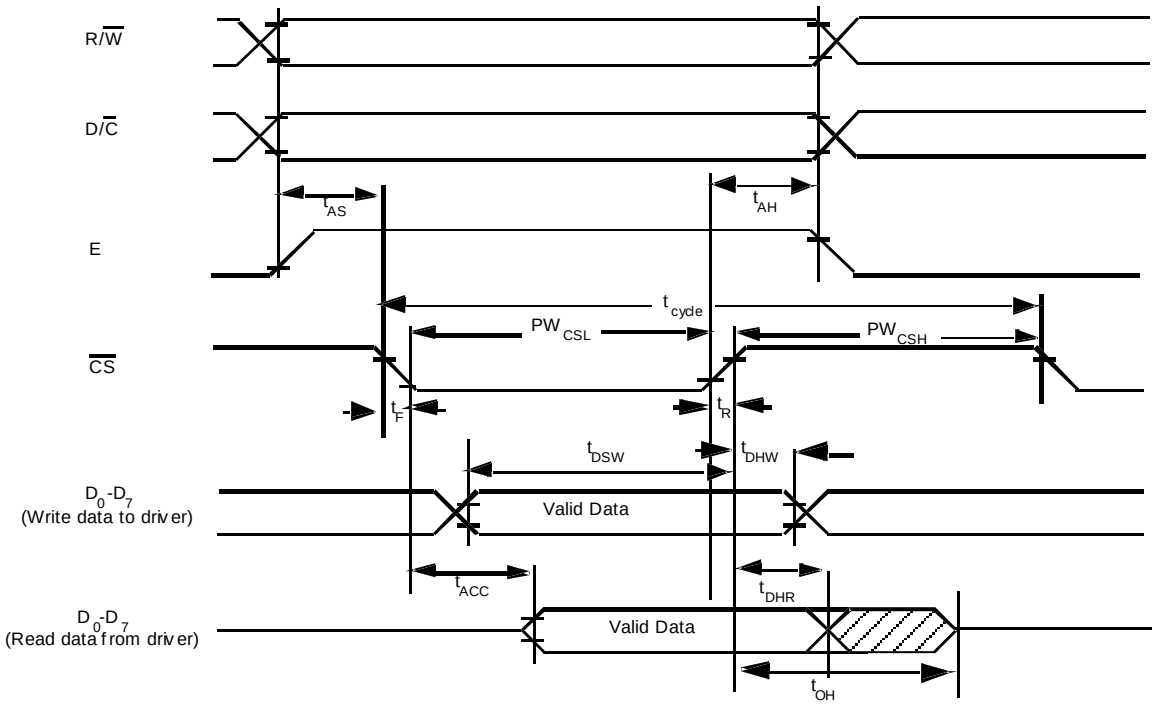


Figure 12-2 : Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 12-4 : Parallel Timing Characteristics (TA = -40 to 85˚C, VDDIO = 1.8V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycl}	Clock Cycle Time (write cycle)	200	1000	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DH}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 100	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	200 200	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

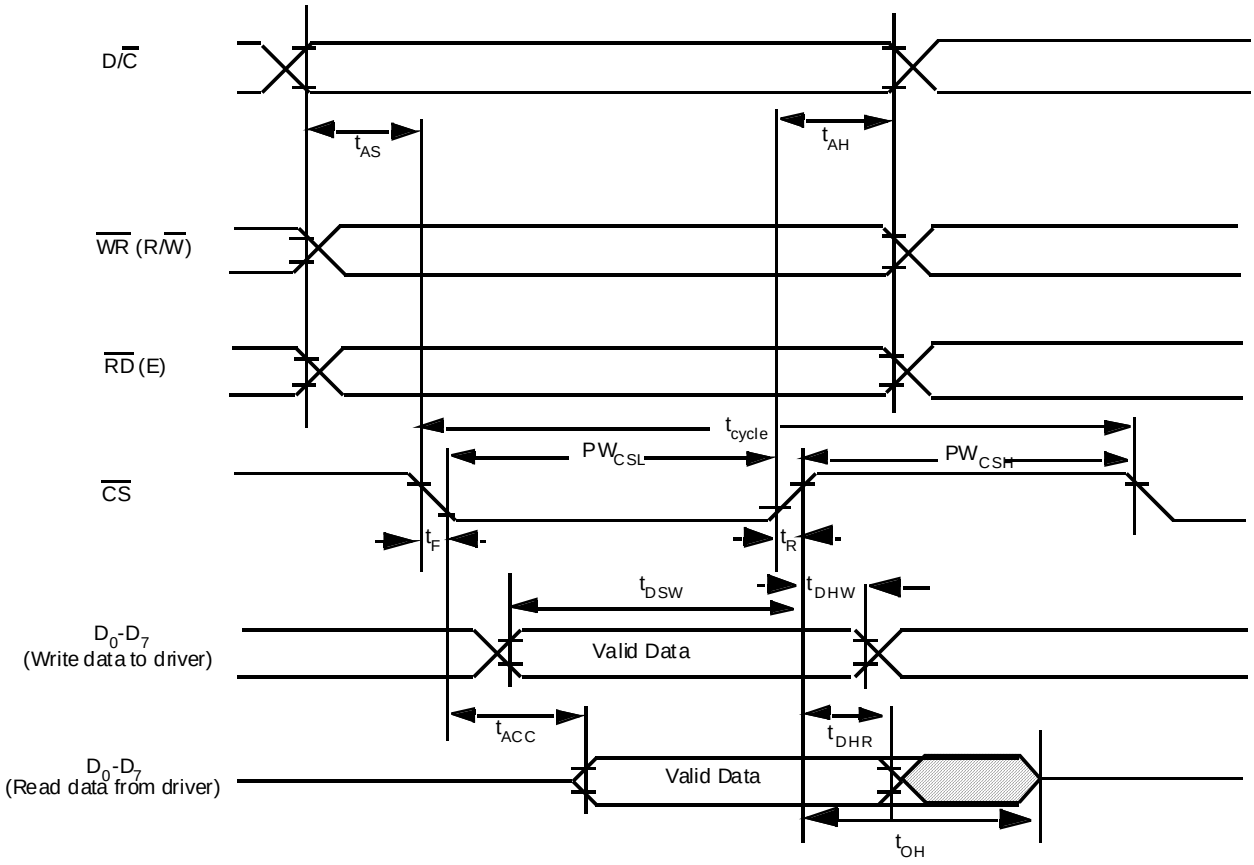


Figure 12-3 : Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 12-5 : Parallel Timing Characteristics (TA = -40 to 85˚C, VDDIO = 2.7V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cyce}	Clock Cycle Time (write cycle)	100	500	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DW}	Write Data Setup Time	30	-	-	ns
t_{DH}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	100 100	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

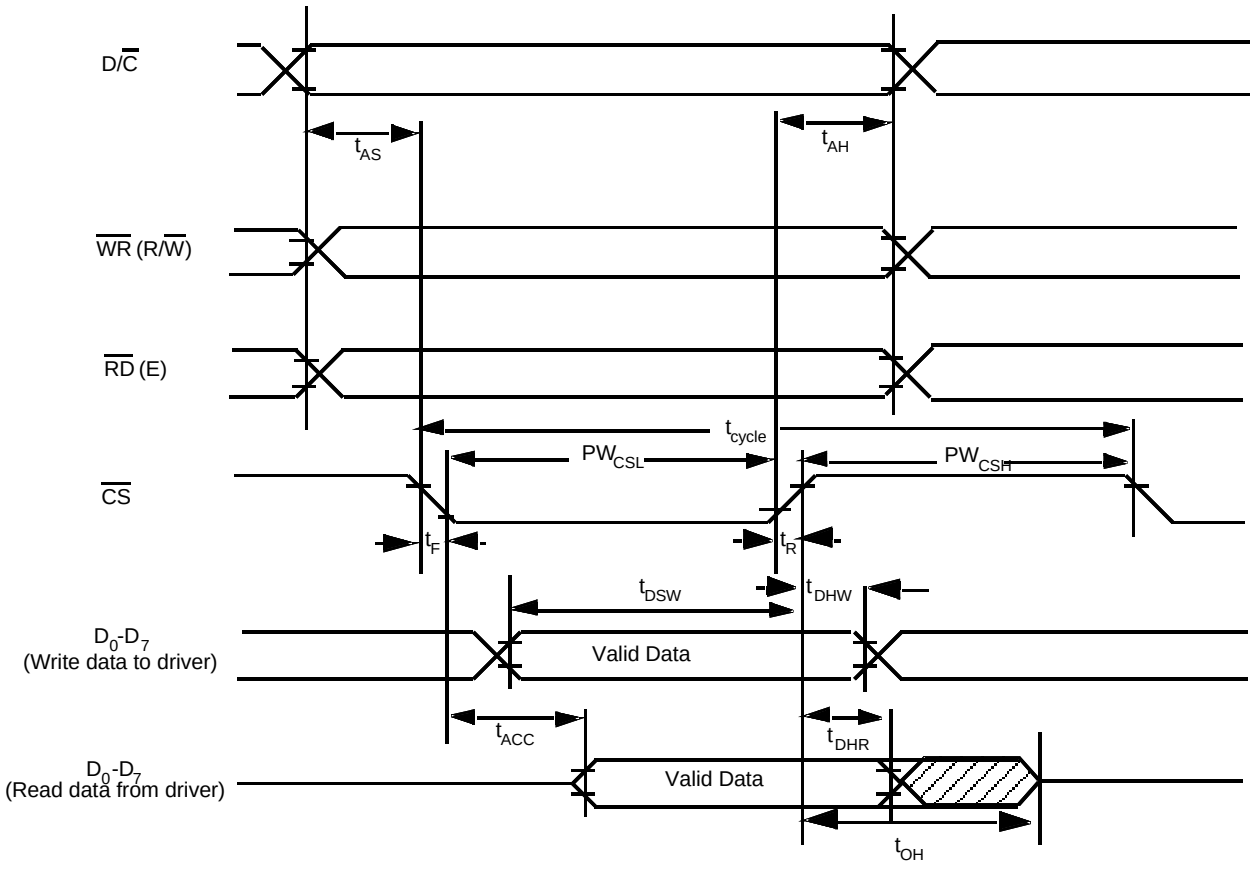


Figure 12-4 : Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 12-6 : Serial Timing Characteristics (TA = -40 to 85° C, VDDIO = 2.7V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycl}	Clock Cycle Time	58.8	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	30	-	-	ns
t_{CSH}	Chip Select Hold Time	29.4	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{OHW}	Write Data Hold Time	30	-	-	ns
t_{CLKL}	Clock Low Time	29.4	-	-	ns
t_{CLKH}	Clock High Time	29.4	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

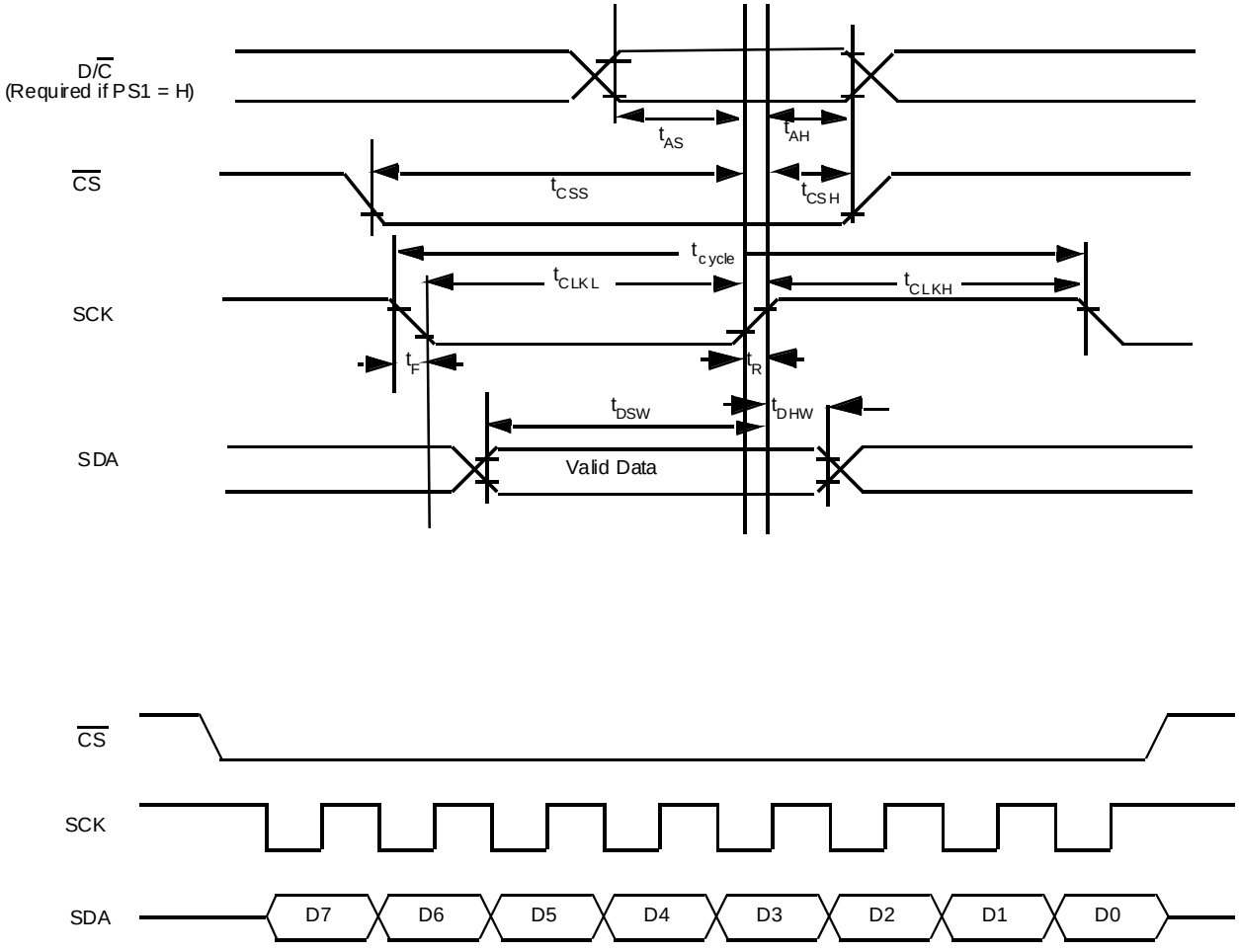


Figure 12-5 : Serial Timing Characteristics (PS0 = L)

Table 12-7 : Serial Timing Characteristics (TA = -40 to 85° C, VDDIO = 1.8V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycl}	Clock Cycle Time	111	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{CSS}	Chip Select Setup Time	60	-	-	ns
t_{CSH}	Chip Select Hold Time	55.5	-	-	ns
t_{DSW}	Write Data Setup Time	60	-	-	ns
t_{OHW}	Write Data Hold Time	60	-	-	ns
t_{CLKL}	Clock Low Time	55.5	-	-	ns
t_{CLKH}	Clock High Time	55.5	-		ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

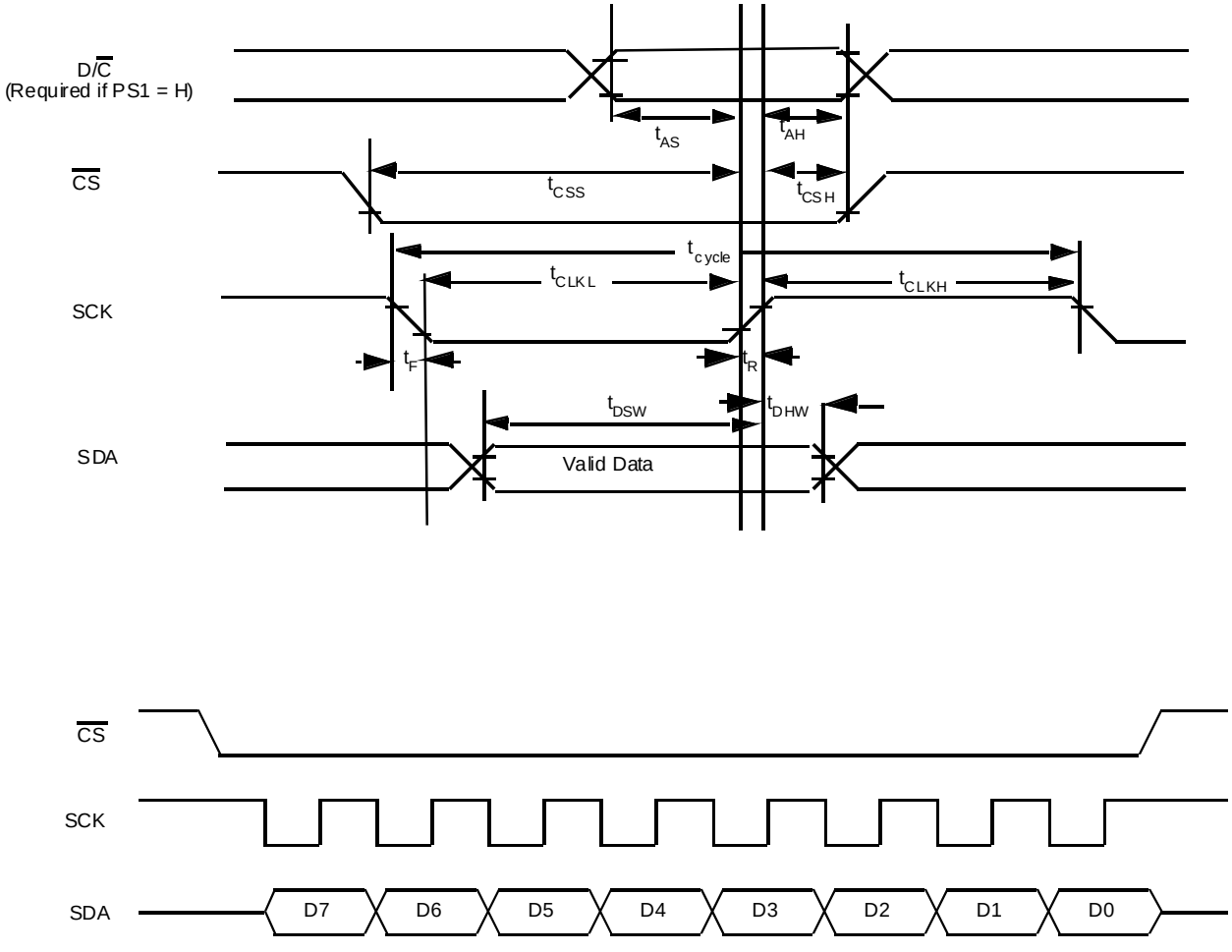
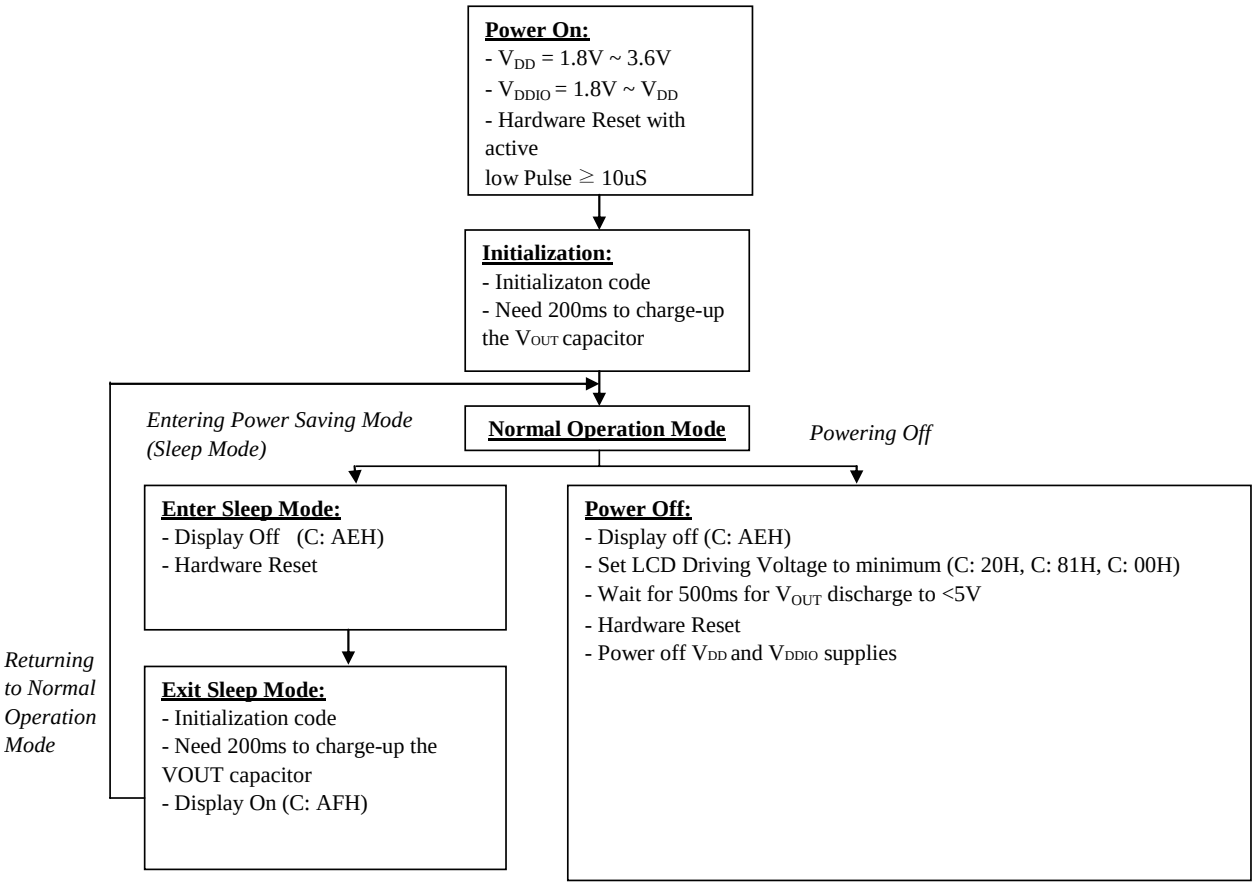


Figure 12-6 : Serial Timing Characteristics (PS0 = L)

13 POWER UP/DOWN SEQUENCE AND ENTER/EXIT POWER SAVING MODE

Abnormal Power Up/Down sequence may introduce abnormal display and cause damage to the IC driver, in order to prevent this, normal Power Up/Down Sequence are suggested. It is strongly recommended that the Normal Power Up/Down Sequence is applied when operating the chip. Also, Enter/Exit Power Saving Mode sequence are introduced for normal operation. Please refer to Figure 13-1 in P. 43.

Figure 13-1: Normal Power Up/Down Sequence and Enter/Exit Power Saving Mode Flowchart

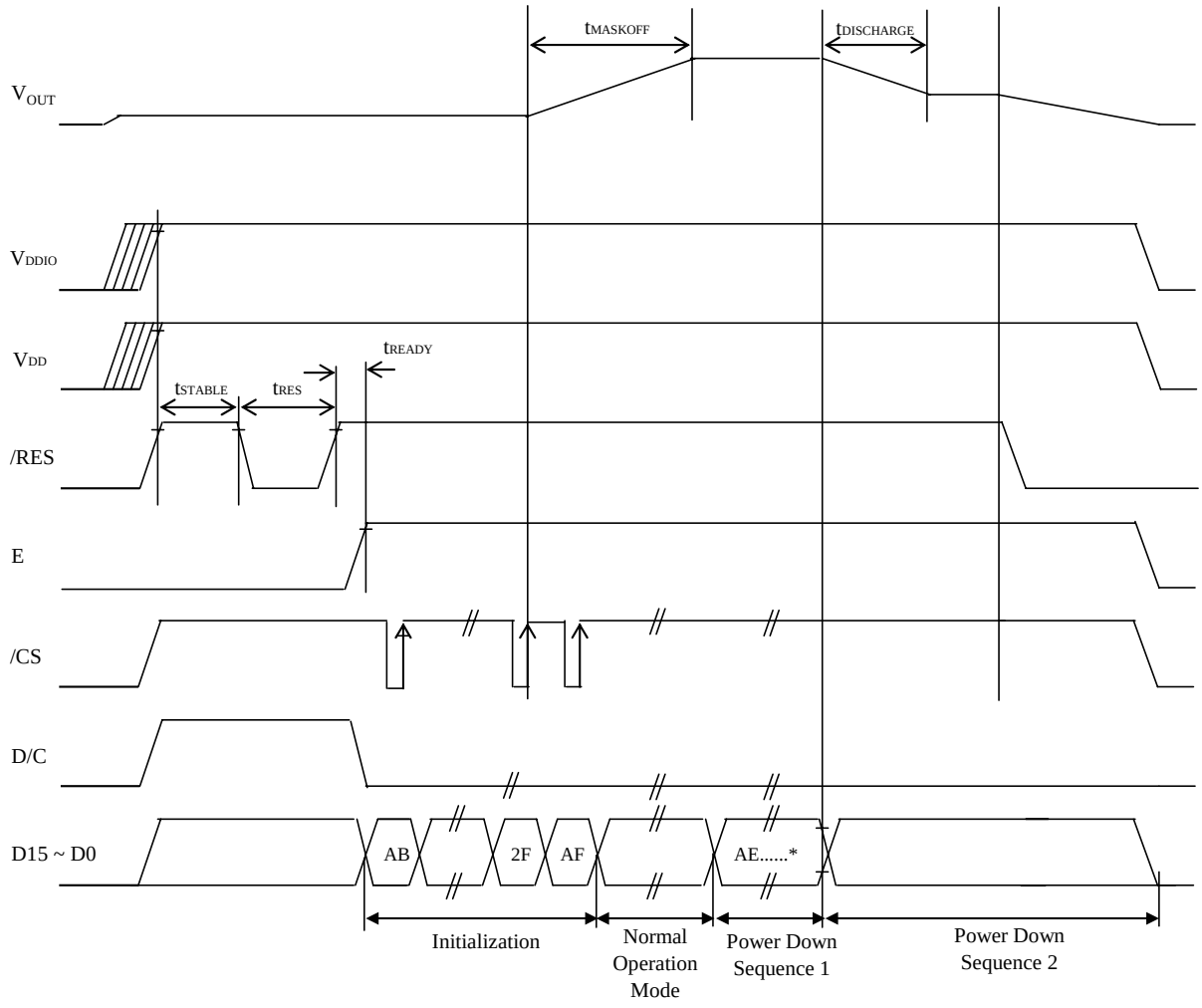


13.1 Power Up/Down Sequence

Table 13-1: Power Up/Down Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{STABLE}	Chip stable time after Power On	10	-	-	us
t_{RES}	Reset pulse width	10	-	-	us
t_{READY}	Chip need time after hardware reset	-	-	5	us
$t_{MASKOFF}$	V_{OUT} Charge up wait time	200	-	-	ms
$t_{DISCHARGE}$	V_{OUT} discharging time after enter Power Down Sequence 1*	100	500	-	ms

Figure 13-2: Power Up/Down Sequence and Timing Characteristics



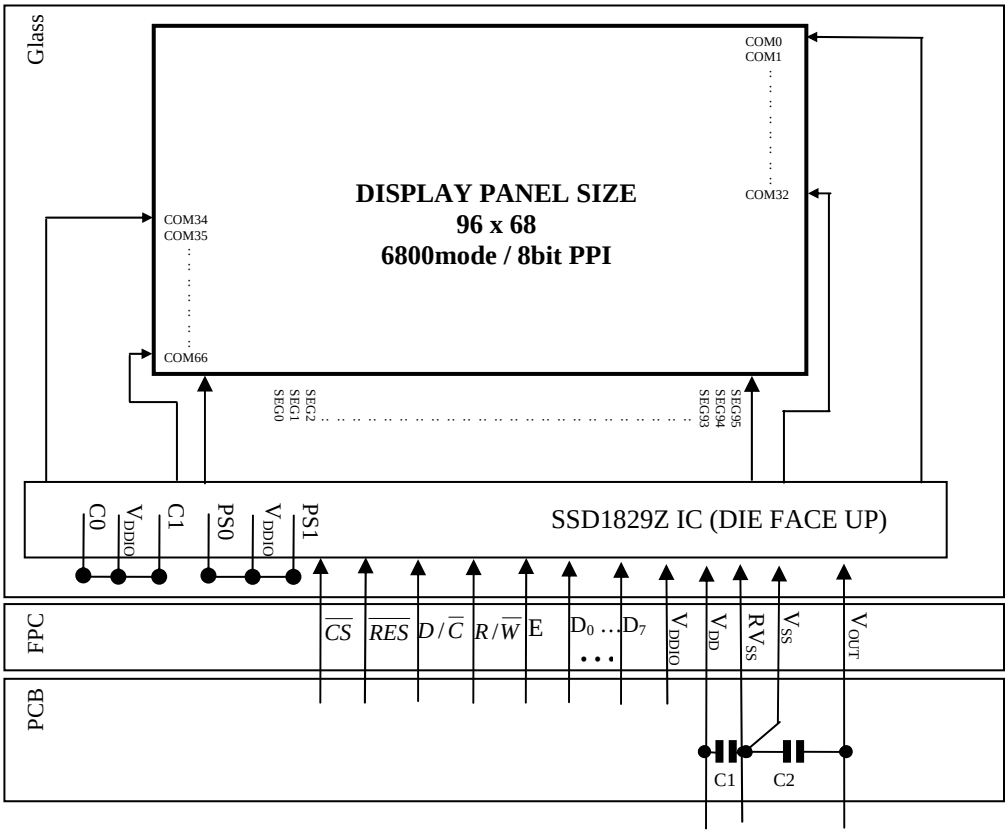
- *After LCD Driving Voltage is applied, there is 200ms mask off period that is used to provide a wait time for charging up V_{OUT} capacitors. Within the mask off period, SEGMENT and COMMON do not output any output waveforms.*
- *With regards to the Power Off, V_{OUT} should be discharged at least below than 5V before turning off the V_{DD}/V_{DDIO} power supplies.*
- **Remark: The Power Down Sequence 1 Software Program:*

C: 0XAE,	*//Display off*
C: 0X20,	*//Set internal resistor IR=0*
C: 0X81	*//Set Contrast to 0*
C: 0X00	*//Set Minimum LCD Driving Voltage*

14 APPLICATION EXAMPLES

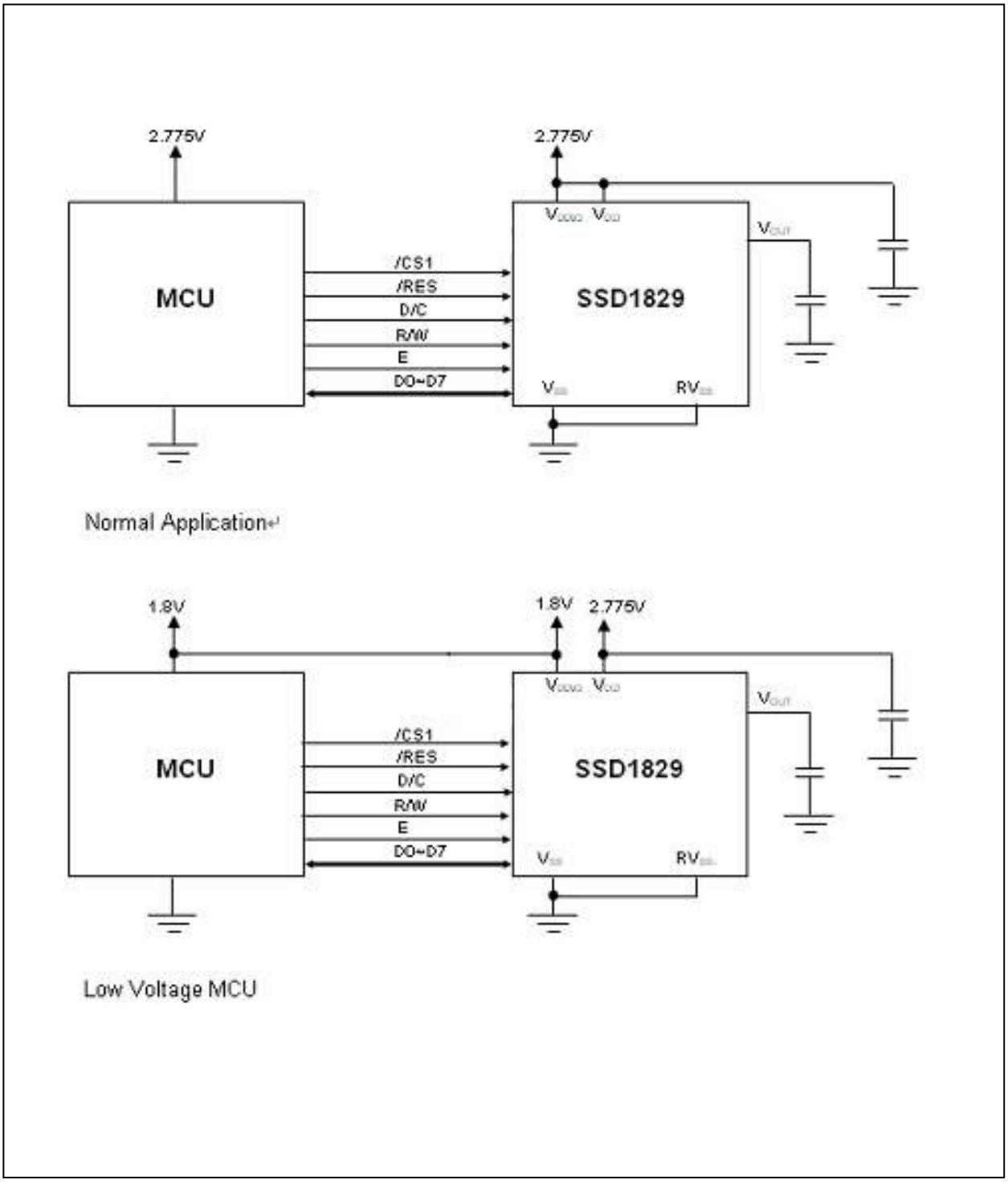
14.1 Application Diagram

Figure 14-1 : Application Examples I



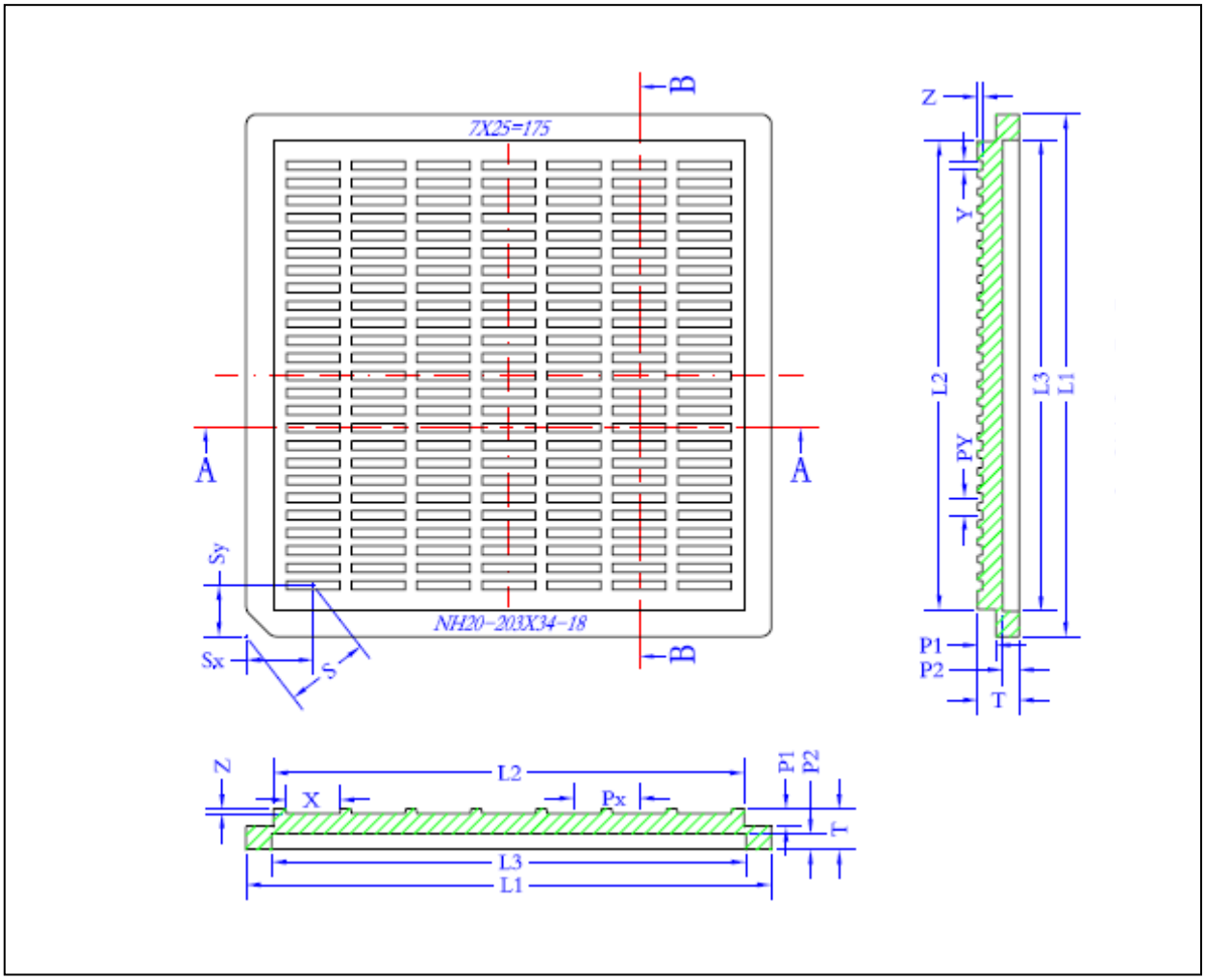
, where
C1 = 1uF ~ 2uF
C2 = 2.2uF ~4.7uF, exact capacitance value depends on ITO/ panel loading

Figure 14-2 : Application notes for V_{DD}/ V_{DDIO} connection



15 SSD1829 Die Tray Dimension

Figure 15-1 : SSD1829 Die Tray Dimension



Spec	mm	Spec	mm
L1	50.75	Z	0.46±0.05
L2	45.50	Px	6.30
L3	45.70	Px	1.70
T	4.00	Nx	7
Sx	6.48	Ny	25
Sy	4.98	N	175
S	8.17	P1	1.76
X	5.16±0.05	P2	1.60
Y	0.87±0.05		

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