

SSD1808

Product Preview

132 x 68 STN

LCD Segment / Common Monochrome Driver with Controller

This document contains information on a product under development. Solomon Systech reserves the right to change or discontinue this product without notice.

<http://www.solomon-systech.com>

SSD1808

Rev 0.20 | P 1/53 | Feb 2009

Copyright © 2009 Solomon Systech Limited



Appendix: IC Revision history of SSD1808 Specification

Version	Change Items	Effective Date
0.10	1 st Release	16-Jan-09
0.20	No Change	18-Feb-09

Confidential

CONTENTS

1	GENERAL DESCRIPTION	7
2	FEATURES.....	7
3	ORDERING INFORMATION	7
4	BLOCK DIAGRAM	8
5	DIE PAD FLOOR PLAN	9
6	PIN DESCRIPTIONS	14
7	FUNCTIONAL BLOCK DESCRIPTIONS.....	19
7.1	MICROPROCESSOR INTERFACE LOGIC	19
7.2	RESET CIRCUIT	20
7.3	5V IO REGULATOR.....	21
7.4	COMMAND DECODER AND COMMAND INTERFACE.....	21
7.5	GRAPHIC DISPLAY DATA RAM (GDDRAM).....	21
7.6	LCD DRIVING VOLTAGE GENERATOR AND REGULATOR	23
7.7	OSCILLATOR CIRCUIT	24
7.8	DISPLAY DATA LATCH	24
7.9	LEVEL SELECTOR	24
7.10	LCD PANEL DRIVING WAVEFORM.....	24
8	COMMAND TABLE	26
9	COMMAND DESCRIPTIONS.....	31
9.1	FUNDAMENTAL COMMAND	31
9.1.1	<i>Data Read / Write</i>	<i>31</i>
9.1.2	<i>Set Lower Column Address.....</i>	<i>31</i>
9.1.3	<i>Set Higher Column Address.....</i>	<i>31</i>
9.1.4	<i>Set Internal Gain Resistors Ratio.....</i>	<i>31</i>
9.1.5	<i>Set Power Control Register.....</i>	<i>31</i>
9.1.6	<i>Set Display Start Line</i>	<i>31</i>
9.1.7	<i>Set Contrast Control Register</i>	<i>33</i>
9.1.8	<i>Set Segment Re-map.....</i>	<i>33</i>
9.1.9	<i>Set LCD Bias.....</i>	<i>33</i>
9.1.10	<i>Set Entire Display On/Off.....</i>	<i>33</i>
9.1.11	<i>Set Normal/Reverse Display</i>	<i>33</i>
9.1.12	<i>Set Display On/Off.....</i>	<i>33</i>
9.1.13	<i>Set Page Address</i>	<i>33</i>
9.1.14	<i>Set COM Output Scan Direction.....</i>	<i>33</i>
9.1.15	<i>Set Read-Modify-Write Mode.....</i>	<i>34</i>
9.1.16	<i>Software Reset.....</i>	<i>34</i>
9.1.17	<i>Set End of Read-Modify-Write Mode</i>	<i>34</i>
9.1.18	<i>Set Indicator On/Off.....</i>	<i>34</i>
9.1.19	<i>Set Power Save Mode.....</i>	<i>34</i>
9.1.20	<i>NOP</i>	<i>34</i>
9.2	EXTENDED COMMAND.....	35
9.2.1	<i>OTP setting and programming</i>	<i>35</i>
9.2.2	<i>Set Bias Ratio.....</i>	<i>37</i>
9.2.3	<i>Set Temperature Coefficient (TC) Value.....</i>	<i>37</i>
9.2.4	<i>Modify Oscillator Frequency.....</i>	<i>37</i>

9.2.5	<i>Set Icon Enabled</i>	37
9.2.6	<i>Set Total Frame Phases</i>	38
9.2.7	<i>Set Test Mode</i>	38
9.3	READ STATUS COMMAND.....	38
9.3.1	<i>Status register Read</i>	38
10	MAXIMUM RATINGS	39
11	DC CHARACTERISTICS	40
12	AC CHARACTERISTICS	42
13	APPLICATION EXAMPLES	49
13.1	APPLICATION DIAGRAM.....	49
13.2	INITIALIZATION PROGRAM.....	51
14	PACKAGE INFORMATION	52
14.1	DIE TRAY DIMENSIONS.....	52

Confidential

TABLES

TABLE 6-1 : POWER SUPPLY PIN DESCRIPTION.....	14
TABLE 6-2: LCD DRIVER SUPPLY PIN DESCRIPTION.....	14
TABLE 6-3: SYSTEM CONTROL PIN DESCRIPTION.....	15
TABLE 6-4: MCU INTERFACE PIN DESCRIPTION	16
TABLE 6-5: LCD DRIVER OUTPUT PIN DESCRIPTION	17
TABLE 6-6: MISCELLANEOUS PIN DESCRIPTION.....	17
TABLE 6-7: ARRANGEMENT OF COMMON AT DIFFERENT MULTIPLEX MODES.....	18
TABLE 7-1: DATA BUS SELECTION MODES	20
TABLE 7-2: 5V IO REGULATOR PIN DESCRIPTION	21
TABLE 7-3: GRAPHIC DISPLAY DATA RAM (GDDRAM) ADDRESS MAP.....	22
TABLE 8-1 : COMMAND TABLE (R/W (/WR) = 0, E= 1 (/RD= 1) UNLESS SPECIFIC SETTING IS STATED).....	26
TABLE 8-2 : EXTENDED COMMAND TABLE (R/W (/WR) = 0, E= 1 (/RD = 1) UNLESS SPECIFIC SETTING IS STATED).....	28
TABLE 8-3 : READ COMMAND TABLE(R/W (/WR) = 1, E= 1 (/RD = 0) UNLESS SPECIFIC SETTING IS STATED).....	30
TABLE 9-1: AUTOMATIC ADDRESS INCREMENT	31
TABLE 9-2: GRAPHIC DISPLAY DATA RAM (GDDRAM) ADDRESS MAO WITH DISPLAY START LINE SET TO 18H.....	32
TABLE 10-1 : MAXIMUM RATINGS (VOLTAGE REFERENCED TO V _{SS}).....	39
TABLE 11-1 : DC CHARACTERISTICS.....	40
TABLE 12-1 : AC CHARACTERISTICS.....	42
TABLE 12-2: PARALLEL TIMING CHARACTERISTICS (TA = -40 to 85 ° C, VDDIO = 2.4V, VSS =0V).....	43
TABLE 12-3 : PARALLEL TIMING CHARACTERISTICS (TA = -40 to 85 ° C, VDDIO = 2.7, VSS =0V).....	44
TABLE 12-4 : PARALLEL TIMING CHARACTERISTICS (TA = -40 to 85 ° C, VDDIO = 2.4V, VSS =0V).....	45
TABLE 12-5 : PARALLEL TIMING CHARACTERISTICS (TA = -40 to 85 ° C, VDDIO = 2.7V, VSS =0V).....	46
TABLE 12-6 : SERIAL TIMING CHARACTERISTICS (TA = -40 to 85 ° C, VDDIO = 2.4V, VSS =0V).....	47
TABLE 12-7 : SERIAL TIMING CHARACTERISTICS (TA = -40 to 85 ° C, VDDIO = 2.7V, VSS =0V).....	48

Confidential

FIGURES

FIGURE 4-1 : SSD1808 BLOCK DIAGRAM.....	8
FIGURE 7-1: DISPLAY DATA READ WITH THE INSERTION OF DUMMY READ.....	19
FIGURE 7-2: VOLTAGE REGULATOR CIRCUIT	23
FIGURE 7-3: CONTRAST CURVE	24
FIGURE 7-4: LCD DRIVING WAVEFORM	25
FIGURE 9-1: CONTRAST CONTROL FLOW	33
FIGURE 9-2: OTP PROGRAMMING CIRCUITRY	35
FIGURE 9-3: FLOW CHART OF OTP PROGRAMMING PROCEDURE	36
FIGURE 12-1 : PARALLEL 6800-SERIES INTERFACE TIMING CHARACTERISTICS (PS0 = H, PS1 = H)	43
FIGURE 12-2 : PARALLEL 6800-SERIES INTERFACE TIMING CHARACTERISTICS (PS0 = H, PS1 = H)	44
FIGURE 12-3 : PARALLEL 8080-SERIES INTERFACE TIMING CHARACTERISTICS (PS0 = H, PS1 = L).....	45
FIGURE 12-4 : PARALLEL 8080-SERIES INTERFACE TIMING CHARACTERISTICS (PS0 = H, PS1 = L).....	46
FIGURE 12-5 : SERIAL TIMING CHARACTERISTICS (PS0 = L).....	47
FIGURE 12-6 : SERIAL TIMING CHARACTERISTICS (PS0 = L).....	48
FIGURE 13-1 : APPLICATION EXEMPLE I (3V IO APPLICATION).....	49
FIGURE 13-2 : APPLICATION EXEMPLE II (5V IO APPLICATION)	50

Confidential

1 GENERAL DESCRIPTION

SSD1808 is a single-chip CMOS LCD driver with controller for dot-matrix graphic liquid crystal display system. SSD1808 consists of 200 high-voltage driving output pins for driving maximum 132 Segments, 68 Commons / 132 Segments, 64 Commons and 1 icon-driving Common / 132 Segments, 48 Commons and 1 icon-driving Common / 132 Segments, 32 Commons and 1 icon-driving Common. SSD1808 can be switched among 32, 48, 64 or 68 display multiplex ratios by hardware pin selection.

SSD1808 consists of 132 x 68 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 8-bit 6800-series / 8080-series compatible Parallel Interface or 4-wires Serial Peripheral Interface by hardware pin selection.

SSD1808 embeds DC-DC Converter, On-Chip Oscillator and Bias Divider to reduce the number of external components. With the advance design, low power consumption, stable LCD operating voltage and flexible die package layout, SSD1808 is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- Power Supply (2 options): [3V I/O application]VDD=VDDIO=2.4-3.6V
or
[5V I/O application]VDDIO=4.5-5.5V, VDD outputs 3V in this option
- LCD Driving Output Voltage: $V_{LCD} = +12V$
- Low Current Sleep Mode
- Pin Selectable 68/64+1/48+1/32+1 Multiplex Ratio and Programmable Bias Ratio Configuration:

Duty ratio	Applicable LCD bias	Maximum display area
1/68	1/7 or 1/9	132 x 68
1/(64+1)	1/7 or 1/9	132 x 65
1/(48+1)	1/6 or 1/8	132 x 49
1/(32+1)	1/5 or 1/6	132 x 33

- 8-bit 6800-series/ 8080-series Parallel Interface, 4-wires Serial Peripheral Interface
- On-Chip 132 x 68 = 8,976bits Graphic Display Data RAM
- On-Chip Oscillator Circuit
- On-Chip DC-DC Converter: 4X – 5X
- 64 Levels Internal Contrast Control
- Programmable LCD Driving Voltage Temperature Compensation Coefficients
- On-Chip Bias Divider with internal compensation capacitors (except VOUT)
- Column Re-mapping and RAM Page Scan Direction Control
- Vertical Scrolling by Common
- Display Offset Control
- Non- Volatile Memory (OTP) for calibration

3 ORDERING INFORMATION

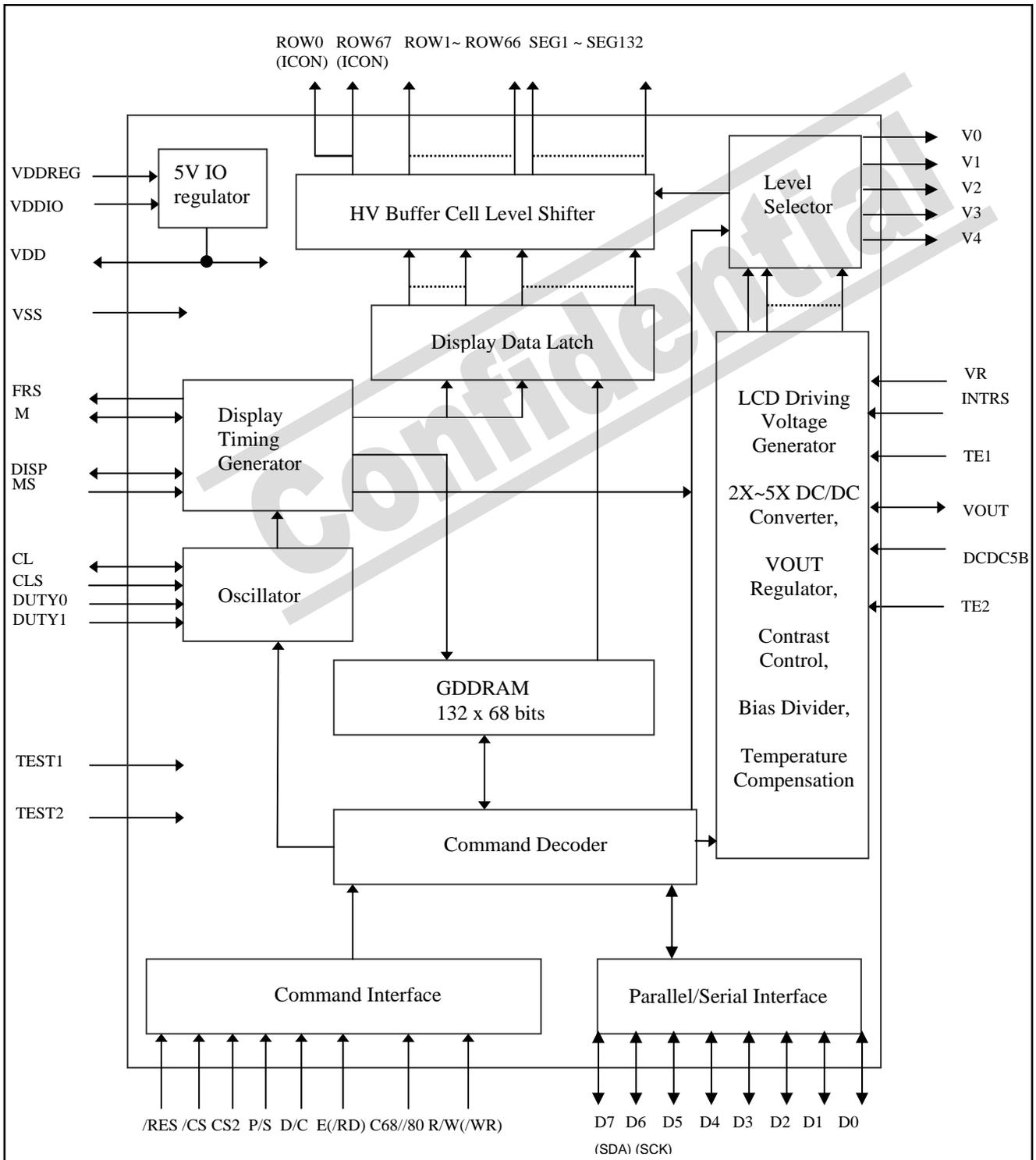
Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1808Z	132	64/48/32 + 1 icon or 68	Gold Bump Die	Figure 5-1 on P.9	-

4

BLOCK DIAGRAM

Figure 4-1 : SSD1808 Block Diagram



Confidential

Table 5-1: SSD1808 Bump Die Pad Coordinates (Bump center)

Pad#	Pad Name	X-pos	Y-pos	Pad#	Pad Name	X-pos	Y-pos	Pad#	Pad Name	X-pos	Y-pos
1	DUMMY	-3232.5	-331.5	49	DUTY1	-825	-331.5	97	NC	1575	-331.5
2	FRS	-3175	-331.5	50	VSS	-775	-331.5	98	NC	1625	-331.5
3	M	-3125	-331.5	51	MS	-725	-331.5	99	NC	1675	-331.5
4	CL	-3075	-331.5	52	CLS	-675	-331.5	100	NC	1725	-331.5
5	DISP	-3025	-331.5	53	VDDIO	-625	-331.5	101	NC	1775	-331.5
6	DUMMY	-2975	-331.5	54	C68/80	-575	-331.5	102	NC	1825	-331.5
7	NC	-2925	-338	55	P/S	-525	-331.5	103	NC	1875	-331.5
8	NC	-2875	-338	56	VSS	-475	-331.5	104	VSS	1925	-331.5
9	NC	-2825	-338	57	VSS	-425	-331.5	105	VSS	1975	-331.5
10	NC	-2775	-338	58	VSS	-375	-331.5	106	VR	2025	-331.5
11	NC	-2725	-338	59	VSS	-325	-331.5	107	VR	2075	-331.5
12	NC	-2675	-338	60	VSS	-275	-331.5	108	V0	2125	-331.5
13	NC	-2625	-338	61	VSS	-225	-331.5	109	V0	2175	-331.5
14	NC	-2575	-338	62	VSS	-175	-331.5	110	V1	2225	-331.5
15	NC	-2525	-338	63	VSS	-125	-331.5	111	V1	2275	-331.5
16	NC	-2475	-338	64	VSS	-75	-331.5	112	V2	2325	-331.5
17	NC	-2425	-338	65	VSS	-25	-331.5	113	V2	2375	-331.5
18	NC	-2375	-338	66	VDDIO	25	-331.5	114	V3	2425	-331.5
19	NC	-2325	-338	67	VDDIO	75	-331.5	115	V3	2475	-331.5
20	NC	-2275	-338	68	VDDIO	125	-331.5	116	V4	2525	-331.5
21	NC	-2225	-338	69	VDD	175	-331.5	117	V4	2575	-331.5
22	NC	-2175	-338	70	VDD	225	-331.5	118	VSS	2625	-331.5
23	NC	-2125	-338	71	VDD	275	-331.5	119	VSS	2675	-331.5
24	NC	-2075	-338	72	VDD	325	-331.5	120	TE1	2725	-331.5
25	NC	-2025	-338	73	VDD	375	-331.5	121	DCDC5B	2775	-331.5
26	DUMMY	-1975	-331.5	74	VDD	425	-331.5	122	VDDIO	2825	-331.5
27	VSS	-1925	-331.5	75	VDD	475	-331.5	123	TE2	2875	-331.5
28	/CS	-1875	-331.5	76	VOUT	525	-331.5	124	INTRS	2925	-331.5
29	CS2	-1825	-331.5	77	VOUT	575	-331.5	125	VSS	2975	-331.5
30	VDDIO	-1775	-331.5	78	VOUT	625	-331.5	126	TEST2	3025	-331.5
31	/RES	-1725	-331.5	79	VOUT	675	-331.5	127	VDDIO	3075	-331.5
32	D/C	-1675	-331.5	80	NC	725	-331.5	128	VDDREG	3125	-331.5
33	VSS	-1625	-331.5	81	NC	775	-331.5	129	VSS	3175	-331.5
34	R/W(/WR)	-1575	-331.5	82	NC	825	-331.5	130	DUMMY	3232.5	-331.5
35	E(/RD)	-1525	-331.5	83	NC	875	-331.5	131	DUMMY	3260	-236.5
36	VDDIO	-1475	-331.5	84	NC	925	-331.5	132	ROW0	3260	-189
37	D0	-1425	-331.5	85	NC	975	-331.5	133	ROW1	3260	-156
38	D1	-1375	-331.5	86	NC	1025	-331.5	134	ROW2	3260	-123
39	D2	-1325	-331.5	87	NC	1075	-331.5	135	ROW3	3260	-90
40	D3	-1275	-331.5	88	NC	1125	-331.5	136	ROW4	3260	-57
41	D4	-1225	-331.5	89	NC	1175	-331.5	137	ROW5	3260	-24
42	D5	-1175	-331.5	90	NC	1225	-331.5	138	DUMMY	3260	23.5
43	D6(SCK)	-1125	-331.5	91	NC	1275	-331.5	139	DUMMY	3202	328.5
44	D7(SDA)	-1075	-331.5	92	NC	1325	-331.5	140	ROW6	3154.5	328.5
45	TEST1	-1025	-331.5	93	NC	1375	-331.5	141	ROW7	3121.5	328.5
46	VSS	-975	-331.5	94	NC	1425	-331.5	142	ROW8	3088.5	328.5
47	VDDIO	-925	-331.5	95	NC	1475	-331.5	143	ROW9	3055.5	328.5
48	DUTY0	-875	-331.5	96	NC	1525	-331.5	144	ROW10	3022.5	328.5

Pad#	Pad Name	X-pos	Y-pos	Pad#	Pad Name	X-pos	Y-pos	Pad#	Pad Name	X-pos	Y-pos
145	ROW11	2989.5	328.5	193	SEG27	1386	328.5	241	SEG72	-198	328.5
146	ROW12	2956.5	328.5	194	SEG28	1353	328.5	242	SEG73	-231	328.5
147	ROW13	2923.5	328.5	195	SEG29	1320	328.5	243	SEG74	-264	328.5
148	ROW14	2890.5	328.5	196	SEG30	1287	328.5	244	SEG75	-297	328.5
149	ROW15	2857.5	328.5	197	SEG31	1254	328.5	245	SEG76	-330	328.5
150	ROW16	2824.5	328.5	198	SEG32	1221	328.5	246	SEG77	-363	328.5
151	ROW17	2791.5	328.5	199	SEG33	1188	328.5	247	SEG78	-396	328.5
152	ROW18	2758.5	328.5	200	SEG34	1155	328.5	248	SEG79	-429	328.5
153	ROW19	2725.5	328.5	201	SEG35	1122	328.5	249	SEG80	-462	328.5
154	ROW20	2692.5	328.5	202	SEG36	1089	328.5	250	SEG81	-495	328.5
155	ROW21	2659.5	328.5	203	SEG37	1056	328.5	251	SEG82	-528	328.5
156	ROW22	2626.5	328.5	204	SEG38	1023	328.5	252	SEG83	-561	328.5
157	ROW23	2593.5	328.5	205	SEG39	990	328.5	253	SEG84	-594	328.5
158	ROW24	2560.5	328.5	206	SEG40	957	328.5	254	SEG85	-627	328.5
159	ROW25	2527.5	328.5	207	SEG41	924	328.5	255	SEG86	-660	328.5
160	ROW26	2494.5	328.5	208	SEG42	891	328.5	256	SEG87	-693	328.5
161	ROW27	2461.5	328.5	209	SEG43	858	328.5	257	SEG88	-726	328.5
162	ROW28	2428.5	328.5	210	SEG44	825	328.5	258	SEG89	-759	328.5
163	ROW29	2395.5	328.5	211	SEG45	792	328.5	259	SEG90	-792	328.5
164	ROW30	2362.5	328.5	212	SEG46	759	328.5	260	SEG91	-825	328.5
165	ROW31	2329.5	328.5	213	SEG47	726	328.5	261	SEG92	-858	328.5
166	ROW32	2296.5	328.5	214	SEG48	693	328.5	262	SEG93	-891	328.5
167	SEG1	2244	328.5	215	SEG49	660	328.5	263	SEG94	-924	328.5
168	SEG2	2211	328.5	216	SEG50	627	328.5	264	SEG95	-957	328.5
169	SEG3	2178	328.5	217	SEG51	594	328.5	265	SEG96	-990	328.5
170	SEG4	2145	328.5	218	SEG52	561	328.5	266	SEG97	-1023	328.5
171	SEG5	2112	328.5	219	SEG53	528	328.5	267	SEG98	-1056	328.5
172	SEG6	2079	328.5	220	SEG54	495	328.5	268	SEG99	-1089	328.5
173	SEG7	2046	328.5	221	SEG55	462	328.5	269	SEG100	-1122	328.5
174	SEG8	2013	328.5	222	SEG56	429	328.5	270	SEG101	-1155	328.5
175	SEG9	1980	328.5	223	SEG57	396	328.5	271	SEG102	-1188	328.5
176	SEG10	1947	328.5	224	SEG58	363	328.5	272	SEG103	-1221	328.5
177	SEG11	1914	328.5	225	SEG59	330	328.5	273	SEG104	-1254	328.5
178	SEG12	1881	328.5	226	SEG60	297	328.5	274	SEG105	-1287	328.5
179	SEG13	1848	328.5	227	SEG61	264	328.5	275	SEG106	-1320	328.5
180	SEG14	1815	328.5	228	SEG62	231	328.5	276	SEG107	-1353	328.5
181	SEG15	1782	328.5	229	SEG63	198	328.5	277	SEG108	-1386	328.5
182	SEG16	1749	328.5	230	SEG64	165	328.5	278	SEG109	-1419	328.5
183	SEG17	1716	328.5	231	SEG65	132	328.5	279	SEG110	-1452	328.5
184	SEG18	1683	328.5	232	SEG66	99	328.5	280	SEG111	-1485	328.5
185	SEG19	1650	328.5	233	DUMMY	66	328.5	281	SEG112	-1518	328.5
186	SEG20	1617	328.5	234	DUMMY	33	328.5	282	SEG113	-1551	328.5
187	SEG21	1584	328.5	235	DUMMY	0	328.5	283	SEG114	-1584	328.5
188	SEG22	1551	328.5	236	SEG67	-33	328.5	284	SEG115	-1617	328.5
189	SEG23	1518	328.5	237	SEG68	-66	328.5	285	SEG116	-1650	328.5
190	SEG24	1485	328.5	238	SEG69	-99	328.5	286	SEG117	-1683	328.5
191	SEG25	1452	328.5	239	SEG70	-132	328.5	287	SEG118	-1716	328.5
192	SEG26	1419	328.5	240	SEG71	-165	328.5	288	SEG119	-1749	328.5

Pad#	Pad Name	X-pos	Y-pos
289	SEG120	-1782	328.5
290	SEG121	-1815	328.5
291	SEG122	-1848	328.5
292	SEG123	-1881	328.5
293	SEG124	-1914	328.5
294	SEG125	-1947	328.5
295	SEG126	-1980	328.5
296	SEG127	-2013	328.5
297	SEG128	-2046	328.5
298	SEG129	-2079	328.5
299	SEG130	-2112	328.5
300	SEG131	-2145	328.5
301	SEG132	-2178	328.5
302	ROW67	-2230.5	328.5
303	ROW66	-2263.5	328.5
304	ROW65	-2296.5	328.5
305	ROW64	-2329.5	328.5
306	ROW63	-2362.5	328.5
307	ROW62	-2395.5	328.5
308	ROW61	-2428.5	328.5
309	ROW60	-2461.5	328.5
310	ROW59	-2494.5	328.5
311	ROW58	-2527.5	328.5
312	ROW57	-2560.5	328.5
313	ROW56	-2593.5	328.5
314	ROW55	-2626.5	328.5
315	ROW54	-2659.5	328.5
316	ROW53	-2692.5	328.5
317	ROW52	-2725.5	328.5
318	ROW51	-2758.5	328.5
319	ROW50	-2791.5	328.5
320	ROW49	-2824.5	328.5
321	ROW48	-2857.5	328.5
322	ROW47	-2890.5	328.5
323	ROW46	-2923.5	328.5
324	ROW45	-2956.5	328.5
325	ROW44	-2989.5	328.5
326	ROW43	-3022.5	328.5
327	ROW42	-3055.5	328.5
328	ROW41	-3088.5	328.5
329	ROW40	-3121.5	328.5
330	ROW39	-3154.5	328.5
331	DUMMY	-3202	328.5
332	DUMMY	-3260	23.5
333	ROW38	-3260	-24
334	ROW37	-3260	-57
335	ROW36	-3260	-90
336	ROW35	-3260	-123
337	ROW34	-3260	-156
338	ROW33	-3260	-189
339	DUMMY	-3260	-236.5

Bump Size

Pad #	X [um]	Y [um]	Pad pitch [um] (Min)
1	50	80	57.5
2-6	32	80	50
7-25	30	67	50
26-129	32	80	50
130	50	80	57.5
131	86	50	47.5
132-137	86	18	33
138	86	50	47.5
139	50	86	47.5
140-166, 167-301, 302-330	18	86	33
331	50	86	47.5
332	86	50	47.5
333-338	86	18	33
339	86	50	47.5

Confidential

6 PIN DESCRIPTIONS

Key:

I = Input
 O = Output
 IO = Bi-directional (input/output)
 P = Power pin

Table 6-1 : Power Supply Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
VSS	P	System Ground	-	The VSS is the ground reference of the system.
VDD	P	[3V I/O] System VDD, 2.4 – 3.6V [5V I/O] Stabilizing Capacitor	-	In 3V IO application, this pin is the system power supply In 5V IO application, this pin outputs 3V and should be connected with a capacitor to VSS.
VDDIO	P	[3V I/O] System VDD, 2.4 – 3.6V [5V I/O] System VDD, 4.5 – 5.5V	-	This pin is the system power supply in both 3V and 5V IO application. In 3V application, it is shorted with VDD.
VDDREG	I	VDDIO or VSS	-	This pin must be pulled low in 3V IO application, and pulled high in 5V IO application.

Table 6-2: LCD Driver Supply Pin Description

Pin Name	Type	Connect To	When Not in Use	Description																														
VOUT	P	Stabilizing Capacitor	-	This is the most positive voltage supply pin of the chip. It is output of internal DC-DC converter.																														
VR	IO	Resistors between V0 and VSS	Open	This pin is the input of the built-in voltage regulator for generating V0. When external resistor network is selected (INTRS pulled low) to generate the LCD driving level, V0, two external resistors, R1 and R2, should be connected between VSS and VR, and VR and V0, respectively. When internal network is used, it should be left open.																														
V0/ V1/ V2/ V3/ V4	IO	Stabilizing Capacitor	Open	These are LCD driver supply voltages. The voltages are determined by the bias setting and have the following relationship: $V0 > V1 > V2 > V3 > V4 > VSS$ <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/9</td> <td>(8/9)V0</td> <td>(7/9)V0</td> <td>(2/9)V0</td> <td>(1/9)V0</td> </tr> <tr> <td>1/8</td> <td>(7/8)V0</td> <td>(6/8)V0</td> <td>(2/8)V0</td> <td>(1/8)V0</td> </tr> <tr> <td>1/7</td> <td>(6/7)V0</td> <td>(5/7)V0</td> <td>(2/7)V0</td> <td>(1/7)V0</td> </tr> <tr> <td>1/6</td> <td>(5/6)V0</td> <td>(4/6)V0</td> <td>(2/6)V0</td> <td>(1/6)V0</td> </tr> <tr> <td>1/5</td> <td>(4/5)V0</td> <td>(3/5)V0</td> <td>(2/5)V0</td> <td>(1/5)V0</td> </tr> </tbody> </table>	Bias	V1	V2	V3	V4	1/9	(8/9)V0	(7/9)V0	(2/9)V0	(1/9)V0	1/8	(7/8)V0	(6/8)V0	(2/8)V0	(1/8)V0	1/7	(6/7)V0	(5/7)V0	(2/7)V0	(1/7)V0	1/6	(5/6)V0	(4/6)V0	(2/6)V0	(1/6)V0	1/5	(4/5)V0	(3/5)V0	(2/5)V0	(1/5)V0
Bias	V1	V2	V3	V4																														
1/9	(8/9)V0	(7/9)V0	(2/9)V0	(1/9)V0																														
1/8	(7/8)V0	(6/8)V0	(2/8)V0	(1/8)V0																														
1/7	(6/7)V0	(5/7)V0	(2/7)V0	(1/7)V0																														
1/6	(5/6)V0	(4/6)V0	(2/6)V0	(1/6)V0																														
1/5	(4/5)V0	(3/5)V0	(2/5)V0	(1/5)V0																														
DCDCB5	I	VDDIO or VSS	-	This pin is connected to VDDIO and VSS for 4X and 5 X boosters respectively.																														

INTRS	I	VDDIO or VSS	-	This is the input pin to enable the internal resistors network for the voltage regulator. When this pin is pulled high, the internal feedback resistors of the internal regulator for generating V0 will be enabled. When it is pulled low, external resistors, R1 and R2, should be connected to VSS and VR, and VR and V0, respectively.
-------	---	--------------	---	--

Table 6-3: System Control Pin Description

Pin Name	Type	Connect To	When Not in Use	Description															
FRS	O	Static Indicator	Open	This pin is the static indicator driving output. The frame signal output pin, M, should be used as the back plane signal for the static indicator. The duration of overlapping could be programmable.															
M	IO	Static Indicator or Slave Device	Open	This pin is the frame signal input/output. In master mode, the pin supplies frame signal to slave devices while in slave mode, the pin receives frame signal from the master device.															
CL	IO	Slave Device	Open	This pin is the display clock input/output. In master mode with internal oscillator enabled (CLS pin pulled high), this pin supplies display clock signal to slave devices. In slave mode or when internal oscillator is disabled, the pin receives display clock signal from the master device or external clock source.															
DISP	IO	Slave Device	Open	This pin is display blanking control between master and slave devices. In master mode, this pin supplies on/off signal to slave devices. In slave mode, this pin receives on/off signal from the master device.															
DUTY0 DUTY1	I	VDDIO or VSS	-	<p>These pins are the Chip Mode Selection input. The chip mode is determined by multiplex ratio. Altogether there are four chip modes. Please see the following list for reference.</p> <table border="1"> <thead> <tr> <th>DUTY1</th> <th>DUTY0</th> <th>Chip Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>32+1 MUX Mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>48+1 MUX Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>64+1 MUX Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>68 MUX Mode</td> </tr> </tbody> </table>	DUTY1	DUTY0	Chip Mode	0	0	32+1 MUX Mode	0	1	48+1 MUX Mode	1	1	64+1 MUX Mode	1	0	68 MUX Mode
DUTY1	DUTY0	Chip Mode																	
0	0	32+1 MUX Mode																	
0	1	48+1 MUX Mode																	
1	1	64+1 MUX Mode																	
1	0	68 MUX Mode																	
MS	I	VDDIO or VSS	-	This pin is the master/slave mode selection input. When this pin is pulled high, master mode is selected, which CL, M, FRS and DISP signals will be output for slave devices. When this pin is pulled low, slave mode is selected, which CL, M, DISP are required to be input from master device. FRS will still be an output signal in slave mode.															
CLS	I	VDDIO or VSS	-	This pin is the internal clock enable pin. When this pin is pulled high, internal clock is enabled. The internal clock will be disabled when it is pulled low, an external clock source must be input to CL pin for normal operation.															

Table 6-4: MCU Interface Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
/CS, CS2	I	MCU	VDDIO	These pins are the chip select inputs. The chip is enabled for MCU communication only when both /CS is pulled low and CS2 is pulled high.
/RES	I	MCU	VDDIO	This pin is the reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for reset sequence is 20us.
D/C	I	MCU	VDDIO	This pin is Data/Command control pin. When the pin is pulled high, the data at D7 - D0 is treated as display data. When the pin is pulled low, the data at D7 - D0 will be transferred to the command register.
R/W(/WR)	I	MCU	VSS	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low. When 8080 interface mode is selected, this pin is the Write (/WR) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface mode is selected, this pin must be pulled low.
E(/RD)	I	MCU	VDDIO	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected. When 8080 interface mode is selected, this pin is the Read (/RD) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface mode is selected, this pin must be pulled high.
D7~D0	IO	MCU	VDDIO	These pins are the 8-bit bi-directional data bus in parallel interface mode. D7 is the MSB while D0 is the LSB. When serial mode is selected, D7 is the serial data input (SDA) and D6 is the serial clock input (SCK).
C68/80	I	VDDIO or VSS	VDDIO or VSS	This pin is MCU parallel interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series interface is selected. If Serial Interface is selected (P/S pulled low), the setting of this pin is ignored, but it must be connected to a known logic (either high or low).
P/S	I	VDDIO or VSS	-	This pin is serial/parallel interface selection input. When this pin is pulled high, parallel interface mode is selected. When it is pulled low, serial interface will be selected. <u>Note1:</u> For serial mode, R/W must be connected to VSS. E(/RD) must be connected to VDD. D0 to D5 and C68/80 can be connected to either VDD or VSS. <u>Note2:</u> Read Back operation is only available in parallel mode.

Table 6-5: LCD Driver Output Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
ROW0 (ICON), ROW1 ~ROW66, ROW67 (ICON)	O	LCD	Open	These pins provide the Common driving signals to the LCD panel. There are ICON pins on the chip when either 64 or 48 or 32 Mux mode is selected. Both ICON pins output are the same and should left open when they are not in use. The ICON pins are located at the ROW0 pin and ROW67 pin. For details, please refers Table6-7 Arrangement of common at different multiplex modes in P.17
SEG1 ~SEG132	O	LCD	Open	These pins provide the LCD segment driving signals. The output voltage level of these pins is VSS during sleep mode and standby mode.

Table 6-6: Miscellaneous Pin Description

Pin Name	Type	Connect To	When Not in Use	Description
DUMMY	-	-	-	These pins are floating pins and have no connection inside the IC. These pins can be shorted together or connected to any signal
TE1, TE2	I	VDDIO	VDDIO	These pins are test enable pins. In normal application, these pins must be shorted with VDDIO.
TEST1, TEST2	-	-	-	These pins are reserved for test purpose. Nothing should be connected to these pins, nor are they connected together.
NC	-	-	-	These pins must be left open and cannot be connected together.

Table 6-7: Arrangement of common at different multiplex modes

Command	DUTY0 = 0; DUTY1 = 0;	DUTY0 = 1; DUTY1 = 0;	DUTY0 = 1; DUTY1 = 1;	DUTY0 = 0; DUTY1 = 1;
Pin Name	32Mux Mode	48Mux Mode	64Mux Mode	68Mux Mode
ROW0	ICON	ICON	ICON	COM0
ROW1	COM0	COM0	COM0	COM1
ROW2	COM1	COM1	COM1	COM2
ROW3	COM2	COM2	COM2	COM3
ROW4	COM3	COM3	COM3	COM4
ROW5	COM4	COM4	COM4	COM5
ROW6	COM5	COM5	COM5	COM6
ROW7	COM6	COM6	COM6	COM7
ROW8	COM7	COM7	COM7	COM8
ROW9	COM8	COM8	COM8	COM9
ROW10	COM9	COM9	COM9	COM10
ROW11	COM10	COM10	COM10	COM11
ROW12	COM11	COM11	COM11	COM12
ROW13	COM12	COM12	COM12	COM13
ROW14	COM13	COM13	COM13	COM14
ROW15	COM14	COM14	COM14	COM15
ROW16	COM15	COM15	COM15	COM16
ROW17	Non-select	COM16	COM16	COM17
ROW18	Non-select	COM17	COM17	COM18
ROW19	Non-select	COM18	COM18	COM19
ROW20	Non-select	COM19	COM19	COM20
ROW21	Non-select	COM20	COM20	COM21
ROW22	Non-select	COM21	COM21	COM22
ROW23	Non-select	COM22	COM22	COM23
ROW24	Non-select	COM23	COM23	COM24
ROW25	Non-select	Non-select	COM24	COM25
ROW26	Non-select	Non-select	COM25	COM26
ROW27	Non-select	Non-select	COM26	COM27
ROW28	Non-select	Non-select	COM27	COM28
ROW29	Non-select	Non-select	COM28	COM29
ROW30	Non-select	Non-select	COM29	COM30
ROW31	Non-select	Non-select	COM30	COM31
ROW32	Non-select	Non-select	COM31	COM32
ROW33	Non-select	Non-select	Non-select	COM33
ROW34	Non-select	Non-select	Non-select	COM34
ROW35	Non-select	Non-select	COM33	COM35
ROW36	Non-select	Non-select	COM34	COM36
ROW37	Non-select	Non-select	COM35	COM37
ROW38	Non-select	Non-select	COM36	COM38
ROW39	Non-select	Non-select	COM37	COM39
ROW40	Non-select	Non-select	COM38	COM40
ROW41	Non-select	Non-select	COM39	COM41
ROW42	Non-select	Non-select	COM40	COM42
ROW43	Non-select	COM24	COM41	COM43
ROW44	Non-select	COM25	COM42	COM44
ROW45	Non-select	COM26	COM43	COM45
ROW46	Non-select	COM27	COM44	COM46
ROW47	Non-select	COM28	COM45	COM47
ROW48	Non-select	COM29	COM46	COM48
ROW49	Non-select	COM30	COM47	COM49
ROW50	Non-select	COM31	COM48	COM50
ROW51	COM16	COM32	COM49	COM51
ROW52	COM17	COM33	COM50	COM52
ROW53	COM18	COM34	COM51	COM53
ROW54	COM19	COM35	COM52	COM54
ROW55	COM20	COM36	COM53	COM55
ROW56	COM21	COM37	COM54	COM56
ROW57	COM22	COM38	COM55	COM57
ROW58	COM23	COM39	COM56	COM58
ROW59	COM24	COM40	COM57	COM59
ROW60	COM25	COM41	COM58	COM60
ROW61	COM26	COM42	COM59	COM61
ROW62	COM27	COM43	COM60	COM62
ROW63	COM28	COM44	COM61	COM63
ROW64	COM29	COM45	COM62	COM64
ROW65	COM30	COM46	COM63	COM65
ROW66	COM31	COM47	COM64	COM66
ROW67	ICON	ICON	ICON	COM67

Remarks: “Non-select” means no common signal will be selected to support those output ROW pins.

7 FUNCTIONAL BLOCK DESCRIPTIONS

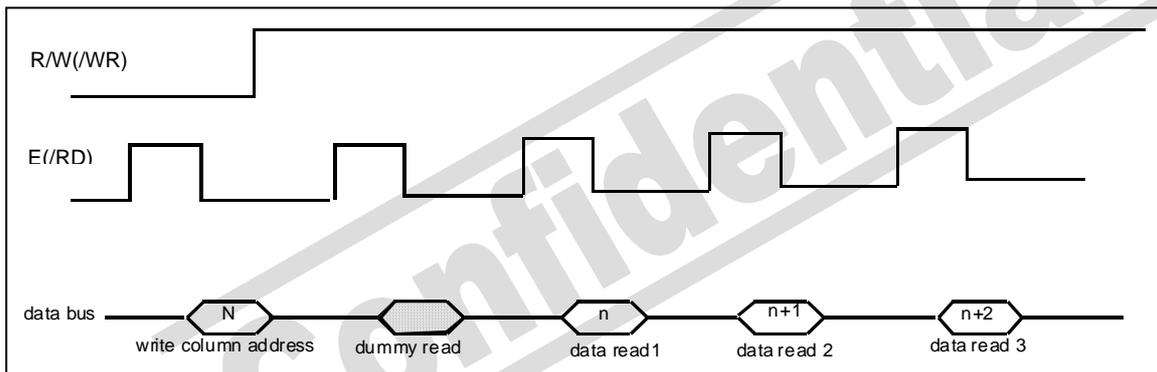
7.1 Microprocessor Interface Logic

The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface and 4-wires serial peripheral interface. The selection of different interfaces is done by P/S pin and C68/80 pin. Please refer to the pin descriptions on P.13-16.

a) MPU 6800-series Parallel Interface (PS = "H" C68/80="H")

The parallel interface consists of 8 bi-directional data pins (D7-D0), R/W(/WR), D/C, E(/RD), /CS and CS2. R/W(/WR) input high indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(/WR) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(/RD) input serves as data latch signal (clock) when high provided that /CS and CS2 are low and high respectively. Please refer to P.42-43 for Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1: Display Data Read with the insertion of dummy read



b) MPU 8080-series Parallel Interface (PS = "H" C68/80="L")

The parallel interface consists of 8 bi-directional data pins (D7-D0), E(/RD), R/W(/WR), D/C, /CS and CS2. E(/RD) input serves as data read latch signal (clock) when low provided that /CS and CS2 are low and high respectively. Whether reading the display data from GDDRAM or reading the status from status register is controlled by D/C. R/W(/WR) input serves as data write latch signal (clock) when low provided that /CS and CS2 are low and high respectively. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/C, a dummy read is also required before the first actual display data read for 8080-series interface. Please refer to P.44-45 for Parallel Interface Timing Diagram of 8080-series microprocessors.

c) MPU 4-wires Serial Interface (PS = “L” C68/80=“H” or “L”)

The 4-wires serial interface consists of serial clock SCK (D6), serial data SDA (D7), D/C, /CS and CS2. SDA is shifted into a 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6, ..., data bit 0. D/C is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to P.46-47 for serial interface timing.

Remarks: For SPI mode, it is necessary to add one time of software reset command (code: E2) in the first line of the initialization code.

Table 7-1 summarized the data bus selection modes in different microprocessor logic.

Table 7-1: Data bus selection modes

	6800-series Parallel Interface	8080-series Parallel Interface	4-wires Serial Peripheral Interface
Data Read	8-bits	8-bits	No
Data Write	8-bits	8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

7.2 Reset Circuit

This block is integrated into the Microprocessor Interface Logic that includes Power On Reset (POR) circuitry and the hardware reset pin, /RES. Both of these having the same reset function. Once receives a negative reset pulse, all internal circuitry will start to initialize. Minimum pulse width for completing the reset sequence is 20us. Status of the chip after reset is given by:

When input is low, the chip is initialized to the following:

- | | | |
|-----|--|--|
| 1) | Display ON/OFF: | Display is turned OFF |
| 2) | Normal/Inverse Display: | Normal Display |
| 3) | Com Scan Direction: | COM0 -> COM67 |
| 4) | Internal Oscillator: | Enable |
| 5) | Internal DC-DC Converter: | Disable |
| 6) | Bias Divider: | Disable |
| 7) | Booster level: | Determined by pin [DCDCB5] |
| 8) | Bias ratio: | 1/5 for 32mux
1/6 for 48mux
1/7 for 64mux
1/7 for 68mux |
| 9) | Multiplex ratio: | Determine by pins [DUTY0, DUTY1] |
| 10) | Electronic volume control: | 20 hex |
| 11) | Built-in resistance ratio: | 20 hex |
| 12) | Average temperature gradient: | -0.05%/oC |
| 13) | Display data column address mapping: | Normal |
| 14) | Display start line: | GDDRAM row 0 |
| 15) | Column address counter: | 00 hex |
| 16) | Page address: | 00 hex |
| 17) | Static indicator: | Disable |
| 18) | Read-modify-write mode: | Disable |
| 19) | Test mode: | Disable |
| 20) | Shift register data in serial interface: | Clear |

While /RES is “L”, no instruction except read status can be accepted. Reset status is read in D4, when D4 is “L”, instruction can be accepted. /RES is essential before initialization in normal operation.

7.3 5V IO Regulator

SSD1808 accepts two power supply range: 2.4-3.6V [**3V IO application**] and 4.5-5.5V [**5V IO application**]. 5V IO Regulator is enabled to regulate 5V IO input to 3/ 3.3V for power supply of internal circuit blocks.

Note: In 5V IO application, VOUT should not be lower than VDDIO.

Table 7-2 summarizes the input/ output connection of 5V IO regulator in normal application.

Table 7-2: 5V IO regulator pin description

Pin Name	3V IO application	5V IO application
VDDREG	Low, disable 5V IO regulator	High, enable 5V IO regulator
VDD	2.4 -3.6V	NC with stabilizing capacitor It outputs 3V
VDDIO	2.4 -3.6V	4.5 -5.5V

7.4 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C pin is high, data is written to Graphic Display Data RAM (GDDRAM). If D/C pin is low, the input at D0 – D7 is interpreted as a Command and it will be decoded. The decoded command will be written to the corresponding command register.

7.5 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is $132 \times 68 = 8,976$ bits. Table 7-3 on P.21 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data mapped to the display. For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage. Please be noticed that the display offset cannot be greater than the default mux mode for any circumstance.

Table 7-3: Graphic Display Data RAM (GDDRAM) Address Map

RAM Row	RAM							32 Mux Mode Common Pins		48 Mux Mode Common Pins		64 Mux Mode Common Pins		68 Mux Mode Common Pins	
	Column	Normal Remapped	00h 83h	01h 82h	--- 01h 00h	82h 83h	00h 01h	Normal	Remapped	Normal	Remapped	Normal	Remapped	Normal	Remapped
00h	Page 0	DB0 (LSB)			---			0	31	0	47	0	63	0	67
01h		DB1			---			1	30	1	46	1	62	1	66
02h		DB2			---			2	29	2	45	2	61	2	65
03h		DB3			---			3	28	3	44	3	60	3	64
04h		DB4			---			4	27	4	43	4	59	4	63
05h		DB5			---			5	26	5	42	5	58	5	62
06h		DB6			---			6	25	6	41	6	57	6	61
07h		DB7 (MSB)			---			7	24	7	40	7	56	7	60
08h	Page 1	DB0 (LSB)			---			8	23	8	39	8	55	8	59
09h		DB1			---			9	22	9	38	9	54	9	58
0Ah		DB2			---			10	21	10	37	10	53	10	57
0Bh		DB3			---			11	20	11	36	11	52	11	56
0Ch		DB4			---			12	19	12	35	12	51	12	55
0Dh		DB5			---			13	18	13	34	13	50	13	54
0Eh		DB6			---			14	17	14	33	14	49	14	53
0Fh		DB7 (MSB)			---			15	16	15	32	15	48	15	52
10h	Page 2	DB0 (LSB)			---			16	15	16	31	16	47	16	51
11h		DB1			---			17	14	17	30	17	46	17	50
12h		DB2			---			18	13	18	29	18	45	18	49
13h		DB3			---			19	12	19	28	19	44	19	48
14h		DB4			---			20	11	20	27	20	43	20	47
15h		DB5			---			21	10	21	26	21	42	21	46
16h		DB6			---			22	9	22	25	22	41	22	45
17h		DB7 (MSB)			---			23	8	23	24	23	40	23	44
18h	Page 3	DB0 (LSB)			---			24	7	24	23	24	39	24	43
19h		DB1			---			25	6	25	22	25	38	25	42
1Ah		DB2			---			26	5	26	21	26	37	26	41
1Bh		DB3			---			27	4	27	20	27	36	27	40
1Ch		DB4			---			28	3	28	19	28	35	28	39
1Dh		DB5			---			29	2	29	18	29	34	29	38
1Eh		DB6			---			30	1	30	17	30	33	30	37
1Fh		DB7 (MSB)			---			31	0	31	16	31	32	31	36
20h	Page 4	DB0 (LSB)			---			Non-select	Non-select	32	15	32	31	32	35
21h		DB1			---			Non-select	Non-select	33	14	33	30	33	34
22h		DB2			---			Non-select	Non-select	34	13	34	29	34	33
23h		DB3			---			Non-select	Non-select	35	12	35	28	35	32
24h		DB4			---			Non-select	Non-select	36	11	36	27	36	31
25h		DB5			---			Non-select	Non-select	37	10	37	26	37	30
26h		DB6			---			Non-select	Non-select	38	9	38	25	38	29
27h		DB7 (MSB)			---			Non-select	Non-select	39	8	39	24	39	28
28h	Page 5	DB0 (LSB)			---			Non-select	Non-select	40	7	40	23	40	27
29h		DB1			---			Non-select	Non-select	41	6	41	22	41	26
2Ah		DB2			---			Non-select	Non-select	42	5	42	21	42	25
2Bh		DB3			---			Non-select	Non-select	43	4	43	20	43	24
2Ch		DB4			---			Non-select	Non-select	44	3	44	19	44	23
2Dh		DB5			---			Non-select	Non-select	45	2	45	18	45	22
2Eh		DB6			---			Non-select	Non-select	46	1	46	17	46	21
2Fh		DB7 (MSB)			---			Non-select	Non-select	47	0	47	16	47	20
30h	Page 6	DB0 (LSB)			---			Non-select	Non-select	Non-select	Non-select	48	15	48	19
31h		DB1			---			Non-select	Non-select	Non-select	Non-select	49	14	49	18
32h		DB2			---			Non-select	Non-select	Non-select	Non-select	50	13	50	17
33h		DB3			---			Non-select	Non-select	Non-select	Non-select	51	12	51	16
34h		DB4			---			Non-select	Non-select	Non-select	Non-select	52	11	52	15
35h		DB5			---			Non-select	Non-select	Non-select	Non-select	53	10	53	14
36h		DB6			---			Non-select	Non-select	Non-select	Non-select	54	9	54	13
37h		DB7 (MSB)			---			Non-select	Non-select	Non-select	Non-select	55	8	55	12
38h	Page 7	DB0 (LSB)			---			Non-select	Non-select	Non-select	Non-select	56	7	56	11
39h		DB1			---			Non-select	Non-select	Non-select	Non-select	57	6	57	10
3Ah		DB2			---			Non-select	Non-select	Non-select	Non-select	58	5	58	9
3Bh		DB3			---			Non-select	Non-select	Non-select	Non-select	59	4	59	8
3Ch		DB4			---			Non-select	Non-select	Non-select	Non-select	60	3	60	7
3Dh		DB5			---			Non-select	Non-select	Non-select	Non-select	61	2	61	6
3Eh		DB6			---			Non-select	Non-select	Non-select	Non-select	62	1	62	5
3Fh		DB7 (MSB)			---			Non-select	Non-select	Non-select	Non-select	63	0	63	4
40h	Page 8	DB0 (LSB)			---			ICON	ICON	ICON	ICON	ICON	ICON	64	3
41h		DB1			---									65	2
42h		DB2			---									66	1
43h		DB3			---									67	0

Segment Pins 0 1 --- 130 131

Remarks: DB0-DB7 represent the data bit of the GDDRAM

“Non-select” means no common signal will be selected to support those output ROW pins.

7.6 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. It takes a single supply input and generates necessary bias voltage. It consists of:

a) 4X, 5X DC-DC voltage converter using internal booster capacitors

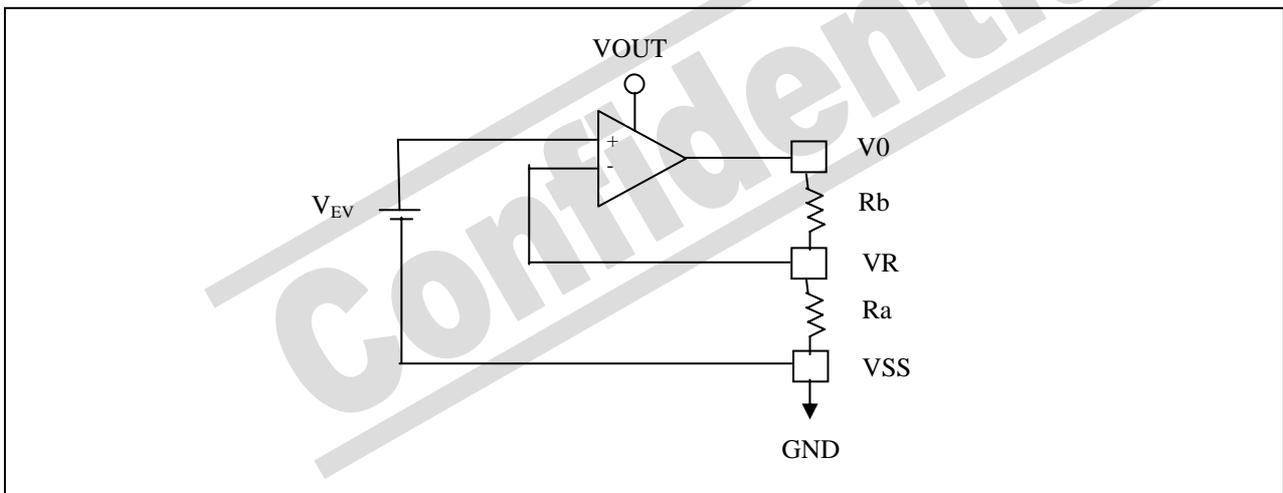
The built-in DC-DC regulated voltage converter is used to generate the large positive voltage supply. SSD1808 can produce 4X or 5X boosting from the potential difference between VDD - VSS to output at VOUT. 5X boosting is chosen if DCDCB5 pin is "L" while 4X boosting is chosen if DCDCB5 pin is "H", No external boosting capacitors are required for this configuration.

b) Voltage regulator circuits (Gain) and Contrast Control

There is a voltage regulator circuits to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of $|V0| < |VOUT|$. The circuits consist of an operational-amplifier circuits and a feedback gain control.

VOUT is the operating voltage for the op-amp, it is required to supply internally or externally. The feedback gain control for LCD driving contrast curves can be selected by INTRS pin either internally (IRS pin = H) or externally (IRS pin = L). If internal resistor network is enabled, eight settings can be selected through software command (20-27h). If external control is selected, external resistors are required to connect between Vss and VR, and between VR and V0. The application circuit diagrams for detail connections are shown in Figure 7-2:

Figure 7-2: Voltage regulator circuit



Software control of the 64 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

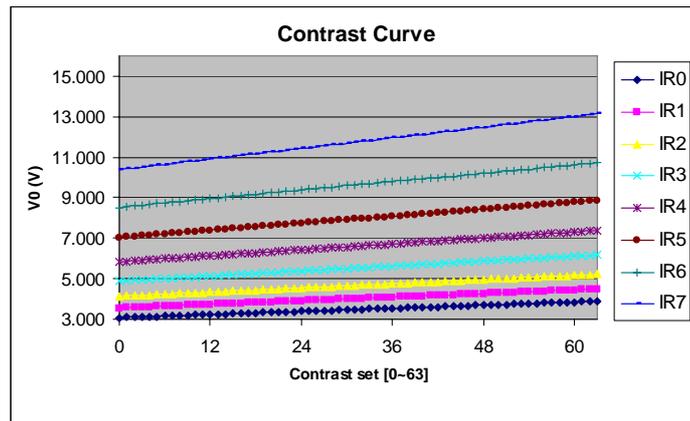
$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} [V] \text{ -----(Equation 1)}$$

$$V_{EV} = \left[1 - \frac{(63 - \alpha)}{300}\right] \times V_{REF} [V] \text{ --(Equation 2)}$$

, where $V_{REF} = 2$ and $\alpha = \text{contrast setting}_{(d)}$

Please refer to Figure 7-3 for the contrast curve with 8 sets of internal resistor network gain.

Figure 7-3: Contrast curve



c) Bias Divider

If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the voltage regulator circuit output (V0) to give the LCD driving levels. External stabilizing capacitors for the divider is optional to reduce the external hardware and pin counts.

d) Bias Ratio Selection circuitry

The software control circuit of 1/4 to 1/9 bias ratio in order to match the characteristic of LCD panel.

e) Self adjust temperature compensation circuitry

Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is $-0.05\%/^{\circ}\text{C}$.

7.7 Oscillator Circuit

This module is an On-Chip low power temperature compensation oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

7.8 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level. The numbers of latches of different members are given by:

32 Mux mode: $132 + 33 = 165$

48 Mux mode: $132 + 49 = 181$

64 Mux mode: $132 + 65 = 197$

68 Mux mode: $132 + 68 = 200$ HV Buffer Cell (Level Shifter)

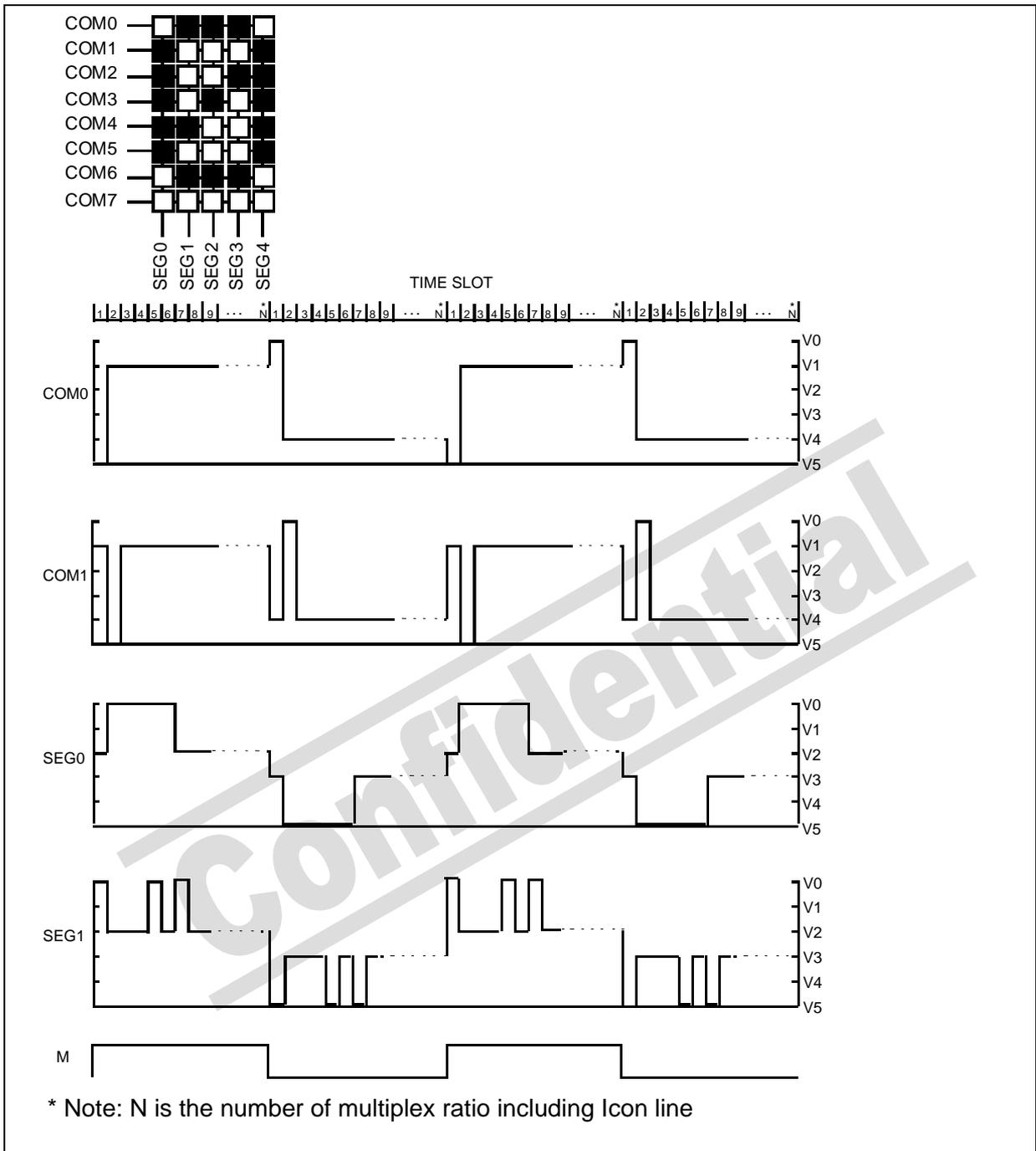
7.9 Level Selector

This block is embedded in the Segment/Common Driver Circuits. Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

7.10 LCD Panel Driving Waveform

Figure 7-4 is an example of how the Common and Segment drivers can be connected to a LCD panel. The waveforms provide an illustration of the multiplex scheme.

Figure 7-4: LCD Driving Waveform



8 COMMAND TABLE

Table 8-1 : Command Table (R/W (/WR) = 0, E= 1 (/RD= 1) unless specific setting is stated)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00 – 0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Address	Set the lower nibble of the column address register using X ₃ X ₂ X ₁ X ₀ as data bits. The lower nibble of column address is reset to 0000b after POR.
0	10 – 1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Address	Set the higher nibble of the column address register using X ₃ X ₂ X ₁ X ₀ as data bits. The higher nibble of column address is reset to 0000b after POR.
0	20 – 27	0	0	1	0	0	X ₂	X ₁	X ₀	Set Internal Gain Resistor Ratio	Feedback gain of the internal regulated DC-DC converter for generating V _{OUT} increases as X ₂ X ₁ X ₀ increased from 000b to 111b. X ₂ X ₁ X ₀ = 000b: 1.9(POR) X ₂ X ₁ X ₀ = 001b: 2.2 X ₂ X ₁ X ₀ = 010b: 2.6 X ₂ X ₁ X ₀ = 011b: 3.0 X ₂ X ₁ X ₀ = 100b: 3.6 X ₂ X ₁ X ₀ = 101b: 4.4 X ₂ X ₁ X ₀ = 110b: 5.3 X ₂ X ₁ X ₀ = 111b: 6.5
0	28 – 2F	0	0	1	0	1	X ₂	X ₁	X ₀	Set Power Control Register	X ₂ X ₁ =11,10 Turn on internal DC DC converter, V ₀ =V _{out} X ₂ X ₁ =01,00 Turn off internal DC DC converter X ₀ =1 Turn on output op amp buffer X ₀ =0 Turn off output op amp buffer After POR, X ₂ X ₁ X ₀ = 000b.
0 0	40 – 7F	0 *	1 Y ₆	X ₅ Y ₅	X ₄ Y ₄	X ₃ Y ₃	X ₂ Y ₂	X ₁ Y ₁	X ₀ Y ₀	Set Display Start Line	For 68 MUX mode, set X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ = 111111 and set the GDDRAM display start line register from 0-67 using Y ₆ Y ₅ Y ₄ Y ₃ Y ₂ Y ₁ Y ₀ For 64/48/32 MUX modes, set GDDRAM display start line register from 0-63 using X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ . There is no need to send the Y ₆ Y ₅ Y ₄ Y ₃ Y ₂ Y ₁ Y ₀ parameters. Display start line register is reset to 000000 after POR for all MUX modes.
0 0	81	1 0	0 0	0 X ₅	0 X ₄	0 X ₃	0 X ₂	0 X ₁	1 X ₀	Set Contrast Control Register	Select contrast level from 64 contrast steps. Contrast increases (V _{OUT} decreases) as X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ is increased from 000000b to 111111b. X ₅ X ₄ X ₃ X ₂ X ₁ X ₀ = 100000b after POR
0	A0 – A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map	X ₀ =0: column address 00h is mapped to SEG0 (POR) X ₀ =1: column address 83h is mapped to SEG0

0	A2 – A3	1	0	1	0	0	0	1	X ₀	Set LCD Bias	X ₀ =0: POR default bias: 32 MUX mode = 1/5 48 MUX mode = 1/6 64 MUX mode = 1/7 68 MUX mode = 1/7 X ₀ =1: alternate bias: 32 MUX mode = 1/6 48 MUX mode = 1/8 64 MUX mode = 1/9 68 MUX mode = 1/9
0	A4 – A5	1	0	1	0	0	1	0	X ₀	Set Entire Display On/Off	X ₀ =0: normal display (POR) X ₀ =1: entire display on
0	A6 – A7	1	0	1	0	0	1	1	X ₀	Set Normal/Reverse Display	X ₀ =0: normal display (POR) X ₀ =1: reverse display
0	AE – AF	1	0	1	0	1	1	1	X ₀	Set Display On/Off	X ₀ =0: turns off LCD panel (POR) X ₀ =1: turns on LCD panel
0	B0 – B8	1	0	1	1	X ₃	X ₂	X ₁	X ₀	Set Page Address	Set GDDRAM Page Address (0-8) for read/write using X ₃ X ₂ X ₁ X ₀
0	C0 – C8	1	1	0	0	X ₃	*	*	*	Set COM Output Scan Direction	X ₃ =0: normal mode (POR) X ₃ =1: remapped mode, COM0 to COM [N-1] becomes COM [N-1] to COM0 when Multiplex ratio is equal to N.
0	E0	1	1	1	0	0	0	0	0	Set Read-Modify-Write Mode	Read-Modify-Write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF.
0	E2	1	1	1	0	0	0	1	0	Software Reset	Initialize internal status registers.
0	EE	1	1	1	0	1	1	1	0	Set End of Read-Modify-Write Mode	Exit Read-Modify-Write mode. RAM Column address before entering the mode will be restored. After POR, Read-modify-write mode is OFF.
0 0	AC – AD	1 *	0 *	1 *	0 *	1 *	1 *	0 Y ₁	X ₀ Y ₀	Indicator Display Mode	X ₀ = 0: indicator off (POR, second command byte is not required) X ₀ = 1: indicator on (second command byte required) Y ₁ Y ₀ = 00: indicator off Y ₁ Y ₀ = 01: indicator on and blinking at ~1 second interval Y ₁ Y ₀ = 10: indicator on and blinking at ~1/2 second interval Y ₁ Y ₀ = 11: indicator on constantly This second byte command is required ONLY when "Set Indicator On" command is sent.
0 0 0 0	AE A5	1 1 1 *	0 0 0 *	1 1 1 *	0 0 0 *	1 0 1 *	1 1 1 *	1 0 0 X ₁	0 1 0 X ₀	Set Power Save Mode	Either standby or sleep mode will be entered using compound commands. Issue compound commands "Set Display Off" followed by "Set Entire Display On". Standby mode will be entered when the static indicator is on constantly. Sleep mode will be entered when static indicator is off.
0	E3	1	1	1	0	0	0	1	1	NOP	Command result in No Operation.

Table 8-2 : Extended Command Table (R/W (/WR) = 0, E= 1 (/RD = 1) unless specific setting is stated)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	82	1 *	0 0	0 0	0 X ₄	0 X ₃	0 X ₂	1 X ₁	0 X ₀	OTP Setting	X4X3X2X1X0: OTP fuse value 00000 : original contrast 00001 : original contrast + 1 steps 00010 : original contrast + 2 steps 00011 : original contrast + 3 steps 00100 : original contrast + 4 steps 00101 : original contrast + 5 steps 00110 : original contrast + 6 steps 00111 : original contrast + 7 steps 01000 : original contrast + 8 steps 01001 : original contrast + 9 steps 01010 : original contrast + 10 steps 01011 : original contrast + 11 steps 01100 : original contrast + 12 steps 01101 : original contrast + 13 steps 01110 : original contrast + 14 steps 01111 : original contrast + 15 steps 10000 : original contrast - 16 steps 10001 : original contrast - 15 steps 10010 : original contrast - 14 steps 10011 : original contrast - 13 steps 10100 : original contrast - 12 steps 10101 : original contrast - 11 steps 10110 : original contrast - 10 steps 10111 : original contrast - 9 steps 11000 : original contrast - 8 steps 11001 : original contrast - 7 steps 11010 : original contrast - 6 steps 11011 : original contrast - 5 steps 11100 : original contrast - 4 steps 11101 : original contrast - 3 steps 11110 : original contrast - 2 steps 11111 : original contrast - 1 steps
0	83	1	0	0	0	0	0	1	1	OTP Programming	This command starts to program LCD driver with OTP offset value. Each bit can be programmed to 1 once

0 0	A9	1 X ₇	0 X ₆	1 X ₅	0 X ₄	1 X ₃	0 X ₂	0 X ₁	1 X ₀	Set Bias Ratio Set TC Value Modify Frame Frequency	MUX X ₁ X ₀ = 00 01 10 11 32: 1/6 or 1/8 1/5 or 1/6(POR) 1/7 or 1/9 P 49:1/6 or 1/8(POR) 1/5 or 1/6 1/7 or 1/9 P 64: 1/6 or 1/8 1/5 or 1/6 1/7 or 1/9(POR) P 68: 1/6 or 1/8 1/5 or 1/6 1/7 or 1/9(POR) P P stands for prohibited settings X ₄ X ₃ X ₂ = 011: (TC3) Typ. -0.20%/° C X ₄ X ₃ X ₂ = 100: (TC4) Typ. -0.30%/° C X ₄ X ₃ X ₂ = 101: (TC5) Typ. -0.50%/° C X ₄ X ₃ X ₂ = 110: (TC6) Typ. -0.80%/° C Increase the value of X ₇ X ₆ X ₅ will increase the frame frequency and vice versa. Default Mode: X ₇ X ₆ X ₅ Frame Frequency (Hz) 000 55 001 65 010 75 011 84 (POR) 100 92 101 100 110 106 111 112 Remarks: By software program the multiplex ratio, the typical frame frequency is listed above.
0	D0 – D1	1	1	0	1	0	0	0	X ₀	Set icon enabled	X ₀ = 0: icon is off. X ₀ = 1: icon is on. (POR)
0 0	D4	1 0	1 0	0 X ₅	1 X ₄	0 0	1 0	0 0	0 0	Set Total Frame Phases	The On/Off of the Static Icon is given by 3 phases / 1 phase overlapping of the M and MSTAT signals. This command set total phases of the M/MSTAT signals for each frame. The more the total phases, the less the overlapping time and thus the lower the effective driving voltage. X ₅ X ₄ = 00: 5 phases X ₅ X ₄ = 01: 7 phases X ₅ X ₄ = 10: 9 phases (POR) X ₅ X ₄ = 11: 16 phases
0	F0 – F1	1	1	1	1	0	0	0	X ₀	Set Test Mode	Reserved for IC testing. Do NOT use.
0 0	F2	1 0	1 N ₆	1 N ₅	1 N ₄	0 N ₃	0 N ₂	1 N ₁	0 N ₀	Set N-line	This command uses to set the N-line inversion The second byte data N ₆ N ₅ N ₄ N ₃ N ₂ N ₁ N ₀ sets the n-line inversion register from 2 to 68 lines to reduce display crosstalk. Register values from 0000010b to 1000100b are mapped to 2 lines to 68 lines respectively. Value 0000000 is the POR value and max n is equals to mux setting. To avoid a fix polarity at some lines, it should be noted that the total number of mux should NOT be a multiple of the lines of inversion (n).
0	F3 – FF	1	1	1	1	X ₃	X ₂	X ₁	X ₀	Set Test Mode	Reserved for IC testing. Do NOT use.

Table 8-3 : Read Command Table(R/W (/WR) = 1, E= 1 (/RD = 0) unless specific setting is stated)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00 - FF	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Status Register Read	<p>X₇=0: indicates the driver is ready for command.</p> <p>X₇=1: indicates the driver is Busy.</p> <p>X₆=0: indicates normal segment mapping with column address.</p> <p>X₆=1: indicates reverse segment mapping with column address.</p> <p>X₅=0: indicates the display is ON.</p> <p>X₅=1: indicates the display is OFF.</p> <p>X₄ = /RES</p> <p>X₃X₂X₁X₀ = 0010, the 4-bit is fixed to 0010 which could be used to identify as Solomon Systech Device.</p>

Confidential

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Data Read / Write

To read data from the GDDRAM, input High to R/W(/WR) pin and D/C pin for 6800-series parallel mode, input Low to E(/RD) pin and High to D/C pin for 8080-series parallel mode. No data read is provided in serial interface mode. In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode. Also, a dummy read is required before first valid data is read. See Figure 7.1 on page 18 in Functional Block Descriptions section for detail waveform diagram. To write data to the GDDRAM, input Low to R/W(/RD) pin and High to D/C pin for both 6800-series and 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write. It should be noted that, after the automatic column address increment, the pointer will NOT wrap round to 0. The pointer will exit the memory address space after accessing the last column. Therefore, the pointer should be re-initialized when progress to another page address.

Table 9-1: Automatic Address Increment

D/C	R/W(/WR)	Action	Auto Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

9.1.2 Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

9.1.3 Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

9.1.4 Set Internal Gain Resistors Ratio

This command enables any one of the eight internal resistor sets for different gains when using internal resistor network (INTRS pin pulled high). In other words, this command is used to select which contrast curve from the eight possible selections. Please refer to Functional Block Descriptions section for detail calculation of the LCD driving voltage.

9.1.5 Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three related power sub-circuits could be turned on/off by this command. Internal voltage booster is used to generate the positive voltage supply (VOUT) from the voltage input (VCI - VSS1). An external positive power supply is required if this option is turned off. Output op-amp buffer is the internal divider for dividing the different voltage levels from the internal voltage booster, VOUT. External voltage sources should be fed into this driver if this circuit is turned off.

9.1.6 Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 67. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0 and so on. Display start line values of 0 to 67 are assigned to Page 0 to 8. Please refer to Table 9-2 as an example for display start line set to 24 (18h).

Table 9-2: Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 18h

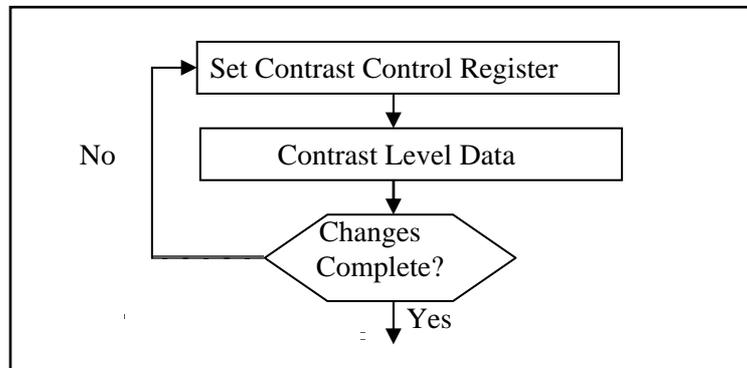
RAM Row	RAM Column	Normal Remapped	00h 83h	01h 82h	--- 01h 00h	82h 83h	32 Mux Mode Common Pins		48 Mux Mode Common Pins		64 Mux Mode Common Pins		68 Mux Mode Common Pins	
							Normal	Remapped	Normal	Remapped	Normal	Remapped	Normal	Remapped
00h	Page 0	DB0 (LSB)			---		8	23	24	23	40	23	44	23
01h		DB1			---		9	22	25	22	41	22	45	22
02h		DB2			---		10	21	26	21	42	21	46	21
03h		DB3			---		11	20	27	20	43	20	47	20
04h		DB4			---		12	19	28	19	44	19	48	19
05h		DB5			---		13	18	29	18	45	18	49	18
06h		DB6			---		14	17	30	17	46	17	50	17
07h		DB7 (MSB)			---		15	16	31	16	47	16	51	16
08h	Page 1	DB0 (LSB)			---		16	15	32	15	48	15	52	15
09h		DB1			---		17	14	33	14	49	14	53	14
0Ah		DB2			---		18	13	34	13	50	13	54	13
0Bh		DB3			---		19	12	35	12	51	12	55	12
0Ch		DB4			---		20	11	36	11	52	11	56	11
0Dh		DB5			---		21	10	37	10	53	10	57	10
0Eh		DB6			---		22	9	38	9	54	9	58	9
0Fh		DB7 (MSB)			---		23	8	39	8	55	8	59	8
10h	Page 2	DB0 (LSB)			---		24	7	40	7	56	7	60	7
11h		DB1			---		25	6	41	6	57	6	61	6
12h		DB2			---		26	5	42	5	58	5	62	5
13h		DB3			---		27	4	43	4	59	4	63	4
14h		DB4			---		28	3	44	3	60	3	64	3
15h		DB5			---		29	2	45	2	61	2	65	2
16h		DB6			---		30	1	46	1	62	1	66	1
17h		DB7 (MSB)			---		31	0	47	0	63	0	67	0
18h	Page 3	DB0 (LSB)			---		0	31	0	47	0	63	0	67
19h		DB1			---		1	30	1	46	1	62	1	66
1Ah		DB2			---		2	29	2	45	2	61	2	65
1Bh		DB3			---		3	28	3	44	3	60	3	64
1Ch		DB4			---		4	27	4	43	4	59	4	63
1Dh		DB5			---		5	26	5	42	5	58	5	62
1Eh		DB6			---		6	25	6	41	6	57	6	61
1Fh		DB7 (MSB)			---		7	24	7	40	7	56	7	60
20h	Page 4	DB0 (LSB)			---		Non-select	Non-select	8	39	8	55	8	59
21h		DB1			---		Non-select	Non-select	9	38	9	54	9	58
22h		DB2			---		Non-select	Non-select	10	37	10	53	10	57
23h		DB3			---		Non-select	Non-select	11	36	11	52	11	56
24h		DB4			---		Non-select	Non-select	12	35	12	51	12	55
25h		DB5			---		Non-select	Non-select	13	34	13	50	13	54
26h		DB6			---		Non-select	Non-select	14	33	14	49	14	53
27h		DB7 (MSB)			---		Non-select	Non-select	15	32	15	48	15	52
28h	Page 5	DB0 (LSB)			---		Non-select	Non-select	16	31	16	47	16	51
29h		DB1			---		Non-select	Non-select	17	30	17	46	17	50
2Ah		DB2			---		Non-select	Non-select	18	29	18	45	18	49
2Bh		DB3			---		Non-select	Non-select	19	28	19	44	19	48
2Ch		DB4			---		Non-select	Non-select	20	27	20	43	20	47
2Dh		DB5			---		Non-select	Non-select	21	26	21	42	21	46
2Eh		DB6			---		Non-select	Non-select	22	25	22	41	22	45
2Fh		DB7 (MSB)			---		Non-select	Non-select	23	24	23	40	23	44
30h	Page 6	DB0 (LSB)			---		Non-select	Non-select	Non-select	Non-select	24	39	24	43
31h		DB1			---		Non-select	Non-select	Non-select	Non-select	25	38	25	42
32h		DB2			---		Non-select	Non-select	Non-select	Non-select	26	37	26	41
33h		DB3			---		Non-select	Non-select	Non-select	Non-select	27	36	27	40
34h		DB4			---		Non-select	Non-select	Non-select	Non-select	28	35	28	39
35h		DB5			---		Non-select	Non-select	Non-select	Non-select	29	34	29	38
36h		DB6			---		Non-select	Non-select	Non-select	Non-select	30	33	30	37
37h		DB7 (MSB)			---		Non-select	Non-select	Non-select	Non-select	31	32	31	36
38h	Page 7	DB0 (LSB)			---		Non-select	Non-select	Non-select	Non-select	32	31	32	35
39h		DB1			---		Non-select	Non-select	Non-select	Non-select	33	30	33	34
3Ah		DB2			---		Non-select	Non-select	Non-select	Non-select	34	29	34	33
3Bh		DB3			---		Non-select	Non-select	Non-select	Non-select	35	28	35	32
3Ch		DB4			---		Non-select	Non-select	Non-select	Non-select	36	27	36	31
3Dh		DB5			---		Non-select	Non-select	Non-select	Non-select	37	26	37	30
3Eh		DB6			---		Non-select	Non-select	Non-select	Non-select	38	25	38	29
3Fh		DB7 (MSB)			---		Non-select	Non-select	Non-select	Non-select	39	24	39	28
40h	Page 8	DB0 (LSB)			---		ICON	ICON	ICON	ICON	ICON	ICON	40	27
41h		DB1			---								41	26
42h		DB2			---								42	25
43h		DB3			---								43	24

Segment Pins 0 1 --- 130 131

9.1.7 Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, VOUT, provided by the On-Chip power circuits. VOUT is set with 64 steps (6-bit) in the contrast control register by a set of compound commands. See Figure 9-1 for the contrast control flow.

Figure 9-1: Contrast Control Flow



9.1.8 Set Segment Re-map

This command changes the mapping between the display data column addresses and segment drivers. It allows flexibility in mechanical layout of LCD glass design. Please refer to Table 9-2 for example.

9.1.9 Set LCD Bias

This command is used to select a suitable bias ratio required for driving the particular LCD panel in use. The selectable values of this command for 68/64 MUX are 1/7 or 1/9, 48 MUX is 1/6 or 1/8 and 33 MUX is 1/5 or 1/6. For other bias ratio settings, extended commands should be used.

9.1.10 Set Entire Display On/Off

This command forces the entire display, including the icon row, to be illuminated regardless of the contents of the GDDRAM. In addition, this command has higher priority than the normal/reverse display. This command is used together with "Set Display ON/OFF" command to form a compound command for entering power save mode. See "Set Power Save Mode" later in this section.

9.1.11 Set Normal/Reverse Display

This command turns the display to be either normal or reverse. In normal display, a RAM data of 1 indicates an illumination on the corresponding pixel. While in reverse display, a RAM data of 0 will turn on the pixel. It should be noted that the icon line will not affect, that is not reverse by this command.

9.1.12 Set Display On/Off

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered. See "Set Power Save Mode" later in this section for details.

9.1.13 Set Page Address

This command enters the page address from 0 to 8 to the RAM page register for read/write operations. Please refer to Table 9-2 for detail mapping.

9.1.14 Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. See Table 9-2 for the relationship between turning on or off of this feature. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

9.1.15 Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. Column address is saved before entering the mode
2. Column address is increased only after display data write but not after display data read.

This Read-Modify-Write mode is used to save the MCU's loading when a very portion of display area is being updated frequently. As reading the data will not change the column address, it could be get back from the chip and do some operation in the MCU. Then the updated data could be written back to the GDDRAM with automatic address increment. After updating the area, "Set End of Read-Modify-Write Mode" is sent to restore the column address and ready for next update sequence.

9.1.16 Software Reset

Issuing this command causes some of the chip's internal status registers to be initialized:

Read-Modify-Write mode is off

Static indicator is turned OFF

Display start line register is cleared to 0

Column address counter is cleared to 0

Page address is cleared to 0

Normal scan direction of the COM outputs

Internal gain resistors Ratio is set to 0

Contrast control register is set to 20h

9.1.17 Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address before entering read-modify-write mode will be restored no matter how much modification during the read-modify-write mode.

9.1.18 Set Indicator On/Off

This command turns on or off the static indicator driven by the M and MSTAT pins.

When the "Set Indicator On" command is sent, the second command byte "Indicator Display Mode" must be followed. However, the "Set Indicator Off" command is a single byte command and no second byte command is required.

The status of static indicator also controls whether standby mode or sleep mode will be entered, after issuing the power save compound command. See "Set Power Save Mode" later in this section.

9.1.19 Set Power Save Mode

Entering Standby or Sleep Mode should be done by using a compound command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When "Set Entire Display ON" is issued when display is OFF, either Standby Mode or Sleep Mode will be entered. The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

Internal oscillator and LCD power supply circuits are stopped

Segment and Common drivers output VSS level

The display data and operation mode before sleep are held

Internal display RAM can still be accessed

If the static indicator is on, the chip enters Standby Mode that is similar to sleep mode except addition with:

Internal oscillator is on

Static drive system is on

Please also be noted that during Standby Mode, if the software reset command is issued, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin /RES.

9.1.20 NOP

A command causing the chip takes No Operation.

9.2 Extended Command

These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip.

9.2.1 OTP setting and programming

OTP (One Time Programming) is a method to adjust V_{OUT}. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules. OTP setting and programming should include two major steps. Find the OTP offset and OTP programming as following,

Step 1. Find OTP offset

- (1) Hardware Reset (sending an active low reset pulse to /RES pin)
- (2) Send original initialization routines
- (3) Set and display any test patterns
- (4) Adjust the contrast value 0x81, 0x00~0x3F until there is the best visual contrast
- (5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1

Contrast value of original initialization = 0x20
 Contrast value of the best original initialization = 0x24
 OTP offset value = 0x24 - 0x20 = +4
 OTP setting command should be (0x82, 0x04)

Example 2:

Contrast value of original initialization = 0x20
 Contrast value of the best original initialization = 0x1B
 OTP setting = 0x1B - 0x20 = -6
 OTP setting command should be (0x82, 0x0A)

Step 2. OTP programming

- (6) Hardware Reset (sending an active low reset pulse to /RES pin)
- (7) Connect an external V_{OUT} by closing SW1 (see diagram below)
- (8) Send OTP setting commands that we find in step 1 (0x82, 0x00~0X0F)
- (9) Send OTP programming command (0x83)
- (10) Wait at least 2 seconds
- (11) Disconnect the external V_{out} by opening SW1
- (12) Discharge the capacitor C by closing the switch SW2 and wait for 1 second
- (13) Hardware Reset (sending an active low reset pulse to /RES pin)
- (14) Verify the result by repeating step 1. (2) – (3)

Figure 9-2: OTP programming circuitry

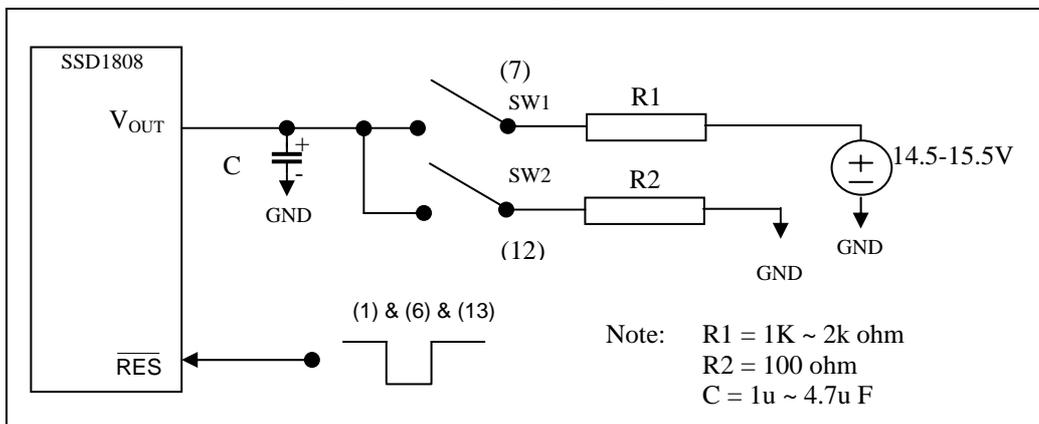
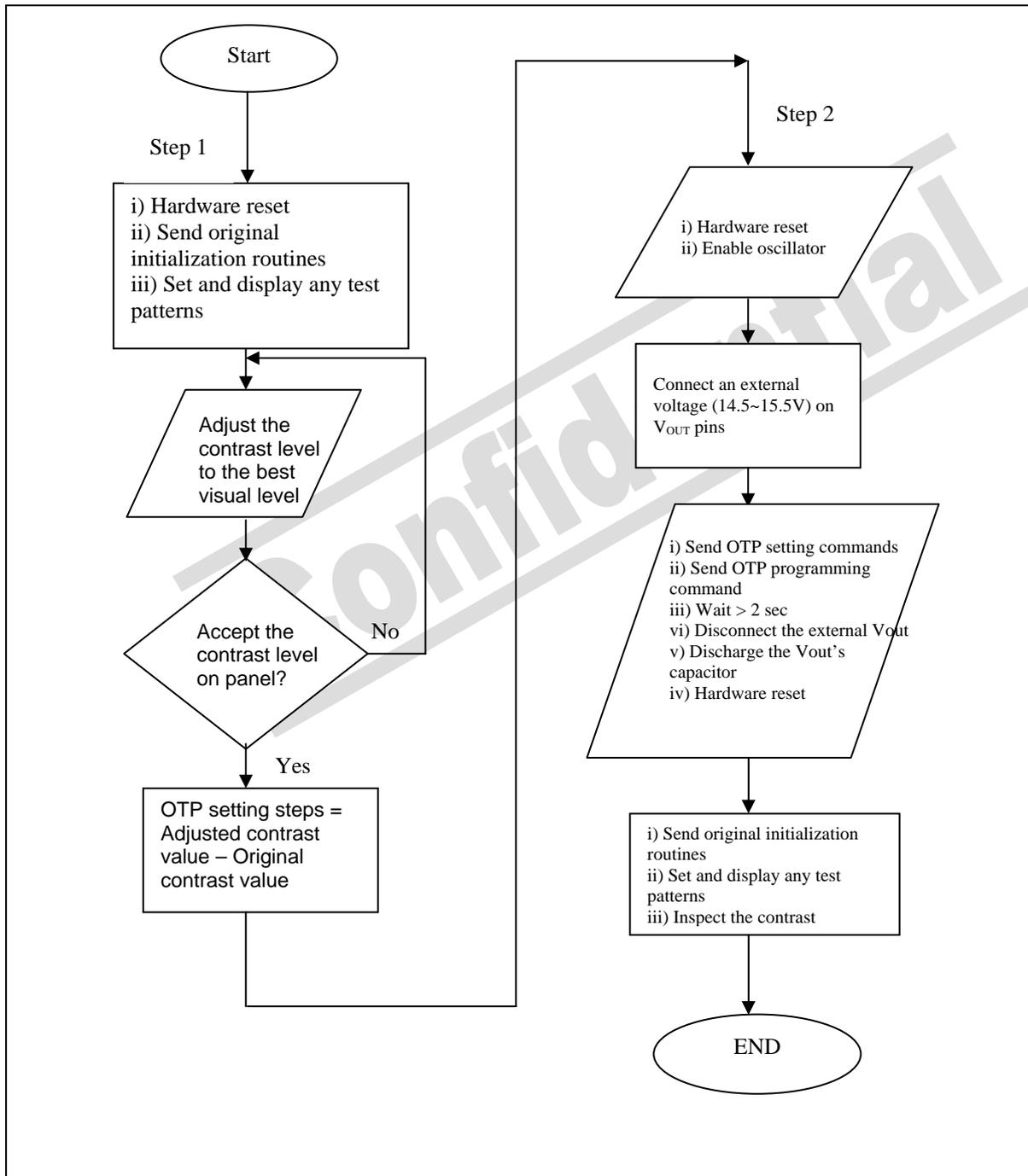


Figure 9-3: Flow chart of OTP programming Procedure



OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin
2. 0X2F \\ turn on the internal voltage booster & output op-amp buffer.
3. 0XA3 \\ Set Biasing ratio 1/9 for 68/64 MUX mode
4. 0X81 \\ Set target gain and contrast.
 0X20 \\ contrast = 20 Hex.
 0X24 \\ IR4
5. \\ Set target display contents
 0x00 \\ set start column address at 0000 binary for lower nibble
 0X10 \\ set start column address at 0000 binary for upper nibble
 0XB0 \\ set page address at page 0
 0xAF \\ display on
6. OTP offset calculation... target OTP offset value is +6

OTP programming:

7. Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin
8. Connect a external V_{OUT} (14.5V~15.5V)
9. 0X82 \\ Set OTP offset value to +6 (0110)
 0X06 \\ 0000 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value
 0X83 \\ Send the OTP programming command.
10. Wait at least 2 seconds for programming wait time.
11. Disconnect an external V_{out}
12. Discharge the V_{out} 's capacitor
13. Hardware reset by sending an active low reset pulse to $\overline{\text{RES}}$ pin

Verify the result:

14. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

9.2.2 Set Bias Ratio

Except the 1/4 bias, all other available bias ratios could be selected using this command plus the "Set LCD Bias" command. For detail setting values and POR default, please refer to the extended command table, Table 8-2.

9.2.3 Set Temperature Coefficient (TC) Value

One out of 4 different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades. Please refer to the extended command table, Table 8-2, for detailed TC values.

9.2.4 Modify Oscillator Frequency

The oscillator frequency can be fine tuned by applying this command. Since the oscillator frequency will be affected by some other factors, this command is not recommended for general usage. Please contact Solomon Systech application engineers for more detail explanation on this command.

9.2.5 Set Icon Enabled

This command enables or disables the icon. It should be noticed that the default setting (POR) will enable the icon.

9.2.6 Set Total Frame Phases

The total number of phases for one display frame is set by this command. The Static Icon is generated by the overlapping of M and MSTAT signals. These two pins output either VSS or VDD at same frequency but with phase difference. To turn on the Static Icon, 3 phases overlapping is applied to these signals, while 1 phase overlapping is given to the off status. The more the total number of phases in one frame, the less the overlapping time. Thus the lower the effective driving voltage at the Static Icon on the LCD panel.

9.2.7 Set Test Mode

This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, users should NOT use this command.

9.3 Read Status Command

9.3.1 Status register Read

This command is issued by pulling D/C Low during a data read (refer to Figure 12-1, 12-2, 12-3, 12-4 for parallel interface waveforms). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

Confidential

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDD	Supply voltage range	-0.3 to +7.0	V
VDDIO		-0.3 to +7.0	V
VOUT		-0.3 to +18	V
VIN	Input voltage range	-0.3 to VDD+0.3	V
I	Current Drain Per Pin excluding VDD, VDDIO and VSS	25	mA
T _A	Operating Temperature	-40 to 85	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} and V_{OUT} be constrained to the range V_{SS} < V_{DD} ≤ V_{DDIO} < V_{OUT}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

Confidential

11 DC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

$V_{DD} = 2.4$ to $3.6V$

$T_A = -40$ to $85^\circ C$

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.6	V
V_{DDIO}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage [3V IO Application] [5V IO Application]	VDD 4.5	VDD 5	VDD 5.5	V V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, Voltage Generator On, 4X Internal DC-DC Converter Enabled, Write accessing, $T_{cyc} = 3.3MHz$, Typ. Osc. Freq., Display On, no panel attached.	-	400	600	μA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 3V$, $V_{OUT} = 11V$, External Vout is supplied, Internal DCDC converter is off, R/\overline{W} (\overline{WR}) Halt, Typ. Osc. Freq., Display On, no panel attached.	-	70	100	μA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 3V$, $V_{OUT} = 11V$, Voltage Generator On, 4X Internal DC-DC Converter Enabled, R/\overline{W} (\overline{WR}) Halt, Typ. Osc. Freq., Display On, no panel attached.	-	90	120	μA
I_{SB} I_{SLEEP}	Standby Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, LCD Driving Waveform Off, Typ. Osc. Freq., R/\overline{W} (\overline{WR}) halt.	-	-	10	μA
	Sleep Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, LCD Driving Waveform Off, Oscillator Off, R/\overline{W} (\overline{WR}) halt.	-	-	2	μA
V_{OUT}	LCD Driving Voltage Generator Output (V_{OUT} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	4.0	-	12.5	V
	Internal Converter Efficiency	4X/ 5X boosting, no panel loading	95	99	-	%
V_{LCD}	LCD Driving Voltage Input (V_{OUT} Pin)	Voltage Generator Disabled.	2.0	-	12.5	V
V_{REF}	Reference Voltage	$T_a = 25^\circ C$, $TC = -0.05\%/^\circ C$	1.94	2.00	2.06	V
V_{OH1}	Logic High Output Voltage	$I_{VOUT} = -0.5mA$	0.8* V_{DDIO}	-	V_{DDIO}	V
V_{OL1}	Logic Low Output Voltage	$I_{VOUT} = +0.5mA$	0	-	0.2* V_{DDIO}	V
V_{IH1}	Logic High Input voltage		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2* V_{DDIO}	V

I _{OH}	Logic High Output Current Source	V _{OUT} = V _{DDIO} -0.4V V _{OUT} = 0.4V	50	-	-	μA
I _{OL}	Logic Low Output Current Drain		-	-	-50	μA
I _{OZ}	Logic Output Tri-state Current Drain Source		-3	-	3	μA
I _{IL} /I _{IH}	Logic Input Current		-1	-	1	μA
C _{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
R _{ON}	LCD driver ON reistance	Ta =25 °C, V0=8V	-	2.0	3.0	kΩ
ΔV _{OUT}	Variation of V _{OUT} Output (V _{DD} is fixed)	Regulated DC-DC Converter Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-2	0	2	%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
TC3	Temperature Coefficient Compensation 3*	Regulated DC-DC Converter Enabled	-0.01	-0.02	-0.03	%/°C
TC4	Temperature Coefficient Compensation 4*		-0.02	-0.03	-0.04	%/°C
TC5	Temperature Coefficient Compensation 5*(POR)		-0.04	-0.05	-0.06	%/°C
TC6	Temperature Coefficient Compensation 6*		-0.07	-0.08	-0.09	%/°C

The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref\ at\ 50^{\circ}C} - V_{ref\ at\ 0^{\circ}C}}{50^{\circ}C - 0^{\circ}C} \times \frac{1}{V_{ref\ at\ 25^{\circ}C}} \times 100\%$$

Confidential

12 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

$V_{DD} = 2.4$ to $3.6V$

$T_A = -40$ to $85^\circ C$

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fosc	Oscillation Frequency of Display Timing Generator	Internal Oscillator Enabled (default), $V_{DD} = 2.7V$ Remark: Ta=25°C, duty ratio 1/68	80.3	102	134	kHz
		Ta=25°C, duty ratio 1/65	80.3	102	134	
		Ta=25°C, duty ratio 1/49	80.3	102	134	
		Ta=25°C, duty ratio 1/33	80.3	102	134	
FCL	Oscillation Frequency of Display Timing Generator	Internal Oscillator Disabled (external), $V_{DD} = 2.7V$ Remark: Ta=25°C, duty ratio 1/68	4.46	5.67	7.44	kHz
		Ta=25°C, duty ratio 1/65	4.23	5.37	7.05	
		Ta=25°C, duty ratio 1/49	3.49	4.43	5.83	
		Ta=25°C, duty ratio 1/33	2.29	2.91	3.83	
FFRM	Frame Frequency	Display ON, Internal Oscillator Enabled				
		132 x 68 Graphic Display Mode	fosc/18*68			Hz
		132 x 65 Graphic Display Mode	fosc/19*65			Hz
		132 x 49 Graphic Display Mode	fosc/23*49			Hz
		132 x 33 Graphic Display Mode	fosc/35*33			Hz
		Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.				
		132 x 68 Graphic Display Mode	fCL/68			Hz
		132 x 65 Graphic Display Mode	fCL/65			Hz
132 x 49 Graphic Display Mode	fCL/49			Hz		
132 x 33 Graphic Display Mode	fCL/33			Hz		

Note

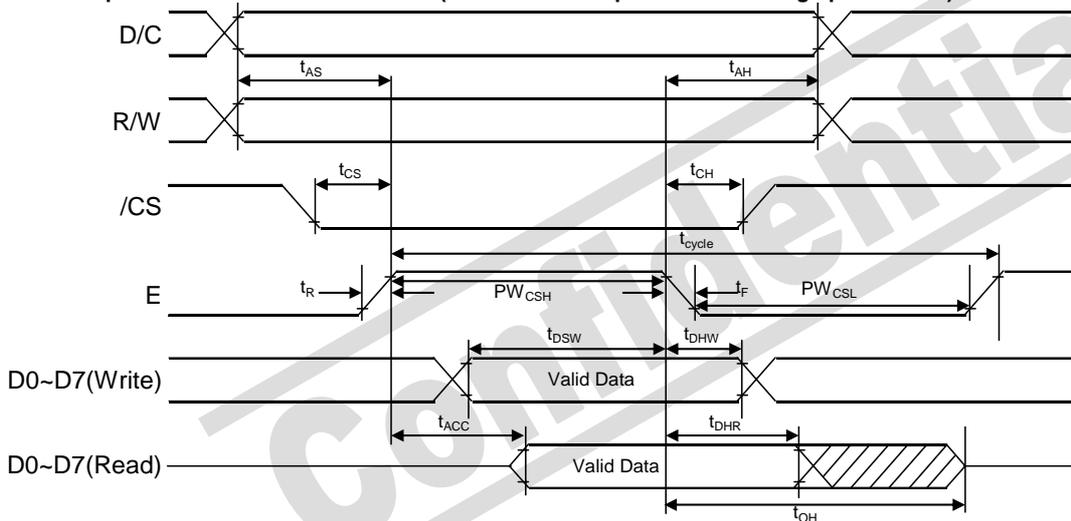
- (1) Fext stands for the frequency value of external clock feeding to the CL pin.
- (2) Fosc stands for the frequency value of internal oscillator.

Table 12-2: Parallel Timing Characteristics (TA = -40 to 85° C, VDDIO = 2.4V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t _{AS}	Address Setup Time	13	-	-	ns
t _{AH}	Address Hold Time	17	-	-	ns
t _{CS}	Chip Select Time	0	-	-	ns
t _{CH}	Chip Select Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	35	-	-	ns
t _{DHW}	Write Data Hold Time	13	-	-	ns
t _{DHR}	Read Data Hold Time	13	-	-	ns
t _{OH}	Output Disable Time	10	-	90	ns
t _{ACC}	Access Time (RAM)	-	-	125	ns
	Access Time (command)	-	-	125	ns
PW _{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read Command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW _{CSH}	Chip Select High Pulse Width (read)	125	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

6800-series parallel interface characteristics (Form 1: /CS low pulse width > E high pulse width)



6800-series parallel interface characteristics (Form 2: /CS low pulse width < E high pulse width)

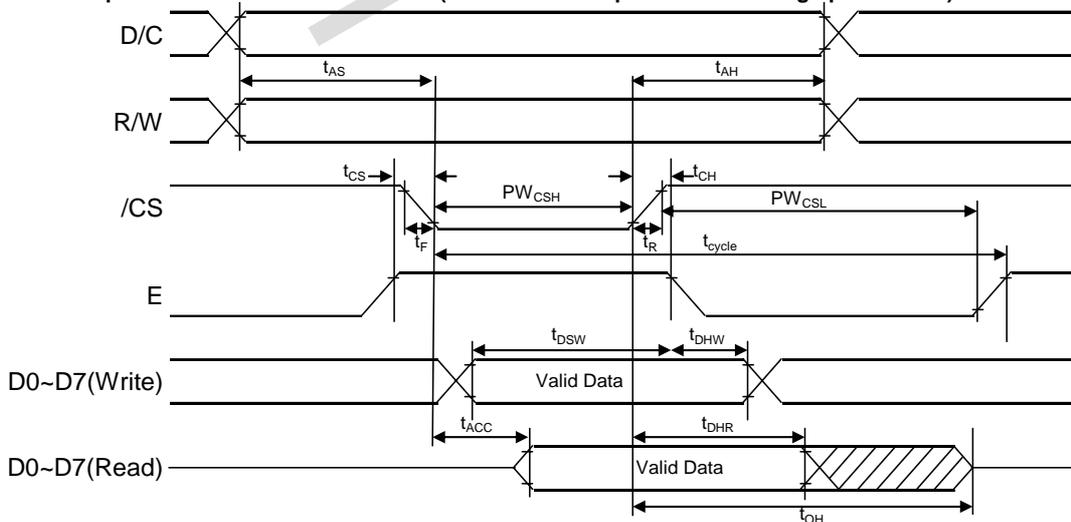


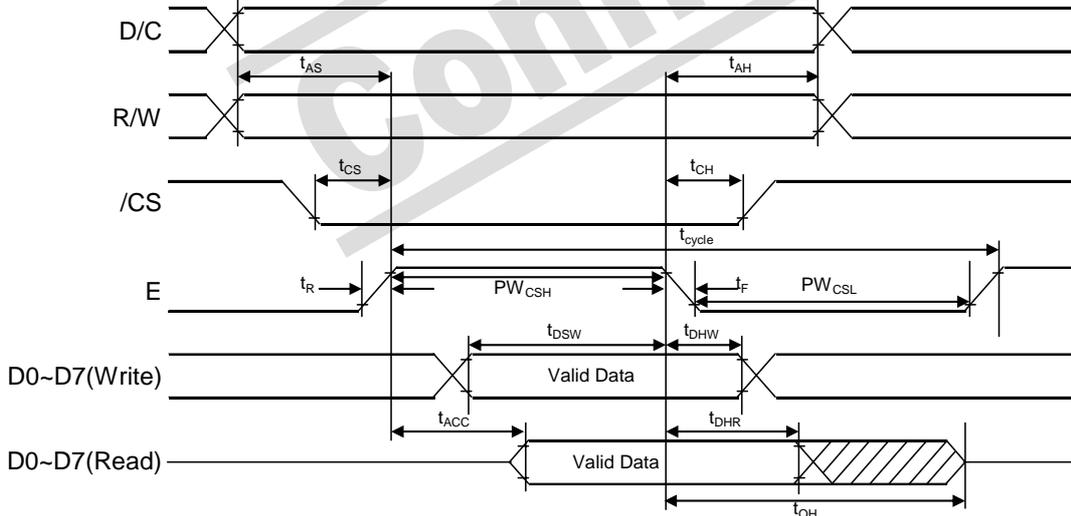
Figure 12-1 : Parallel 6800-series Interface Timing Characteristics (C68/80 = H, P/S = H)

Table 12-3 : Parallel Timing Characteristics (TA = -40 to 85° C, VDDIO = 2.7, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t _{AS}	Address Setup Time	13	-	-	ns
t _{AH}	Address Hold Time	17	-	-	ns
t _{CS}	Chip Select Time	0	-	-	ns
t _{CH}	Chip Select Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	35	-	-	ns
t _{DHW}	Write Data Hold Time	13	-	-	ns
t _{DHR}	Read Data Hold Time	13	-	-	ns
t _{OH}	Output Disable Time	10	-	90	ns
t _{ACC}	Access Time (RAM)	-	-	125	ns
	Access Time (command)	-	-	125	ns
PW _{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read Command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW _{CSH}	Chip Select High Pulse Width (read)	125	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

6800-series parallel interface characteristics (Form 1: /CS low pulse width > E high pulse width)



6800-series parallel interface characteristics (Form 2: /CS low pulse width < E high pulse width)

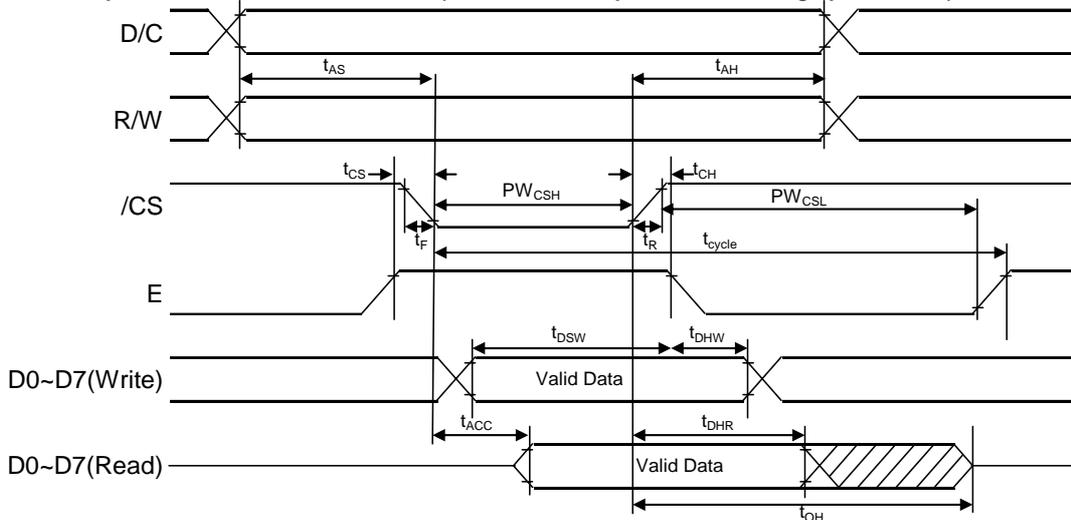


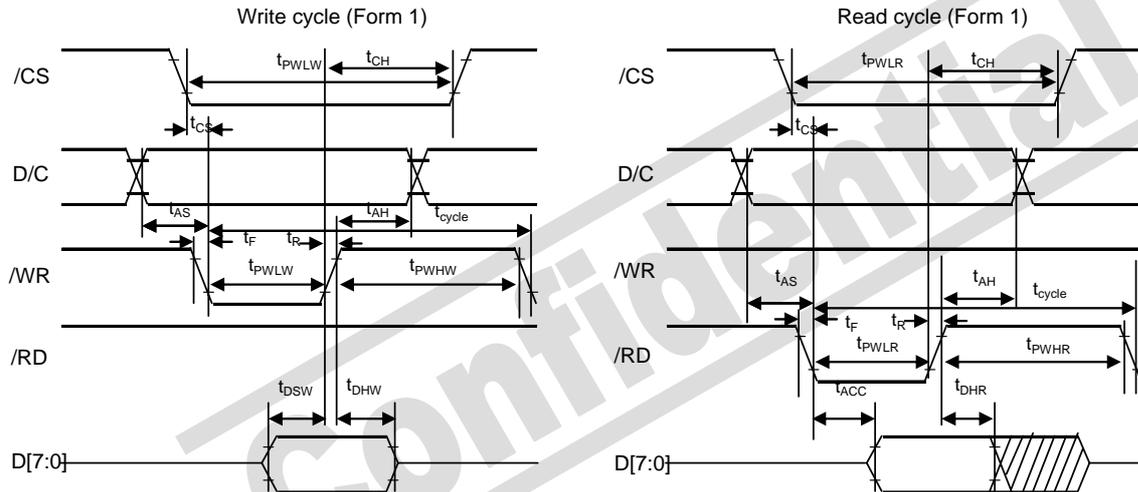
Figure 12-2 : Parallel 6800-series Interface Timing Characteristics (C68/80 = H, P/S = H)

Table 12-4 : Parallel Timing Characteristics (TA = -40 to 85 ° C, VDDIO = 2.4V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	13	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	125	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read Command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	125	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of $V_{DDIO}-V_{SS}$

8080-series parallel interface characteristics (Form 1: /CS low pulse width > W/ R low pulse width)



8080-series parallel interface characteristics (Form 2: /CS low pulse width < W/ R low pulse width)

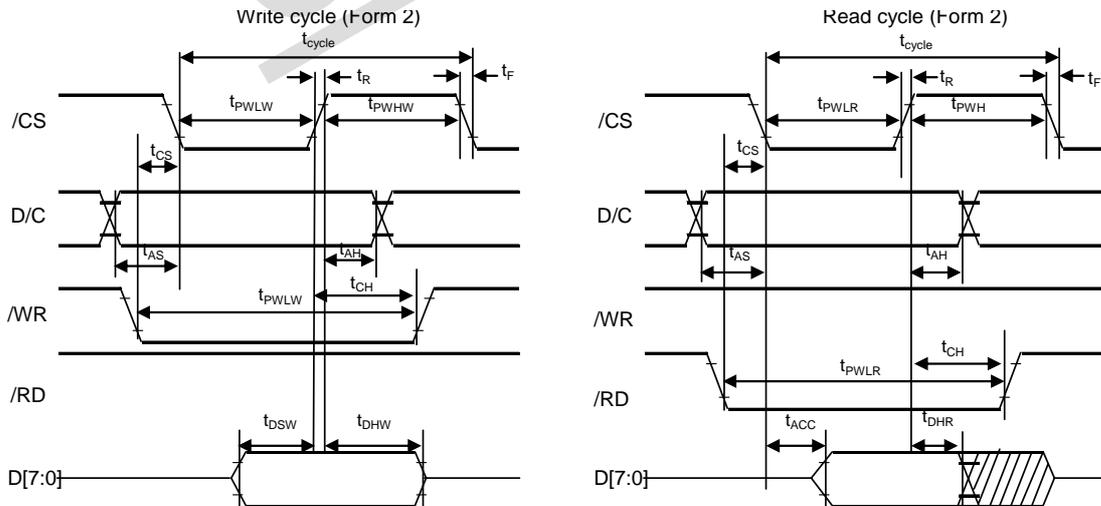


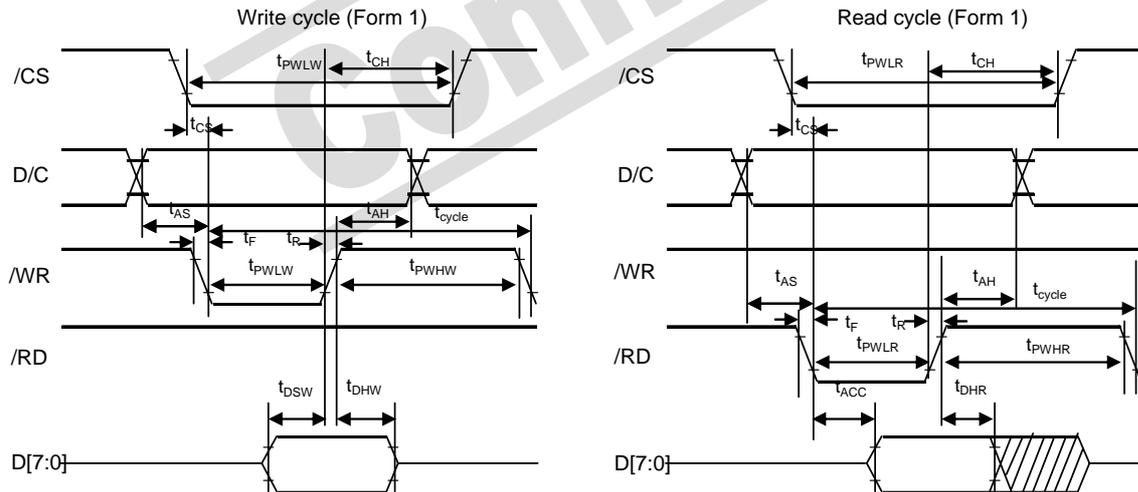
Figure 12-3 : Parallel 8080-series Interface Timing Characteristics (C68/80 = L, P/S = H)

Table 12-5 : Parallel Timing Characteristics (TA = -40 to 85 ° C, VDDIO = 2.7V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t _{AS}	Address Setup Time	13	-	-	ns
t _{AH}	Address Hold Time	17	-	-	ns
t _{CS}	Chip Select Time	0	-	-	ns
t _{CS}	Chip Select Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	35	-	-	ns
t _{DHW}	Write Data Hold Time	13	-	-	ns
t _{DHR}	Read Data Hold Time	13	-	-	ns
t _{ACC}	Access Time (RAM)	-	-	125	ns
t _{ACC}	Access Time (command)	-	-	-	ns
t _{PWLR}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
t _{PWLR}	Chip Select Low Pulse Width (read Command)	250	-	-	ns
t _{PWLW}	Chip Select Low Pulse Width (write)	50	-	-	ns
t _{PWHR}	Chip Select High Pulse Width (read)	125	-	-	ns
t _{PWHW}	Chip Select High Pulse Width (write)	55	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

8080-series parallel interface characteristics (Form 1: /CS low pulse width > W/ R low pulse width)



8080-series parallel interface characteristics (Form 2: /CS low pulse width < W/ R low pulse width)

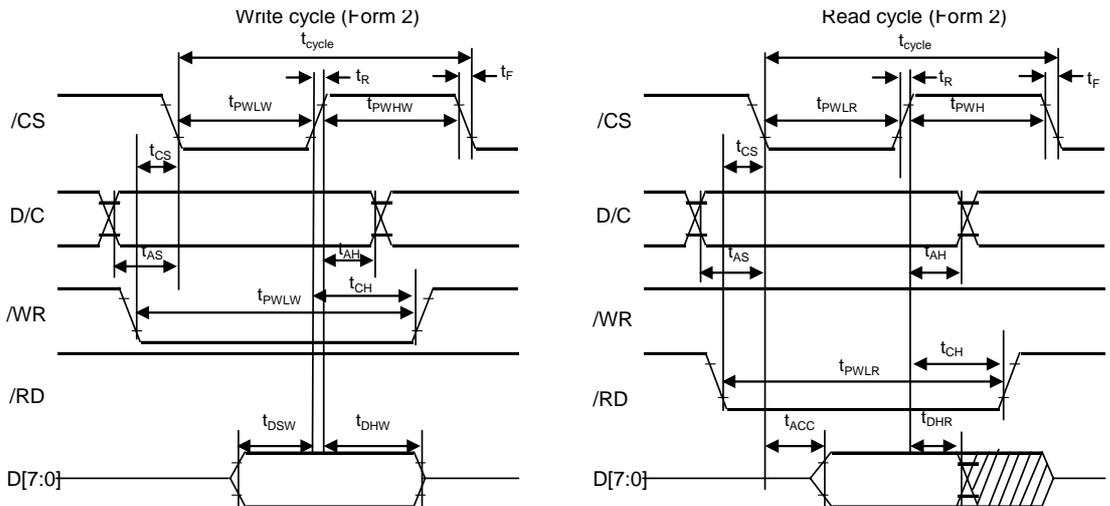


Figure 12-4 : Parallel 8080-series Interface Timing Characteristics (C68/80 = L, P/S = H)

Table 12-6 : Serial Timing Characteristics (TA = -40 to 85 ° C, VDDIO = 2.4V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	450	-	-	ns
t_{AS}	Address Setup Time	90	-	-	ns
t_{AH}	Address Hold Time	360	-	-	ns
t_{CSS}	Chip Select Setup Time	55	-	-	ns
t_{CSH}	Chip Select Hold Time	180	-	-	ns
t_{DSW}	Write Data Setup Time	90	-	-	ns
T_{DHW}	Write Data Hold Time	90	-	-	ns
t_{CLKL}	Clock Low Time	135	-	-	ns
t_{CLKH}	Clock High Time	180	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of $V_{DDIO}-V_{SS}$

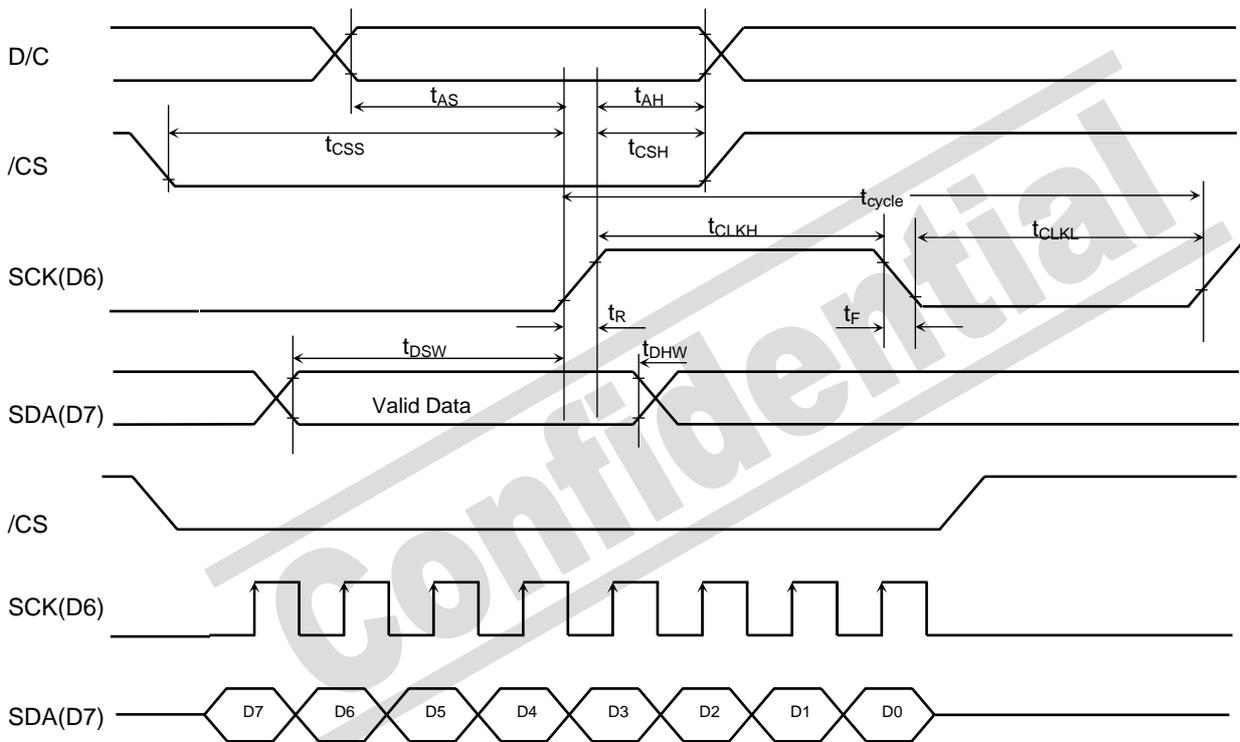


Figure 12-5 : Serial Timing Characteristics (P/S = L)

Table 12-7 : Serial Timing Characteristics (TA = -40 to 85 ° C, VDDIO = 2.7V, VSS =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cyle}	Clock Cycle Time	450	-	-	ns
t_{AS}	Address Setup Time	90	-	-	ns
t_{AH}	Address Hold Time	360	-	-	ns
t_{CSS}	Chip Select Setup Time	55	-	-	ns
t_{CSH}	Chip Select Hold Time	180	-	-	ns
t_{DSW}	Write Data Setup Time	90	-	-	ns
T_{DHW}	Write Data Hold Time	90	-	-	ns
t_{CLKL}	Clock Low Time	135	-	-	ns
t_{CLKH}	Clock High Time	180	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note: All timings are based on 20% to 80% of $V_{DDIO}-V_{SS}$

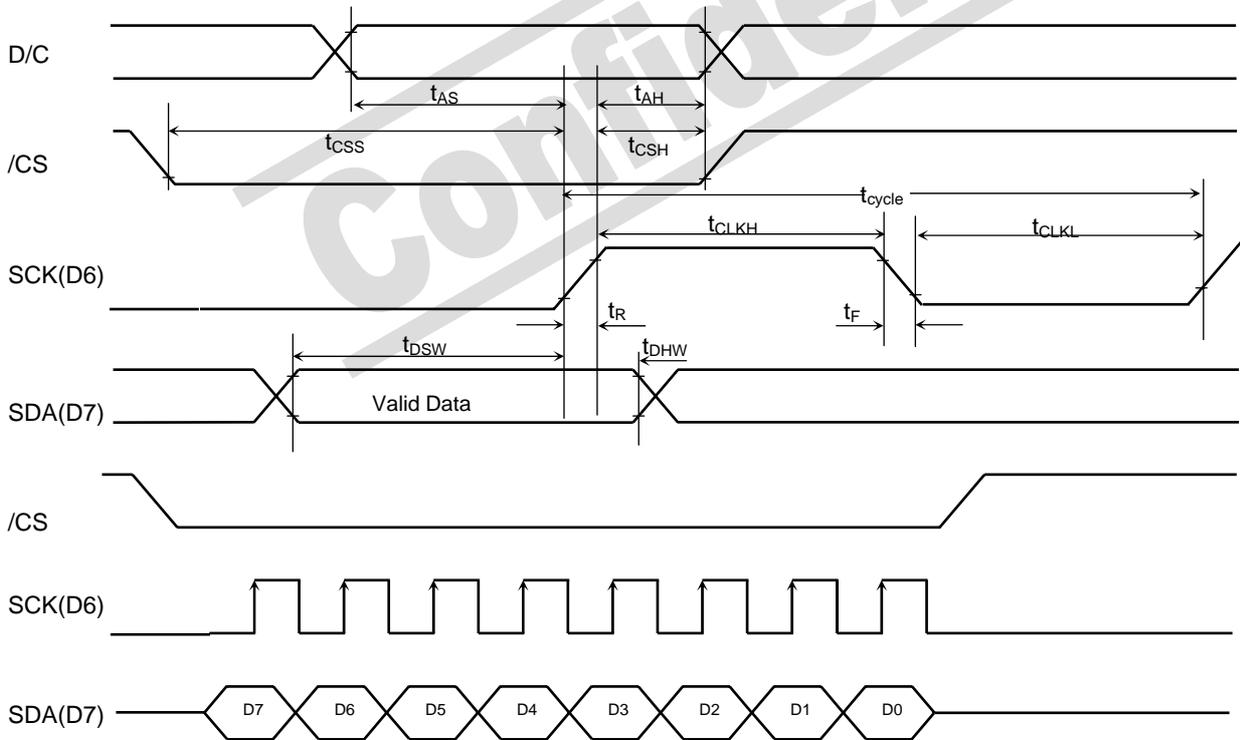


Figure 12-6 : Serial Timing Characteristics (P/S = L)

13 APPLICATION EXAMPLES

13.1 Application Diagram

Figure 13-1 : Application Exemple I (3V IO Application)

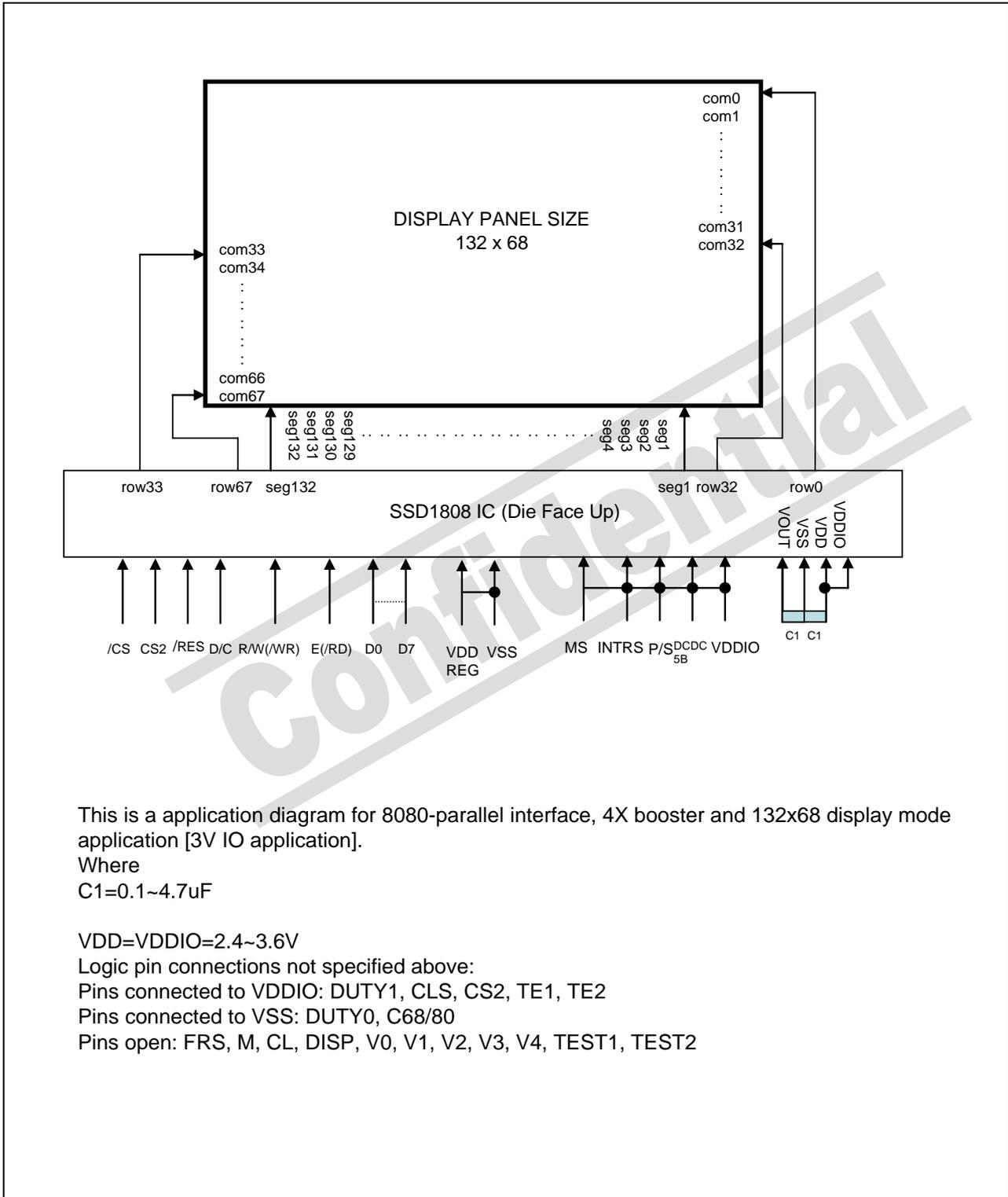
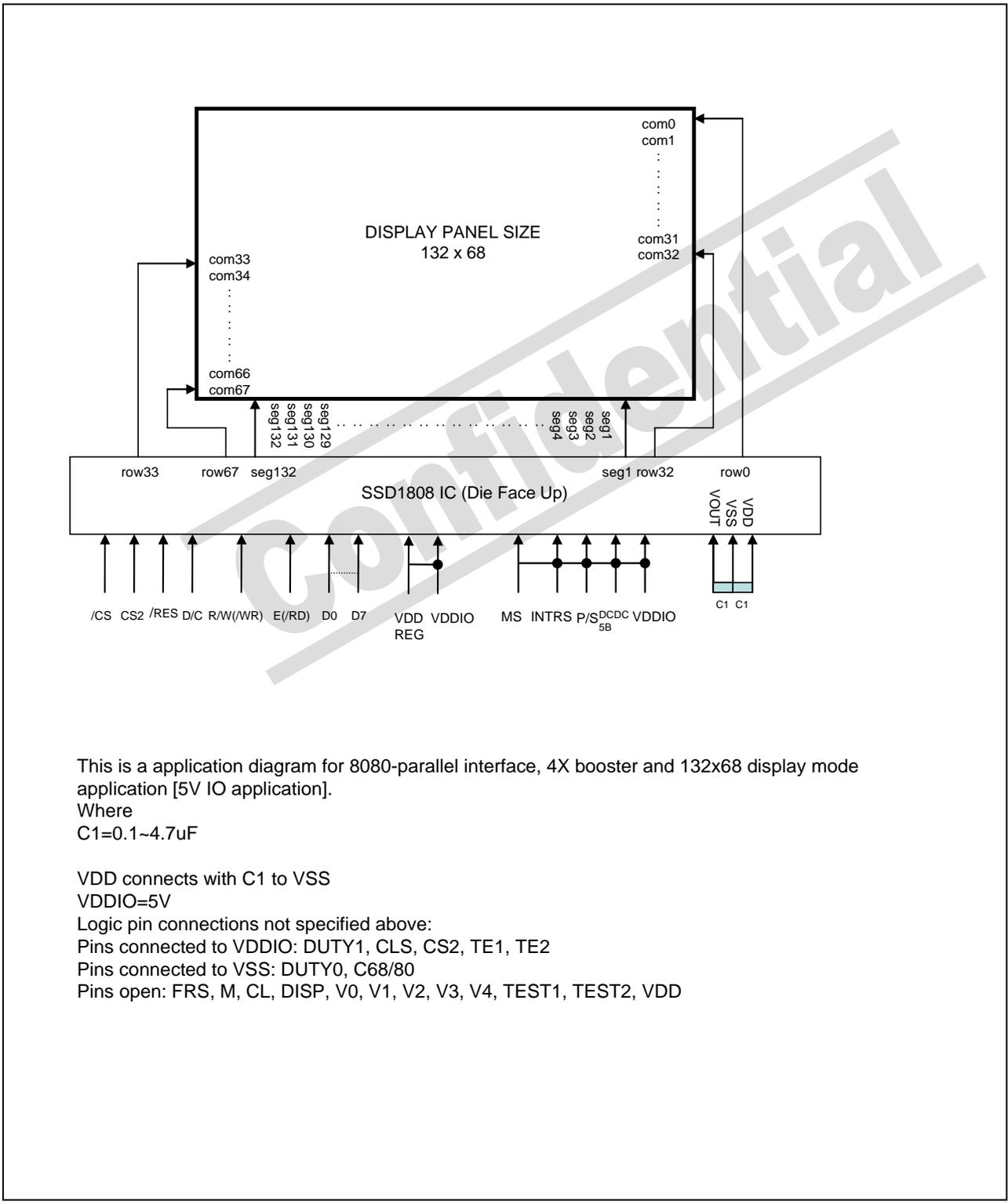


Figure 13-2 : Application Exemple II (5V IO Application)



This is an application diagram for 8080-parallel interface, 4X booster and 132x68 display mode application [5V IO application].

Where

C1=0.1~4.7uF

VDD connects with C1 to VSS

VDDIO=5V

Logic pin connections not specified above:

Pins connected to VDDIO: DUTY1, CLS, CS2, TE1, TE2

Pins connected to VSS: DUTY0, C68/80

Pins open: FRS, M, CL, DISP, V0, V1, V2, V3, V4, TEST1, TEST2, VDD

13.2 Initialization Program

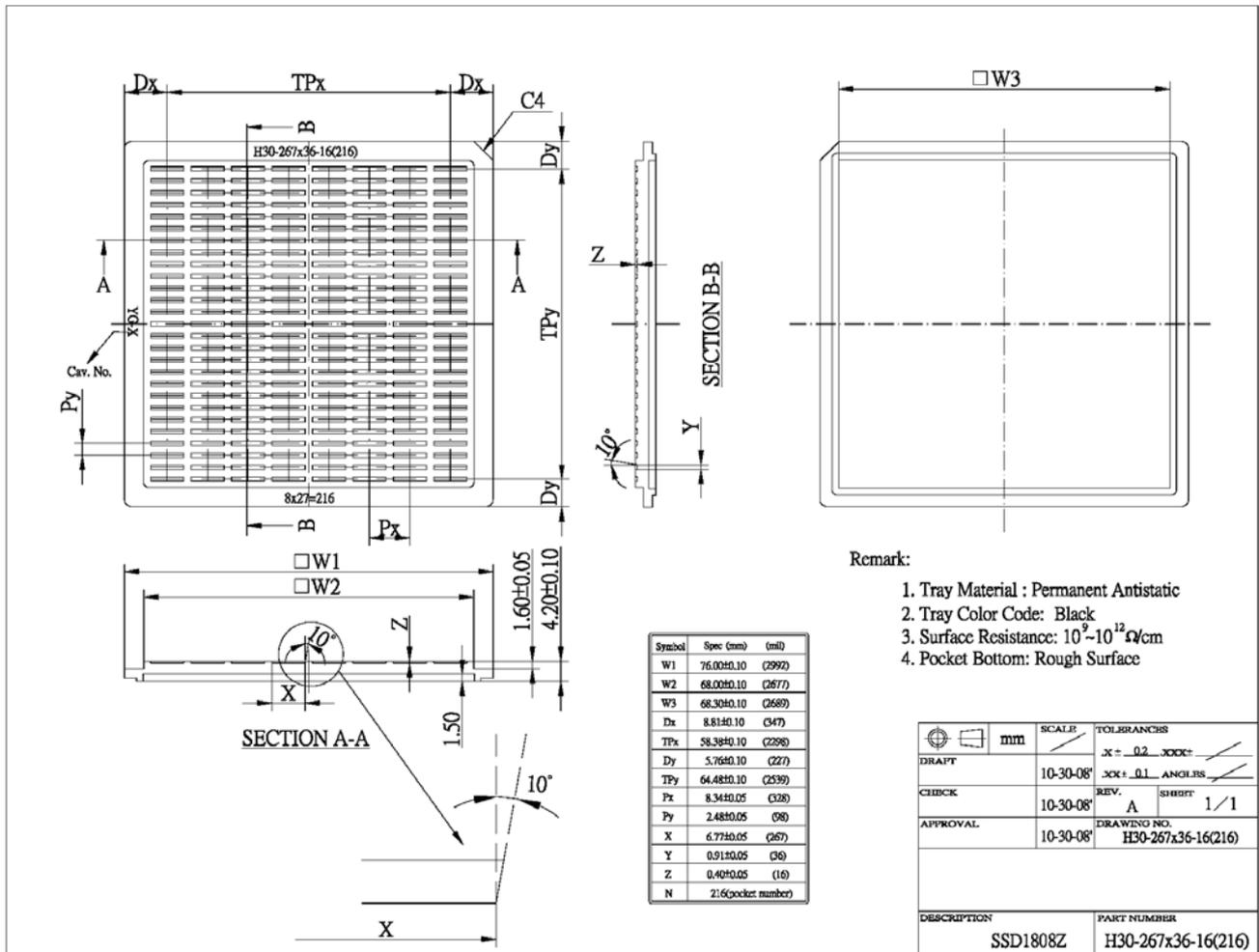
Code E2 //software reset
Code A3 //1/9 bias
Code 27 //set gain
Code 81 //set contrast
Code 30 //contrast value
Code 2F //power control register on
Code A4 //normal display
Code 40 //set display start line
Code AF //display on

// Code - command; Data - data

Confidential

14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS



Confidential

Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typical" must be validated for each customer application by the customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) "Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)" and China standard "电子信息产品污染控制标识要求 (SJ/T11364-2006)" with  control Marking Symbol. Hazardous Substances test report is available upon requested.

<http://www.solomon-systech.com>