SSD1621

Advance Information

93-Segment with Common
3-Level Bistable Display Driver with Controller
CMOS

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1621 is a CMOS bistable display driver with controller. It has 92-segment plus 1 background signal and 1 common signal with 3-voltage levels output.

SSD1621 embeds DC-DC controller, bias divider and VCI regulator to minimize number of external components. SSD1621 is designed for SPI interface with hardware address setting pin, allowing two SSD1621 connected to same SPI bus, increasing the available number of segments.

2 FEATURES

- Design for Segment / Icon type display
- Power supply
  - VDD: 2.4 to 3.5V (Logic operation)
  - VDDIO: 2.4 to VDD (MCU interface)
  - V0: 13 to 32V (High voltage panel driving)
  - VCI: 2.4 to 3.5V (Charge pump power supply)
  - VBAT: 2.8 to 4.2V (Battery supply)
- VBAT can be supplied from Li - battery
- Optional VCI regulator from VBAT supply
- V0 can be supplied from internal DC/DC or external power supply
- V1 can be supplied from internal voltage divider or external power supply
- Output channel
  - 92 Segments (SEG[92:1]) for normal segment/icon driving
  - 1 Background Segment (SEG0) for background driving, with pads on both sides
  - 1 Common (COM) with pads on both sides
- Built-in driving waveform for panel
- On chip 93 x 2 bit data latch
- SPI interface with ADDR_MAP address setting pin
- Built in programmable frequency divider to divide external clock signal (32 kHz) for IC operations.

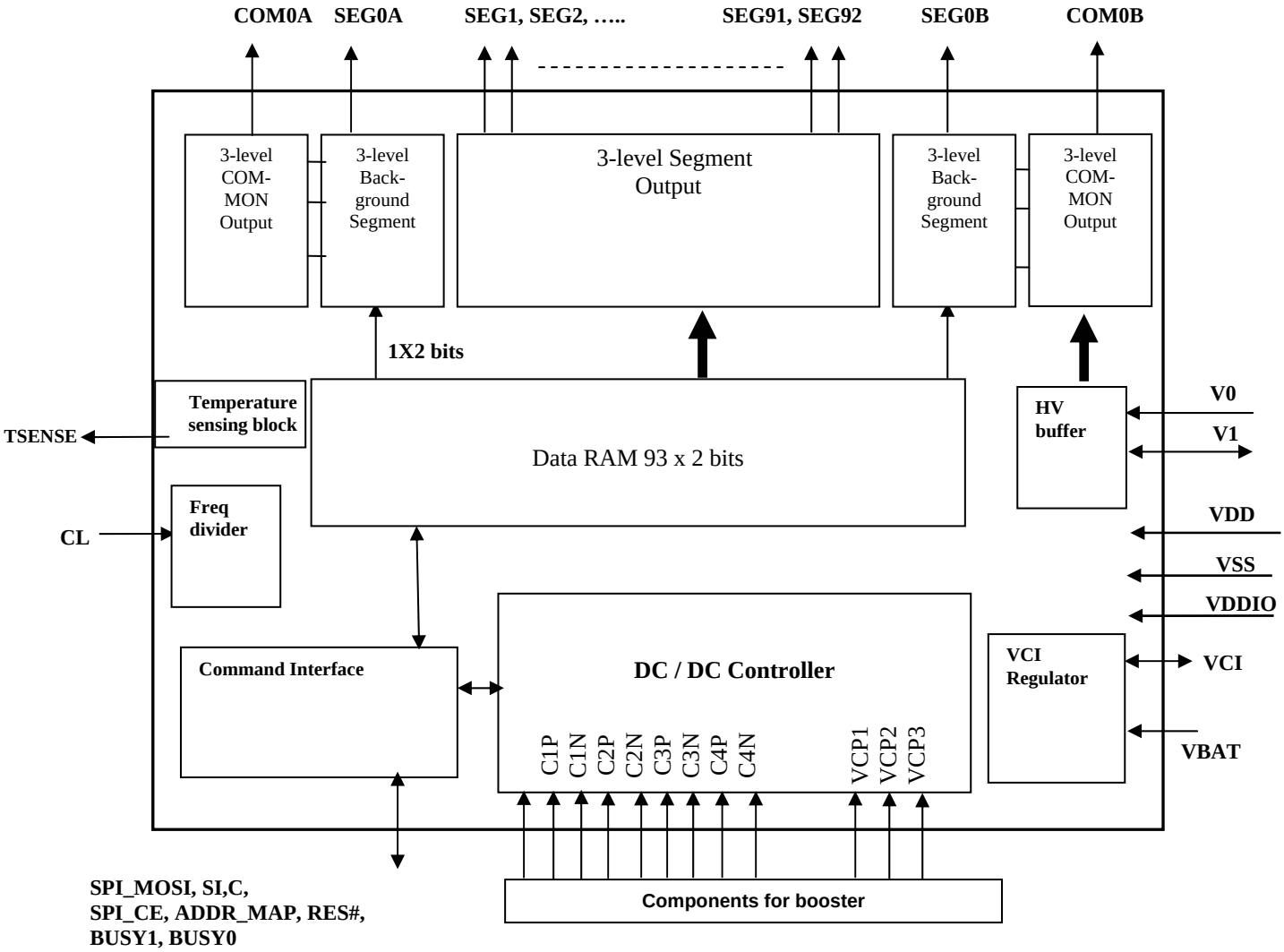
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD1621V	Bare die
SSD1621Z	Au-bumped die
SSD1621U	COF

4 BLOCK DIAGRAM

Figure 4-1 : SSD1621 Block Diagram



5 DIE ARRANGEMENT

Figure 5-1 : SSD1621V layout diagram (Pad face up)

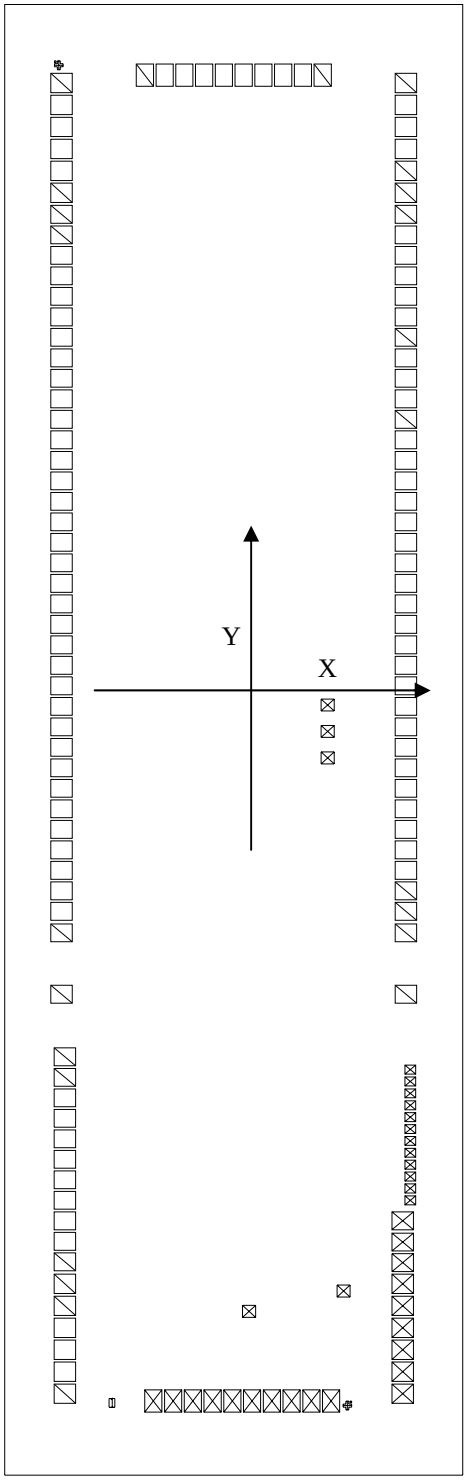


Figure 5-2 : SSD1621Z layout diagram (Pad face up)

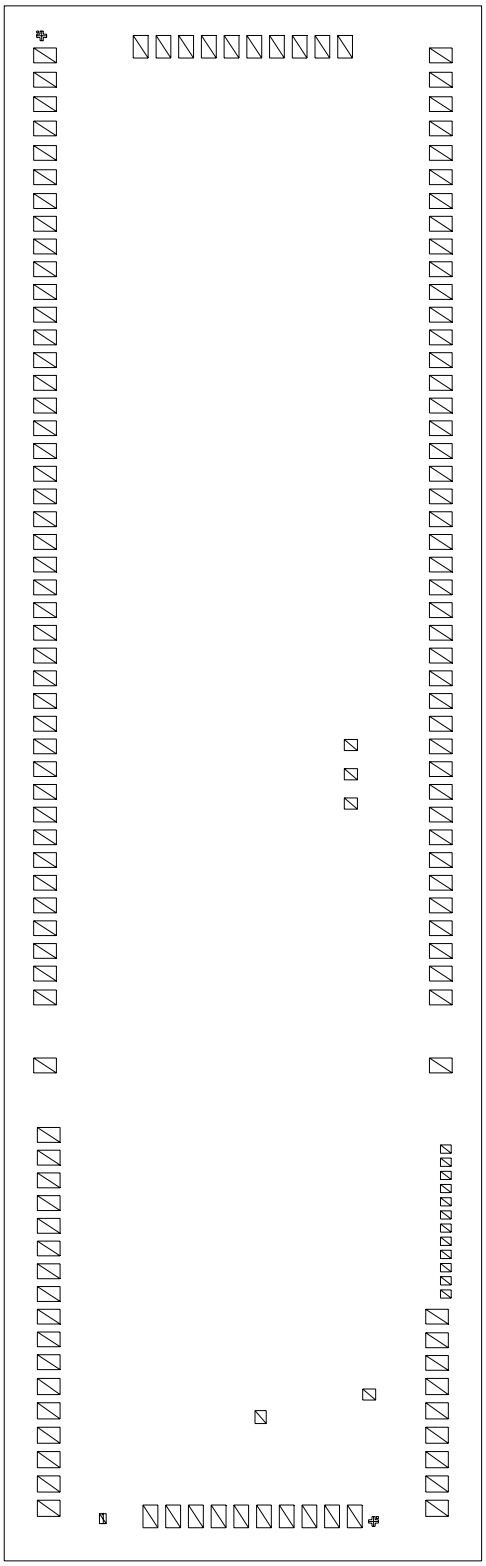


Figure 5-3 : SSD1621V pad layout

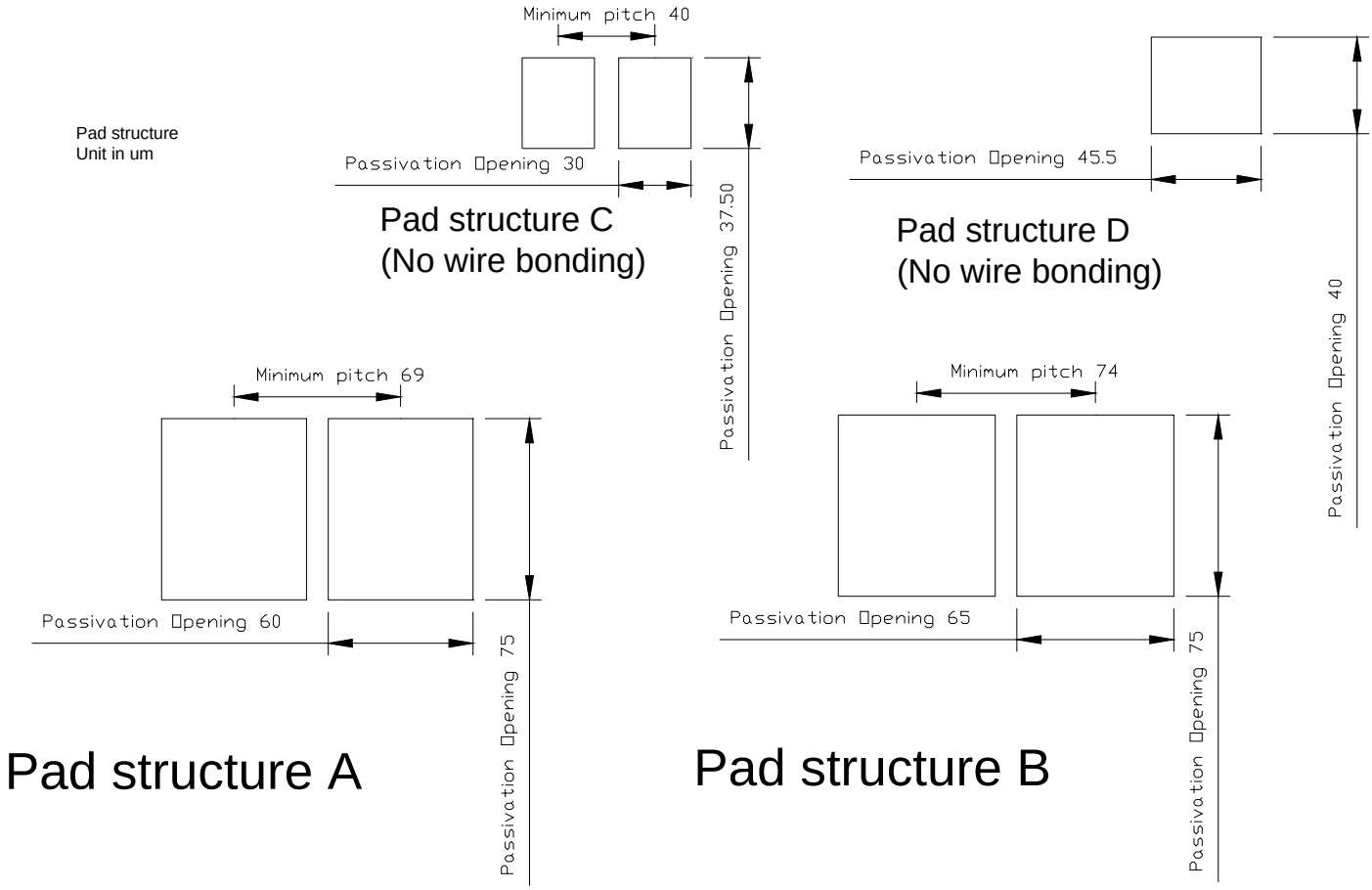


Figure 5-4 : SSD1621Z pad layout

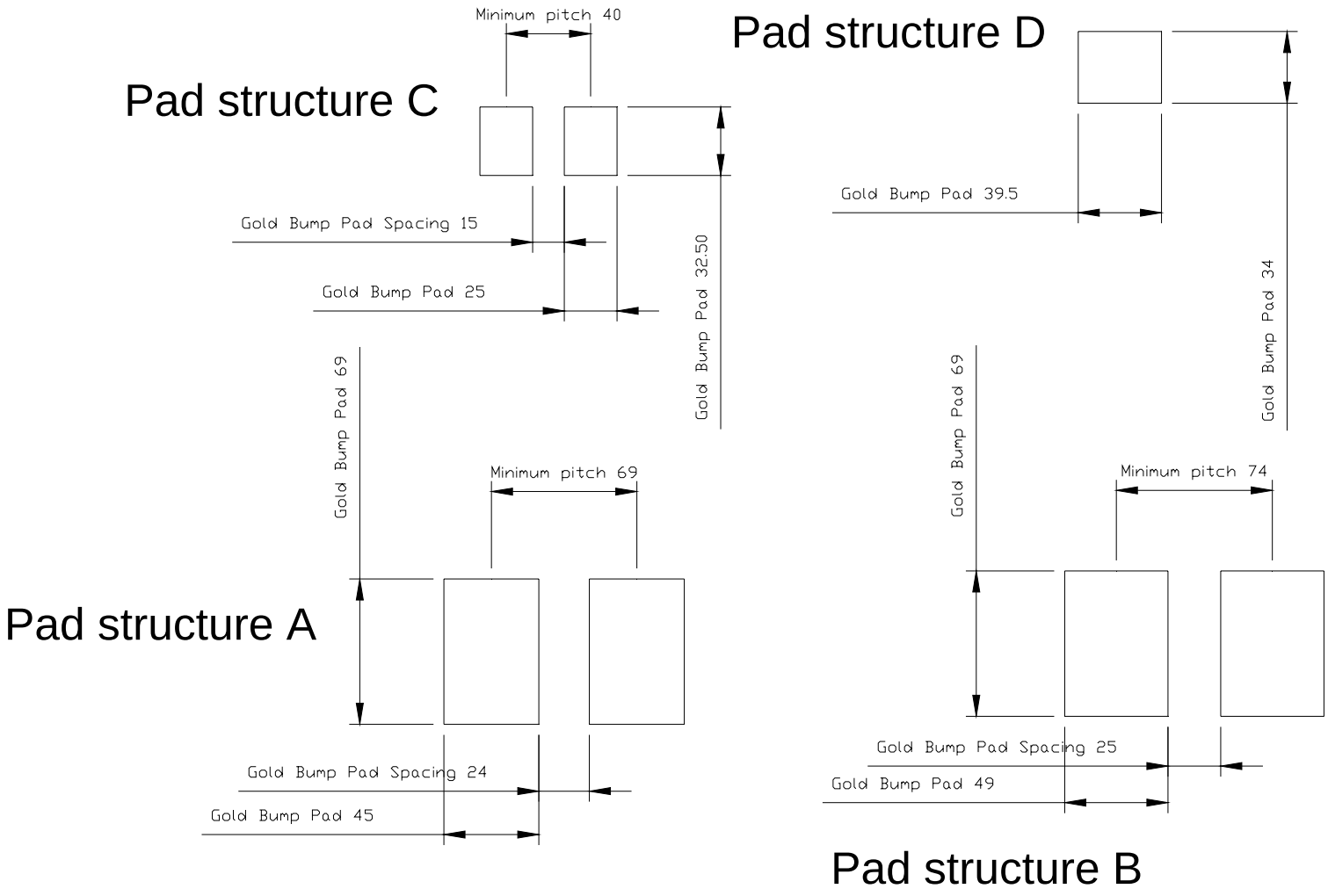


Figure 5-5 : SSD1621V and SSD1621Z alignment mark

Alignment mark
Unit in um

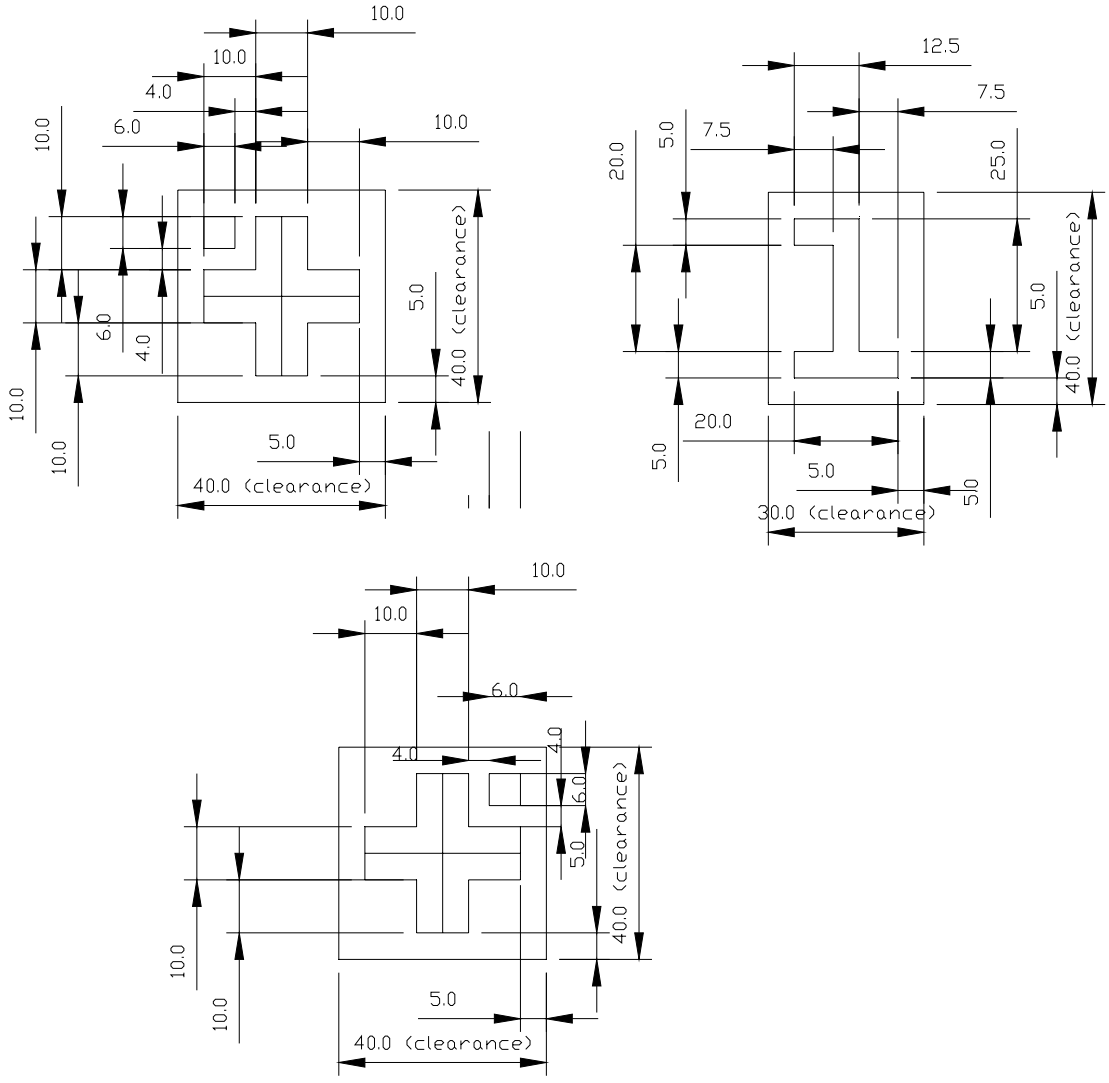
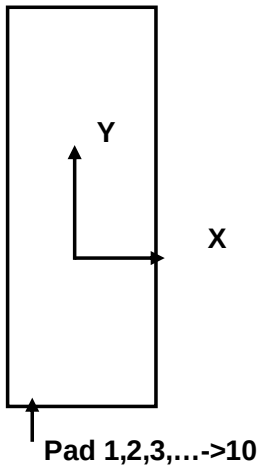


Table 5-1: SSD1621V and SSD1621Z pad coordinates

Pad No	Pin name	X	Y
1	CVSS	-281.0	-2225.5
2	VBAT	-212.0	-2225.5
3	VBAT	-143.0	-2225.5
4	VBAT	-74.0	-2225.5
5	VCI	-5.0	-2225.5
6	C3P	64.1	-2225.5
7	C3N	133.1	-2225.5
8	VCP3	202.1	-2225.5
9	C4P	271.1	-2225.5
10	C4N	340.1	-2225.5
11	C2N	589.9	-2201.3
12	C2P	589.9	-2127.3
13	VCP2	589.9	-2053.3
14	C1N	589.9	-1979.3
15	C1P	589.9	-1905.3
16	VCP1	589.9	-1831.3
17	V1	589.9	-1759.8
18	V0	589.9	-1690.8
19	VSS	589.9	-1619.3
20	TR1	616.9	-1550.3
21	TR2	616.9	-1510.3
22	TR3	616.9	-1470.3
23	TR4	616.9	-1430.3
24	TR5	616.9	-1390.3
25	TR6	616.9	-1350.3
26	TR7	616.9	-1310.3
27	TR8	616.9	-1270.3
28	TR9	616.9	-1230.3
29	TR10	616.9	-1190.3
30	TR11	616.9	-1150.3
31	TR12	616.9	-1110.3
32	COMB	601.4	-856.4
33	SEG0B	601.4	-650.1
34	SEG92	601.4	-577.6
35	SEG91	601.4	-508.6
36	SEG90	601.4	-439.6
37	SEG89	601.4	-370.6
38	SEG88	601.4	-301.6
39	SEG87	601.4	-232.6
40	SEG86	601.4	-163.6
41	SEG85	601.4	-94.6
42	SEG84	601.4	-25.6
43	SEG83	601.4	43.4
44	SEG82	601.4	112.4
45	SEG81	601.4	181.4
46	SEG80	601.4	250.4
47	SEG79	601.4	319.4
48	SEG78	601.4	388.4
49	SEG77	601.4	457.4
50	SEG76	601.4	526.4
51	SEG75	601.4	595.4
52	SEG74	601.4	664.4
53	SEG73	601.4	733.4
54	SEG72	601.4	802.4
55	SEG71	601.4	871.4
56	SEG70	601.4	940.4
57	SEG69	601.4	1009.4
58	SEG68	601.4	1078.4
59	SEG67	601.4	1147.4
60	SEG66	601.4	1216.4
61	SEG65	601.4	1285.4
62	SEG64	601.4	1354.4
63	SEG63	601.4	1423.4
64	SEG62	601.4	1492.4
65	SEG61	601.4	1561.4
66	SEG60	601.4	1630.4
67	SEG59	601.4	1699.4
68	SEG58	601.4	1768.4
69	SEG57	601.4	1840.7
70	SEG56	601.4	1914.7
71	SEG55	601.4	1988.7
72	SEG54	601.4	2062.7
73	SEG53	601.4	2136.7
74	SEG52	601.4	2210.7
75	SEG51	310.5	2237.0
76	SEG50	241.5	2237.0
77	SEG49	172.5	2237.0
78	SEG48	103.5	2237.0
79	SEG47	34.5	2237.0
80	SEG46	-34.5	2237.0
81	SEG45	-103.5	2237.0
82	SEG44	-172.5	2237.0
83	SEG43	-241.5	2237.0
84	SEG42	-310.5	2237.0

Pad No	Pin name	X	Y
85	SEG41	-601.4	2210.7
86	SEG40	-601.4	2136.7
87	SEG39	-601.4	2062.7
88	SEG38	-601.4	1988.7
89	SEG37	-601.4	1914.7
90	SEG36	-601.4	1840.7
91	SEG35	-601.4	1768.4
92	SEG34	-601.4	1699.4
93	SEG33	-601.4	1630.4
94	SEG32	-601.4	1561.4
95	SEG31	-601.4	1492.4
96	SEG30	-601.4	1423.4
97	SEG29	-601.4	1354.4
98	SEG28	-601.4	1285.4
99	SEG27	-601.4	1216.4
100	SEG26	-601.4	1147.4
101	SEG25	-601.4	1078.4
102	SEG24	-601.4	1009.4
103	SEG23	-601.4	940.4
104	SEG22	-601.4	871.4
105	SEG21	-601.4	802.4
106	SEG20	-601.4	733.4
107	SEG19	-601.4	664.4
108	SEG18	-601.4	595.4
109	SEG17	-601.4	526.4
110	SEG16	-601.4	457.4
111	SEG15	-601.4	388.4
112	SEG14	-601.4	319.4
113	SEG13	-601.4	250.4
114	SEG12	-601.4	181.4
115	SEG11	-601.4	112.4
116	SEG10	-601.4	43.4
117	SEG9	-601.4	-25.6
118	SEG8	-601.4	-94.6
119	SEG7	-601.4	-163.6
120	SEG6	-601.4	-232.6
121	SEG5	-601.4	-301.6
122	SEG4	-601.4	-370.6
123	SEG3	-601.4	-439.6
124	SEG2	-601.4	-508.6
125	SEG1	-601.4	-577.6
126	SEG0A	-601.4	-650.1
127	COMA	-601.4	-856.4
128	SPI_MOSI	-589.9	-1067.3
129	SPI_MISO	-589.9	-1136.3
130	SPI_CLK	-589.9	-1205.3
131	SPI_CE	-589.9	-1274.3
132	BUSY0	-589.9	-1343.3
133	BUSY1	-589.9	-1412.3
134	RES	-589.9	-1481.3
135	VDD	-589.9	-1550.3
136	VDDIO	-589.9	-1619.3
137	ADDR_MAP	-589.9	-1688.3
138	VSS	-589.9	-1757.3
139	CL	-589.9	-1831.3
140	TSENSE	-589.9	-1905.3
141	ATESTPAD	-589.9	-1979.3
142	AVDD	-589.9	-2053.3
143	AVSS	-589.9	-2127.3
144	VSS	-589.9	-2201.3

Pad No	Pin name	X	Y
145	TR14	53.6	-1924.1
146	TR17	328.1	116.7
147	TR16	328.1	-61.1
148	TR15	383.8	-1855.7
149	VSS	328.1	27.8



Die size	1.60mm x 4.95mm

Pad size:

	SSD1621V passivation opening	SSD1621Z gold bump pad size
1-10, 17-19, 32-138	60um x 75um	69um x 45um
11-16, 139-144	65um x 75um	69um x 49um
20-31	37.5um x 30um	32.5um x 25um
145-149	45.5um x 40um	39.5um x 34um

Alignment Mark:

Type	Size	Coordinate (Centre of marks)
+ shape	30um x 30um	-613.0, 2270.0
+ shape	30um x 30um	397.0, -2241.0
pin1	30um x 20um	-425.6, -2232.2

6 PIN DESCRIPTION

Table 6-1: Pin description

Pin Name	Type	Pad #	Description
V_{BAT}	P	2, 3, 4	Power supply for VCI regulator. Direct connection to battery.
V_{CI}	P	5	Power supply for DC/DC circuit. It can be supplied externally or regulated from V_{BAT} internally.
V_{DD}	P	135	Power supply for IC digital circuit. It should be connected with V_{DDA}
V_{DDA}	P	142	Power supply for IC analog circuit. It should be connected with V_{DD}
V_{DDIO}	P	136	Power supply for MCU interface level.
V_{SS}	P	19, 138, 144	Ground pins of IC. V_{SS} should be connected with V_{SSC} and V_{SSA}
V_{SSC}	P	1	Ground pins of Charge pump circuit. V_{SS} should be connected to V_{SS} and V_{SSA}
V_{SSA}	P	143	Ground pins of analog circuits V_{SSA} should be connected to V_{SSC} and V_{SS}
V_0	P	18	Panel driving voltage power pin Connect to VCP1 if internal DC/DC is used
V_1	P	17	Panel driving voltage power pin. Voltage level is ½ V0. The voltage can be regulated from V0 or supplied externally
C1P	I/O	15	Pin for charge pump capacitor Connection to C1N with a capacitor.
C1N	I/O	14	Pin for charge pump capacitor Connection to C1P with a capacitor.
C2P	I/O	12	Pin for charge pump capacitor Connection to C2N with a capacitor.
C2N	I/O	11	Pin for charge pump capacitor Connection to C2P with a capacitor.
C3P	I/O	6	Pin for charge pump capacitor Connection to C3N with a capacitor.
C3N	I/O	7	Pin for charge pump capacitor Connection to C3P with a capacitor.
C4P	I/O	9	Pin for charge pump capacitor Connection to C4N with a capacitor.

C4N	I/O	10	Pin for charge pump capacitor Connection to C4P with a capacitor.
VCP1	O	16	Internal DC/DC Output pin. Connect to ground with a capacitor to stabilize the voltage. Connect to V0 for normal application, even if internal DC/DC is not used.
VCP2	O	13	Intermediate DC/DC output. Connect to ground with a capacitor to stabilize the voltage.
VCP3	O	8	Intermediate DC/DC output. Connect to ground with a capacitor to stabilize the voltage.
COM0	O	32, 127	Common electrode output terminals. There are two pads of this signal, locate at different side of the chip for more flexibility on PCB layout.
SEG[92:1]	O	34 - 125	Segment driving output terminals.
SEG0	O	33, 126	Background Segment driving output terminals. There are two pads of this signal, locate at different side of the chip for more flexibility on PCB layout.
CL	I	139	External clock input pin.
RES#	I	134	This pin is the reset signal input. This pin is internally pulled up. When the pin is low, initialization of the chip is executed. Keep this pin high during normal operation.
SPI_CE	I	131	This pin is the chip select input connecting to the MCU.
SPI_CLK	I	130	Data clock pin.
SPI_MOSI	I	128	Data master out, slave in.
SPI_MISO	I	129	Data master in, slave out. This pin is in high impedance stage when there is no output.
ADDR_MAP	I	137	Address setting pin. Indicates whether the IC uses the high memory (ADDR_MAP=1) or low memory address (ADDR_MAP=0) in address space
BUSY[1:0]	O	133, 132	An output pin that indicates the IC is outputting the driving waveform.
TSENSE	O	140	Test pin. Keep NC during normal operations
TR[11:0]	I	20-31	Testing Reserved pins. Keep NC during normal operations
TPA	O	141	Test pin. Keep NC during normal operations

7 FUNCTIONAL BLOCK DESCRIPTION

The device is used to drive a 93 segments (including background) passive direct drive display. It composes of 92 Segment drivers, 2 Background Segment drivers and 2 Common drivers.

The device can drive high voltage at 13~30 Volts signal simultaneously according to the stored image data.

7.1 MCU Interface

The IC has a slave SPI interface, which is comprised of 4 signals, plus one configuration pin:

SPI_MOSI — Data master out, slave in. Input to EPD display driver IC.
SPI_MISO — Data master in, slave out. Output from EPD display driver IC.
SPI_CLK — SPI Clock. Input to EPD display driver.
SPI_CE — Chip enable. Input to EPD display driver.
ADDR_MAP — Indicates whether the IC uses the high memory (*ADDR_MAP*=1) or low memory addresses (*PAGE*=0) in address space

SPI transactions are 32 bits in length. These 32 bits are organized into several fields.

The first field is a single bit (the first bit of the transaction) which indicates whether the transfer is a read or a write action (high for a write).

The next field is the address field. This field is comprised of 6 bits (A0-A5—the 2nd through the 7th bits of the SPI transaction). The address indicates the data register that is to be accessed (read from and possibly written to).

Addresses 0x00 to 0x05 are special "command" registers, which contain a set of command bits which control the operation of the IC. The command register is accessed any time addresses 0x00 to 0x05 are written to — regardless of the state of the ADDR_MAP pin. The command page (addresses 0x00 to 0x05) should be written any time addresses 0x00 to 0x05 are decoded (whether ADDR_MAP is high or low).

The ADDR_MAP pin indicates whether the IC is mapped to the low memory locations (addresses b000000-b011111) or the high memory locations (b100000-b111111). If the ADDR_MAP pin is low, the IC should only decode addresses where the Address5 bit is low. If the ADDR_MAP pin is high, then the IC should decode addresses where Address5 is high. All other addresses (with the exception of addresses 0x00 to 0x05) should be ignored and the MISO pin should output logic zeros (low) for the duration of that particular transaction. The ADDR_MAP pin is intended to be used to configure a particular IC by tying it high or low on the PCB—it is not intended to be changed "on-the-fly".

The next field in the SPI transaction (the 7th bit) is a special bit called the "dead" bit. It is essentially a placeholder and does not contain any data. This placeholder allows a full clock period for the address to be decoded by the logic before receiving the data portion of the transaction.

The final field is comprised of 24 bits of data (D0-D23). This is the data that is written to (in a write transaction) and read from whatever address register is encoded in A0-A6. If an address is decoded for a register which is not physically realized in the IC, then logic zeros will be output on the MISO pin for the remainder of the transaction.

Field	# of bits	Content
1	1	Read / Write
2	6	Address (IC and register)
3	1	Dead bit
4	24	Data / Command
Total	**32**	

7.2 Data RAM

The driver has an embedded 93x2 bits data RAM. The data RAM content will be updated to panel only after sending register "Update". For the relation between RAM data and the output waveform of driver, please refer to section 7.7.

7.3 Frequency Divider

External clock is required to input into CL pin. The frequency divider is used to divide the income clock signal for IC operations.

7.4 DC / DC Converter

A low power, high multiplier charge pump DC/DC is built into SSD1621.

7.5 VCI charge pump regulator

Regulate VCI from VBAT for charge pump operations. This regulator can be turned on/off by register setting.

7.6 Temperature sensing circuit

The IC has temperature sensing circuit and the sensed value will be put into register through ADC.
The temperature sensor reading is in 6 bit format (64 steps).

Table 7-1 – Sensor reading and temperature look up table

Typical Temperature (°C)	Sensor reading
-10	010100
-5	010101
0	010110
5	011000
10	011001
15	011011
20	011100
25	011101
30	011111
35	100000
40	100010

7.7 Segment and Common output

After all image data is stored in the data registers, the device is ready to drive the selected voltage to the display. After setting the display update register, each output pin drives voltage according to the corresponding stored data.

After power on and reset, all outputs are set at V_{SS}.

The driver can output the preset data 1, data 0 waveform.

Figure 7-1: Output waveform (Polarity bit = 0)

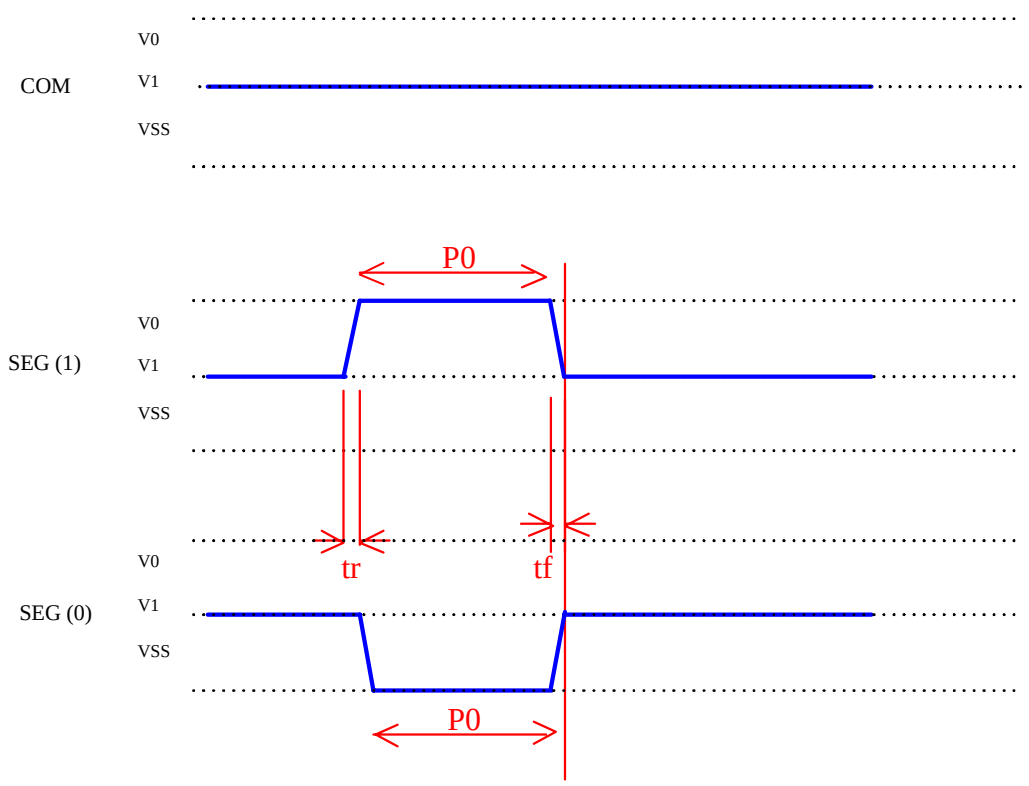


Figure 7-2: Output waveform (Polarity bit = 1)

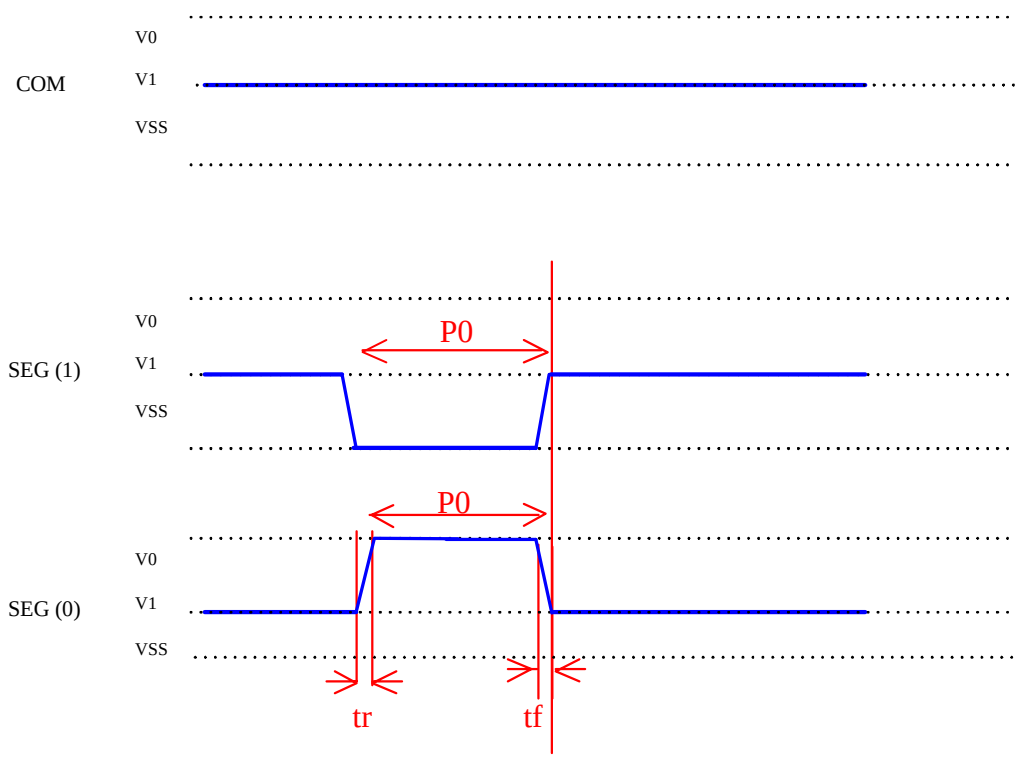


Table 7-2: Driving Waveform Timing Diagram

Item	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Rise time	Tr_com	0.5nF, Vss to V_1 or V_1 to V_0	COM SEG0			1	ms
Rise time	Tr_icon	0.025nF, Vss to V_1 or V_1 to V_0	SEG[92:1]			1	ms
Fall time	Tf_com	0.5nF, V_1 to Vss or V_0 to V_1	COM SEG0			1	ms
Fall time	Tf_icon	0.025nF, V_1 to Vss or V_0 to V_1	SEG[92:1]			1	ms
Update pulse period	P0	*	All	20		5120	ms

* These duration are programmable. Please refer to register table.

8 REGISTER TABLE

Table 8-1: Register Table

Register Name	Description	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Common set 0	Display update		Update	OutputOff					
Common set 1	Update timing	P0[7]	P0[6]	P0[5]	P0[4]	P0[3]	P0[2]	P0[1]	P0[0]
Reserved									
Common set 3	Overall timing scaling	CLK2	CLK1	CLK0	CLK_E#				
Common set 4	Waveform options		Polarity			ForceTransition			
Common set 5	Lock registers	LOCK1	LOCK0						
Reserved									
Reserved									
Reserved									
Reserved									
Command Register 1	Analog Control	VCIRegEn	DCDCEn	DC/DCDischarge	BiasEnable	HvBufferEn		TsenseADCEn	TsenseEnable
Command Register 2	Read Status 1	TSEN[5]	TSEN[4]	TSEN[3]	TSEN[2]	TSEN[1]	TSEN[0]		
Reserved									
Reserved									
Reserved									
Reserved									
Data register 1	SEG[23:0]	S23	S22	S21	S20	S19	S18	S17	S16
Data register 2	SEG[47:24]	S47	S46	S45	S44	S43	S42	S41	S40
Data register 3	SEG[71:48]	S71	S70	S69	S68	S67	S66	S65	S64
Data register 4	SEG[89:72]				S92	S91	S90	S89	S88
Reserved for Data									
Reserved for Data									
Reserved for Data									
Reserved for Data									
Reserved									
Reserved									
Reserved									
Reserved									
Reserved									
Reserved									
Reserved									

Register Address	Register Name	Description	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
00	Common set 0	Display update								
01	Common set 1	Update timing								
02	Reserved									
03	Common set 3	Overall timing scaling								
04	Common set 4	Waveform options								
05	Common set 5	Lock registers								
06	Reserved									
07	Reserved									
08	Reserved									
09	Reserved									
0A	Command Register 1	Analog Control	Discharge Duration[1](0)	Discharge Duration[0](0)						
0B	Command Register 2	Read Status 1	BUSY[1]	BUSY[0]						
0D	Reserved									
0E	Reserved									
0F	Reserved									
0C	Reserved									
10	Data register 1	SEG[23:0]	S15	S14	S13	S12	S11	S10	S9	S8
11	Data register 2	SEG[47:24]	S39	S38	S37	S36	S35	S34	S33	S32
12	Data register 3	SEG[71:48]	S63	S62	S61	S60	S59	S58	S57	S56
13	Data register 4	SEG[89:72]	S87	S86	S85	S84	S83	S82	S81	S80
14	Reserved for Data									
15	Reserved for Data									
16	Reserved for Data									
17	Reserved for Data									
18	Reserved									
19	Reserved									
1A	Reserved									
1B	Reserved									
1C	Reserved									
1D	Reserved									
1E	Reserved									
1F	Reserved									

Register Address	Register Name	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	Common set 0	Display update								
01	Common set 1	Local Update timing								
02	Reserved									
03	Common set 3	Overall timing scaling								
04	Common set 4	Waveform options								
05	Common set 5	Lock registers								
06	Reserved									
07	Reserved									
08	Reserved									
09	Reserved									
0A	Command Register 1	Analog Control								
0B	Command Register 2	Read Status 1								
0D	Reserved									
0E	Reserved									
0F	Reserved									
0C	Reserved									
10	Data register 1	SEG[23:0]	S7	S6	S5	S4	S3	S2	S1	S0
11	Data register 2	SEG[47:24]	S31	S30	S29	S28	S27	S26	S25	S24
12	Data register 3	SEG[71:48]	S55	S54	S53	S52	S51	S50	S49	S48
13	Data register 4	SEG[89:72]	S79	S78	S77	S76	S75	S74	S73	S72
14	Reserved for Data									
15	Reserved for Data									
16	Reserved for Data									
17	Reserved for Data									
18	Reserved									
19	Reserved									
1A	Reserved									
1B	Reserved									
1C	Reserved									
1D	Reserved									
1E	Reserved									
1F	Reserved									

9 REGISTER DESCRIPTIONS

***Address 00 to 05h is common registers. i.e. ADDR_MAP bit setting will be ignored when doing register write.**

Address 00h:

Update:
When this bit is set to 1, update will begin. This bit will be reset to 0 after update is started.
Output_Off:
0: Normal operation (Default)
1: All output segments and commons will be set to V_{SS} level.

Address 01h:

P0[7:0]: the pulse duration of the update waveform.
Available setting 20ms to 5120ms in step of 20ms
00000000: 5120ms (Default)
Others: 20ms x P0[7:0]

Address 02h:

Reserved

Address 03h:

CLK[2:0] => the selection of the clock speed of the driving circuit
POR: 32k input clock will generate 20ms for LSB of P0[7:0]
000 : 5ms
001 : 10ms
010 : 20ms (Default)
011 : 40ms
100 : reserved
101 : reserved
110 : reserved
111 : reserved

CLK_E#:
0: Normal operation (Default)
1: External CLK input will be masked off.

Address 04h:

Polarity:
0: Default
When RAM data changed from 0 to 1, SEG goes from V1 to V0.
When RAM data changed from 1 to 0, SEG goes from V1 to VSS.
1: When RAM data changed from 0 to 1, SEG goes from V1 to VSS.
When RAM data changed from 1 to 0, SEG goes from V1 to V0.

Force_Transition:
1: Must be set to 1 during normal operation.
0: Test mode. (Default)

Address 05h:

LOCK[1:0] => lock register
00: Normal operations (Default)
01: Normal operations
10: Normal operations
11: Lock stage. Once these lock bits are set, only unlock bit can be set. No other register setting are accepted
At lock mode, reset pulse width requirement will be increased.

Address 0Ah: VCI_Reg_En:
0: Disable VCI regulator (Default)
1: Enable VCI regulator

DCDC_En:
0: Disable DC/DC (Default)
1: Enable DC/DC

DC/DC_Discharge
0: Disable (Default)
1: Enable DC/DC discharge function for 4ms.

Bias_En
0: Disable divider (Default)
1: Enable divider

HV_Buffer_En
0: Turn off HV buffer (Default)
1: Turn On HV buffer for V1 generation.

Tsense_Digital_En
0: Disable digital output of temperature sensing (Default)
1: Enable ADC function and allow digital output of temperature sensing block.

Tsense_En
0: Disable Temperature sensing function (Default)
1: Enable TSENSE sensing function.

DC/DC Discharge Duration
Discharge Duration [1:0] => the selection of the time duration of DC/DC discharge
00: 4ms (Default)
01: 2ms
10: 8ms
11: 16ms

Address 0Bh: Read status of TSEN[5:0] and BUSY
TSEN[5:0]: 6 bit of the temperature value from the temperature sensor
BUSY[1]:
0: Indicates no waveform update is on going
1: Indicates the chip is running update waveform.
BUSY[0]:
Don’t care

Address 10h: Write the RAM data of S0 to S23
Address 11h: Write the RAM data of S24 to S47
Address 12h: Write the RAM data of S48 to S71
Address 13h: Write the RAM data of S72 to S92

Address 14h: Reserved for data
Address 15h: Reserved for data
Address 16h: Reserved for data
Address 17h: Reserved for data

Address 1A-1Fh:
Address reserved for production testing use.

10 ABSOLUTE MAXIMUM RATINGS

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Logic supply voltage	-0.5 to +4.0	V
V_{DDIO}	I/O supply voltage	-0.5 to V_{DD}+0.5	V
V_{CI}	DC/DC circuit supply voltage	-0.5 to +4.5	V
V_{BAT}	Battery supply power	-0.5 to +4.5	V
V_0	Panel driving voltage	-0.5 to +33	V
V_{IN}	Logic Input voltage	-0.5 to V_{DD}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DD}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to 150	°C

Note:
Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
The device may be light sensitive. Caution should be taken to avoid exposure of the front side (the pad side) of this device to any light source during normal operation. This device is not radiation protected.

11 OPERATING RATINGS

Table 11-1: DC Operating Rating

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.4		3.5	V
V_{DDIO}	I/O supply voltage		2.4		V_{DD}	V
V_{BAT}	VCI regulator supply voltage		2.8		4.2	V
V_{CI}	Charge pump power supply		2.4		3.5	V
V_0	Driver supply voltage		13		32	V
V_1	Driver supply voltage			V_0/2		V

12 ELECTRICAL CHARACTERISTICS

12.1 DC Electrical Characteristics

The following specifications apply for: Vss=0V, V_{DD}=+2.4V, V_{DDIO} = +2.4V, V_{BAT}= +3.5V

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{DD}	V_{DD} operation voltage		V_{DD}	2.4		3.5	V
V_{DDIO}	V_{DDIO} voltage		V_{DDIO}	2.4		V_{DD}	V
V_0	V_0 operation voltage		V_0	13		32	V
V_{BAT}	V_{BAT} operating voltage		V_{BAT}	2.8		4.2	V
V_{CI}	DC/DC input voltage		V_{CI}	2.4		3.5	V
V_{CI}	VCI regulator output voltage		V_{CI}		3.0		V
V_{CI}	DC/DC input voltage	V_{cp0} = 30V typical	V_{CI}	2.75			V
V_{CP0}	DC/DC output voltage	V_{CI}=3.0V, Loading at V_0 = 5nF, 1MΩ	V_0	28	30	32	V
V_1	V_1 output voltage	V_0=30V, Loading at V_1 = 5nF, 1MΩ	V_1	V_0/2 x 0.98	V_0/2	V_0/2 x 1.02	V
	V_0, V_1 matching	Abs((V_0-V_1) / (V_1 – V_{SS}))		0.98	1	1.02	
VIH	High level input voltage			0.8V_{DDIO}			V
VIL	Low level input voltage					0.2V_{DDIO}	V
VOH	High level output voltage	IOH = -100uA		0.9V_{DD}			V
VOL	Low level output voltage	IOL = 100uA				0.1V_{DD}	V
ILIN		Vin = GND		-1.0			uA
Cin	Logic input pin capacitance					10	pF
Ron_SEG	Segment ON resistance	V_0=30V, dV=0.5V	SEG[92:1]		10k		Ohm
Ron_S0	Background segment ON resistance	V_0=30V, dV=0.5V	SEG0		1k		Ohm
Ron_COM	Common ON resistance	V_0=30V, dV=0.5V	COM		1k		Ohm
Islp_vdd	Sleep mode current	V_{DD}=2.8V DC/DC off No clock No output load	V_{DD}		1	13	uA

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Islp_vddio	Sleep mode current	V_{DDIO} = V_{DD} =1.8V DC/DC off No clock No output load	V_{DDIO}		1	7	uA
Islp_vci	Sleep mode current	V_{DDIO} = V_{DD} =1.8V V_{CI}=3V DC/DC off No clock No output load	V_{CI}		1	5	uA
Islp_vbat	Sleep mode current	V_{DDIO} = V_{DD} =1.8V V_{CI} regulator off V_{BAT}=3.5V DC/DC off No clock No output load	V_{BAT}		1	5	uA
Iop_vdd	Operating current	V_{DD}=V_{DDIO}=1.8V DC/DC on V_0=30V CL=32kHz No output load Segment not changing	V_{DD}		20	110	uA
Iop_vci	Operating current	V_{DD}=V_{DDIO}=1.8V VCI=3.0V DC/DC on V_0=30V CL=32kHz VCOM / VSEG all tie to V_1	VCI		800	1310	uA
Iop-vbat	VBAT Operating Current	DC/DC on CL=32kHz No output load V0 = 30V All COM/ SEG = V1	VBAT		1050	2650	uA

Table 12-2: Temperature sensor characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
	Temperature senor operating range			-45		95	°C
RES_{TS}	Resolution of temperature sensor				3.5		°C
Acc_{TS}	Accuracy of temperature sensor reading			-3.5		+3.5	°C

13 AC CHARACTERISTICS

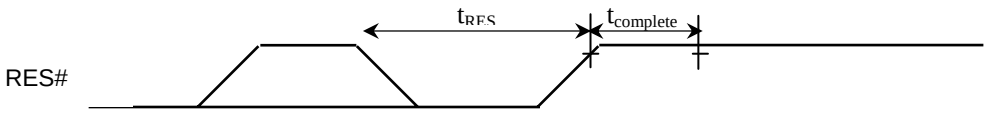
13.1 Reset timing

Table 13-1: Reset Timing Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.8V, V_{DDIO}=1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{RES-unlock}$	Reset pulse width (unlocked)			20	us
$t_{RES-lock}$	Reset pulse width (locked)	10			ms
$t_{Complete}$	Reset completion time			20	us

Figure 13-1: Reset timing diagram



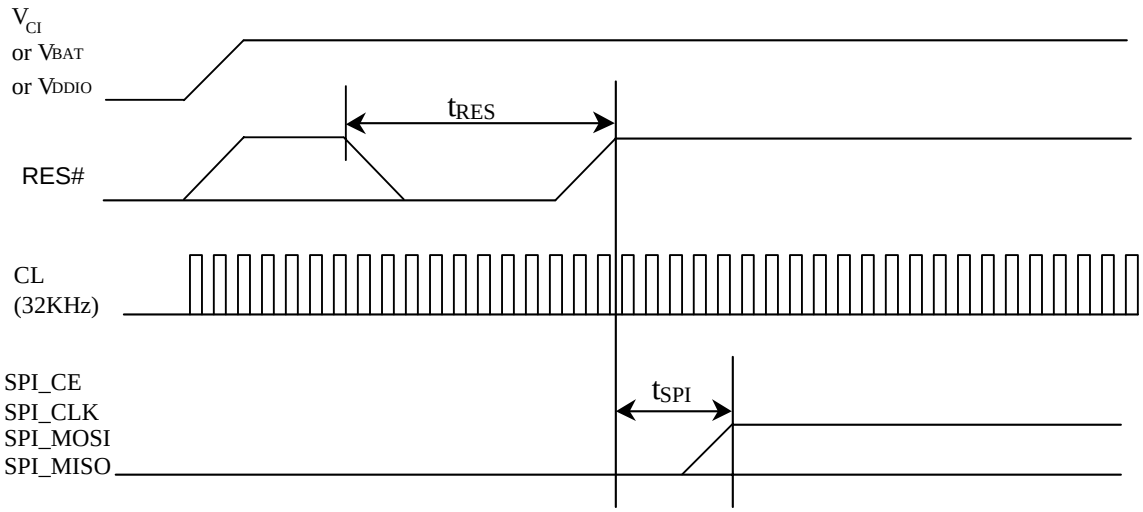
13.2 Power Up Sequence

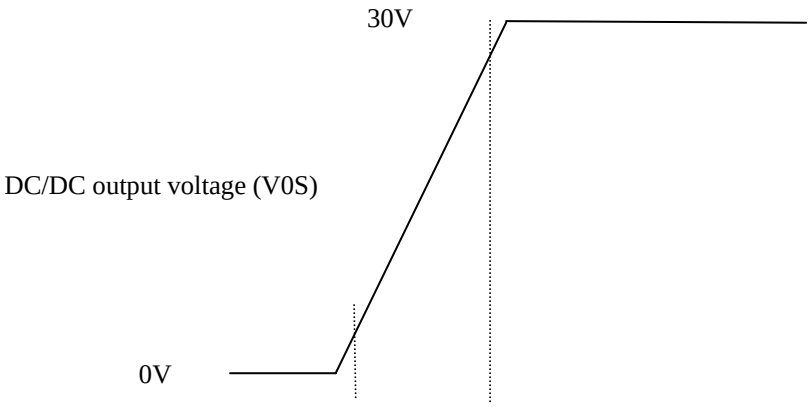
Table 13-2: Power up timing characteristics

Symbol	Characteristic	Min.	Typ.	Max	Units
t_{RES}	Reset Pulse Width	10			ms
t_{SPI}	SPI Stable Time	100			ns
	DC/DC output steady time (Refer to application circuit Figure 14-1)		400		ms

Note: In all cases, VDDIO and VCI (or V_{BAT}) power up sequence should not have any impact on the driver/ display functionalities/ performance.
Including the IC is idling with VBAT = 2.8 to 4.2V, while V_{DD} = 0V to VIH.
CL clock should be present during the reset period.

Figure 13-2: Power up timing diagram





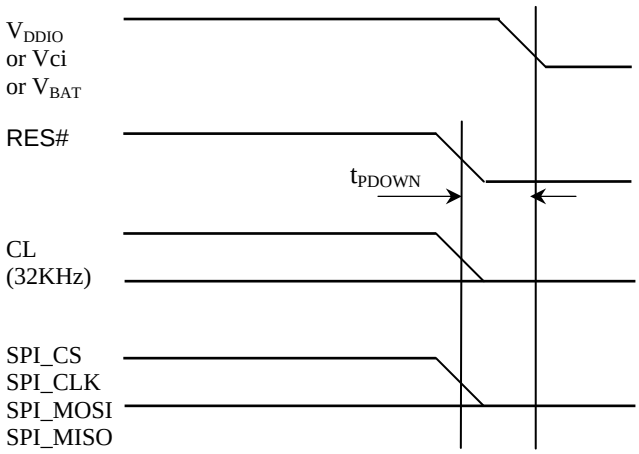
13.3 Power Down Sequence

Table 13-3: Power down timing characteristics

Symbol	Characteristic	Min.	Typ.	Max	Units
t_{PDOWN}	Power Hold Time	100			ns

Note: The IC performs DC/DC discharge on all high voltages during abnormal power supply removal to avoid any functional corruption upon next power up. Including the IC is idling with VBAT = 2.8 to 4.2V, while V_{DD} = 0V to VIH.

Figure 13-3: Power down timing diagram



13.4 SPI Timing

Table 13-4: SPI Timing Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.8V, T_A = -20 to 70 °C)

Symbol	Parameter	Time min (ns)
t_{CESU}	Time CE has to be low before the first rising edge of CLK	20
t_{CEHLD}	Time CE has to remain low after the last falling edge of CLK	20
t_{CEHIGH}	Time CE has to remain high between two transfers	20
t_{CKPER}	Clock period of CLK (1)	38.46
t_{CKHIGH}	Part of the clock period where CLK has to remain high	15
t_{CLKLOW}	Part of the clock period where CLK has to remain low	15
t_{MOSISU}	Time MOSI has to be stable before the next rising edge of CLK	5
$t_{MOSIGHLD}$	Time MOSI has to remain stable after the rising edge of CLK	5
t_{MISOSU}	Time MISO will be stable before the next rising edge of CLK	5
$t_{MISOHLD}$	Time MISO will remain stable after the falling edge of CLK	5
$t_{MISODIS}$	Time MISO needs to become inactive after the rising edge of CS	5

(1) Equivalent to a maximum clock frequency of 26MHz.

Figure 13-4: SPI Timing Diagram

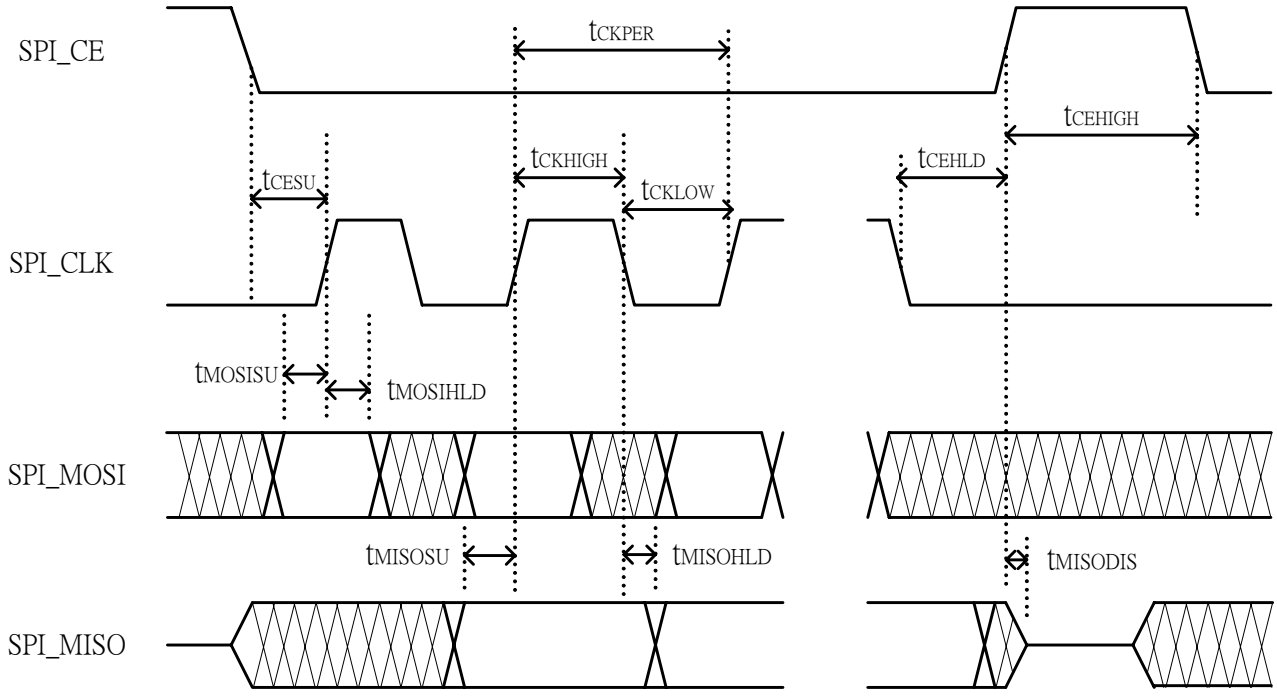


Figure 13-5: Sample SPI Transfer

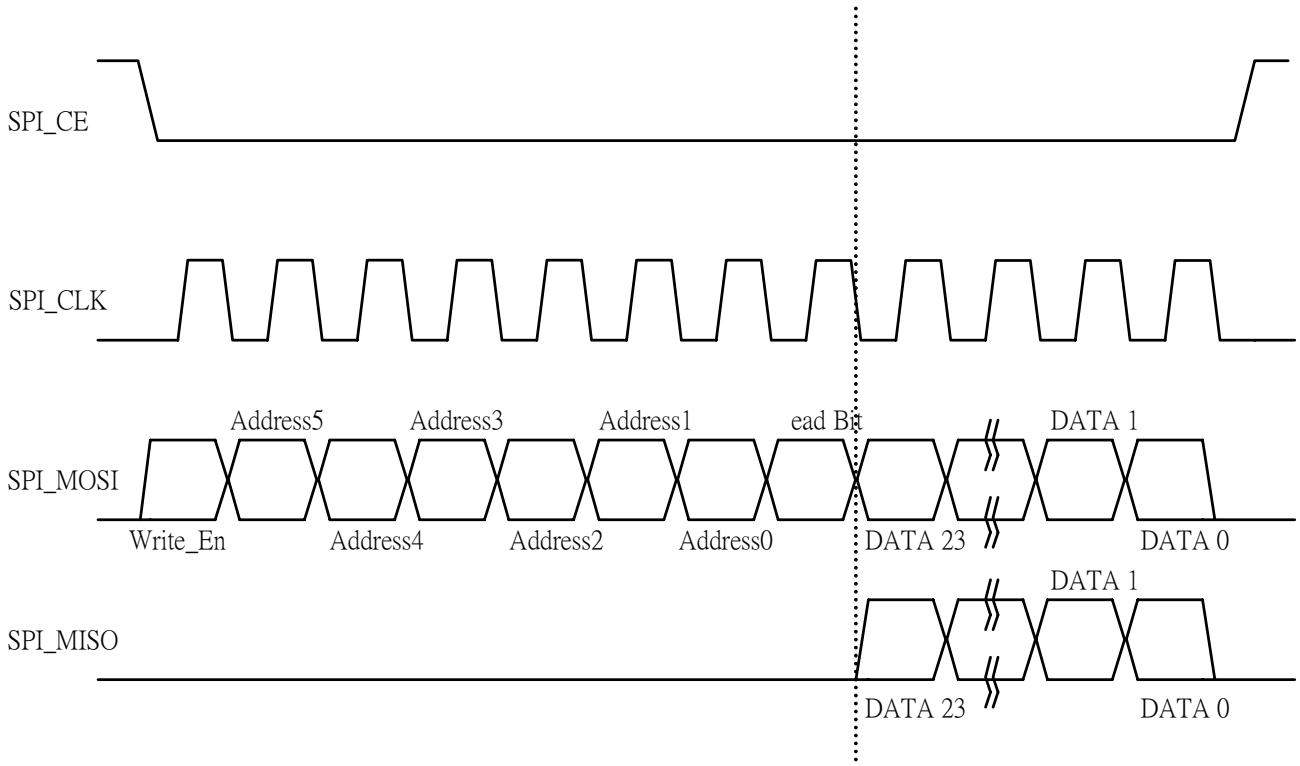
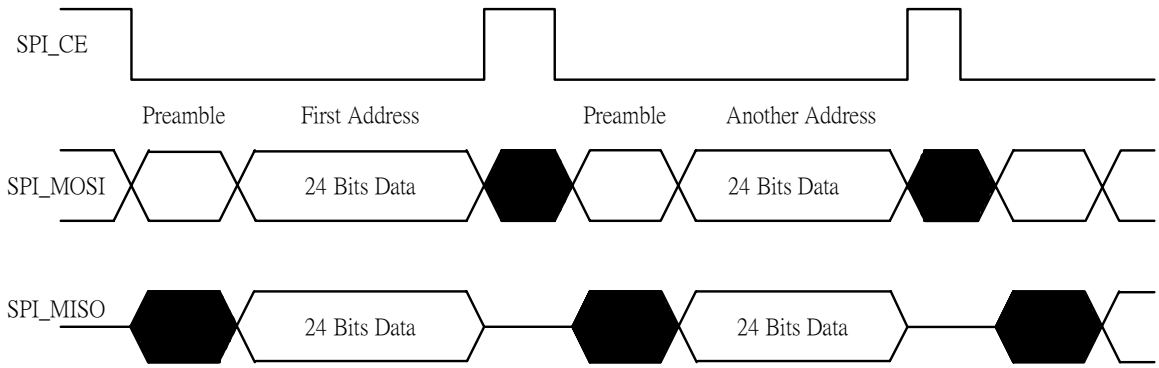


Figure 13-6: Consecutive SPI Transfers



14 APPLICATION CIRCUIT

Figure 14-1: Typical application diagram

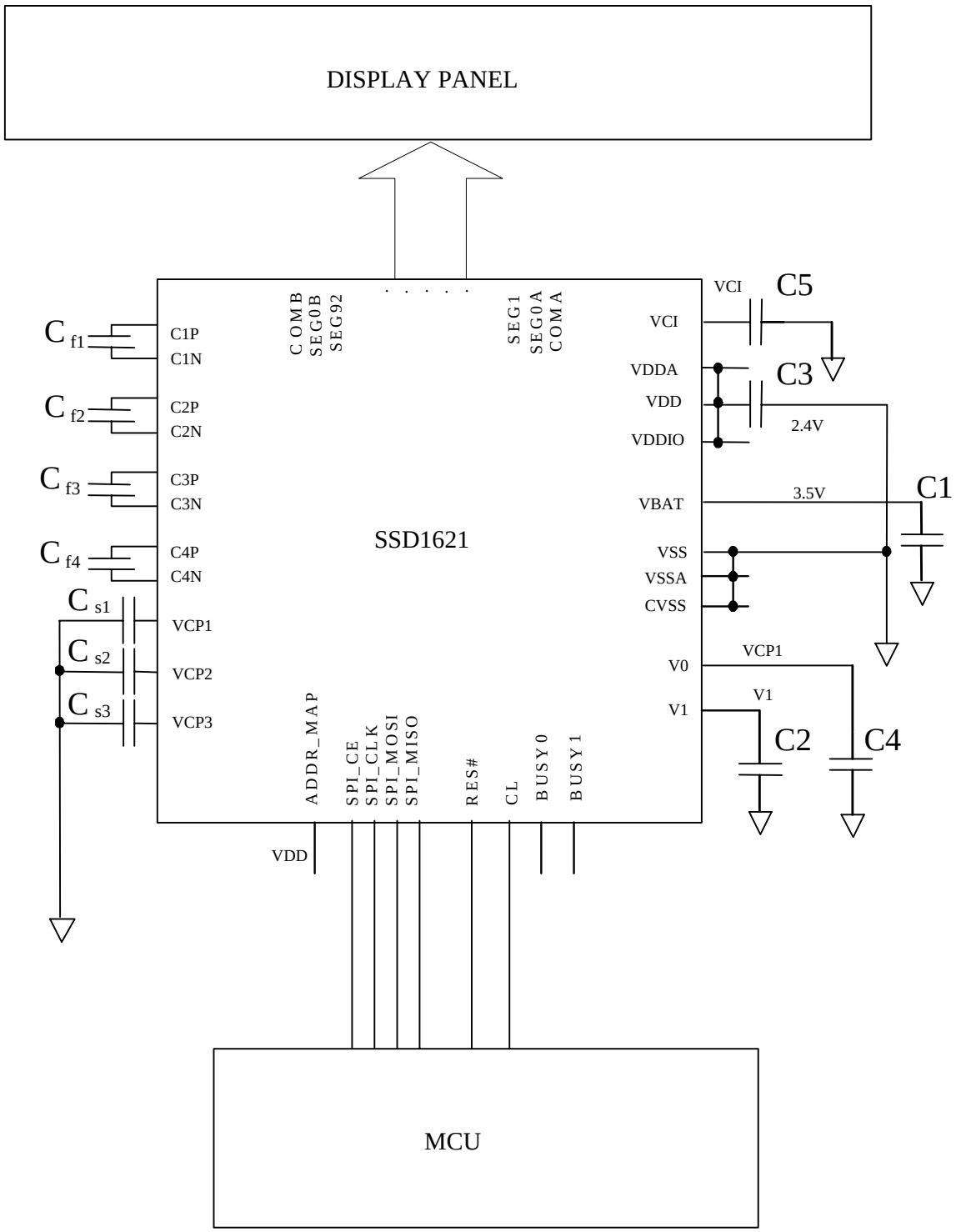
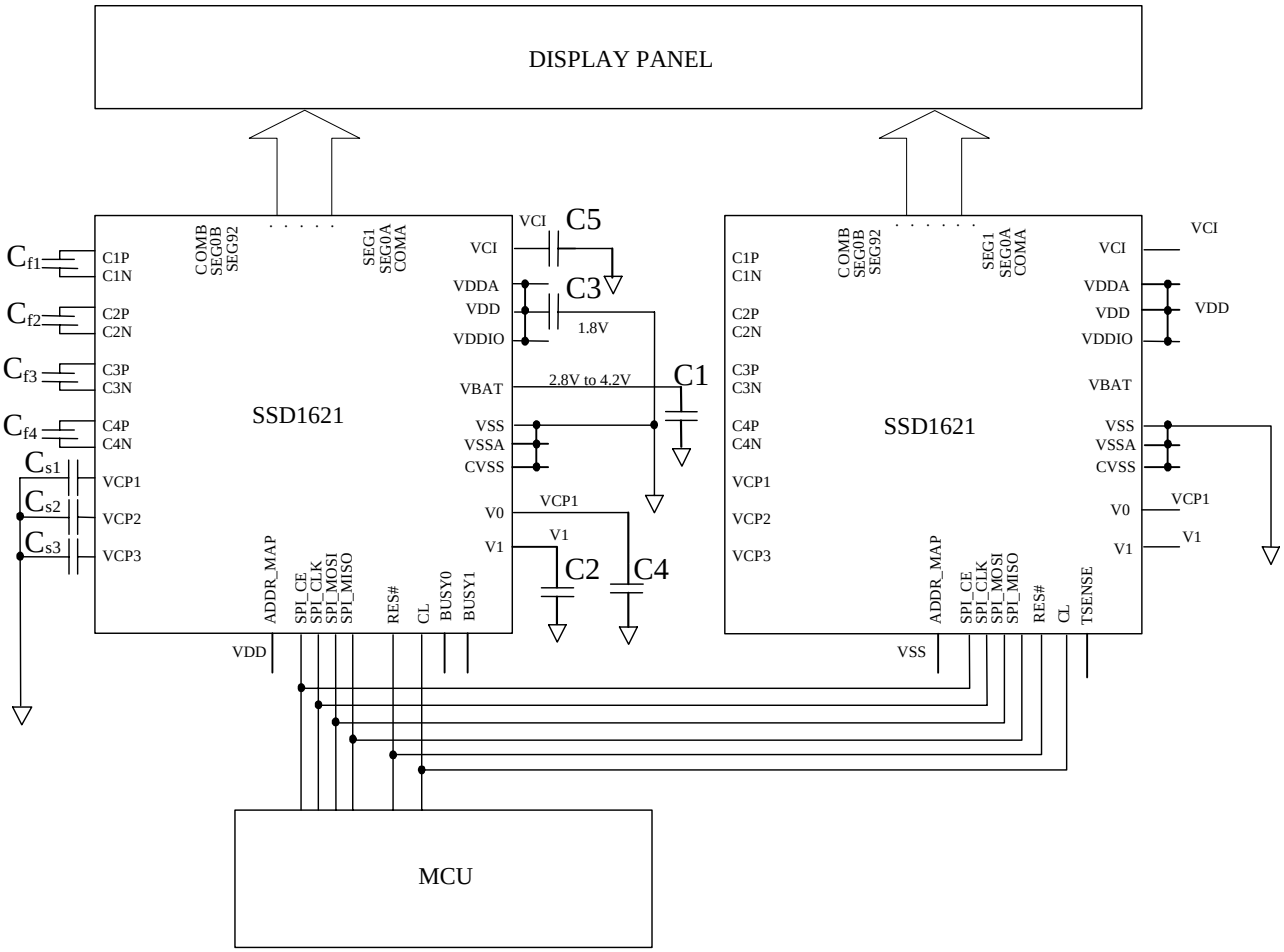


Figure 14-2: Typical application diagram (Cascade mode)



14.1 DC-DC Converter Application Circuit

Figure 14-3: DC-DC converter application diagram

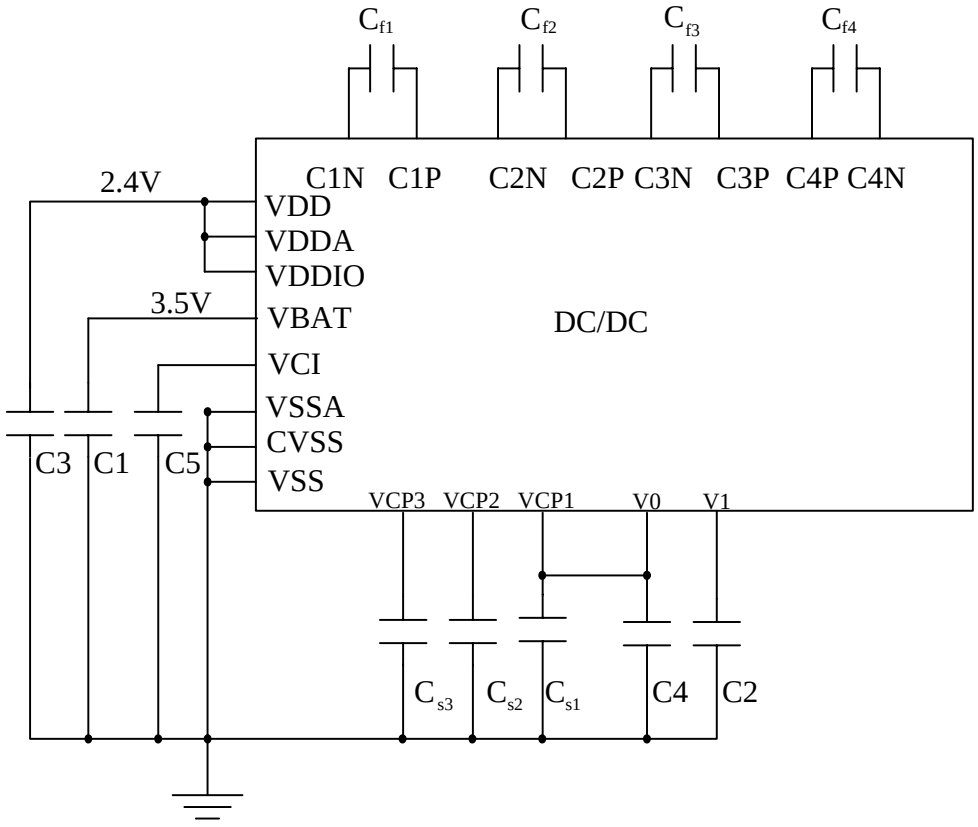


Table 14-1: Reference Capacitor Value

Part reference	Value (uF)	Min Rating
Cf1	2.2	50V
Cf2	2.2	25V
Cf3	2.2	25V
Cf4	2.2	10V
Cs1	1.0	50V
Cs2	1.0	25V
Cs3	0.68	10V
C1	1.0	10V
C2	1.0	25V
C3	1.0	10V
C4	1.0	50V
C5	1.0	10V

- Capacitor values requirement depends on panel loading and voltage setting.

15 APPLICATION FLOW

15.1 Power on / off command sequence

Table 15-1: Typical power on flow

1. Provide power VDDIO and VDD and then
2. Provide power VBAT, within 1ms after VDDIO/VDD on
3. Pull SSD1621 RES# signal L for at least 10ms with 32kHz CL
4. Release RES# to H.
5. Set VCI regulator on, DC/DC on, bias divider on (0x0A)
6. Set Update timing parameter (0x01)
7. Set Overall timing scaling (0x03)
8. Enable Force transition option (0x04)
9. Set data register value (0x10 to 0x13)
10. Issue update (0x00)

Table 15-2: Typical update flow

1. Read busy status of the chip (0x0B)
2. Verify if BUSY[1] = 0 or 1.
    i. If BUSY[1] = 0, the chip is ready for update.
    ii. If BUSY[1] = 1, repeat step 2
3. Set data register value (0x10 to 0x13)
4. Issue update (0x00)
5. Repeat from step 1 for new image update.

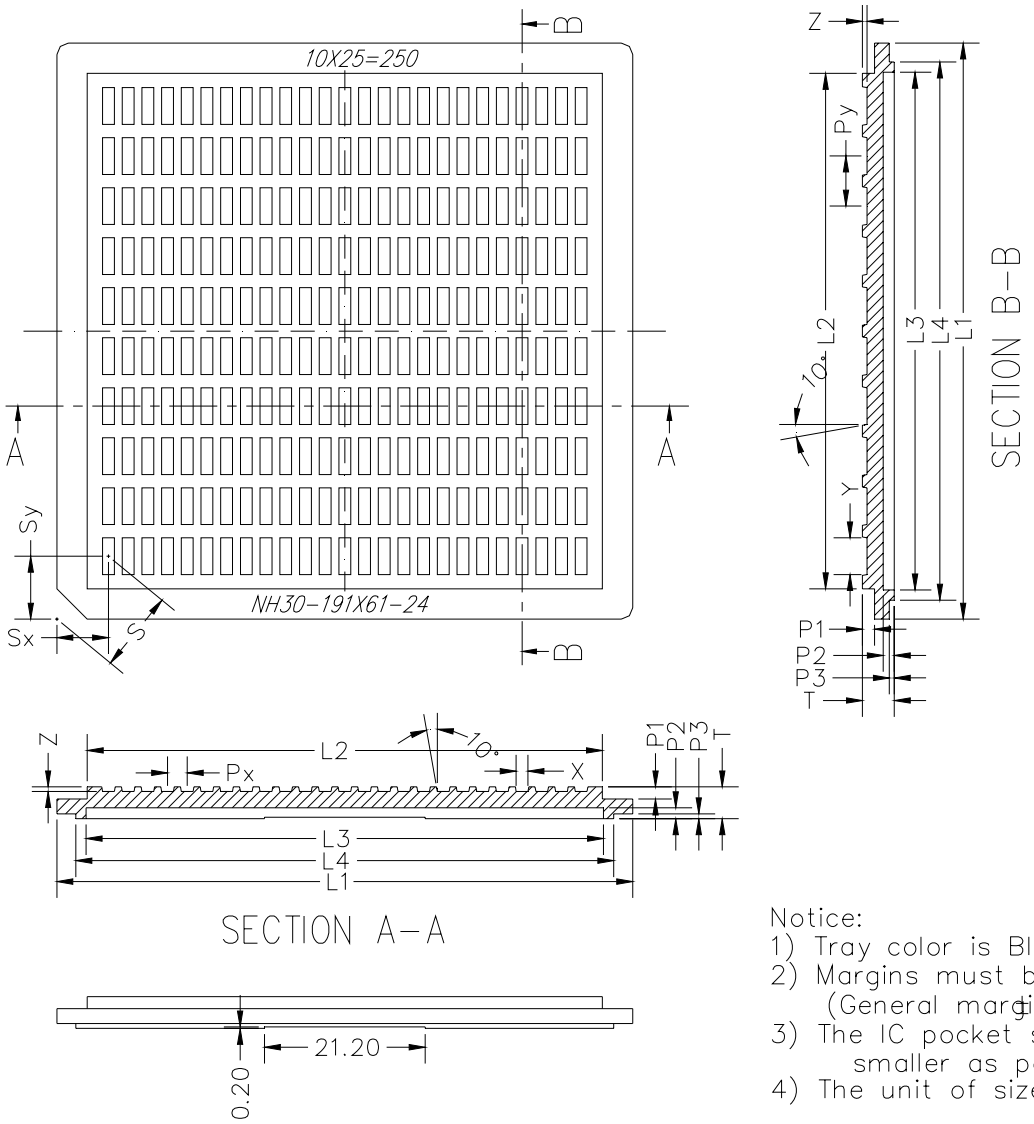
Table 15-3: Typical power off flow

1. Read busy status of the chip (0x0B)
2. Verify if BUSY[1] = 0 or 1.
    i. If BUSY[1] = 0, the chip is ready to be power off
    ii. If BUSY[1] = 1, repeat step 2
3. Set all outputs off (0x00)
4. Set DC/DC off, bias divider off, VCI regulator off (0x0A)
5. Set DC/DC discharge
6. Delay 50ms
7. Power off VBAT
8. Power off VDD/VDDIO within 1ms after VBAT. RES# goes L and stop CL (pull low)

16 PACKAGE INFORMATION

16.1 SSD1621V and SSD1621Z Die Tray Information

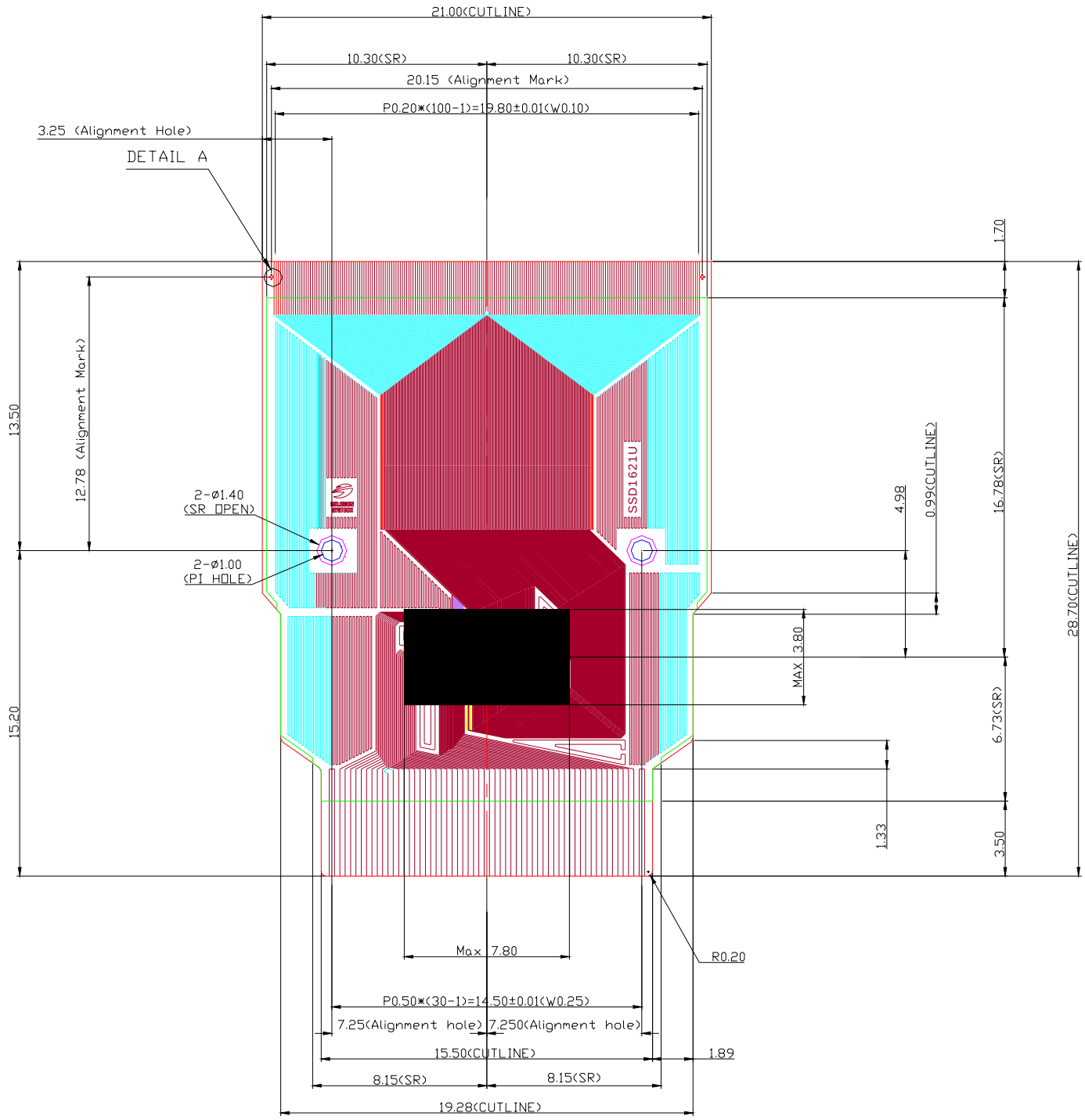
Figure 16-1 : SSD1621V and SSD1621Z die tray information



SPEC	
	MM
(L1)	76.00±0.10
(L2)	68.00±0.10
(L3)	68.30±0.10
(L4)	71.00±0.10
(T)	4.20±0.05
(SX)	6.80
(SY)	8.30
(S)	10.73
(X)	1.56±0.05
(Y)	4.85±0.05
(Z)	0.61±0.05
(Px)	2.60±0.10
(Py)	6.60±0.10
(Nx)	25
(Ny)	10
(N)	250
(P1)	1.60±0.10
(P2)	1.45±0.10
(P3)	0.65±0.10

16.2 SSD1621U Detail Dimension

Figure 16-2 : SSD1621U Detail dimension



NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: KAPTON 150 EN 38±4um
   CU: 8±2um
   SR: 15±10um SN-9000
   (OTHER TOLERANCE: ±0.20mm)
3. SN PLATING: 0.23±0.05um
4. DIE SIZE: 4.95mm x 1.6mm

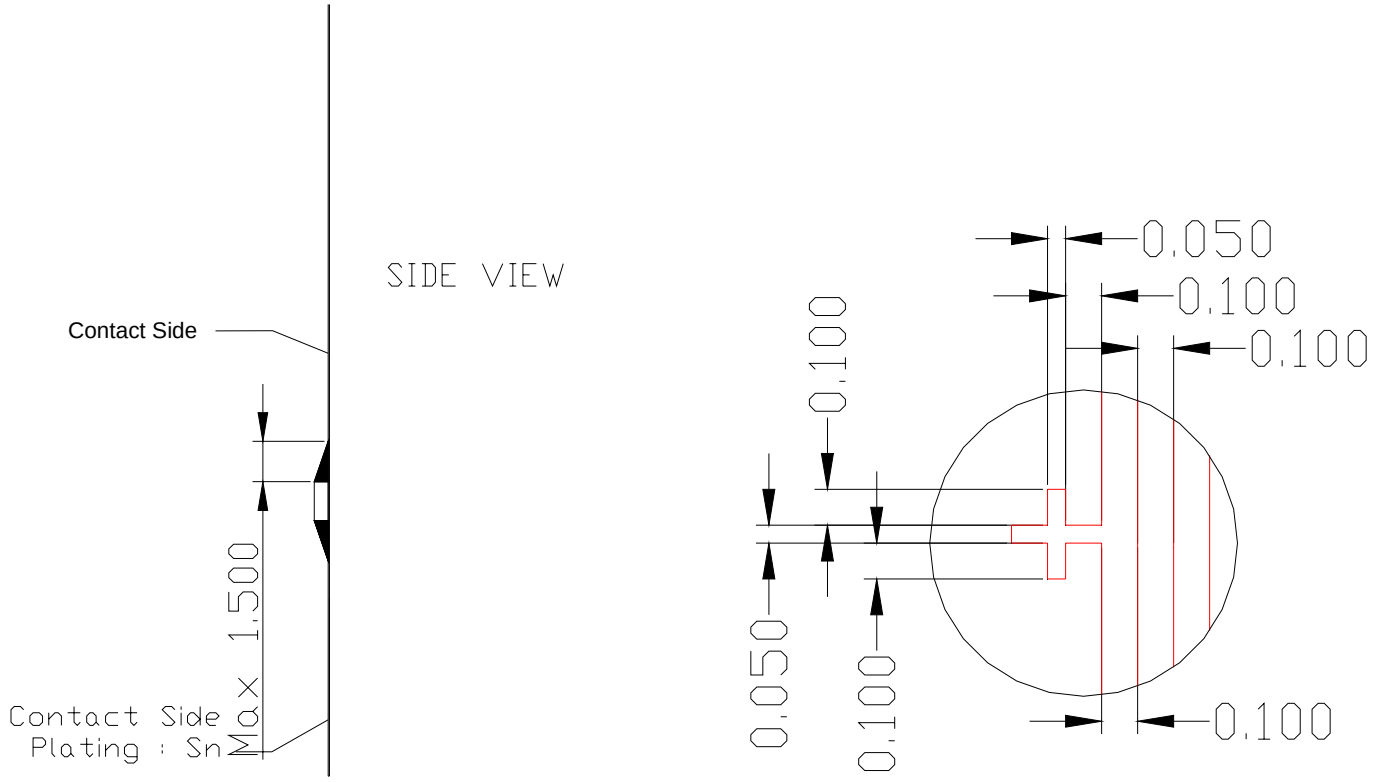


Figure 16-3 : SSD1621U Pin Assignment

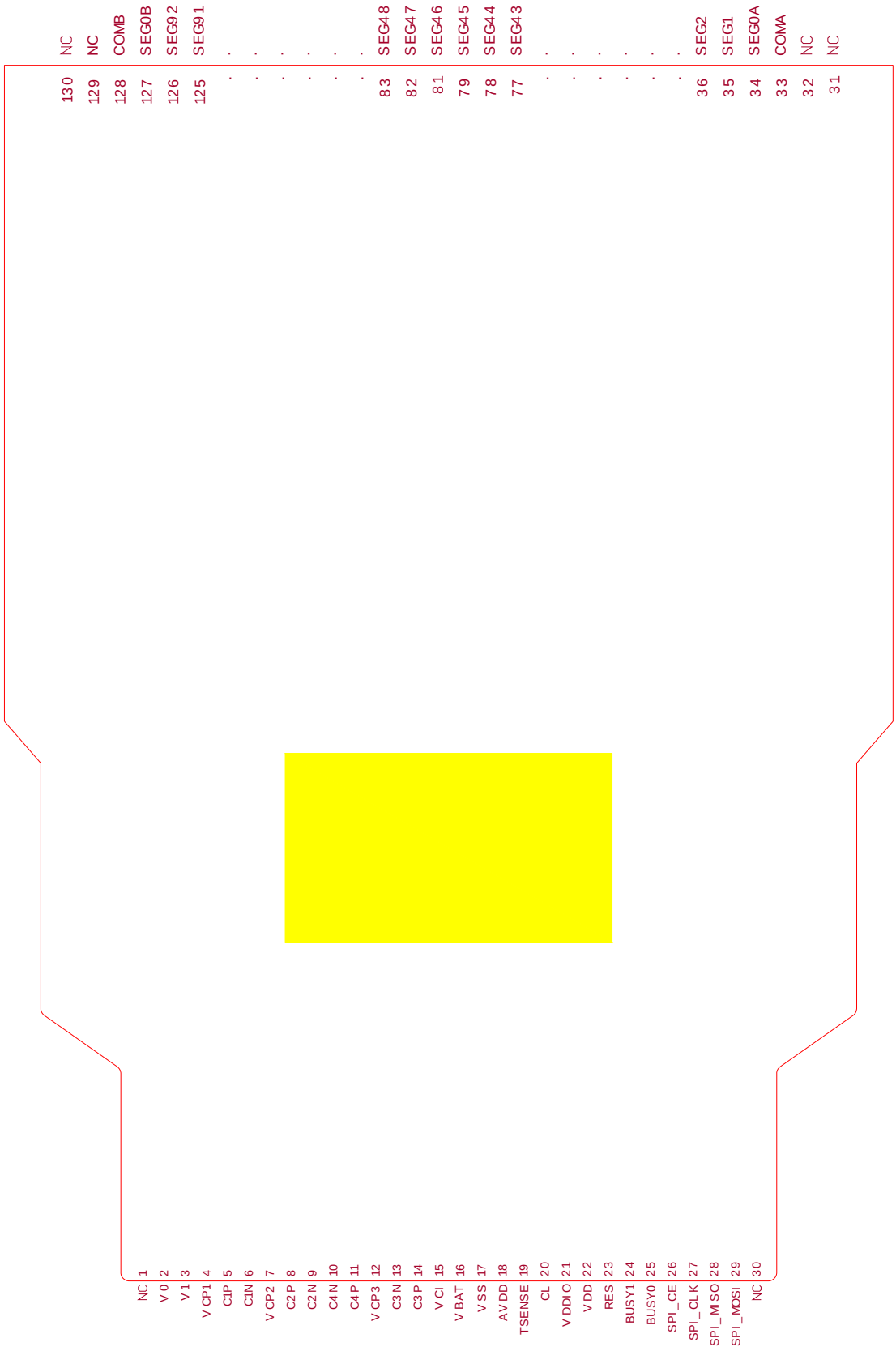


Table 16-1: SSD1621U Pin Assignment Table

Pin No	Pin Name
1	NC
2	V0
3	V1
4	VCP1
5	C1P
6	C1N
7	VCP2
8	C2P
9	C2N
10	C4N
11	C4P
12	VCP3
13	C3N
14	C3P
15	VCI
16	VBAT
17	VSS
18	AVDD
19	ISENSE
20	CL
21	VDDIO
22	VDD
23	RES
24	BUSY1
25	BUSY0
26	SPI_CE
27	SPI_CLK
28	SPI_MISO
29	SPI_MOSI
30	NC
31	NC
32	NC
33	COMA
34	SEG0A
35	SEG1
36	SEG2
37	SEG3
38	SEG4
39	SEG5
40	SEG6
41	SEG7
42	SEG8
43	SEG9
44	SEG10
45	SEG11
46	SEG12
47	SEG13
48	SEG14
49	SEG15
50	SEG16
51	SEG17
52	SEG18
53	SEG19
54	SEG20
55	SEG21
56	SEG22
57	SEG23
58	SEG24
59	SEG25
60	SEG26
61	SEG27
62	SEG28
63	SEG29
64	SEG30
65	SEG31
66	SEG32
67	SEG33
68	SEG34
69	SEG35
70	SEG36
71	SEG37
72	SEG38
73	SEG39
74	SEG40
75	SEG41
76	SEG42
77	SEG43
78	SEG44
79	SEG45
80	SEG46

Pin No	Pin name
81	SEG47
82	SEG48
83	SEG49
84	SEG50
85	SEG51
86	SEG52
87	SEG53
88	SEG54
89	SEG55
90	SEG56
91	SEG57
92	SEG58
93	SEG59
94	SEG60
95	SEG61
96	SEG62
97	SEG63
98	SEG64
99	SEG65
100	SEG66
101	SEG67
102	SEG68
103	SEG69
104	SEG70
105	SEG71
106	SEG72
107	SEG73
108	SEG74
109	SEG75
110	SEG76
111	SEG77
112	SEG78
113	SEG79
114	SEG80
115	SEG81
116	SEG82
117	SEG83
118	SEG84
119	SEG85
120	SEG86
121	SEG87
122	SEG88
123	SEG89
124	SEG90
125	SEG91
126	SEG92
127	SEG0B
128	COMB
129	NC
130	NC

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol  . Hazardous Substances test report is available upon requested.

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