SSD1603

Advance Information

132 x 64 Bistable Display Driver with Controller

Appendix: IC Revision history of SSD1603 Specification

Version	Change Items	Effective Date
1.0	Initial Release	05-May-09

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1603 is a single-chip CMOS Bistable display driver with controller for dot-matrix type Bistable display. It consists of high-voltage driving outputs for driving maximum 132 Segments x 64 Commons. Charge Pump, On-Chip Oscillator and Bias Divider are built in for minimal system area.

2 FEATURES

- Power supply:
  - o V_{DD} = 2.4V to 3.5V for IC logic and analog
  - o V_0 = 14.0V to 35.0V for Panel driving
  - o V_{DDIO} = 1.6V to V_{DD} for MCU interface
- Resolution: 132 x 64 dot matrix panel
- Extra 2 dummy segments and 2 dummy commons for dummy ITO area driving
- On chip 132 x 64 bit graphic display RAM
- Charge pump with 35V output
- Circuit selectable charge pump multiplier ratio
- On chip charge pump or external panel driving power supply selectable
- Column remap and COM remap scan function
- Vertical scroll by COM and RAM display offset
- Partial COM display update
- Programmable duration for each driving phase.
- Programmable MUX ratio
- Programmable on chip bias, 1/4, 1/5, 1/6, 1/7, 1/8, 1/9
- 8-bit 80 parallel / 8-bit 68 parallel / 3 & 4-wire SPI support / I^2C interface
- Slim die design for COF / TCP

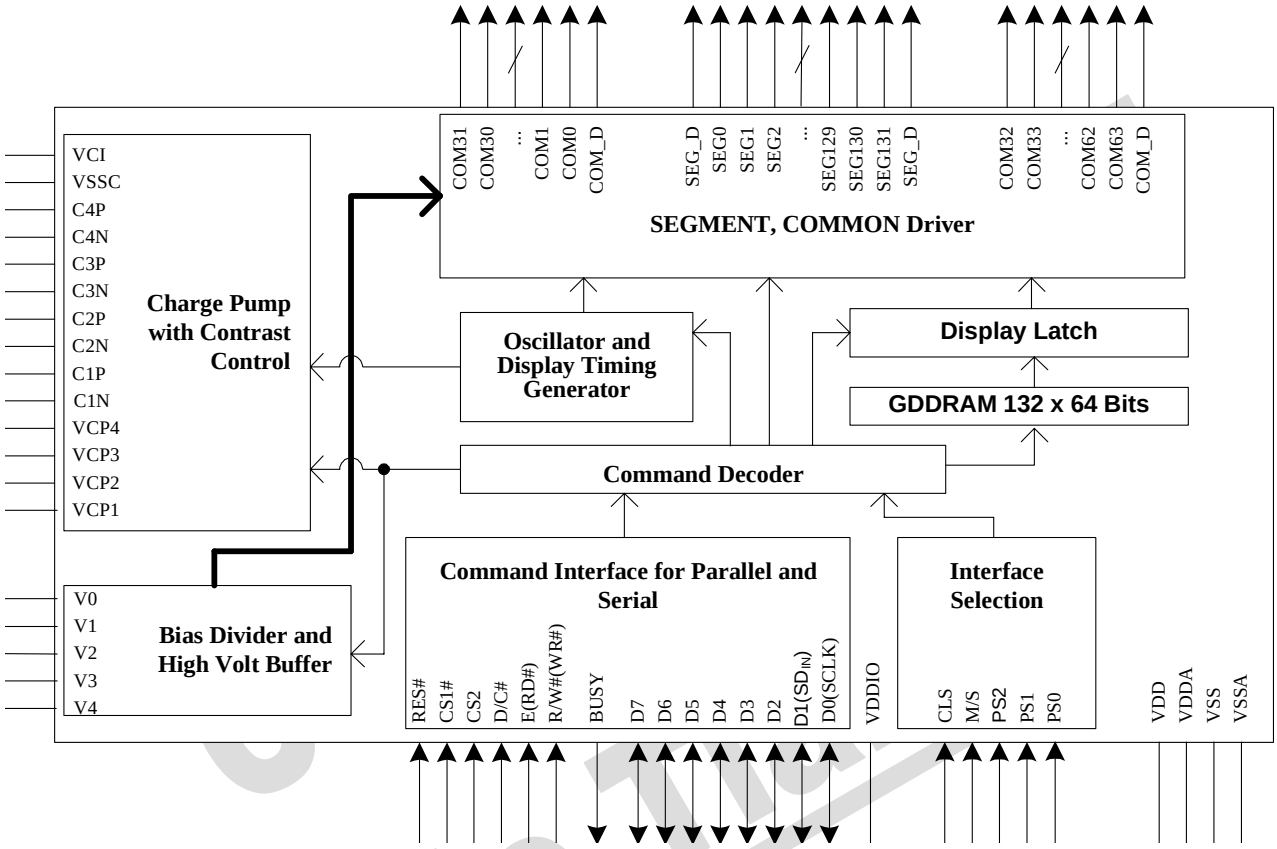
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1603Z	132	64	Gold Bump Die	Page 11	• Min SEG,COM pad pitch: 40um • Min pad pitch: 40um

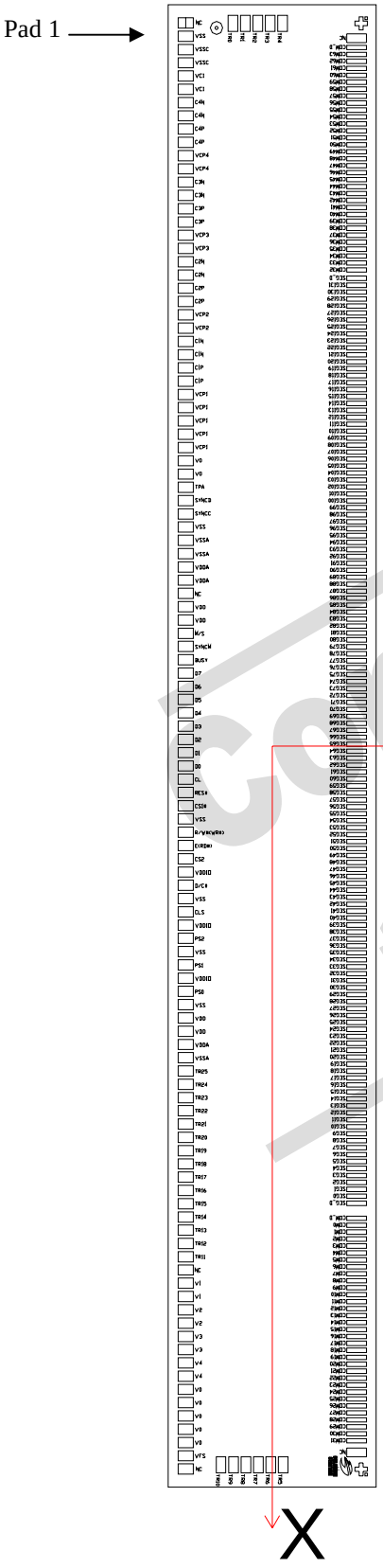
4 BLOCK DIAGRAM

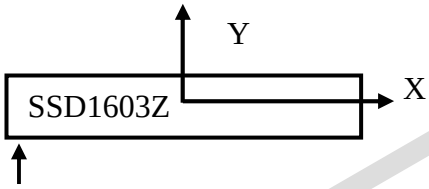
Figure 4-1 : Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1603Z Die Drawing





Pad 1,2,3,…->110
Gold Bumps face up

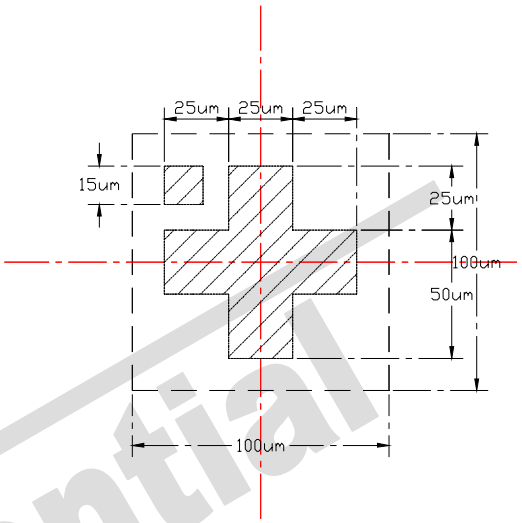
Die Size	8.5mm x 1.3mm
Die Thickness	533 um ± 25 um
Min I/O pad pitch	76.3 um
Min SEG pad pitch	40 um
Min COM pad pitch	40 um
Bump Height	Nominal 15 um

Bump Size		
Pad #	**X [um]**	**Y [um]**
1-110	59	92
118-317	25	120
117,318	50	120
111-116, 319-323	92	59

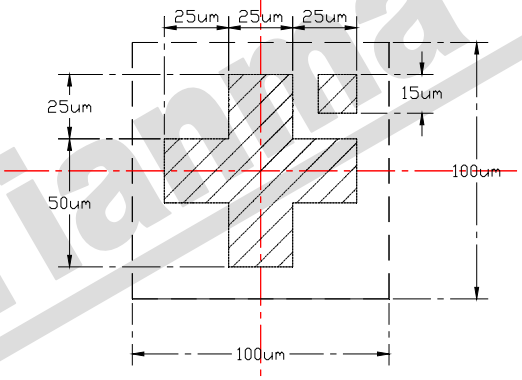
Figure 5-2 : SSD1603Z Alignment Marks Dimension

Note
(1) Diagram showing the die face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold bump.

Center
(-4156,545)
Size
75umx75um



Center
(4160,545)
Size
75umx75um



Center
(-4130,-341)
Diameter
75um

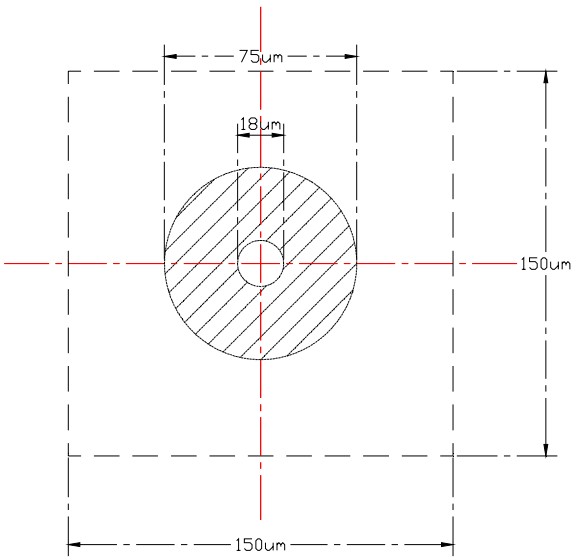


Table 5-1 : SSD1603Z Bump Die Pad Coordinates

Pin #	Pin name	X	Y
1	NC	-4158.4	-530.0
2	VSS	-4082.1	-530.0
3	VSSC	-4005.8	-530.0
4	VSSC	-3929.5	-530.0
5	VCI	-3853.2	-530.0
6	VCI	-3776.9	-530.0
7	C4N	-3700.6	-530.0
8	C4N	-3624.3	-530.0
9	C4P	-3548.0	-530.0
10	C4P	-3471.7	-530.0
11	VCP4	-3395.4	-530.0
12	VCP4	-3319.1	-530.0
13	C3N	-3242.8	-530.0
14	C3N	-3166.5	-530.0
15	C3P	-3090.2	-530.0
16	C3P	-3013.9	-530.0
17	VCP3	-2937.6	-530.0
18	VCP3	-2861.3	-530.0
19	C2N	-2785.0	-530.0
20	C2N	-2708.7	-530.0
21	C2P	-2632.4	-530.0
22	C2P	-2556.1	-530.0
23	VCP2	-2479.8	-530.0
24	VCP2	-2403.5	-530.0
25	C1N	-2327.2	-530.0
26	C1N	-2250.9	-530.0
27	C1P	-2174.6	-530.0
28	C1P	-2098.3	-530.0
29	VCP1	-2022.0	-530.0
30	VCP1	-1945.7	-530.0
31	VCP1	-1869.4	-530.0
32	VCP1	-1793.1	-530.0
33	VCP1	-1716.8	-530.0
34	V0	-1640.5	-530.0
35	V0	-1564.2	-530.0
36	TPA	-1487.9	-530.0
37	SYNCD	-1411.6	-530.0
38	SYNCC	-1335.3	-530.0
39	VSS	-1259.0	-530.0
40	VSSA	-1182.7	-530.0
41	VSSA	-1106.4	-530.0
42	VDDA	-1030.1	-530.0
43	VDDA	-953.8	-530.0
44	NC	-877.5	-530.0
45	VDD	-801.2	-530.0
46	VDD	-724.9	-530.0
47	M/S	-648.6	-530.0
48	SYNCM	-572.3	-530.0
49	BUSY	-496.0	-530.0
50	D7	-419.7	-530.0
51	D6	-343.4	-530.0
52	D5	-267.1	-530.0
53	D4	-190.8	-530.0
54	D3	-114.5	-530.0
55	D2	-38.2	-530.0
56	D1	38.2	-530.0
57	D0	114.5	-530.0
58	CL	190.8	-530.0
59	RES#	267.1	-530.0
60	CS1#	343.4	-530.0
61	VSS	419.7	-530.0
62	R/W#(WR#)	496.0	-530.0
63	E(RD#)	572.3	-530.0
64	CS2	648.6	-530.0
65	VDDIO	724.9	-530.0
66	D/C#	801.2	-530.0
67	VSS	877.5	-530.0
68	CLS	953.8	-530.0
69	VDDIO	1030.1	-530.0
70	PS2	1106.4	-530.0
71	VSS	1182.7	-530.0
72	PS1	1259.0	-530.0
73	VDDIO	1335.3	-530.0
74	PS0	1411.6	-530.0
75	VSS	1487.9	-530.0
76	VDD	1564.2	-530.0
77	VDD	1640.5	-530.0
78	VDDA	1716.8	-530.0
79	VSSA	1793.1	-530.0
80	TR25	1869.4	-530.0
81	TR24	1945.7	-530.0
82	TR23	2022.0	-530.0
83	TR22	2098.3	-530.0
84	TR21	2174.6	-530.0
85	TR20	2250.9	-530.0
86	TR19	2327.2	-530.0
87	TR18	2403.5	-530.0
88	TR17	2479.8	-530.0
89	TR16	2556.1	-530.0
90	TR15	2632.4	-530.0
91	TR14	2708.7	-530.0
92	TR13	2785.0	-530.0
93	TR12	2861.3	-530.0
94	TR11	2937.6	-530.0
95	NC	3013.9	-530.0
96	V1	3090.2	-530.0
97	V1	3166.5	-530.0
98	V2	3242.8	-530.0
99	V2	3319.1	-530.0
100	V3	3395.4	-530.0
101	V3	3471.7	-530.0
102	V4	3548.0	-530.0
103	V4	3624.3	-530.0
104	V0	3700.6	-530.0
105	V0	3776.9	-530.0
106	V0	3853.2	-530.0
107	V0	3929.5	-530.0
108	V0	4005.8	-530.0
109	VFS	4082.1	-530.0
110	NC	4158.4	-530.0
111	TR10	4134.2	-313.5
112	TR9	4134.2	-237.2
113	TR8	4134.2	-160.9
114	TR7	4134.2	-84.6
115	TR6	4134.2	-8.3
116	TR5	4134.2	68.0
117	NC	4063.4	517.4
118	COM31	3995.9	517.4
119	COM30	3955.9	517.4
120	COM29	3915.9	517.4
121	COM28	3875.9	517.4
122	COM27	3835.9	517.4
123	COM26	3795.9	517.4
124	COM25	3755.9	517.4
125	COM24	3715.9	517.4
126	COM23	3675.9	517.4
127	COM22	3635.9	517.4
128	COM21	3595.9	517.4
129	COM20	3555.9	517.4
130	COM19	3515.9	517.4
131	COM18	3475.9	517.4
132	COM17	3435.9	517.4
133	COM16	3395.9	517.4
134	COM15	3355.9	517.4
135	COM14	3315.9	517.4
136	COM13	3275.9	517.4
137	COM12	3235.9	517.4
138	COM11	3195.9	517.4
139	COM10	3155.9	517.4
140	COM9	3115.9	517.4
141	COM8	3075.9	517.4
142	COM7	3035.9	517.4
143	COM6	2995.9	517.4
144	COM5	2955.9	517.4
145	COM4	2915.9	517.4
146	COM3	2875.9	517.4
147	COM2	2835.9	517.4
148	COM1	2795.9	517.4
149	COM0	2755.9	517.4
150	COM_D	2715.9	517.4
151	SEG_D	2629.9	517.4
152	SEG0	2589.9	517.4
153	SEG1	2549.9	517.4
154	SEG2	2509.9	517.4
155	SEG3	2469.9	517.4
156	SEG4	2429.9	517.4
157	SEG5	2389.9	517.4
158	SEG6	2349.9	517.4
159	SEG7	2309.9	517.4
160	SEG8	2269.9	517.4

Pin #	Pin name	X	Y
161	SEG9	2229.9	517.4
162	SEG10	2189.9	517.4
163	SEG11	2149.9	517.4
164	SEG12	2109.9	517.4
165	SEG13	2069.9	517.4
166	SEG14	2029.9	517.4
167	SEG15	1989.9	517.4
168	SEG16	1949.9	517.4
169	SEG17	1909.9	517.4
170	SEG18	1869.9	517.4
171	SEG19	1829.9	517.4
172	SEG20	1789.9	517.4
173	SEG21	1749.9	517.4
174	SEG22	1709.9	517.4
175	SEG23	1669.9	517.4
176	SEG24	1629.9	517.4
177	SEG25	1589.9	517.4
178	SEG26	1549.9	517.4
179	SEG27	1509.9	517.4
180	SEG28	1469.9	517.4
181	SEG29	1429.9	517.4
182	SEG30	1389.9	517.4
183	SEG31	1349.9	517.4
184	SEG32	1309.9	517.4
185	SEG33	1269.9	517.4
186	SEG34	1229.9	517.4
187	SEG35	1189.9	517.4
188	SEG36	1149.9	517.4
189	SEG37	1109.9	517.4
190	SEG38	1069.9	517.4
191	SEG39	1029.9	517.4
192	SEG40	989.9	517.4
193	SEG41	949.9	517.4
194	SEG42	909.9	517.4
195	SEG43	869.9	517.4
196	SEG44	829.9	517.4
197	SEG45	789.9	517.4
198	SEG46	749.9	517.4
199	SEG47	709.9	517.4
200	SEG48	669.9	517.4
201	SEG49	629.9	517.4
202	SEG50	589.9	517.4
203	SEG51	549.9	517.4
204	SEG52	509.9	517.4
205	SEG53	469.9	517.4
206	SEG54	429.9	517.4
207	SEG55	389.9	517.4
208	SEG56	349.9	517.4
209	SEG57	309.9	517.4
210	SEG58	269.9	517.4
211	SEG59	229.9	517.4
212	SEG60	189.9	517.4
213	SEG61	149.9	517.4
214	SEG62	109.9	517.4
215	SEG63	69.9	517.4
216	SEG64	29.9	517.4
217	SEG65	-10.1	517.4
218	SEG66	-50.1	517.4
219	SEG67	-90.1	517.4
220	SEG68	-130.1	517.4
221	SEG69	-170.1	517.4
222	SEG70	-210.1	517.4
223	SEG71	-250.1	517.4
224	SEG72	-290.1	517.4
225	SEG73	-330.1	517.4
226	SEG74	-370.1	517.4
227	SEG75	-410.1	517.4
228	SEG76	-450.1	517.4
229	SEG77	-490.1	517.4
230	SEG78	-530.1	517.4
231	SEG79	-570.1	517.4
232	SEG80	-610.1	517.4
233	SEG81	-650.1	517.4
234	SEG82	-690.1	517.4
235	SEG83	-730.1	517.4
236	SEG84	-770.1	517.4
237	SEG85	-810.1	517.4
238	SEG86	-850.1	517.4
239	SEG87	-890.1	517.4
240	SEG88	-930.1	517.4

Pin #	Pin name	X	Y
241	SEG89	-970.1	517.4
242	SEG90	-1010.1	517.4
243	SEG91	-1050.1	517.4
244	SEG92	-1090.1	517.4
245	SEG93	-1130.1	517.4
246	SEG94	-1170.1	517.4
247	SEG95	-1210.1	517.4
248	SEG96	-1250.1	517.4
249	SEG97	-1290.1	517.4
250	SEG98	-1330.1	517.4
251	SEG99	-1370.1	517.4
252	SEG100	-1410.1	517.4
253	SEG101	-1450.1	517.4
254	SEG102	-1490.1	517.4
255	SEG103	-1530.1	517.4
256	SEG104	-1570.1	517.4
257	SEG105	-1610.1	517.4
258	SEG106	-1650.1	517.4
259	SEG107	-1690.1	517.4
260	SEG108	-1730.1	517.4
261	SEG109	-1770.1	517.4
262	SEG110	-1810.1	517.4
263	SEG111	-1850.1	517.4
264	SEG112	-1890.1	517.4
265	SEG113	-1930.1	517.4
266	SEG114	-1970.1	517.4
267	SEG115	-2010.1	517.4
268	SEG116	-2050.1	517.4
269	SEG117	-2090.1	517.4
270	SEG118	-2130.1	517.4
271	SEG119	-2170.1	517.4
272	SEG120	-2210.1	517.4
273	SEG121	-2250.1	517.4
274	SEG122	-2290.1	517.4
275	SEG123	-2330.1	517.4
276	SEG124	-2370.1	517.4
277	SEG125	-2410.1	517.4
278	SEG126	-2450.1	517.4
279	SEG127	-2490.1	517.4
280	SEG128	-2530.1	517.4
281	SEG129	-2570.1	517.4
282	SEG130	-2610.1	517.4
283	SEG131	-2650.1	517.4
284	SEG_D	-2690.1	517.4
285	COM32	-2737.6	517.4
286	COM33	-2777.6	517.4
287	COM34	-2817.6	517.4
288	COM35	-2857.6	517.4
289	COM36	-2897.6	517.4
290	COM37	-2937.6	517.4
291	COM38	-2977.6	517.4
292	COM39	-3017.6	517.4
293	COM40	-3057.6	517.4
294	COM41	-3097.6	517.4
295	COM42	-3137.6	517.4
296	COM43	-3177.6	517.4
297	COM44	-3217.6	517.4
298	COM45	-3257.6	517.4
299	COM46	-3297.6	517.4
300	COM47	-3337.6	517.4
301	COM48	-3377.6	517.4
302	COM49	-3417.6	517.4
303	COM50	-3457.6	517.4
304	COM51	-3497.6	517.4
305	COM52	-3537.6	517.4
306	COM53	-3577.6	517.4
307	COM54	-3617.6	517.4
308	COM55	-3657.6	517.4
309	COM56	-3697.6	517.4
310	COM57	-3737.6	517.4
311	COM58	-3777.6	517.4
312	COM59	-3817.6	517.4
313	COM60	-3857.6	517.4
314	COM61	-3897.6	517.4
315	COM62	-3937.6	517.4
316	COM63	-3977.6	517.4
317	COM_D	-4017.6	517.4
318	NC	-4070.1	517.4
319	TR4	-4156.0	64.2
320	TR3	-4156.0	-12.2
321	TR2	-4156.0	-88.5
322	TR1	-4156.0	-164.8
323	TR0	-4156.0	-241.1

6 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull LOW =connect to V_{SS}, Pull HIGH = connect to V_{DDIO}

Table 6-1 : Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	This pin is the system power supply pin of the logic block.
V_{DDA}	P	This pin is the system power supply pin of the analog block. It must be connected to V_{DD}.
V_{DDIO}	P	Power supply for interface logic level. It should be match with the MCU interface voltage level. It must always be equal or lower than V_{DD}
V_{CI}	P	Power supply for Charge Pump and analog part of the chip. It should be connected to V_{DD}.
V_{SS}	P	This is a ground pin
V_{SSA}	P	The V_{SSA} is the ground reference of the system connected to V_{SS}.
V_{SSC}	P	The V_{SSC} is the ground reference of the analog system. It should be connected to V_{SS}.
V_0	P	It is the high voltage power input pin and panel driving voltage. It should be connected to VCP1
V_1	C	Panel driving voltage. If bias divider is enabled with the presence of V_0. The voltage is equal to (N-1)/N * V_0, where N is equal to the Bias ratio Setting
V_2	C	Panel driving voltage. If bias divider is enabled with the presence of V_0. The voltage is equal to (N-2)/N * V_0, where N is equal to the Bias ratio Setting
V_3	C	Panel driving voltage. If bias divider is enabled with the presence of V_0. The voltage is equal to 2/N * V_0, where N is equal to the Bias ratio Setting
V_4	C	Panel driving voltage. If bias divider is enabled with the presence of V_0. The voltage is equal to 1/N * V_0, where N is equal to the Bias ratio Setting
CL	IO	This pin is the display clock input/output.
CLS	I	This pin is the internal clock enable pin. When this pin is pulled high to V_{DDIO}, internal clock is enabled. The internal clock will be disabled when it is pulled low to V_{SS}, an external clock source must be input to CL pin for normal operation.
CS1#, CS2	I	These pins are the chip select inputs for communication between MCU. To select the chip CS1# must be low and CS2 must set high
RES#	I	This pin is the reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for reset sequence is 20us.
D/C#	I	This pin is Data/Command control pin. A high at D/C indicates data input while a low at D/C indicates command input. In I^2C mode, this pin acts as SA0 for slave address selection.

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>R/W# (WR#)</td><td>I</td><td>This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode when low. When 8080 interface mode is selected, this pin is the Write (WR#) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected.

When serial interface mode is selected, this pin must be pulled low.</td></tr>
<tr><td>E (RD#)</td><td>I</td><td>This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected. When 8080 interface mode is selected, this pin is the Read (RD#) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected.

When serial interface mode is selected, this pin must be pulled high.</td></tr>
<tr><td>D0 ~ D7</td><td>I/O</td><td>These pins are the 8-bit bi-directional data bus.

In parallel interface mode, D7 is the MSB whlile D0 is the LSB.
In serial interface mode, D1 is the serial data input (SD_{IN}), D_0 is the serial clock input, (SCLK).
In I^2C mode is selected, D2 is SDA_{OUT}, D1 is SDA_{IN}. Tie D2 and D1 together will serve as SDA, D0 is the I2C clock input (SCL).</td></tr>
<tr><td>PS0 ~ PS2</td><td>I</td><td>These pins are for selecting different bus interface.

Table 6-2 : Bus Interface selection
<table><tr><td>PS2</td><td>PS1</td><td>PS0</td><td>MPU Interface</td></tr><tr><td>L</td><td>L</td><td>L</td><td>4-lines serial peripheral interface (SPI)</td></tr><tr><td>L</td><td>L</td><td>H</td><td>8-bit 8080 parallel interface</td></tr><tr><td>L</td><td>H</td><td>L</td><td>3-lines serial peripheral interface (SPI) – 9 bits SPI</td></tr><tr><td>L</td><td>H</td><td>H</td><td>8-bit 6800 parallel interface</td></tr><tr><td>H</td><td>L</td><td>L</td><td>I2C</td></tr></table>
Note
(1) L is connected to V_{SS}
(2) H is connected to V_{DDIO}</td></tr>
<tr><td>COM0 ~ COM63</td><td>O</td><td>These pins provide the Common driving signals to the Bistable panel.</td></tr>
<tr><td>SEG0 ~ SEG131</td><td>O</td><td>These pins provide the Segment driving signals to the Bistable panel.</td></tr>
<tr><td>SEG_D</td><td>O</td><td>These pins provide the Segment driving signals for the border to the Bistable panel.</td></tr>
<tr><td>COM_D</td><td>O</td><td>These pins provide the Common driving signals for the border to the Bistable panel.</td></tr>
</table>

Pin Name	Pin Type	Description
C1N, C1P	C	Charge Pump flying capacitor terminal. Connect a capacitor between C1N and C1P.
C2N, C2P	C	Charge Pump flying capacitor terminal. Connect a capacitor between C2N and C2P.
C3N, C3P	C	Charge Pump flying capacitor terminal. Connect a capacitor between C3N and C3P.
C4N, C4P	C	Charge Pump flying capacitor terminal. Connect a capacitor between C4N and C4P.
VCP1	P	Charge Pump output voltage. Connect with a capacitor to $V_{SSC.}$ It should be connected to V_0.
VCP2	P	Charge Pump intermediate output voltage. Connect with a capacitor to V_{SSC} If using external mode with BIAS VOLTAGE buffer enabled, it should be connected to V_0.
VCP3	C	Charge Pump intermediate output voltage. Connect with a capacitor to V_{SSC}
VCP4	C	Charge Pump intermediate output voltage. Connect with a capacitor to V_{SSC}.
BUSY	O	A high level indicates busy status (output driving waveform) of the driver.
M/S	I	Test pin. Tied High for normal operations
SYNCC, SYNCD, SYNCM	NC	Test pins. Keep NC.
TPA	NC	Test pin. Keep NC.
VFS	NC	Test pin. Keep NC.
TR0 – TR25	NC	Test reserved pins. Keep NC.
NC	NC	These pins have no connections. However, nothing should be connected to these pins, nor they are connected together.

7 FUNCTIONAL BLOCK DESCRIPTIONS

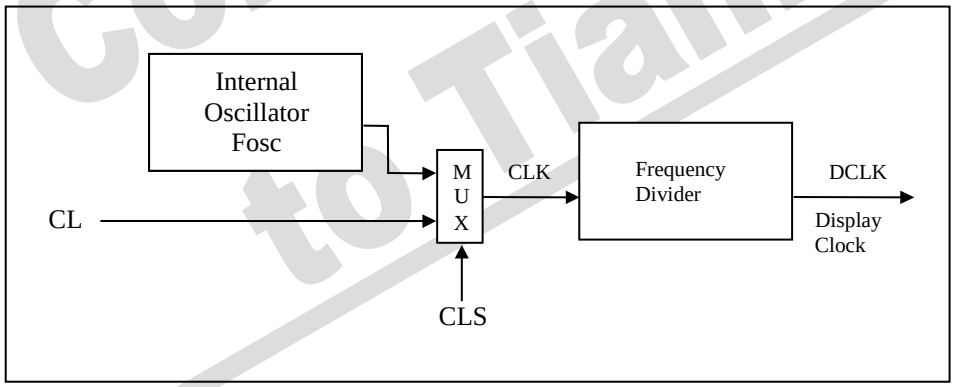
7.1 Reset Circuit

When RES# input is LOW, the chip is initialized to the following status:

Driving Update:	Update halt
Normal/Inverse Display:	Normal Display
Com Scan Direction:	COM0 -> COM63
Internal Oscillator:	Disable
Internal Charge Pump:	Disable
Bias Divider:	Disable
Bias ratio:	1/7
Multiplex ratio:	64
Display data column address mapping:	Normal
Display start line:	GDDRAM row 0
Column address counter:	00 hex
Page address:	00 hex
Shift register data in serial interface:	Clear

7.2 Oscillator Circuit and Display Time Generator

Figure 7-1 : Oscillator Circuit and Display Time Generator



This module is an on-chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin low disables internal oscillator and external clock must be connected to CL pins for proper operation.

7.3 Command Decoder and MPU Interface

This module determines if the input data will be interpreted as data, or a command. When the D/C# is set HIGH the inputs at D_7-D_0 are interpreted as data and will be written to Graphic Display Data RAM (GDDRAM). When it is set LOW the inputs at D_7-D_0 are interpreted as a command and will be decoded and written to the corresponding command registers.

7.4 MPU Interface Selection

MCU interface consist of 8 data pins and 6 control pins. The pin assignment at different interface mode is summarized in Table 7-1. Different MCU mode can be set by hardware selection on PS [2:0] pins (please refer to Table 6-2 : Bus Interface selection for PS [2:0] setting).

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name	Data/Command Interface								Control Signal					
Bus Interface	D7	D6	D5	D4	D3	D2	D1	D0	E (RD#)	R/W# (WR#)	CS1#	CS2	D/C#	RES#
SPI4	Tie LOW					NC	SDin	SCLK	H	L	CS#	H	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS1#	CS2	D/C#	RES#
SPI3	Tie LOW					NC	SDin	SCLK	H	L	CS#	H	L	RES#
8-bit 6800	D[7:0]								E	R/W#	CS1#	CS2	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	H	L	L	H	SA0	RES#

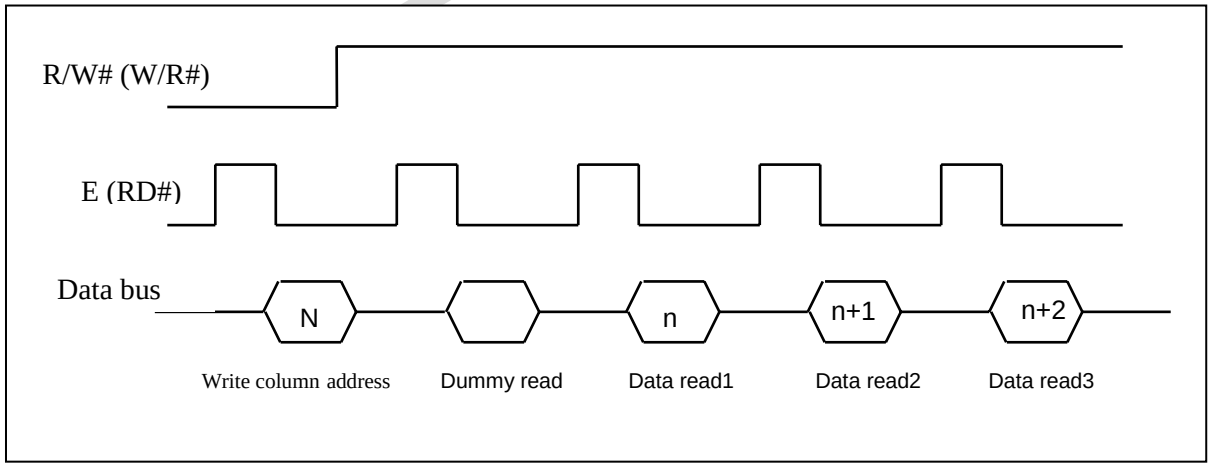
7.5 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins: (D_7-D_0), R/W# (WR#), E (RD#), D/C#, CS1# and CS2.

When the R/W# (WR#) pin is pulled HIGH Read operation from the Graphic Display Data RAM (GDDRAM), or the status register, occurs.
When the R/W# (WR#) pin is pulled LOW Write operation to the Display Data RAM, or Internal Command Registers, occurs, depending on the status of the D/C# input.

The E (RD#) input serves as the data latch signal (clock) when on HIGH, provided the CS1# is pulled LOW and CS2 is pulled high. Please refer to the Parallel Interface Timing Diagram of the 6800-series microprocessors.
In order to match the operating frequency of the display RAM with that of the microprocessor, pipeline processing is performed internally, which requires the insertion of a dummy read before the first actual display data read. See Figure 7-2 below.

Figure 7-2 : Display data read back procedure - insertion of dummy read



7.6 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W# (WR#), E (RD#), D/C#, CS1# and CS2. The E (RD#) input serves as the data read latch signal (clock) when on LOW, provided the CS1# is also pulled LOW and CS2 is pulled HIGH. Display data, or status register read, is controlled by the D/C# signal.
R/W# (WR#) input serves as the data write latch signal (clock) when on HIGH, provided the chip selected. Display data, or command register write, is controlled by the D/C#. Please refer to Parallel Interface Timing Diagram of the 8080-series microprocessors. Similar to the 6800-series interface, a dummy read is also required before the first, actual display data read.

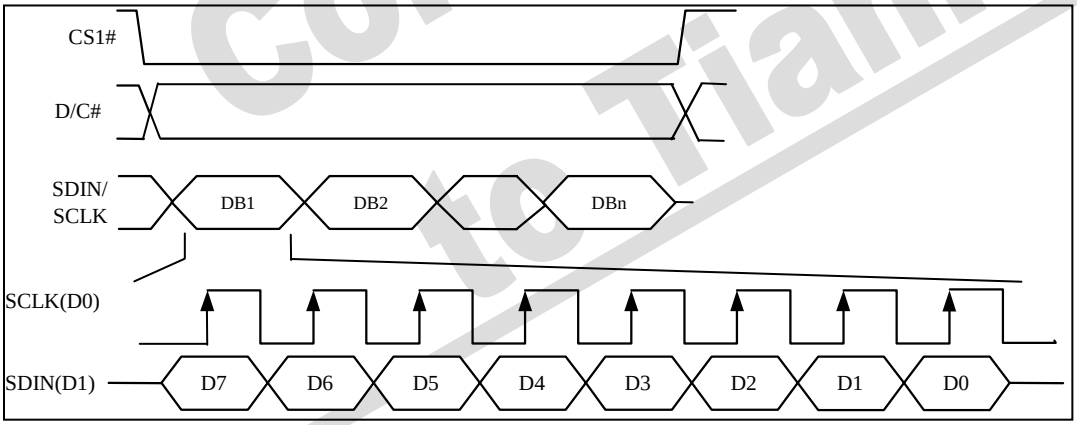
7.7 MPU Serial Interface (4 wire)

The serial interface consists of the serial clock SCLK and serial data SDIN, D/C#, CS1#.

In SPI mode, D0 acts as SCLK and D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W can be connected to an external ground and E; CS2 should be connected to VDDIO.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM, or command register, in the same clock. See Figure 7-3 below.

Figure 7-3 : Display data write procedure in SPI4 mode



7.8 MPU Serial Interface (3 wire)

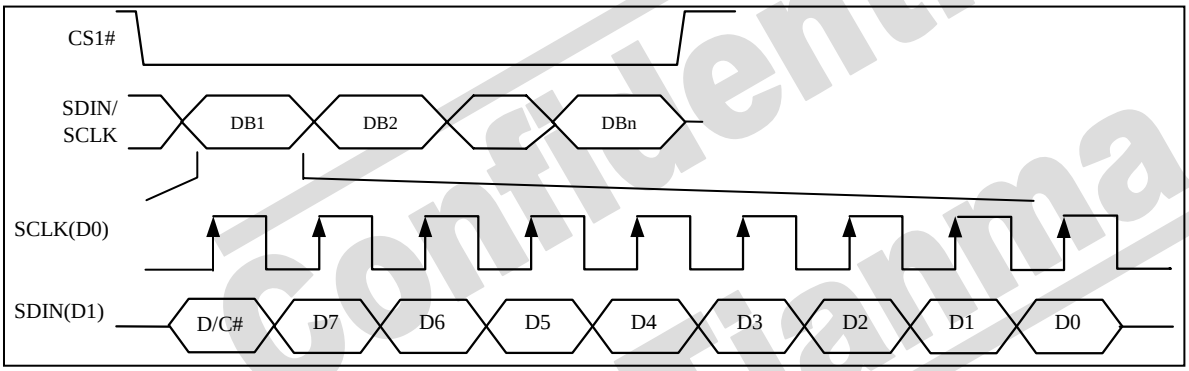
The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS1#.

In 3-wire SPI mode, D1 acts as SCLK, D0 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W can be connected to an external ground and E; CS2 should be connected to VDDIO.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Under serial mode, only write operations are allowed.

Figure 7-4 : Command write procedure in SPI3 mode



7.9 MPU I²C Interface

In I^2C mode, for the unused data pins, the pins from D3 to D7, R/W and CS1# should be connected to an external ground; E and CS2 should be connected to VDDIO.

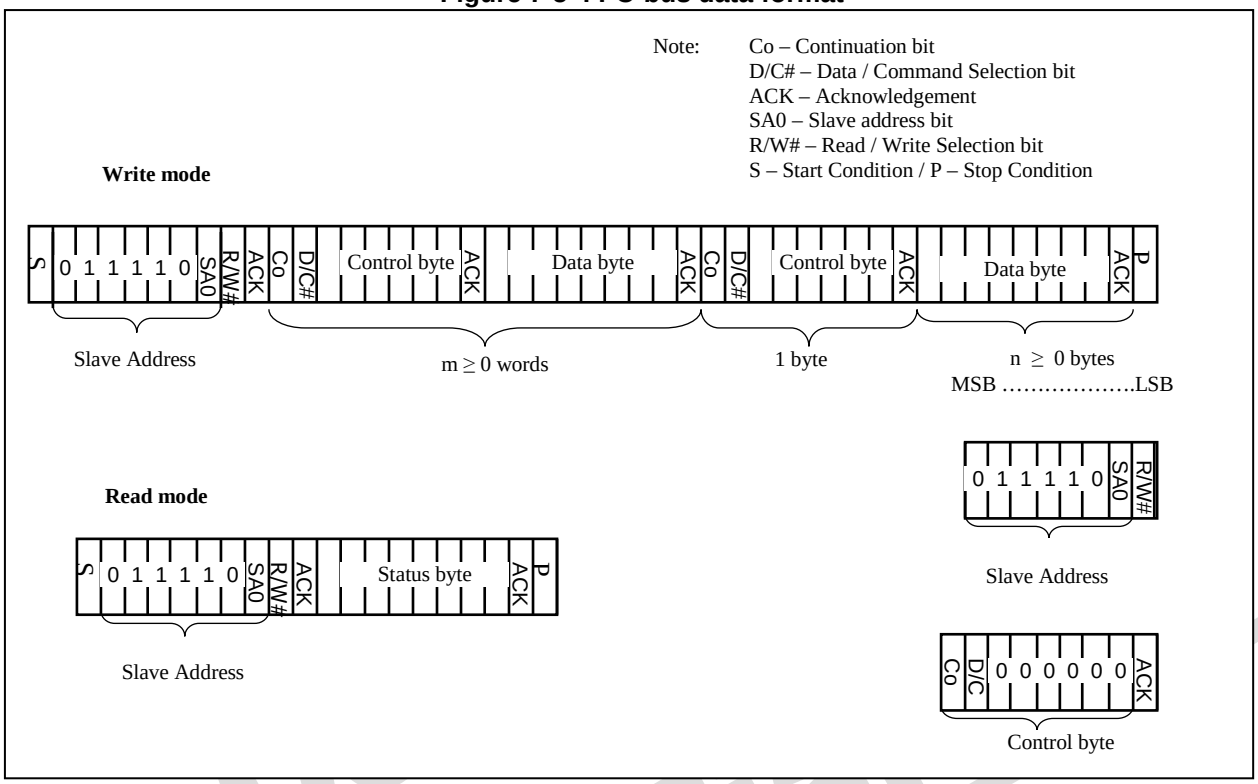
The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

1. Slave address bit (SA0)
    - The Chip has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
    - b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
    - 0 1 1 1 1 0 SA0 R/W#
    - "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101" can be selected as the slave address of the chip.
    - D/C# pin acts as SA0 for slave address selection.
    - "R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.
2. I^2C-bus data signal (SDA)
    - SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
    - "SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.
3. I^2C-bus clock signal (SCL)
    - The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.9.1 I²C-bus Write Data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 7-5 for the write mode of I²C-bus in chronological order.

Figure 7-5 : I²C-bus data format



7.9.2 Write Mode for I²C

The master device initiates the data communication by a start condition.

The definition of the start condition is shown in Figure 7-6.The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.

The slave address is following the start condition for recognition use. The slave address is either "b011 1100" or "b011 1101" by changing the SA0 to LOW or HIGH (D/C# pin acts as SA0). The write mode is established by setting the R/W# bit to logic "0".

An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-7 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.

After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0"'s.

If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only. No control byte is applied until the stop condition.

The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

Acknowledge bit will be generated after receiving each control byte or data byte.
The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-6. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 7-6 : Definition of the Start and Stop Condition

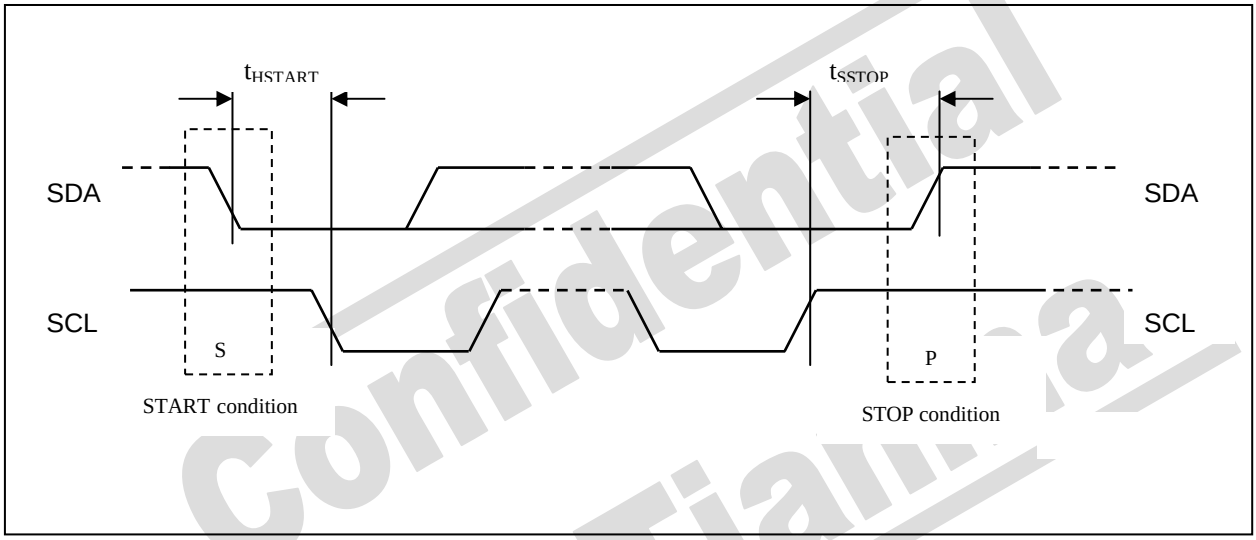
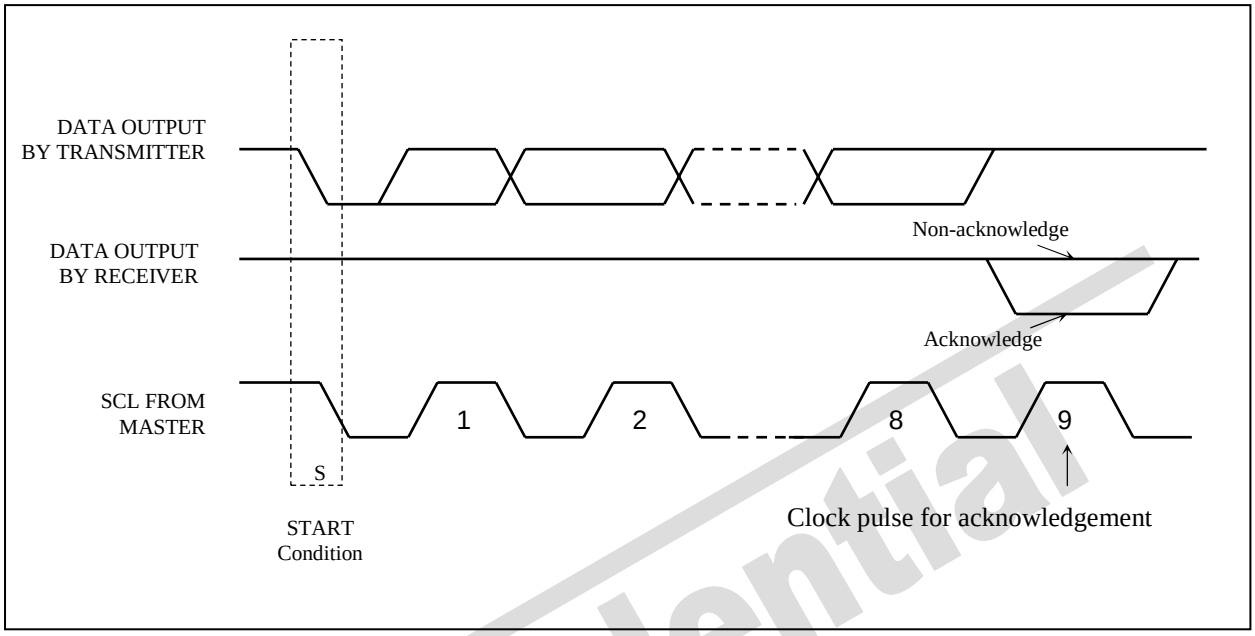
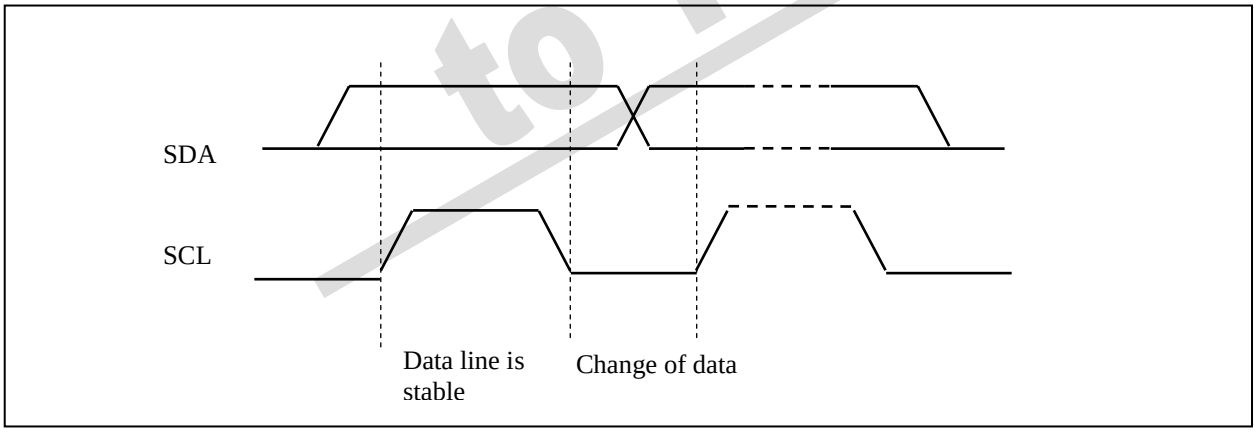


Figure 7-7 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.
The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-8 for graphical representations.
Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

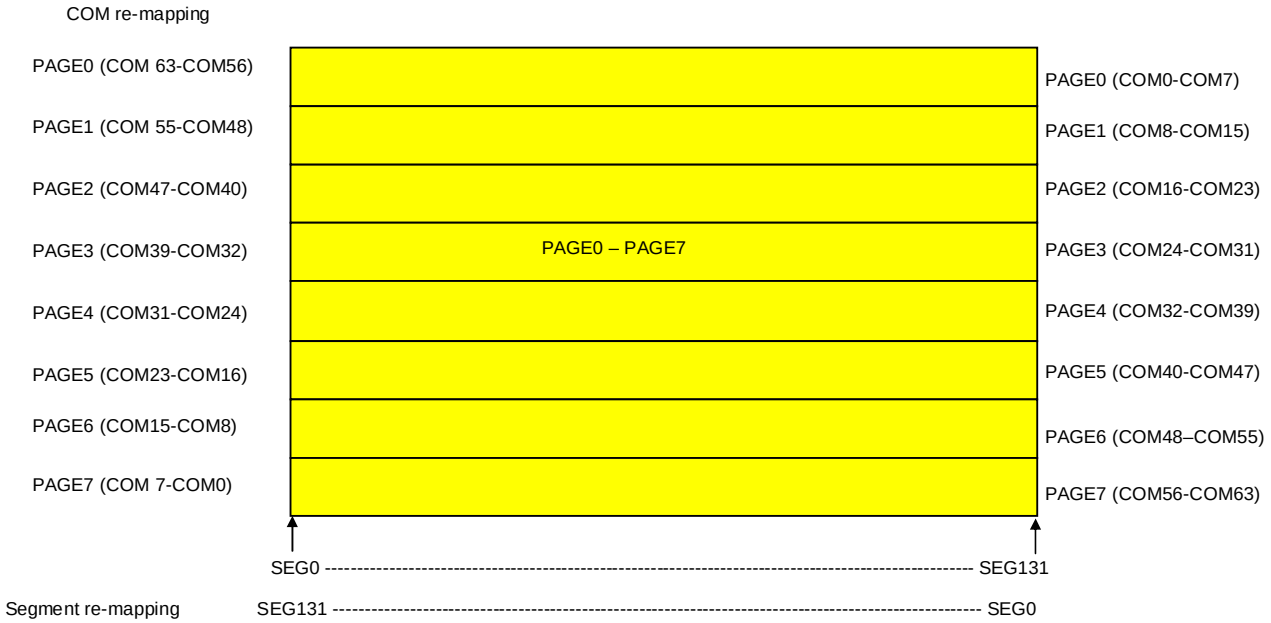
Figure 7-8 : Definition of the data transfer condition



7.10 Graphic Display Data RAM (GDDRAM)

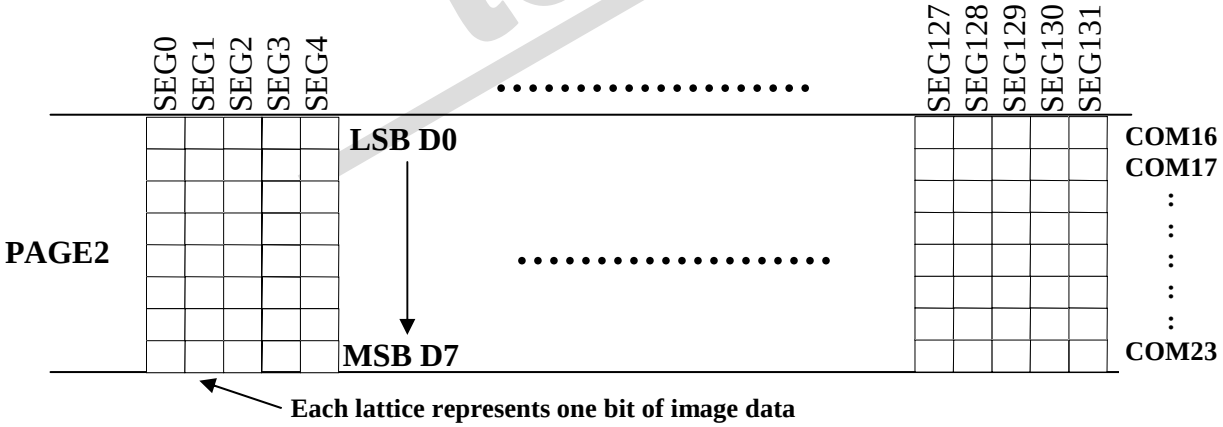
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, as shown in Figure 7-9.

Figure 7-9 : GDDRAM pages structure



When one data byte is written into GDDRAM, all the COMs image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top COM; while data bit D7 is written into bottom COM as shown in Figure 7-10.

Figure 7-10 : Enlargement of GDDRAM (No COM re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 7-9.

For vertical shifting of the display, an internal register storing the display offset can be set to control the portion of the RAM data to be mapped to the display (command D3h).

7.11 Bias Voltage Generator

This module generates the high voltage required for display driving output. It takes a single supply input and generates necessary bias voltage. It consists of:

1. High multiplier charge pump with contrast control
2. Bias Divider
3. Bias Voltage Buffer
4. Bias Ratio Selection Circuitry

The built-in regulated charge pump is used to generate the high positive voltage supply. It can produce 8X/16X boosting from the potential difference between V_{CI} - V_{SS}.

The output from the charge pump can be controlled by the contrast control command.

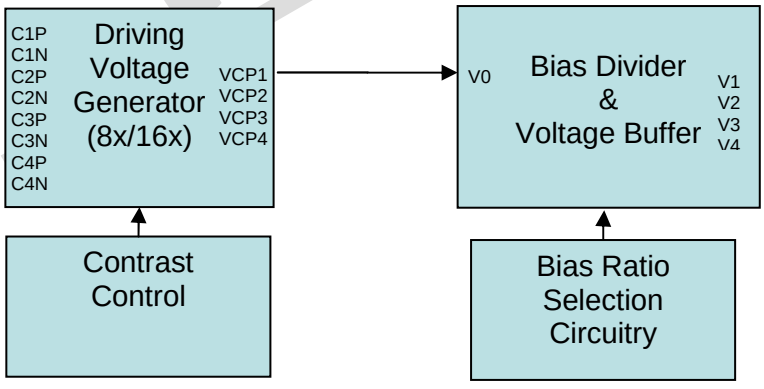
The contrast voltage level can be set with step size 0.25V. Refer to Table 7-5 : Voltage Setting Table (For Clearing and Driving Voltage Setting) for the setting details

If the buffer option in Set Power Control Register command is enabled, this circuit block will divide the High voltage V_0 to give the panel driving levels. The divider does not require external components to reduce the external hardware and pin counts.

The Bias Ratio Selection circuitry controls the buffers output. 1/4 to 1/9 bias ratio is selectable in order to match the characteristic of panel.

Bias Voltage Buffer Pin	Output level
V1	[1- 1/N] * V_0
V2	[1- 2/N] * V_0
V3	2/N * V_0
V4	1/N * V_0

Figure 7-11 : Block Diagram of the relationship between Bias Voltage Generator, Contrast Control Regulator, Bias Ration Selection Circuitry and Bias Divider & Buffer



7.12 Segment Drivers / Common Drivers

The Segment/Common Driver Circuits works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector that is synchronized with the internal M signal.

7.13 Driving Scheme setting

Data in clearing phase can be set to 0 or 1.

The polarity or M can be set 0 or 1 for clearing phase and driving phase separately

7.14 Driving waveform

On Clearing, all Segment and Common have the same output waveform according to the setting in command 0x32.
(Remark: M in the following diagram is the polarity setting according to the Command Setting 0x32, which is an internal signal.)

The below table shows the waveform on the clearing duration, (M starts with 1 for the illustration)

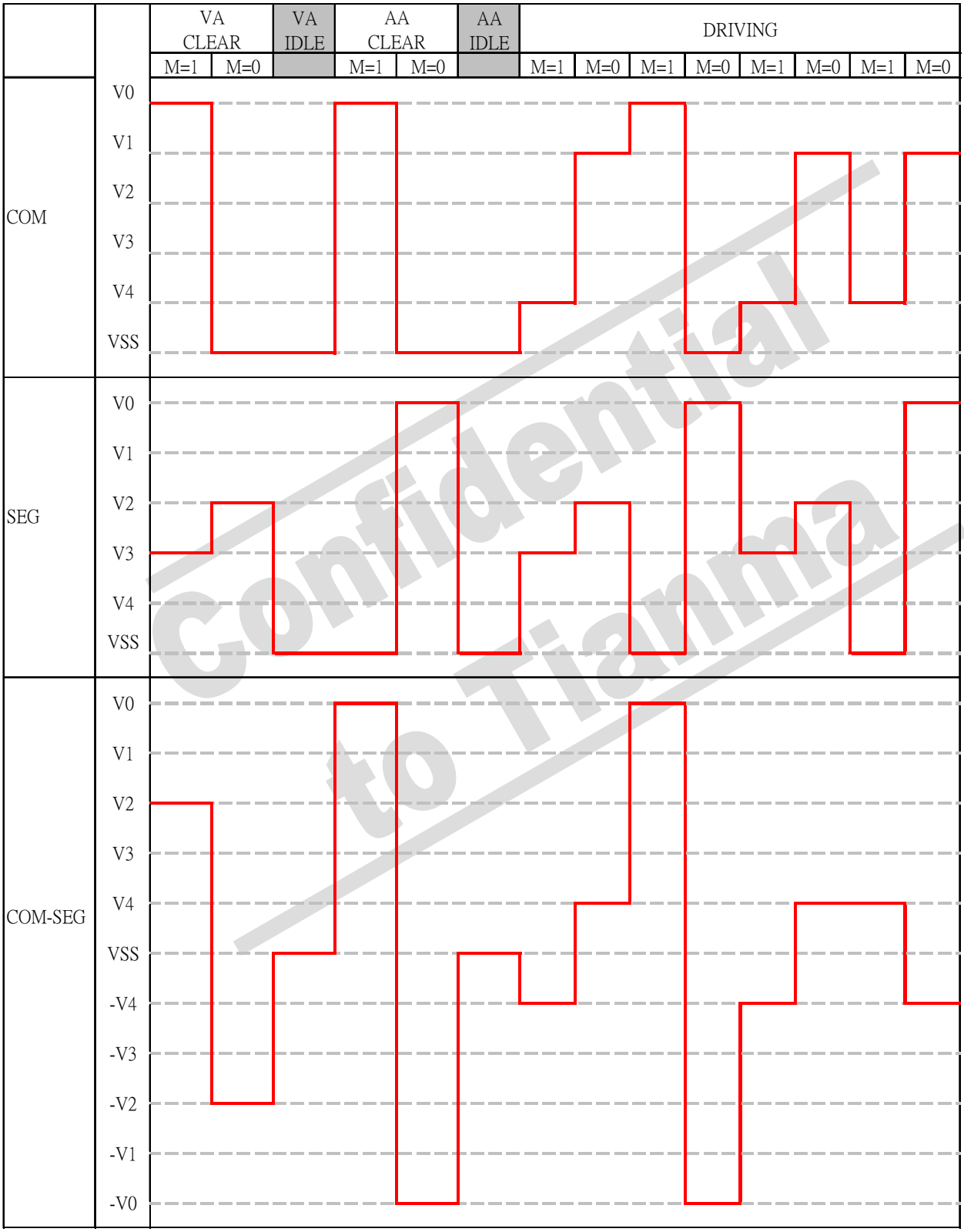
Table 7-2 : Waveform on Clearing Phase

Setting		COM	
		M=1	M=0
Non-Select	V0		
	V1		
	V2		
	V3		
	V4		
	VSS		
Select	V0		
	V1		
	V2		
	V3		
	V4		
	VSS		

Data		SEG	
		M=1	M=0
0	V0		
	V1		
	V2		
	V3		
	V4		
	VSS		
1	V0		
	V1		
	V2		
	V3		
	V4		
	VSS		

For a complete illustration,

Table 7-3 : The typical waveform of SEG/COM



7.15 Contrast setting control

User can define the timing for clear, idle, driving phases and voltages individually.
8 bytes are entered for Clear Duration, Idle Duration, Drive Duration, Clear Voltage, and Drive Voltage.

For Contrast settings, there are 7 bits to set the waveform duration, and the remaining MSB 1 bits are Don't care bits.
For all timing settings, there are 5 bits to set the waveform duration, and the remaining MSB 3 bits are Don't care bits.
For clearing and driving voltage, the value is in step of 0.5V from 14V to 35V on the Vcp1.

Table 7-4 : Clearing, idle & driving phase programmable time duration

$X_4X_3X_2X_1X_0$	Time for 1 pixel /ms
00000	0.08
00001	0.2
00010	0.4
00011	0.8
00100	1
00101	2
00110	4
00111	6
01000	8
01001	10
01010	12
01011	14
01100	18
01101	20
01110	25
01111	30

$X_4X_3X_2X_1X_0$	Time for 1 pixel /ms
10000	35
10001	40
10010	50
10011	60
10100	80
10101	100
10110	150
10111	200
11000	250
11001	350
11010	500
11011	750
11100	1,000
11101	2,000
11110	4,000
11111	10,000

Table 7-5 : Voltage Setting Table (For Clearing and Driving Voltage Setting)

$X_6X_5X_4X_3X_2X_1$	Vcp1[V]
001100	14.0
001101	14.5
001110	15.0
001111	15.5
010000	16.0
010001	16.5
010010	17.0
010011	17.5
010100	18.0
010101	18.5
010110	19.0
010111	19.5
011000	20.0
011001	20.5
011010	21.0
011011	21.5
011100	22.0
011101	22.5
011110	23.0
011111	23.5
100000	24.0
Remark: X0 = 0	for all setting.

$X_6X_5X_4X_3X_2X_1$	Vcp1[V]
100001	24.5
100010	25.0
100011	25.5
100100	26.0
100101	26.5
100110	27.0
100111	27.5
101000	28.0
101001	28.5
101010	29.0
101011	29.5
101100	30.0
101101	30.5
101110	31.0
101111	31.5
110000	32.0
110001	32.5
110010	33.0
110011	33.5
110100	34.0
110101	34.5
110110	35.0

7.16 Charge Pump Application Circuit

Figure 7-12: Charge Pump application diagram

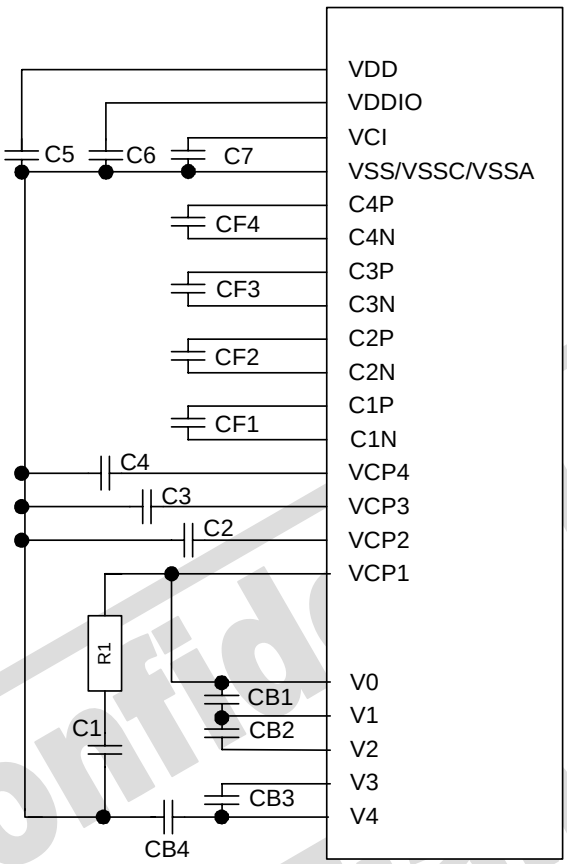


Table 7-6: Reference Capacitor Value

Part reference	**Value (uF)**	**Min Rating**
CF1	1.0	50V
CF2	1.0	25V
CF3	1.0	25V
CF4	1.0	10V
C1	4.7	50V
C2	0.1	25V
C3	0.1	10V
C4	0.1	10V
C5	1.0	10V
C6	1.0	10V
C7	1.0	10V
CB1	1.0	10V
CB2	1.0	10V
CB3	1.0	10V
CB4	1.0	10V
Part reference	**Value (Ohm)**	**Remark**
R1	0	For Typical case

Capacitor values requirement depends on panel loading and voltage setting.

8 COMMAND TABLE

Table 8-1: Command Table

(D/C# = 0, R/W#(WR#) = 0, E=1(RD# = 1) unless specific setting is stated)

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0	10 – 1F	0	0	0	1	A_3	A_2	A_1	A_0	Set column address	Set the higher nibble of the column address register using $A_3A_2A_1A_0$ as data bits. The higher nibble of column address is reset to 0000b after POR. [POR=10_{HEX}] Set the lower nibble of the column address register using $B_3B_2B_1B_0$ as data bits. The lower nibble of column address is reset to 0000b after POR. [POR=00_{HEX}]
0		0	0	0	0	B_3	B_2	B_1	B_0		
0	2A – 2F	0	0	1	0	1	X_2	1	X_0	Set Power Control Register	X_2=0: turns off Charge Pump X_2=1: turns on Charge Pump X_0= 0: turns off Bias Voltage buffer X_0=1: turns on Bias Voltage buffer [POR=$2A_{HEX}$]
0	31	0	0	1	1	0	0	0	1	Driving update	Update RAM content to the screen through segment and common pins. Driving sequence is always in: VA clearing phase →Idle 1 phase → AA clearing phase → Idle 2 phase → Driving phase
0	32	0	0	1	1	0	0	1	0	Driving Scheme	Driving Scheme Setting Active Area Control after clearing X_6X_5 =01, Active Area is responsible to data 1 X_6X_5 =11, Active Area is responsible to data 0 Border Control after clearing X_4 =X_1 =0, Border is responsible to data 0 X_4 =X_1 =1, Border is responsible to data 1 X_3: driving polarity 0: M starts as 1 at Driving phase 1: M starts as 0 at Driving phase X_2: clearing polarity 0: M starts as 1 at Clearing phase 1: M starts as 0 at Clearing phase [POR=00_{HEX}]
0		0	X_6	X_5	X_4	X_3	X_2	X_1	0		
0	40 – 7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Display start line register is reset to 000000 after POR for all MUX modes. [POR=40_{HEX}]
0	80	1	0	0	0	0	0	0	0	Set the control scheme	Set the control scheme. B[4:0] : VA Clearing Duration C[4:0] : Idle 1 Duration D[4:0] : AA Clearing Duration E[4:0] : Idle 2 Duration F[4:0] : Driving Duration G[6:1] : Clearing Voltage H[6:1] : Driving Voltage
0	00	0	0	0	0	0	0	0	0		
0	B[4:0]	0	0	0	B_4	B_3	B_2	B_1	B_0		
0	C[4:0]	0	0	0	C_4	C_3	C_2	C_1	C_0		
0	D[4:0]	0	0	0	D_4	D_3	D_2	D_1	D_0		
0	E[4:0]	0	0	0	E_4	E_3	E_2	E_1	E_0		
0	F[4:0]	0	0	0	F_4	F_3	F_2	F_1	F_0		
0	G[6:1]	0	G_6	G_5	G_4	G_3	G_2	G_1	0		
0	H[6:1]	0	H_6	H_5	H_4	H_3	H_2	H_1	0		
0	93	1	0	0	1	0	0	1	1	Set view area phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If VA clearing phase repeat time is set to 0, it is also needed to set the idle 1 phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	94	1	0	0	1	0	1	0	0	Set idle 1 phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If Idle 1 phase repeat time is set to 0, it is also needed to set the VA clearing phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	95	1	0	0	1	0	1	0	1	Set active area clearing phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If AA clearing phase repeat time is set to 0, it is also needed to set the idle2 phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	96	1	0	0	1	0	1	1	0	Set idle 2 phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If Idle 2 phase repeat time is set to 0, it is also needed to set the AA clearing phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	97	1	0	0	1	0	1	1	1	Set drive phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0	A0 – A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X_0=0: Column address 00h is mapped to SEG0 X_0=1: Column address 83h is mapped to SEG0 [POR=$A0_{HEX}$]
0 0	A2	1 0	0 0	1 0	0 0	0 0	0 X_2	1 X_1	0 X_0	Set LCD Bias	$X_2X_1X_0$=000: 1/9 $X_2X_1X_0$=001: 1/8, $X_2X_1X_0$=010: 1/7, $X_2X_1X_0$=011: 1/6, $X_2X_1X_0$=100: 1/5, $X_2X_1X_0$=111: 1/4 [POR=00_{HEX}]
0 0	A3	1 0	0 0	1 0	0 X_4	0 X_3	0 0	1 X_1	1 0	Set analog control	X_4X_3 = 00: Disable X_4X_3 = 11: Enable X_1 = 0: Standard BIAS VOLTAGE Buffer Setting X_1 = 1: Extra BIAS VOLTAGE Buffer Setting [POR=00_{HEX}]
0	A4 – A5	1	0	1	0	0	1	0	X_0	Set Entire Display On/Off	X_0=0: normal display X_0=1: entire display on [POR=$A4_{HEX}$]
0	A6 – A7	1	0	1	0	0	1	1	X_0	Set Normal/Reverse Display	X_0=0: normal display X_0=1: reverse display [POR=$A6_{HEX}$]
0 0	A8	1 0	0 X_6	1 X_5	0 X_4	1 X_3	0 X_2	0 X_1	0 X_0	Set Multiplex Ratio	To select multiplex ratio N MUX $X_6X_5X_4X_3X_2X_1X_0$ = N from 2 to 64 [POR=40_{HEX}]
0 0	A9	1 0	0 0	1 0	0 0	1 0	0 0	0 0	1 X_0	Analog Control Auto ON/OFF	X_0= 0: OFF X_0= 1: ON [POR=00_{HEX}]
0 0	AD	1 0	0 0	1 0	0 0	1 0	1 0	0 0	1 X_0	RAM Read/Write Direction	X_0= 0: RAM read/write horizontal X_0= 1: RAM read/write vertical [POR=00_{HEX}]
0 0	AE	1 0	0 X_6	1 X_5	0 X_4	1 X_3	1 X_2	1 X_1	0 X_0	Set Auto Charge pump Threshold Value	$X_6X_5X_4X_3X_2X_1X_0$: Auto Charge Pump Threshold If contrast setting > threshold, 16X Charge Pump setting would be selected, Otherwise, 8X Charge Pump is used. [POR=20_{HEX}]
0	B0 – B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Address	Set GDDRAM Page Address (0-7) for read/write using $X_2X_1X_0$ [POR=$B0_{HEX}$]
0	C0 / C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	X_3=0: normal mode X_3=1: remapped mode COM0 to COM [N-1] becomes COM [N-1] to COM0 when Multiplex ratio is equal to N. [POR=$C0_{HEX}$]
0 0	D3	1 0	1 0	0 X_5	1 X_4	0 X_3	0 X_2	1 X_1	1 X_0	Set Display Offset	After setting MUX ratio less than default value, data will be displayed at the beginning/towards the end of display matrix. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = Y – L Note: max value of L = Y – display MUX Y represents POR default MUX [POR=00_{HEX}]
0 0	E2	1 1	1 1	1 1	0 0	0 0	0 0	1 1	0 1	Software Reset	Initialize internal status registers.
0	E3	1	1	1	0	0	0	1	1	NOP	No operation
0 0	E9	1 X_7	1 0	1 0	0 0	1 0	0 1	0 0	1 0	Set Bias Resistor Ladder	X_7= 0: Disable X_7= 1: Enable [POR=04_{HEX}]
0 0	F6	1 0	1 X_6	1 0	1 0	0 0	1 0	1 0	0 0	Set Internal Oscillator	X_6= 0: Disable X_6= 1: Enable [POR=00_{HEX}]
0 0	FD	1 0	1 0	1 0	1 1	1 0	1 X_2	0 1	1 0	Lock/unlock driver	X_2= 0: unlock driver X_2= 1: lock driver Or unlock driver when hardware reset (No command or data will be written to driver when the lock is high) [POR=12_{HEX}]

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0 0	FE	1 X_7	1 0	1 0	1 0	1 0	1 0	1 0	0 0	Set Clock Enable	X_7= 0: Disable X_7= 1: Enable [POR=00_{HEX}]

Table 8-2 : Read Command Table

(D/C# = 0, R/W#(WR#) = 1, E=1(RD# = 0) unless specific setting is stated)

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0	00 - FF	X_7	X_6	X_5	0	X_3	X_2	X_1	X_0	Status Register Read	X_7=0: indicates the driver is ready for command. X_7=1: indicates the driver is Busy. X_6=0: indicates normal segment mapping with column address. X_6=1: indicates reverse segment mapping with column address. X_5=0: indicates the display is ON. X_5=1: indicates the display is OFF. $X_3X_2X_1X_0$ = 0010, the 4-bit is fixed to 0010 which could be used to identify as Solomon Systech Device.

8.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.

Also, a dummy read is required before the first data read. See Figure 7-2 in the Functional Block Description.

To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 8-3 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

9 COMMAND DESCRIPTIONS

9.1 Set Column Start Address for Page Addressing Mode (10h~1Fh)

This command specifies the nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Section 9.15 for setting details.

9.2 Set Power Control Register (2A ~ 2Fh)

This command enables the BIAS VOLTAGE Buffer and the Charge Pump.

Command in Hex	Description
2A	Disable BIAS VOLTAGE buffer and Charge Pump
2B	Enable BIAS VOLTAGE buffer and Disable Charge Pump
2E	Disable BIAS VOLTAGE buffer and Enable Charge Pump
2F	Enable BIAS VOLTAGE buffer and Charge Pump

9.3 Driving Update (31h)

This command enables driving update. After the command set:

1. Latch the setting from Control Scheme for the clearing, driving phase length and voltage.
2. Output Driving waveform according to the repeating setting from 91h to 97h. The driving sequence is:
   a. View Area Clearing
   b. Idle1
   c. Active Area Clearing
   d. Idle2
   e. Driving

9.4 Driving Scheme Setting (32h)

This command provides different display on the Bistable display. Please refer to Table 8-1: Command Table for the setting reference.

a. Driving Polarity (X_3)

It is used to control the starting polarity of the Driving Phase.

b. Clearing Polarity (X_2)

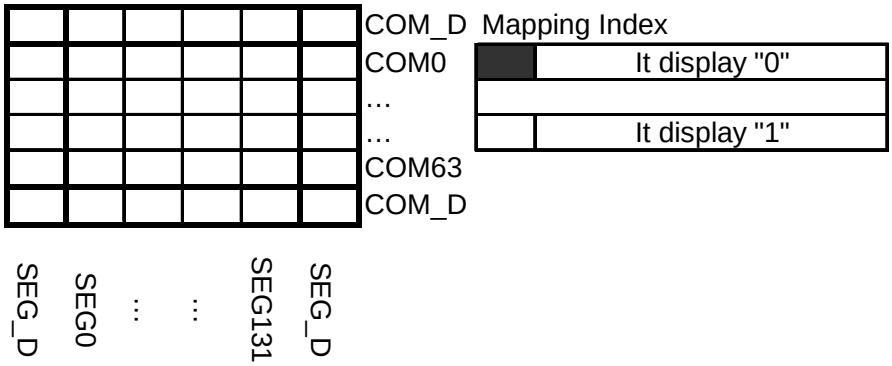
It is used to control the starting polarity of the Clearing Phase.

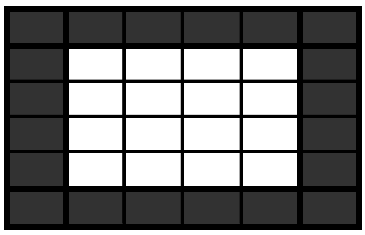
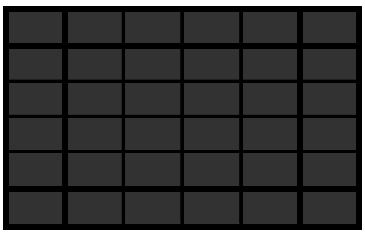
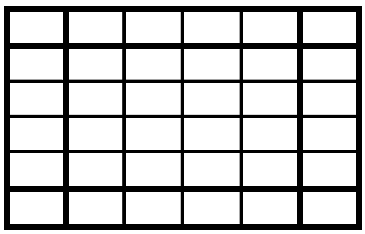
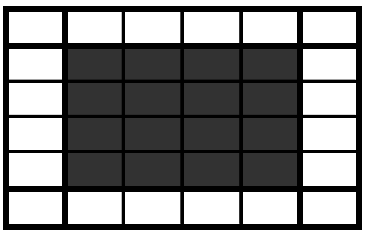
c. Scheme Setting (X_6, X_5, X_4, X_1)

It is used to set the display before driving phase if the clearing 1 and clearing 2 phase are applied.

Table 9-1: Example of Panel Display under different Schemes before Driving

Mapping of Panel



	X6X5 = 01	X6X5 = 11
X4 = X1 = 0		
X4 = X1 = 1		

9.5 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM COM 0 is mapped to COM0. With value equal to 1, RAM COM 1 is mapped to COM0 and so on.

Refer to Table 9-2 for more illustrations.

9.6 Set Control Scheme (80h)

This command stored up Control scheme into RAM. It would updated into the system once the driving update command (31h)

9.7 Set repeating phases (93h~97h)

These commands stored up the repeating phases for VA Clearing, VA Idle, AA Clearing, AA Idle and driving phase repeat times respectively. They can store up from 0 up to 15 times of repeat phase.

If VA or AA is set to 0, both 93h and 94h are needed to set 0 for VA clearing and idle; 95h and 96h are needed to set 0 for AA clearing before driving update.

9.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in Bistable module design.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

9.9 Set Bias Level (A2h)

This command is used to select a suitable bias ratio required for driving the particular LCD panel in use. 7 sets of Biasing level are embedded in the IC. The bias ratio setting N is 4, 5, 6, 7, 8 and 9.

9.10 Set Analog Control (A3h)

This command is used to enable the analog block of the system. For POR 00h is stored, two types of setting can be applied.
For standard application, A3h, 18h is applied into the system.
For extra BIAS VOLTAGE buffer application to much stabilize the buffer output level, A3h, 1Ah is applied the system after High Volt buffer is enabled (either 2Bh or 2Fh).

9.11 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display “ON” phase.

A5h command forces the entire display to be “ON”, regardless of the contents of the display data RAM and Set Normal/Inverse Display (A6h/A7h).

9.12 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

9.13 Set Multiplex Ratio (A8h)

This command switches the default 64 multiplex mode to any multiplex ratio, ranging from 2 to 64. The output pads COM0~COM63 will be switched to the corresponding COM signal.

9.14 Set Analog Auto On/ Off (A9h)

This command is used to init the system automatically. After executing Auto On command (A9h, 01h): The block would be init in a sequence of:

a. Analog Block
b. Oscillator
c. High Voltage Buffer
d. Charge Pump

If applied Auto off (A9h, 00h). The block would be shut down in:

a. Charge Pump
b. High Voltage Buffer
c. Oscillator
d. Analog Block

For the Analog Auto On/ off command, it is a master command on the Analog Block (A3h), Oscillator (F6h), BIAS VOLTAGE Buffer and Charge Pump (2Ah~2Fh).

9.15 Set Memory Addressing Mode (ADh)

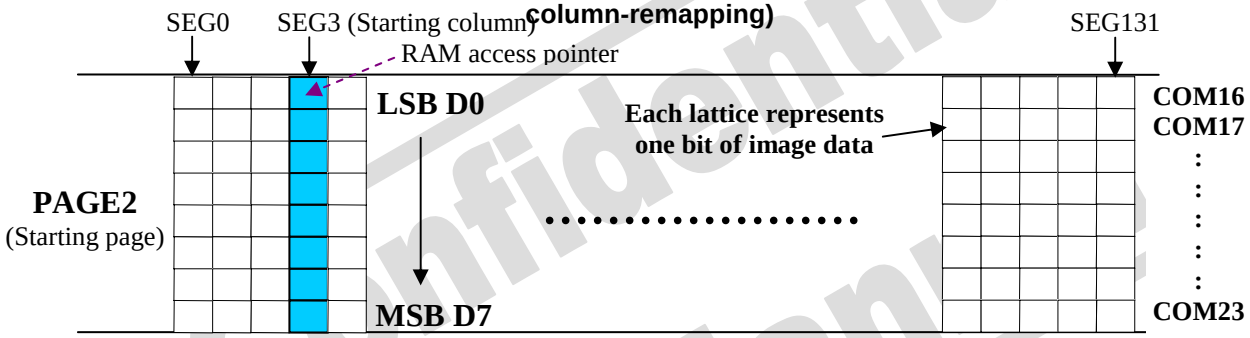
There are 2 different memory addressing mode in the IC: horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes. In there, “COL” means the graphic display data RAM column.

In normal display data RAM read or write and page-addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the start column address of pointer by command 10h~1Fh.
- Set the page start address of the target display location by command B0h to B7h.

For example, if the upper column address is 00h (0x10), lower column address is 03h (0x03) and the page address is set to 02h (0xB2) then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 9-1. The input data byte will be written into RAM position of column 3.

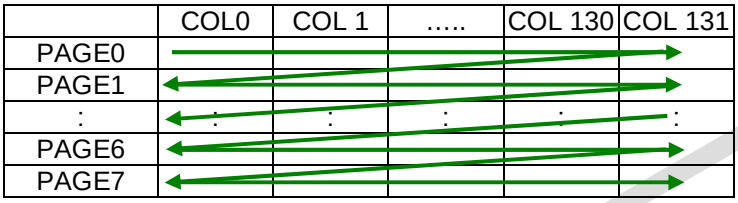
Figure 9-1 : Example of GDDRAM access pointer setting in Page Addressing Mode (No COM and column-remapping)



Horizontal addressing mode (0xAD, 0x00)

In horizontal addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 9-2.

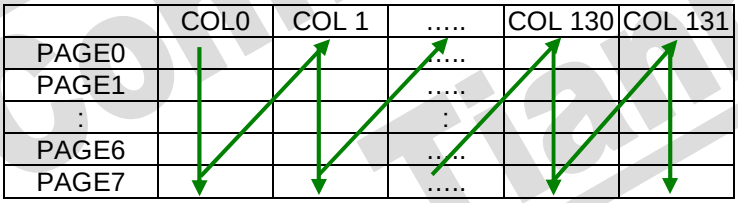
Figure 9-2 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (0xAD, 0x01)

In vertical addressing mode, after the display RAM is read / written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 9-3.

Figure 9-3 : Address Pointer Movement of Vertical addressing mode



9.16 Set Auto Charge Pump Threshold Value (AEh)

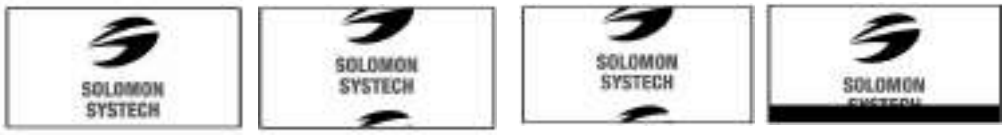
This command is used to select the booster setting, which is selected the 8x /16x booster. If the threshold of the Charge Pump setting is 0x20, 16x booster would be used when the contrast setting [located in 80h-87h] is larger than the threshold (e.g. 0x58, 30V). Otherwise, a 8x booster would be used. (e.g. 0x08,10V). For the voltage value table, please refer to Table 7-5 for reference.

9.17 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 7 in GDDRAM under Page Addressing Mode. Please refer to Section 9.15 for details.

Table 9-2 : Example of Set Display Offset and Display Start Line with no Remap

	Output												
	64		64		64		56		56		56		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offset (D3h)
pin name	0		0		8		0		0		8		Display start line (40h - 7Fh)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	-	-	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	-	-	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	-	-	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	-	-	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	-	-	Row55	RAM63	
COM56	Row56	RAM56	Row0	RAM0	Row56	RAM0	-	-	Row0	RAM0	-	-	
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	Row1	RAM1	-	-	
COM58	Row58	RAM58	Row2	RAM2	Row58	RAM2	-	-	Row2	RAM2	-	-	
COM59	Row59	RAM59	Row3	RAM3	Row59	RAM3	-	-	Row3	RAM3	-	-	
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	Row4	RAM4	-	-	
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	Row5	RAM5	-	-	
COM62	Row62	RAM62	Row6	RAM6	Row62	RAM6	-	-	Row6	RAM6	-	-	
COM63	Row63	RAM63	Row7	RAM7	Row63	RAM7	-	-	Row7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

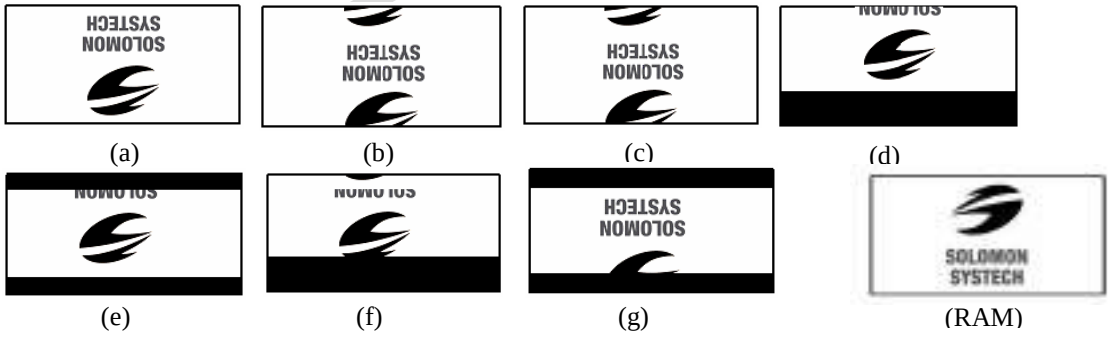


(a) (b) (c) (d)

(e) (f) (RAM)

Table 9-3: Example of Set Display Offset and Display Start Line with Remap

	Output														
	64		64		64		48		48		48		48		Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0h / C8h)
Hardware	0		56		0		0		56		0		56		Display offset (D3h)
pin name	0		0		8		0		0		8		16		Display start line (40h - 7Fh)
COM0	Row 63	RAM63	Row 7	RAM7	Row 63	RAM7	Row 47	RAM47	-	-	Row 47	RAM7	-	-	
COM1	Row 62	RAM62	Row 6	RAM6	Row 62	RAM6	Row 46	RAM46	-	-	Row 46	RAM6	-	-	
COM2	Row 61	RAM61	Row 5	RAM5	Row 61	RAM5	Row 45	RAM45	-	-	Row 45	RAM5	-	-	
COM3	Row 60	RAM60	Row 4	RAM4	Row 60	RAM4	Row 44	RAM44	-	-	Row 44	RAM4	-	-	
COM4	Row 59	RAM59	Row 3	RAM3	Row 59	RAM3	Row 43	RAM43	-	-	Row 43	RAM3	-	-	
COM5	Row 58	RAM58	Row 2	RAM2	Row 58	RAM2	Row 42	RAM42	-	-	Row 42	RAM2	-	-	
COM6	Row 57	RAM57	Row 1	RAM1	Row 57	RAM1	Row 41	RAM41	-	-	Row 41	RAM1	-	-	
COM7	Row 56	RAM56	Row 0	RAM0	Row 56	RAM0	Row 40	RAM40	-	-	Row 40	RAM0	-	-	
COM8	Row 55	RAM55	Row 63	RAM63	Row 55	RAM63	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 47	RAM63	
COM9	Row 54	RAM54	Row 62	RAM62	Row 54	RAM62	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 46	RAM62	
COM10	Row 53	RAM53	Row 61	RAM61	Row 53	RAM61	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 45	RAM61	
COM11	Row 52	RAM52	Row 60	RAM60	Row 52	RAM60	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 44	RAM60	
COM12	Row 51	RAM51	Row 59	RAM59	Row 51	RAM59	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 43	RAM59	
COM13	Row 50	RAM50	Row 58	RAM58	Row 50	RAM58	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 42	RAM58	
COM14	Row 49	RAM49	Row 57	RAM57	Row 49	RAM57	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 41	RAM57	
COM15	Row 48	RAM48	Row 56	RAM56	Row 48	RAM56	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 40	RAM56	
COM16	Row 47	RAM47	Row 55	RAM55	Row 47	RAM55	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 39	RAM55	
COM17	Row 46	RAM46	Row 54	RAM54	Row 46	RAM54	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 38	RAM54	
COM18	Row 45	RAM45	Row 53	RAM53	Row 45	RAM53	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 37	RAM53	
COM19	Row 44	RAM44	Row 52	RAM52	Row 44	RAM52	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 36	RAM52	
COM20	Row 43	RAM43	Row 51	RAM51	Row 43	RAM51	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 35	RAM51	
COM21	Row 42	RAM42	Row 50	RAM50	Row 42	RAM50	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 34	RAM50	
COM22	Row 41	RAM41	Row 49	RAM49	Row 41	RAM49	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 33	RAM49	
COM23	Row 40	RAM40	Row 48	RAM48	Row 40	RAM48	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 32	RAM48	
COM24	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 31	RAM47	
COM25	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 30	RAM46	
COM26	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 29	RAM45	
COM27	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 28	RAM44	
COM28	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 27	RAM43	
COM29	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 26	RAM42	
COM30	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 25	RAM41	
COM31	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 24	RAM40	
COM32	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	Row 23	RAM39	
COM33	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	Row 22	RAM38	
COM34	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	Row 21	RAM37	
COM35	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	Row 20	RAM36	
COM36	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	Row 19	RAM35	
COM37	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	Row 18	RAM34	
COM38	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	Row 17	RAM33	
COM39	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	Row 16	RAM32	
COM40	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	Row 15	RAM31	
COM41	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	Row 14	RAM30	
COM42	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	Row 13	RAM29	
COM43	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	Row 12	RAM28	
COM44	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 3	RAM3	Row 11	RAM11	Row 3	RAM11	Row 11	RAM27	
COM45	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	Row 10	RAM26	
COM46	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	Row 9	RAM25	
COM47	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	Row 8	RAM24	
COM48	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	-	-	Row 7	RAM7	-	-	Row 7	RAM23	
COM49	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	-	-	Row 6	RAM6	-	-	Row 6	RAM22	
COM50	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	-	-	Row 5	RAM5	-	-	Row 5	RAM21	
COM51	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	-	-	Row 4	RAM4	-	-	Row 4	RAM20	
COM52	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	-	-	Row 3	RAM3	-	-	Row 3	RAM19	
COM53	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	-	-	Row 2	RAM2	-	-	Row 2	RAM18	
COM54	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	-	-	Row 1	RAM1	-	-	Row 1	RAM17	
COM55	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	-	-	Row 0	RAM0	-	-	Row 0	RAM16	
COM56	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	-	-	-	-	-	-	-	-	
COM57	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	-	-	-	-	-	-	-	-	
COM58	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	-	-	-	-	-	-	-	-	
COM59	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	-	-	-	-	-	-	-	-	
COM60	Row 3	RAM3	Row 11	RAM11	Row 3	RAM11	-	-	-	-	-	-	-	-	
COM61	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	-	-	-	-	-	-	-	-	
COM62	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	-	-	-	-	-	-	-	-	
COM63	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



9.18 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the Bistable module design. If this command is sent then the graphic display will be vertically flipped on next Driving Update.

Refer to Table 9-2 for more illustrations.

9.19 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).
For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 – 16, so the second byte would be 100000b.

9.20 Software Reset (E2h)

This command is used to reset the system into initial phase mentioned in Section 7.1by input (E2h, E3h) into the system.

9.21 NOP (E3h)

No Operation Command

9.22 Set Bias Enable (E9h)

This command is used to enable the resistor ladder of the bias divider circuit by (E9h, 84h) and disable the circuit by (E9h, 04h).

9.23 Set Oscillator Enable (F6h)

This command is used to enable the internal oscillator (F6h, 40h) and disable the circuit by (F6h, 00h).

9.24 Set Clock Output Enable (FEh)

This command is used to enable the Clock Mode (FEh, 80h) which enable signal output on CL, SYNCM, SYNCC and SYNCD; Disable the Clock Mode by (FEh, 00h).

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings

(Voltage Reference to V_{SS} = 0V)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +3.6	V
V_{DDIO}		-0.3 to Min(V_{DD} +0.5,+3.6)	V
V_0		-0.3 to 38	V
V_{CI}		-0.3 to +3.6	V
V_{in}	Input Voltage	V_{SS} -0.3 to V_{DDIO} +0.3	V
T_A	Operating Temperature	-30 to +80	ºC
T_{STG}	Storage Temperature Range	-65 to +150	ºC

Maximum Ratings are those beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

11 DC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

V_{DD} = 2.4 to 3.5V

T_A = 25°C

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min	Typ	Max	Unit
V_{DD}	IC logic Power supply	-	V_{DD}	2.4	2.8	3.5	V
V_{DDIO}	MCU interface logic level power supply	-	V_{DDIO}	1.6	-	V_{DD}	V
V_{CI}	Charge Pump power supply	-	V_{CI}	-	V_{DD}	-	V
V_0	Panel driving power supply	-	V_0	14	-	35	V
V_{OH}	Logic High Output Voltage	IVOUT = -100uA	MCU interface pins	0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Logic Low Output Voltage	IVOUT = 100uA	MCU interface pins	0	-	0.1* V_{DDIO}	V
V_{IH}	Logic High Input voltage		MCU interface pins	0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Logic Low Input voltage		MCU interface pins	0	-	0.2* V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V_{OUT} = V_{DDIO}-0.4V V_{OUT} = 0.4V		50	-	-	uA
I_{OL}	Logic Low Output Current Drain	V_{OUT} = V_{DDIO}-0.4V V_{OUT} = 0.4V		-	-	-50	uA
I_{SLP}	Sleep mode Current	V_{DD}=2.8V, OSC OFF, Charge Pump off, No panel attached	V_{DD}	-5	-	+5	uA
I_{SLP}	Sleep mode Current	V_{DDIO}=2.8V, OSC OFF, Charge Pump off, No panel attached	V_{DDIO}	-5	-	+5	uA
I_{SLP}	Sleep mode Current	V_{CI}=2.8V, OSC OFF , Charge Pump off, No panel attached	V_{CI}	-5	-	+5	uA
I_{SLP}	Sleep mode Current	V_{CI}=2.8V, OSC OFF , Charge Pump off, No panel attached	Total of V_{DD} ,V_{DDIO} ,V_{CI}	-5	-	+5	uA
I_{DP1}	Display Mode Supply Current	V_{DD} = V_{CI} = 2.8V, V0 = 30V, Charge Pump On, Bias Voltage Buffer Off, No driving Update	V_{DD}	-	100	-	uA
I_{DP1}	Display Mode Supply Current	V_{DD} = V_{CI} = 2.8V, V0 = 30V, Charge Pump On, Bias Voltage Buffer Off, No driving Update	V_{CI}	-	1.5	-	mA
I_{OZ}	Logic Output Tri-state Current Drain Source			-1	-	1	uA
I_{IL}/I_{IH}	Logic Input Current			-1	-	1	uA
C_{IN}	Logic Pins Input Capacitance			-	5	7.5	pF

12 AC CHARACTERISTICS

Conditions:
Voltage referenced to V_{SS}
V_{DD} = 2.8V
T_A = 25°C

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Internal Oscillator Enabled, V_{DD} = 2.8V		200		kHz

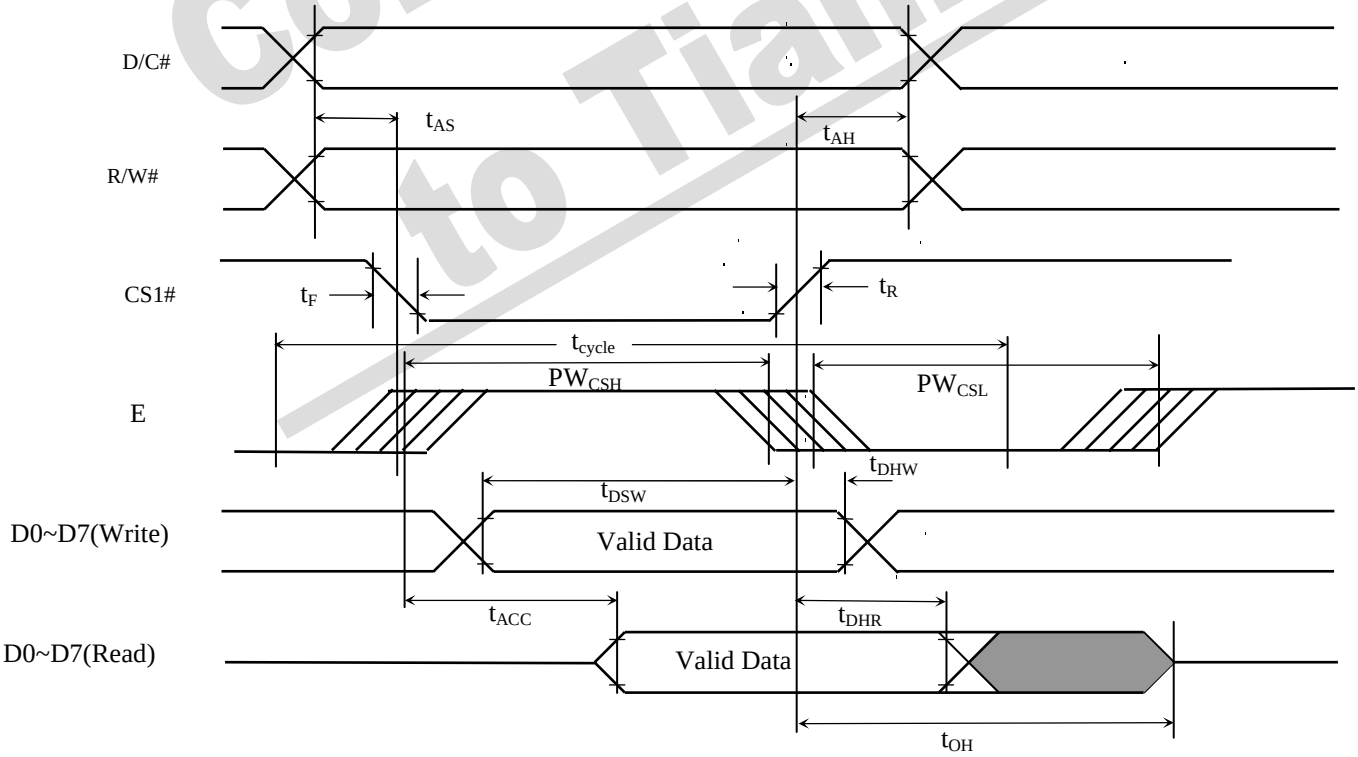
Conditions:

T_A = -35 to 85°C
V_{DD} = V_{CI} = 2.4V to 3.5V
V_{DDIO} = 1.6V to 2.4V

Table 12-2 : Parallel 6800-series Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	200	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	-	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 100	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	200 100	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 12-1 : Parallel 6800-series Interface Timing Characteristics



The PW_{CSH} timing reference is 50% of the rising / falling edge of E or CS1# pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of E or CS1# pin.

Conditions:

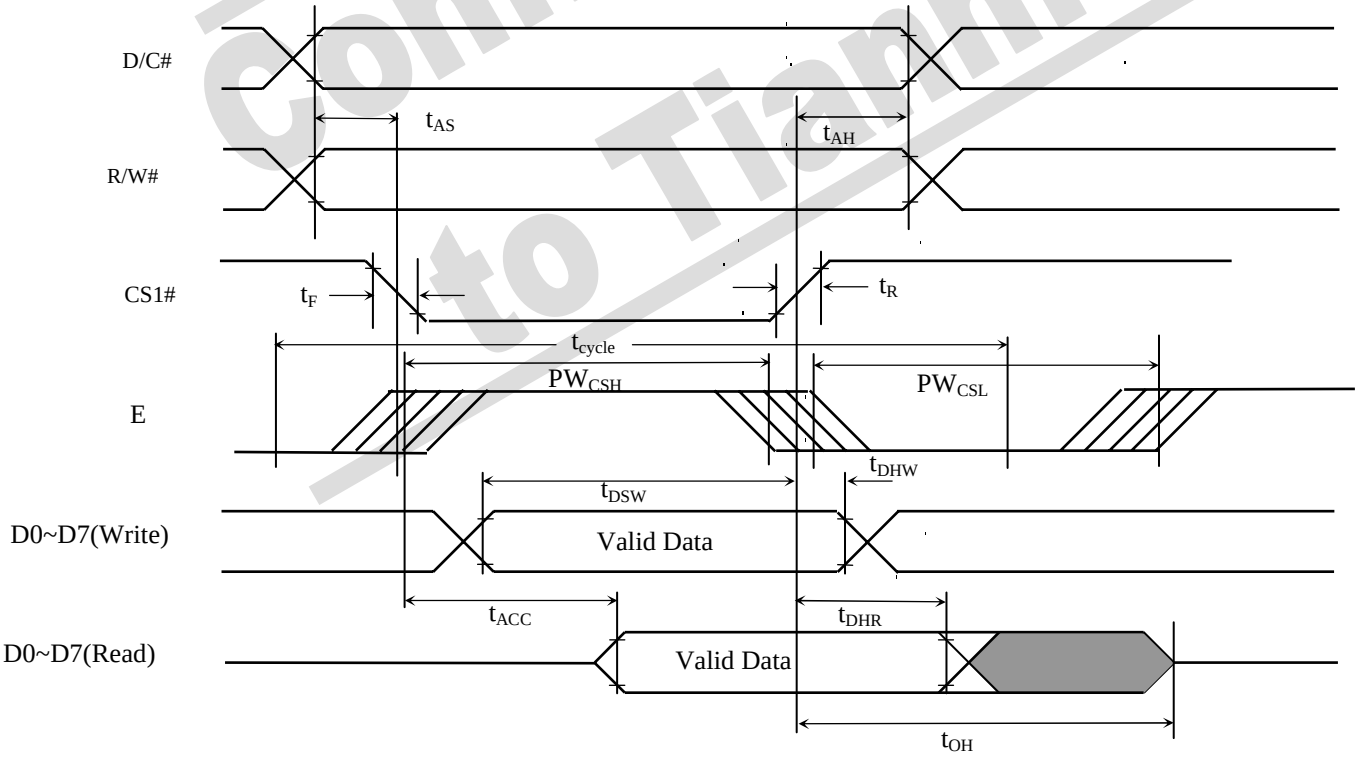
T_A = -35 to 85°C

V_{DD} = V_{CI} = V_{DDIO} = 2.4V to 3.5V

Table 12-3 : Parallel 6800-series Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	100 50	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 12-2 : Parallel 6800-series Interface Timing Characteristics



The PW_{CSH} timing reference is 50% of the rising / falling edge of E or CS1# pin.

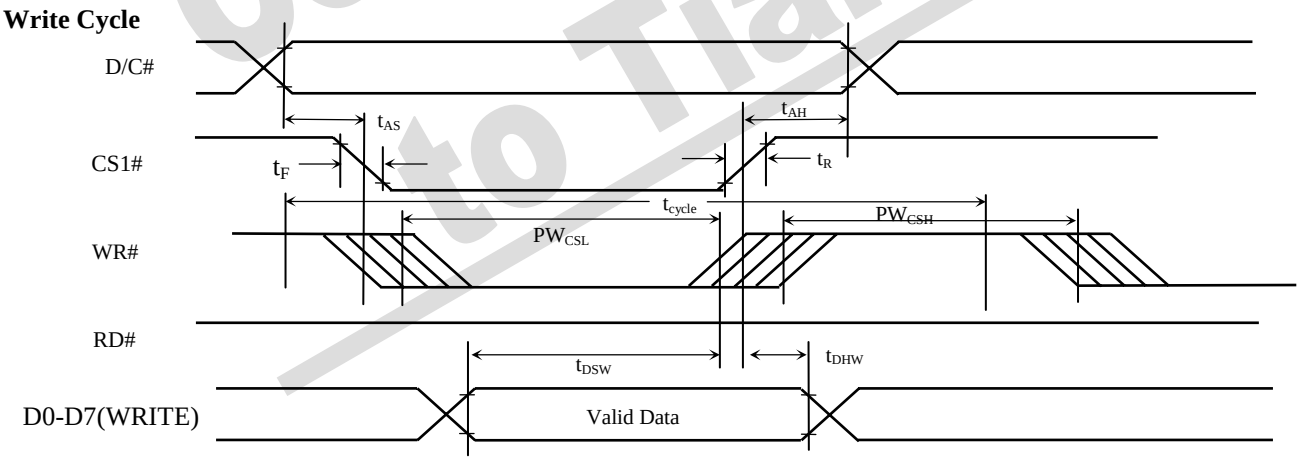
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of E or CS1# pin.

Conditions:
T_A = -35 to 85°C
V_{DD} = V_{CI} = 2.4V to 3.5V
V_{DDIO} = 1.6V to 2.4V

Table 12-4 : Parallel 8080-series Interface Timing Characteristics

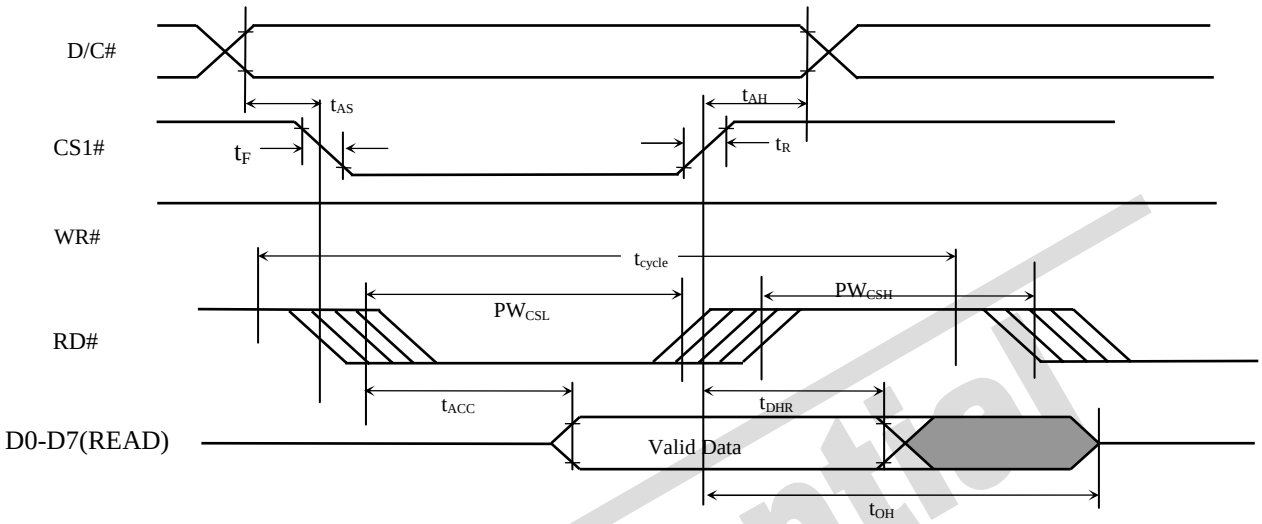
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	200	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 100	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	200 100	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 12-3 : Parallel 8080-series Interface Timing Characteristics



The PW_{CSL} timing reference is 50% of the rising / falling edge of WR# or CS1# pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of WR# or CS1# pin.

Read Cycle



The PW_{CSL} timing reference is 50% of the rising / falling edge of RD# or CS1# pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of RD# or CS1# pin.

Conditions:

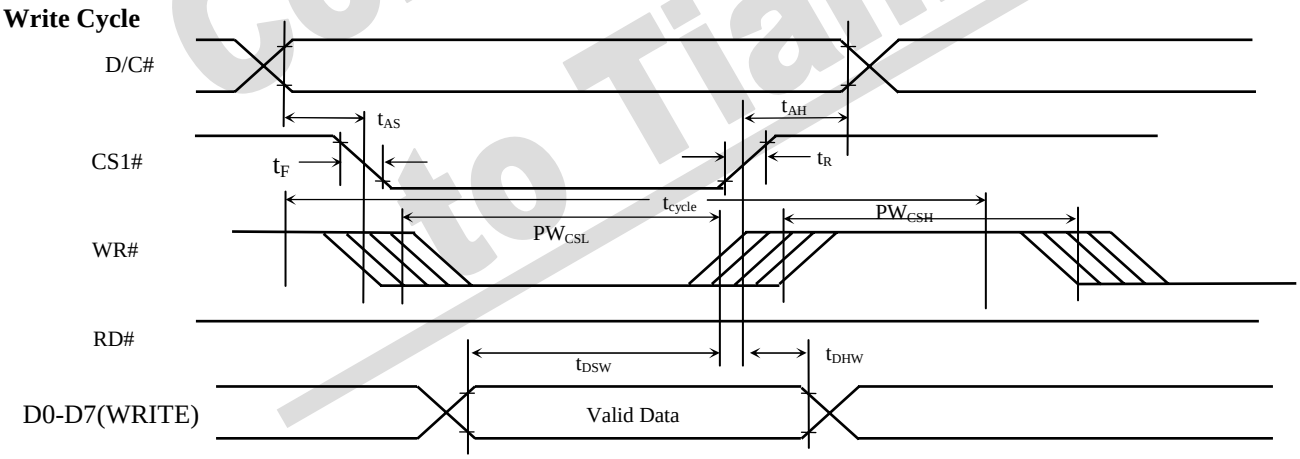
T_A = -35 to 85°C

V_{DD} = V_{CI} = V_{DDIO} = 2.4V to 3.5V

Table 12-5 : Parallel 8080-series Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	100 50	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

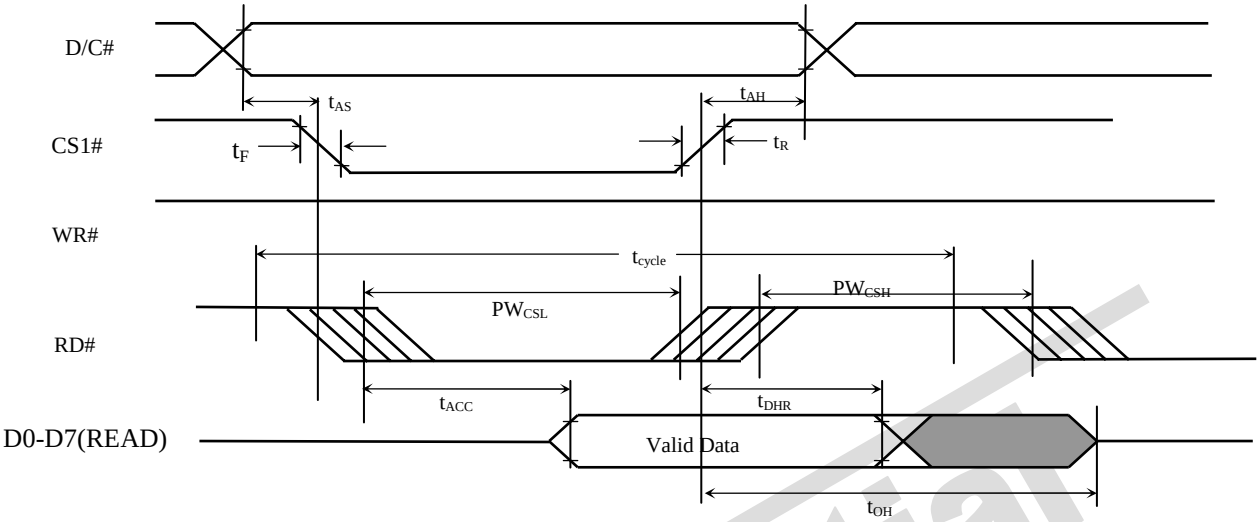
Figure 12-4 : Parallel 8080-series Interface Timing Characteristics



The PW_{CSL} timing reference is 50% of the rising / falling edge of WR# or CS1# pin.

The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of WR# or CS1# pin.

Read Cycle



The PW_{CSL} timing reference is 50% of the rising / falling edge of RD# or CS1# pin.
The t_{DSW} and t_{DHW} timing is reference to the 50% of rising / falling edge of RD# or CS1# pin.

Conditions:

T_A = -35 to 85°C

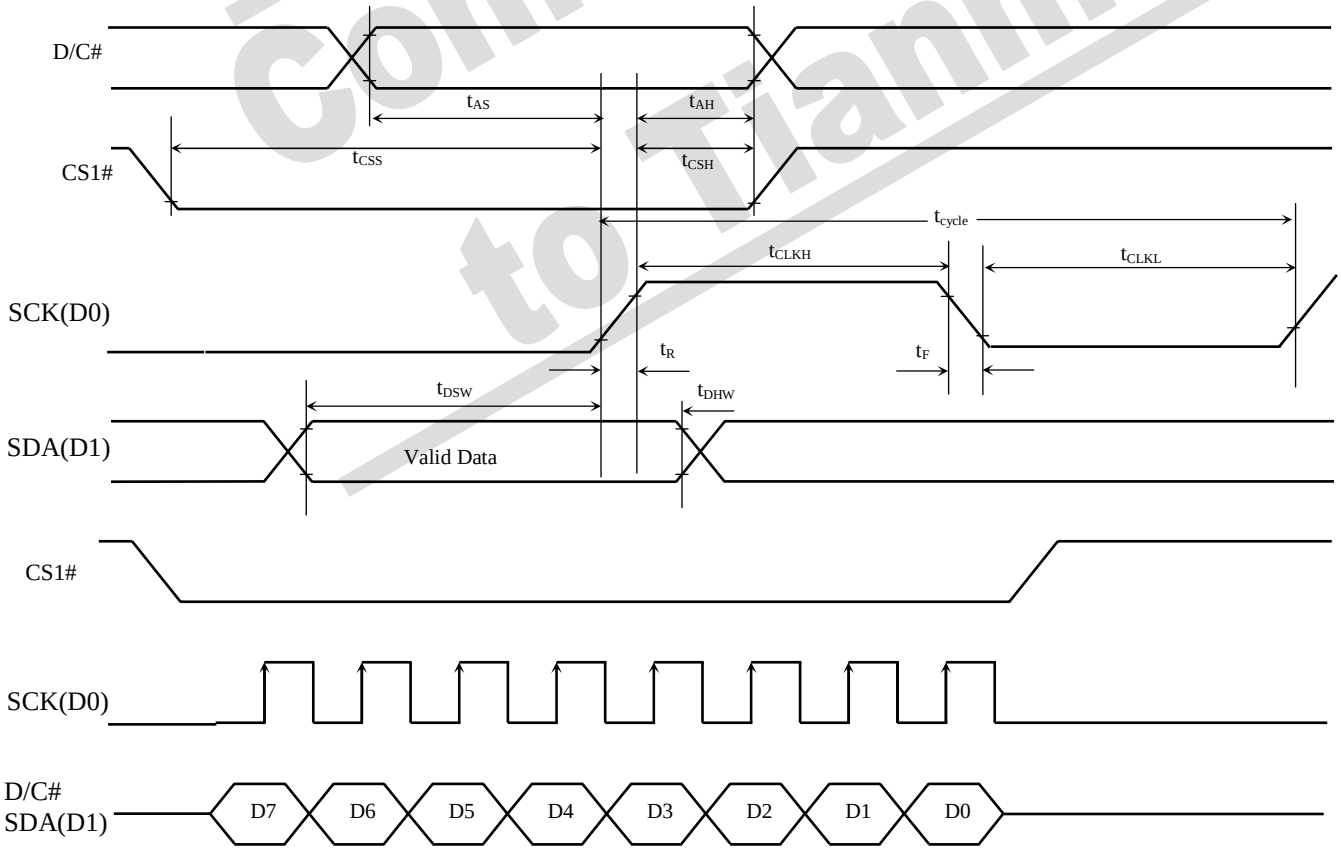
V_{DD} = V_{CI} = 2.4V to 3.5V

V_{DDIO} = 1.6V to 2.4V

Table 12-6 : 4-wires Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	120	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	60	-	-	ns
t_{DHW}	Write Data Hold Time	60	-	-	ns
t_{CLKL}	Clock Low Time	60	-	-	ns
t_{CLKH}	Clock High Time	60	-	-	ns
t_{CSS}	Chip Select Setup Time (for D7 input)	60	-	-	ns
t_{CSH}	Chip Select Hold Time (for D0 input)	60	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 12-5 : 4-wires Serial Interface Timing Characteristics



Conditions:

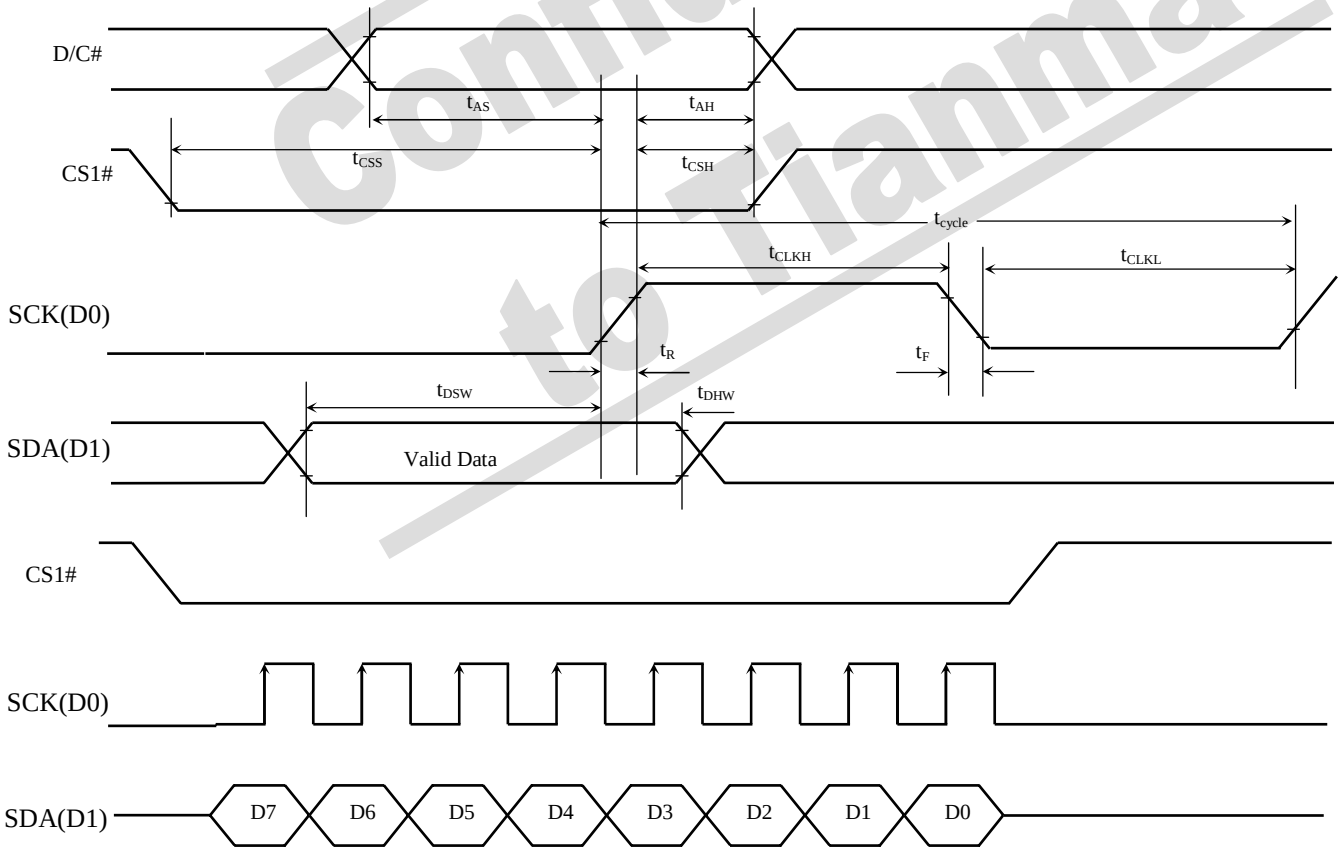
T_A = -35 to 85°C

V_{DD} = V_{CI} = V_{DDIO} = 2.4V to 3.5V

Table 12-7 : 4-wires Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	60	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
T_{CLKL}	Clock Low Time	30	-	-	ns
T_{CLKH}	Clock High Time	30	-	-	ns
t_{CSS}	Chip Select Setup Time (for D7 input)	30	- -	- -	ns
t_{CSH}	Chip Select Hold Time (for D0 input)	30	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 12-6 : 4-wires Serial Interface Timing Characteristics



Conditions:

T_A = -35 to 85°C

V_{DD} = V_{CI} = V_{DDIO} = 2.4V to 3.5V

Table 12-8 : 3-wire Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	80	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	30	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	20	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	40	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 12-7 : 3-wire Serial interface characteristics

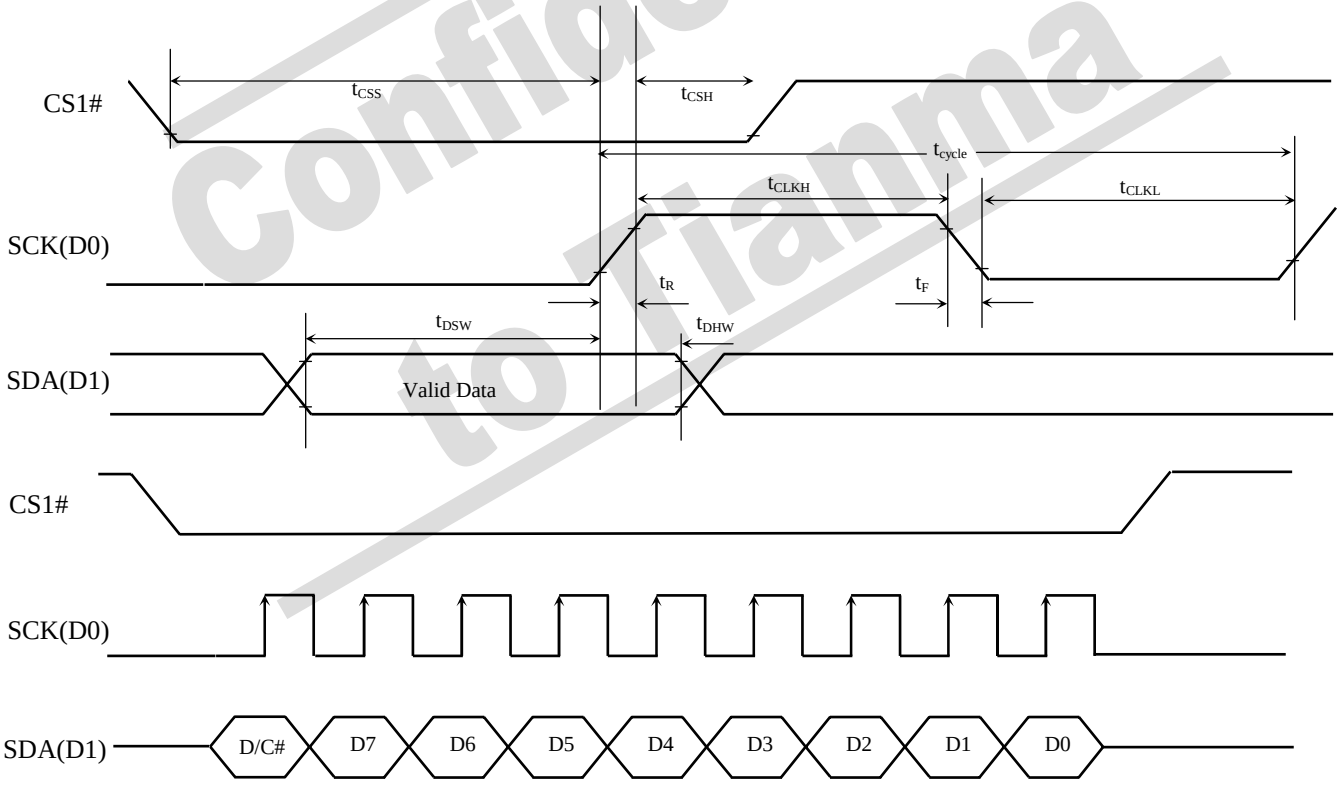


Table 12-9 : I²C Interface Timing Characteristics

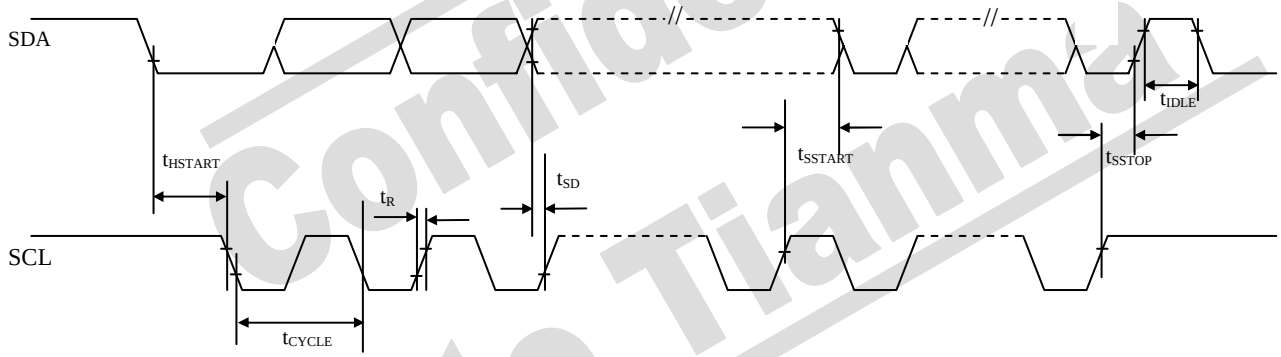
Conditions:

T_A = -35 to 85°C

V_{DD} = V_{CI} = V_{DDIO} = 2.4V to 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

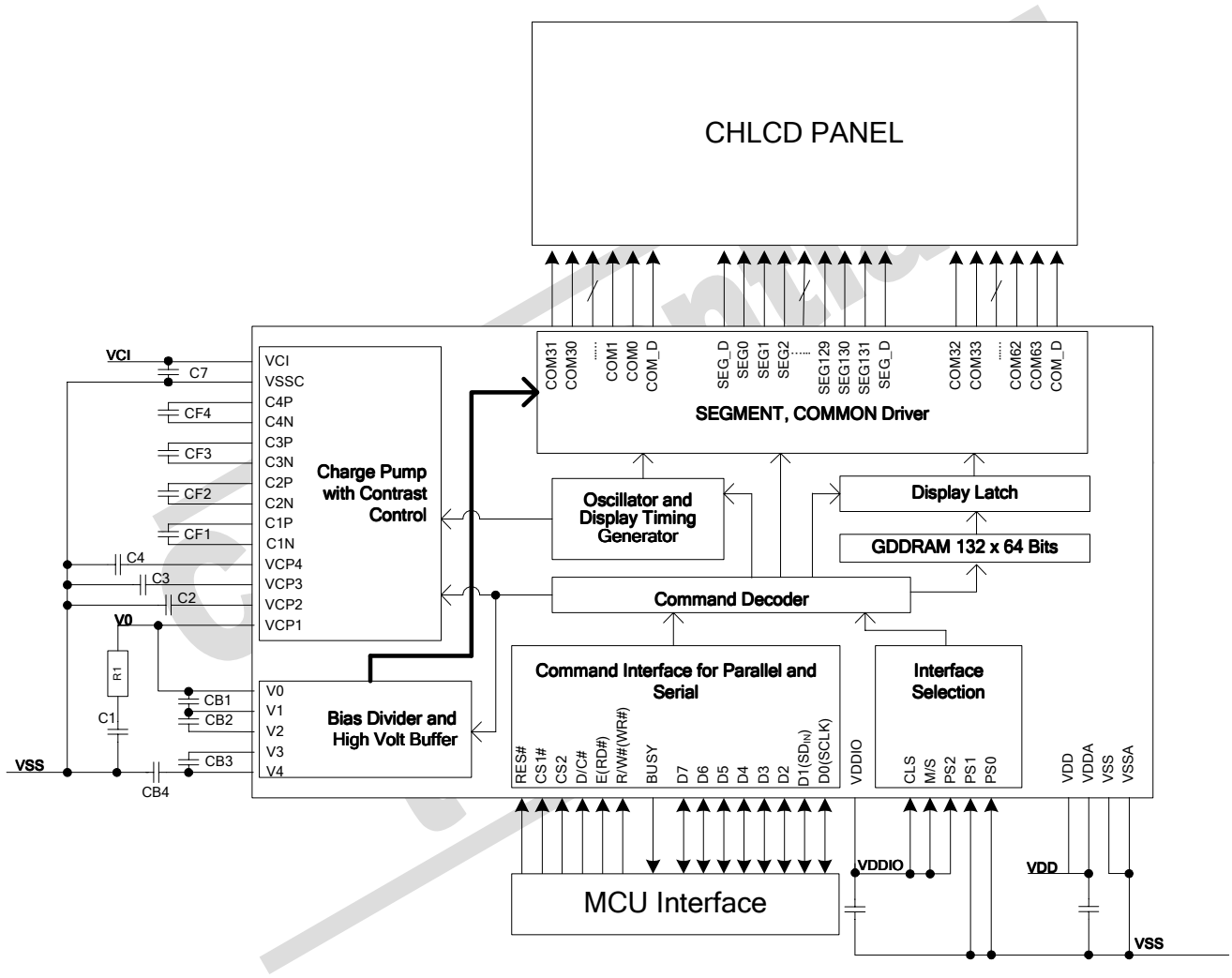
Figure 12-8 : I²C Interface Timing Characteristics



13 APPLICATION EXAMPLE

13.1 Single Chip Application

Figure 13-1 : 8 bit 8080 interface, internal clock, internal Charge Pump application circuit



Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, CS1#, CS2, RES#

Note

(1) The capacitor value refers to Table 7-6

Table 13-1: Typical Start up Procedure with Init Code

Power Up	Power on Vdd and Vddio
Reset	Pull the RES# low with 10ms
Start Up Command (in Hex)	
E9	Enable BIAS VOLTAGE Resistor
84	
80	Set Control Table
00	
00	
00	
(D)	(D) is Clearing Duration
(E)	(E) is Idle Duration
(F)	(F) is Driving Duration
(G)	(G) is Clearing Voltage level
(H)	(H) is Bias Voltage level
93	No of Clearing 1 Repeat Phase
01	Set to 1
94	No of Idle 1 Repeat Phase
01	Set to 1
95	No of Clearing 2 Repeat Phase
01	Set to 1
96	No of Idle 2 Repeat Phase
01	Set to 1
97	No of Driving Repeat Phase
01	Set to 1
32	Select Driving Scheme
00	Default polarity
A3	Enable others analog block
1A	
A9	Automatically Enable the analog block
01	
31	Driving Update to execute the parameter setting

Table 13-2: Typical Write RAM Procedure with Driving Update

A0/A1	Segment Remap
C0/C8	Column Remap
A2,##	## is the LCD Bias Setting
AD,00	Using Horizontal addressing mode
10	Set Higher Column Address to 0
00	Set Lower Column Address to 0
B0	Set Page Address to 0
Write RAM	
31	Driving Update

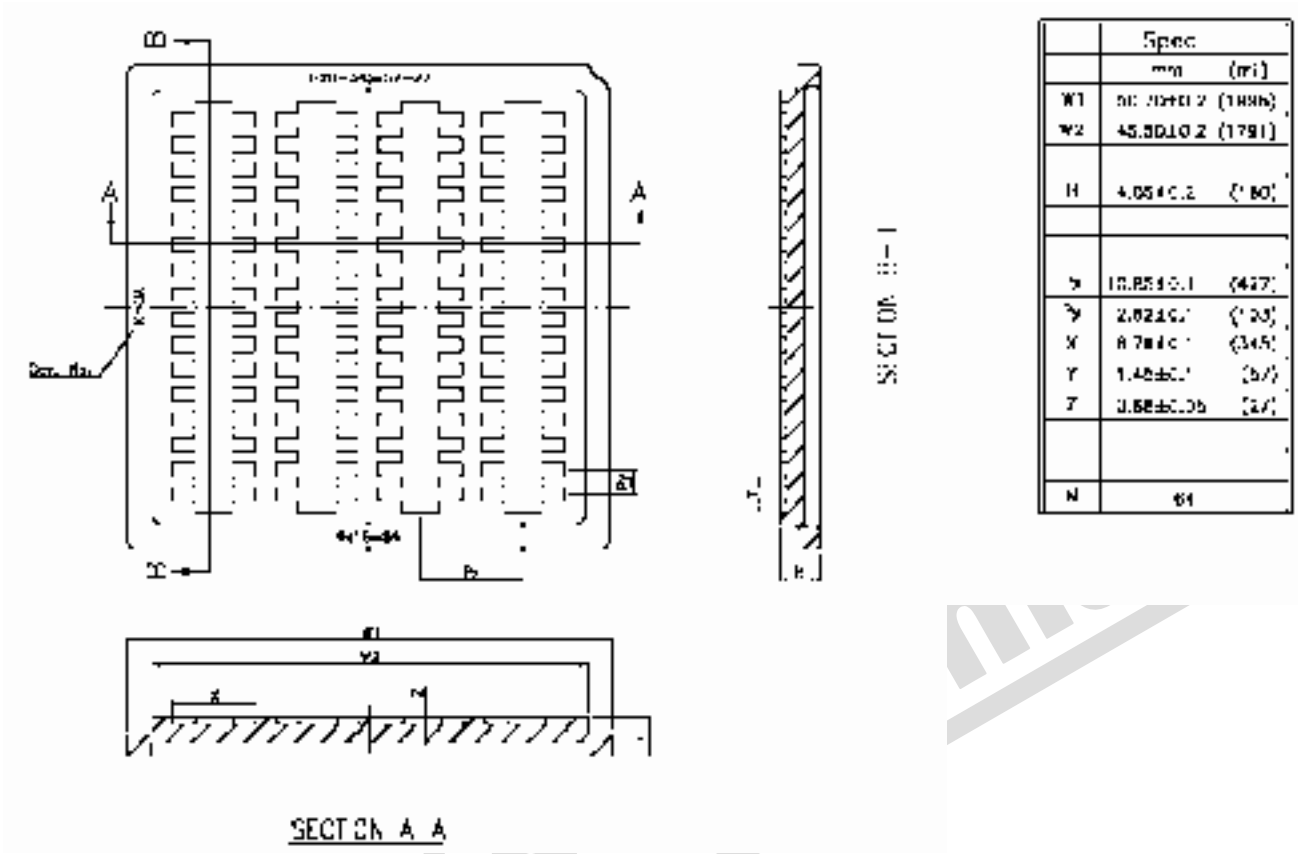
Table 13-3: Typical Power Off sequence

E9	Disable BIAS VOLTAGE Resistor
04	
A3	Disable others analog block
00	
A9	Automatically Power off
00	

14 PACKAGE INFORMATION

14.1 SSD1603Z Die Tray Information

Figure 14-1 : SSD1603Z die tray information



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