

SSD1327

Advance Information

128 x 128, 16 Gray Scale Dot Matrix OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1327

Rev 1.1

P 1/68

Dec 2008

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Appendix: IC Revision history of SSD1327 Specification

| Version | Change Items | Effective Date |
|----------------|--|-----------------------|
| 0.10 | 1 st release | 30-May-08 |
| 0.20 | P.17 Added TR[6:0] on pin description section P.37, 38 Added notes for commands B1h and B8h on command table P.54 Updated the DC characteristics table P.55 Updated the AC characteristics table | 04-Sep-08 |
| 0.30 | P.8, 10 Revise die thickness tolerance from $\pm 25\mu\text{m}$ to $\pm 15\mu\text{m}$ P.11, 12 Revised the typo of LVSS to VLSS on the table of SSD1327Z Bump Die Pad Coordinates P.15, 39, 50 Added command D5h and corresponding information on the command table and related section P.49 Added display on and display off sequences P.62 Added notes (4) and (5) on the application example of SSD1327Z | 21-Nov-08 |
| 1.0 | Change to Advance information P.7 Added title " V_{CI} and V_{DD} range" for Table 2-1 P.35 Updated section 8.10 VDD regulator P.37 Revised command table of "Function Selection A (ABh)" P.49 Revised description of section 10.1.10 Function Selection A (ABh) P.49, 50 Revised section 10.1.11 Set display ON/OFF P.59 – 63 Updated the condition of AC characteristics from ($V_{DD} - V_{SS} = 2.4\text{V}$ to 2.6V , $V_{CI} = 3.3\text{V}$) to ($V_{CI} - V_{SS} = 1.65\text{V}$ to 3.5V) on Table 13-2 to Table 13-6 | 09-Dec-08 |
| 1.1 | P.38 Added a note for command B6h on command table P.51 Revised the description of command B6h | 23-Dec-08 |

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1 GENERAL DESCRIPTION

SSD1327 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 128 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1327 displays data directly from its internal 128 x 128 x 4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable I²C Interface, 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

2 FEATURES

- Resolution: 128 x 128 matrix panel
- Power supply
 - $V_{CC} = 8V \sim 18V$ (Panel driving power supply)
 - $V_{CI} = 1.65V - 3.5V$ (MCU interface logic level & low voltage power supply)
 - $V_{DD} = 1.65V - 2.6V$ (Core V_{DD} power supply, details refer to Table 2-1)

Table 2-1 V_{CI} and V_{DD} range

| V_{CI} | V_{DD} | Remark |
|---------------|--------------|---|
| 1.65 V ~ 2.6V | 1.65V ~ 2.6V | V_{DD} should be tied to V_{CI} and supplied by external power source |
| 2.6V ~ 3.5V | 2.4V ~ 2.6V | V_{DD} is regulated from V_{CI} |

- V_{CI} must be higher than or equivalent to V_{DD} at any circumstance
- For matrix display
 - Segment maximum source current: 300uA
 - Common maximum sink current: 40mA
 - 256 step contrast brightness current control
- Embedded 128 x 128 x 4 bit SRAM display buffer
- 16 gray scale
- Pin selectable MCU Interfaces:
 - 8-bit 6800/8080-series parallel interface
 - 3/4 wire Serial Peripheral Interface
 - I²C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Programmable Frame Rate
- Programmable Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Power On Reset (POR)
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

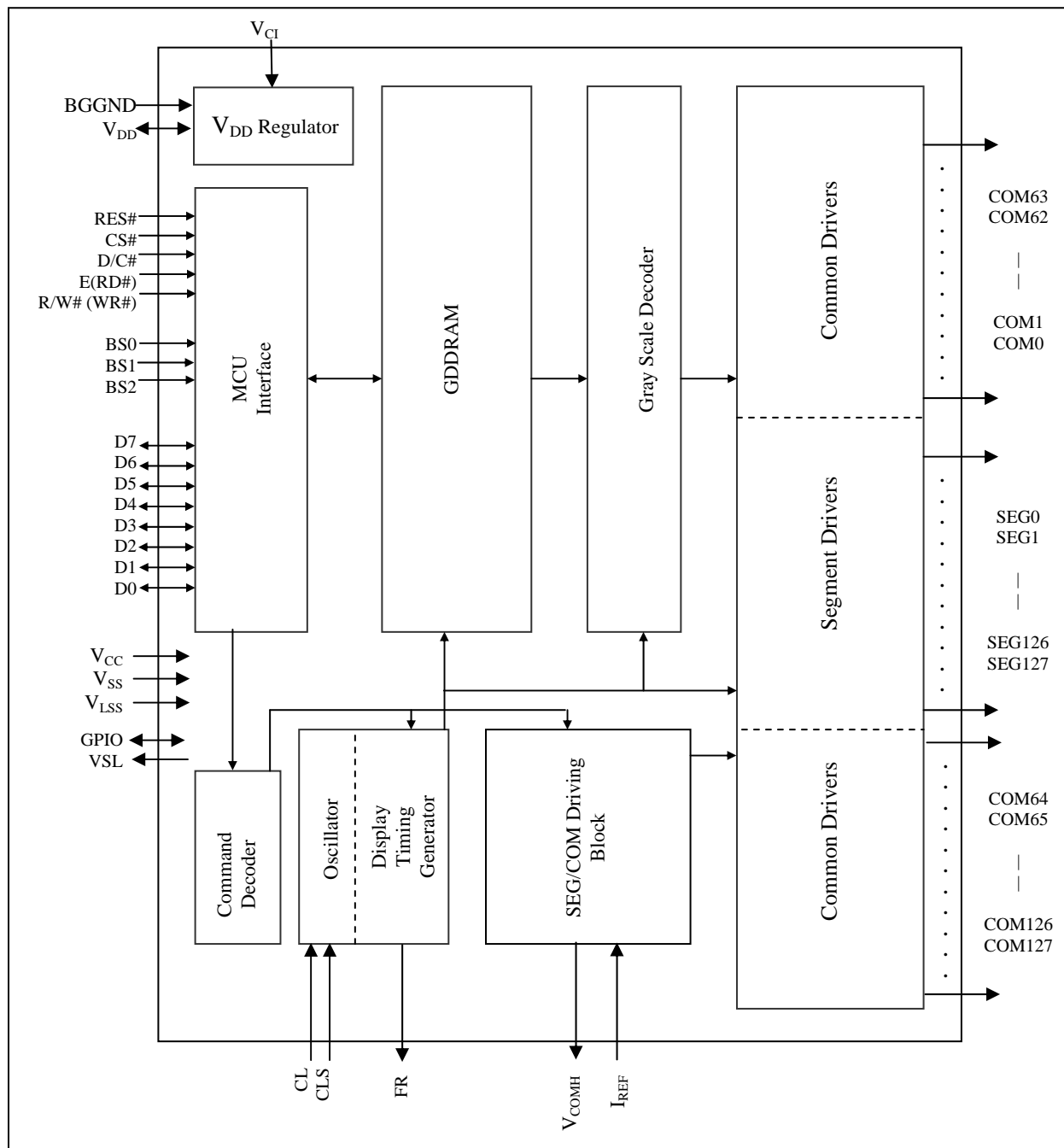
3 ORDERING INFORMATION

Table 3-1: Ordering Information

| Ordering Part Number | SEG | COM | Package Form | Reference | Remark |
|----------------------|-----|-----|--------------|-----------|--|
| SSD1327Z | 128 | 128 | COG | Page 10 | <ul style="list-style-type: none">○ Min SEG pad pitch : 28um○ Min COM pad pitch : 28um○ Min I/O pad pitch : 60um○ Die thickness: 300 +/- 15um |
| SSD1327UR1 | 128 | 80 | COF | Page 13 | <ul style="list-style-type: none">○ Output lead pitch: 0.12mm x 0.998 = 0.11976mm○ 4 SPH, 35m film○ 8-bit 80 / 68 / I²C / 4 line SPI interfaces |

4 BLOCK DIAGRAM

Figure 4-1: SSD1327 Block Diagram



5 DIE PAD FLOORPLAN

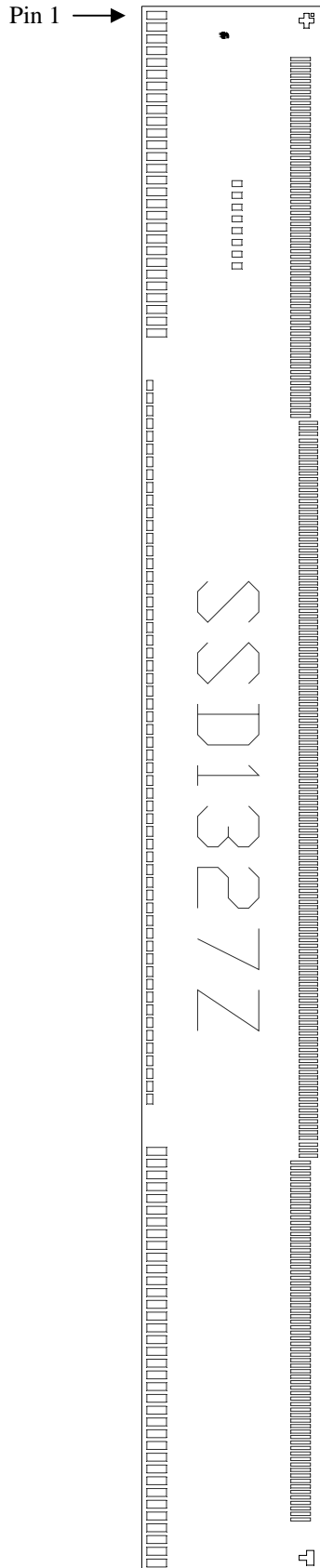


Figure 5-1: SSD1327Z Die Drawing

| | |
|-------------------|------------------|
| Die size | 8.0 mm x 0.92 mm |
| Die thickness | 300 +/- 15um |
| Min I/O pad pitch | 60um |
| Min SEG pad pitch | 28um |
| Min COM pad pitch | 28um |
| Bump height | Nominal 15um |

| Bump size | | |
|------------------|-------|-------|
| Pad# | X[um] | Y[um] |
| 1-28, 86-121 | 40 | 100 |
| 29-85 | 50 | 30 |
| 122-187, 322-387 | 16 | 100 |
| 188-321 | 16 | 94 |
| 388-395 | 30 | 50 |

| Alignment mark | Position | Size |
|----------------|--------------|-------------|
| + shape | (-3920, 380) | 75um x 75um |
| T shape | (3920, 380) | 75um x 75um |
| SSL Logo | (-3843, -27) | - |

(For details dimension please see Figure 5-2)

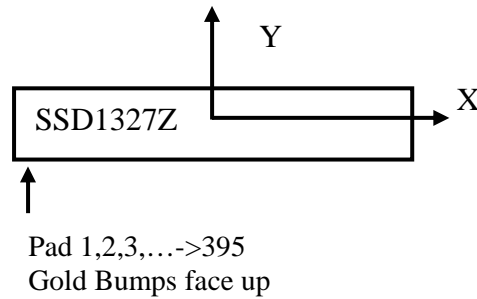


Figure 5-2: SSD1327Z alignment mark dimension

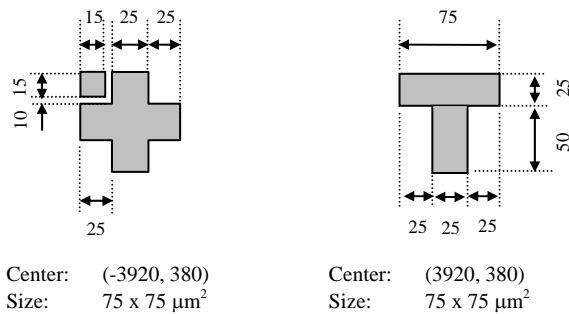


Table 5-1: SSD1327Z Bump Die Pad Coordinates

| Pad no. | Pin name | X-pos | Y-pos | Pad no. | Pin name | X-pos | Y-pos | Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|-------|---------|----------|-------|-------|---------|----------|-------|-------|
| 1 | NC | -3947 | -385 | 81 | VLSS | 1320 | -420 | 161 | COM26 | 2632 | 350 |
| 2 | VSL | -3887 | -385 | 82 | VLSS | 1385 | -420 | 162 | COM25 | 2604 | 350 |
| 3 | VSL | -3827 | -385 | 83 | VLSS | 1450 | -420 | 163 | COM24 | 2576 | 350 |
| 4 | VLSS | -3767 | -385 | 84 | VLSS | 1515 | -420 | 164 | COM23 | 2548 | 350 |
| 5 | VLSS | -3707 | -385 | 85 | VLSS | 1580 | -420 | 165 | COM22 | 2520 | 350 |
| 6 | VSS | -3647 | -385 | 86 | VLSS | 1847 | -385 | 166 | COM21 | 2492 | 350 |
| 7 | VSS | -3587 | -385 | 87 | IREF | 1907 | -385 | 167 | COM20 | 2464 | 350 |
| 8 | BGGND | -3527 | -385 | 88 | FR | 1967 | -385 | 168 | COM19 | 2436 | 350 |
| 9 | NC | -3467 | -385 | 89 | CL | 2027 | -385 | 169 | COM18 | 2408 | 350 |
| 10 | VCC | -3407 | -385 | 90 | VSS | 2087 | -385 | 170 | COM17 | 2380 | 350 |
| 11 | VCC | -3347 | -385 | 91 | CS# | 2147 | -385 | 171 | COM16 | 2352 | 350 |
| 12 | VCC | -3287 | -385 | 92 | RES# | 2207 | -385 | 172 | COM15 | 2324 | 350 |
| 13 | VCOMH | -3227 | -385 | 93 | D/C# | 2267 | -385 | 173 | COM14 | 2296 | 350 |
| 14 | VCOMH | -3167 | -385 | 94 | VSS | 2327 | -385 | 174 | COM13 | 2268 | 350 |
| 15 | GPIO | -3107 | -385 | 95 | R/W(WR#) | 2387 | -385 | 175 | COM12 | 2240 | 350 |
| 16 | VDD | -3047 | -385 | 96 | E(RD#) | 2447 | -385 | 176 | COM11 | 2212 | 350 |
| 17 | VCI | -2987 | -385 | 97 | D0 | 2507 | -385 | 177 | COM10 | 2184 | 350 |
| 18 | VCI | -2927 | -385 | 98 | D1 | 2567 | -385 | 178 | COM9 | 2156 | 350 |
| 19 | VDD | -2867 | -385 | 99 | D2 | 2627 | -385 | 179 | COM8 | 2128 | 350 |
| 20 | VDD | -2807 | -385 | 100 | D3 | 2687 | -385 | 180 | COM7 | 2100 | 350 |
| 21 | VCI | -2747 | -385 | 101 | D4 | 2747 | -385 | 181 | COM6 | 2072 | 350 |
| 22 | BS0 | -2687 | -385 | 102 | D5 | 2807 | -385 | 182 | COM5 | 2044 | 350 |
| 23 | VSS | -2627 | -385 | 103 | D6 | 2867 | -385 | 183 | COM4 | 2016 | 350 |
| 24 | BS1 | -2567 | -385 | 104 | D7 | 2927 | -385 | 184 | COM3 | 1988 | 350 |
| 25 | VCI | -2507 | -385 | 105 | VSS | 2987 | -385 | 185 | COM2 | 1960 | 350 |
| 26 | BS2 | -2447 | -385 | 106 | NC | 3047 | -385 | 186 | COM1 | 1932 | 350 |
| 27 | VSS | -2387 | -385 | 107 | CLS | 3107 | -385 | 187 | COM0 | 1904 | 350 |
| 28 | VLSS | -2327 | -385 | 108 | VCI | 3167 | -385 | 188 | VCC | 1869 | 390 |
| 29 | VLSS | -2060 | -420 | 109 | VCI | 3227 | -385 | 189 | VCC | 1841 | 390 |
| 30 | VLSS | -1995 | -420 | 110 | VDD | 3287 | -385 | 190 | VCC | 1813 | 390 |
| 31 | VLSS | -1930 | -420 | 111 | VDD | 3347 | -385 | 191 | SEG0 | 1778 | 390 |
| 32 | VLSS | -1865 | -420 | 112 | VCOMH | 3407 | -385 | 192 | SEG1 | 1750 | 390 |
| 33 | VLSS | -1800 | -420 | 113 | VCOMH | 3467 | -385 | 193 | SEG2 | 1722 | 390 |
| 34 | VLSS | -1735 | -420 | 114 | VCC | 3527 | -385 | 194 | SEG3 | 1694 | 390 |
| 35 | VLSS | -1670 | -420 | 115 | VCC | 3587 | -385 | 195 | SEG4 | 1666 | 390 |
| 36 | VLSS | -1605 | -420 | 116 | VCC | 3647 | -385 | 196 | SEG5 | 1638 | 390 |
| 37 | VLSS | -1540 | -420 | 117 | NC | 3707 | -385 | 197 | SEG6 | 1610 | 390 |
| 38 | VLSS | -1475 | -420 | 118 | VSS | 3767 | -385 | 198 | SEG7 | 1582 | 390 |
| 39 | VLSS | -1410 | -420 | 119 | VSS | 3827 | -385 | 199 | SEG8 | 1554 | 390 |
| 40 | VLSS | -1345 | -420 | 120 | VSS | 3887 | -385 | 200 | SEG9 | 1526 | 390 |
| 41 | VLSS | -1280 | -420 | 121 | NC | 3947 | -385 | 201 | SEG10 | 1498 | 390 |
| 42 | VLSS | -1215 | -420 | 122 | NC | 3724 | 350 | 202 | SEG11 | 1470 | 390 |
| 43 | VLSS | -1150 | -420 | 123 | NC | 3696 | 350 | 203 | SEG12 | 1442 | 390 |
| 44 | VLSS | -1085 | -420 | 124 | COM63 | 3668 | 350 | 204 | SEG13 | 1414 | 390 |
| 45 | VLSS | -1020 | -420 | 125 | COM62 | 3640 | 350 | 205 | SEG14 | 1386 | 390 |
| 46 | VLSS | -955 | -420 | 126 | COM61 | 3612 | 350 | 206 | SEG15 | 1358 | 390 |
| 47 | VLSS | -890 | -420 | 127 | COM60 | 3584 | 350 | 207 | SEG16 | 1330 | 390 |
| 48 | VLSS | -825 | -420 | 128 | COM59 | 3556 | 350 | 208 | SEG17 | 1302 | 390 |
| 49 | VLSS | -760 | -420 | 129 | COM58 | 3528 | 350 | 209 | SEG18 | 1274 | 390 |
| 50 | VLSS | -695 | -420 | 130 | COM57 | 3500 | 350 | 210 | SEG19 | 1246 | 390 |
| 51 | VLSS | -630 | -420 | 131 | COM56 | 3472 | 350 | 211 | SEG20 | 1218 | 390 |
| 52 | VLSS | -565 | -420 | 132 | COM55 | 3444 | 350 | 212 | SEG21 | 1190 | 390 |
| 53 | VLSS | -500 | -420 | 133 | COM54 | 3416 | 350 | 213 | SEG22 | 1162 | 390 |
| 54 | VLSS | -435 | -420 | 134 | COM53 | 3388 | 350 | 214 | SEG23 | 1134 | 390 |
| 55 | VLSS | -370 | -420 | 135 | COM52 | 3360 | 350 | 215 | SEG24 | 1106 | 390 |
| 56 | VLSS | -305 | -420 | 136 | COM51 | 3332 | 350 | 216 | SEG25 | 1078 | 390 |
| 57 | VLSS | -240 | -420 | 137 | COM50 | 3304 | 350 | 217 | SEG26 | 1050 | 390 |
| 58 | VLSS | -175 | -420 | 138 | COM49 | 3276 | 350 | 218 | SEG27 | 1022 | 390 |
| 59 | VLSS | -110 | -420 | 139 | COM48 | 3248 | 350 | 219 | SEG28 | 994 | 390 |
| 60 | VLSS | -45 | -420 | 140 | COM47 | 3220 | 350 | 220 | SEG29 | 966 | 390 |
| 61 | VLSS | 20 | -420 | 141 | COM46 | 3192 | 350 | 221 | SEG30 | 938 | 390 |
| 62 | VLSS | 85 | -420 | 142 | COM45 | 3164 | 350 | 222 | SEG31 | 910 | 390 |
| 63 | VLSS | 150 | -420 | 143 | COM44 | 3136 | 350 | 223 | SEG32 | 882 | 390 |
| 64 | VLSS | 215 | -420 | 144 | COM43 | 3108 | 350 | 224 | SEG33 | 854 | 390 |
| 65 | VLSS | 280 | -420 | 145 | COM42 | 3080 | 350 | 225 | SEG34 | 826 | 390 |
| 66 | VLSS | 345 | -420 | 146 | COM41 | 3052 | 350 | 226 | SEG35 | 798 | 390 |
| 67 | VLSS | 410 | -420 | 147 | COM40 | 3024 | 350 | 227 | SEG36 | 770 | 390 |
| 68 | VLSS | 475 | -420 | 148 | COM39 | 2996 | 350 | 228 | SEG37 | 742 | 390 |
| 69 | VLSS | 540 | -420 | 149 | COM38 | 2968 | 350 | 229 | SEG38 | 714 | 390 |
| 70 | VLSS | 605 | -420 | 150 | COM37 | 2940 | 350 | 230 | SEG39 | 686 | 390 |
| 71 | VLSS | 670 | -420 | 151 | COM36 | 2912 | 350 | 231 | SEG40 | 658 | 390 |
| 72 | VLSS | 735 | -420 | 152 | COM35 | 2884 | 350 | 232 | SEG41 | 630 | 390 |
| 73 | VLSS | 800 | -420 | 153 | COM34 | 2856 | 350 | 233 | SEG42 | 602 | 390 |
| 74 | VLSS | 865 | -420 | 154 | COM33 | 2828 | 350 | 234 | SEG43 | 574 | 390 |
| 75 | VLSS | 930 | -420 | 155 | COM32 | 2800 | 350 | 235 | SEG44 | 546 | 390 |
| 76 | VLSS | 995 | -420 | 156 | COM31 | 2772 | 350 | 236 | SEG45 | 518 | 390 |
| 77 | VLSS | 1060 | -420 | 157 | COM30 | 2744 | 350 | 237 | SEG46 | 490 | 390 |
| 78 | VLSS | 1125 | -420 | 158 | COM29 | 2716 | 350 | 238 | SEG47 | 462 | 390 |
| 79 | VLSS | 1190 | -420 | 159 | COM28 | 2688 | 350 | 239 | SEG48 | 434 | 390 |
| 80 | VLSS | 1255 | -420 | 160 | COM27 | 2660 | 350 | 240 | SEG49 | 406 | 390 |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|-------|
| 241 | SEG50 | 378 | 390 |
| 242 | SEG51 | 350 | 390 |
| 243 | SEG52 | 322 | 390 |
| 244 | SEG53 | 294 | 390 |
| 245 | SEG54 | 266 | 390 |
| 246 | SEG55 | 238 | 390 |
| 247 | SEG56 | 210 | 390 |
| 248 | SEG57 | 182 | 390 |
| 249 | SEG58 | 154 | 390 |
| 250 | SEG59 | 126 | 390 |
| 251 | SEG60 | 98 | 390 |
| 252 | SEG61 | 70 | 390 |
| 253 | SEG62 | 42 | 390 |
| 254 | SEG63 | 14 | 390 |
| 255 | SEG64 | -14 | 390 |
| 256 | SEG65 | -42 | 390 |
| 257 | SEG66 | -70 | 390 |
| 258 | SEG67 | -98 | 390 |
| 259 | SEG68 | -126 | 390 |
| 260 | SEG69 | -154 | 390 |
| 261 | SEG70 | -182 | 390 |
| 262 | SEG71 | -210 | 390 |
| 263 | SEG72 | -238 | 390 |
| 264 | SEG73 | -266 | 390 |
| 265 | SEG74 | -294 | 390 |
| 266 | SEG75 | -322 | 390 |
| 267 | SEG76 | -350 | 390 |
| 268 | SEG77 | -378 | 390 |
| 269 | SEG78 | -406 | 390 |
| 270 | SEG79 | -434 | 390 |
| 271 | SEG80 | -462 | 390 |
| 272 | SEG81 | -490 | 390 |
| 273 | SEG82 | -518 | 390 |
| 274 | SEG83 | -546 | 390 |
| 275 | SEG84 | -574 | 390 |
| 276 | SEG85 | -602 | 390 |
| 277 | SEG86 | -630 | 390 |
| 278 | SEG87 | -658 | 390 |
| 279 | SEG88 | -686 | 390 |
| 280 | SEG89 | -714 | 390 |
| 281 | SEG90 | -742 | 390 |
| 282 | SEG91 | -770 | 390 |
| 283 | SEG92 | -798 | 390 |
| 284 | SEG93 | -826 | 390 |
| 285 | SEG94 | -854 | 390 |
| 286 | SEG95 | -882 | 390 |
| 287 | SEG96 | -910 | 390 |
| 288 | SEG97 | -938 | 390 |
| 289 | SEG98 | -966 | 390 |
| 290 | SEG99 | -994 | 390 |
| 291 | SEG100 | -1022 | 390 |
| 292 | SEG101 | -1050 | 390 |
| 293 | SEG102 | -1078 | 390 |
| 294 | SEG103 | -1106 | 390 |
| 295 | SEG104 | -1134 | 390 |
| 296 | SEG105 | -1162 | 390 |
| 297 | SEG106 | -1190 | 390 |
| 298 | SEG107 | -1218 | 390 |
| 299 | SEG108 | -1246 | 390 |
| 300 | SEG109 | -1274 | 390 |
| 301 | SEG110 | -1302 | 390 |
| 302 | SEG111 | -1330 | 390 |
| 303 | SEG112 | -1358 | 390 |
| 304 | SEG113 | -1386 | 390 |
| 305 | SEG114 | -1414 | 390 |
| 306 | SEG115 | -1442 | 390 |
| 307 | SEG116 | -1470 | 390 |
| 308 | SEG117 | -1498 | 390 |
| 309 | SEG118 | -1526 | 390 |
| 310 | SEG119 | -1554 | 390 |
| 311 | SEG120 | -1582 | 390 |
| 312 | SEG121 | -1610 | 390 |
| 313 | SEG122 | -1638 | 390 |
| 314 | SEG123 | -1666 | 390 |
| 315 | SEG124 | -1694 | 390 |
| 316 | SEG125 | -1722 | 390 |
| 317 | SEG126 | -1750 | 390 |
| 318 | SEG127 | -1778 | 390 |
| 319 | VCC | -1813 | 390 |
| 320 | VCC | -1841 | 390 |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|-------|
| 321 | VCC | -1869 | 390 |
| 322 | COM64 | -1904 | 350 |
| 323 | COM65 | -1932 | 350 |
| 324 | COM66 | -1960 | 350 |
| 325 | COM67 | -1988 | 350 |
| 326 | COM68 | -2016 | 350 |
| 327 | COM69 | -2044 | 350 |
| 328 | COM70 | -2072 | 350 |
| 329 | COM71 | -2100 | 350 |
| 330 | COM72 | -2128 | 350 |
| 331 | COM73 | -2156 | 350 |
| 332 | COM74 | -2184 | 350 |
| 333 | COM75 | -2212 | 350 |
| 334 | COM76 | -2240 | 350 |
| 335 | COM77 | -2268 | 350 |
| 336 | COM78 | -2296 | 350 |
| 337 | COM79 | -2324 | 350 |
| 338 | COM80 | -2352 | 350 |
| 339 | COM81 | -2380 | 350 |
| 340 | COM82 | -2408 | 350 |
| 341 | COM83 | -2436 | 350 |
| 342 | COM84 | -2464 | 350 |
| 343 | COM85 | -2492 | 350 |
| 344 | COM86 | -2520 | 350 |
| 345 | COM87 | -2548 | 350 |
| 346 | COM88 | -2576 | 350 |
| 347 | COM89 | -2604 | 350 |
| 348 | COM90 | -2632 | 350 |
| 349 | COM91 | -2660 | 350 |
| 350 | COM92 | -2688 | 350 |
| 351 | COM93 | -2716 | 350 |
| 352 | COM94 | -2744 | 350 |
| 353 | COM95 | -2772 | 350 |
| 354 | COM96 | -2800 | 350 |
| 355 | COM97 | -2828 | 350 |
| 356 | COM98 | -2856 | 350 |
| 357 | COM99 | -2884 | 350 |
| 358 | COM100 | -2912 | 350 |
| 359 | COM101 | -2940 | 350 |
| 360 | COM102 | -2968 | 350 |
| 361 | COM103 | -2996 | 350 |
| 362 | COM104 | -3024 | 350 |
| 363 | COM105 | -3052 | 350 |
| 364 | COM106 | -3080 | 350 |
| 365 | COM107 | -3108 | 350 |
| 366 | COM108 | -3136 | 350 |
| 367 | COM109 | -3164 | 350 |
| 368 | COM110 | -3192 | 350 |
| 369 | COM111 | -3220 | 350 |
| 370 | COM112 | -3248 | 350 |
| 371 | COM113 | -3276 | 350 |
| 372 | COM114 | -3304 | 350 |
| 373 | COM115 | -3332 | 350 |
| 374 | COM116 | -3360 | 350 |
| 375 | COM117 | -3388 | 350 |
| 376 | COM118 | -3416 | 350 |
| 377 | COM119 | -3444 | 350 |
| 378 | COM120 | -3472 | 350 |
| 379 | COM121 | -3500 | 350 |
| 380 | COM122 | -3528 | 350 |
| 381 | COM123 | -3556 | 350 |
| 382 | COM124 | -3584 | 350 |
| 383 | COM125 | -3612 | 350 |
| 384 | COM126 | -3640 | 350 |
| 385 | COM127 | -3668 | 350 |
| 386 | NC | -3696 | 350 |
| 387 | NC | -3724 | 350 |
| 388 | TR6 | -3089 | 25 |
| 389 | TR5 | -3029 | 25 |
| 390 | TR4 | -2969 | 25 |
| 391 | VSS | -2909 | 25 |
| 392 | TR3 | -2849 | 25 |
| 393 | TR2 | -2789 | 25 |
| 394 | TR1 | -2729 | 25 |
| 395 | TR0 | -2669 | 25 |

6 PIN ARRANGEMENT

Figure 6-1: SSD1327UR1 Pin Assignment

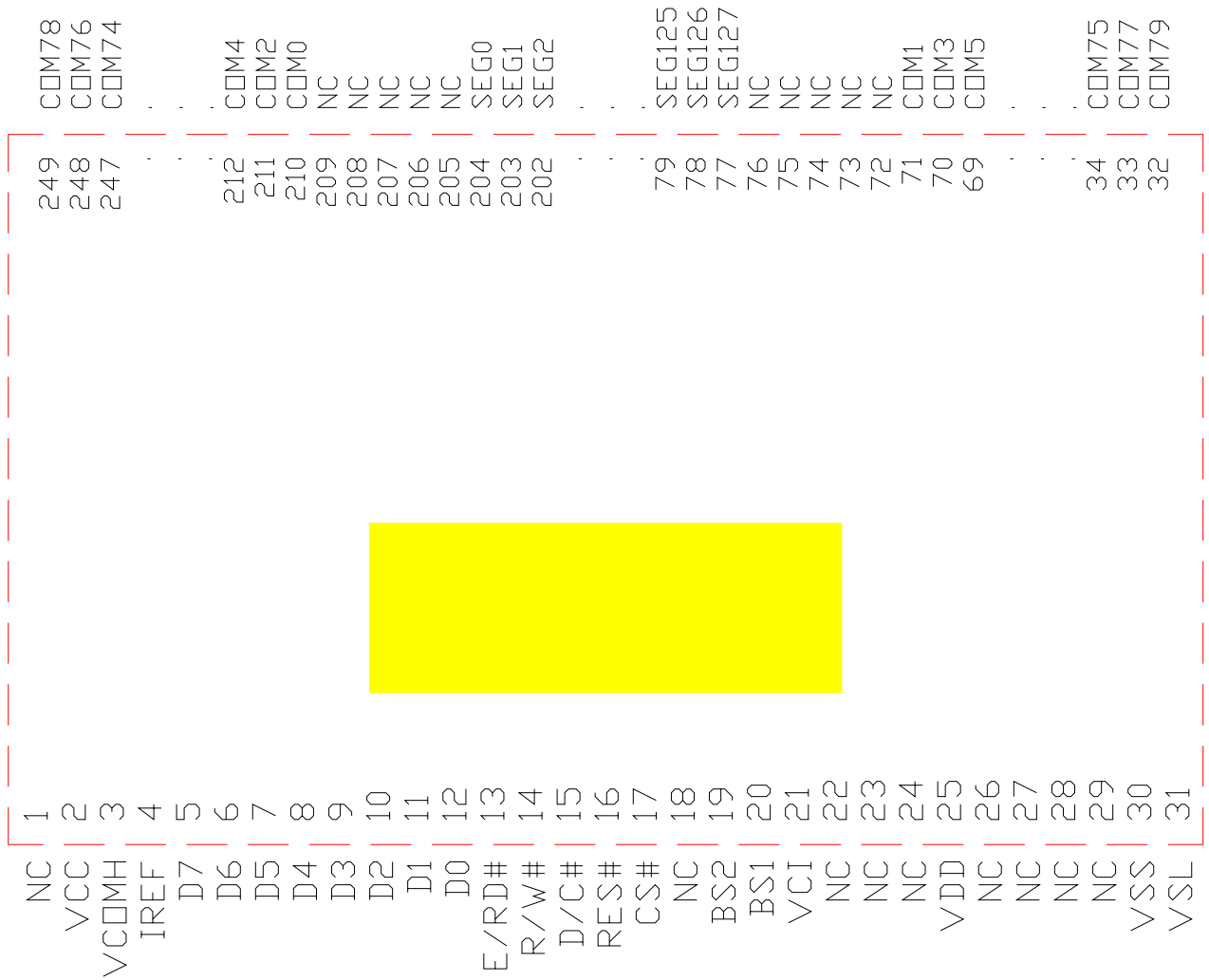


Table 6-1: SSD1327UR1 Pin Assignment Table

| PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | NC | 81 | SEG123 | 161 | SEG43 | 241 | COM62 |
| 2 | VCC | 82 | SEG122 | 162 | SEG42 | 242 | COM64 |
| 3 | VCOMH | 83 | SEG121 | 163 | SEG41 | 243 | COM66 |
| 4 | IREF | 84 | SEG120 | 164 | SEG40 | 244 | COM68 |
| 5 | D7 | 85 | SEG119 | 165 | SEG39 | 245 | COM70 |
| 6 | D6 | 86 | SEG118 | 166 | SEG38 | 246 | COM72 |
| 7 | D5 | 87 | SEG117 | 167 | SEG37 | 247 | COM74 |
| 8 | D4 | 88 | SEG116 | 168 | SEG36 | 248 | COM76 |
| 9 | D3 | 89 | SEG115 | 169 | SEG35 | 249 | COM78 |
| 10 | D2 | 90 | SEG114 | 170 | SEG34 | | |
| 11 | D1 | 91 | SEG113 | 171 | SEG33 | | |
| 12 | D0 | 92 | SEG112 | 172 | SEG32 | | |
| 13 | E/RD# | 93 | SEG111 | 173 | SEG31 | | |
| 14 | R/W# | 94 | SEG110 | 174 | SEG30 | | |
| 15 | D/C# | 95 | SEG109 | 175 | SEG29 | | |
| 16 | RES# | 96 | SEG108 | 176 | SEG28 | | |
| 17 | CS# | 97 | SEG107 | 177 | SEG27 | | |
| 18 | NC | 98 | SEG106 | 178 | SEG26 | | |
| 19 | BS2 | 99 | SEG105 | 179 | SEG25 | | |
| 20 | BS1 | 100 | SEG104 | 180 | SEG24 | | |
| 21 | VCI | 101 | SEG103 | 181 | SEG23 | | |
| 22 | NC | 102 | SEG102 | 182 | SEG22 | | |
| 23 | NC | 103 | SEG101 | 183 | SEG21 | | |
| 24 | NC | 104 | SEG100 | 184 | SEG20 | | |
| 25 | VDD | 105 | SEG99 | 185 | SEG19 | | |
| 26 | NC | 106 | SEG98 | 186 | SEG18 | | |
| 27 | NC | 107 | SEG97 | 187 | SEG17 | | |
| 28 | NC | 108 | SEG96 | 188 | SEG16 | | |
| 29 | NC | 109 | SEG95 | 189 | SEG15 | | |
| 30 | VSS | 110 | SEG94 | 190 | SEG14 | | |
| 31 | VSL | 111 | SEG93 | 191 | SEG13 | | |
| 32 | COM79 | 112 | SEG92 | 192 | SEG12 | | |
| 33 | COM77 | 113 | SEG91 | 193 | SEG11 | | |
| 34 | COM75 | 114 | SEG90 | 194 | SEG10 | | |
| 35 | COM73 | 115 | SEG89 | 195 | SEG9 | | |
| 36 | COM71 | 116 | SEG88 | 196 | SEG8 | | |
| 37 | COM69 | 117 | SEG87 | 197 | SEG7 | | |
| 38 | COM67 | 118 | SEG86 | 198 | SEG6 | | |
| 39 | COM65 | 119 | SEG85 | 199 | SEG5 | | |
| 40 | COM63 | 120 | SEG84 | 200 | SEG4 | | |
| 41 | COM61 | 121 | SEG83 | 201 | SEG3 | | |
| 42 | COM59 | 122 | SEG82 | 202 | SEG2 | | |
| 43 | COM57 | 123 | SEG81 | 203 | SEG1 | | |
| 44 | COM55 | 124 | SEG80 | 204 | SEG0 | | |
| 45 | COM53 | 125 | SEG79 | 205 | NC | | |
| 46 | COM51 | 126 | SEG78 | 206 | NC | | |
| 47 | COM49 | 127 | SEG77 | 207 | NC | | |
| 48 | COM47 | 128 | SEG76 | 208 | NC | | |
| 49 | COM45 | 129 | SEG75 | 209 | NC | | |
| 50 | COM43 | 130 | SEG74 | 210 | COM0 | | |
| 51 | COM41 | 131 | SEG73 | 211 | COM2 | | |
| 52 | COM39 | 132 | SEG72 | 212 | COM4 | | |
| 53 | COM37 | 133 | SEG71 | 213 | COM6 | | |
| 54 | COM35 | 134 | SEG70 | 214 | COM8 | | |
| 55 | COM33 | 135 | SEG69 | 215 | COM10 | | |
| 56 | COM31 | 136 | SEG68 | 216 | COM12 | | |
| 57 | COM29 | 137 | SEG67 | 217 | COM14 | | |
| 58 | COM27 | 138 | SEG66 | 218 | COM16 | | |
| 59 | COM25 | 139 | SEG65 | 219 | COM18 | | |
| 60 | COM23 | 140 | SEG64 | 220 | COM20 | | |
| 61 | COM21 | 141 | SEG63 | 221 | COM22 | | |
| 62 | COM19 | 142 | SEG62 | 222 | COM24 | | |
| 63 | COM17 | 143 | SEG61 | 223 | COM26 | | |
| 64 | COM15 | 144 | SEG60 | 224 | COM28 | | |
| 65 | COM13 | 145 | SEG59 | 225 | COM30 | | |
| 66 | COM11 | 146 | SEG58 | 226 | COM32 | | |
| 67 | COM9 | 147 | SEG57 | 227 | COM34 | | |
| 68 | COM7 | 148 | SEG56 | 228 | COM36 | | |
| 69 | COM5 | 149 | SEG55 | 229 | COM38 | | |
| 70 | COM3 | 150 | SEG54 | 230 | COM40 | | |
| 71 | COM1 | 151 | SEG53 | 231 | COM42 | | |
| 72 | NC | 152 | SEG52 | 232 | COM44 | | |
| 73 | NC | 153 | SEG51 | 233 | COM46 | | |
| 74 | NC | 154 | SEG50 | 234 | COM48 | | |
| 75 | NC | 155 | SEG49 | 235 | COM50 | | |
| 76 | NC | 156 | SEG48 | 236 | COM52 | | |
| 77 | SEG127 | 157 | SEG47 | 237 | COM54 | | |
| 78 | SEG126 | 158 | SEG46 | 238 | COM56 | | |
| 79 | SEG125 | 159 | SEG45 | 239 | COM58 | | |
| 80 | SEG124 | 160 | SEG44 | 240 | COM60 | | |

7 PIN DESCRIPTIONS

Key:

| | |
|-------------------------------------|---------------------------------------|
| I = Input | NC = Not Connected |
| O = Output | Pull LOW= connect to Ground |
| I/O = Bi-directional (input/output) | Pull HIGH= connect to V _{CI} |
| P = Power pin | |

Table 7-1 : SSD1327 Pin Description

| Pin Name | Pin Type | Description | | | | | | | | | | | | |
|-------------------|---------------------|--|---------|-----------|-----|------------|-----|------------|-----|------------------|-----|---------------------|-----|---------------------|
| V _{DD} | P | Power supply pin for core logic operation. V _{DD} can be supplied externally (within the range of 2.4V to 2.6V) or regulated internally from V _{CI} . A capacitor should be connected between V _{DD} and V _{SS} under all circumstances. | | | | | | | | | | | | |
| V _{CI} | P | Low voltage power supply and power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source. V _{CI} must always set to be equivalent to or higher than V _{DD} . | | | | | | | | | | | | |
| V _{CC} | P | Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source. | | | | | | | | | | | | |
| V _{SS} | P | Ground pin. It must be connected to external ground. | | | | | | | | | | | | |
| V _{LSS} | P | Analog system ground pin. It must be connected to external ground. | | | | | | | | | | | | |
| V _{COMH} | P | COM signal deselected voltage level. A capacitor should be connected between this pin and V _{SS} . No external power supply is allowed to connect to this pin. | | | | | | | | | | | | |
| BGGND | P | It is a reserved pin. It should be connected to Ground. | | | | | | | | | | | | |
| GPIO | I/O | It is a GPIO pin. Details refer to command B5h. | | | | | | | | | | | | |
| VSL | P | This is segment voltage (output low level) reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, connect with resistor and diode to ground (details depends on application). Note (1) Refer to Table 9-1 Command D5h for details. | | | | | | | | | | | | |
| BS[2:0] | I | MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. Table 7-2 : Bus Interface selection <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BS[2:0]</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>4 line SPI</td> </tr> <tr> <td>001</td> <td>3 line SPI</td> </tr> <tr> <td>010</td> <td>I²C</td> </tr> <tr> <td>110</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>100</td> <td>8-bit 6800 parallel</td> </tr> </tbody> </table> Note (1) 0 is connected to V _{SS} (2) 1 is connected to V _{CI} | BS[2:0] | Interface | 000 | 4 line SPI | 001 | 3 line SPI | 010 | I ² C | 110 | 8-bit 8080 parallel | 100 | 8-bit 6800 parallel |
| BS[2:0] | Interface | | | | | | | | | | | | | |
| 000 | 4 line SPI | | | | | | | | | | | | | |
| 001 | 3 line SPI | | | | | | | | | | | | | |
| 010 | I ² C | | | | | | | | | | | | | |
| 110 | 8-bit 8080 parallel | | | | | | | | | | | | | |
| 100 | 8-bit 6800 parallel | | | | | | | | | | | | | |

| Pin Name | Pin Type | Description |
|------------------|----------|---|
| I _{REF} | I | This pin is the segment output current reference pin. A resistor should be connected between this pin and V _{SS} to maintain the current around 10uA. |
| CL | I | External clock input pin. When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground. When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin. |
| CLS | I | Internal clock selection pin. When this pin is pulled HIGH, internal oscillator is enabled (normal operation). When this pin is pulled LOW, an external clock signal should be connected to CL. |
| CS# | I | This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW). |
| RES# | I | This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation. |
| D/C# | I | This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I ² C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V _{SS} . For detail relationship to MCU interface signals, please refer to Table 8-1 |
| R/W# (WR#) | I | This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I ² C interface is selected, this pin must be connected to V _{SS} . |
| E (RD#) | I | This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I ² C interface is selected, this pin must be connected to V _{SS} . |

| Pin Name | Pin Type | Description |
|-----------------|-----------------|--|
| D[7:0] | I/O | <p>These pins are bi-directional data bus connecting to the MCU data bus.</p> <p>Unused pins are recommended to tie LOW.</p> <p>When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.</p> <p>When I²C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.</p> |
| FR | O | <p>This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.</p> |
| TR[6:0] | - | Reserved pin and must be kept float. |
| SEG0 ~ SEG127 | O | These pins provide the OLED segment driving signals. These pins are V _{SS} state when display is OFF. |
| COM0 ~ COM127 | I/O | These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF. |

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1327 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-2 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

| Pin Name Bus Interface | Data/Command Interface | | | | | | | | Control Signal | | | | |
|---------------------------|------------------------|----|----|----|--------------------|-------------------|------|---------|----------------|------|---------|------|------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E | R/W# | CS# | D/C# | RES# |
| 8-bit 8080 | D[7:0] | | | | | | | | RD# | WR# | CS# | D/C# | RES# |
| 8-bit 6800 | D[7:0] | | | | | | | | E | R/W# | CS# | D/C# | RES# |
| 3-wire SPI | Tie LOW | | | | NC | SDIN | SCLK | Tie LOW | | CS# | Tie LOW | RES# | |
| 4-wire SPI | Tie LOW | | | | NC | SDIN | SCLK | Tie LOW | | CS# | D/C# | RES# | |
| I ² C | Tie LOW | | | | SDA _{OUT} | SDA _{IN} | SCL | Tie LOW | | | SA0 | RES# | |

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-2 : Control pins of 6800 interface

| Function | E | R/W# | CS# | D/C# |
|---------------|---|------|-----|------|
| Write command | ↓ | L | L | L |
| Read status | ↓ | H | L | L |
| Write data | ↓ | L | L | H |
| Read data | ↓ | H | L | H |

Note

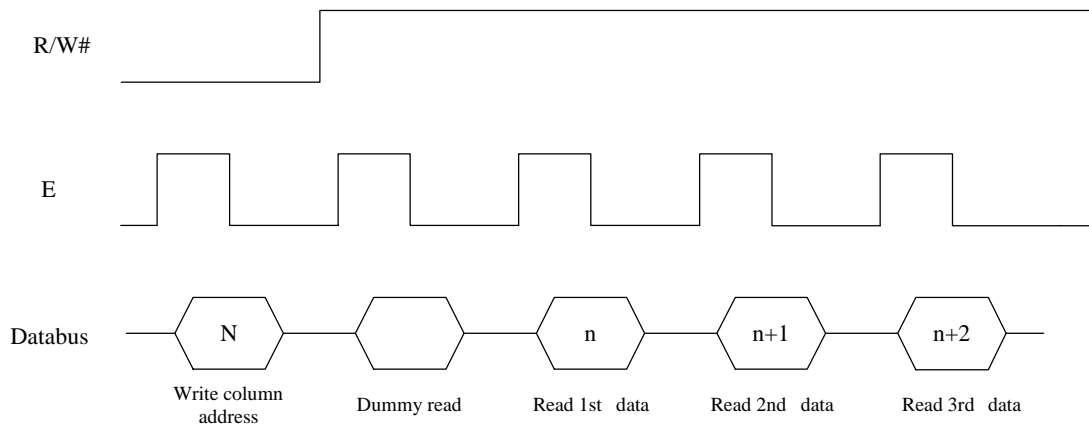
⁽¹⁾ ↓ stands for falling edge of signal

H stands for HIGH in signal

L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

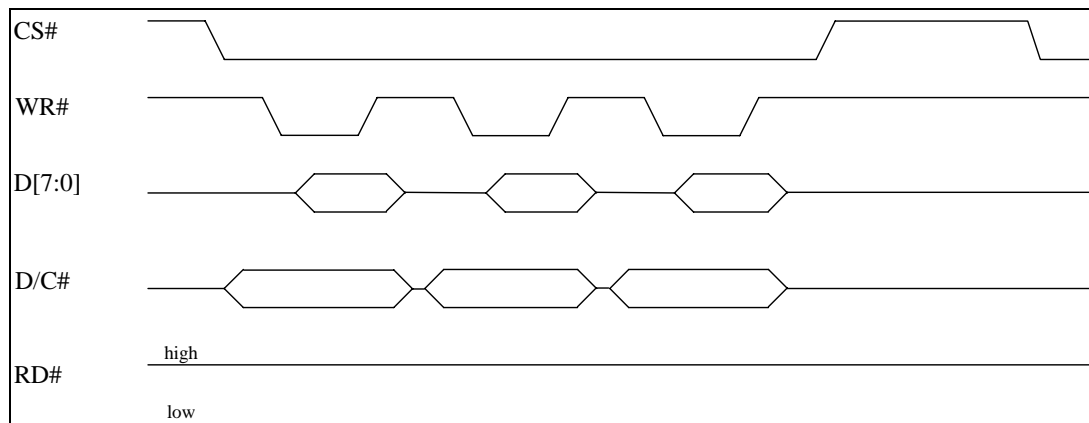


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

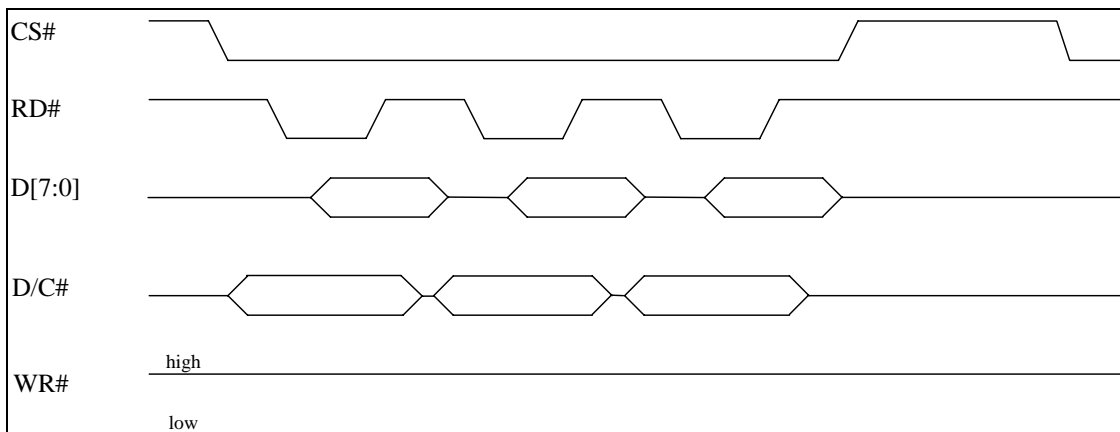


Table 8-3 : Control pins of 8080 interface

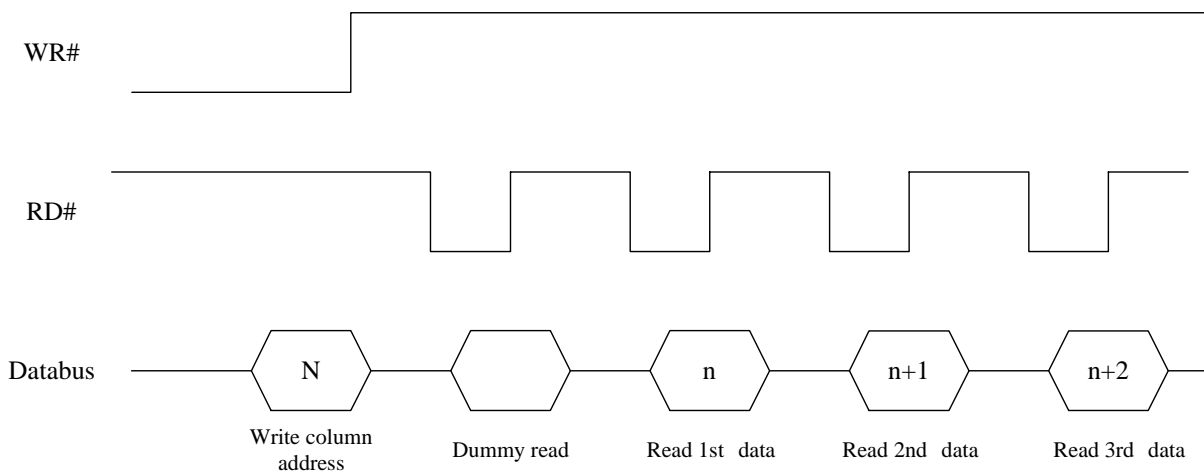
| Function | RD# | WR# | CS# | D/C# |
|---------------|-----|-----|-----|------|
| Write command | H | ↑ | L | L |
| Read status | ↑ | H | L | L |
| Write data | H | ↑ | L | H |
| Read data | ↑ | H | L | H |

Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

| Function | E(RD#) | R/W#(WR#) | CS# | D/C# | D0 |
|---------------|---------|-----------|-----|------|----|
| Write command | Tie LOW | Tie LOW | L | L | ↑ |
| Write data | Tie LOW | Tie LOW | L | H | ↑ |

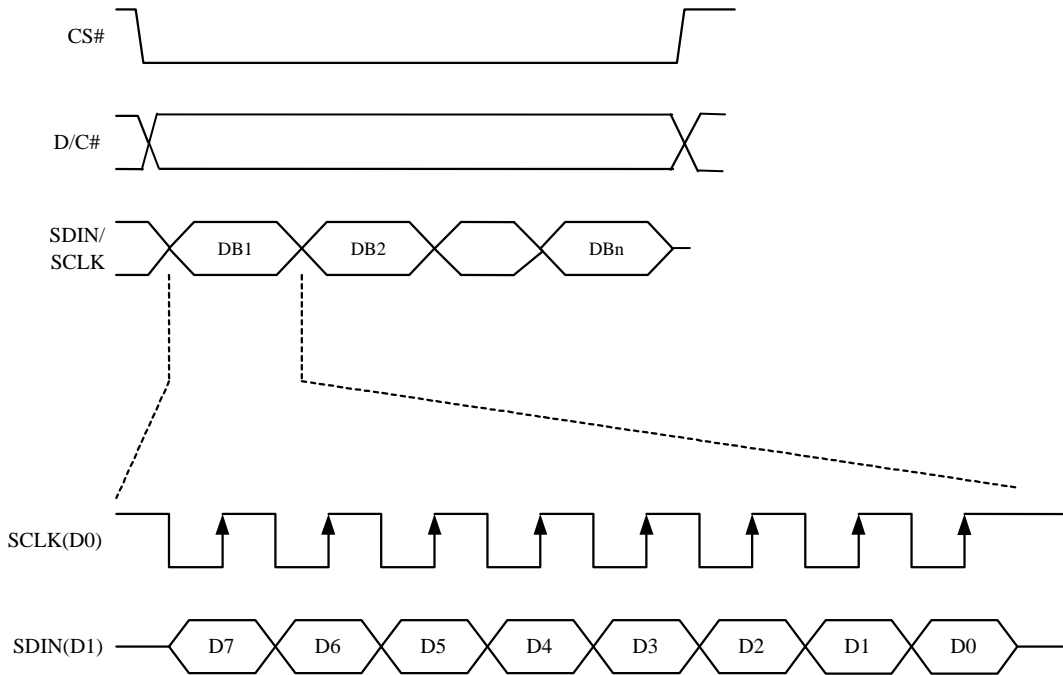
Note

- (1) H stands for HIGH in signal
- (2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

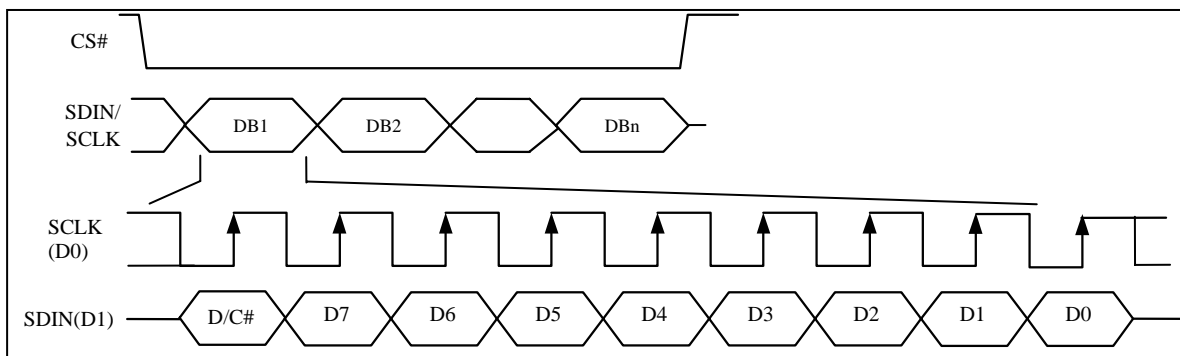
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-5: Control pins of 3-wire Serial interface

| Function | E(RD#) | R/W#(WR#) | CS# | D/C# | D0 |
|---------------|---------|-----------|-----|---------|----|
| Write command | Tie LOW | Tie LOW | L | Tie LOW | ↑ |
| Write data | Tie LOW | Tie LOW | L | Tie LOW | ↑ |

Note
⁽¹⁾ L stands for LOW in signal

Figure 8-6: Write procedure in 3-wire Serial interface mode



8.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D₂ for output and SDA_{IN}/D₁ for input) and I²C-bus clock signal SCL (D₀). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)

SSD1327 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀
0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1327. D/C# pin acts as SA0 for slave address selection.

“R/W#” bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

“SDA_{IN}” and “SDA_{OUT}” are tied together and serve as SDA. The “SDA_{IN}” pin must be connected to act as SDA. The “SDA_{OUT}” pin may be disconnected. When “SDA_{OUT}” pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

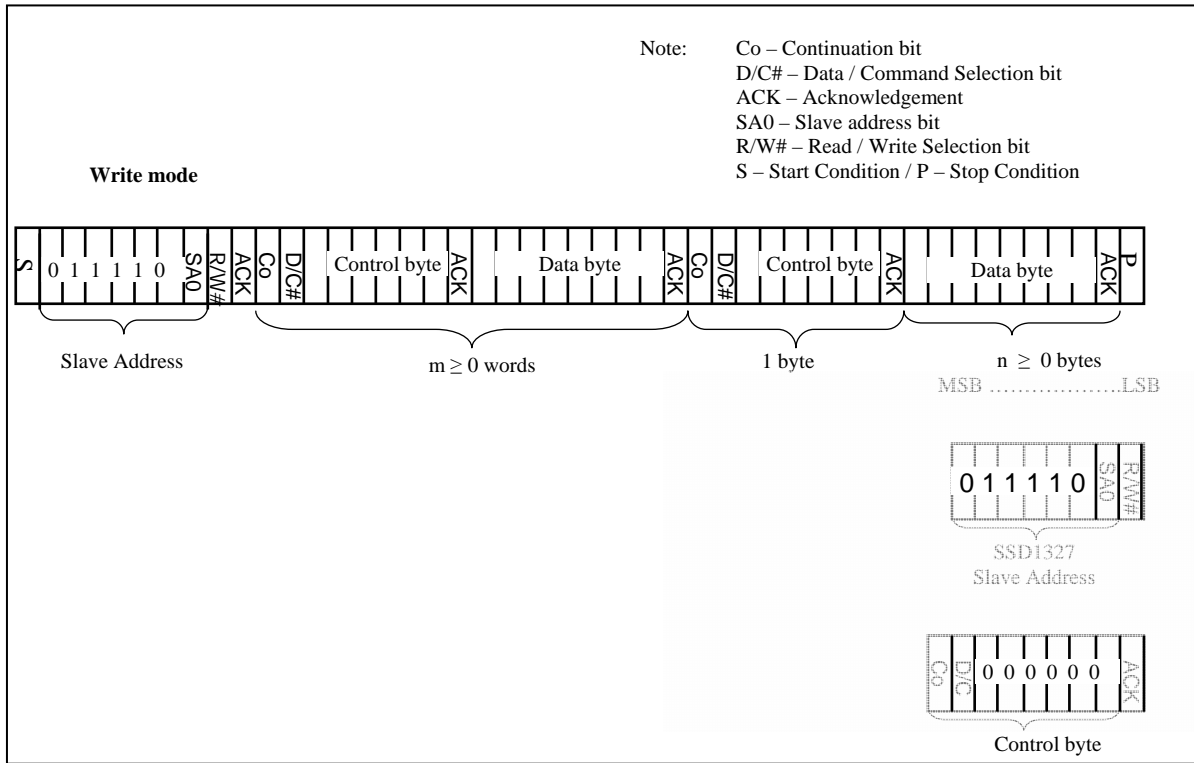
c) I²C-bus clock signal (SCL)

The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I²C-bus in chronological order.

Figure 8-7 : I²C-bus data format



8.1.5.2 Write mode for I²C

- 1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
- 2) The slave address is following the start condition for recognition use. For the SSD1327, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
- 3) The write mode is established by setting the R/W# bit to logic “0”.
- 4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
- 5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
 - a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
 - b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
- 6) Acknowledge bit will be generated after receiving each control byte or data byte.
- 7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

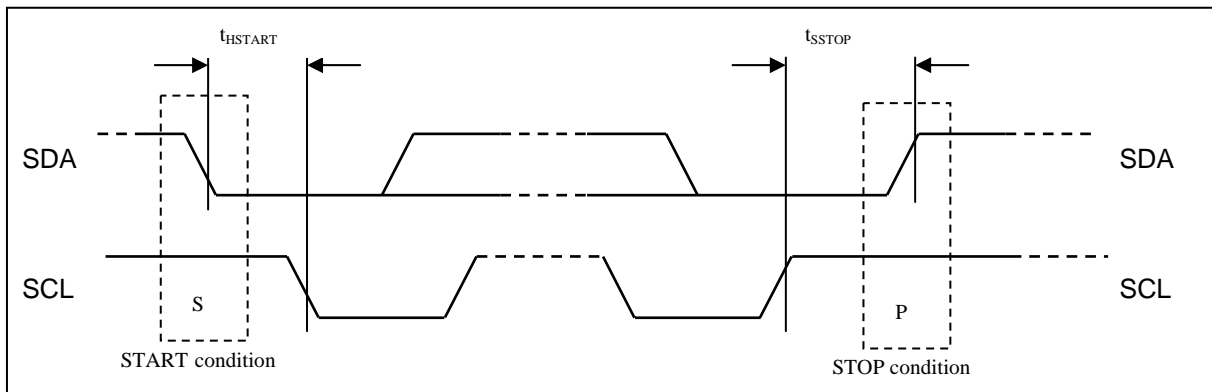
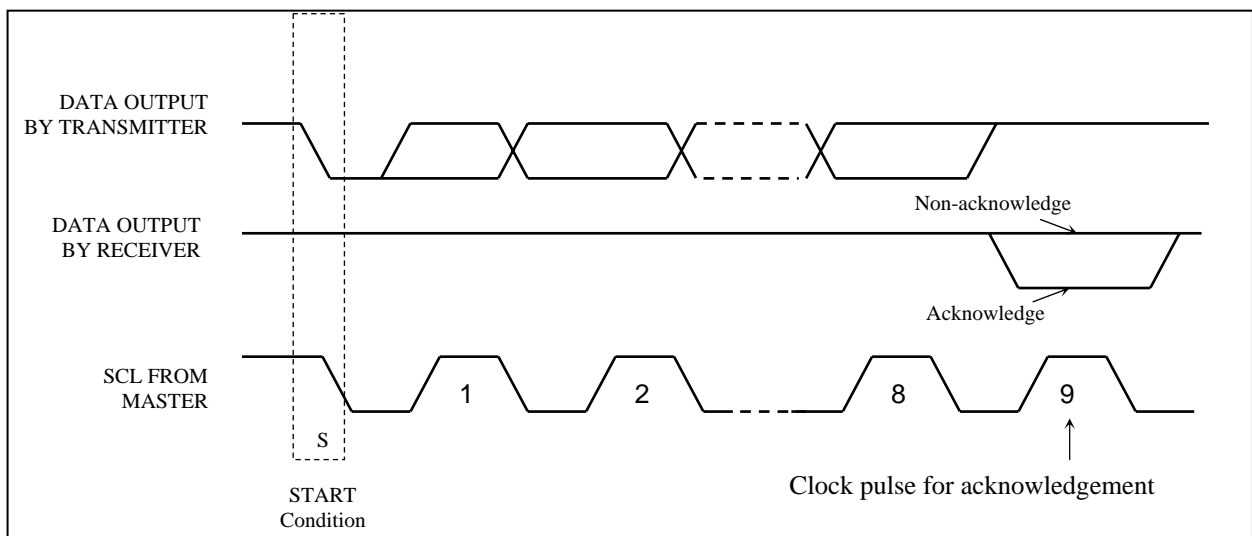


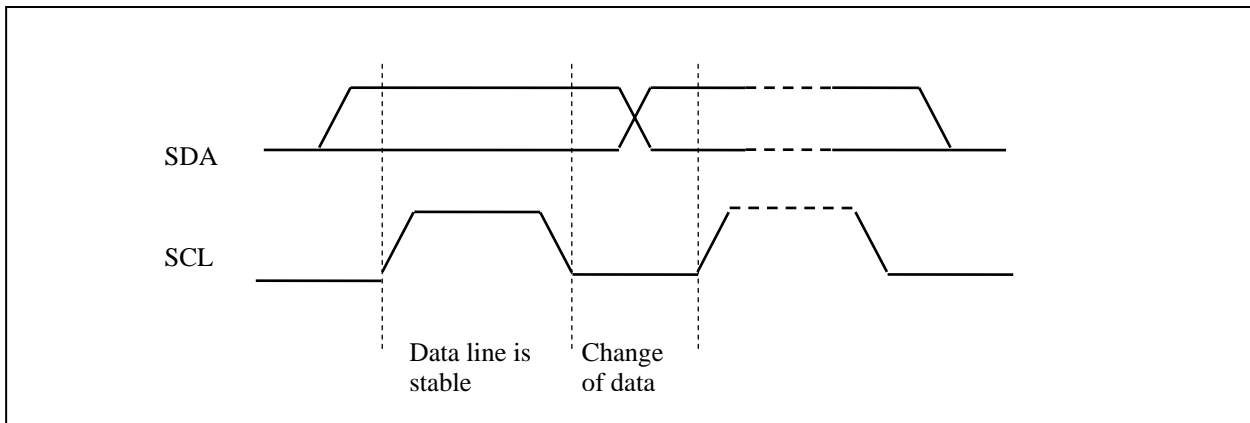
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

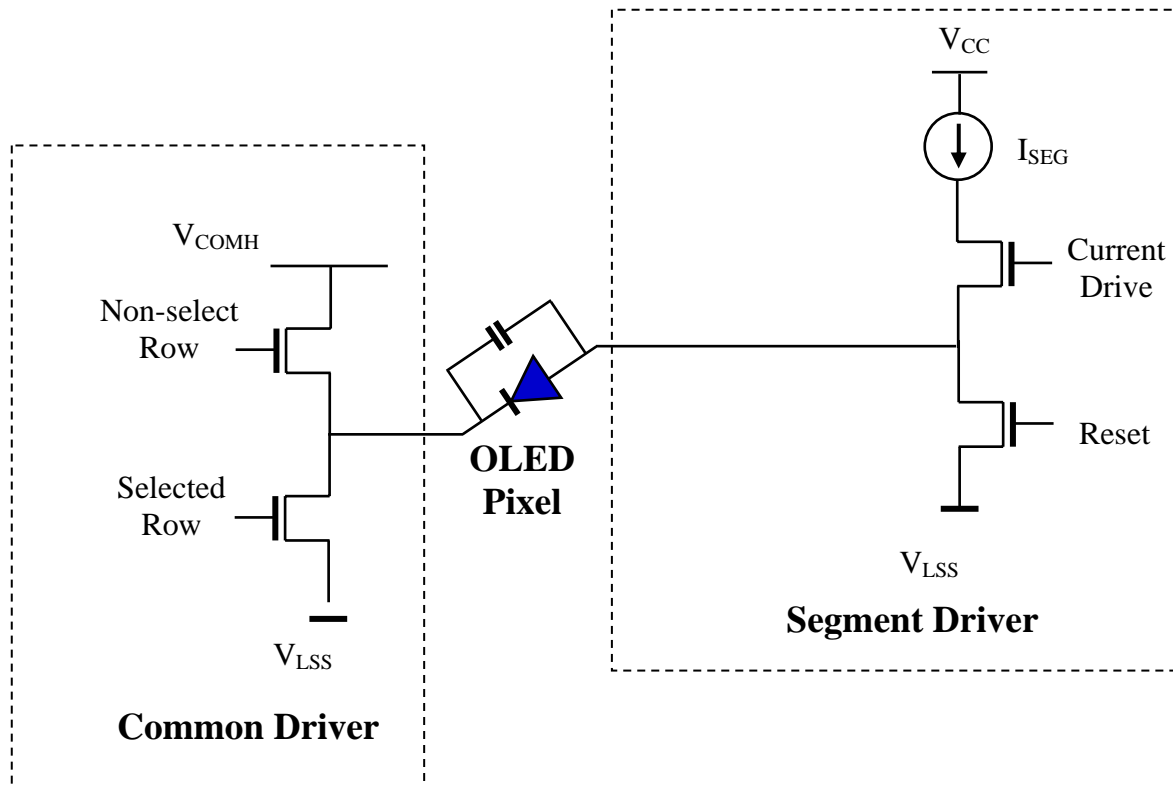
Figure 8-10 : Definition of the data transfer condition



8.2 Segment Drivers/Common Drivers

Segment drivers have 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 8 bits, 256 steps by contrast setting command (81h). Common drivers generate voltage scanning pulses. The block diagrams and waveforms of the segment and common driver are shown as follow.

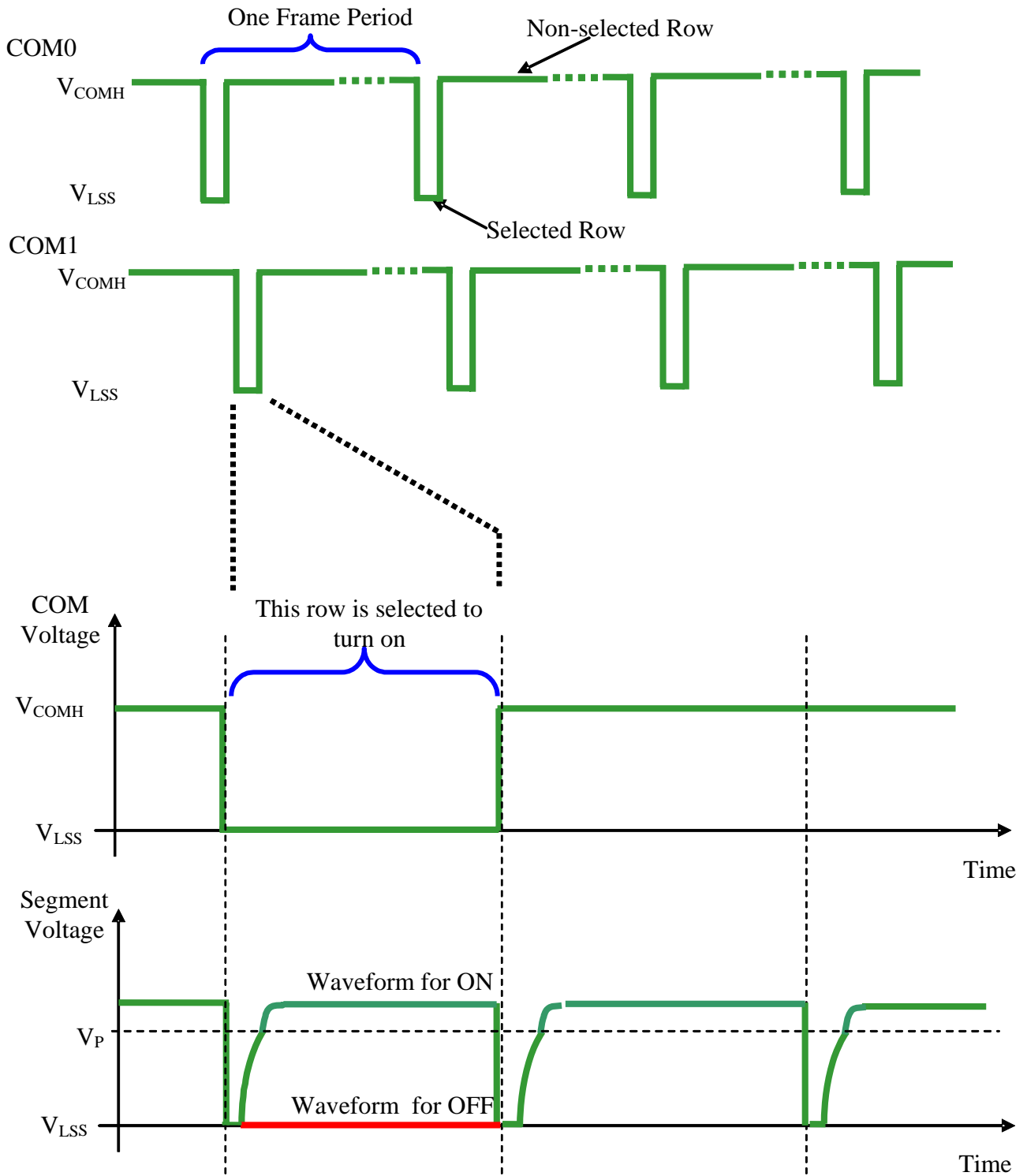
Figure 8-11: Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-12.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-12 : Segment and Common Driver Signal Waveform



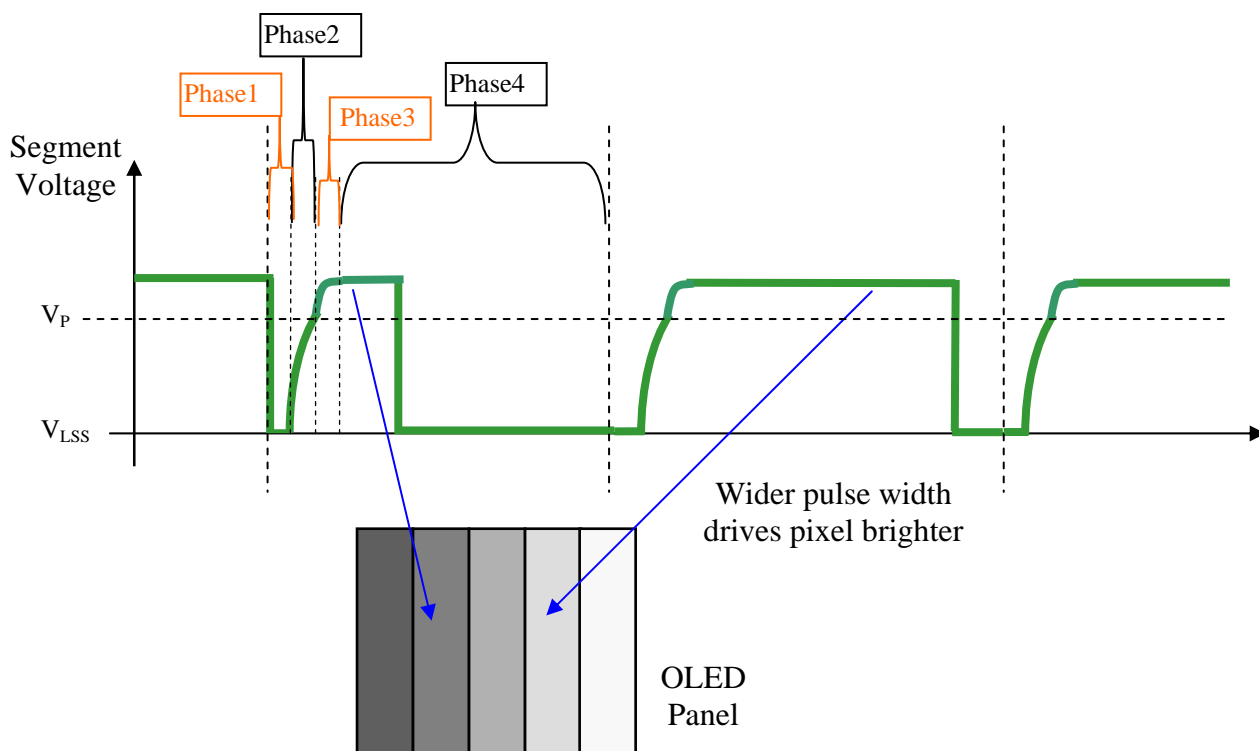
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS} . The amplitude of V_P can be programmed by the command BCh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B6h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h/B9h. The bigger gamma setting (the wider pulse widths) in the current drive stage results in brighter pixels and vice versa (details refer to Section 8.8). This is shown in the following figure.

Figure 8-13 : Gray Scale Control by PWM in Segment



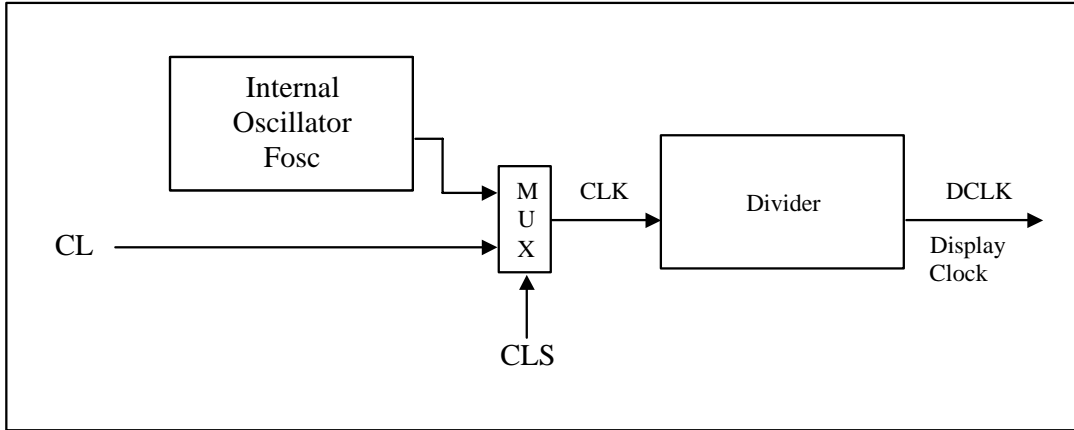
After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h or B9h. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.3 Oscillator Circuit and Display Time Generator

This module is an On-Chip low power RC oscillator circuitry (Figure 8-14). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is HIGH, internal oscillator is chosen and CL should be pulled to LOW. If CLS pin is LOW, external clock from CL pin will be used for CLK for proper operation. The frequency of internal oscillator F_{OSC} can be programmed by command B3h.

Figure 8-14: Oscillator Circuit



The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor “D” can be programmed from 1 to 16 by command B3h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
 $K = \text{Phase 1 period} + \text{Phase 2 period} + X$
 $X = \text{DCLKs in current drive period; Default } X = 30$
 Default K is $4 + 7 + 30 = 41$
- Number of multiplex ratio is set by command A8h. The reset value is 127 (i.e. 128MUX).
- F_{osc} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.4 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, the input at D₇-D₀ is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D₇-D₀ is interpreted as a Command which will be decoded and be written to the corresponding command register.

8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 128 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

8.6 SEG/COM Driving Block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

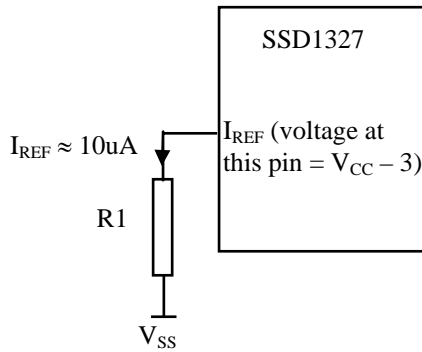
$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor}$$

in which

the contrast (0~255) is set by Set Contrast command (81h).

For example, in order to achieve I_{SEG} = 300uA at maximum contrast 255, I_{REF} is set to around 10uA. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 8-15.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Recommended I_{REF} = 10uA.

Since the voltage at I_{REF} pin is V_{CC} - 3V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} = 12V:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (12 - 3) / 10\mu\text{A}$$

$$\approx 910\text{k}\Omega$$

8.7 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table 8-6 to Table 8-10 show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 ... D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

Table 8-6 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Horizontal Address Increment (A[2]=0)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

Table 8-6 : GDDRAM address map 1

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs Column Address (HEX) | |
|-------------|-------------------|------------|------------|------------|------------|--|------------|------------|------------|------------|--|----------------------|
| | | 00 | | 01 | | | 3E | | 3F | | | |
| COM0 | 00 | D0[3:0] | D0[7:4] | D1[3:0] | D1[7:4] | | D62[3:0] | D62[7:4] | D63[3:0] | D63[7:4] | | |
| COM1 | 01 | D64[3:0] | D64[7:4] | D65[3:0] | D65[7:4] | | D126[3:0] | D126[7:4] | D127[3:0] | D127[7:4] | | |
| | | | | | | | | | | | | |
| COM126 | 7E | D8064[3:0] | D8064[7:4] | D8065[3:0] | D8065[7:4] | | D8126[3:0] | D8126[7:4] | D8127[3:0] | D8127[7:4] | | |
| COM127 | 7F | D8128[3:0] | D8128[7:4] | D8129[3:0] | D8129[7:4] | | D8190[3:0] | D8190[7:4] | D8191[3:0] | D8191[7:4] | | |
| COM Outputs | Row Address (HEX) | | | | | | | | | | | Nibble re-map A[1]=0 |

Table 8-7 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Vertical Address Increment (A[2]=1)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

Table 8-7 : GDDRAM address map 2

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs Column Address (HEX) | |
|-----------------------|-------------------|-----------|-----------|-----------|-----------|--|------------|------------|------------|------------|--|----------------------|
| | | 00 | | 01 | | | 3E | | 3F | | | |
| COM0 | 00 | D0[3:0] | D0[7:4] | D128[3:0] | D128[7:4] | | D7936[3:0] | D7936[7:4] | D8064[3:0] | D8064[7:4] | | |
| COM1 | 01 | D1[3:0] | D1[7:4] | D129[3:0] | D129[7:4] | | D7937[3:0] | D7937[7:4] | D8065[3:0] | D8065[7:4] | | |
| | | | | | | | | | | | | |
| COM126 | 7E | D126[3:0] | D126[7:4] | D254[3:0] | D254[7:4] | | D8062[3:0] | D8062[7:4] | D8190[3:0] | D8190[7:4] | | |
| COM127 | 7F | D127[3:0] | D127[7:4] | D255[3:0] | D255[7:4] | | D8063[3:0] | D8063[7:4] | D8191[3:0] | D8191[7:4] | | |
| COM Outputs | Row Address (HEX) | | | | | | | | | | | |
| (Display Startline=0) | | | | | | | | | | | | Nibble re-map A[1]=0 |

Table 8-8 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Enable Column Address Re-map (A[0]=1)
 - Enable Nibble Re-map (A[1]=1)
 - Enable Horizontal Address Increment (A[2]=0)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

Table 8-8 : GDDRAM address map 3

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs Column Address (HEX) | |
|-----------------------|-------------------|------------|------------|------------|------------|--|------------|------------|------------|------------|--|----------------------|
| | | 3F | | 3E | | | 01 | | 00 | | | |
| COM0 | 00 | D63[7:4] | D63[3:0] | D62[7:4] | D62[3:0] | | D1[7:4] | D1[3:0] | D0[7:4] | D0[3:0] | | |
| COM1 | 01 | D127[7:4] | D127[3:0] | D126[7:4] | D126[3:0] | | D65[7:4] | D65[3:0] | D64[7:4] | D64[3:0] | | |
| | | | | | | | | | | | | |
| COM126 | 7E | D8127[7:4] | D8127[3:0] | D8126[7:4] | D8126[3:0] | | D8065[7:4] | D8065[3:0] | D8064[7:4] | D8064[3:0] | | |
| COM127 | 7F | D8191[7:4] | D8191[3:0] | D8190[7:4] | D8190[3:0] | | D8129[7:4] | D8129[3:0] | D8128[7:4] | D8128[3:0] | | |
| COM Outputs | Row Address (HEX) | | | | | | | | | | | |
| (Display Startline=0) | | | | | | | | | | | | Nibble re-map A[1]=1 |

Table 8-9 shows the example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Horizontal Address Increment (A[2]=0)
 - Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)

- Data byte sequence: D0, D1, D2 ... D8191

Table 8-9 : GDDRAM address map 4

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs Column Address (HEX) | |
|--|----------------------|-----------|------------|------------|------------|--|------------|------------|------------|------------|--|----------------------|
| | | 00 | | 01 | | | 3E | | 3F | | | |
| COM119 | 00 | D0[3:0] | D0[7:4] | D1[3:0] | D1[7:4] | | D62[3:0] | D62[7:4] | D63[3:0] | D63[7:4] | | |
| COM118 | 01 | D1[3:0] | D64[7:4] | D65[3:0] | D65[7:4] | | D126[3:0] | D126[7:4] | D127[3:0] | D127[7:4] | | |
| | | | | | | | | | | | | |
| COM121 | 7E | D126[3:0] | D8064[7:4] | D8065[3:0] | D8065[7:4] | | D8126[3:0] | D8126[7:4] | D8127[3:0] | D8127[7:4] | | |
| COM120 | 7F | D127[3:0] | D8128[7:4] | D8129[3:0] | D8129[7:4] | | D8190[3:0] | D8190[7:4] | D8191[3:0] | D8191[7:4] | | |
| COM Outputs (Display Startline=78H) | Row Address (HEX) | | | | | | | | | | | Nibble re-map A[1]=0 |

Table 8-10 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Horizontal Address Increment (A[2]=0)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 ... D7811

Table 8-10 : GDDRAM address map 5

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG124 | SEG125 | SEG126 | SEG127 | SEG Outputs Column Address (HEX) | |
|--------------------------------------|----------------------|------|------|------------|------------|--|------------|------------|--------|--------|--|----------------------|
| | | 00 | | 01 | | | 3E | | 3F | | | |
| COM0 | 00 | | | | | | | | | | | |
| COM1 | 01 | | | D0[3:0] | D0[7:4] | | D61[3:0] | D61[7:4] | | | | |
| | | | | | | | | | | | | |
| COM126 | 7E | | | D7750[3:0] | D7750[7:4] | | D7811[3:0] | D7811[7:4] | | | | |
| COM127 | 7F | | | | | | | | | | | |
| COM Outputs (Display Startline=0) | Row Address (HEX) | | | | | | | | | | | Nibble re-map A[1]=0 |

Notes:

- (1) Please refer to Table 9-1 for the details of setting command “Set Re-map” A0h.
- (2) The “Display Start Line” is set by the command “Set Display Start Line” A1h and please refer to Table 9-1 for the setting details.
- (3) The “Column Start/End Address” is set by the command “Set Column Address” 15h and please refer to Table 9-1 for the setting details.
- (4) The “Row Start/End Address” is set by the command “Set Row Address” 75h and please refer to Table 9-1 for the setting details.

8.8 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2, 3) and current drive (phase 4). The driving period is controlled by the gray scale settings (setting 0 ~ setting 127). The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding gray scale setting of the 16 gray scale levels (GS0~GS15) through the software commands B8h or B9h.

As shown in Figure 8-16, GDDRAM data has 4 bits, represent the 16 gray scale levels from GS0 to GS15. Note that the frame frequency is affected by GS15 setting.

Figure 8-16 : Relation between GDDRAM content and Gray Scale table entry (under command B9h Enable Linear Gray Scale Table)

| GDDRAM data (4 bits) | Gray Scale Table | Default Gamma Setting (Command B9h) |
|----------------------|--------------------|-------------------------------------|
| 0000 | GS0 | Setting 0 |
| 0001 | GS1 ⁽¹⁾ | Setting 0 |
| 0010 | GS2 | Setting 2 |
| 0011 | GS3 | Setting 4 |
| : | : | : |
| : | : | : |
| 1101 | GS13 | Setting 24 |
| 1110 | GS14 | Setting 26 |
| 1111 | GS15 | Setting 28 |

Note:

⁽¹⁾ Both GS0 and GS1 have no 2nd pre-charge (phase 3) and current drive (phase 4), however GS1 has 1st pre-charge (phase 2).

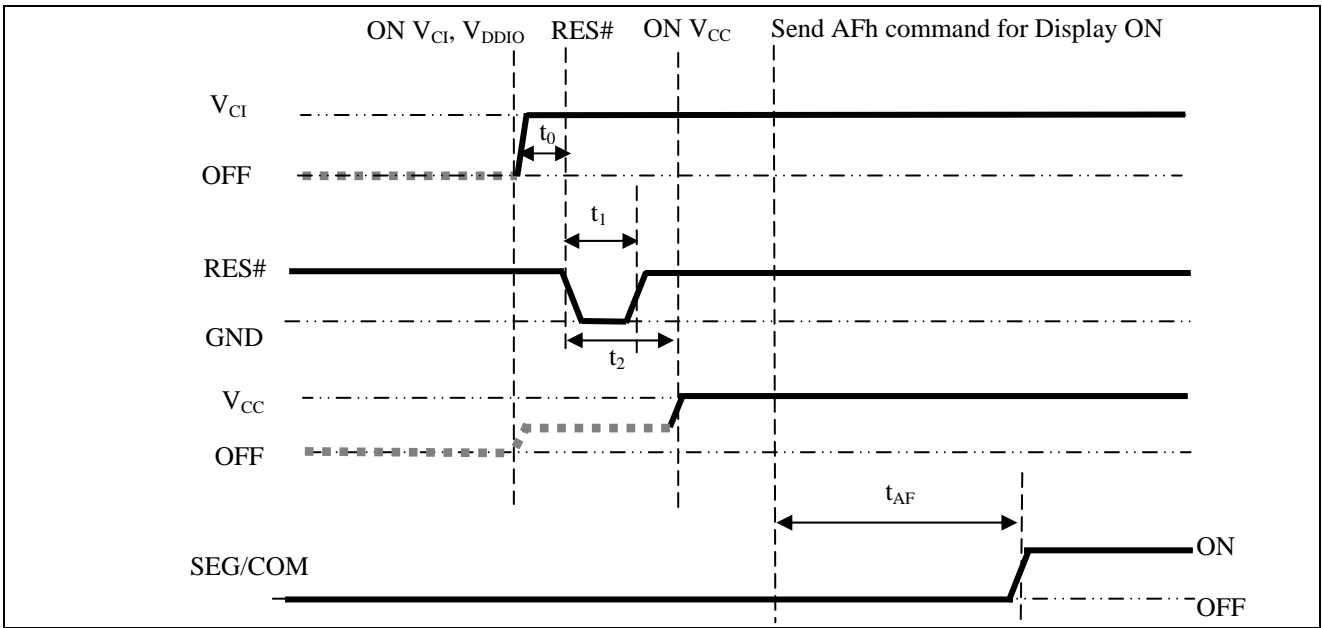
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1327 (assume internal V_{DD} is used).

Power ON sequence:

1. Power ON V_{CI} .
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).

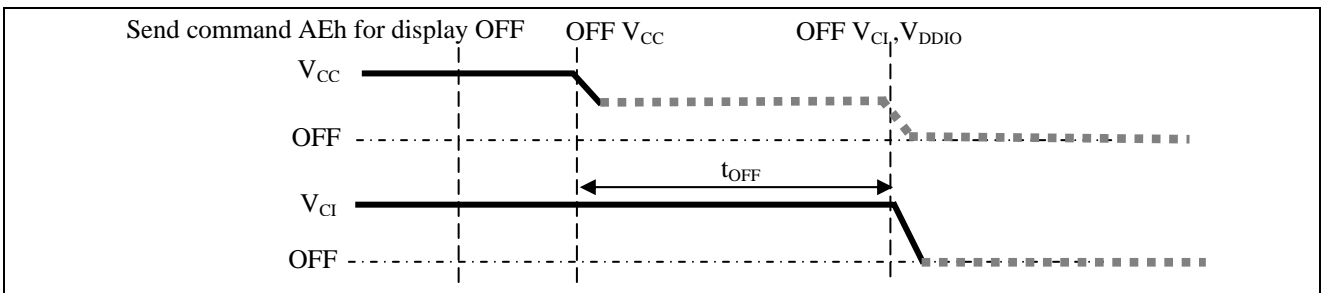
Figure 8-17 : The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2), (3)}
3. Wait for t_{OFF} . Power OFF V_{CI} . (where Minimum $t_{OFF}=0ms$ ⁽⁵⁾, Typical $t_{OFF}=100ms$)

Figure 8-18 : The Power OFF sequence



Note:

- (1) Since an ESD protection circuit is connected between V_{CI} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-17 and Figure 8-18.
- (2) V_{CC} should be kept float (disable) when it is OFF.
- (3) Power pins (V_{CI} , V_{CC}) can never be pulled to ground under any circumstance.
- (4) The register values are reset after t_1 .
- (5) V_{CI} should not be Power OFF before V_{CC} Power OFF.

8.10 V_{DD} Regulator

In SSD1327, the power supply pin for core logic operation, V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

The internal V_{DD} regulator is enabled by setting bit A[0] to 1b in command ABh “Function Selection”. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator. The typical regulated V_{DD} is about 2.5V

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated; V_{CI} must always be set equivalent to or higher than V_{DD}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 8-19 V_{CI} > 2.6V, V_{DD} regulator enable pin connection scheme

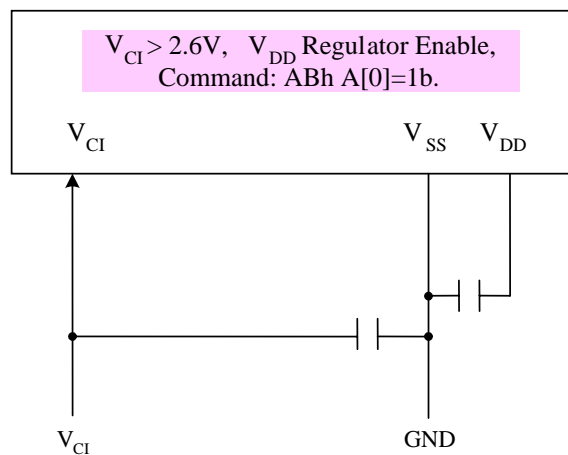
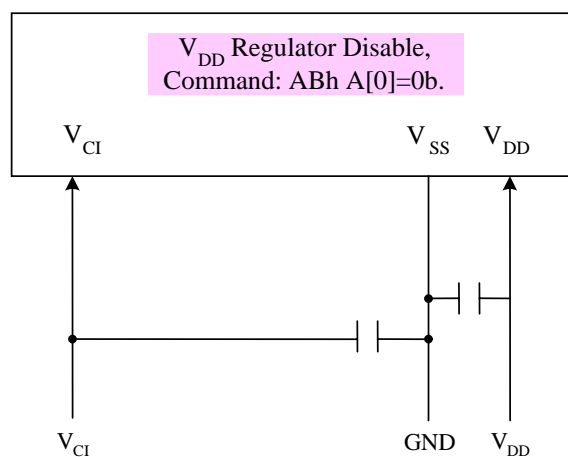


Figure 8-20 V_{DD} regulator disable pin connection scheme



No RAM access through MCU interface when there is no external / internal V_{DD}.

9 Command Table

Table 9-1: Command Table

(R/W#(WR#) = 0, E(RD#) = 1 unless specific setting is stated)

| 1. Fundamental Command Table | | | | | | | | | | | |
|------------------------------|------------------------|---------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|------------------------|--|
| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 0 0 | 15 A[5:0] B[5:0] | 0 * * | 0 * * | 0 A ₅ A ₅ | 1 A ₄ A ₄ | 0 A ₃ A ₃ | 1 A ₂ A ₂ | 0 A ₁ A ₁ | 1 A ₀ A ₀ | Set Column Address | Setup Column start and end address A[5:0]: Start Address, range:00h~3Fh, (RESET = 00h) B[5:0]: End Address, range:00h~3Fh, (RESET = 3Fh) |
| 0 0 0 | 75 A[6:0] B[6:0] | 0 * * | 0 A ₆ A ₆ | 0 A ₅ A ₅ | 1 A ₄ A ₄ | 0 A ₃ A ₃ | 1 A ₂ A ₂ | 0 A ₁ A ₁ | 1 A ₀ A ₀ | Set Row Address | Setup Row start and end address A[6:0]: Start Address, range:00h~7Fh, (RESET = 00h) B[6:0]: End Address, range:00h~7Fh, (RESET = 7Fh) |
| 0 0 | 81 A[7:0] | 1 A ₇ | 0 A ₆ | 0 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Contrast Control | Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh) |
| 0 | 84 ~ 86 | 1 | 0 | 0 | 0 | 0 | 1 | X ₁ | X ₀ | Reserved | Command for no operation |
| 0 0 | A0 A[7:0] | 1 0 | 0 A ₆ | 1 0 | 0 A ₄ | 0 0 | 0 A ₂ | 0 A ₁ | 0 A ₀ | Set Re-map | Re-map setting in Graphic Display Data RAM (GDDRAM) A[0] = 0b, Disable Column Address Re-map (RESET) A[0] = 1b, Enable Column Address Re-map A[1] = 0b, Disable Nibble Re-map (RESET) A[1] = 1b, Enable Nibble Re-map A[2] = 0b, Enable Horizontal Address Increment (RESET) A[2] = 1b, Enable Vertical Address Increment A[3] = 0b, Reserved (RESET) A[4] = 0b, Disable COM Re-map (RESET) A[4] = 1b, Enable COM Re-map A[5] = 0b, Reserved (RESET) A[6] = 0b, Disable COM Split Odd Even (RESET) A[6] = 1b, Enable COM Split Odd Even A[7] = 0b, Reserved (RESET) |
| 0 0 | A1 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Display Start Line | A[6:0]: Vertical shift by setting the starting address of display RAM from 0 ~ 127 (RESET = 00h) |

| 1. Fundamental Command Table | | | | | | | | | | | |
|------------------------------|--------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|----------------------|--|
| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 0 | A2 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Display Offset | A[6:0]: Set vertical offset by COM from 0 ~ 127 (RESET = 00h) e.g. Set A[6:0] to 010000b to move COM16 towards COM0 direction for 16 row |
| 0 | A4 ~ A7 | 1 | 0 | 1 | 0 | 0 | 1 | X ₁ | X ₀ | Set Display Mode | A4h = Normal display (RESET) A5h = All ON (All pixels have gray scale of 15, GS15) A6h = All OFF (All pixels have gray scale of 0, GS0) A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, ...) |
| 0 0 | A8 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 1 A ₃ | 0 A ₂ | 0 A ₁ | 0 A ₀ | Set MUX Ratio | A[6:0]: Set MUX ratio from 16MUX ~ 128MUX: A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 126 represents 127MUX A[6:0] = 127 represents 128MUX (RESET) It should be noted that A[6:0]=0~14 is not allowed |
| 0 0 | AB A[0] | 1 0 | 0 0 | 1 0 | 0 0 | 1 0 | 0 0 | 1 0 | 1 A ₀ | Function Selection A | A[0]=0b, Select external V _{DD} (i.e. Disable internal V _{DD} regulator) A[0]=1b, Enable internal V _{DD} regulator (RESET) |
| 0 | AE / AF | 1 | 0 | 1 | 0 | 1 | 1 | 1 | A ₀ | Set Display ON/OFF | A[0] = 0b, AEh = Display OFF (sleep mode) (RESET) A[0] = 1b, AFh = Display ON in normal mode |
| 0 0 | B1 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Phase Length | A[3:0]: Phase 1 period of 1~15 DCLK's e.g. A[3:0] = 1111b, 15 DCLK Clock (RESET = 0100b) A[7:4]: Phase 2 period of 1~15 DCLK's e.g. A[7:4] = 1111b, 15 DCLK Clocks (RESET = 0111b) Note (¹) 0 DCLK is invalid in phase 1 & phase 2 (²) GS15 level pulse width must be set larger than the period of phase 1 + phase 2 |
| 0 | B2 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | NOP | Command for no operation |

| 1. Fundamental Command Table | | | | | | | | | | | |
|--|--|-------------------------------------|-------------------------------------|---|---|---|---|---|---|---|--|
| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 0 | B3 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Set Front Clock Divider /Oscillator Frequency | A[3:0]: Define divide ratio (D) of display clock (DCLK) Divide ratio=A[3:0]+1 (RESET is 0000b, i.e. divide ratio = 1) A[7:4]: Set the Oscillator Frequency, F _{osc} . Oscillator Frequency increases with the value of A[7:4] and vice versa. (Range:0000b~1111b) (RESET = 0000b) |
| 0 0 | B5 A[1:0] | 1 0 | 0 0 | 1 0 | 1 0 | 0 0 | 1 0 | 0 A ₁ | 1 A ₀ | GPIO | A[1:0] = 00b represents GPIO pin HiZ, input disable (always read as low) A[1:0] = 01b represents GPIO pin HiZ, input enable A[1:0] = 10b represents GPIO pin output Low (RESET) A[1:0] = 11b represents GPIO pin output High |
| 0 0 | B6 A[3:0] | 1 * | 0 * | 1 * | 1 * | 0 A ₃ | 1 A ₂ | 1 A ₁ | 0 A ₀ | Set Second pre-charge Period | A[3:0]: Second Pre-charge period of 1~15 DCLK's e.g. A[3:0] = 1111b, 15 DCLK Clock (RESET = 0100b) Note (1) This command is used to adjust the second pre-charge period after enabling the second pre-charge by setting A[1] = 1b in command D5h |
| 0 0 0 0 0 | B8 A1[5:0] A2[5:0] A14[5:0] A15[5:0] | 1 * * * * | 0 * * * * | 1 A ₁₅ A ₂₅ A ₁₄₅ A ₁₅₅ | 1 A ₁₄ A ₂₄ A ₁₄₄ A ₁₅₄ | 1 A ₁₃ A ₂₃ A ₁₄₃ A ₁₅₃ | 0 A ₁₂ A ₂₂ A ₁₄₂ A ₁₅₂ | 0 A ₁₁ A ₂₁ A ₁₄₁ A ₁₅₁ | 0 A ₁₀ A ₂₀ A ₁₄₀ A ₁₅₀ | Set Gray Scale Table | The next 15 data bytes set the gray scale pulse width in unit of DCLK's. A1[5:0], value for GS1 level Pulse width A2[5:0], value for GS2 level Pulse width ... A14[5:0], value for GS14 level Pulse width A15[5:0], value for GS15 level Pulse width Note (1) The pulse width value of GS1, GS2, ..., GS15 should not be equal. i.e. 0<GS1<GS2 ... <GS15 (2) GS15 level pulse width must be set larger than the period of phase 1 + phase 2 |
| 0 | B9 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Linear LUT | The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 2; GS3 level pulse width = 4; : : GS14 level pulse width = 26; GS15 level pulse width = 28 |

1. Fundamental Command Table

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description | | | | | | | | | | | | | | | | | | | | | |
|--------|--------------|--------------------------------|--------|--------|--------|---------------------|---------------------|---------------------|---------------------|------------------------|--|--------|----------|--------------------|------|-----|------------------------|---|---|---|------|-----|--------------------------------|---|---|---|------|-----|-------------------------|------|-----|-------------------|
| 0 | BB | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | NOP | Command for no operation | | | | | | | | | | | | | | | | | | | | | |
| 0 0 | BC A[3:0] | 1 0 | 0 0 | 1 0 | 1 0 | 1 A ₃ | 1 A ₂ | 0 A ₁ | 0 A ₀ | Set Pre-charge voltage | Set pre-charge voltage level. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A[3:0]</th> <th>Hex code</th> <th>Pre-charge voltage</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h</td> <td>0.20 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>0101</td> <td>05h</td> <td>0.5 x V_{CC} (RESET)</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>0111</td> <td>07h</td> <td>0.613 x V_{CC}</td> </tr> <tr> <td>1xxx</td> <td>08h</td> <td>V_{COMH}</td> </tr> </tbody> </table> | A[3:0] | Hex code | Pre-charge voltage | 0000 | 00h | 0.20 x V _{CC} | : | : | : | 0101 | 05h | 0.5 x V _{CC} (RESET) | : | : | : | 0111 | 07h | 0.613 x V _{CC} | 1xxx | 08h | V _{COMH} |
| A[3:0] | Hex code | Pre-charge voltage | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | 00h | 0.20 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101 | 05h | 0.5 x V _{CC} (RESET) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | 07h | 0.613 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1xxx | 08h | V _{COMH} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 0 | BE A[2:0] | 1 0 | 0 0 | 1 0 | 1 0 | 1 0 | 1 A ₂ | 1 A ₁ | 0 A ₀ | Set V _{COMH} | Set COM deselect voltage level. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A[2:0]</th> <th>Hex code</th> <th>V_{COMH}</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>00h</td> <td>0.72 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>101</td> <td>05h</td> <td>0.82 x V_{CC} (RESET)</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>111</td> <td>07h</td> <td>0.86 x V_{CC}</td> </tr> </tbody> </table> | A[2:0] | Hex code | V _{COMH} | 000 | 00h | 0.72 x V _{CC} | : | : | : | 101 | 05h | 0.82 x V _{CC} (RESET) | : | : | : | 111 | 07h | 0.86 x V _{CC} | | | |
| A[2:0] | Hex code | V _{COMH} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 00h | 0.72 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101 | 05h | 0.82 x V _{CC} (RESET) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | 07h | 0.86 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 0 | D5 A[2:0] | 1 0 | 1 1 | 0 1 | 1 0 | 0 0 | 1 0 | 0 A ₁ | 1 A ₀ | Function Selection B | A[1] = 0b: Disable second precharge (RESET) A[1] = 1b: Enable second precharge A[0] = 0b: Internal VSL (RESET) A[0] = 1b: Enable external VSL Note ⁽¹⁾ Refer to Table 7-1 for VSL pin details | | | | | | | | | | | | | | | | | | | | | |
| 0 0 | FD A[2] | 1 0 | 1 0 | 1 0 | 1 1 | 1 0 | 1 A ₂ | 0 1 | 1 0 | Set Command Lock | A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note ⁽¹⁾ The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command | | | | | | | | | | | | | | | | | | | | | |

2. Scrolling Command Table

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|------|---------|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------------------------|---|
| 0 | 26 / 27 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | X ₀ | Continuous Horizontal Scroll Setup | 26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) |
| 0 | A[7:0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | A[7:0] : Dummy byte (Set as 00h) |
| 0 | B[6:0] | * | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | B[2:0] : Define start row address; range:00h~7Fh, (RESET = 00h) |
| 0 | C[2:0] | * | * | * | 0 | 0 | C ₂ | C ₁ | C ₀ | | C[2:0] : Set time interval between each scroll step in terms of frame frequency |
| 0 | D[6:0] | * | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | |
| 0 | E[5:0] | * | * | E ₅ | E ₄ | E ₃ | E ₂ | E ₁ | E ₀ | | |
| 0 | F[5:0] | * | * | F ₅ | F ₄ | F ₃ | F ₂ | F ₁ | F ₀ | | |
| 0 | G[7:0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | G[7:0] : Dummy byte (Set as 00h) |
| 0 | 2E | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Deactivate scroll | Stop scrolling that is configured by command 26h/27h Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten. |
| 0 | 2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Activate scroll | Start scrolling that is configured by the scrolling setup commands :26h/27h with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. |

Note

(1) "*" stands for "Don't care".

9.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 9-2 : Address increment table (Automatic)

| D/C# | R/W# (WR#) | Comment | Address Increment |
|-------------|-------------------|----------------|--------------------------|
| 0 | 0 | Write Command | No |
| 0 | 1 | Read Status | No |
| 1 | 0 | Write Data | Yes |
| 1 | 1 | Read Data | Yes |

10 COMMAND DESCRIPTIONS

10.1 Fundamental command description

10.1.1 Set Column Address (15h)

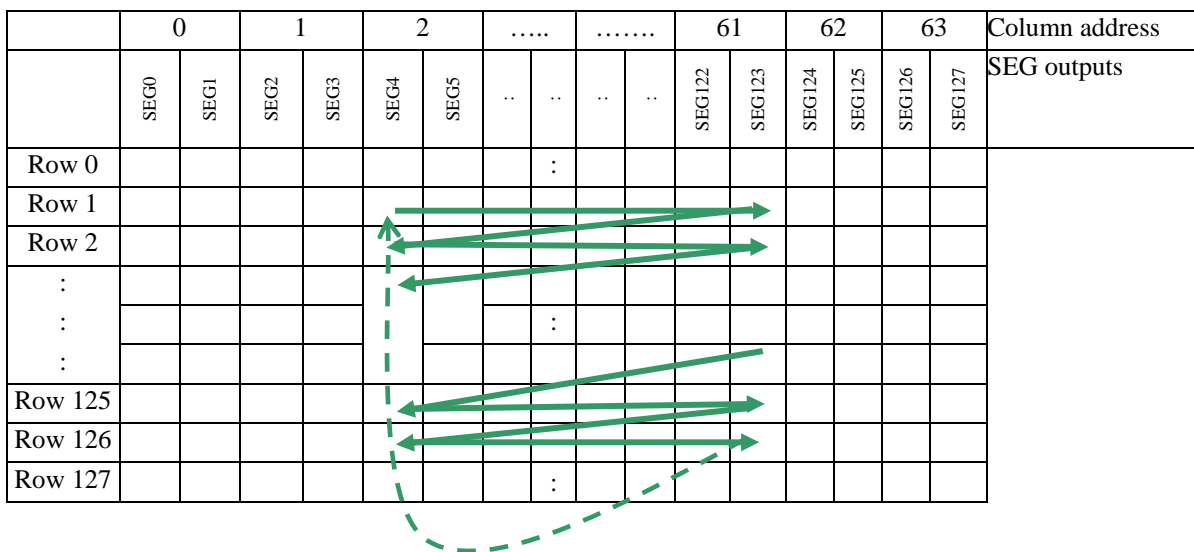
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 61, row start address is set to 1 and row end address is set to 126; horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 61 and from row 1 to row 126 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-1*). Whenever the column address pointer finishes accessing the end column 61, it is reset back to column 2 and row address is automatically increased by 1 (*solid line in Figure 10-1*). While the end row 126 and end column 61 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 10-1*).

Figure 10-1: Example of Column and Row Address Pointer Movement



10.1.3 Set Contrast Current (81h)

This double byte command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

10.1.4 NOP (84h ~ 86h)

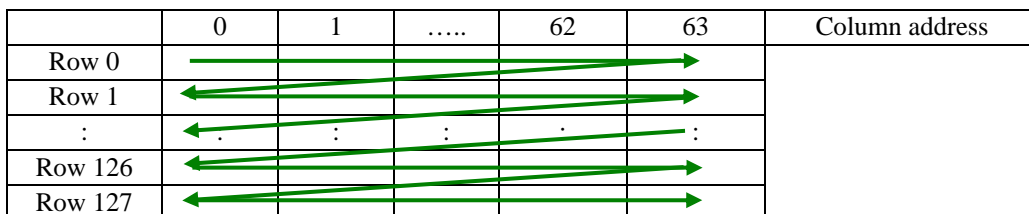
These are no operation commands.

10.1.5 Set Re-map (A0h)

This double byte command has multiple configurations and each bit setting is described as follows:

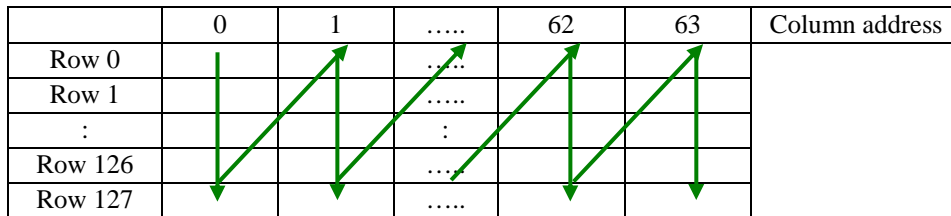
- Column Address Remapping (A[0])**
 This bit is made for increase the flexibility layout of segment signals in OLED module with segment arranged from left to right (when A[0] is set to 0) or from right to left (when A[0] is set to 1).
- Nibble Remapping (A[1])**
 When A[1] is set to 1, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4).
 If this feature works together with Column Address Re-map, it would produce an effect of flipping the outputs from SEG0~127 to SEG127~SEG0 as show in Table 8-8.
- Address increment mode (A[2])**
 When A[2] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-2.

Figure 10-2: Address Pointer Movement of Horizontal Address Increment Mode



When A[2] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-3.

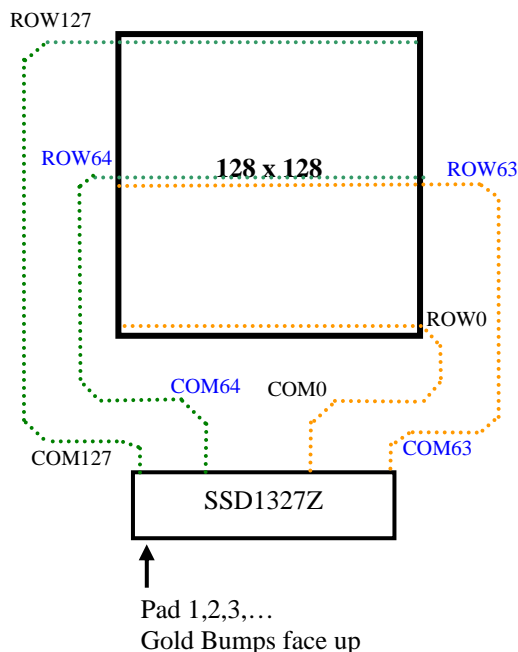
Figure 10-3: Address Pointer Movement of Vertical Address Increment Mode



- **COM Remapping (A[4])**
This bit defines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down (when A[4] is set to 0) or from bottom to up (when A[4] is set to 1). Table 8-9 shows an example of the using the COM Remapping to perform vertical scrolling.
- **Splitting of Odd / Even COM Signals (A[6])**
This bit is made to match the COM layout connection on the panel.

When A[6] is set to 0, no splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 128MUX ratio):

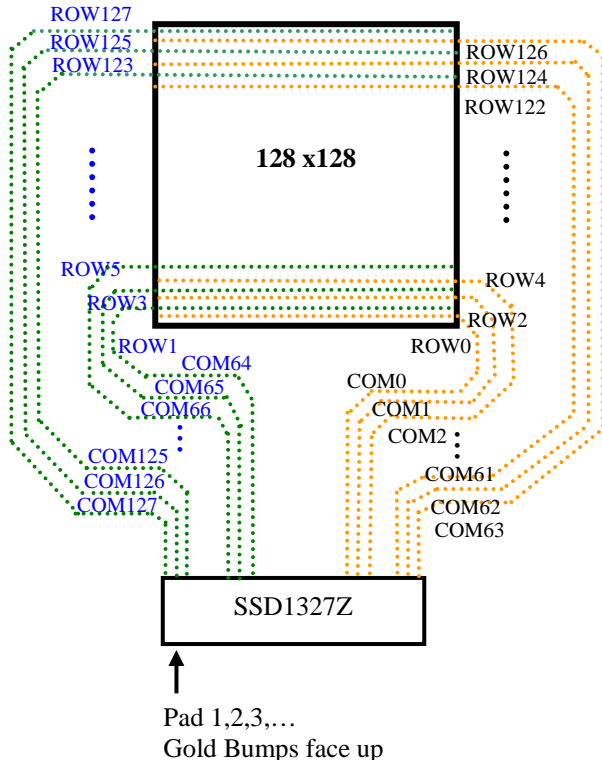
Figure 10-4: Output pin assignment when command A0h bit A[6]=0.



| Output Pin Connection | |
|-----------------------|--------|
| SSD1327Z | Panel |
| COM0 | ROW0 |
| COM1 | ROW1 |
| COM2 | ROW2 |
| COM3 | ROW3 |
| : | : |
| COM63 | ROW63 |
| COM64 | ROW64 |
| : | : |
| COM125 | ROW125 |
| COM126 | ROW126 |
| COM127 | ROW127 |

When A[6] is set to 1, splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 128MUX ratio):

Figure 10-5 : Output pin assignment when command A0h bit A[6]=1.



| Output Pin Connection | |
|-----------------------|-------------|
| SSD1327Z | Panel |
| COM0 | ROW0 (Even) |
| COM1 | ROW2 |
| COM2 | ROW4 |
| : | : |
| COM61 | ROW122 |
| COM62 | ROW124 |
| COM63 | ROW126 |
| COM64 | ROW1 (Odd) |
| COM65 | ROW3 |
| COM66 | ROW5 |
| : | : |
| COM125 | ROW123 |
| COM126 | ROW125 |
| COM127 | ROW127 |

10.1.6 Set Display Start Line (A1h)

This double byte command is to set Display Start Line register for determining the starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 10-6 shows an example using this command of this command when MUX ratio= 128 and MUX ratio= 90 and Display Start Line = 40. In there, “ROW” means the graphic display data RAM row.

Figure 10-6: Example of Set Display Start Line with no Remapping





| | MUX ratio (A8h) = 128 | MUX ratio (A8h) = 128 | MUX ratio (A8h) = 90 | MUX ratio (A8h) = 90 |
|-----------------|------------------------------|-------------------------------|------------------------------|-------------------------------|
| COM Pin | Display Start Line (A1h) = 0 | Display Start Line (A1h) = 40 | Display Start Line (A1h) = 0 | Display Start Line (A1h) = 40 |
| COM0 | ROW0 | ROW40 | ROW0 | ROW40 |
| COM1 | ROW1 | ROW41 | ROW1 | ROW41 |
| COM2 | ROW2 | ROW42 | ROW2 | ROW42 |
| COM3 | ROW3 | ROW43 | ROW3 | ROW43 |
| : | : | : | : | : |
| : | : | : | : | : |
| COM48 | ROW48 | ROW88 | ROW48 | ROW88 |
| COM49 | ROW49 | ROW89 | ROW49 | ROW89 |
| COM50 | ROW50 | ROW90 | ROW50 | ROW90 |
| COM51 | ROW51 | ROW91 | ROW51 | ROW91 |
| : | : | : | : | : |
| : | : | : | : | : |
| COM86 | ROW86 | ROW126 | ROW86 | ROW126 |
| COM87 | ROW87 | ROW127 | ROW87 | ROW127 |
| COM88 | ROW88 | ROW0 | ROW88 | ROW0 |
| COM89 | ROW89 | ROW1 | ROW89 | ROW1 |
| COM90 | ROW90 | ROW2 | - | - |
| COM91 | ROW91 | ROW3 | - | - |
| : | : | : | : | : |
| : | : | : | : | : |
| COM124 | ROW124 | ROW36 | - | - |
| COM125 | ROW125 | ROW37 | - | - |
| COM126 | ROW126 | ROW38 | - | - |
| COM127 | ROW127 | ROW39 | - | - |
| Display Example | | | | |

10.1.7 Set Display Offset (A2h)

This double byte command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0~COM127.

shows an example using this command when MUX ratio= 128 and MUX ratio= 90 and Display Offset = 40. In there, “Row” means the graphic display data RAM row.

Figure 10-7: Example of Set Display Offset with no Remapping

| | MUX ratio (A8h) = 128 | MUX ratio (A8h) = 128 | MUX ratio (A8h) = 90 | MUX ratio (A8h) = 90 |
|-----------------|---|---|--|---|
| COM Pin | Display Offset (A2h)=0 | Display Offset (A2h)=40 | Display Offset (A2h)=0 | Display Offset (A2h)=40 |
| COM0 | ROW0 | ROW40 | ROW0 | ROW40 |
| COM1 | ROW1 | ROW41 | ROW1 | ROW41 |
| COM2 | ROW2 | ROW42 | ROW2 | ROW42 |
| COM3 | ROW3 | ROW43 | ROW3 | ROW43 |
| : | : | : | : | : |
| : | : | : | : | : |
| COM48 | ROW48 | ROW88 | ROW48 | ROW88 |
| COM49 | ROW49 | ROW89 | ROW49 | ROW89 |
| COM50 | ROW50 | ROW90 | ROW50 | - |
| COM51 | ROW51 | ROW91 | ROW51 | - |
| : | : | : | : | : |
| : | : | : | : | : |
| COM86 | ROW86 | ROW126 | ROW86 | - |
| COM87 | ROW87 | ROW127 | ROW87 | - |
| COM88 | ROW88 | ROW0 | ROW88 | ROW0 |
| COM89 | ROW89 | ROW1 | ROW89 | ROW1 |
| COM90 | ROW90 | ROW2 | - | ROW2 |
| COM91 | ROW91 | ROW3 | - | ROW3 |
| : | : | : | : | : |
| : | : | : | : | : |
| COM124 | ROW124 | ROW36 | - | ROW36 |
| COM125 | ROW125 | ROW37 | - | ROW37 |
| COM126 | ROW126 | ROW38 | - | ROW38 |
| COM127 | ROW127 | ROW39 | - | ROW39 |
| Display Example |  |  |  |  |

10.1.8 Set Display Mode (A4h ~ A7h)

These are single byte commands (A4h ~ A7h) and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display, respectively.

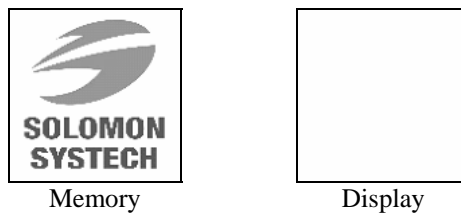
- Normal Display (A4h)
Reset the “Entire Display ON, Entire Display OFF or Inverse Display” effects and turn the data to ON at the corresponding gray level. Figure 10-8 shows an example of Normal Display.

Figure 10-8: Example of Normal Display



- Set Entire Display ON (A5h)
Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM, as shown on Figure 10-9.

Figure 10-9: Example of Entire Display ON



- Set Entire Display OFF (A6h)
Force the entire display to be at gray scale level GS0, regardless of the contents of the display data RAM, as shown on Figure 10-10.

Figure 10-10 : Example of Entire Display OFF



- Inverse Display (A7h)
The gray scale level of display data are swapped such that “GS0” <-> “GS15”, “GS1” <-> “GS14”, etc. Figure 10-11 shows an example of inverse display.

Figure 10-11: Example of Inverse Display



10.1.9 Set Multiplex Ratio (A8h)

This double byte command sets multiplex ratio (MUX ratio) from 16MUX to 128MUX. In RESET, multiplex ratio is 128MUX. Please refer to Figure 10-6 and Figure 10-7 for the example of setting different MUX ratio.

10.1.10 Function selection A (ABh)

This double byte command is used to enable or disable the V_{DD} regulator.

Internal V_{DD} regulator is enabled when the bit A[0] is set to 1b, while internal V_{DD} regulator is disabled when A[0] is set to 0b.

10.1.11 Set Display ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.

When the display is OFF (command AEh), the segment pins are in V_{SS} state and common pins are in high impedance state.

Figure 10-12: Display ON Sequence (when initial start)

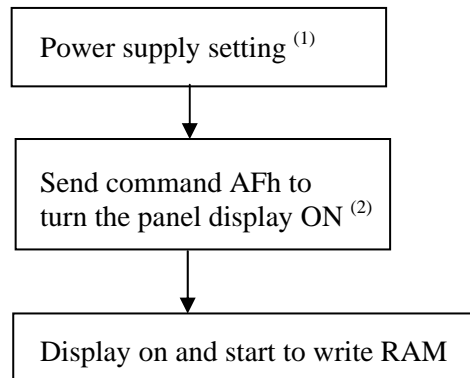
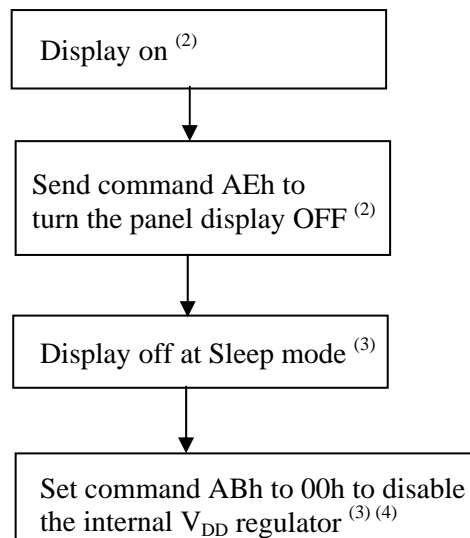


Figure 10-13: Display OFF Sequence



Note:

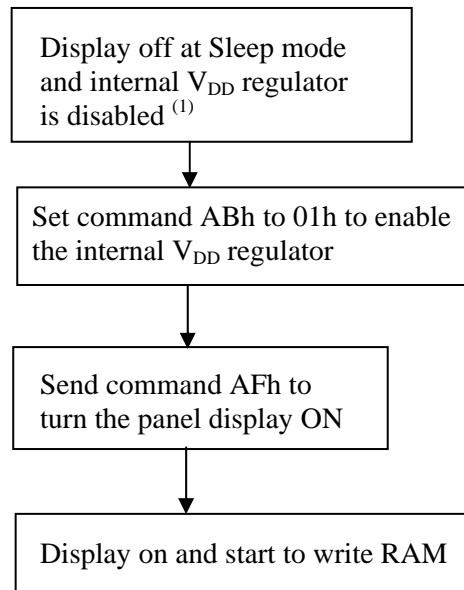
⁽¹⁾ Please follow the power ON sequence as suggested on Figure 8-17

⁽²⁾ Internal V_{DD} regulator is ON as default

⁽³⁾ The RAM content is kept during display off at both sleep mode and the case that internal V_{DD} regulator is disabled.

⁽⁴⁾ It is recommended to disable internal V_{DD} regulator during Sleep mode for power save. Refer to Table 12-1.

Figure 10-14: Display ON Sequence (During Sleep mode and internal V_{DD} regulator is disabled)



Note:

⁽¹⁾ The RAM content is kept during display off at sleep mode and internal V_{DD} regulator is disabled.

10.1.12 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 1 to 15 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_p.

10.1.13 NOP (B2h)

These are no operation commands.

10.1.14 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to Section 8.3 for the detail relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

10.1.15 Set GPIO (B5h)

This double byte command is used to set the states of GPIO0 and GPIO1 pins. Refer to Table 9-1 for details.

10.1.16 Set Second Pre-charge period (B6h)

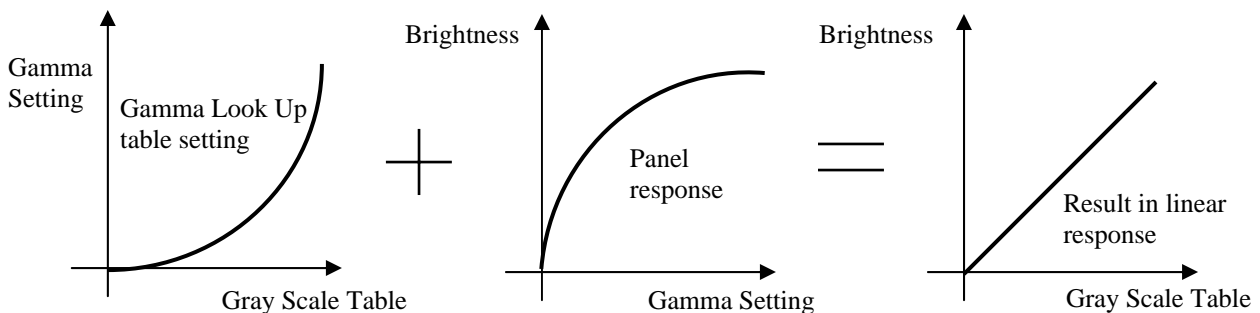
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 0 to 15 DCLK's (as long as the second pre-charge is enabled by setting A[1] of command D5h to 1). Please refer to Table 9-1 for the detail information.

10.1.17 Set Gray Scale Table (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command B8h, the user has to set the gray scale setting for GS1, GS2, ..., GS14, GS15 one by one in sequence. Refer to Section 8.8 for details.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 10-15) can compensate this effect.

Figure 10-15 : Example of Gamma correction by Gamma Look Up table setting



10.1.18 Select Default Linear Gray Scale Table (B9h)

This single byte command reloads the preset linear Gray Scale table as GS0 = Gamma Setting 0, GS1 = Gamma Setting 0, GS2 = Gamma Setting 2, ..., GS14 = Gamma Setting 26, GS15 = Gamma Setting 28. Refer to Section 8.8 for details.

10.1.19 NOP (BBh)

These are no operation commands.

10.1.20 Set Pre-charge voltage (BCh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.21 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH} . The level of V_{COMH} is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.22 Function selection B (D5h)

This double byte command consists of two functions:

- Set second precharge (A[1])
Second precharge is enabled when A[1] is set to 1, whereas it is disabled as default at A[1] = 0. .
- Set VSL (A[0])
External VSL is enabled when A[0] is set to 1, whereas it is set to internal VSL as default at A[0] = 0.
Refer to Table 9-1 for details.

10.1.23 Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

10.2 Graphic Acceleration command description

10.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1327 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 10-16, Figure 10-17, and Figure 10-18) show the examples of using the horizontal scroll:

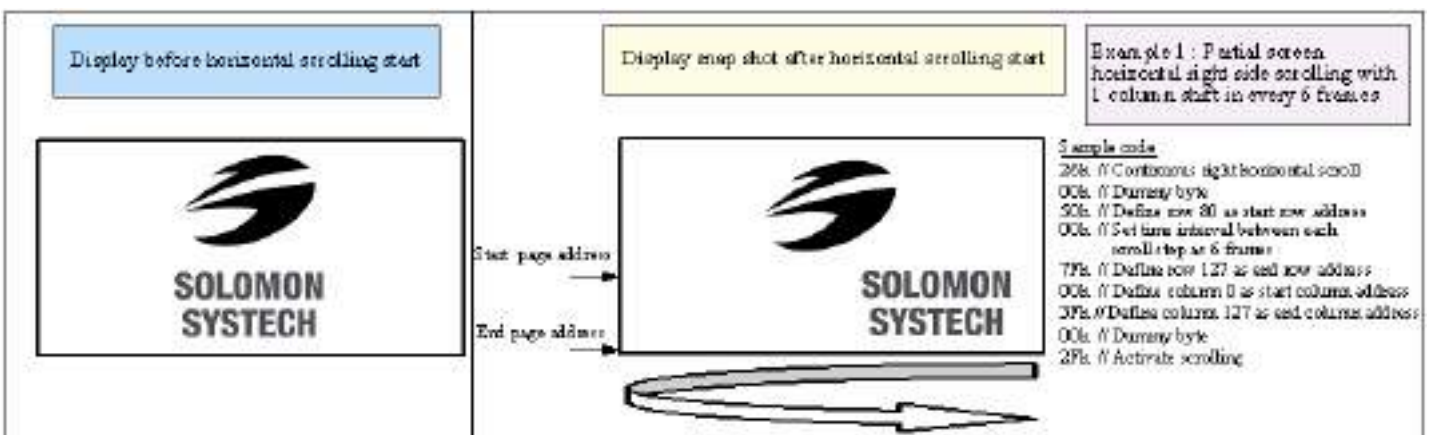
Figure 10-16 : Horizontal scroll example: Scroll RIGHT by 1 column

| | | | | | | | | | | | | | | | |
|-----------------------|--------|------|------|------|------|------|-----|-----|-----|--------|--------|--------|--------|--------|--------|
| Original Setting | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | ... | ... | ... | SEG122 | SEG123 | SEG124 | SEG125 | SEG126 | SEG127 |
| After one scroll step | SEG127 | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | ... | ... | ... | SEG121 | SEG122 | SEG123 | SEG124 | SEG125 | SEG126 |

Figure 10-17 : Horizontal scroll example: Scroll LEFT by 1 column

| | | | | | | | | | | | | | | | |
|-----------------------|------|------|------|------|------|------|-----|-----|-----|--------|--------|--------|--------|--------|--------|
| Original Setting | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | ... | ... | ... | SEG122 | SEG123 | SEG124 | SEG125 | SEG126 | SEG127 |
| After one scroll step | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | ... | ... | ... | SEG123 | SEG124 | SEG125 | SEG126 | SEG127 | SEG0 |

Figure 10-18 : Horizontal scrolling setup example



10.2.2 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.3 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands: 26h / 27h. The setting in the latest scrolling setup command overwrites the setting in the previous scrolling setup command.

The following actions are prohibited after the scrolling is activated,

1. RAM access (Data write or read).
2. Changing the horizontal scroll setup parameters.

11 MAXIMUM RATINGS

Table 11-1: Maximum Ratings

(Voltage Reference to V_{SS})

| Symbol | Parameter | Value | Unit |
|-----------|---------------------------|------------------------------|------|
| V_{DD} | Supply Voltage | -0.5 to 2.75 | V |
| V_{CC} | | -0.5 to 19.0 | V |
| V_{CI} | | -0.3 to 4.0 | V |
| V_{SEG} | SEG output voltage | 0 to V_{CC} | V |
| V_{COM} | COM output voltage | 0 to $0.9 \cdot V_{CC}$ | V |
| V_{in} | Input voltage | $V_{SS}-0.3$ to $V_{CI}+0.3$ | V |
| T_A | Operating Temperature | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

$V_{DD} = 1.65$ to $2.6V$

$V_{CI} = 1.65$ to $3.5V$ (V_{CI} must be larger than or equal to V_{DD})

$T_A = 25^\circ C$

Table 12-1 : DC Characteristics

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | |
|----------------|--|--|---|------|----------------|---------|---------|
| V_{CC} | Operating Voltage | - | 8 | - | 18 | V | |
| V_{DD} | Logic Supply Voltage | - | 1.65 | - | 2.6 | V | |
| V_{CI} | Low voltage power supply, power supply for I/O pins | - | 1.65 | - | 3.5 | V | |
| V_{OH} | High Logic Output Level | $I_{out} = 100\mu A$ | $0.9 * V_{CI}$ | - | V_{CI} | V | |
| V_{OL} | Low Logic Output Level | $I_{out} = 100\mu A$ | 0 | - | $0.1 * V_{CI}$ | V | |
| $V_{IH}^{(1)}$ | High Logic Input Level | - | $0.8 * V_{CI}$ | - | V_{CI} | V | |
| $V_{IL}^{(1)}$ | Low Logic Input Level | - | 0 | - | $0.2 * V_{CI}$ | V | |
| I_{SLP_VDD} | V_{DD} Sleep mode Current | $V_{CI} = 2.8V$, $V_{CC} = OFF$ $V_{DD}(external) = 2.5V$, Display OFF, No panel attached | - | - | 10 | μA | |
| I_{SLP_VCI} | V_{CI} Sleep mode Current | $V_{CI} = 2.8V$, $V_{CC} = OFF$ Display OFF, No panel attached | External $V_{DD} = 2.5V$ | - | - | 10 | μA |
| | | | Enable Internal V_{DD} during Sleep mode | - | - | 40 | μA |
| | | | Disable Internal V_{DD} during Sleep mode (Deep Sleep mode) | - | - | 10 | μA |
| I_{SLP_VCC} | V_{CC} Sleep mode Current | $V_{CI} = 2.8V$, $V_{CC} = 8\sim 18V$ $V_{DD}(external) = 2.5V$, Display OFF, No panel attached | - | - | 10 | μA | |
| I_{DD} | V_{DD} Supply Current | $V_{CI} = 3.5V$, $V_{CC} = 18V$, External $V_{DD} = 2.5V$, Display ON, No panel attached, contrast = FF | - | 22 | - | μA | |
| I_{CI} | V_{CI} Supply Current | $V_{CI} = 3.5V$, $V_{CC} = 18V$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.5V$ | - | 35 | 50 | μA |
| | | | Internal $V_{DD} = 2.5V$ | - | 95 | 120 | μA |
| I_{CC} | V_{CC} Supply Current | $V_{CI} = 3.5V$, $V_{CC} = 18V$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.5V$ | - | 600 | 750 | μA |
| | | | Internal $V_{DD} = 2.5V$ | - | 600 | 750 | μA |
| I_{SEG} | Segment Output Current Setting $V_{CC} = 18V$, $I_{REF} = 10\mu A$ | Contrast = FF | - | 300 | 370 | μA | |
| | | Contrast = AF | - | 206 | - | μA | |
| | | Contrast = 7F | - | 150 | - | μA | |
| | | Contrast = 3F | - | 75 | - | μA | |
| | | Contrast = 1F | - | 37.5 | - | μA | |
| Dev | Segment output current uniformity | $Dev = (I_{SEG} - I_{MID}) / I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ $I_{SEG} =$ Segment current at contrast FF | -3 | - | 3 | % | |
| Adj. Dev | Adjacent pin output current uniformity (contrast = FFh) | $Adj\ Dev = (I[n] - I[n+1]) / (I[n] + I[n+1])$ | -2 | - | 2 | % | |

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

$V_{DD} = 2.4$ to $2.6V$

$T_A = 25^{\circ}C$

Table 13-1 : AC Characteristics

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|-----------------|---|---|------|-------------------------------------|------|------|
| $F_{OSC}^{(1)}$ | Oscillation Frequency of Display Timing Generator | $V_{CI} = 2.8V$, internal V_{DD} | 535 | 595 | 655 | kHz |
| F_{FRM} | Frame Frequency for 128 MUX Mode | 128x128 Graphic Display Mode, Display ON, Internal Oscillator Enabled | - | $F_{OSC} * 1 / (D * K * 128)^{(2)}$ | - | Hz |
| t_{RES} | Reset low pulse width (RES#) | - | 2000 | - | - | ns |

Note

⁽¹⁾ F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

⁽²⁾ D: divide ratio

K: Phase 1 period + Phase 2 period + X

X: DCLKs in current drive period.

Default K is $4 + 7 + 30 = 41$

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

($V_{CI} - V_{SS} = 1.65V$ to $3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-1 : 6800-series MCU parallel interface characteristics

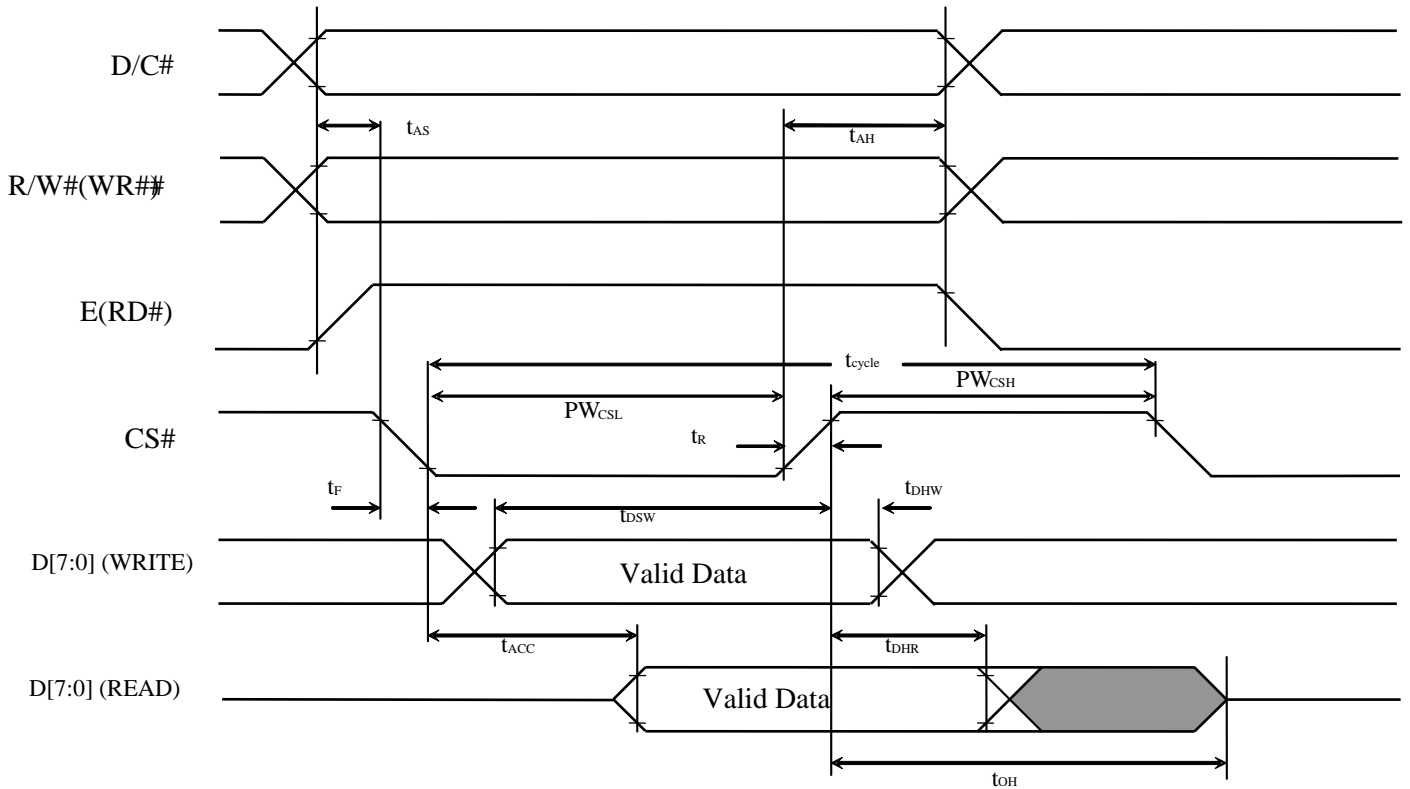


Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

($V_{CI} - V_{SS} = 1.65V$ to $3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| t_{PWLR} | Read Low Time | 150 | - | - | ns |
| t_{PWLW} | Write Low Time | 60 | - | - | ns |
| t_{PWHR} | Read High Time | 60 | - | - | ns |
| t_{PWHW} | Write High Time | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |
| t_{CS} | Chip select setup time | 0 | - | - | ns |
| t_{CSH} | Chip select hold time to read signal | 0 | - | - | ns |
| t_{CSF} | Chip select hold time | 20 | - | - | ns |

Figure 13-2 : 8080-series MCU parallel interface characteristics

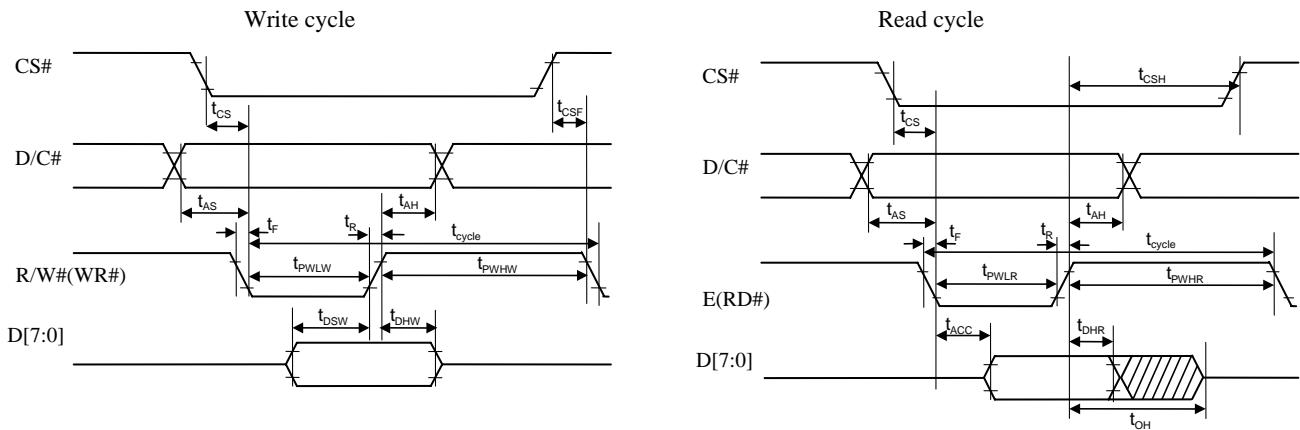


Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

($V_{CI} - V_{SS} = 1.65V$ to $3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 100 | - | - | ns |
| t_{AS} | Address Setup Time | 15 | - | - | ns |
| t_{AH} | Address Hold Time | 15 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-3 : Serial interface characteristics (4-wire SPI)

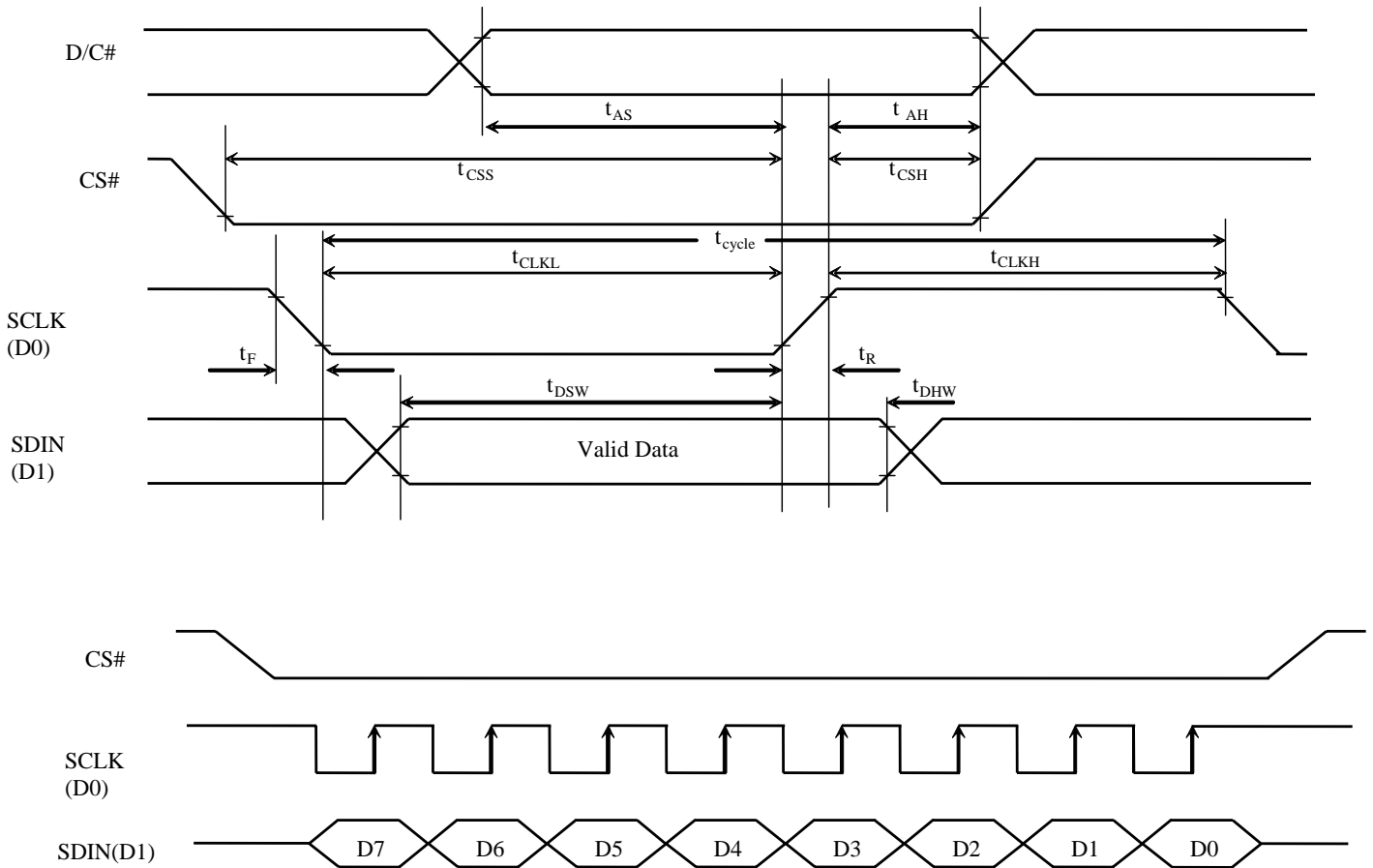


Table 13-5: Serial Interface Timing Characteristics (3-wire SPI)

($V_{CI} - V_{SS} = 1.65V$ to $3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 100 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-4: Serial interface characteristics (3-wire SPI)

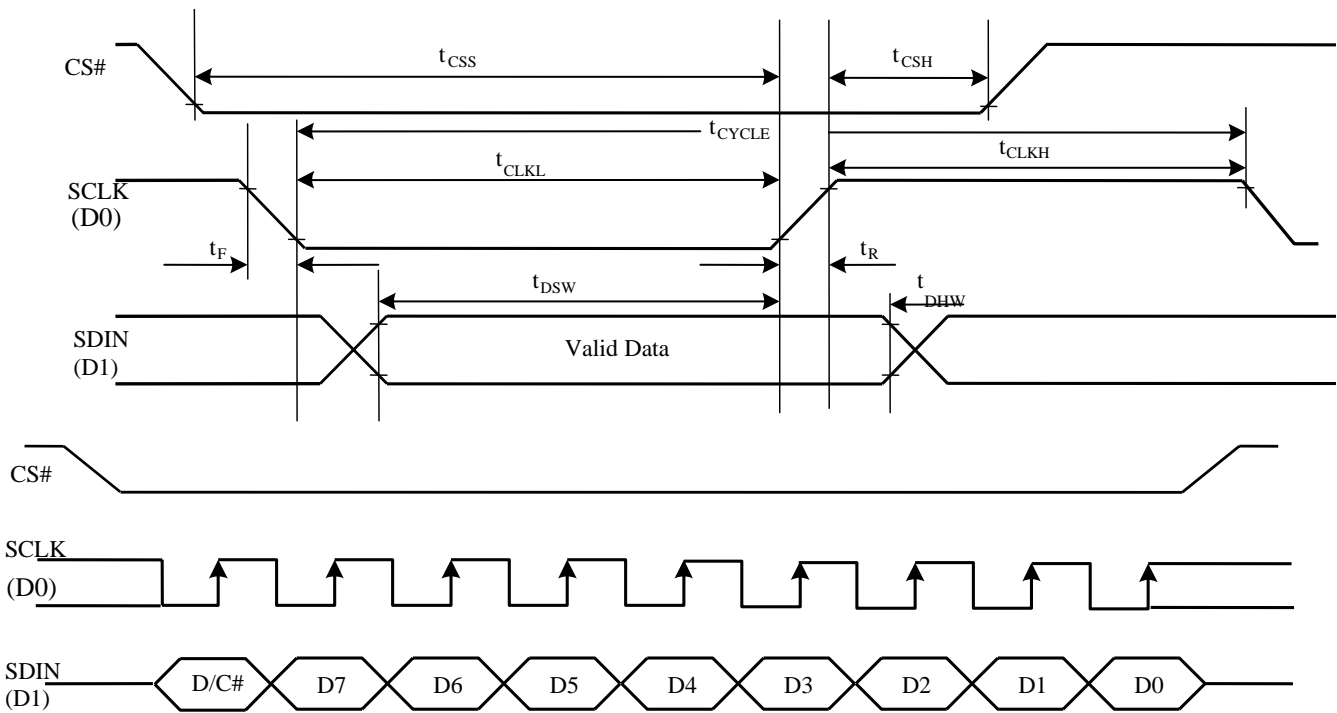
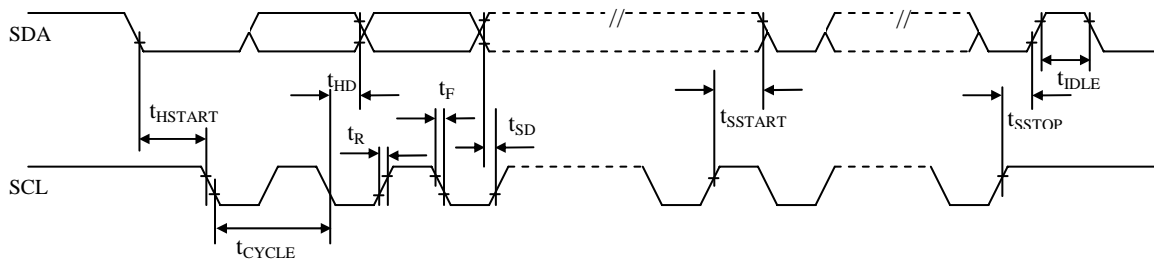


Table 13-6: I²C Interface Timing Characteristics

($V_{CI} - V_{SS} = 1.65V$ to $3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------|---|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 2.5 | - | - | us |
| t_{HSTART} | Start condition Hold Time | 0.6 | - | - | us |
| t_{HD} | Data Hold Time (for “SDA _{OUT} ” pin) | 0 | - | - | ns |
| | Data Hold Time (for “SDA _{IN} ” pin) | 300 | - | - | ns |
| t_{SD} | Data Setup Time | 100 | - | - | ns |
| t_{SSTART} | Start condition Setup Time (Only relevant for a repeated Start condition) | 0.6 | - | - | us |
| t_{SSTOP} | Stop condition Setup Time | 0.6 | - | - | us |
| t_R | Rise Time for data and clock pin | - | - | 300 | ns |
| t_F | Fall Time for data and clock pin | - | - | 300 | ns |
| t_{IDLE} | Idle Time before a new transmission can start | 1.3 | - | - | us |

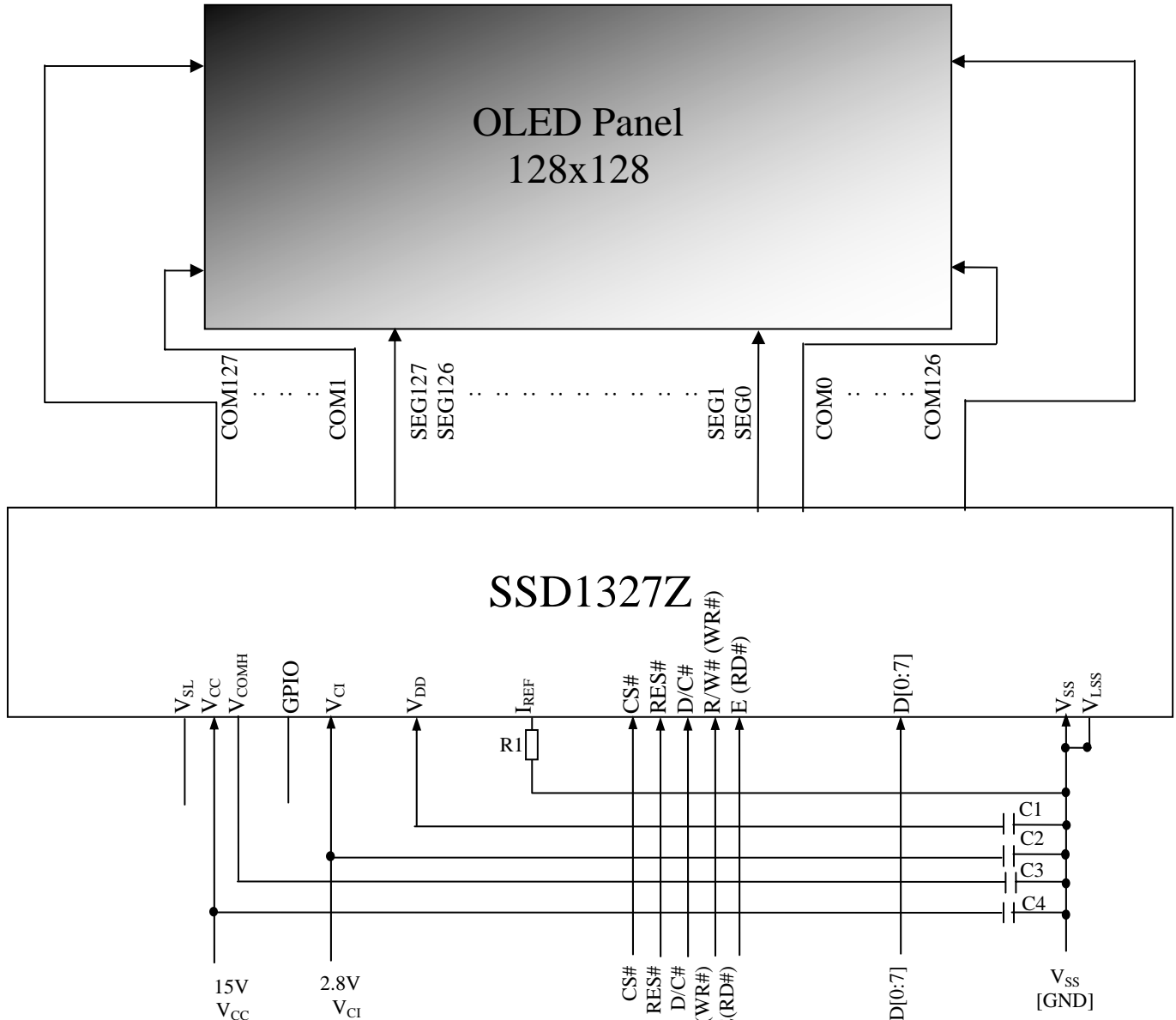
Figure 13-5: I²C interface Timing characteristics



14 APPLICATION EXAMPLES

Figure 14-1 : SSD1327Z application example for 8-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
 ($V_{CI} = 2.8V$ (V_{CI} must be $> 2.6V$), Internal regulated $V_{DD} = 2.5V$, external $V_{CC} = 15V$, $I_{REF} = 10\mu A$)



Voltage at $I_{REF} \approx V_{CC} - 3V$. For $V_{CC} = 15V$, $I_{REF} = 10\mu A$:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$\approx (15 - 3)V / 10\mu A = 1.2M\Omega$$

$$C1 = C2: 1\mu F^{(1)}, C3 = C4: 4.7\mu F^{(1)}$$

Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, CS#, RES#

Pin internally connected to V_{CI} : CLS, BS2

Pin internally connected to V_{SS} : V_{LSS} , BGGND, CL, BS1, BS0

Pin floated: GPIO⁽²⁾, VSL⁽²⁾, FR

Note

⁽¹⁾ The value is recommended value. Select appropriate value against module application.

⁽²⁾ Depends on module application.

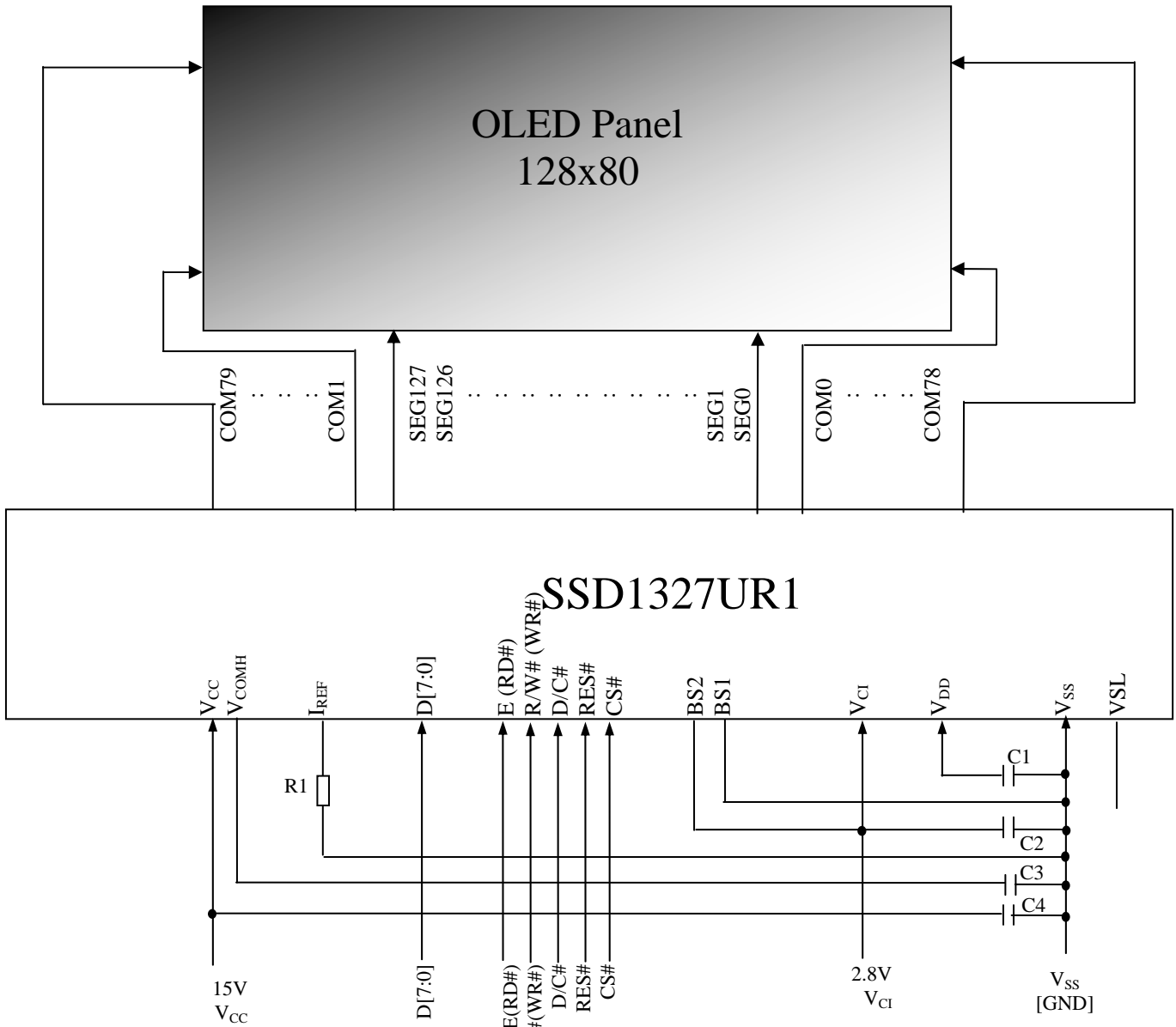
⁽³⁾ Die gold bump face up.

⁽⁴⁾ V_{LSS} of IC pad no. 29 to 85 are recommended to be connected to the V_{LSS} of pad no. 28 and 86 to form a larger area of GND.

⁽⁵⁾ V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level for better grounding and noise insulation.

Figure 14-2 : SSD1327UR1 application example for 8-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
 (V_{CI} = 2.8V (V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, external V_{CC} = 15V, I_{REF} = 10uA)



Voltage at I_{REF} ≈ V_{CC} - 3V.
 For V_{CC} = 15V, I_{REF} = 10uA:
 $R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$
 $\approx (15 - 3)V / 10\mu A = 1.2M\Omega$
 C1 = C2: 1uF⁽¹⁾, C3 = C4: 4.7uF⁽¹⁾

Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, CS#, RES#
 Pin internally connected to V_{CI}: CLS
 Pin internally connected to V_{SS}: V_{LSS}, BGGND, CL, BS0
 Pin floated: VSL⁽¹⁾

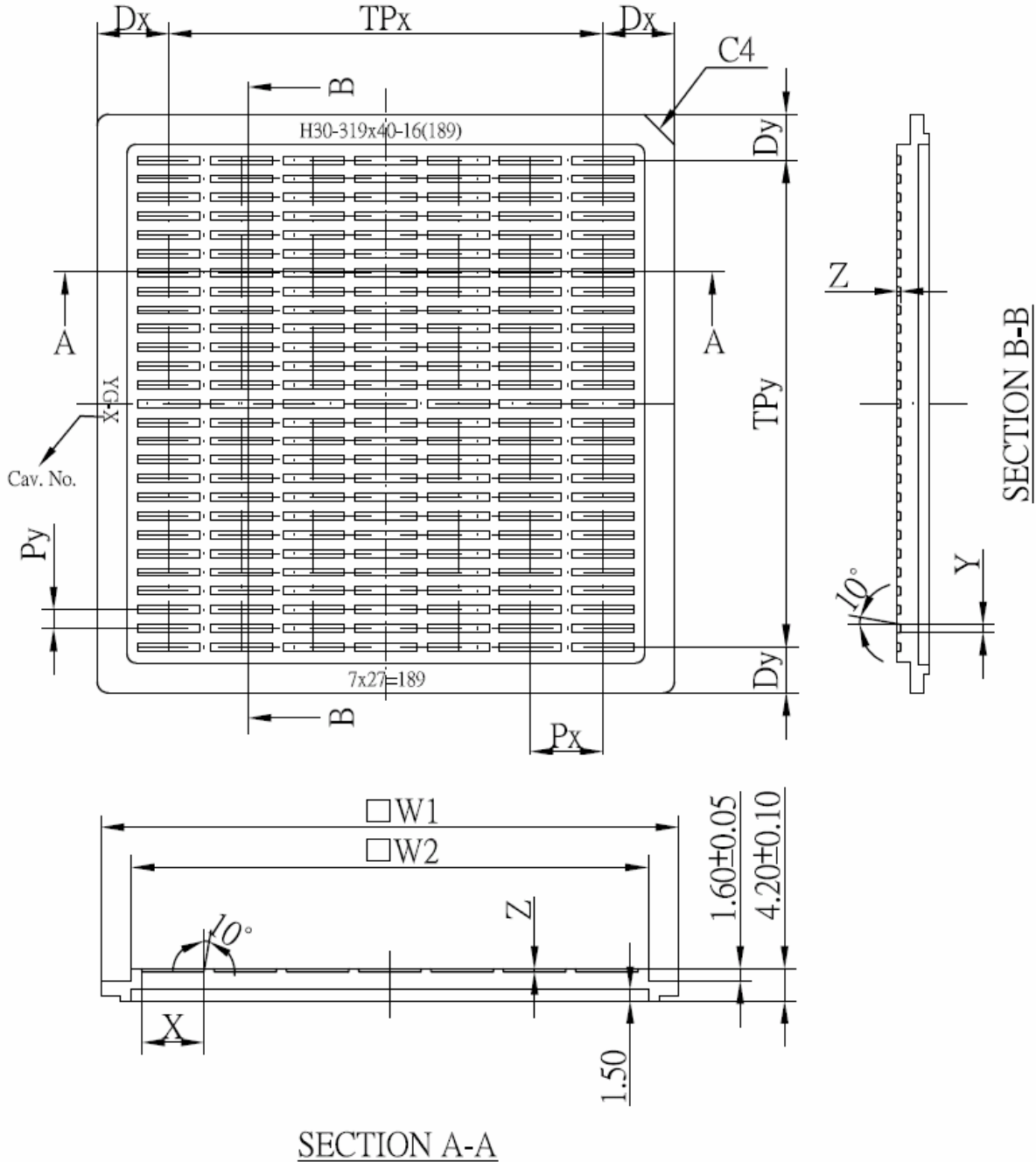
Note

⁽¹⁾ Depends on module application.
⁽²⁾ SSD1327UR1 (COF) with mirror design.

15 PACKAGE INFORMATION

15.1 SSD1327Z Die Tray Information

Figure 15-1: SSD1327Z Die Tray Drawing



Remark

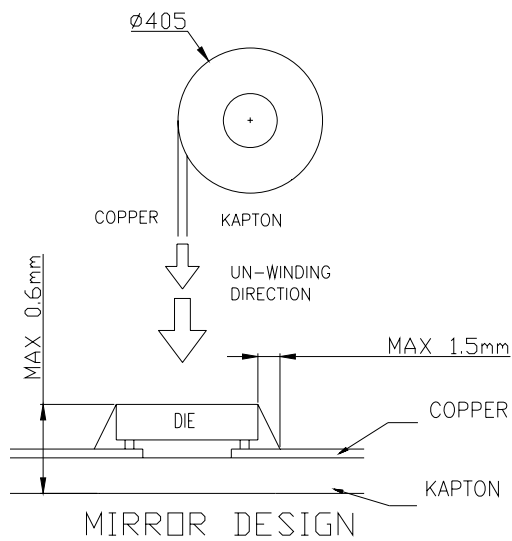
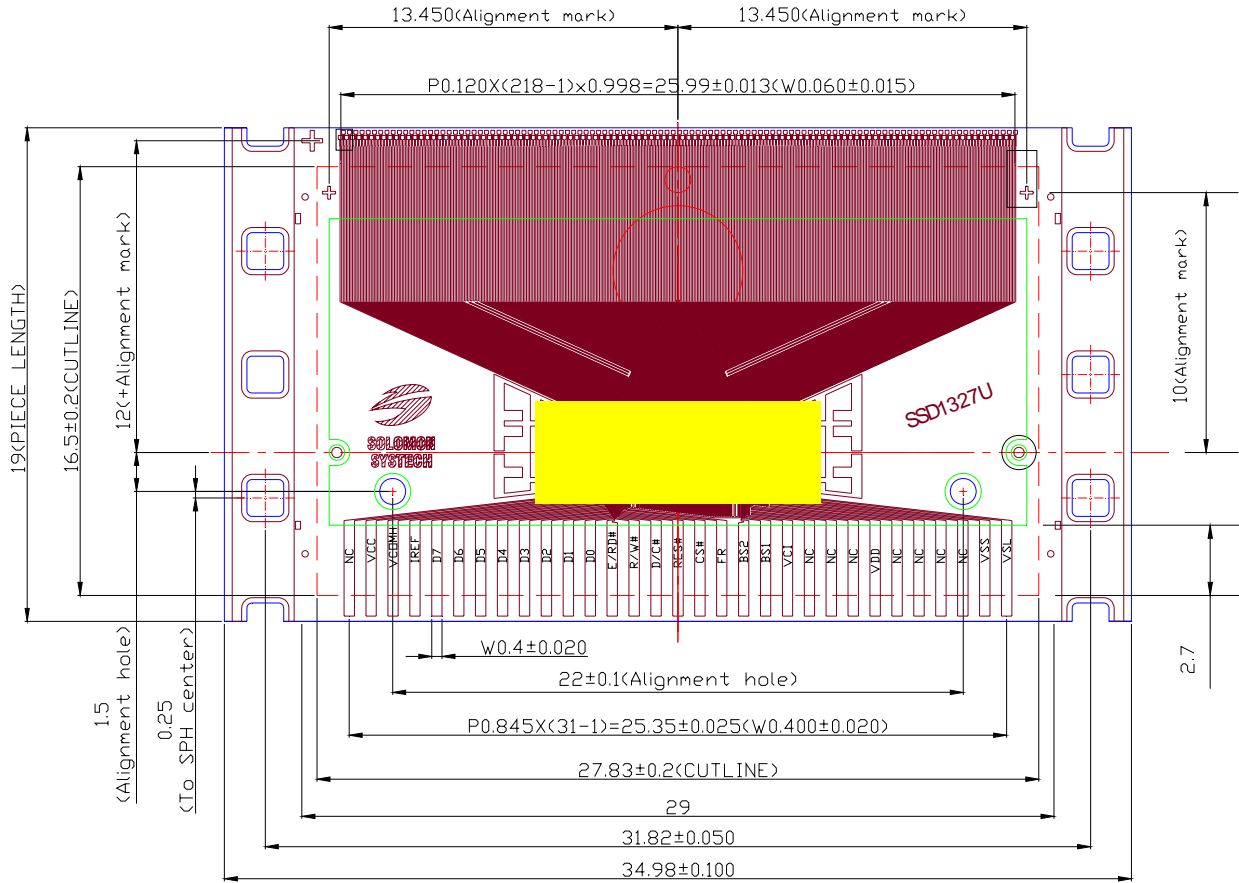
1. Tray material: Permanent Antistatic
2. Tray color code: Black
3. Surface resistance $10^9 \sim 10^{12} \Omega$
4. Pocket bottom: Rough Surface

Table 15-1: SSD1327Z Die Tray Dimensions

| Parameter | Dimensions | |
|-------------------|------------|--------|
| | mm | (mil) |
| W1 | 76.00±0.10 | (2992) |
| W2 | 68.00±0.10 | (2677) |
| W3 | 68.30±0.10 | (2689) |
| D _X | 9.44±0.10 | (372) |
| TP _X | 57.12±0.10 | (2249) |
| D _Y | 6.02±0.10 | (237) |
| TP _Y | 63.96±0.10 | (2518) |
| P _X | 9.52±0.05 | (375) |
| P _Y | 2.46±0.05 | (97) |
| X | 8.09±0.05 | (319) |
| Y | 1.02±0.05 | (40) |
| Z | 0.40±0.05 | (16) |
| | | |
| N (number of die) | 180 | |

15.2 SSD1327UR1 detail dimension


Figure 15-2: SSD1327UR1 Detail Dimension



NOTE:

- GENERAL TOLERANCE: $\pm 0.05\text{mm}$
- MATERIAL
 - PI: $38 \pm 4\mu\text{m}$
 - CU: $8 \pm 2\mu\text{m}$
 - SR: $10 \pm 5\mu\text{m}$
 - (OTHER TOLERANCE: $\pm 0.200\text{mm}$)
- Sn PLATING $0.20 \pm 0.050\mu\text{m}$
- TAP SITE: 4 SPH, 19mm
- Halogen free

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