

SPLC783A1

16COM/80SEG Controller/Driver

Preliminary

OCT. 02, 2007

Version 0.1

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16COM/80SEG CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPLC783A1, a dot-matrix LCD controller and driver from ORISE, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC783A1 provides two types of interfaces to MPU: 4-bit and 8-bit interfaces. The transferring speed of 8-bit is twice faster than 4-bit. A single SPLC783A1 is able to display up to two 16-character lines. By cascading with SPLC100 or SPLC063, the display capability can be extended. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

- Character generator ROM: 10880 bits
 - Character font 5 x 8 dots: 192 characters
- Character font 5 x 10 dots: 64 characters
- Character generator RAM: 512 bits
 - Character font 5 x 8 dots: 8 characters
 - Character font 5 x 10 dots: 4 characters
- 4-bit or 8-bit MPU interfaces
- Direct driver for LCD: 16 COMs x 80 SEGs
- Duty factor (selected by program):
 - 1/8 duty: 1 line of 5 x 8 dots
 - 1/11 duty: 1 line of 5 x 10 dots
 - 1/16 duty: 2 lines of 5 x 8 dots / line
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with external resistor)
- Support external clock operation
- Low Power Consumption
- Package form: bare chip available

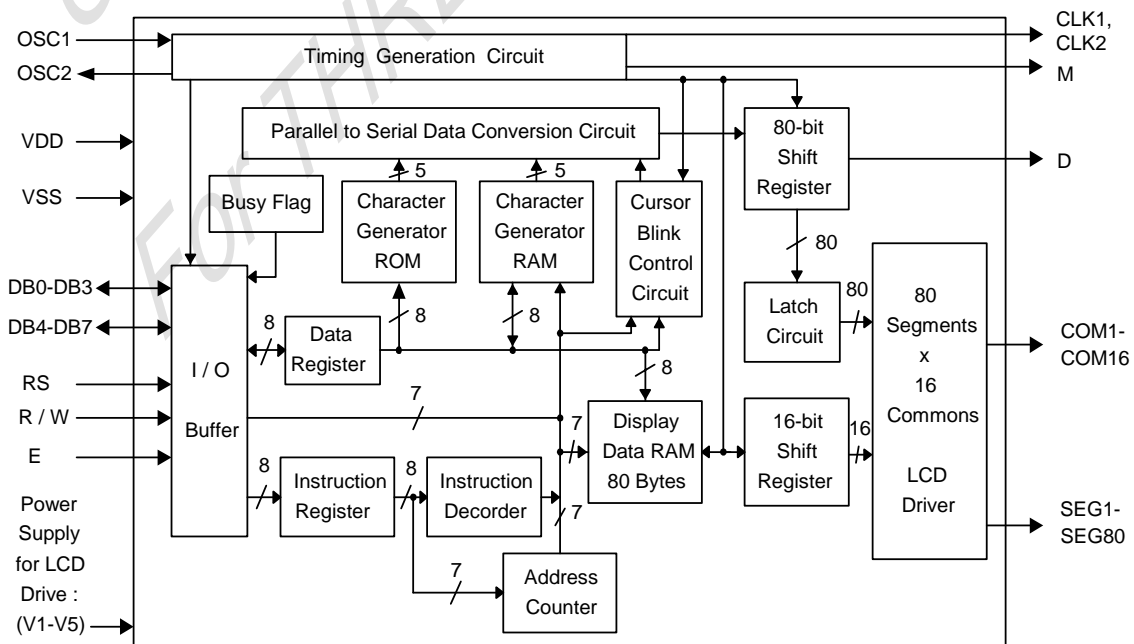
3. ORDERING INFORMATION

Product Number	Package Type
SPLC783A1-NnnV-C	Chip form
SPLC783A1-NnnV-HL111	Green Package form - LQFP 128

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	49	I	Power input
VSS	34	I	Ground
OSC1 OSC2	36 35	-	Both OSC1 and OSC2 are connected to resistor for internal oscillator circuit. For external clock operation, the clock is input to OSC1.
V1 - V5	37 - 41	I	Supply voltage for LCD driving.
E	48	I	A start signal for reading or writing data.
R/W	47	I	A signal for selecting read or write actions. 1: Read, 0: Write.
RS	46	I	A signal for selecting registers. 1: Data Register (for read and write) 0: Instruction Register (for write), Busy flag - Address Counter (for read).
DB0 - DB3	50 - 53	I/O	Low 4-bit data
DB4 - DB7	54 - 57	I/O	High 4-bit data
CLK1	42	O	Clock to latch serial data D.
CLK2	43	O	Clock to shift serial data D.
M	44	O	Switch signal to convert LCD waveform to AC.
D	45	O	Sends character pattern data corresponding to each common signal serially. 1: Selection, 0: Non-selection.
SEG1 - SEG33 SEG34 - SEG80	33 - 1 121 - 75	O	Segment signals for LCD.
COM1 - COM16	59 - 74	O	Common signals for LCD.
TEST	58	I	TEST pin. This pin must be fixed to VDD or open.

6. FUNCTIONAL DESCRIPTIONS

6.1. Oscillator

SPLC783A1 oscillator supports not only the internal oscillator operation, but also the external clock operation.

6.2. Control and Display Instructions

Control and display instructions are described in details as follows:

6.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the entire display and sets Display Data RAM Address 0 in Address Counter.

6.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets Display Data RAM Address 0 in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

6.2.3. Entry mode set

During writing and reading data, it defines cursor moving direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

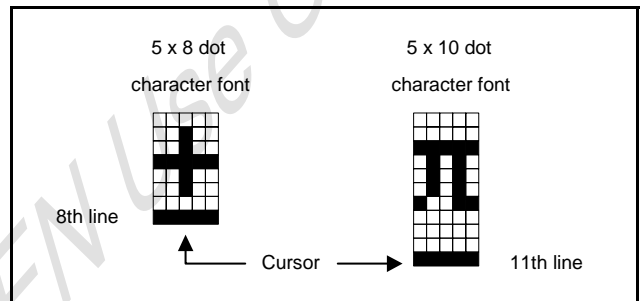
6.2.4. Display ON/OFF control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

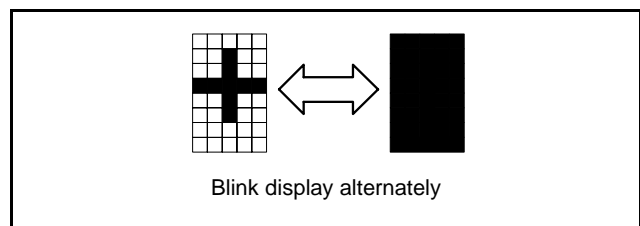
B = 1: Blinks on, B = 0: Blinks off



6.2.5. Cursor or display shift

Without changing DD RAM data, it moves cursor and shifts display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

6.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Data transferred with 8-bit length (DB7 - 0).

DL = 0: Data transferred with 4-bit length (DB7 - 4).

It requires two times to accomplish data transferring.

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

It cannot display two lines with 5 x 10 dots character font.

6.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

It sets Character Generator RAM Address (aaaaaa)₂ to the Address Counter.

Character Generator RAM data can be read or written after this setting.

6.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

It sets Display Data RAM Address (aaaaaa)₂ to the Address Counter.

Display data RAM can be read or written after this setting.

In one-line display (N = 0),

(aaaaaaa)₂: (00)₁₆ - (4F)₁₆.

In two-line display (N = 1),

(aaaaaaa)₂: (00)₁₆ - (27)₁₆ for the first line,

(aaaaaaa)₂: (40)₁₆ - (67)₁₆ for the second line.

6.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	a	a	a	a	a	a	a

When BF = 1, it indicates the system is busy now and it will not accept any instruction until not busy (BF = 0). At the same time, the content of Address Counter (aaaaaaa)₂ is read.

6.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes data (ddddddd)₂ to character generator RAM or display data RAM.

6.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads data (ddddddd)₂ from character generator RAM or display data RAM.

To read data correctly, do the following:

- 1). The address of the Character Generator RAM or Display Data RAM or shift the cursor instruction.
- 2). The "Read" instruction.

6.3. Instruction Table

Instruction	Instruction Code										Description	Execution time			
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Fosc= 190KHz	Fosc= 270KHz	Fosc= 350KHz	
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	2.16ms	1.52ms	1.18ms
Return Home	0	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	2.16ms	1.52ms	1.18ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	53μs	38μs	29μs
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.	53μs	38μs	29μs
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	53μs	38μs	29μs
Function Set	0	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	53μs	38μs	29μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address counter.	53μs	38μs	29μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address counter	53μs	38μs	29μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.			
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs

Note: "-": don't care

6.4. 8-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC783A1 starts initializing)	<input type="text"/>	Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 <input type="text" value="0 0 0 0 1 1 0 0 X X"/>	<input type="text"/>	Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control <input type="text" value="0 0 0 0 0 0 1 1 1 0"/>	<input type="text" value="-"/>	Display on. Cursor appear.
4	Entry mode set <input type="text" value="0 0 0 0 0 0 0 1 1 0"/>	<input type="text" value="-"/>	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 1 0 1 1 1"/>	<input type="text" value="W_"/>	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 1 0 1"/>	<input type="text" value="WE_"/>	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 1 0 1"/>	<input type="text" value="WELCOME_"/>	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set <input type="text" value="0 0 0 0 0 0 0 1 1 1"/>	<input type="text" value="WELCOME_"/>	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 0 1 0 0 0 0 0"/>	<input type="text" value="ELCOME _"/>	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 0 1 1"/>	<input type="text" value="LCOME C_"/>	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 1 1 0 0 1"/>	<input type="text" value="COMPAMY_"/>	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift <input type="text" value="0 0 0 0 0 1 0 0 X X"/>	<input type="text" value="COMPAMY_"/>	Only shift the cursor's position to the left (Y).
15	Cursor or display shift <input type="text" value="0 0 0 0 0 1 0 0 X X"/>	<input type="text" value="COMPAMY_"/>	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 1 1 1 0"/>	<input type="text" value="OMPANY_"/>	Write " N ". The display moves to the left.
17	Cursor or display shift <input type="text" value="0 0 0 0 0 1 1 1 X X"/>	<input type="text" value="COMPAMY_"/>	Shift the display and the cursor's position to the right.
18	Cursor or display shift <input type="text" value="0 0 0 0 0 1 0 1 X X"/>	<input type="text" value="OMPANY_"/>	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 0 0 0"/>	<input type="text" value="COMPAMY_"/>	Write " "(space). The cursor is incremented by one and shifted to the right.
20	:	:	:
21	Return home <input type="text" value="0 0 0 0 0 0 0 0 1 0"/>	<input type="text" value="WELCOME_"/>	Both the display and the cursor return to the original position (address 0).

6.5. 4-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation												
1	Power on. (SPLC783A1 starts initializing)	<input type="text"/>	Power on reset. No display.												
2	Function set RS R/W DB7 DB6 DB5 DB4 <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	0	0	0	0	1	0	<input type="text"/>	Set to 4-bit operation.						
0	0	0	0	1	0										
3	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td></tr></table>	0	0	0	0	1	0	0	0	0	0	X	X	<input type="text"/>	Set to 4-bit operation and select 1-line display line and character font.
0	0	0	0	1	0										
0	0	0	0	X	X										
4	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	1	1	1	0	<input type="text" value="-"/>	Display on. Cursor appears.
0	0	0	0	0	0										
0	0	1	1	1	0										
5	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	0	1	1	0	<input type="text" value="-"/>	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
0	0	0	0	0	0										
0	0	0	1	1	0										
6	<table border="1"><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table>	1	0	0	1	0	1	1	0	0	1	1	1	<input type="text" value="W_"/>	Write " W ". The cursor is incremented by one and shifted to the right.
1	0	0	1	0	1										
1	0	0	1	1	1										

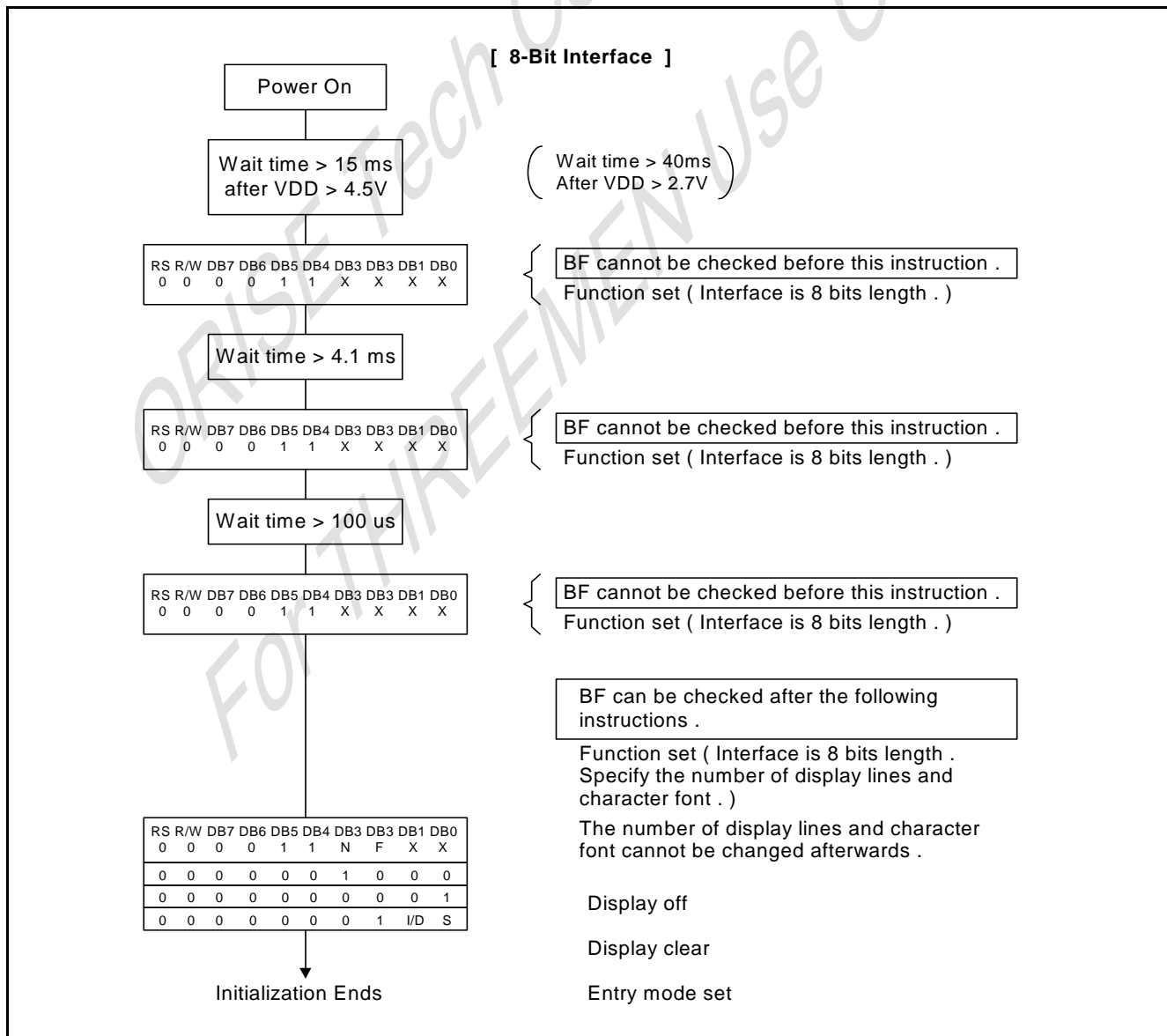
6.6. 8-Bit Operation and 8-Digit 2-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation										
1	Power on. (SPLC783A1 starts initializing)	<input type="text"/>	Power on reset. No display.										
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>X</td><td>X</td></tr></table>	0	0	0	0	1	1	1	0	X	X	<input type="text"/>	Set to 8-bit operation and select 2-line display line and 5 x 8 dot character font.
0	0	0	0	1	1	1	0	X	X				
3	Display on / off control <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	1	1	1	0	<input type="text" value="-"/>	Display on. Cursor appear.
0	0	0	0	0	0	1	1	1	0				
4	Entry mode set <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	0	1	1	0	<input type="text" value="-"/>	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
0	0	0	0	0	0	0	1	1	0				
5	Write data to CG RAM / DD RAM <table border="1"><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table>	1	0	0	1	0	1	0	1	1	1	<input type="text" value="W_"/>	Write " W ". The cursor is incremented by one and shifted to the right.
1	0	0	1	0	1	0	1	1	1				
6	:	:	:										
7	Write data to CG RAM / DD RAM <table border="1"><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr></table>	1	0	0	1	0	0	0	1	0	1	<input type="text" value="WELCOME_"/>	Write " E ". The cursor is incremented by one and shifted to the right.
1	0	0	1	0	0	0	1	0	1				
8	Set DD RAM address <table border="1"><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	1	1	0	0	0	0	0	0	<input type="text" value="WELCOME"/> <input type="text" value="-"/>	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
0	0	1	1	0	0	0	0	0	0				
9	Write data to CG RAM / DD RAM <table border="1"><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table>	1	0	0	1	0	1	0	1	0	0	<input type="text" value="WELCOME"/> <input type="text" value="T_"/>	Write " T ". The cursor is incremented by one and shifted to the right.
1	0	0	1	0	1	0	1	0	0				
10	:	:	:										
11	Write data to CG RAM / DD RAM <table border="1"><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table>	1	0	0	1	0	1	0	1	0	0	<input type="text" value="WELCOME"/> <input type="text" value="TO PART_"/>	Write " T ". The cursor is incremented by one and shifted to the right.
1	0	0	1	0	1	0	1	0	0				

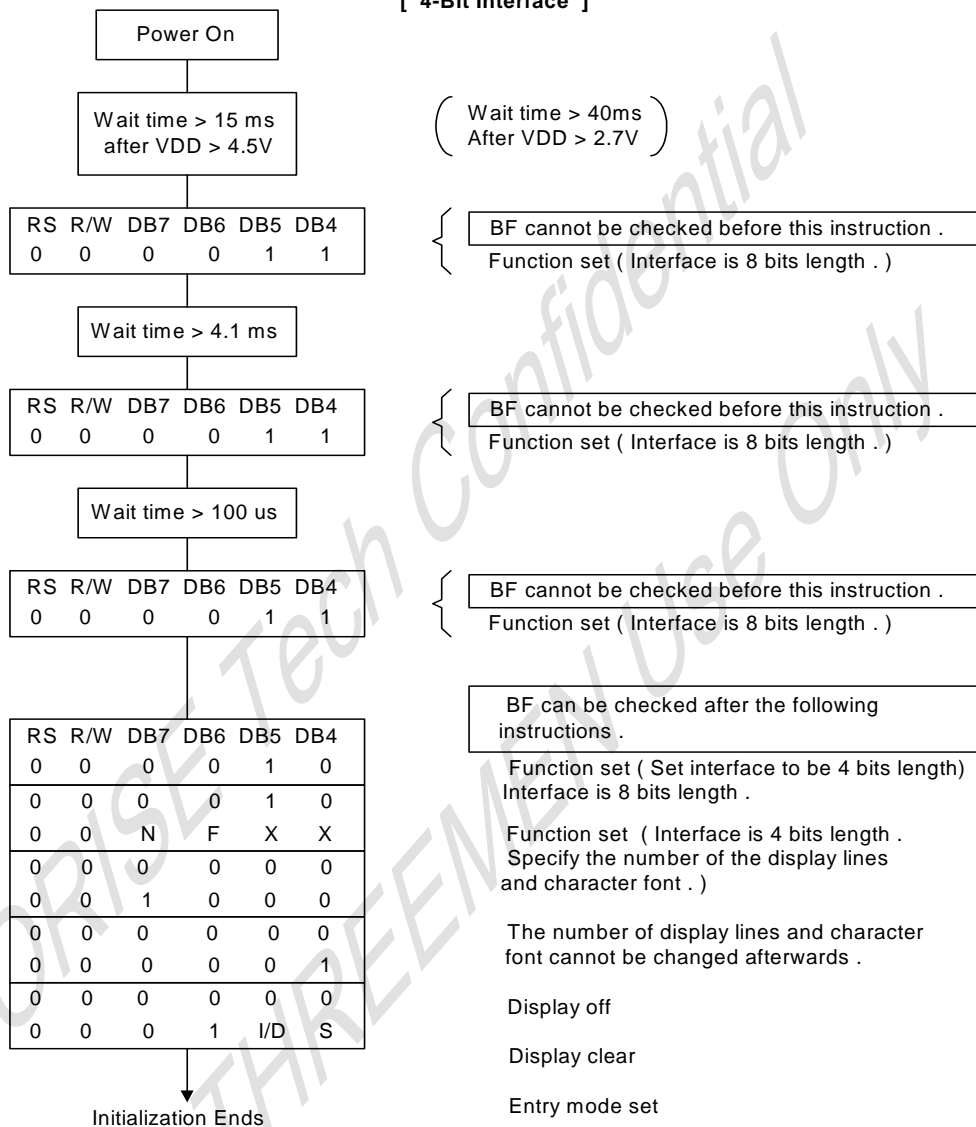
No.	Instruction	Display	Operation
12	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing, it sets mode for the display shift.
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
14	:	:	:
15	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

6.7. RESET Function

At power on, SPLC783A1 starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows:



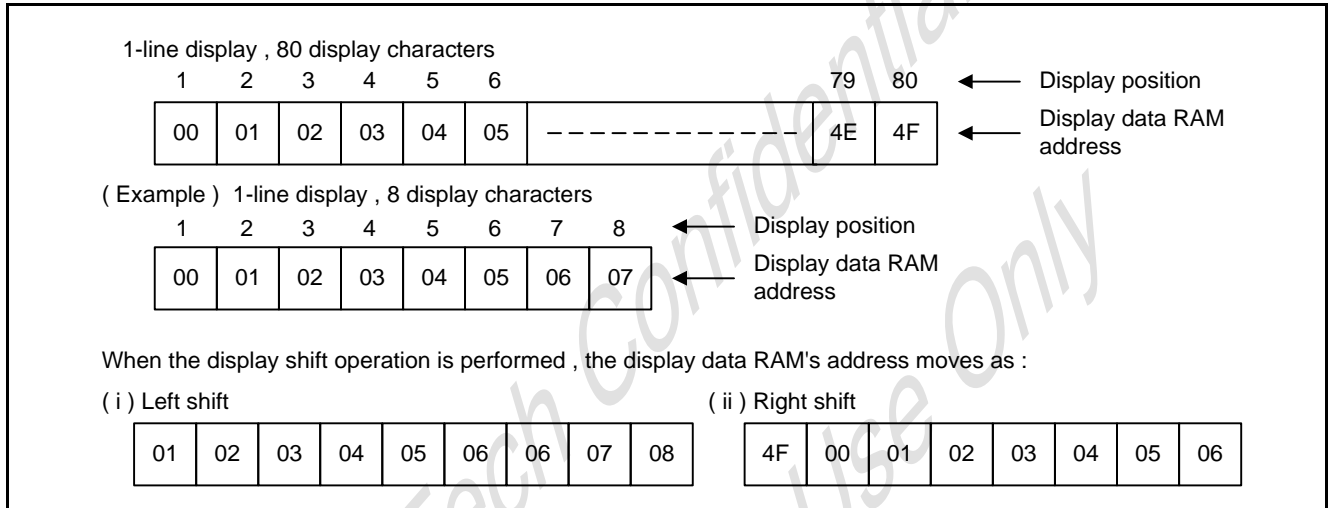
[4-Bit Interface]



6.8. Display Data RAM (DD RAM)

The 80-bit DD RAM is normally used for storing display data. Those DD RAM not used for display data can be used as general data RAM. Its address is configured in the Address Counter.

The relationships between Display Data RAM Address and LCD's position are depicted as follows.



6.9. Timing Generation Circuit

The timing generating circuit is able to generate timing signals to the internal circuits. In order to prevent the internal timing interface, the MPU access timing and the RAM access timing are generated independently.

6.10. LCD Driver Circuit

Total of 16 commons and 80 segments signal drivers are valid in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals output drive-waveforms and the others still output unselected waveforms.

6.11. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 8 dots or 5 x 10 dots character patterns. It also can generate 192's 5 x 8 dots character patterns and 64's 5 x 10 dots character patterns.

6.12. Character Generator RAM (CG RAM)

Users can easily change the character patterns in the character generator RAM through program. It can be written to 5 x 8 dots, 8-character patterns or 5 x 10 dots for 4-character patterns.

The following diagram shows the SPLC783A1 character patterns:

Correspondence between Character Codes and Character Patterns.

		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)																
	1	CG RAM (2)																
	2	CG RAM (3)																
	3	CG RAM (4)																
	4	CG RAM (5)																
	5	CG RAM (6)																
	6	CG RAM (7)																
	7	CG RAM (8)																
	8	CG RAM (1)																
	9	CG RAM (2)																
	A	CG RAM (3)																
	B	CG RAM (4)																
	C	CG RAM (5)																
	D	CG RAM (6)																
	E	CG RAM (7)																
	F	CG RAM (8)																

The relationships between Character Generator RAM Addresses, Character Generator RAM Data (character patterns), and Character Codes are depicted as follows:

1. 5 x 8 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	1	1	1	1	1
					0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0
					0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
					0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0
					1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
					1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0	0
					1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0
					1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
0	0	0	0	X	0	0	1	0	0	1	0	0	0	X	X	X	0	1	1	1	0
					0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0
					0	1	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0
					0	1	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0
					1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0
					1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	0	0
					1	1	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0
					1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Character Pattern Example (1)

Cursor Position ←

Character Pattern Example (2)

- Note1:** It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.
- Note2:** These areas are not used for display, but can be used for the general data RAM.
- Note3:** When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.
- Note4:** " 1 " : Selected , " 0 " : No selected , " X " : Do not care (0 or 1).
- Note5:** For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.
- Note6:** The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

2). 5 X 10 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
										0	0	0	0				1	0	0	0	1
										0	0	0	1				1	0	0	0	1
										0	0	1	0				1	0	0	0	1
										0	0	1	1				1	0	0	0	1
										0	1	0	0				1	0	0	0	1
0	0	0	0	X	0	0	X	0	0	0	1	0	1	X	X	X	1	0	0	0	1
										0	1	1	0				1	0	0	0	1
										0	1	1	1				1	0	0	0	1
										1	0	0	0				1	0	0	0	1
										1	0	0	1				1	1	1	1	1
										1	0	1	0				0	0	0	0	0
										1	0	1	1								
										1	1	0	0								
										1	1	0	1	X	X	X	X	X	X	X	X
										1	1	1	0								
										1	1	1	1								

Character Pattern Example (1)

Cursor Position ←

Note1:  It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

Note2:  These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: "1": Selected, "0": No selected, "X": Do not care (0 or 1).

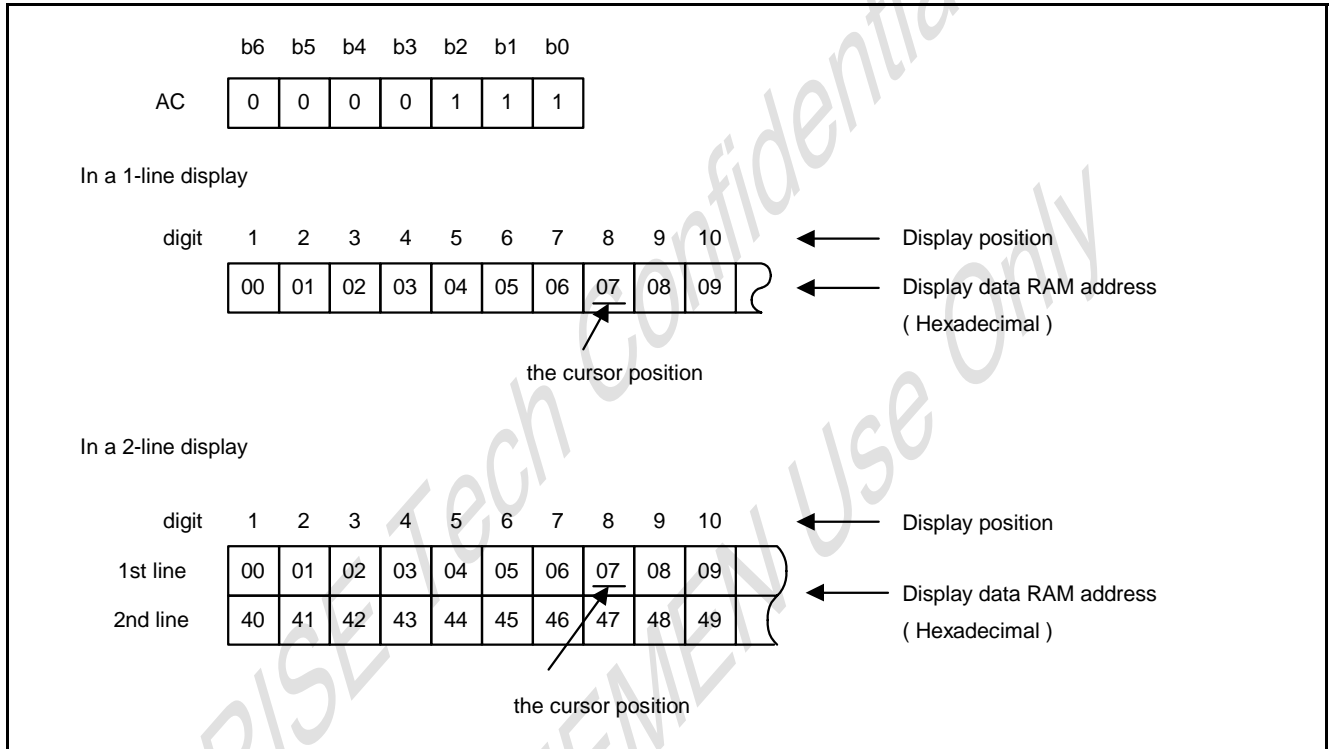
Note5: For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display "U". That means all of the character codes (00) 16, (01) 16, (08) 16, and (09) 16 can display "U" character.

Note6: The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

6.13. Cursor/Blink Control Circuit

This circuit generates the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the Display Data RAM Address defined in the Address Counter.

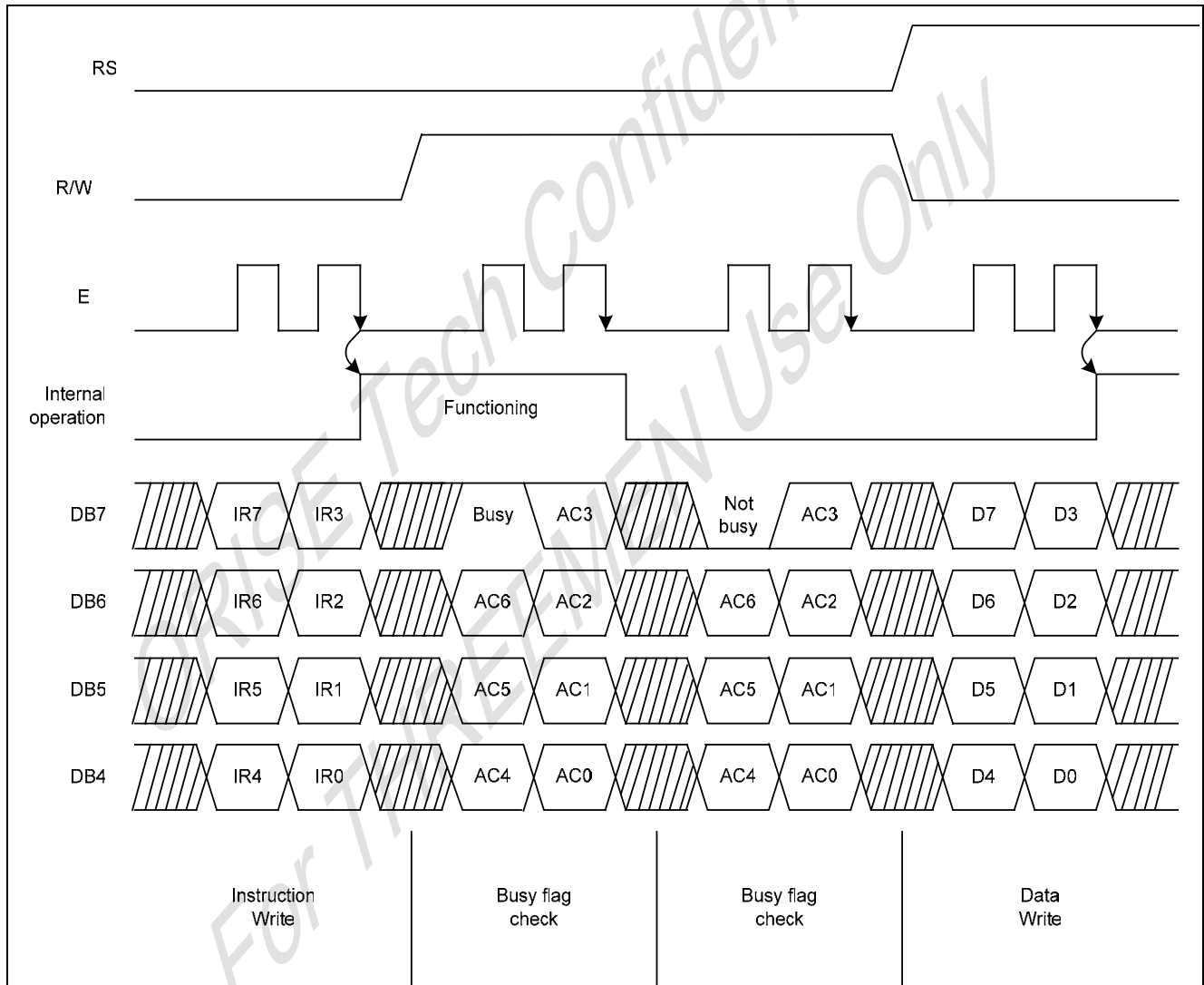
When the Address Counter is (07) 16, the cursor position is shown as belows:



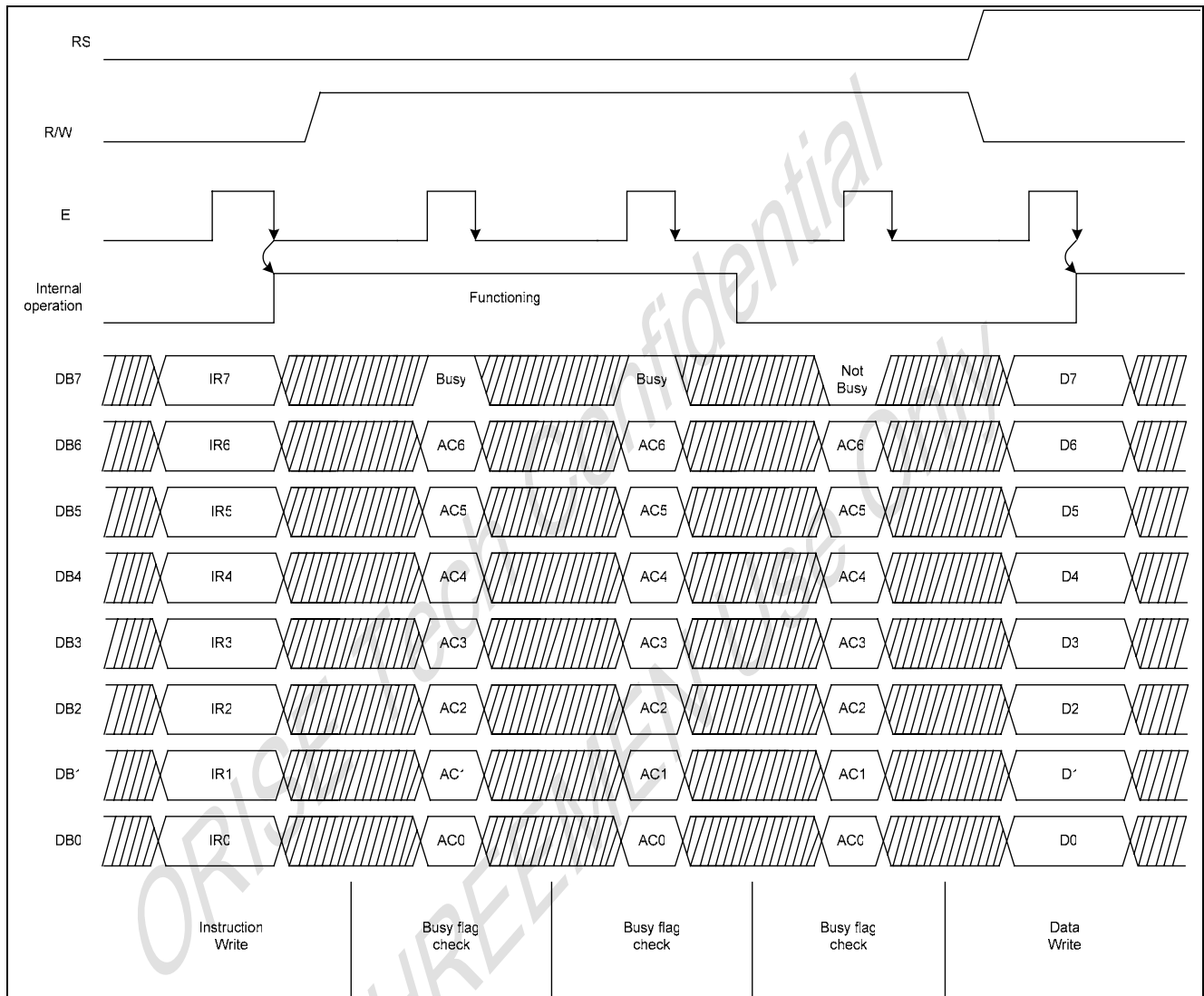
6.14. Interfacing to MPU

There are two types of data operations: 4-bit and 8-bit operations. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4-busline (DB4 to DB7). Thus, DB0 to DB3 bus lines are not used. Using 4-bit MPU to interface 8-bit data requires two times transferring. First, the higher 4-bit data is transferred by

4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4-busline (for 8-bit operation, DB3 to DB0). For 8-bit MPU, the 8-bit data is transferred by 8-buslines (DB0 to DB7).



Example of 4-bit Data Transfer Timing Sequence



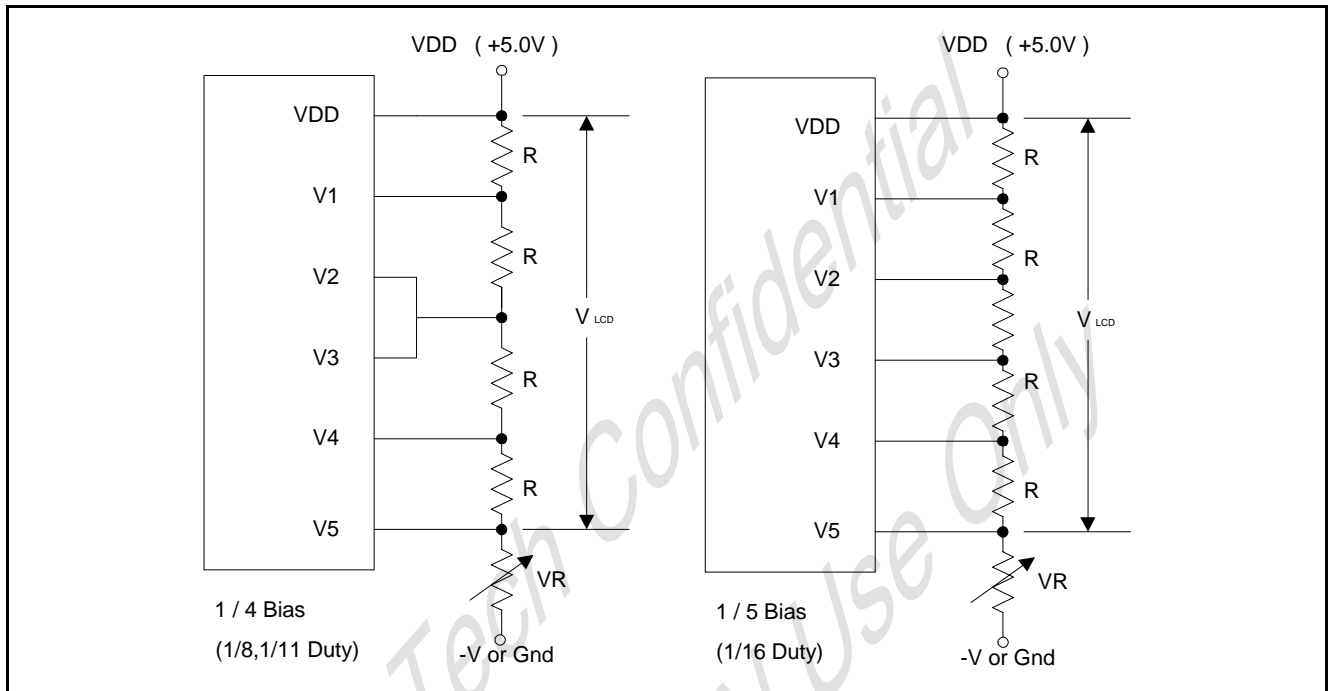
Example of 8-bit Data Transfer Timing Sequence

6.15. Supply Voltage for LCD Drive

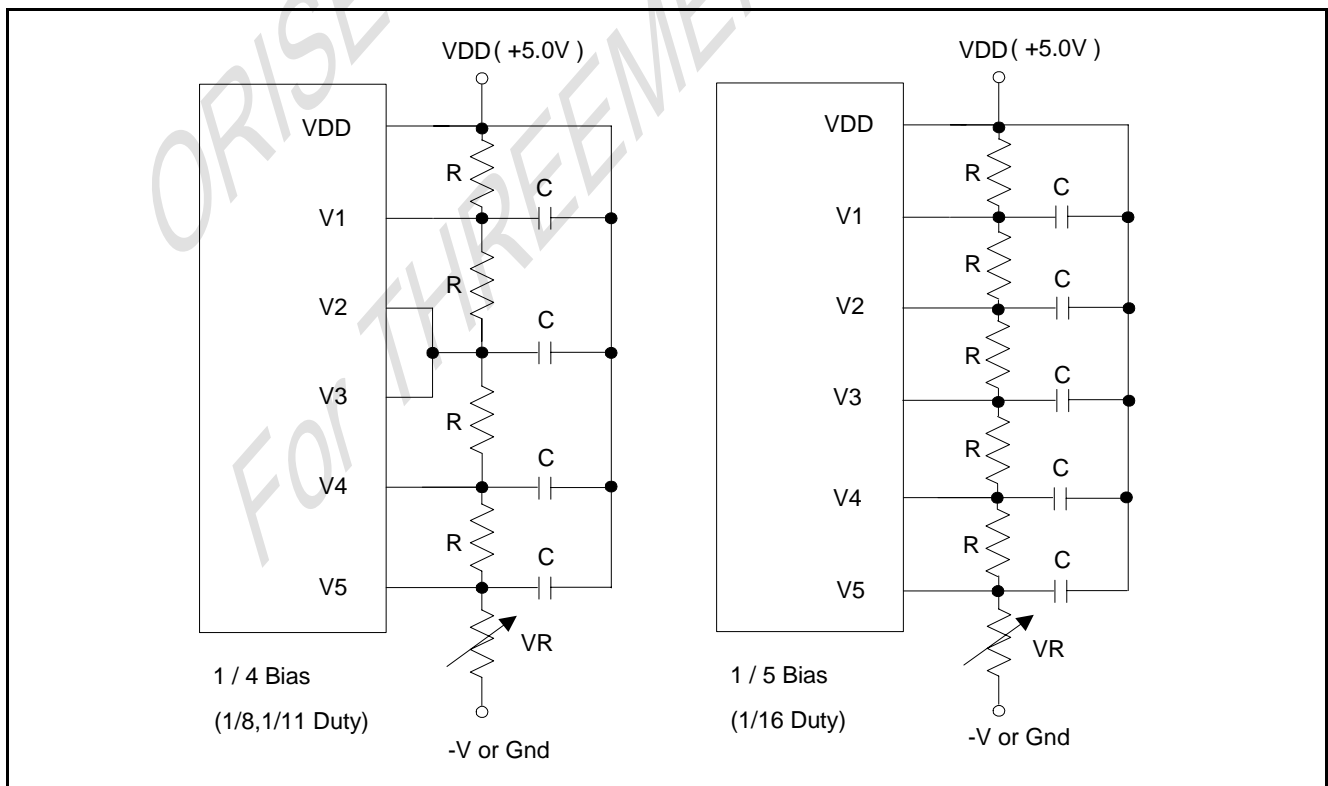
Different voltages can be supplied to SPLC783A1's pins (V5 - 1) for obtaining LCD drive-waveform. The relationships between bias, duty factor and supply voltages are shown as follows:

Supply Voltage	Duty Factor	1/8, 1/11	1/16
		1/4	1/5
V1		$VDD - 1/4 V_{LCD}$	$VDD - 1/5 V_{LCD}$
V2		$VDD - 1/2 V_{LCD}$	$VDD - 2/5 V_{LCD}$
V3		$VDD - 1/2 V_{LCD}$	$VDD - 3/5 V_{LCD}$
V4		$VDD - 3/4 V_{LCD}$	$VDD - 4/5 V_{LCD}$
V5		$VDD - V_{LCD}$	$VDD - V_{LCD}$

6.15.1. The power connections for LCD (1/4 Bias, 1/5 Bias) are shown belows:



The bypass-capacitor improves the LCD display quality.



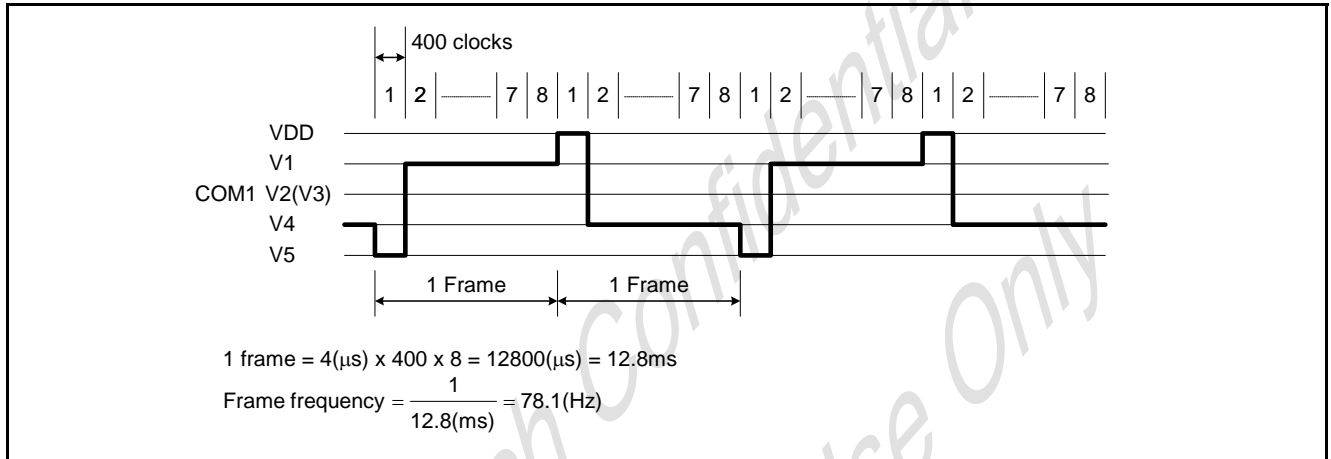
The bias voltage must have the following relations:

$$VDD > V1 > V2 \geq V3 > V4 > V5.$$

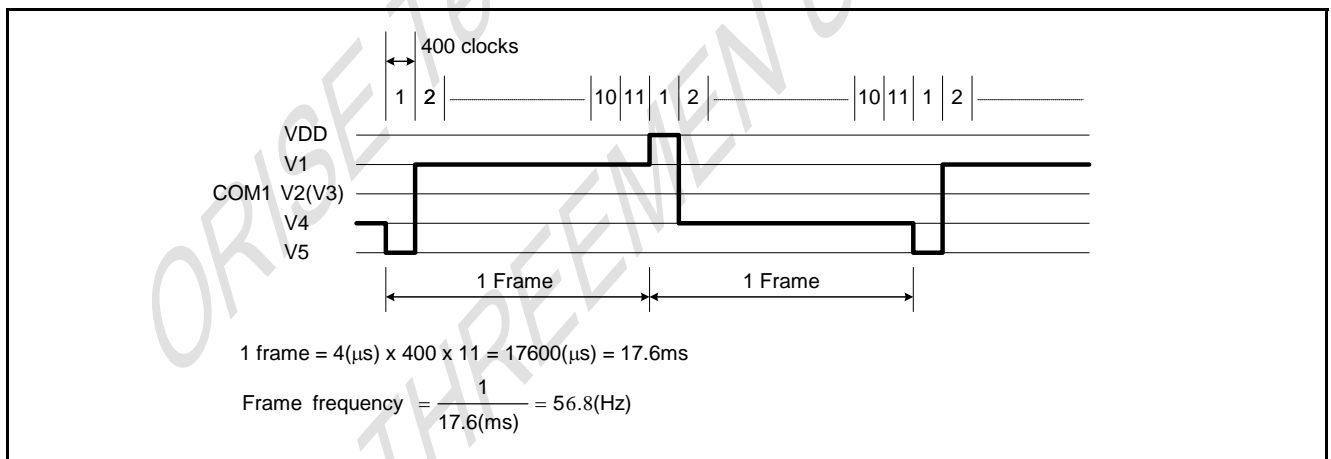
6.15.2. The relationship between LCD frame's frequency and oscillator's frequency.

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0μs)

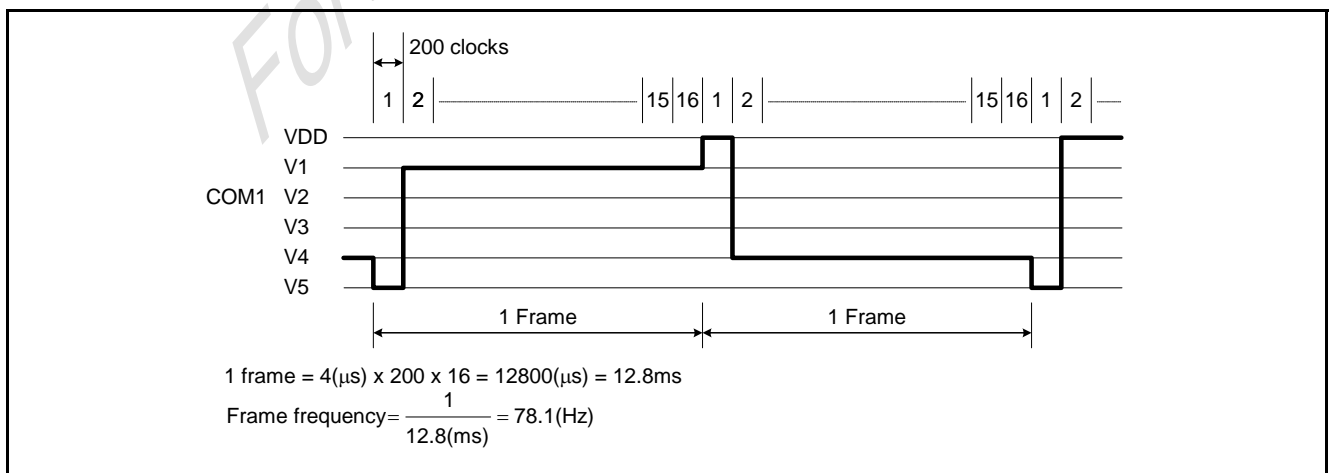
6.15.2.1. 1/8 duty, TYPE-B waveform



6.15.2.2. 1/11 duty, TYPE-B waveform



6.15.2.3. 1/16 duty, TYPE-B waveform



6.16. REGISTER --- IR (Instruction Register) and DR (Data Register)

SPLC783A1 contains two 8-bit registers: Instruction Register (IR) and Data Register (DR). Using combinations of the RS pin and the R/W pin selects the IR and DR, see below:

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and Address Counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

The IR can be written by MPU, but it cannot be read by MPU.

6.17. Busy Flag (BF)

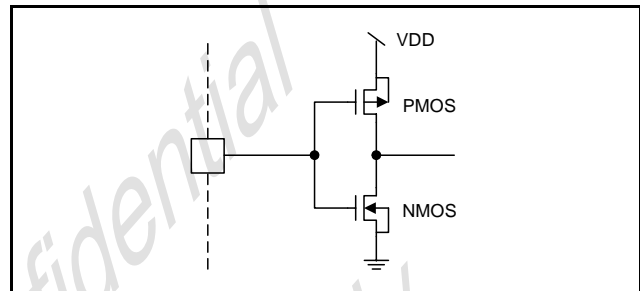
When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag = 1, SPLC783A1 is in busy state and does not accept any instruction until the busy flag = 0.

6.18. Address Counter (AC)

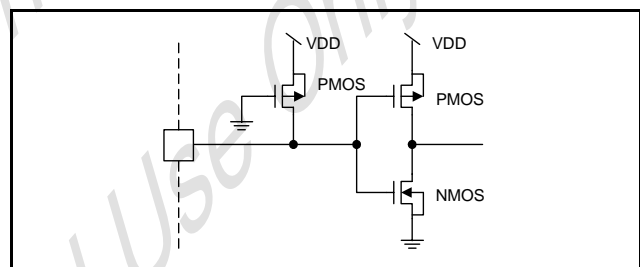
The Address Counter assigns addresses to Display Data RAM and Character Generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing to/reading from Display Data RAM or Character Generator RAM, AC is automatically incremented by one (or decremented by one). The contents of AC are output to DB0 - DB6 when RS = 0 and R/W = 1.

6.19. I/O Port Configuration

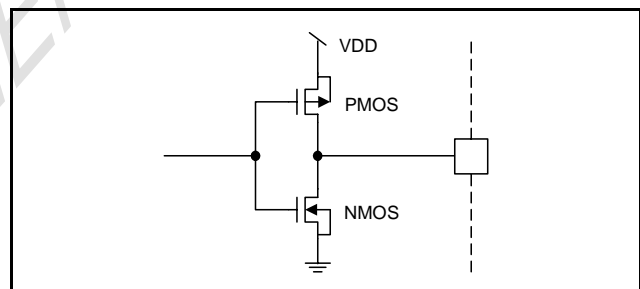
6.19.1. Input port: E



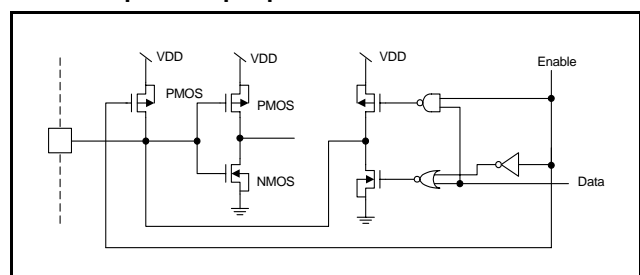
6.19.2. Input port: R / W, RS



6.19.3. Output port: CLK1, CLK2, M, D



6.19.4. Input / Output port: DB7 - 0



7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V _{LCD}	VDD - 12V to VDD + 0.3V
Input Voltage Range	V _{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T _A	-30°C to +80°C
Storage Temperature	T _{STO}	-55°C to +125°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 2.7V to 4.5V, T_A = 25°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I _{DD}	-	0.2	0.4	mA	External clock (Note)
Input High Voltage	V _{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V _{IL1}	-0.3	-	0.4	V	
Input High Voltage	V _{IH2}	0.7VDD	-	VDD	V	Pin OSC1
Input Low Voltage	V _{IL2}	-0.2	-	0.2VDD	V	
Input High Current	I _{IH}	-1.0	-	1.0	μA	Pins: (RS, R/W, DB0 - DB7) VDD = 3.0V
Input Low Current	I _{IL}	-5.0	-15	-30	μA	
Output High Voltage (TTL)	V _{OH1}	2.0	-	-	V	I _{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V _{OL1}	-	-	0.2VDD	V	I _{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V _{OH2}	0.8VDD	-	-	V	I _{OH} = - 40μA, Pins: CLK1, CLK2, M, D
Output Low Voltage (CMOS)	V _{OL2}	-	-	0.2VDD	V	I _{OL} = 40μA, Pins: CLK1, CLK2, M, D
Driver ON Resistance (COM)	R _{COM}	-	-	10	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R _{SEG}	-	-	15	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: SEG1 - SEG80
LCD Voltage	V _{LCD}	3.0	-	11	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{osc} = 270KHz, VDD = 3.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

7.3. AC Characteristics (VDD = 2.7V to 4.5V, T_A = 25°C)
7.3.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F _{OSC1}	190	270	350	KHz	VDD = 3.0V, Rf = 75KΩ±2%

7.3.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F _{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t _r , t _f	-	-	0.2	μs	

7.3.3. Write mode (Writing data from MPU to SPLC783A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t _C	1400	-	-	ns	Pin E
E Pulse Width	t _{PW}	400	-	-	ns	Pin E
E Rise/Fall Time	t _R , t _F	-	-	25	ns	Pin E
Address Setup Time	t _{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t _{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t _{SP2}	140	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t _{HD2}	10	-	-	ns	Pins: DB0 - DB7

7.3.4. Read mode (Reading data from SPLC783A1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t _C	1400	-	-	ns	Pin E
E Pulse Width	t _W	400	-	-	ns	Pin E
E Rise/Fall Time	t _R , t _F	-	-	25	ns	Pin E
Address Setup Time	t _{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t _{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t _O	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t _{HD2}	5.0	-	-	ns	Pin DB0 - DB7

7.4. DC Characteristics (VDD = 4.5V to 5.5V, TA = 25°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I _{DD}	-	0.4	0.6	mA	External clock (Note)
Input High Voltage	V _{IH1}	2.2	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V _{IL1}	-0.3	-	0.6	V	
Input High Voltage	V _{IH2}	VDD-1	-	VDD	V	Pin OSC1
Input Low Voltage	V _{IL2}	-0.2	-	1.0	V	Pin OSC1
Input High Current	I _{IH}	-1.0	-	1.0	μA	Pins: (RS, R/W, DB0 - DB7) VDD = 5.0V
Input Low Current	I _{IL}	-20	-50	-100	μA	
Output High Voltage (TTL)	V _{OH1}	2.4	-	VDD	V	I _{OH} = -0.205mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V _{OL1}	-	-	0.4	V	I _{OL} = 1.2mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V _{OH2}	0.9VDD	-	VDD	V	I _{OH} = -40μA, Pins: CLK1, CLK2, M, D
Output Low Voltage (CMOS)	V _{OL2}	-	-	0.1VDD	V	I _{OL} = 40μA, Pins: CLK1, CLK2, M, D
Driver ON Resistance (COM)	R _{COM}	-	-	10K	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R _{SEG}	-	-	15K	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: SEG1 - SEG80
LCD Voltage	V _{LCD}	3.0	-	11	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{OSC} = 270KHz, VDD = 5.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

7.5. AC Characteristics (VDD = 4.5V to 5.5V, TA = 25°C)

7.5.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F _{OSC1}	190	270	350	KHz	VDD = 5.0V, Rf = 91KΩ±2%

7.5.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F _{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	tr, tf	-	-	0.2	μs	

7.5.3. Write mode (Writing Data from MPU to SPLC783A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	220	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	60	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

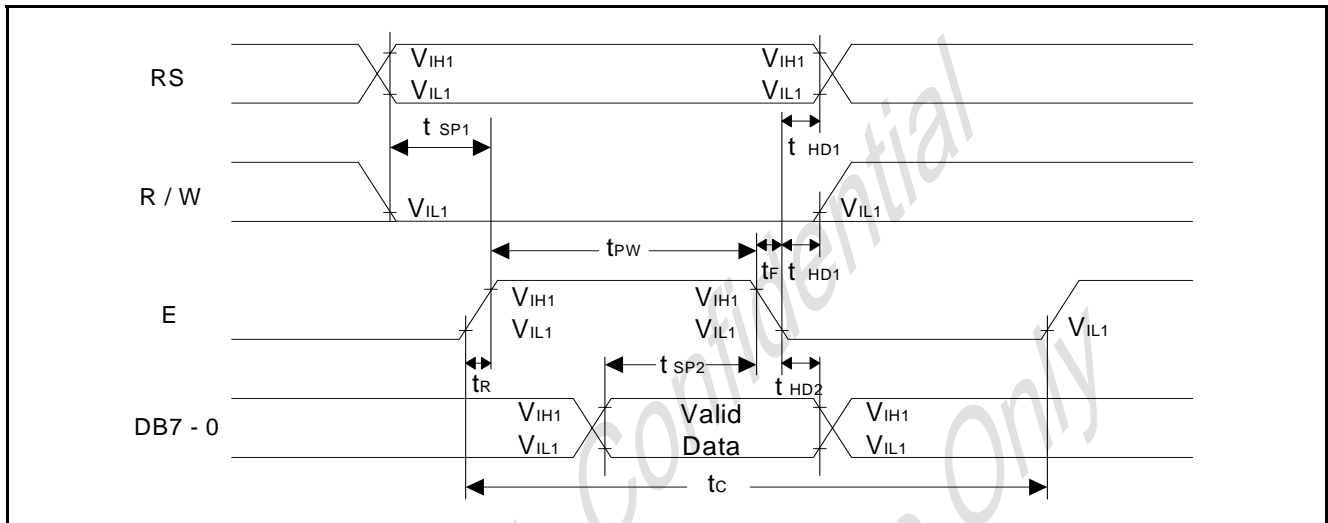
7.5.4. Read mode (Reading Data from SPLC783A1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_W	220	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	120	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	20	-	-	ns	Pin DB0 - DB7

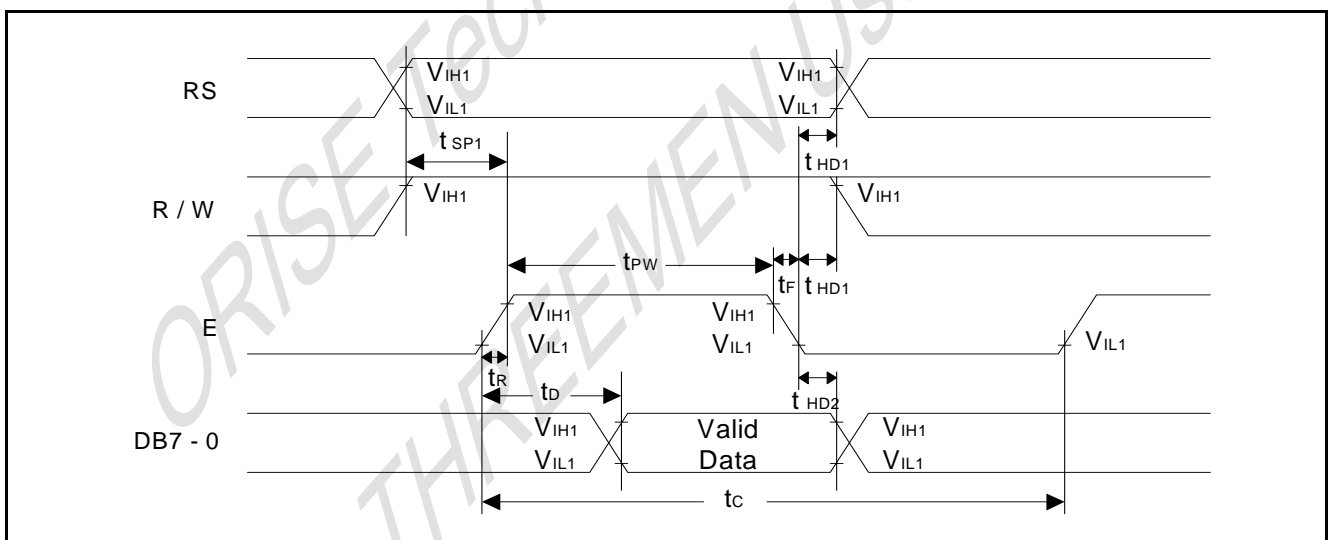
7.5.5. Interface mode with LCD Driver (SPLC100A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Clock pulse width high	t_{PWH}	800	-	-	ns	Pins: CLK1, CLK2
Clock pulse width low	t_{PWL}	800	-	-	ns	Pins: CLK1, CLK2
Clock setup time	t_{CSP}	500	-	-	ns	Pins: CLK1, CLK2
Data setup time	t_{DSP}	300	-	-	ns	Pins: D
Data hold time	t_{HD}	300	-	-	ns	Pins: D
M delay time	t_D	-1000	-	1000	ns	Pins: M

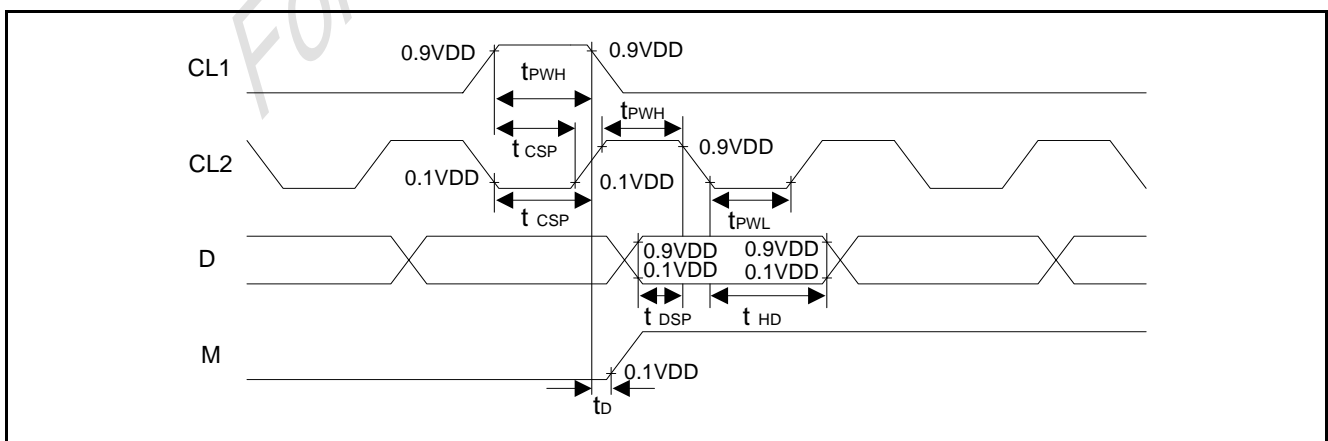
7.5.6. Write mode timing diagram (Writing Data from MPU to SPLC783A1)



7.5.7. Read mode timing diagram (Reading Data from SPLC783A1 to MPU)



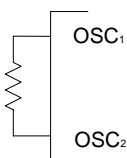
7.5.8. Interface mode with SPLC100A1 timing diagram



8. APPLICATION CIRCUITS

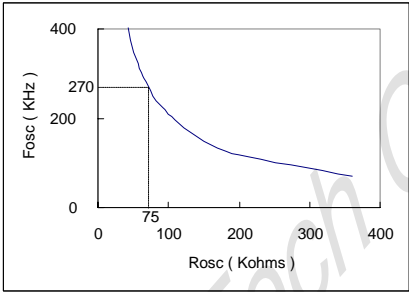
8.1. R-Oscillator

The oscillation resistor R_f is used only for the internal oscillator operation mode.

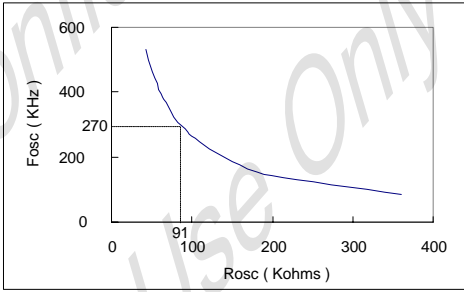


OSC₁: $R_f : 75K\Omega \pm 2\%$ (when VDD = 3.0V)
 $R_f : 91K\Omega \pm 2\%$ (when VDD = 5.0V)

OSC₂: Since the oscillation frequency varies depending on the OSC₁ and OSC₂ pin capacitance, the wiring length to these pins should be minimized.



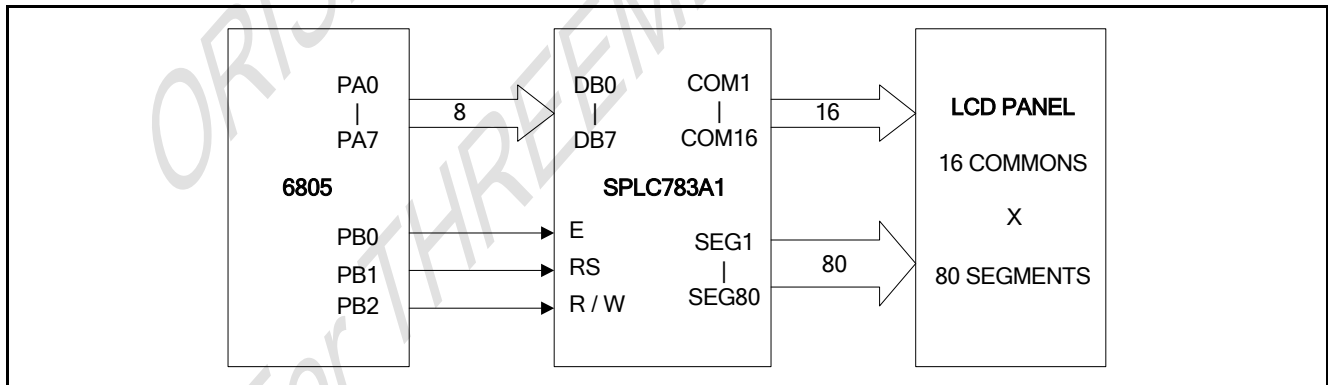
VDD = 3.0V



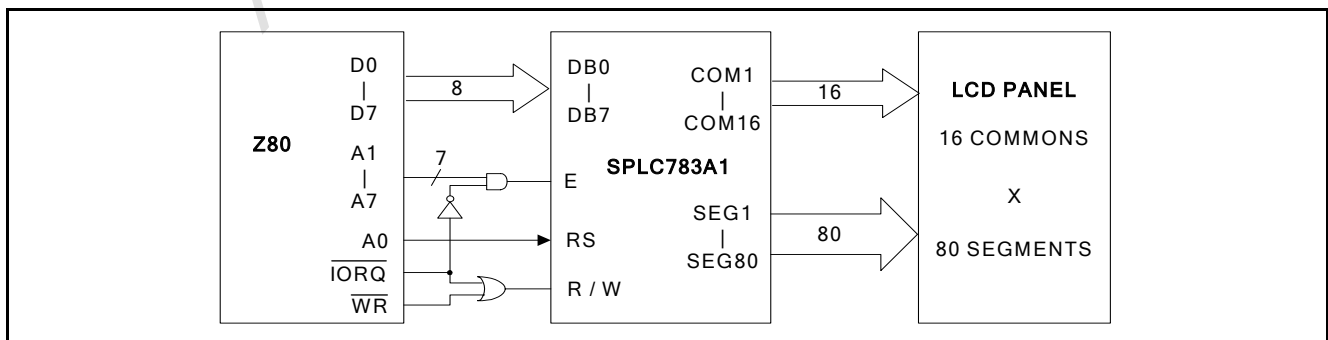
VDD = 5.0V

8.2. Interface to MPU

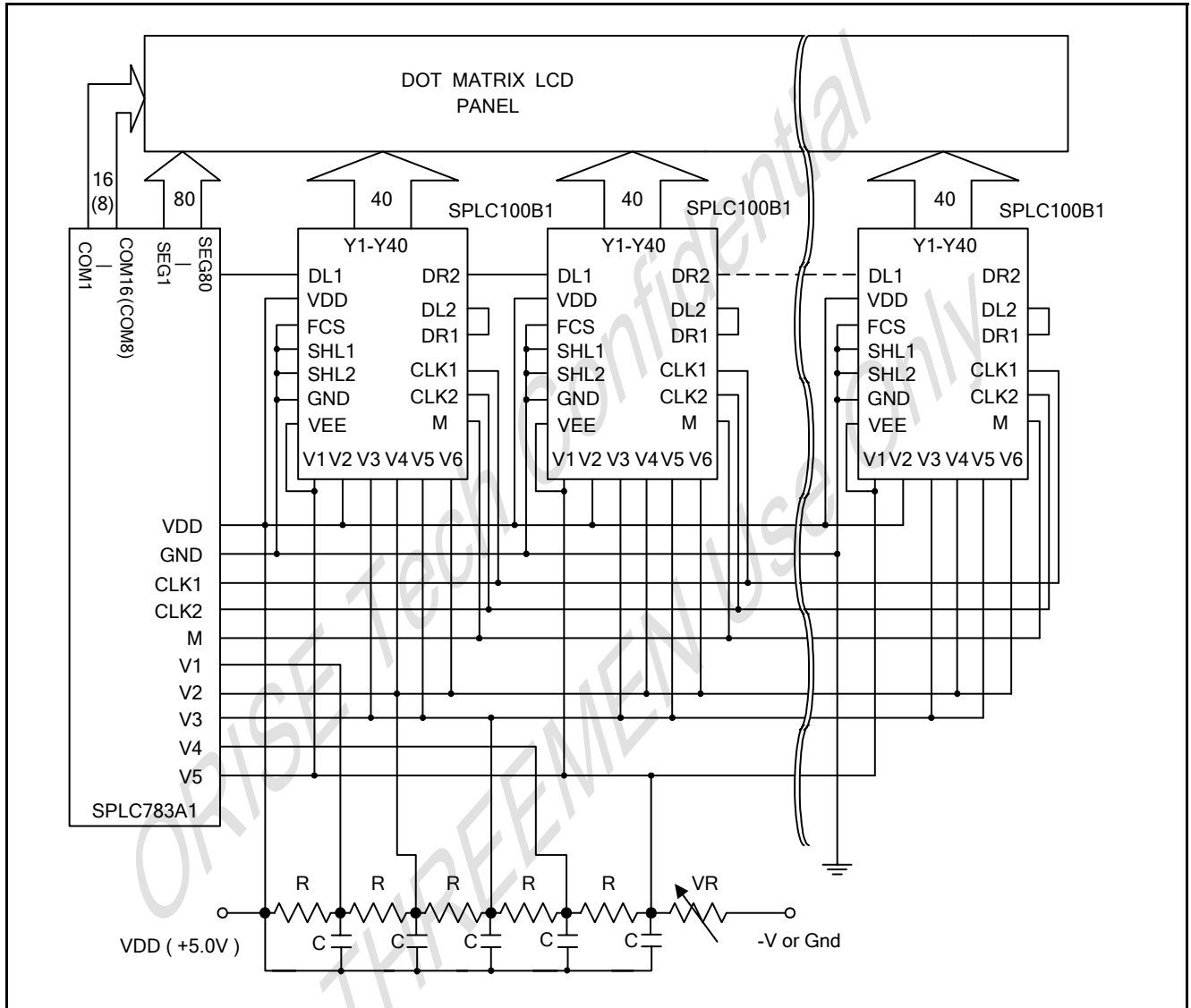
8.2.1. Interface to 8-bit MPU (6805)



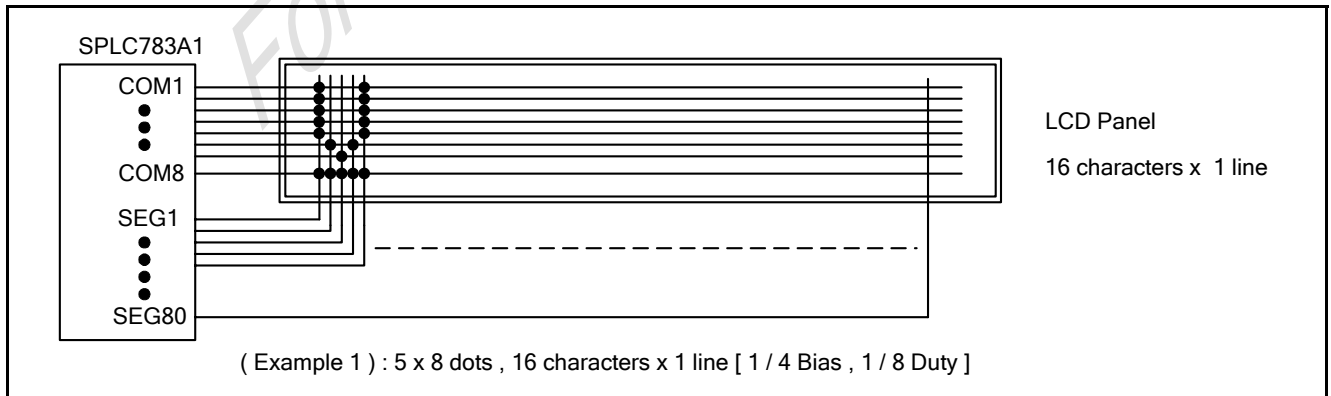
8.2.2. Interface to 8-bit MPU (Z80)

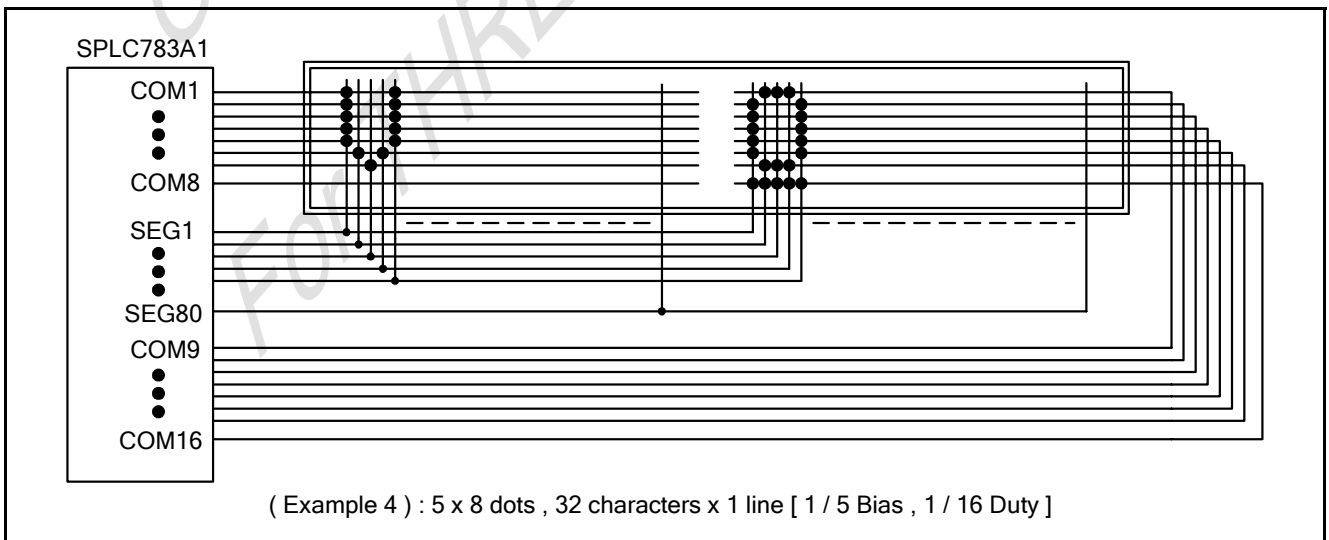
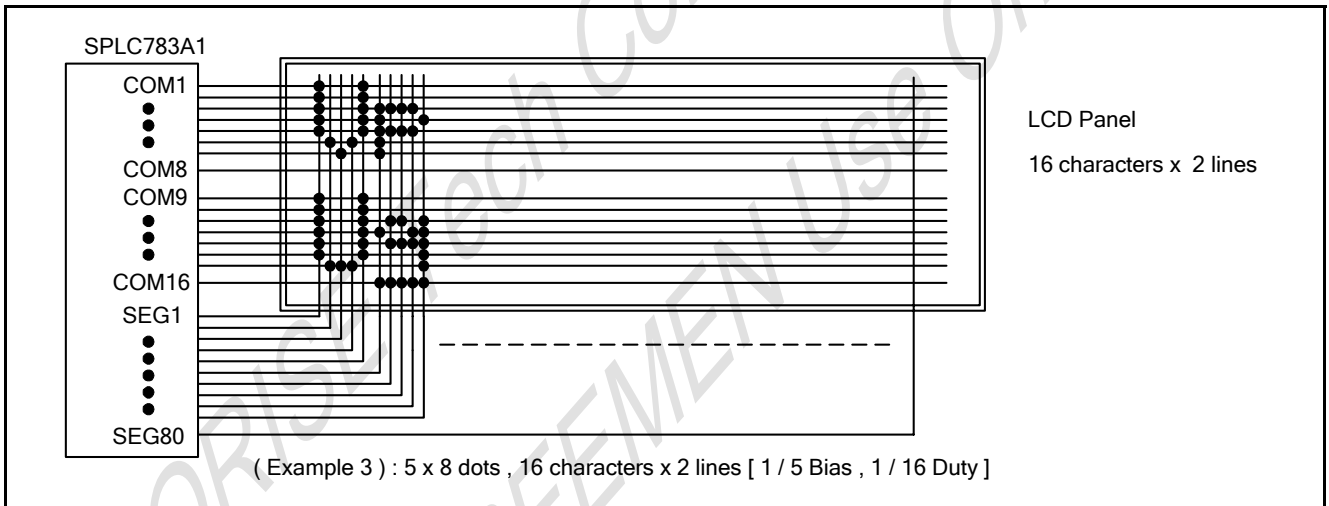
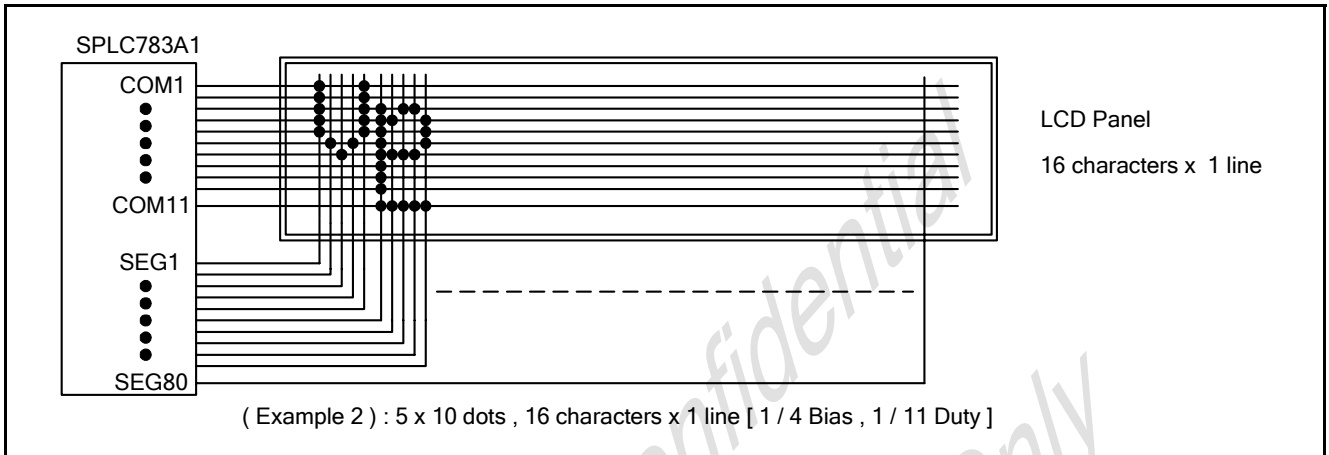


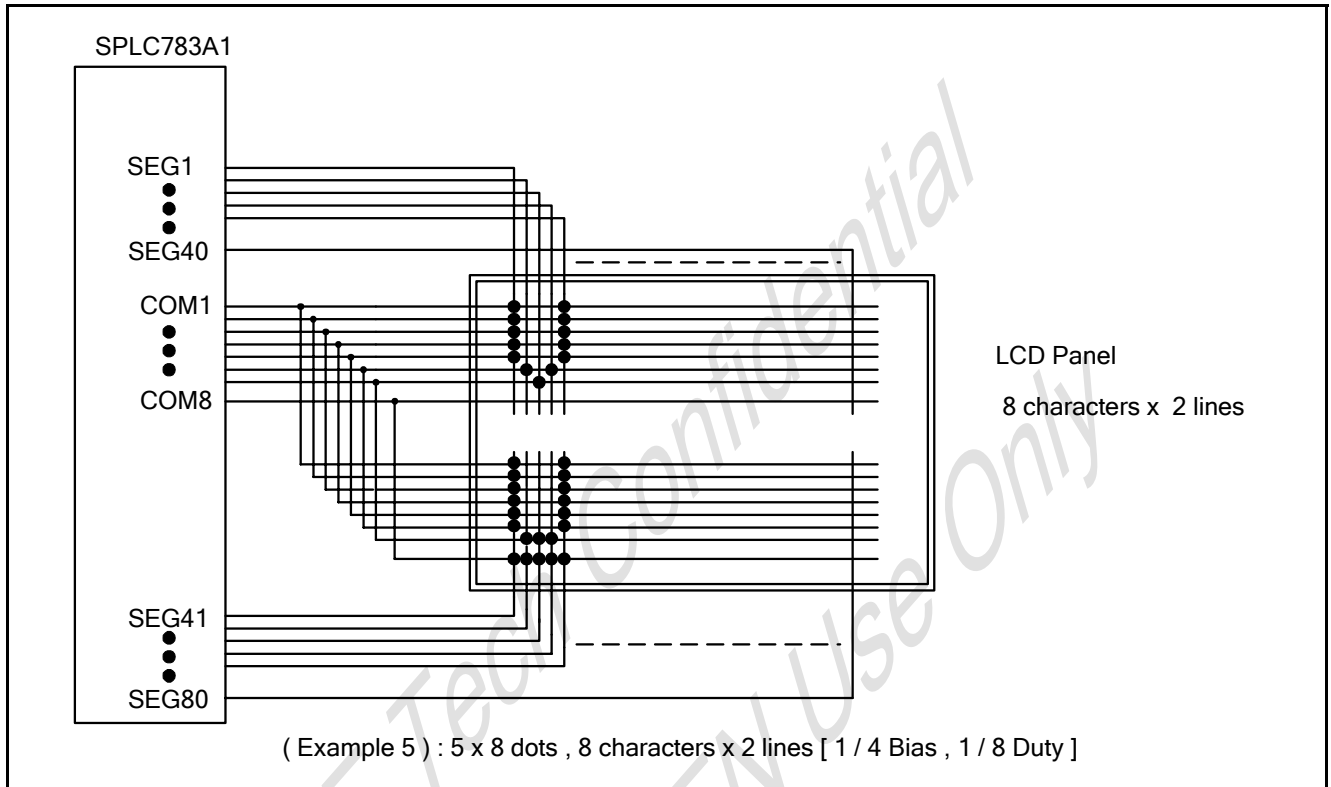
8.3. SPLC783A1 Application Circuit



8.4. Applications for LCD







9. CHARACTER GENERATOR ROM

9.1. SPLC783A1 - 001

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL				0	1	2	3	4	5	6	7	8	9	A	B	C
LLLH			!	0	1	2	3	4			.	ア	チ	ウ	音	留
LLHL			"	2	R	b	r				「	イ	ウ	※	音	留
LLHH			#	3	C	S	c	s			」	ウ	テ	モ	モ	※
LHLL			*	4	D	T	d	t			、	エ	ト	カ	ウ	留
LHLH			%	5	E	U	e	u			・	オ	カ	工	区	留
LHHL			&	6	F	V	f	v			ヲ	カ	ニ	ヨ	留	留
LHHH			'	7	G	W	g	w			ヲ	キ	※	ヲ	留	留
HLLL			(8	H	X	h	x			、	ウ	※	リ	ノ	留
HLLH)	9	I	Y	i	y			ウ	ウ	ル	ノ	留	留
HLHL			*	*	J	Z	j	z			エ	コ	ノ	レ	ジ	キ
HLHH			+	*	K	C	k	c			オ	オ	白	口	※	留
HHLL			,	<	L	*I	l				カ	ウ	フ	フ	キ	留
HHLH			-	=	M	I	m				ユ	※	ノ	レ	キ	留
HHHL			.	>	N	^n	n	*			ヨ	セ	市	ノ	留	留
HHHH			/	?0	L	O	o	*			ウ	ウ	ア	ノ	留	留

9.2. SPLC783A1 - 003

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LLLH	;	!	1	A	Q	a	9	0	;	;	;	;	J	+	Y	U
LLHL	7	"	2	B	R	b	r	;	;	;	;	;	;	;	;	;
LLHH	;	#	3	C	S	c	s	;	;	;	;	;	P	1	E	;
LHLL	;	;	4	D	T	d	t	;	;	;	;	;	;	;	;	;
LHLH	;	;	5	E	U	e	u	;	;	;	;	;	;	;	;	;
LHHL	;	;	6	F	V	f	v	;	;	;	;	;	;	;	;	;
LHHH	;	;	7	G	W	w	w	;	;	;	;	;	;	;	;	;
HLLL	;	;	8	H	X	h	x	;	;	;	;	;	;	;	;	;
HLLH	;	;	9	I	Y	i	y	;	;	;	;	;	;	;	;	;
HLHL	;	;	;	J	Z	j	z	;	;	;	;	;	;	;	;	;
HLHH	;	;	;	K	[k	[;	;	;	;	;	;	;	;	;
HHLL	;	;	;	L	\	l	\	;	;	;	;	;	;	;	;	;
HHLH	;	;	;	M]	m]	;	;	;	;	;	;	;	;	;
HHHL	;	;	;	N	^	n	^	;	;	;	;	;	;	;	;	;
HHHH	;	;	;	O	_	o	_	;	;	;	;	;	;	;	;	;

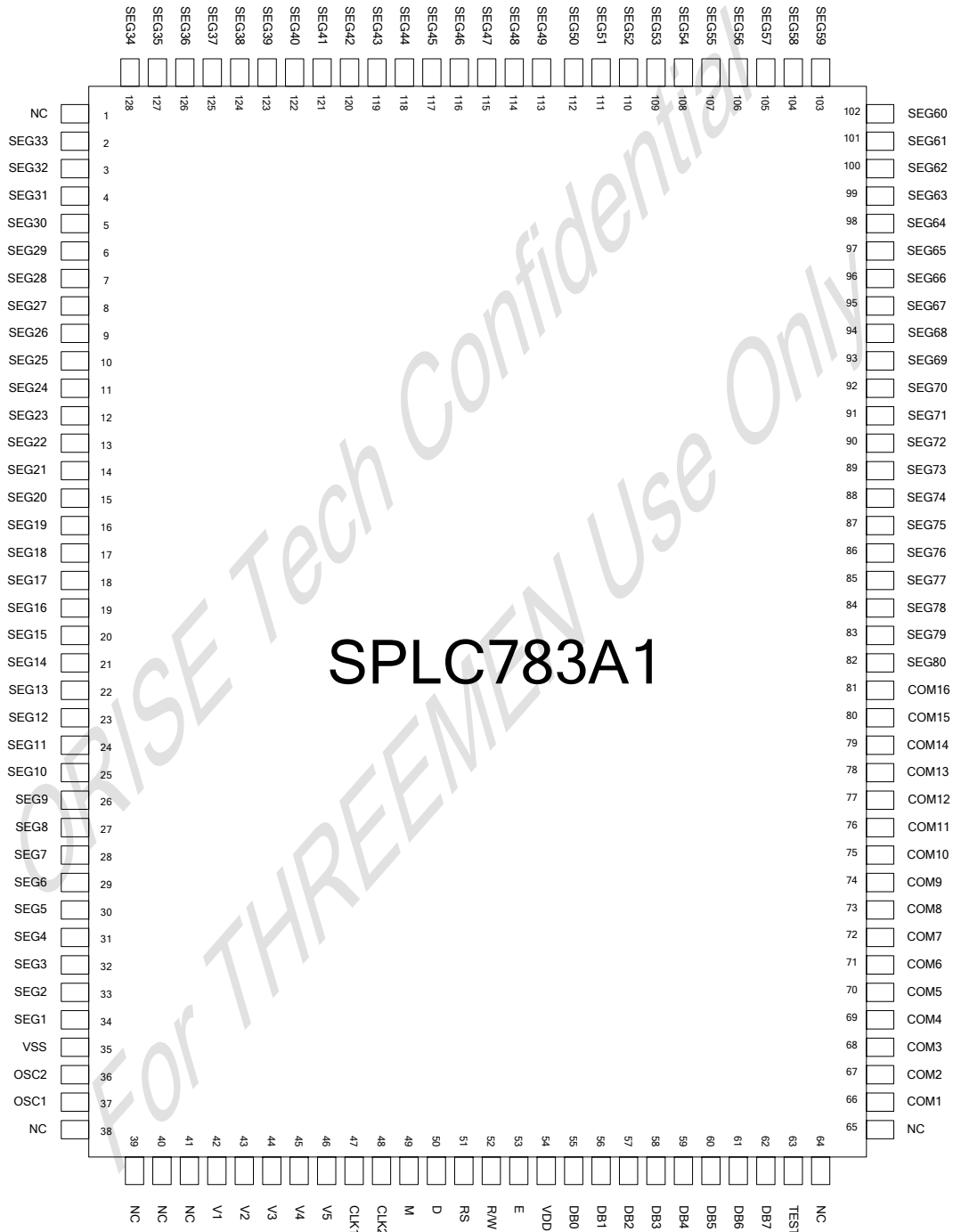
10.2. PAD Locations

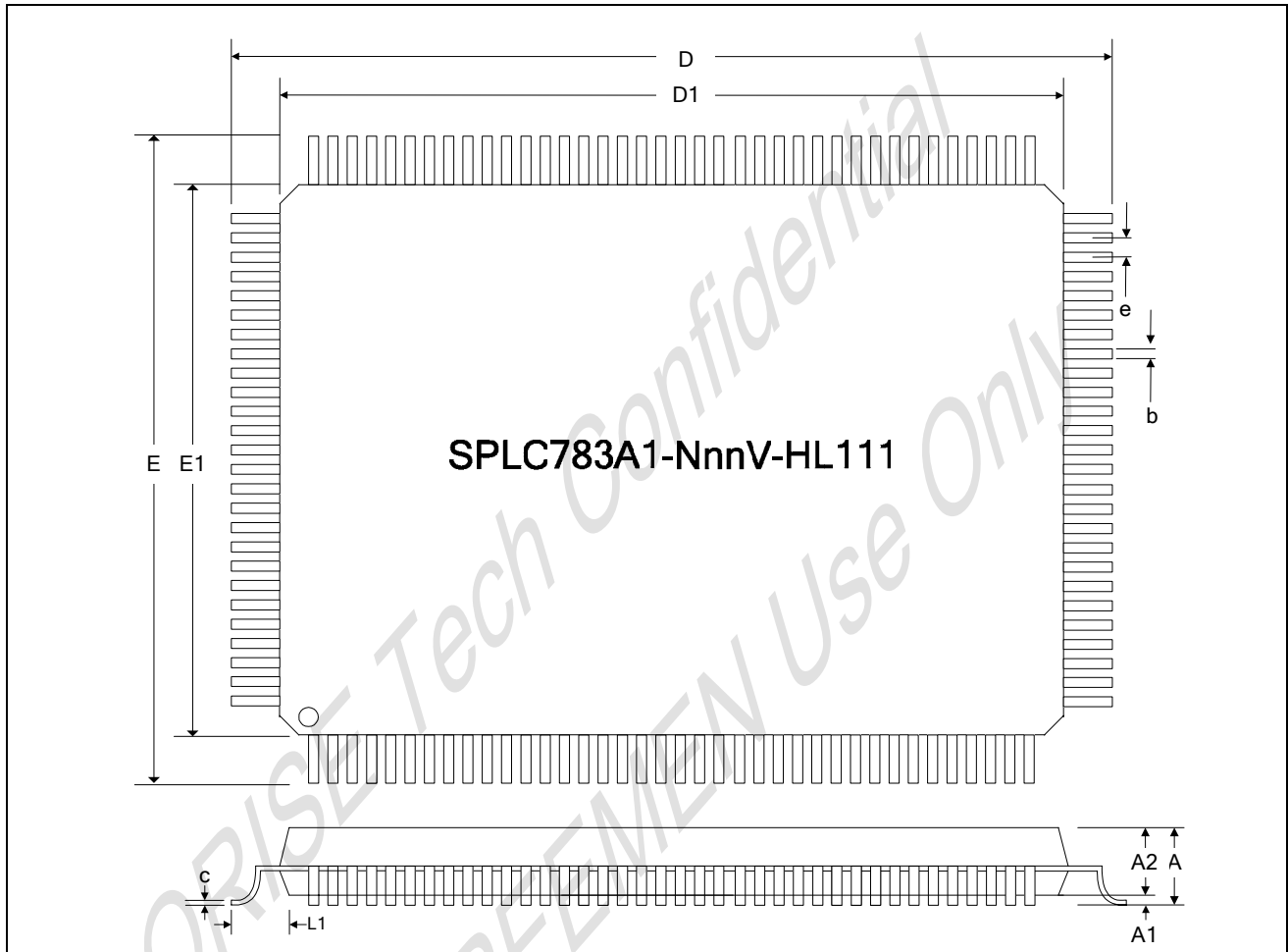
PAD No.	PAD Name	X	Y
1	SEG33	-1433	1889
2	SEG32	-1433	1763
3	SEG31	-1433	1631
4	SEG30	-1433	1505
5	SEG29	-1433	1390
6	SEG28	-1433	1275
7	SEG27	-1433	1160
8	SEG26	-1433	1050
9	SEG25	-1433	940
10	SEG24	-1433	830
11	SEG23	-1433	720
12	SEG22	-1433	610
13	SEG21	-1433	500
14	SEG20	-1433	390
15	SEG19	-1433	280
16	SEG18	-1433	169
17	SEG17	-1433	59
18	SEG16	-1433	-50
19	SEG15	-1433	-160
20	SEG14	-1433	-270
21	SEG13	-1433	-380
22	SEG12	-1433	-490
23	SEG11	-1433	-600
24	SEG10	-1433	-710
25	SEG9	-1433	-820
26	SEG8	-1433	-930
27	SEG7	-1433	-1040
28	SEG6	-1433	-1150
29	SEG5	-1433	-1260
30	SEG4	-1433	-1370
31	SEG3	-1433	-1485
32	SEG2	-1433	-1600
33	SEG1	-1433	-1715
34	VSS	-1433	-1835
35	OSC2	-1433	-1955
36	OSC1	-1433	-2076
37	V1	-1230	-2076
38	V2	-1105	-2076
39	V3	-980	-2076
40	V4	-855	-2076
41	V5	-740	-2076
42	CLK1	-625	-2076

PAD No.	PAD Name	X	Y
43	CLK2	-510	-2076
44	M	-395	-2076
45	D	-282	-2076
46	RS	-172	-2076
47	R/W	-62	-2076
48	E	47	-2076
49	VDD	157	-2076
50	DB0	267	-2076
51	DB1	379	-2076
52	DB2	494	-2076
53	DB3	609	-2076
54	DB4	724	-2076
55	DB5	840	-2076
56	DB6	965	-2076
57	DB7	1090	-2076
58	TEST	1215	-2076
59	COM1	1440	-2106
60	COM2	1440	-1986
61	COM3	1440	-1866
62	COM4	1440	-1746
63	COM5	1440	-1631
64	COM6	1440	-1516
65	COM7	1440	-1401
66	COM8	1440	-1291
67	COM9	1440	-1181
68	COM10	1440	-1071
69	COM11	1440	-961
70	COM12	1440	-851
71	COM13	1440	-741
72	COM14	1440	-631
73	COM15	1440	-521
74	COM16	1440	-411
75	SEG80	1440	-301
76	SEG79	1440	-191
77	SEG78	1440	-81
78	SEG77	1440	28
79	SEG76	1440	138
80	SEG75	1440	248
81	SEG74	1440	358
82	SEG73	1440	468
83	SEG72	1440	578
84	SEG71	1440	688

PAD No.	PAD Name	X	Y
85	SEG70	1440	799
86	SEG69	1440	909
87	SEG68	1440	1019
88	SEG67	1440	1129
89	SEG66	1440	1239
90	SEG65	1440	1354
91	SEG64	1440	1469
92	SEG63	1440	1584
93	SEG62	1440	1704
94	SEG61	1440	1824
95	SEG60	1440	1944
96	SEG59	1442	2096
97	SEG58	1317	2096
98	SEG57	1192	2096
99	SEG56	1067	2096
100	SEG55	952	2096
101	SEG54	837	2096
102	SEG53	722	2096
103	SEG52	607	2096
104	SEG51	495	2096
105	SEG50	385	2096
106	SEG49	275	2096
107	SEG48	165	2096
108	SEG47	55	2096
109	SEG46	-55	2096
110	SEG45	-165	2096
111	SEG44	-275	2096
112	SEG43	-385	2096
113	SEG42	-495	2096
114	SEG41	-607	2096
115	SEG40	-722	2096
116	SEG39	-837	2096
117	SEG38	-952	2096
118	SEG37	-1069	2096
119	SEG36	-1194	2096
120	SEG35	-1319	2096
121	SEG34	-1444	2096

10.3. PIN Assignment



10.4. Package Information (Green Package)


Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	21.90	22.00	22.10
D1	19.90	20.00	20.10
E	15.90	16.00	16.10
E1	13.90	14.00	14.10
e	0.50 BSC.		
b	0.17	0.22	0.27
c	0.09	-	0.20
L1	1.00 REF		

Unit: Millimeter

11. LEAD FRAME PACKAGE PCB DESIGN AND MANUFACTURING GUIDELINES

11.1. Purpose

The purpose of this specification is to identify plastic surface mount devices (SMDs) those are sensitive to moisture-induced stress, so that they can be properly design PCB and assembly packaged, stored and handled to avoid subsequent mechanical damage during the assembly solder reflow attachment and /or repair operation.

11.2. Scope

11.2.1. PCB layout guideline

11.2.2. PCB process

11.2.3. Storage Condition and Period for Package

11.2.4. Recommended SMT Temperature Profile

11.3. Noun definition

11.3.1. NSMD: Non Solder Mask Defined

11.3.2. SMD: Solder Mask Defined

11.3.3. CSP: Chip scale Package

11.3.4. PCB :Printed Circuit Board

11.4. Responsibility unity:

ORISE Quality Assurance unity

11.5. Contents

11.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC-7525: Stencil Design Guidelines

J-STD-020: IPC/JEDEC Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Device

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-HDBK-001: Handbook & Guide to the Requirements of Soldered Electronic Assemblies with Amendment 1

IPC -6016: Qualification & Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-STD-003: Solderability Tests for Printed Boards

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

JESD22-B110: Subassembly Mechanical Shock

IPC-A-610: Acceptability of Electronic Assemblies

11.5.2. PCB layout guideline

PCB designer comply with IPC-SM-782 and IPC-7095 requirements is recommended

11.5.3. PCB process

11.5.3.1. Board material

The Glass transition temperature (T_g) of Board material greater than 170 degree C is recommended for Pb-free and Green package.

11.5.3.2. Surface Finishes

In order to achieve high assembly yields, use of a surface finish that is planar

And has good solderability performance is important. Below methods are all known to provide an acceptable land pad surface.

*OSP (Organic Solderability Preservative)

*Nihau (Electroplated nickel /gold)

*Immersion Ag

*Immersion Sn

- 11.5.3.3. Solder Paste: No clean flux is recommended.
- 11.5.3.4. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process
- 11.5.3.5. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package..
- 11.5.3.6. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green package.
- 11.5.3.7. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.

11.5.4. Storage condition and period for package

Orise technology evaluates all plastic surface mount devices (SMDs) to ICP/JEDEC J-STD-020A, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices, or refers to IPC JEDEC J-STD-033A Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

- 11.5.4.1. The primary facts for the package storage include oxidation, static, and therefore, the following rules are recommended to be applied for the storage.
- 11.5.4.2. The storage temperature should be $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, and the humidity should be in the range of 50% \pm 10% R.H. after opening the dry pack.
After the dry bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing.
- 11.5.4.3. Must be:
 - a. Mounted within 168 hours(Level 3) and 72 hours(Level 4) at factory conditions of $\leq 30^{\circ}\text{C}/ 60\%$ R.H. or
 - b. Stored at $\leq 20\%$ R.H.
- 11.5.4.4. Devices require baking, before mounting, if:
 - a. Humidity Indicator Card shown warning message when read at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, or
 - b. 11.5.4.3 is not met.
- 11.5.4.5. If baking is required. Devices may be baking for:
 - a. 192 hour at $40^{\circ}\text{C} + 5^{\circ}\text{C} / -0^{\circ}\text{C}$ and $< 5\%$ R.H. for low temperature device containers, or
 - b. 24 hours at $125 \pm 5^{\circ}\text{C}$ for high temperature device containers
- 11.5.4.6. The storage condition should be consistent with the operation condition to prevent dewing phenomena.
- 11.5.4.7. The storage location should be kept away from water and smoke; an isolated area with positive pressure control is preferred.
- 11.5.4.8. For a long-term storage, it is recommended to keep in a container with Nitrogen in it.
- 11.5.4.9. Avoid heavy objects stacked on the pack.
- 11.5.4.10. Avoid the static damage; use an anti-static bag for the package.

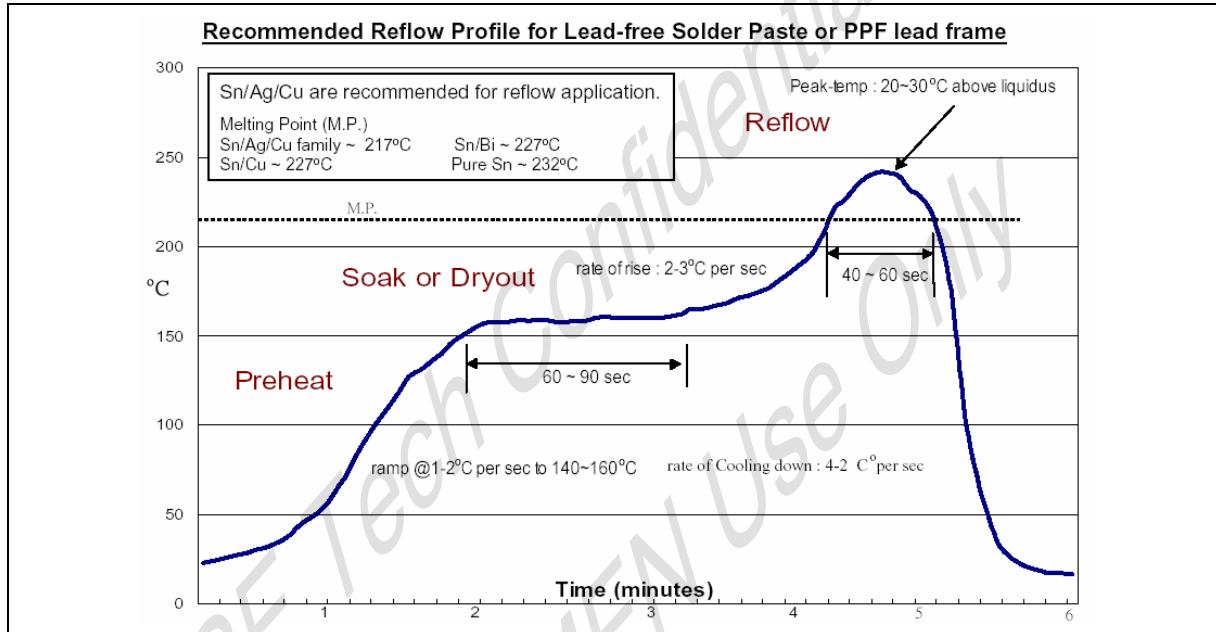
11.5.5. The classification of moisture sensitivity for Orise's product packages are shown in the following

(1) For Lead Free / Green Packages

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
LQFP	LEVEL 3	255 $+5/-0^{\circ}\text{C}$	168Hrs @ $\leq 30^{\circ}\text{C}/ 60\%$ R.H.	Yes

11.5.6. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of ORISE leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240°C~245°C for peak temperature.



11.6. References

IPC:

<http://www.ipc.org>

*NEMI (National Electronics Manufacturing Initiative)

<http://www.nemi.org>

*HDPUG (High Density Package Users Group)

<http://www.hdpug.org>

*JEDEC (Joint Electronic Device Engineering Council)

<http://www.jedec.org>

*JEITA (Japan Electronic Industry Association)

<http://www.jeita.org>

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13. REVISION HISTORY

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