DATA SHEET

旭曜科技 ORISE TECH

SPLC782A1

16COM/80SEG Controller/Driver

Preliminary

OCT. 02, 2007

Version 0.1

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16COM / 80SEG CONTROLLER / DRIVER

1. GENERAL DESCRIPTION

The SPLC782A1, a dot-matrix LCD controller and driver, is a low-power CMOS integrated circuit. The SPLC782A1 is capable of connecting with MPU for LCD application and easily to be used for designing the low-cost products.

2. FEATURES

- Character generator ROM: 10880 bits
  - Character font 5 x 8 dots: 192 characters
  - Character font 5 x 10 dots: 64 characters
- 4 type CGROM mode, Max. 256 characters can be used.
- Character generator RAM: 512 bits
  - Character font 5 x 8 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- Provide connecting to 4-bit or 8-bit MPU
- Direct driver for LCD: 16 COMs x 80 SEGs
- 80-channel Bi-Direction segment driver
- 16-channel Bi-direction common driver
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 8 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 8 dots / line
- LCD type-A, type-B waveform can be selected.
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with internal resistor)
- Built-in Bias resistor
- Support external clock operation
- Package form: Au bump chip

3. ORDERING INFORMATION

Product Number	Package Type
SPLC782A1-NnnV-C	Chip form with gold bump

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

4. BLOCK DIAGRAM

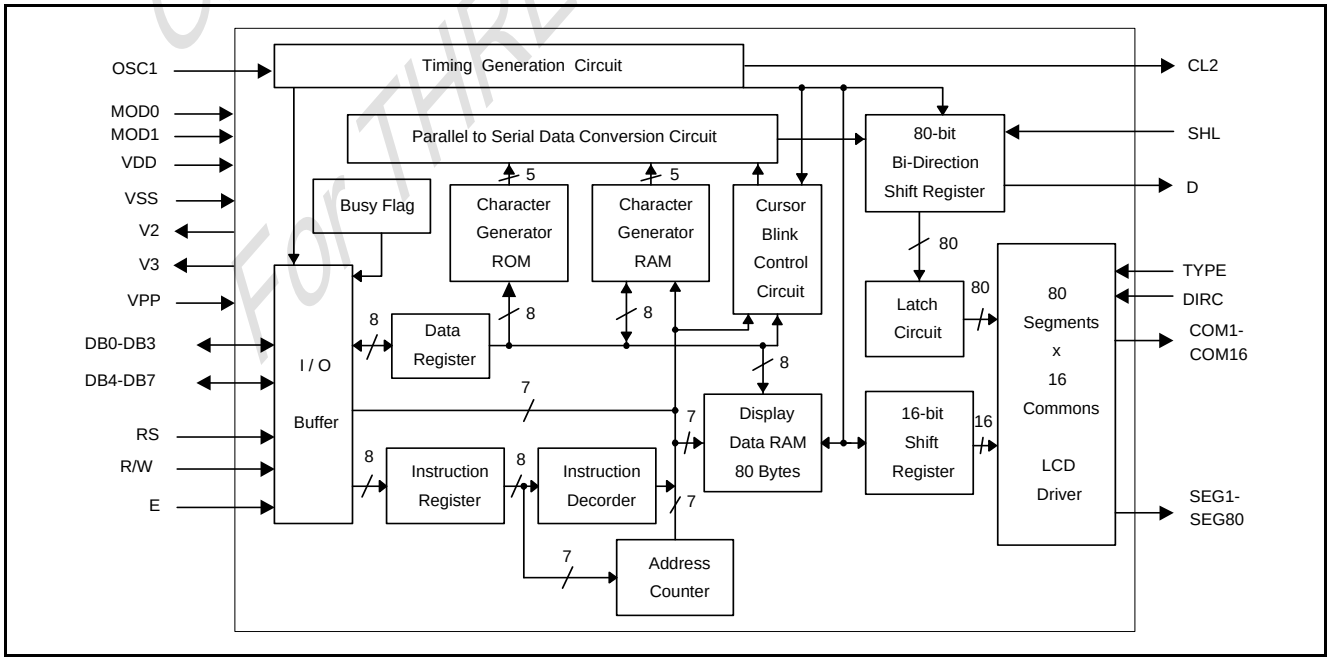


Figure 4-1: Block Diagram

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	19, 20, 28	I	Logic Power input
VSS	11, 12, 37	I	Ground
VPP	23, 24	I	LCD Voltage; V_{LCD} = VPP - VSS
V2 V3	22 21	I	LCD Bias Voltage Control. Open for 1/5 Bias, Short for 1/4 Bias
E	27	I	It is a start signal to read data or write data.
R/W	26	I	It is a signal to select read or write. 1: Read, 0: Write.
RS	25	I	It is a signal to select register. 1: Data register (for read and write) 0: Instruction register (for write), Busy flag -- address counter (for read).
DB3 - DB0	32 - 29	I/O	Low-order 4 data bits
DB7 - DB4	36 - 33	I/O	High-order 4 data bits
SEG80 - SEG1	46 - 125	O	Segment signals for LCD.
COM16 - COM9	45 - 38	O	Common signals for LCD.
COM8 - COM1	1 - 8	O	Common signals for LCD.
TYPE	14	I	LCD Alternate Signals. TYPE = 0: Type-A TYPE = 1: Type-B
DIRC	15	I	Common Scan Direction DIRC = 0: COM1 → COM2 → … → COM15 → COM16 DIRC = 1: COM16 → COM15 → … → COM2 → COM1
SHL	16	I	Segment Shift Direction SHL = 0: SEG1 → SEG2 → … → SEG79 → SEG80 SHL = 1: SEG80 → SEG79 → … → SEG2 → SEG1
MOD1 MOD0	18 17	I	CGROM / CGRAM Mode Select
OSC1	13		For internal clock operation, leave this pin open. For external clock operation, the clock is input to OSC1.
CL2	10	O	Test Mode Clock Output; Open for normally use.
D	9	O	Test Mode Data Output; Open for normally use.

MOD1	MOD0	Function
1	1	$00 - $0F as CGRAM
1	0	$00 - $07 as CGRAM, $08 - $0F as CGROM
0	1	$00 - $03 as CGRAM, $04 - $0F as CGROM
0	0	$00 - $0F as CGROM

6. FUNCTIONAL DESCRIPTIONS

6.1. Oscillator

The built-in RC oscillator generates suitable clock for SPLC782A1 operation.

6.2. Control and Display Instructions

Control and display instructions is shown as follows:

6.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Figure 6-1: Clear Display Instruction Code

It clears the whole display and sets display data RAM′s address 0 in address counter.

6.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

Figure 6-2: Return Home Instruction Code

X: Do not care (0 or 1)

It sets display data RAM′s address 0 in address counter and display returns to its original position. The cursor or blink goes to the left edge of the display (to the 1st line if 2 lines are displayed). The content of the Display Data RAM does not change.

6.2.3. Entry mode set

During writing and reading data, it sets cursor move direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Figure 6-3: Entry Mode Instruction Code

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

Figure 6-4: Shift Direction Patterns According to S and I/D Bits

6.2.4. Display ON/OFF control

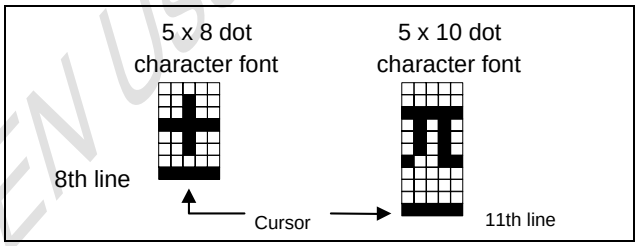
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Figure 6-5: Display ON/OFF Control Instruction Code

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

B = 1: Blinks on, B = 0: Blinks off



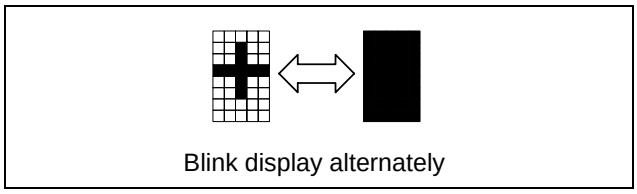


Figure 6-6: Cursor and Blinking

6.2.5. Cursor or display shift

Without changing DD RAM′s data, it can move cursor and shift display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X

Figure 6-7: Cursor or Display Shift Instruction Code

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

Figure 6-8: Shift Patterns According to S/C and R/L Bits

6.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

Figure 6-9: Function Set Instruction Code

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Datas are transferred with 8-bit lengths (DB0 - DB7).

DL = 0: Datas are transferred with 4-bit lengths (DB4 - DB7).

(It requires two times to transfer data)

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

Figure 6-10: Function Set Description

It cannot display two lines with 5 x 10 dot character font.

6.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

Figure 6-11: Set CGRAM address Instruction Code

It sets character generator RAM address $(aaaaaa)_2$ to the address counter. Character generator RAM data can read or write after this setting.

6.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

Figure 6-12: Set DDRAM address Instruction Code

It sets display data RAM address $(aaaaaaa)_2$ to the address counter.

Display data RAM can read or write after this setting.

In one-line display (N = 0),

$(aaaaaaa)_{2:}$ $(00)_{16}$ - $(4F)_{16.}$

In two-line display (N = 1),

$(aaaaaaa)_{2:}$ $(00)_{16}$ - $(27)_{16}$ for the first line,

$(aaaaaaa)_{2:}$ $(40)_{16}$ - $(67)_{16}$ for the second line.

6.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Figure 6-13: Read busy flag and address Instruction Code

When (BF = 1) indicates that the system is busy now; it will not accept any instruction until no busy (BF = 0). At the same time, the address counter contents $(aaaaaaa)_2$ is read out.

6.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

Figure 6-14: Write Data to CGRAM/DDRAM Instruction Code

It writes data $(dddddddd)_2$ to character generator RAM or display data RAM.

6.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

Figure 6-15: Read Data from CGRAM/DDRAM Instruction Code

It reads data $(dddddddd)_2$ from character generator RAM or display data RAM.

To get the correct data readout is shown belows:

1). Set the address of the character generator RAM or display data RAM or shift the cursor instruction.

2). Send the “Read” instruction.

6.3. Instruction Table

Instruction	Instruction Code										Description	Max. Execution time (Temp = -20℃ ~ +75℃)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	4.1ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	4.1ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	100μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.	100μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	100μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	100μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	100μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	100μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	100μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	100μs

Figure 6-16: Instruction Table

Note: "-" don't care

6.4. 8-Bit Operation and 16-Digit 1-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A1 starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 X X		Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WE_	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	COMPAMY _	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY _	Only shift the cursor's position to the left (Y).
15	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM 1 0 0 1 0 0 1 1 1 0	COMPANY	Write " N ". The display moves to the left.
17	Cursor or display shift 0 0 0 0 0 1 1 1 X X	COMPANY	Shift the display and the cursor's position to the right.
18	Cursor or display shift 0 0 0 0 0 1 0 1 X X	COMPANY_	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 0 0	COMPANY _	Write " " (space). The cursor is incremented by one and shifted to the right.
20	:	:	
21	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME _	Both the display and the cursor return to the original position (address 0).

Figure 6-17: 8-Bit Operation and 16-Digit 1-Line Display

6.5. 4-Bit Operation and 16-Digit 1-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A1 starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation.
3	Function set 0 0 0 0 1 0 0 0 0 0 X X		Set to 4-bit operation and select 1-line display line and character font.
4	Display on / off control 0 0 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appears.
5	Entry mode set 0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1 1 1	W_	Write “W". The cursor is incremented by one and shifted to the right.

Figure 6-18: 4-Bit Operation and 16-Digit 1-Line Display

6.6. 8-Bit Operation and 16-Digit 2-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A1 starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display line and 5 x 7 dot character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write " T ". The cursor is incremented by one and shifted to the right.
10	:	:	
11	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.

NO.	Instruction	Display	Operation
12	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.
13	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing, it sets mode for the display shift.
14	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
15	:	:	
16	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

Figure 6-19: 8-Bit Operation and 16-Digit 2-Line Display

6.7. Reset Function

At power on, it starts the internal auto-reset circuit and executes the initial instructions. There are the initial procedures shown as belows:

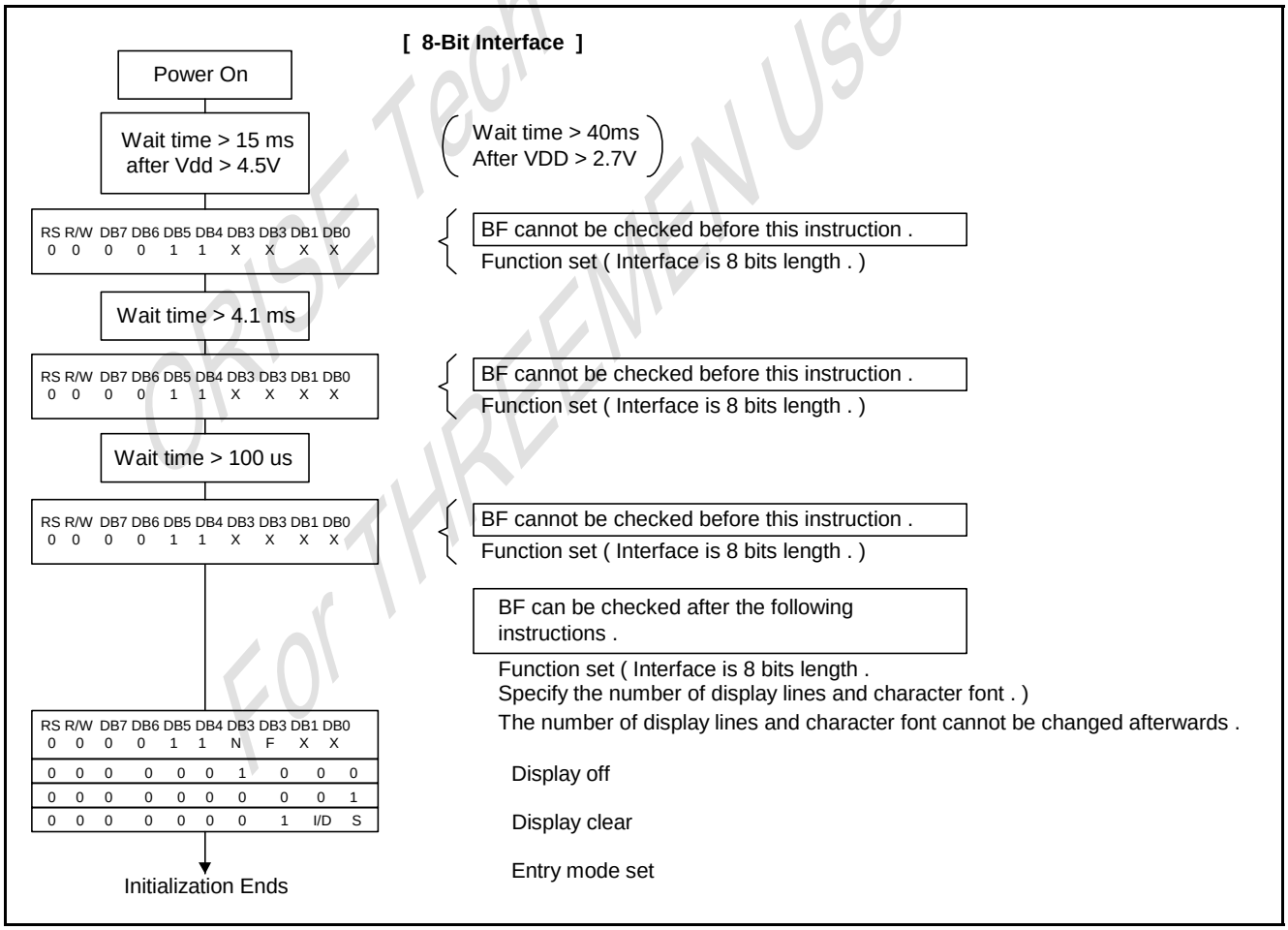


Figure 6-20: Reset Function (8-bit Interface)

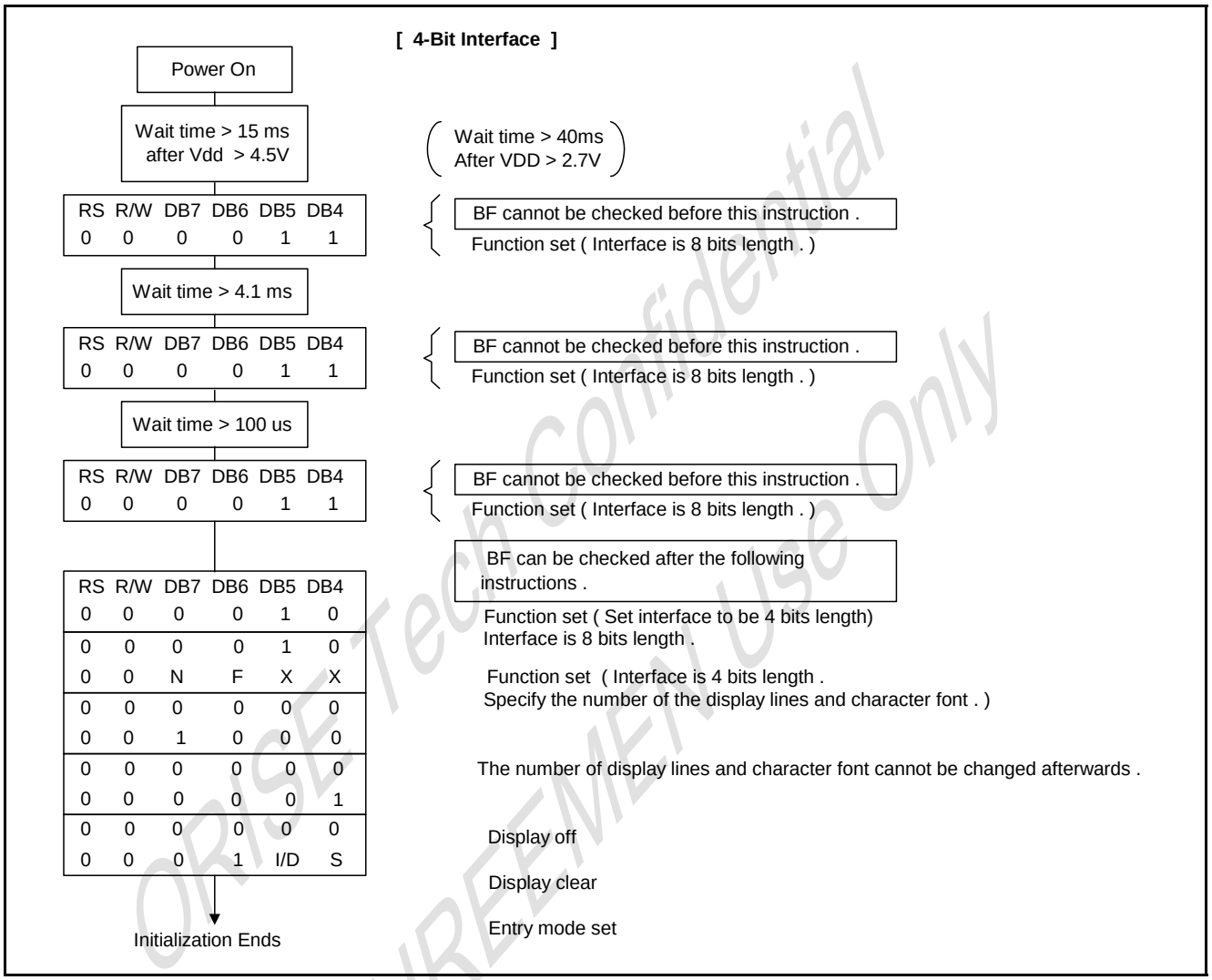


Figure 6-21: Reset Function (4-bit Interface)

6.8. Display Data RAM (DD RAM)

The DD RAM stores display data and its RAM size is 80 bytes. The area in DD RAM that is not used for display can be used as a general data RAM. Its address is set in the address counter.

There are the relations between the display data RAM′s address and the LCD′s position shown belows.

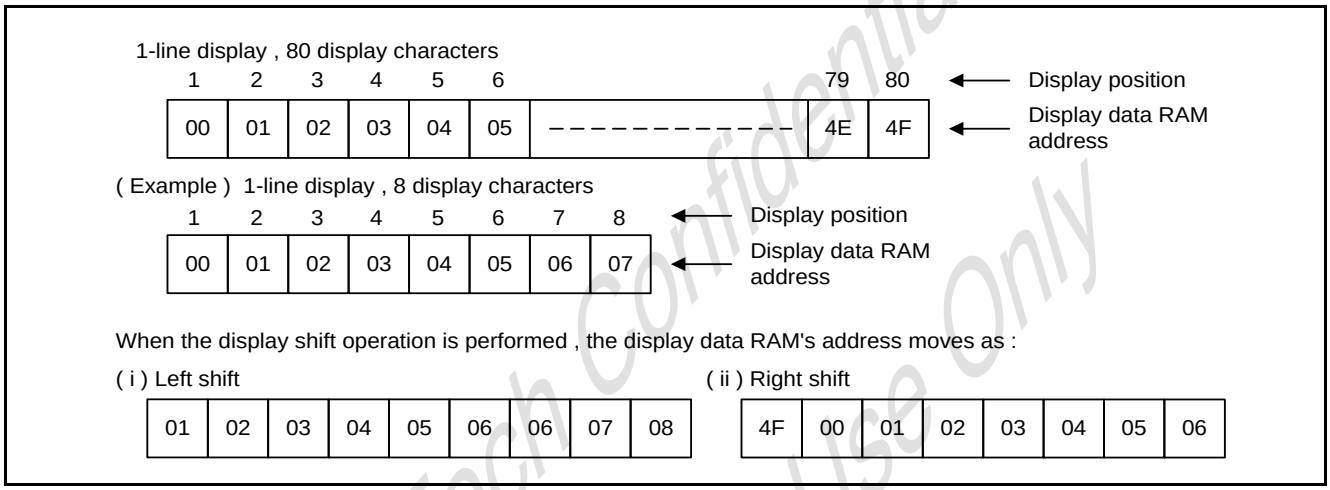


Figure 6-22: Relations Between Display Data Ram's Address and the LCD's Position

6.9. Timing Generation Circuit

The timing generation circuit can generate needed timing signals to the internal circuits. To prevent the internal timing interface, the MPU access timing and the RAM access timing are separately generated.

6.10. LCD Driver Circuit

There are 16 commons x 80 segments signal drivers in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals will output drive waveforms and the others still output unselected waveforms.

6.11. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 8 dot or 5 x 10 dot character patterns. It also can generate 192 5 x 8 dot character patterns and 64 5 x 10 dot character patterns.

6.12. Character Generator RAM (CG RAM)

Using the programs, users can easily change the character patterns in the character generator RAM. It can be written with 5 x 8 dots, 8 character patterns or written with 5 x 10 dots, 4 character patterns.

Here are the SPLC782A1's character patterns shown as belows:

Correspondence between Character Codes and Character Patterns.

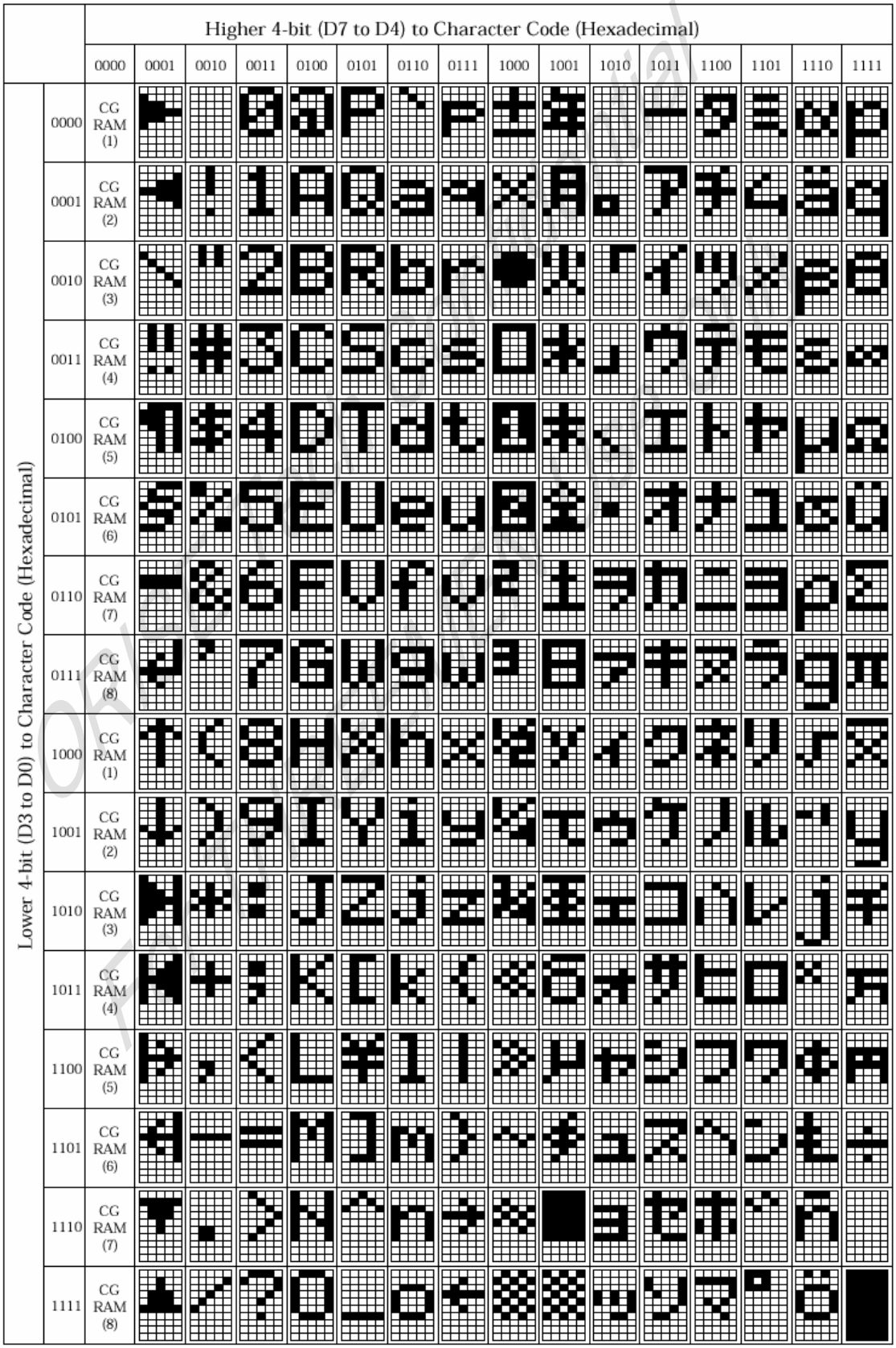


Figure 6-23: Character Code and Character Patterns

The relations between character generator RAM addresses, character generator RAM data (character patterns) and character codes are shown as belows:

6.12.1. 5 x 8 dot character patterns

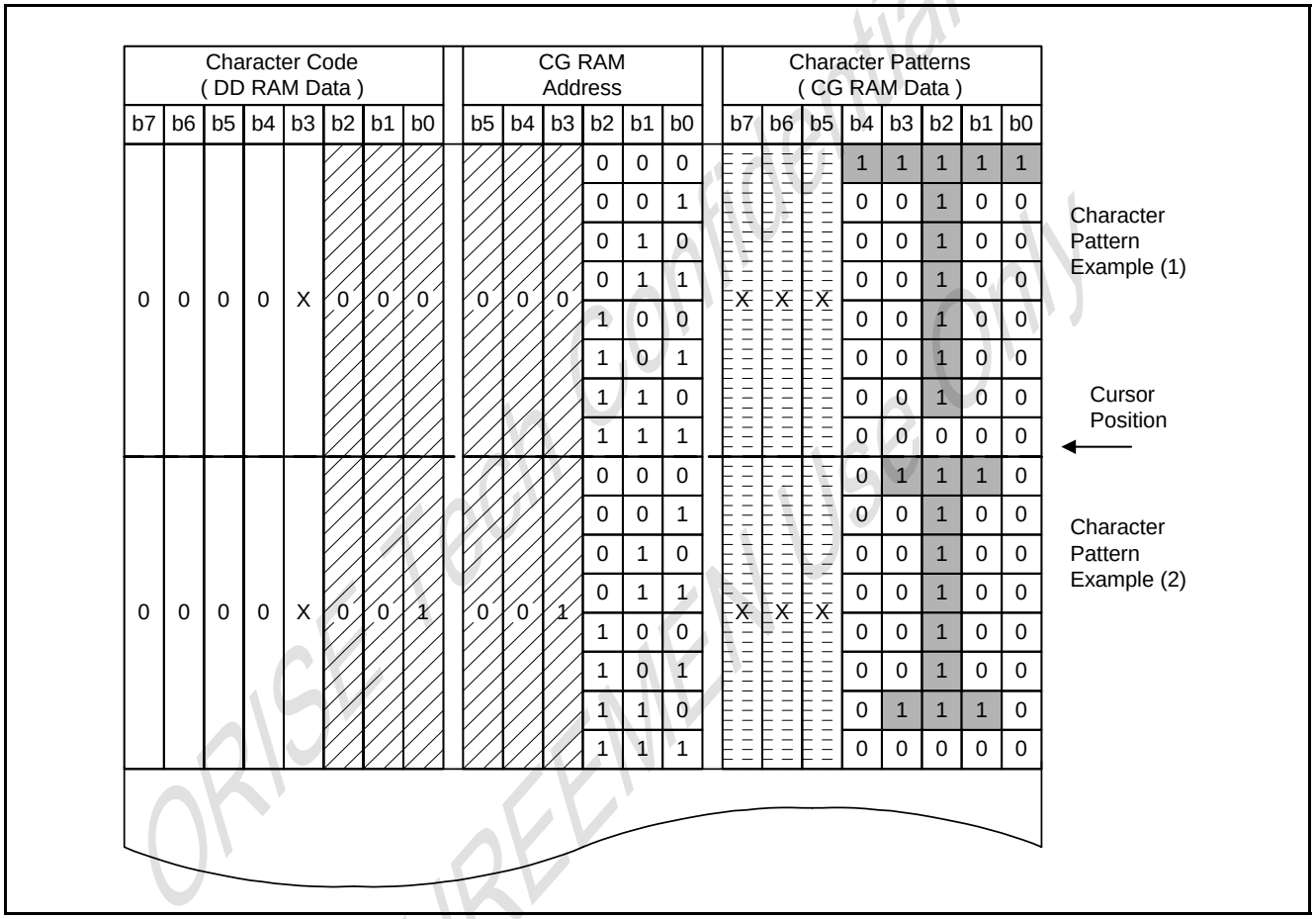


Figure 6-24: 5 x 8 Dot Character Patterns

Note1: ▨ It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 " : No selected , " X " : Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.

Note6: The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

6.12.2. 5 X 10 dot character patterns

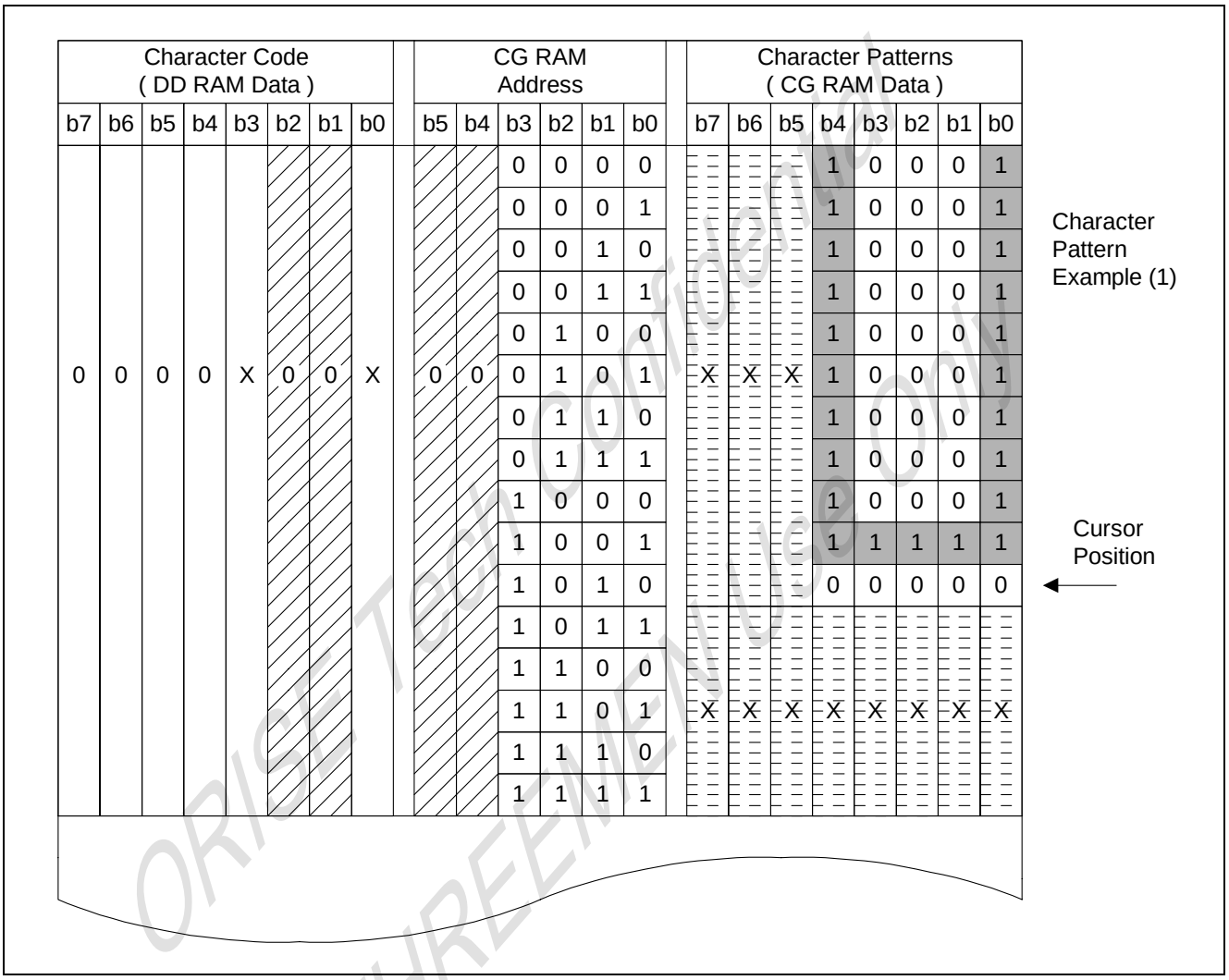


Figure 6-25: 5 x 10 Dot Character Patterns

Note1: It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

Note2: These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 ": No selected, " X ": Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display " U ". That means all of the character codes (00) 16, (01) 16, (08) 16,and (09) 16 can display " U " character.

Note6: The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

6.13. Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

When the address counter is $(07)_{16}$, the cursor's position is shown as follows:

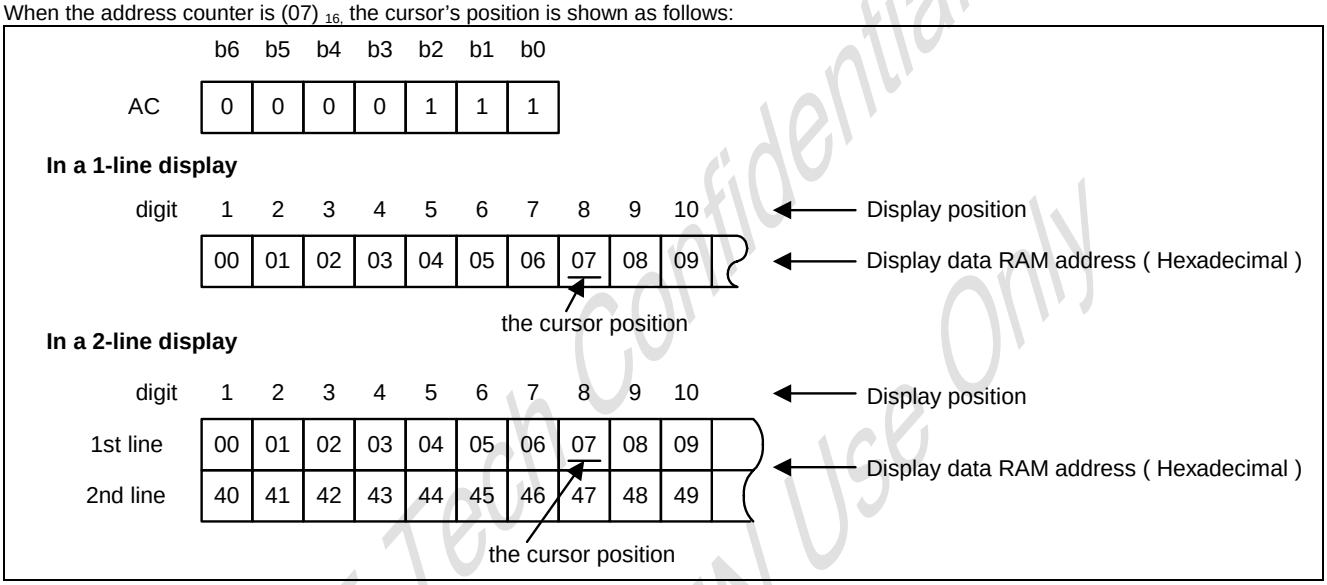


Figure 6-26: Cursor/Blink Control

6.14. Interfacing to MPU

There are two types of data operations: 4-bit operation and 8-bit operation. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4 bus lines (for 8-bit operation, DB7 to DB4). The bus lines of DB0 - DB3 are not used. Using 4-bit MPU to interface 8-bit data needs two times. First, the higher 4-bit data is transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4 bus lines (for 8-bit operation, DB3 to DB0). Using 8-bit MPU, the interfacing 8-bit data is transferred by 8 bus lines (DB0 - DB7).

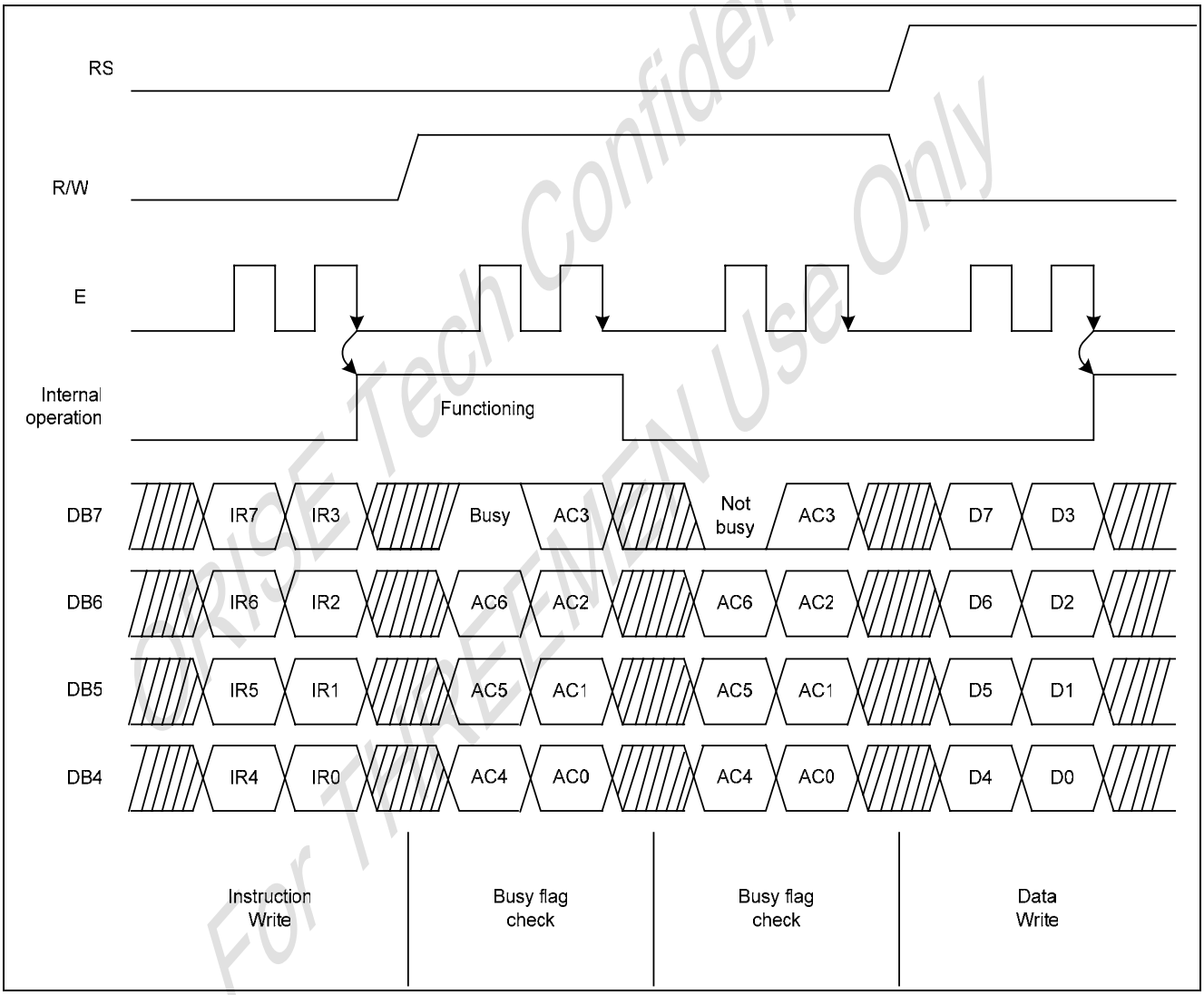


Figure 6-27: Example of 4-bit Data Transfer Timing Sequence

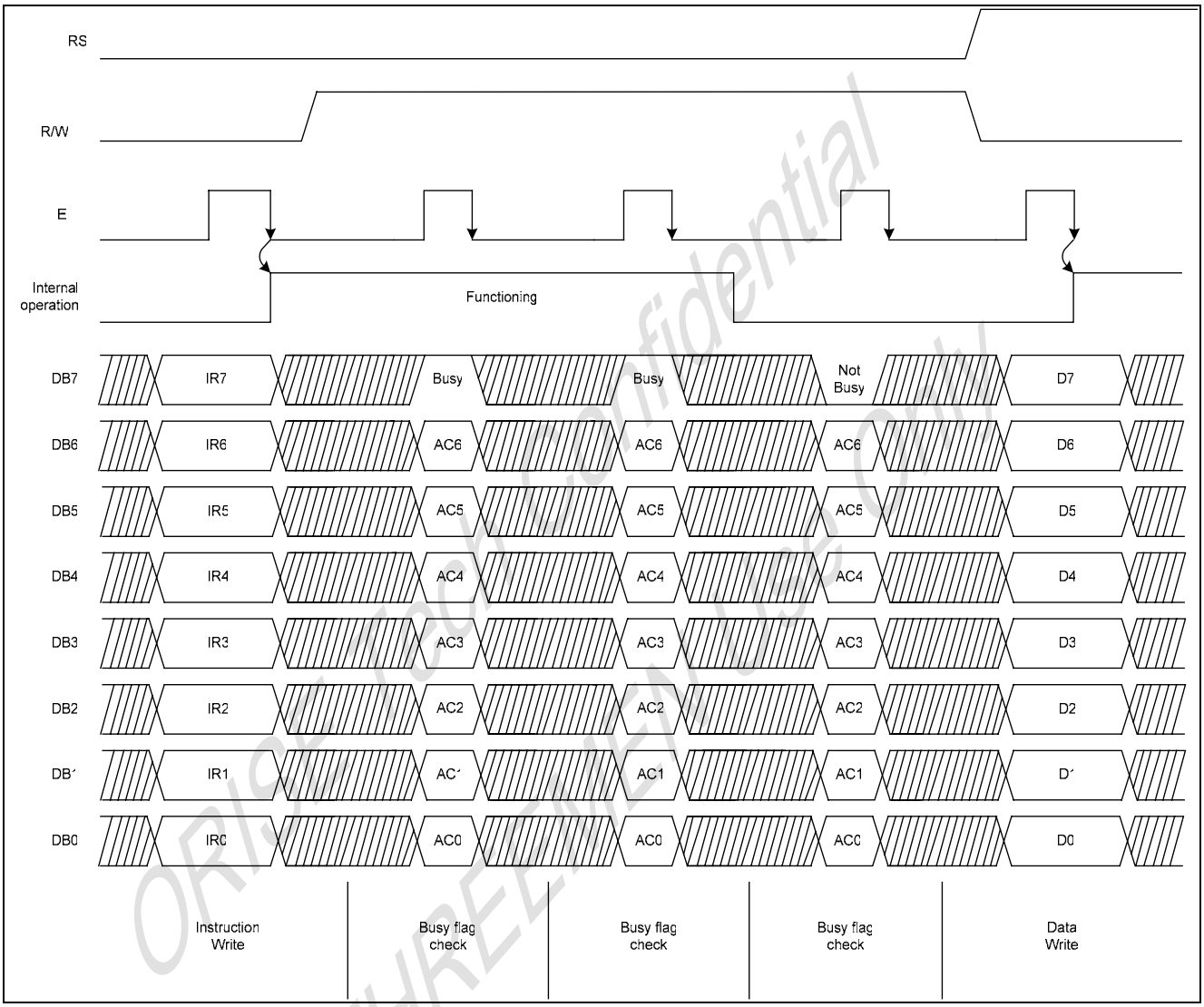


Figure 6-28: Example of 8-bit Data Transfer Timing Sequence

6.15. Supply Voltage for LCD Drive

LCD bias can be selected by open/short V2 and V3 pins.

Duty Factor / Supply Voltage	1/8, 1/11	1/16
	1/4	1/5
V2, V3	Short	Open

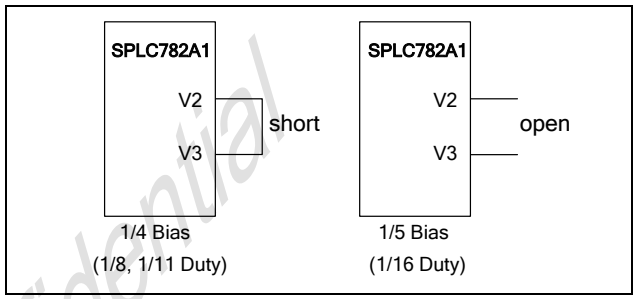
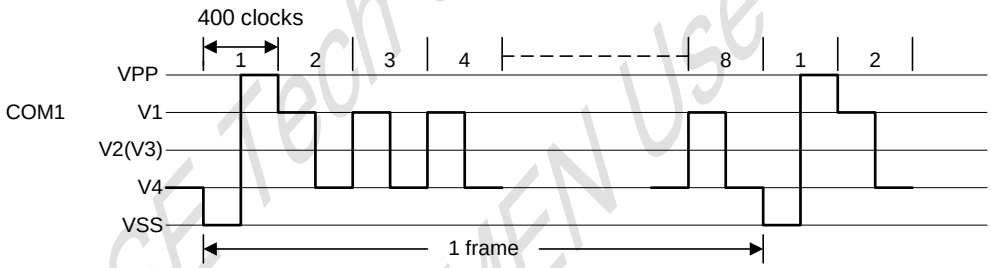


Figure 6-29: Supply Voltage for LCD Drive

6.15.1. The relations between LCD frame′s frequency and oscillator′s frequency

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0μs)

6.15.2. 1/8 Duty, type-A waveform

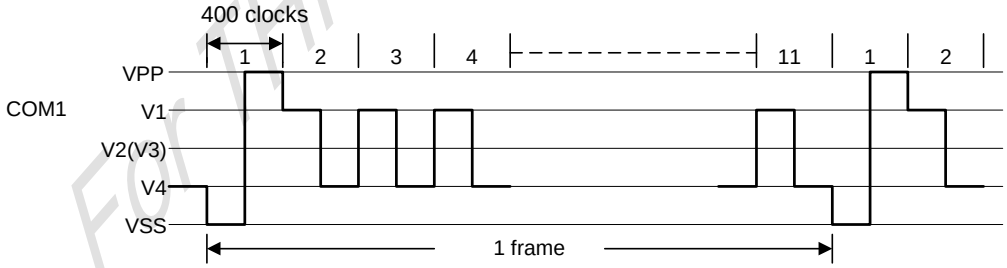


1 frame = 4 (μs) x 400 x 8 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

Figure 6-30: 1/8 Duty type-A waveform

6.15.3. 1/11 Duty, type-A waveform

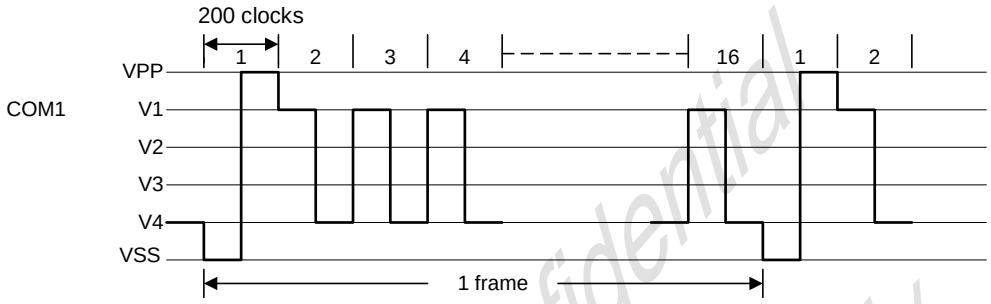


1 frame = 4 (μs) x 400 x 11 = 17600 (μs) = 17.6 ms

Frame frequency = $\frac{1}{17.6\ (ms)}$ = 56.8 (Hz)

Figure 6-31: 1/11 Duty type-A waveform

6.15.4. 1/16 Duty, type-A waveform

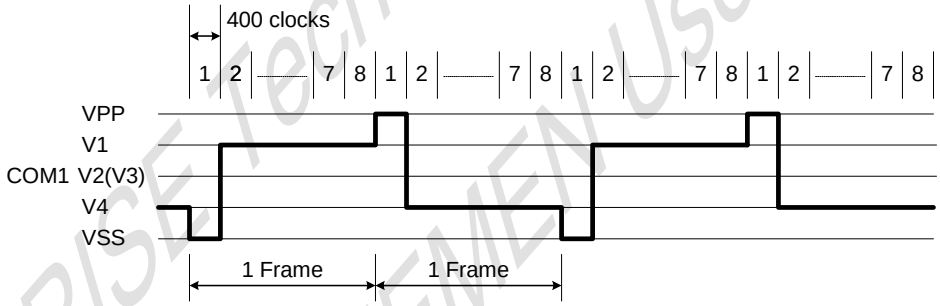


1 frame = 4 (μs) x 200 x 16 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

Figure 6-32: 1/16 Duty type-A waveform

6.15.5. 1/8 Duty, type-B waveform

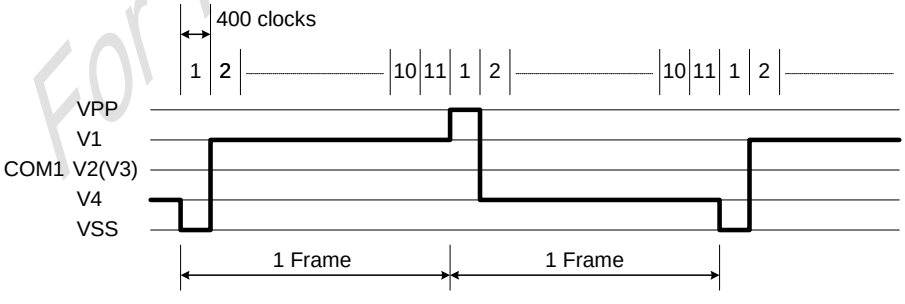


1 frame = 4(μs) x 400 x 8 = 12800(μs) = 12.8ms

Framefrequency = $\frac{1}{12.8(ms)}$ = 78.1(Hz)

Figure 6-33: 1/8 Duty type-B waveform

6.15.6. 1/11 Duty, type-B waveform



1 frame = 4(μs) x 400 x 11 = 17600(μs) = 17.6ms

Framefrequency = $\frac{1}{17.6(ms)}$ = 56.8(Hz)

Figure 6-34: 1/11 Duty type-B waveform

6.15.7. 1/16 Duty, type-B waveform

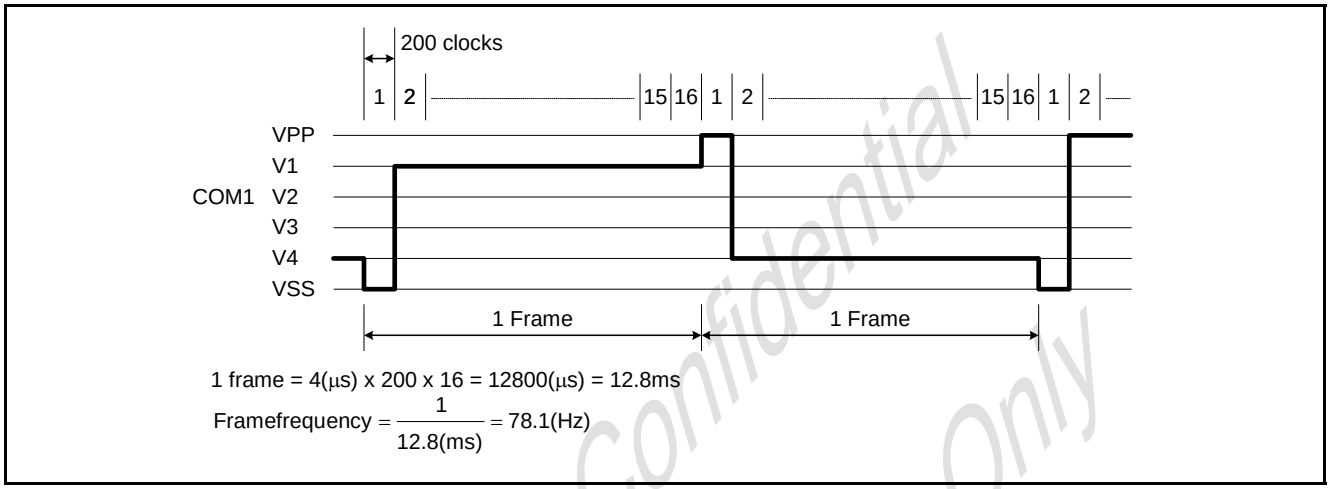


Figure 6-35: 1/16 Duty type-B waveform

6.16. Register --- IR (Instruction Register) and DR (Data Register)

SPLC782A1 has two 8-bit registers - IR (instruction register) and DR (data register). In the followings, we can use the combinations of the RS pin and the R/W pin to select the IR and DR.

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

6.17. Busy Flag (BF)

When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag = 1, SPLC782A1 is in busy state and does not accept any instructions until the busy flag = 0.

6.18. Address Counter (AC)

The address counter assigns addresses to display data RAM and character generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing into (or reading from)display data RAM or character generator RAM, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB0 - DB6 when RS = 0 and R/W = 1.

6.19. Segment Data Direction

SHL is the segment data shift direction control pin.

LCD data is shifted from SEG1 to SEG80 by connecting SHL to VSS, and is reversed by connecting SHL to VDD.

6.20. Common Data Direction

DIRC is the common data shift direction control pin.

LCD common scan sequence from COM1 to COM16 by connecting DIRC to VSS, and is reversed by connecting DIRC to VDD.

6.21. I/O Port Configuration

6.21.1. Input port: E

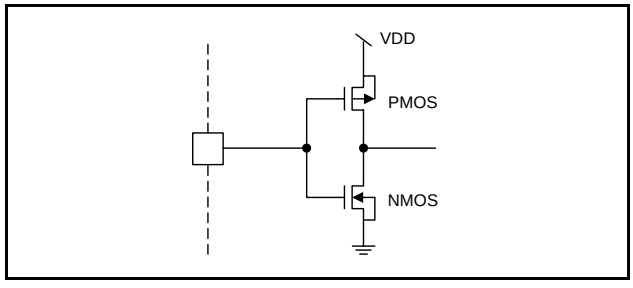


Figure 6-36: Input port: E Configuration

6.21.2. Input port: R/W, RS

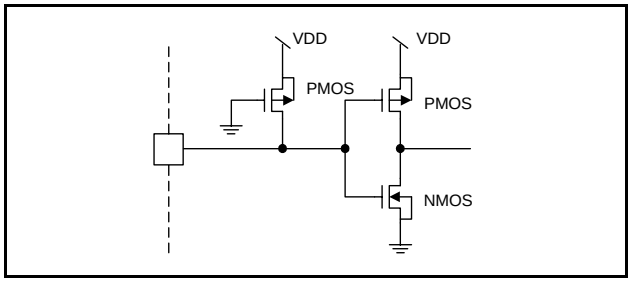


Figure 6-37: Input port: R/W, RS Configuration

6.21.3. Output port: CL2, D

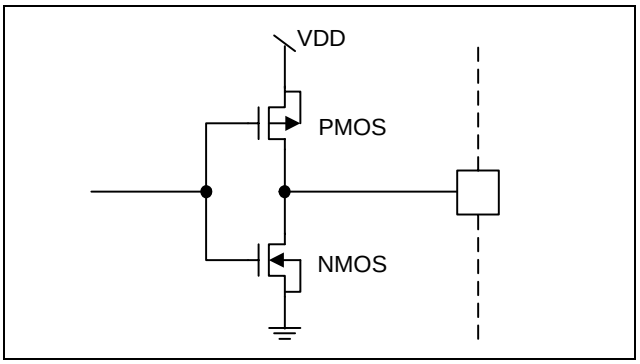


Figure 6-38: Output port: CL2, D Configuration

6.21.4. Input / Output port: DB0 - DB7

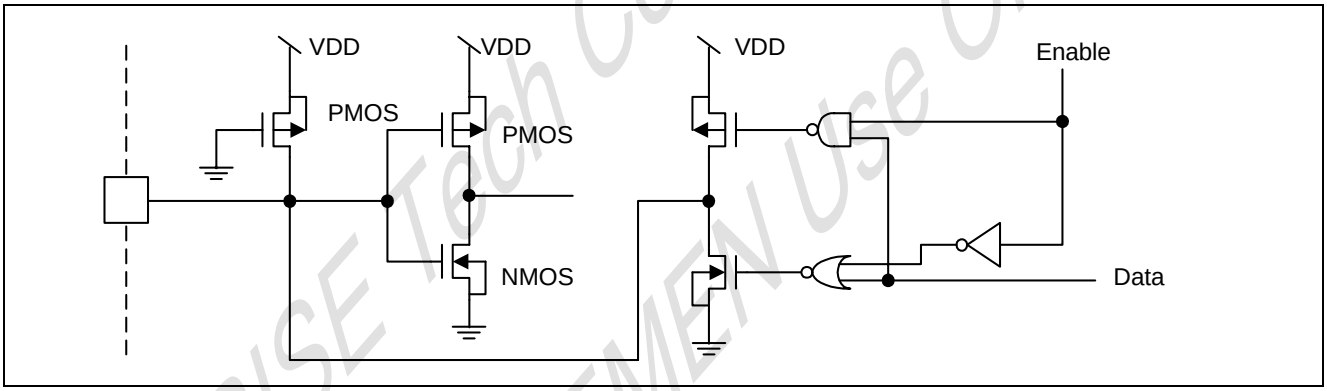


Figure 6-39: Input/Output port: DB0-DB7 Configuration

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{PP}	-0.3V to +7.0V
Input Voltage Range	V_{IN}	-0.3V to VDD +0.3V
Operating Temperature	T_A	-20℃ to +75℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 2.4V to 4.5V, T_A = -20℃ to +75℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	4.5	V	
Operating Current	I_{DD1}	-	0.15	0.25	mA	No access from MPU **(Note1)**
	I_{DD2}	-	0.18	0.48	mA	Access operation from MPU (F_{CYC} = 500KHz)**(Note1)**
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.55	V	
Input High Current	I_{IH}	-	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-5.0	-30	-100	μA	
Output High Voltage	V_{OH1}	0.75VDD	-	VDD	V	I_{OH} = - 0.1mA, Pins: DB0 - DB7
Output Low Voltage	V_{OL1}	-	-	0.2VDD	V	I_{OL} = 0.1mA, Pins: DB0 - DB7
Voltage Drop	V_{DCOM}	-	-	1.0	V	I_O = 0.1mA, Pins: COM1 - COM16
	V_{DSEG}	-	-	1.0	V	I_O = 0.1mA, Pins: SEG1 - SEG80
Operating Current	I_{PP}	-	0.35	0.45	mA	V_{PP} = 6.0V **(Note2)**
LCD Voltage	V_{PP}	3.0	-	6.0	V	1/4 bias or 1/5 bias

Note1: Typ. condition VDD = 3.0V @ 25℃, Max. condition VDD = 4.5V @ -20℃

Note2: Typ. condition VPP = 6.0V @ 25℃, Max. condition VPP = 6.0V @ -20℃

7.3. DC Characteristics (VDD = 4.5V to 5.5V, T_A = -20℃ to +75℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	4.5	-	5.5	V	
Operating Current	I_{DD1}	-	0.25	0.35	mA	No access from MPU **(Note1)**
	I_{DD2}	-	0.45	0.7	mA	Access operation from MPU (F_{CYC} = 500KHz)**(Note1)**
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Current	I_{IH}	-	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-30	-80	-150	μA	
Output High Voltage (TTL)	V_{OH1}	2.4	-	VDD	V	I_{OH} = - 0.1mA, Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA, Pins: DB0 - DB7
Voltage Drop	V_{DCOM}	-	-	1.0	V	I_O = 0.1mA, Pins: COM1 - COM16
	V_{DSEG}	-	-	1.0	V	I_O = 0.1mA, Pins: SEG1 - SEG80
Operating Current	I_{PP}	-	0.35	0.45	mA	V_{PP} = 6.0V **(Note2)**
LCD Voltage	V_{PP}	3.0	-	6.0	V	1/4 bias or 1/5 bias

Note1: Typ. condition VDD = 5.0V @ 25℃, Max. condition VDD = 5.5V @ -20℃

Note2: Typ. condition VPP = 6.0V @ 25℃, Max. condition VPP = 6.0V @ -20℃

7.4. AC Characteristics (VDD = 4.5V to 5.5V, T_A = -20℃ to +75℃)

7.4.1. Internal clock operation (T_A = 25℃, the oscillator frequency chart can be reference on Figure 6-3)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

7.4.2. LCD bias resistor (T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 - R5	3.0	5.0	7.0	K-ohm

7.4.3. Write mode (Writing data from MPU to SPLC782A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	80	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

7.4.4. Read mode (Reading Data from SPLC782A1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_W	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	160	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pins: DB0 - DB7

7.5. AC Characteristics (VDD = 2.4V to 4.5V, T_A = -20℃ to +75℃)

7.5.1. Internal clock operation (T_A = 25℃, the oscillator frequency chart can be reference on Figure 6-3)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

7.5.2. LCD bias resistor (T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 - R5	3.0	5.0	7.0	K-ohm

7.5.3. Write mode (Writing data from MPU to SPLC782A1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	650	-	-	ns	Pin E
E Pulse Width	t_{PW}	300	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

7.5.4. Read mode (Reading data from SPLC782A1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1250	-	-	ns	Pin E
E Pulse Width	t_W	600	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

7.6. Write Mode Timing Diagram (Writing Data from MPU to SPLC782A1)

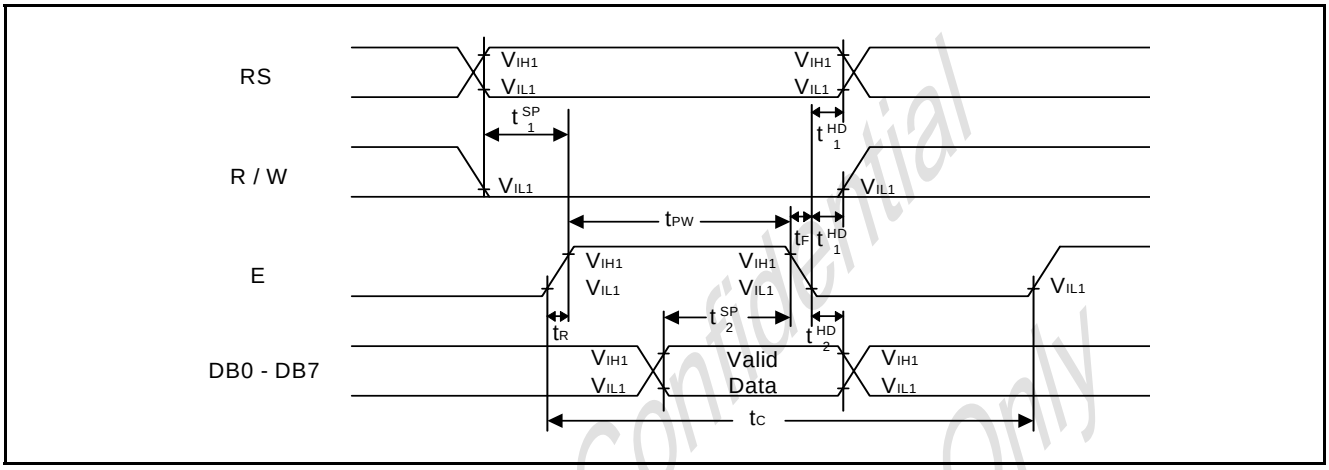


Figure 7-1: Write Mode Timing Diagram

7.7. Read Mode Timing Diagram (Reading Data from SPLC782A1 to MPU)

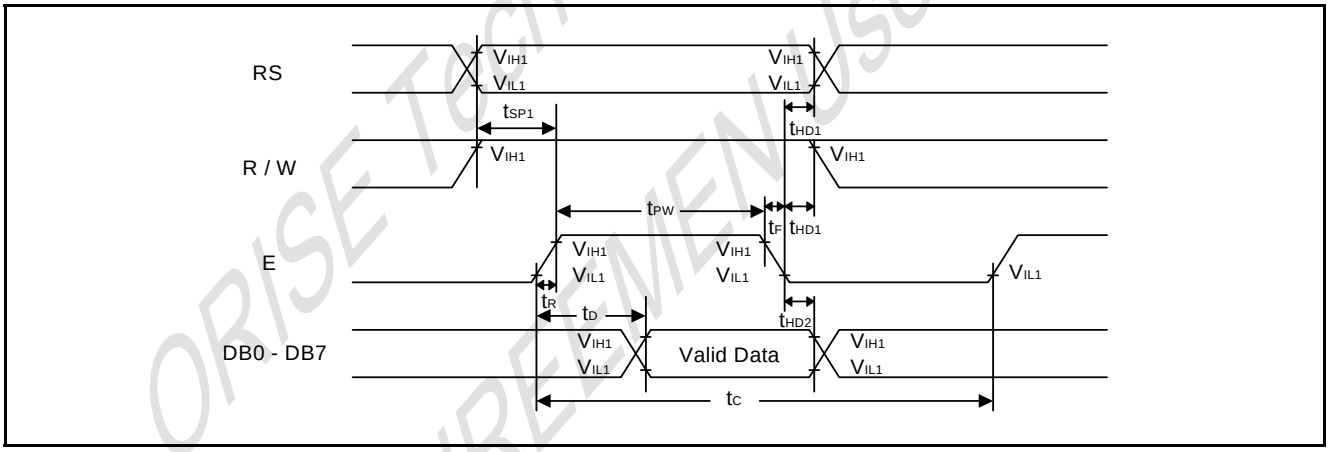
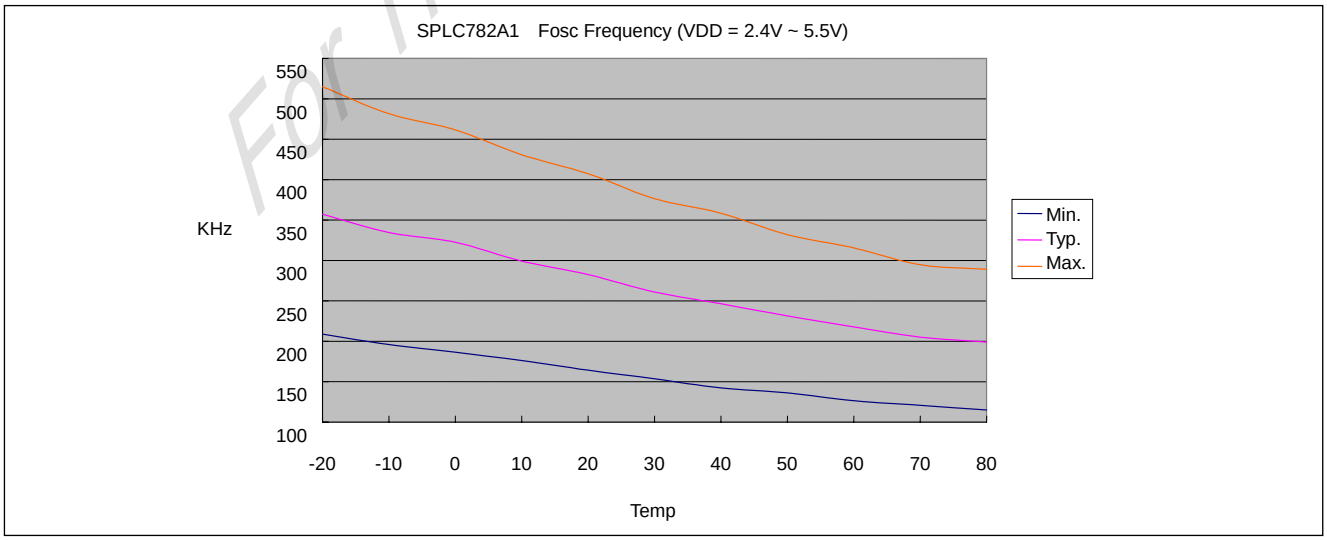


Figure 7-2: Read Mode Timing Diagram

7.8. The Following Graps Show the Relationship Between F_{OSC} and Temperature



F_{OSC} (Max.) = 515KHz @ VDD = 5.5V, Temp = -20℃
F_{OSC} (Min.) = 114KHz @ VDD = 2.4V, Temp = 80℃

Figure 7-3: The Relationship Between Fosc and Temperature

8. APPLICATION CIRCUITS

8.1. Interface to MPU

8.1.1. Interface to 8-bit MPU (6805)

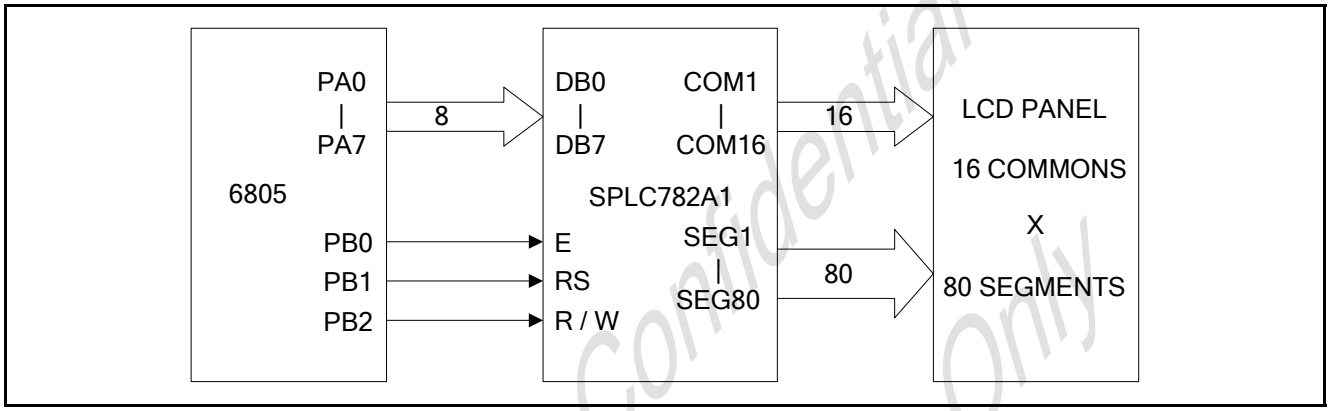


Figure 8-1: Interface to 8-bit MPU (6805)

8.1.2. Interface to 8-bit MPU (Z80)

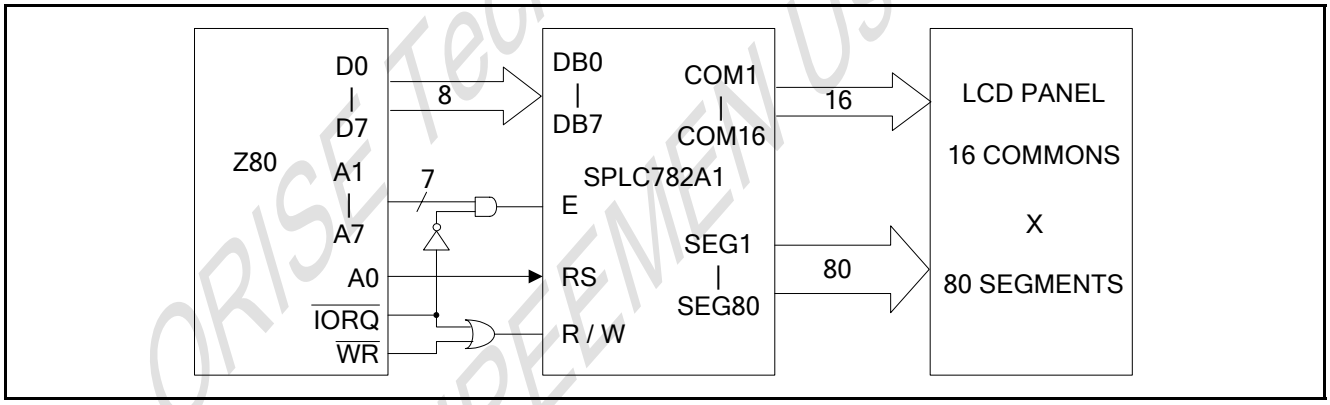


Figure 8-2: Interface to 8-bit MPU (Z80)

8.2. Applications for LCD

8.2.1. Chip bottom & lower view (DIRC = "0", SHL = "0")

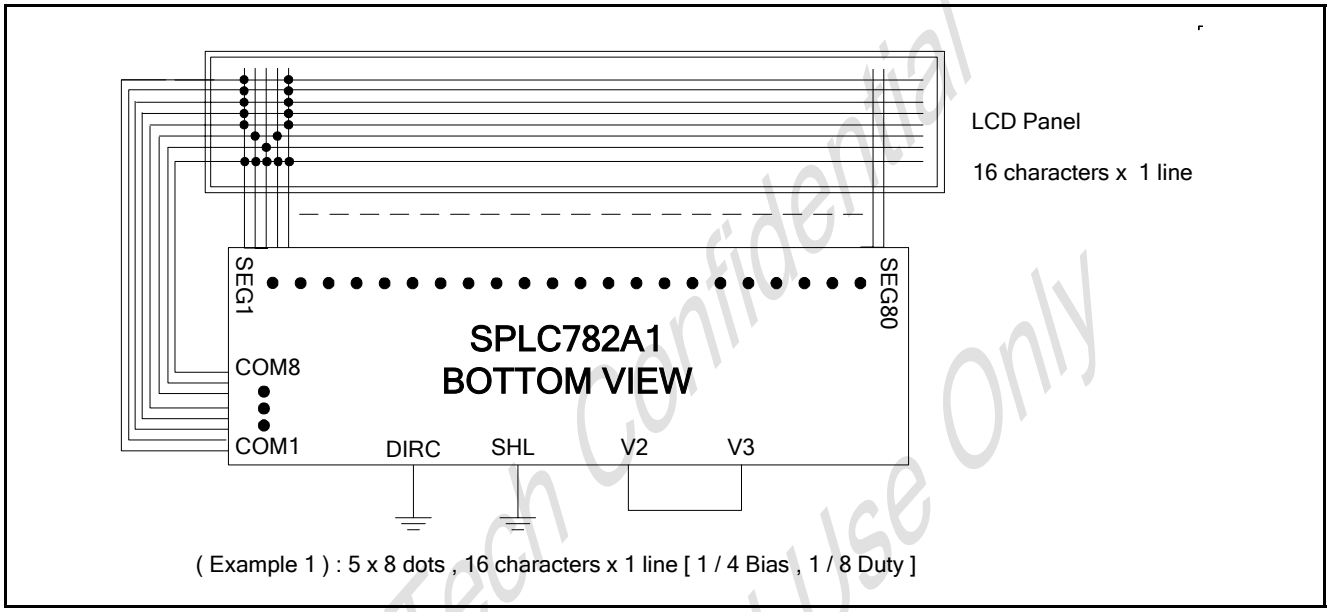


Figure 8-3: Chip Bottom & Lower View (Example 1)

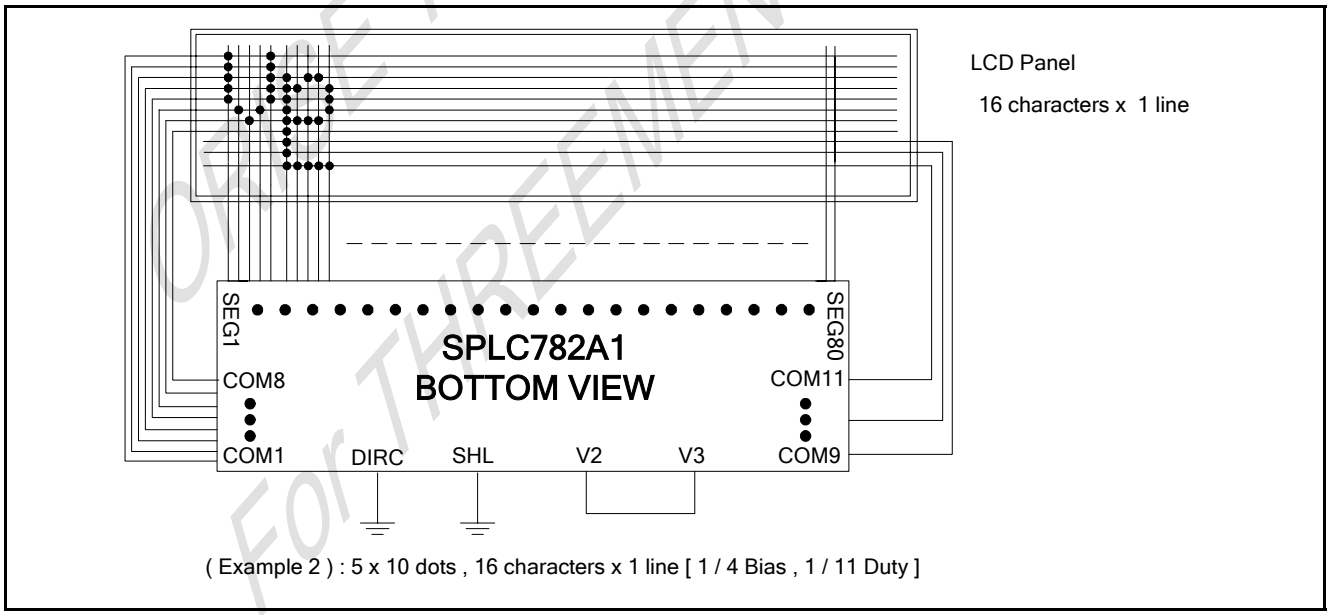


Figure 8-4: Chip Bottom & Lower View (Example 2)]

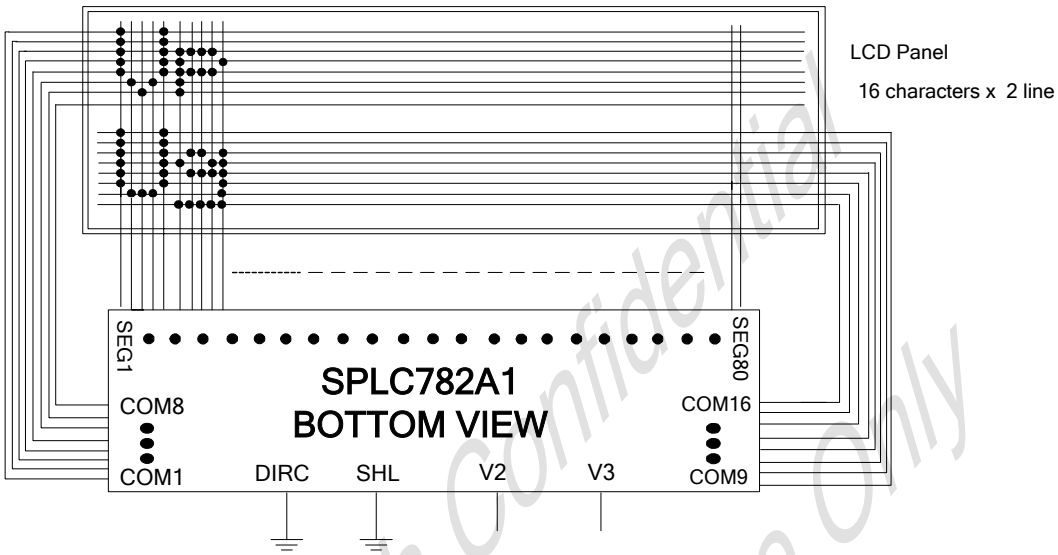


Figure 8-5: Chip Bottom & Lower View (Example 3)

8.2.2. Chip bottom & upper view (DIRC = "1", SHL = "1")

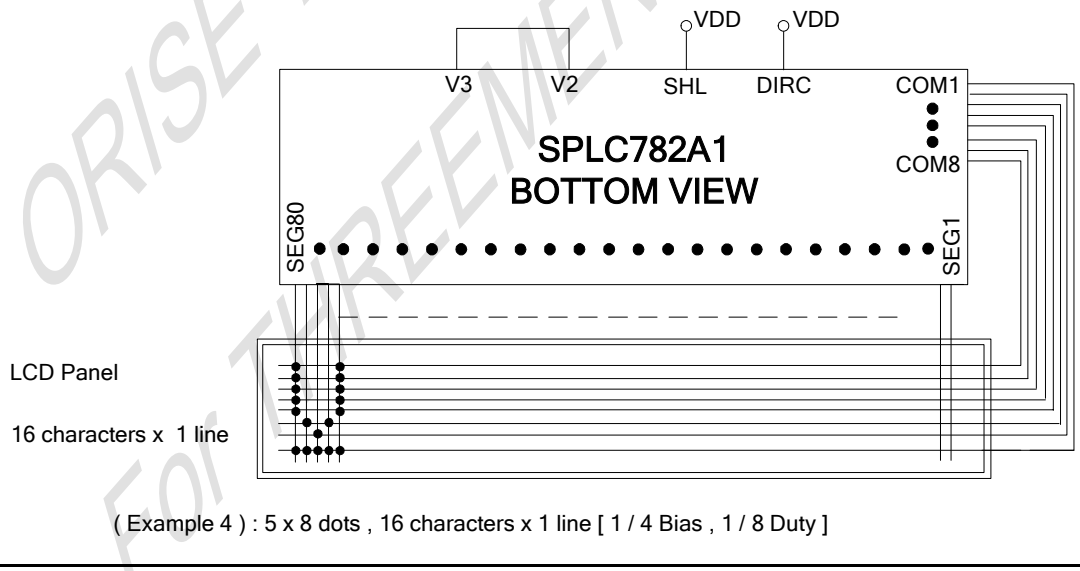


Figure 8-6: Chip Bottom & Upper View (Example 4)

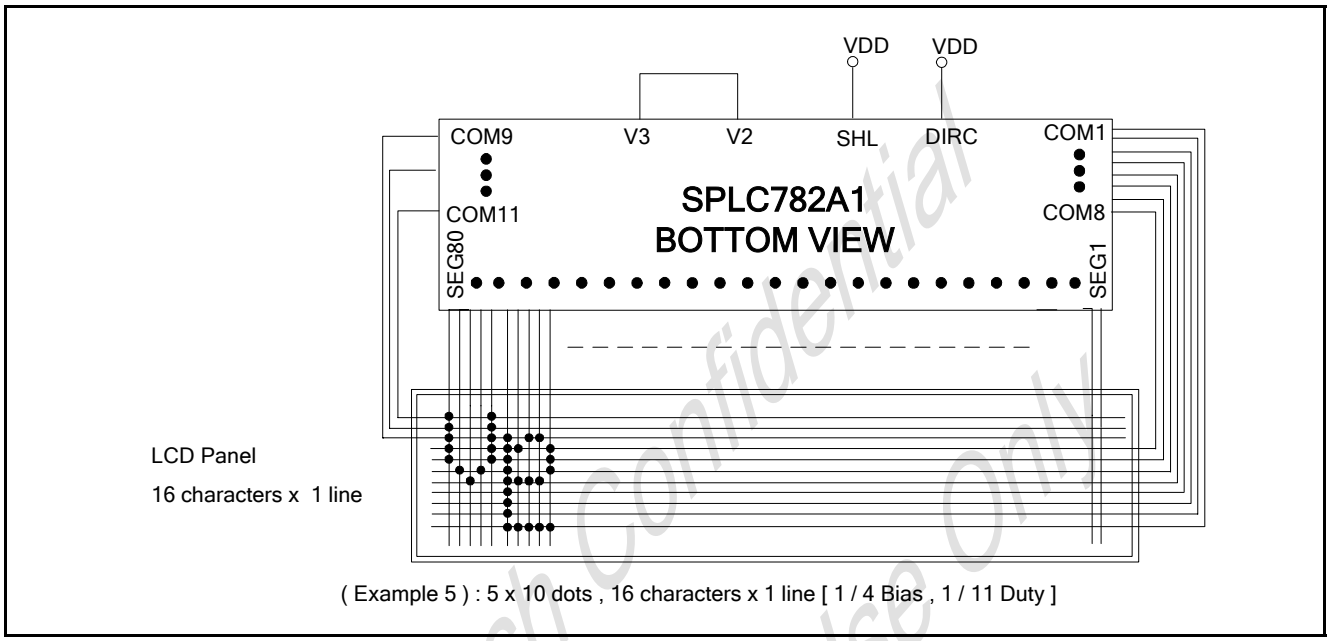


Figure 8-7: Chip Bottom & Upper View (Example 5)

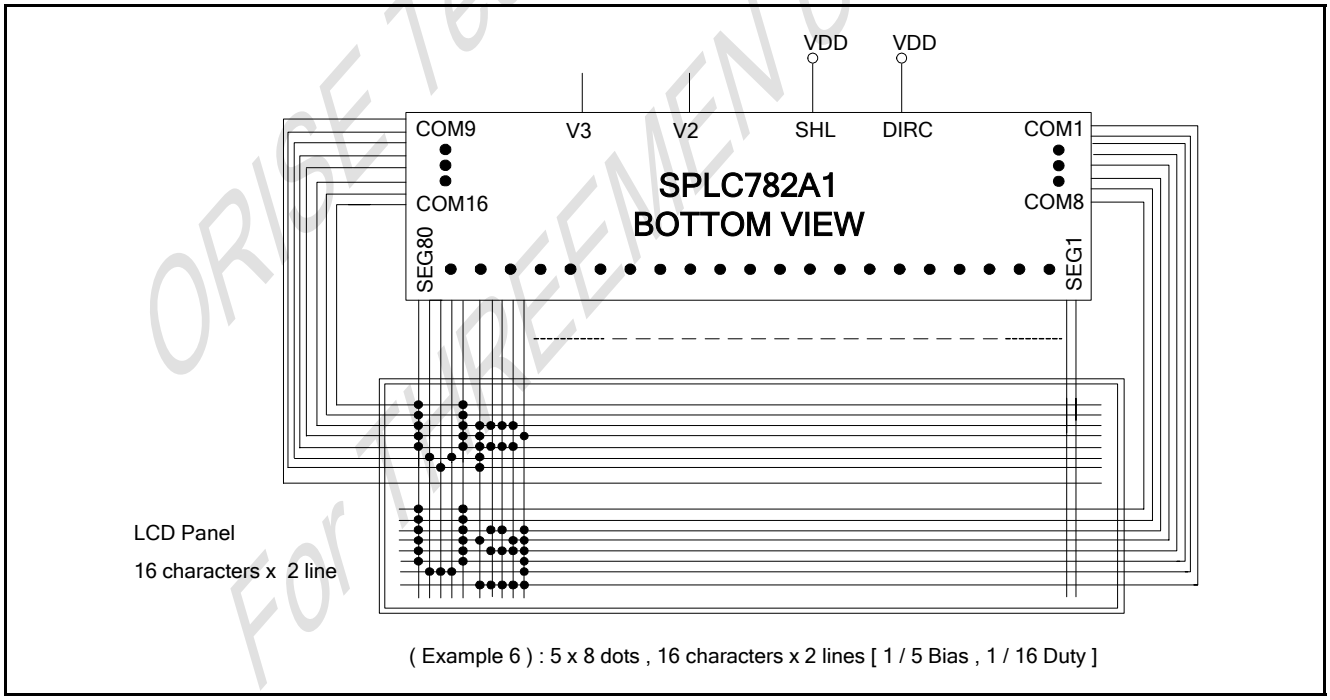


Figure 8-8: Chip Bottom & Upper View (Example 6)

8.2.3. Chip top & lower view (DIRC = "0", SHL = "1")

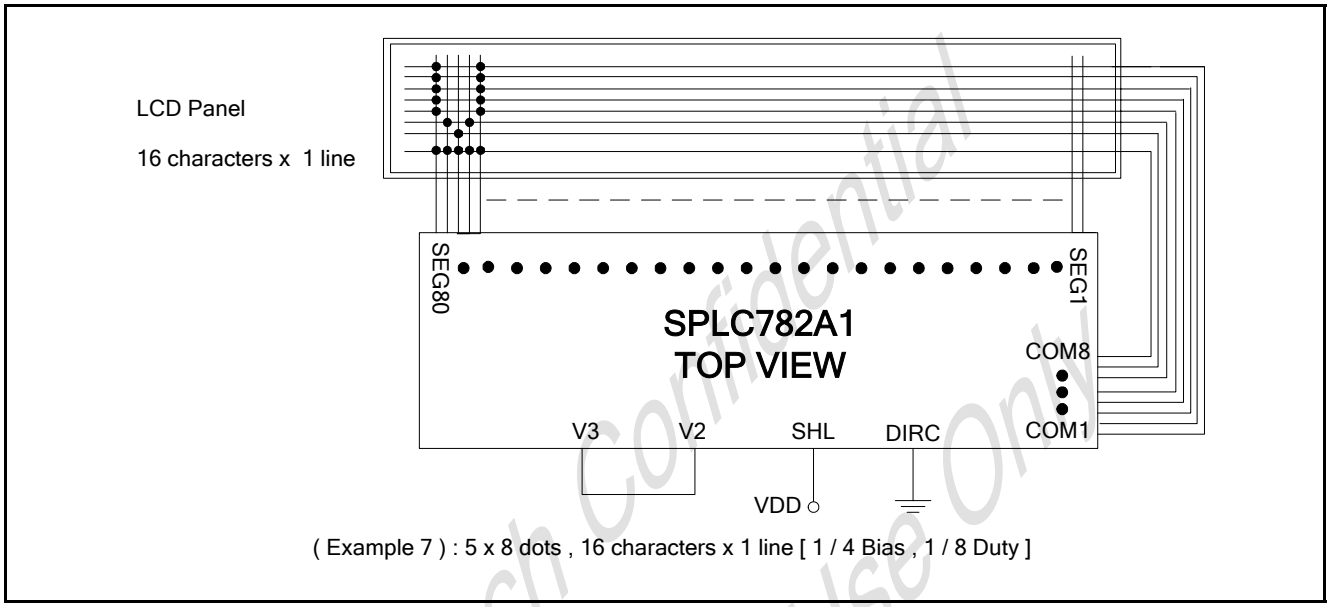


Figure 8-9: Chip Top & Lower View (Example 7)

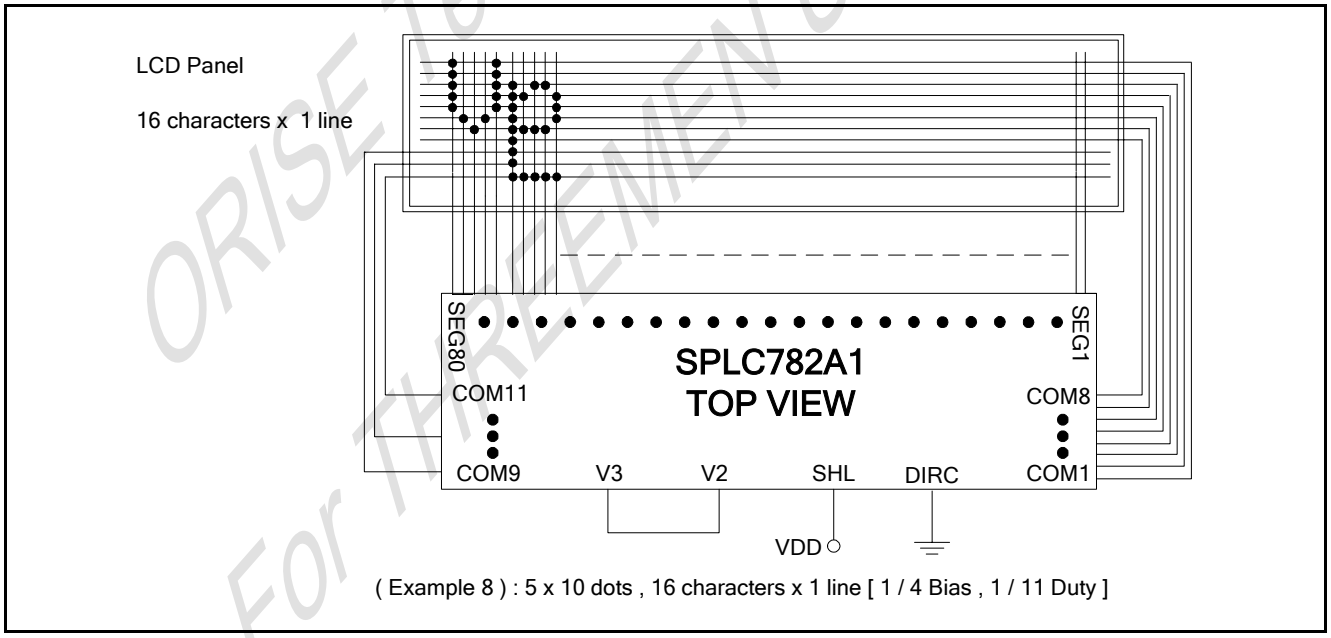


Figure 8-10: Chip Top & Lower View (Example 8)

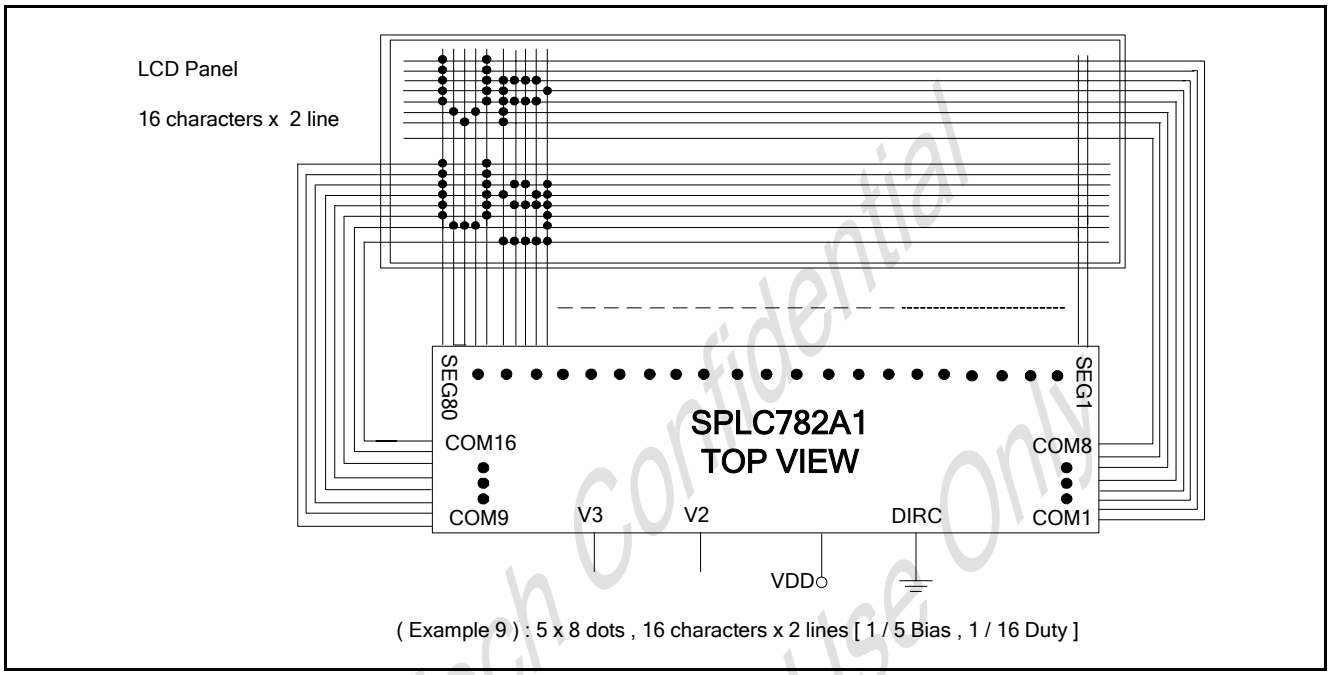


Figure 8-11: Chip Top & Lower View (Example 9)

8.2.4. Chip top & upper view (DIRC = "1", SHL = "0")

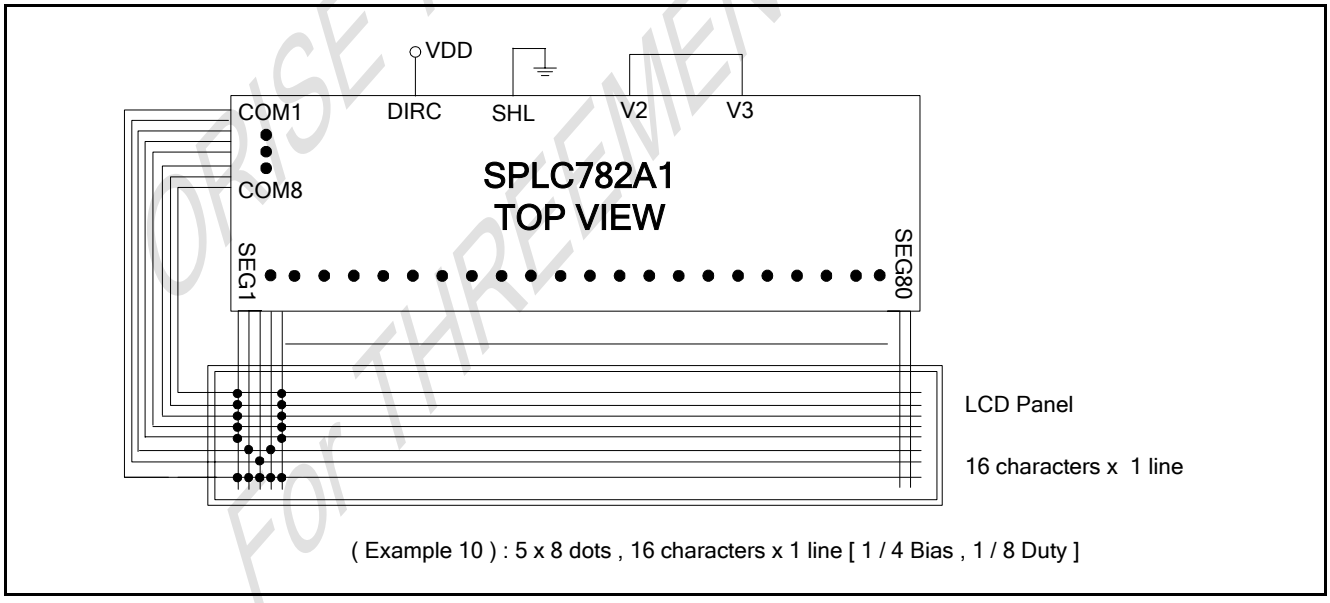
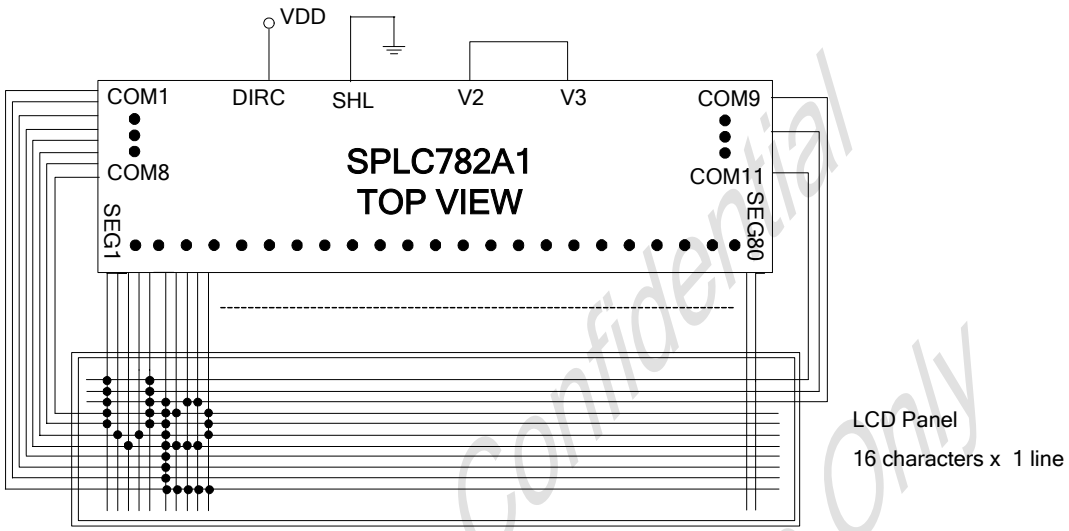
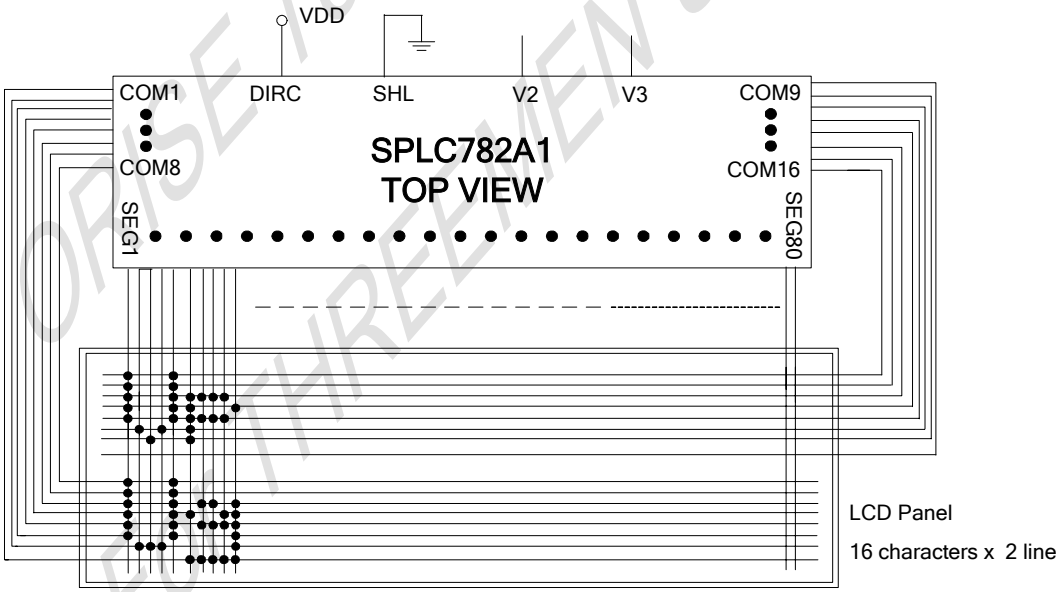


Figure 8-12: Chip Top & Upper View (Example 10)



(Example 11) : 5 x 10 dots , 16 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]

Figure 8-13: Chip Top & Upper View (Example 11)



(Example 12) : 5 x 8 dots , 16 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]

Figure 8-14: Chip Top & Upper View (Example 12)

9. CHARACTER GENERATOR ROM

9.1. SPLC782A1 - 016

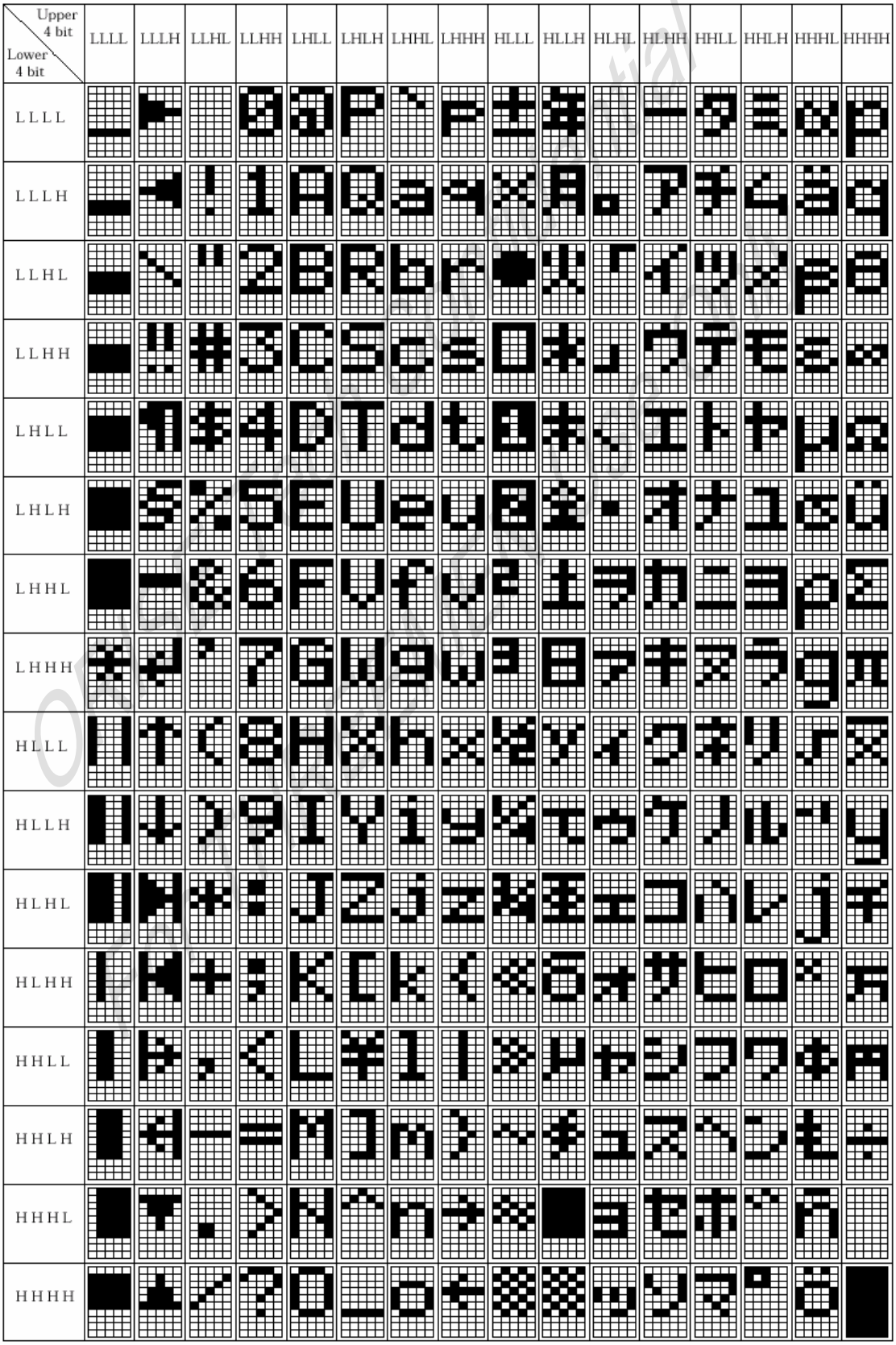


Figure 9-1: CGROM (SPLC782A1-016)

9.2. SPLC782A1 - 022

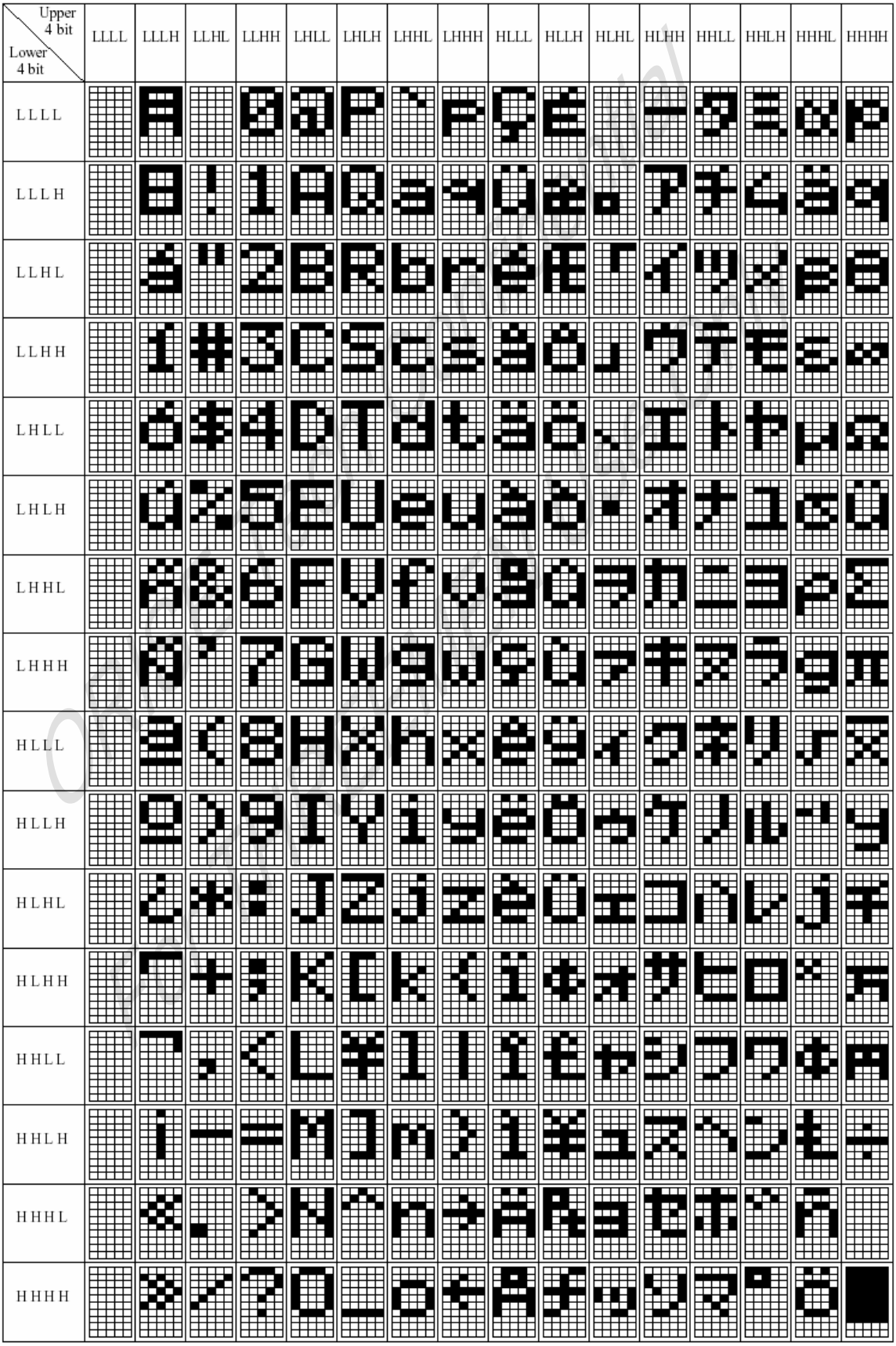
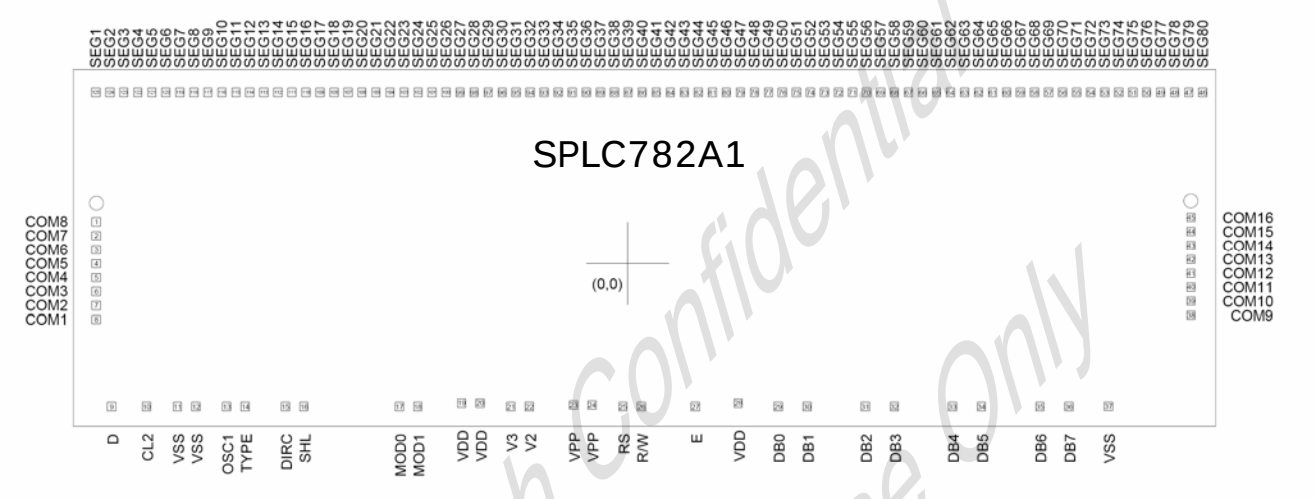


Figure 9-2: CGROM (SPLC782A1-022)

10. CHIP INFORMATION

10.1. PAD Assignment



10.2. PAD Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	5070 ± 25	1640 ± 25	μm
Chip thickness	-	635 ± 25		
PAD Pitch	1 - 8 38 - 45	0	61.2	
	46 - 125	61.2	0	
Bumped PAD Size	1 - 8 38 - 45	85.1	40.3	
	46 - 125	40.3	85.1	
	9 - 37	59.2	112.0	

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

10.3. Bump Characteristic

Item	Standard	Note
Bump Hardness	50HV	± 20HV
Bump Height	18μm	± 3μm
Co-planarity (in Chip)	R≦ 2μm	R : Max-Min
Roughness (in Bump)	R≦ 2μm	R : Max-Min
Bump Size	"X" ± 4μm x "Y" ± 4μm	X/Y: bump size
Shear Force	>4.5g/mil^2	

10.4. PAD Locations

PAD No.	PAD Name	X	Y
1	COM8	-2394.675	115.29
2	COM7	-2394.675	54.09
3	COM6	-2394.675	-7.11
4	COM5	-2394.675	-68.31
5	COM4	-2394.675	-129.51
6	COM3	-2394.675	-190.71
7	COM2	-2394.675	-251.91
8	COM1	-2394.675	-313.11
9	D	-2326.995	-694.44
10	CL2	-2174.715	-694.44
11	VSS	-2040.255	-694.44
12	VSS	-1959.525	-694.44
13	OSC1	-1825.065	-694.44
14	TYPE	-1744.335	-694.44
15	DIRC	-1568.115	-694.44
16	SHL	-1487.385	-694.44
17	MOD0	-1071.045	-694.44
18	MOD1	-990.315	-694.44
19	VDD	-799.155	-678.60
20	VDD	-718.425	-678.60
21	V3	-583.965	-694.44
22	V2	-503.235	-694.44
23	VPP	-309.915	-687.42
24	VPP	-229.185	-687.42
25	RS	-94.455	-694.44
26	R/W	-13.725	-694.44
27	E	222.075	-694.44
28	VDD	409.725	-678.60
29	DB0	582.975	-694.44
30	DB1	709.875	-694.44
31	DB2	964.035	-694.44
32	DB3	1090.935	-694.44
33	DB4	1345.095	-694.44
34	DB5	1471.995	-694.44
35	DB6	1726.155	-694.44
36	DB7	1853.055	-694.44
37	VSS	2026.305	-693.09
38	COM9	2387.205	-294.75
39	COM10	2387.205	-233.55
40	COM11	2387.205	-172.35
41	COM12	2387.205	-111.15
42	COM13	2387.205	-49.95
43	COM14	2387.205	11.25
44	COM15	2387.205	72.45
45	COM16	2387.205	133.65
46	SEG80	2438.325	679.68
47	SEG79	2377.125	679.68
48	SEG78	2315.925	679.68
49	SEG77	2254.725	679.68
50	SEG76	2193.525	679.68
51	SEG75	2132.325	679.68

PAD No.	PAD Name	X	Y
52	SEG74	2071.125	679.68
53	SEG73	2009.925	679.68
54	SEG72	1948.725	679.68
55	SEG71	1887.525	679.68
56	SEG70	1826.325	679.68
57	SEG69	1765.125	679.68
58	SEG68	1703.925	679.68
59	SEG67	1642.725	679.68
60	SEG66	1581.525	679.68
61	SEG65	1520.325	679.68
62	SEG64	1459.125	679.68
63	SEG63	1397.925	679.68
64	SEG62	1336.725	679.68
65	SEG61	1275.525	679.68
66	SEG60	1214.325	679.68
67	SEG59	1153.125	679.68
68	SEG58	1091.925	679.68
69	SEG57	1030.725	679.68
70	SEG56	969.525	679.68
71	SEG55	908.325	679.68
72	SEG54	847.125	679.68
73	SEG53	785.925	679.68
74	SEG52	724.725	679.68
75	SEG51	663.525	679.68
76	SEG50	602.325	679.68
77	SEG49	541.125	679.68
78	SEG48	479.925	679.68
79	SEG47	418.725	679.68
80	SEG46	357.525	679.68
81	SEG45	296.325	679.68
82	SEG44	235.125	679.68
83	SEG43	173.925	679.68
84	SEG42	112.725	679.68
85	SEG41	51.525	679.68
86	SEG40	-9.675	679.68
87	SEG39	-70.875	679.68
88	SEG38	-132.075	679.68
89	SEG37	-193.275	679.68
90	SEG36	-254.475	679.68
91	SEG35	-315.675	679.68
92	SEG34	-376.875	679.68
93	SEG33	-438.075	679.68
94	SEG32	-499.275	679.68
95	SEG31	-560.475	679.68
96	SEG30	-621.675	679.68
97	SEG29	-682.875	679.68
98	SEG28	-744.075	679.68
99	SEG27	-805.275	679.68
100	SEG26	-866.475	679.68
101	SEG25	-927.675	679.68
102	SEG24	-988.875	679.68

PAD No.	PAD Name	X	Y
103	SEG23	-1050.075	679.68
104	SEG22	-1111.275	679.68
105	SEG21	-1172.475	679.68
106	SEG20	-1233.675	679.68
107	SEG19	-1294.875	679.68
108	SEG18	-1356.075	679.68
109	SEG17	-1417.275	679.68
110	SEG16	-1478.475	679.68
111	SEG15	-1539.675	679.68
112	SEG14	-1600.875	679.68
113	SEG13	-1662.075	679.68
114	SEG12	-1723.275	679.68

PAD No.	PAD Name	X	Y
115	SEG11	-1784.475	679.68
116	SEG10	-1845.675	679.68
117	SEG9	-1906.875	679.68
118	SEG8	-1968.075	679.68
119	SEG7	-2029.275	679.68
120	SEG6	-2090.475	679.68
121	SEG5	-2151.675	679.68
122	SEG4	-2212.875	679.68
123	SEG3	-2274.075	679.68
124	SEG2	-2335.275	679.68
125	SEG1	-2396.475	679.68

10.5. Align Key Location

X	Y	Description
-2394.675	186.389	Marked with 29.08μm diameter spot
2387.204	186.389	Marked with 29.08μm diameter spot

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12. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 02, 2007	0.1	Original	41