DATA SHEET

SPLC100B1

40-Channel SEG/COM LCD Driver

Preliminary

SEP. 21, 2007

Version 0.1

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40-CHANNEL SEG/COM LCD DRIVER

1. GENERAL DESCRIPTION

The SPLC100B1 is a Liquid Crystal Display driver that contains two sets of 20-bit bi-directional shift registers, 20 data latch flip-flops and 20 Liquid Crystal Display drivers. It also features 40-channel outputs that can be applied as common or segment driver. The SPLC100B1 receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

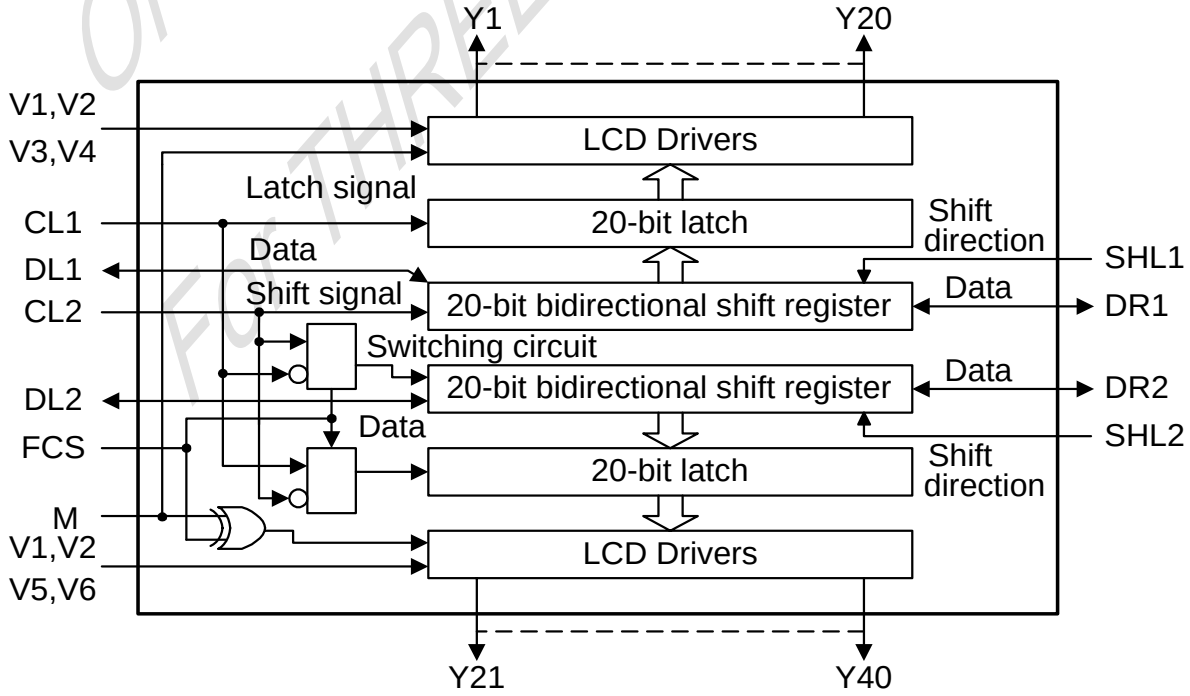
2. FEATURES

- Liquid Crystal Display driver with serial/parallel conversion function.
- Serial transfer facilitates board design.
- Capable of interfacing to liquid crystal display controllers: HD43160AH, HD61830, HD44780, HD44790, SPLC780
- 40 internal LCD drivers.
- Internal serial/parallel conversion circuits:
  - 20-bit shift register × 2
  - 20-bit latch × 2
- Power supply:
  - Internal logic: 2.7V - 5.5V
  - Liquid crystal display driver circuit: 3.0V - 8V
- CMOS process.
- Package form: 64 QFP or bare chip available

3. ORDERING INFORMATION

Product Number	Package Type
SPLC100B1-C	Chip form
SPLC100B1-HQ041	Green Package form - QFP 64L

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Mnemonic</th><th>PIN No.</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD</td><td>22</td><td>I</td><td>Positive power supply voltage input</td></tr>
<tr><td>VSS</td><td>32</td><td>I</td><td>Ground input</td></tr>
<tr><td>VEE</td><td>29</td><td>I</td><td>Power supply voltage for liquid crystal display drive</td></tr>
<tr><td>Y1 - Y6
Y7 - Y20</td><td>28 - 23
21 - 8</td><td>O</td><td>Liquid crystal driver output (Channel 1)</td></tr>
<tr><td>Y21 - Y27
Y28 - Y40</td><td>7 - 1
59 - 47</td><td>O</td><td>Liquid crystal driver output (Channel 2)</td></tr>
<tr><td>V1, V2</td><td>41, 42</td><td>I</td><td>Power supply for liquid crystal display drive (Select level)</td></tr>
<tr><td>V3, V4</td><td>43, 44</td><td>I</td><td>Power supply for liquid crystal display drive (Non-select level for channel 1)</td></tr>
<tr><td>V5, V6</td><td>45, 46</td><td>I</td><td>Power supply for liquid crystal display drive (Non-select level for channel 2)</td></tr>
<tr><td>SHL1</td><td>38</td><td>I</td><td>Selection of the shift direction of channel 1 shift register
<table>
<tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr>
<tr><td>VDD</td><td>Out</td><td>In</td></tr>
<tr><td>GND</td><td>In</td><td>Out</td></tr>
</table></td></tr>
<tr><td>SHL2</td><td>39</td><td>I</td><td>Selection of the shift direction of channel 2 shift register
<table>
<tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr>
<tr><td>VDD</td><td>Out</td><td>In</td></tr>
<tr><td>GND</td><td>In</td><td>Out</td></tr>
</table></td></tr>
<tr><td>DL1, DR1</td><td>33, 34</td><td>I/O</td><td>Data Input / Output of channel 1 shift register</td></tr>
<tr><td>DL2, DR2</td><td>35, 36</td><td>I/O</td><td>Data Input / Output of channel 2 shift register</td></tr>
<tr><td>M</td><td>37</td><td>I</td><td>Alternated signal for liquid crystal driver output</td></tr>
<tr><td>CL1</td><td>30</td><td>I</td><td>Latch signal for channel 1 (↓) *1
Used for channel 2 when FCS is GND</td></tr>
<tr><td>CL2</td><td>31</td><td>I</td><td>Shift signal for channel 1 (↓) *1
Used for channel 2 when FCS is GND</td></tr>
<tr><td>FCS</td><td>40</td><td>I</td><td>Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift of channel 2 and inverts M for channel 2.Thus, this signal exchanges the function of channel 2.
<table>
<tr><td rowspan="2">FCS Level</td><td colspan="2">Channel 2</td><td rowspan="2">M Polarity</td><td rowspan="2">Function</td></tr>
<tr><td>Latch signal</td><td>Shift signal</td></tr>
<tr><td>VDD</td><td>CL2 ↑</td><td>CL1 ↑</td><td>M</td><td>For common drive</td></tr>
<tr><td>GND</td><td>CL1 ↓</td><td>CL2 ↓</td><td>M</td><td>For segment drive</td></tr>
<tr><td></td><td>*1</td><td>*1</td><td></td><td>*2</td></tr>
</table></td></tr>
</table>

Note: *1. ↑ and ↓ indicate the latches at rise and fall times, respectively.

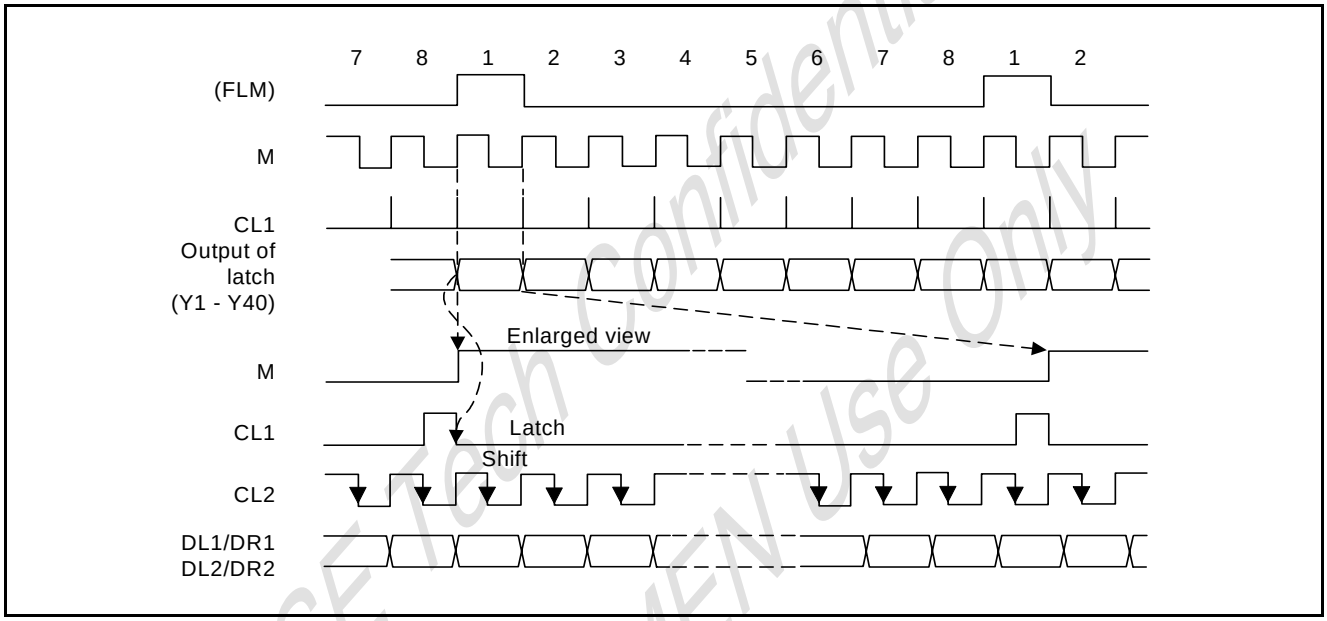
Note: *2. The output level relationship between channel 1 and channel 2 based on the FCS signal level as follows:

FCS	Data	M	Output Level	
			Channel 1(Y1 - Y20)	Channel 2(Y21 - Y40)
VDD (H)	H (Select)	H	V1	V2
		L	V2	V1
	L (Non-select)	H	V3	V6
		L	V4	V5
GND (L)	H (Select)	H	V1	V1
		L	V2	V2
	L (Non-select)	H	V3	V5
		L	V4	V6

6. FUNCTIONAL DESCRIPTIONS

6.1. Segment Driver

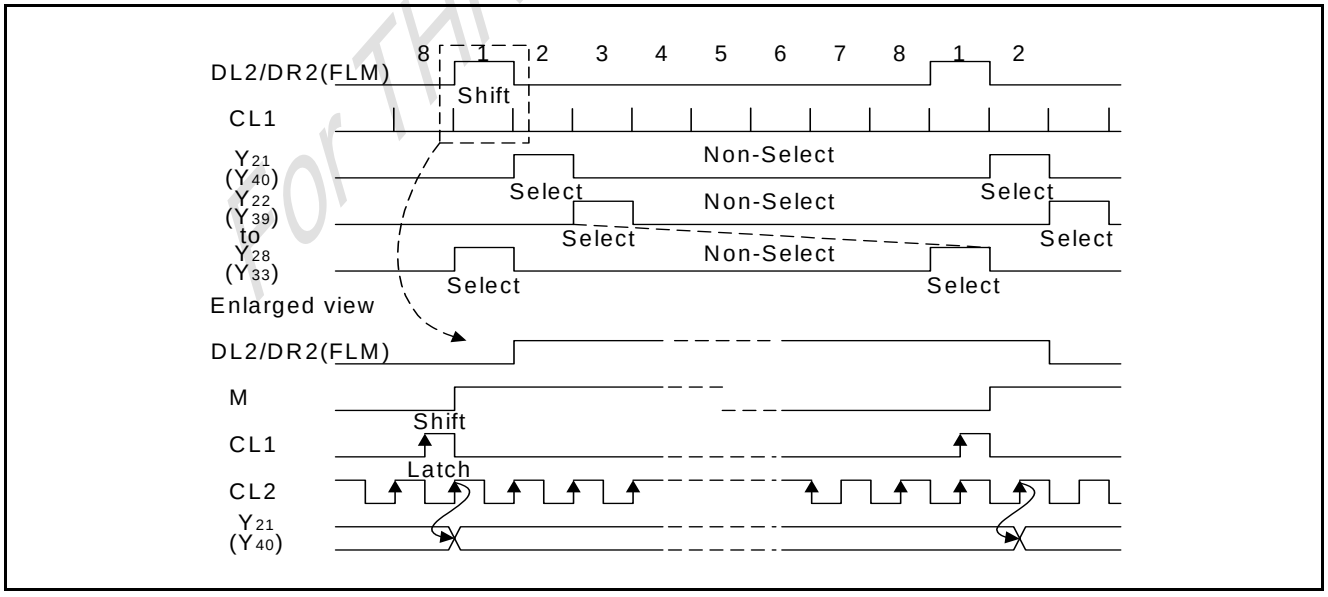
When SPLC100B1 is used as a segment driver, FCS is connected to VSS. In this case, both channel 1 and channel 2 shift data at the falling edge of CL2 and latch it at the falling edge of CL1. V3 and V5, V4 and V6 of the liquid crystal display driver power supply are short-circuited, respectively.



Segment data waveforms (A type waveforms, 1/8 duty cycle)

6.2. Common Driver

In this case, channel 1 is used as a segment driver and channel 2 as common driver. When channel 2 of SPLC100B1 is used as common driver, FCS is connected to VDD. In this case, channel 2 shifts data at the rising edge of CL1 and latches it at the rising edge of CL2.



Common data waveforms (A type waveforms of channel 2, 1/8 duty cycle)

6.3. Both Channel 1 and Channel 2 Used as Common Drivers (FCS = VSS)

6.3.1. Common drivers (FCS = VSS)

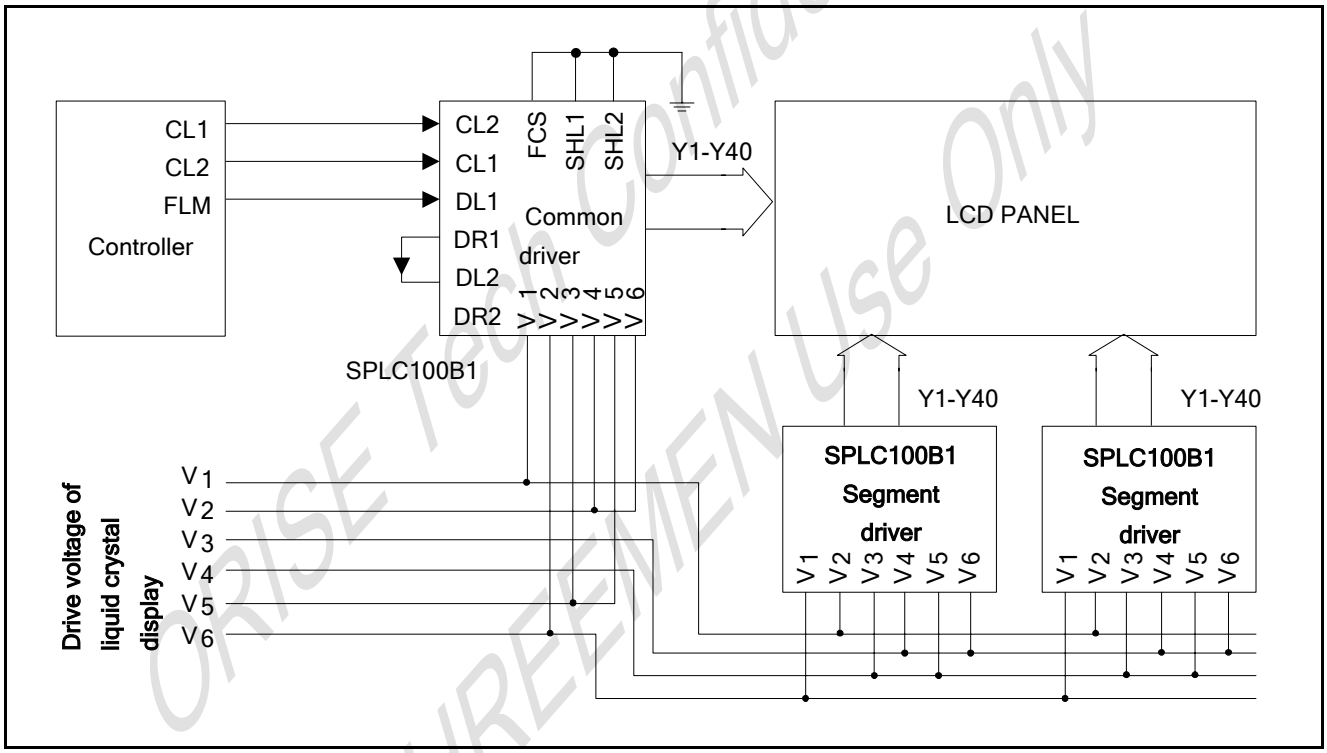
When both of channel 1 and channel 2 are used common drives, FCS is connected to VSS and the signals (CL1, CL2, FLM) from the controller are connected as following.

In this case, connection of the Liquid Crystal Display driver power supply is different from that of segment driver,

1). V1, V2: Select level of segment and common

2). V3, V4: Non-select level of segment

3). V5, V6: Non-select level of common



7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD *1	-0.3V to + 7.0V
LCD Driver Supply Voltage	VEE *2	VDD – 10.0V to VDD+ 0.3V
Input Voltage 1	V_{IN1}	-0.3V to VDD + 0.3V
Input Voltage 2 (V1 - V6)	V_{IN2}	VDD + 0.3V to VEE -0.3V
Operating Temperature	T_{OPR}	-20℃ to + 75℃
Storage Temperature	T_{STG}	-55℃ to + 125℃

Note1: It will cause damage to IC if the supply voltage is greater than above.
Note2: Connect a protection resistor of 220Ω±5% to VEE.
Note3: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

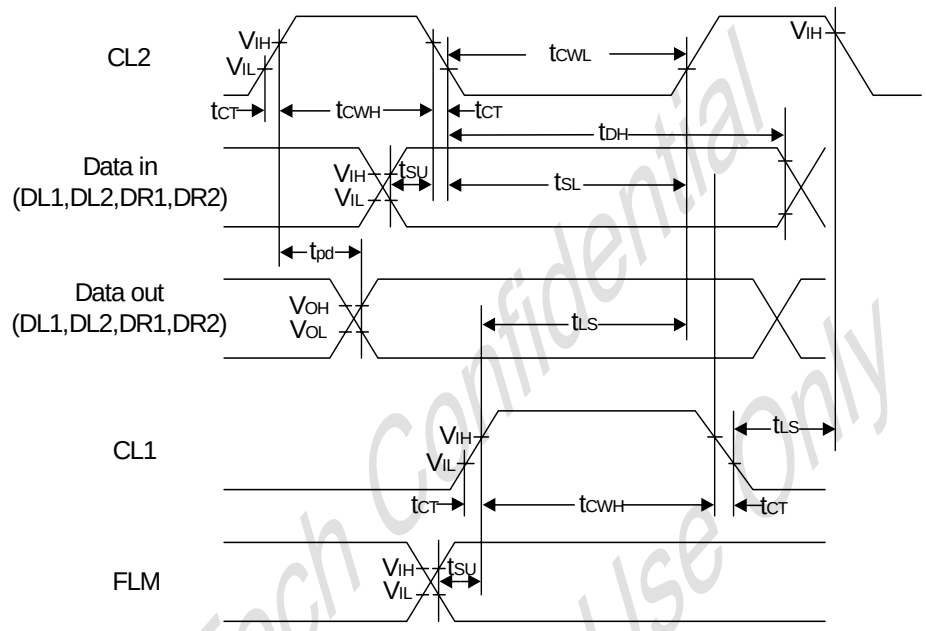
7.2. DC Characteristics

(VDD = 2.7V - 5.5V, VDD - VEE = 3.0V –8.0V , VSS = 0V, T_A = +25℃)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Voltage	V_{IH}	0.7VDD	-	VDD	V	
(CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS)	V_{IL}	0	-	0.3VDD	V	
Output Voltage	V_{OH}	VDD-0.4	-	-	V	I_{OH} = -0.1mA
(DL1, DL2, DR1, DR2)	V_{OL}	-	-	0.4	V	I_{OL} = +0.1mA
LCD Driver Voltage	V_{LCD}	3.0	-	11	V	VDD - V5
Vi-Yj Voltage Descending	V_{D1}	-	-	1.1	V	I_{ON} = 0.1mA for one of Yj
V(V1 - V6)-Y(Y1 - Y40)	V_{D2}	-	-	1.5	V	I_{ON} = 0.05mA for each Yj
Input Leakage Current (CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS)	I_{IL}	-5.0	-	5.0	μA	V_{IN} = 0 to VDD
Vi Leakage Current V1 - V6	I_{VL}	-10	-	10	μA	V_{IN} = VDD - VEE (Output Y1 - Y40: floating)
Power Supply Current	I_{CC}	-	-	1.0	mA	F_{CL2} = 400KHz
	I_{EE}	-	-	10	μA	F_{CL1} = 1.0KHz

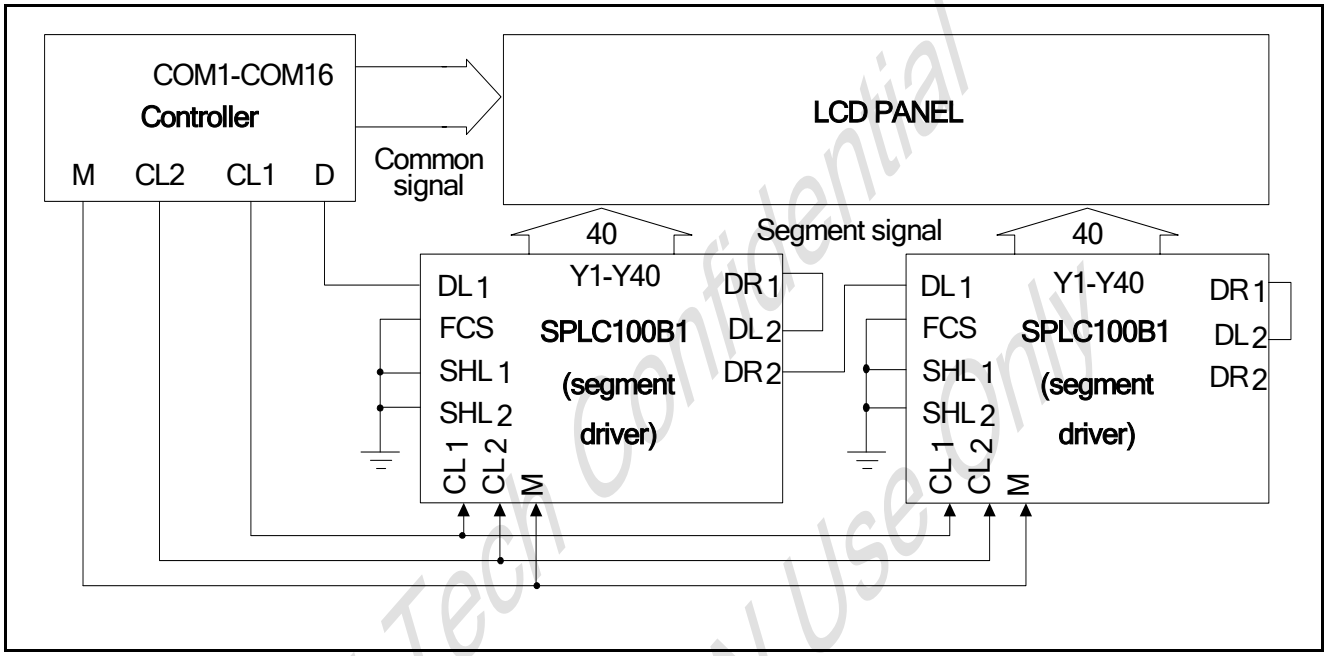
7.3. AC Characteristics

Characteristics		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Data Shift Frequency (CL2)		F_{CL}	-	-	400	KHz	
Clock Width	High Level (CL1, CL2)	t_{CWH}	800	-	-	ns	
	Low Level (CL2)	t_{CWL}	800	-	-	ns	
Data Set-up Time (DL1, DL2, DR1, DR2, FLM)		t_{SU}	300	-	-	ns	
Clock Set-up Time (CL1, CL2)		t_{SL}	500	-	-	ns	(CL2→CL1)
Clock Set-up Time (CL1, CL2)		t_{LS}	500	-	-	ns	(CL1→CL2)
Date Delay Time (DL1, DL2, DR1, DR2)		t_{PD}	-	-	500	ns	CL = 15pF
Clock Rise/Fall Time (CL1, CL2)		t_{CT}	-	-	200	ns	
Date Hold Time (DL1, DL2, DR1, DR2, FLM)		t_{DH}	300	-	-	ns	

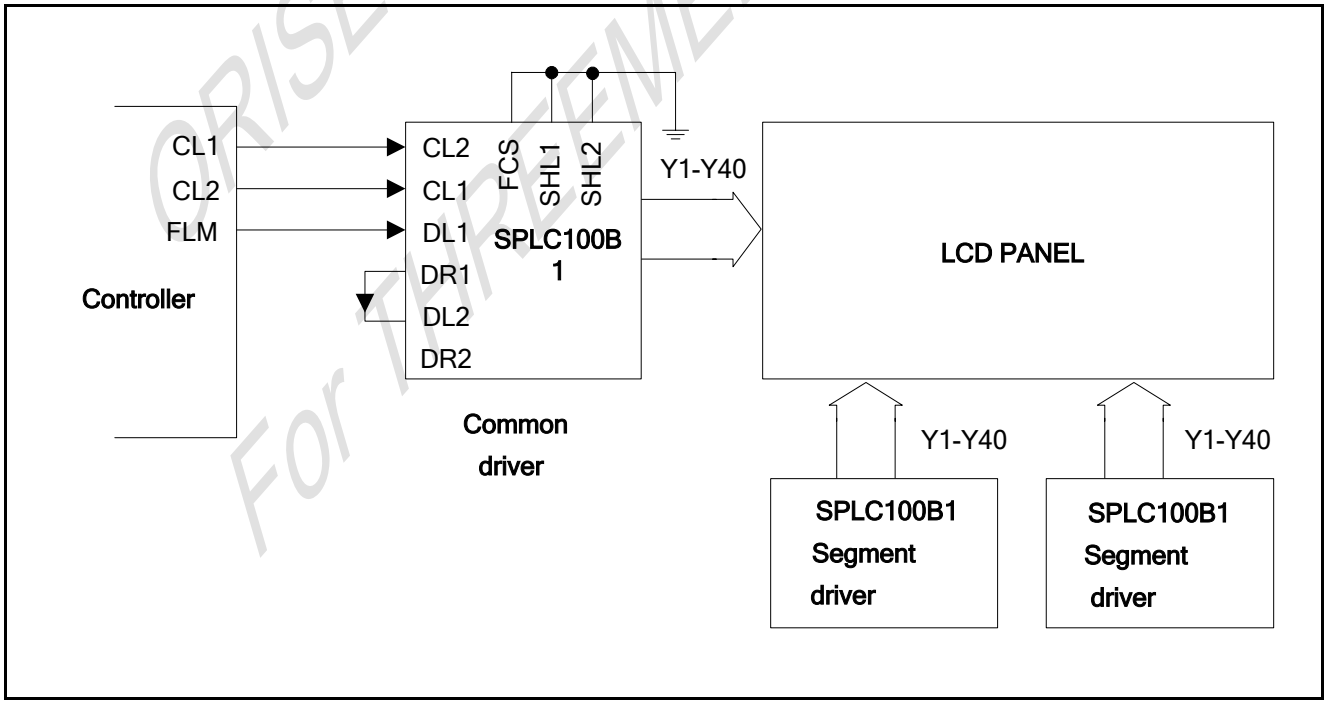


8. APPLICATION CIRCUITS

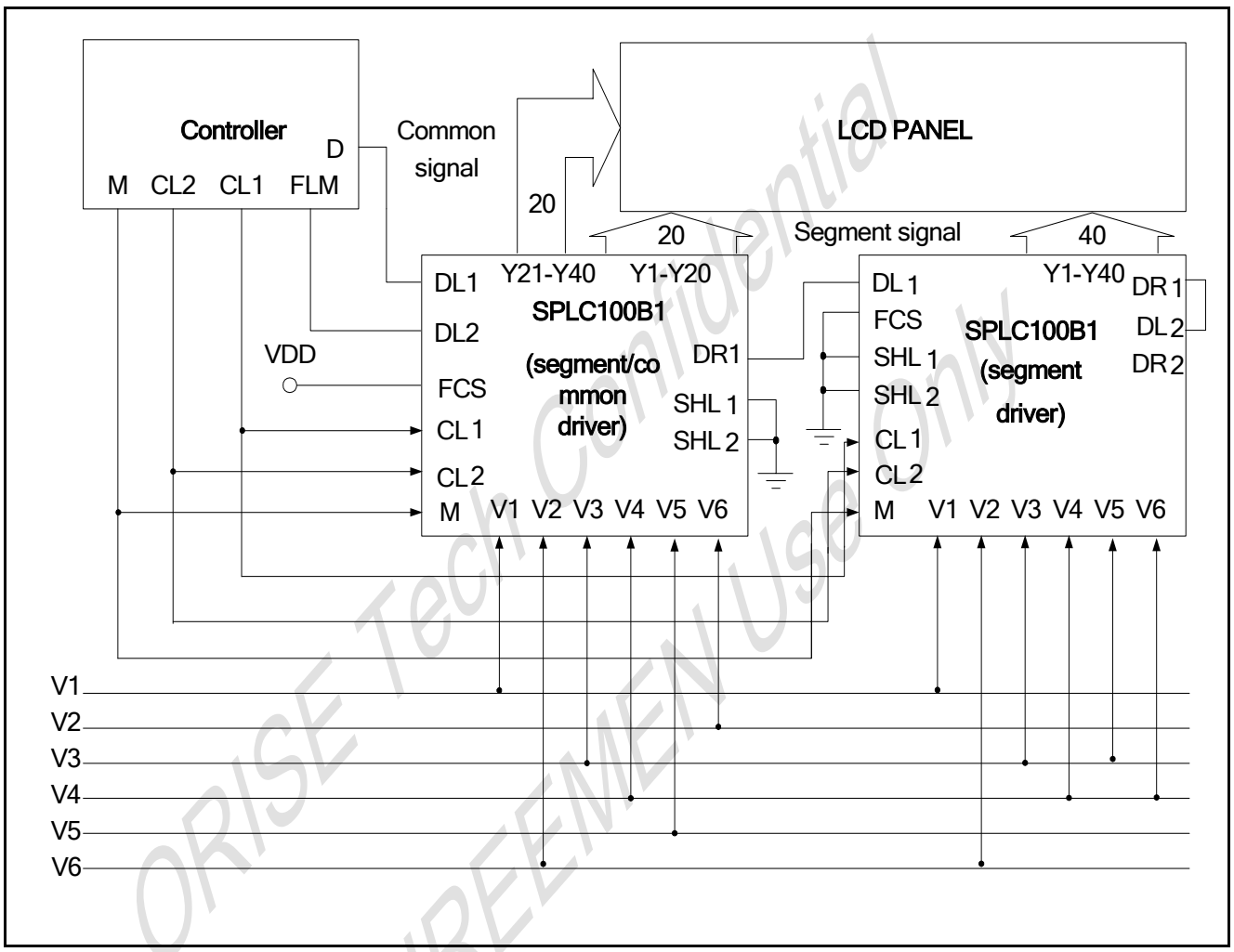
8.1. Segment Driver



8.2. Common Driver

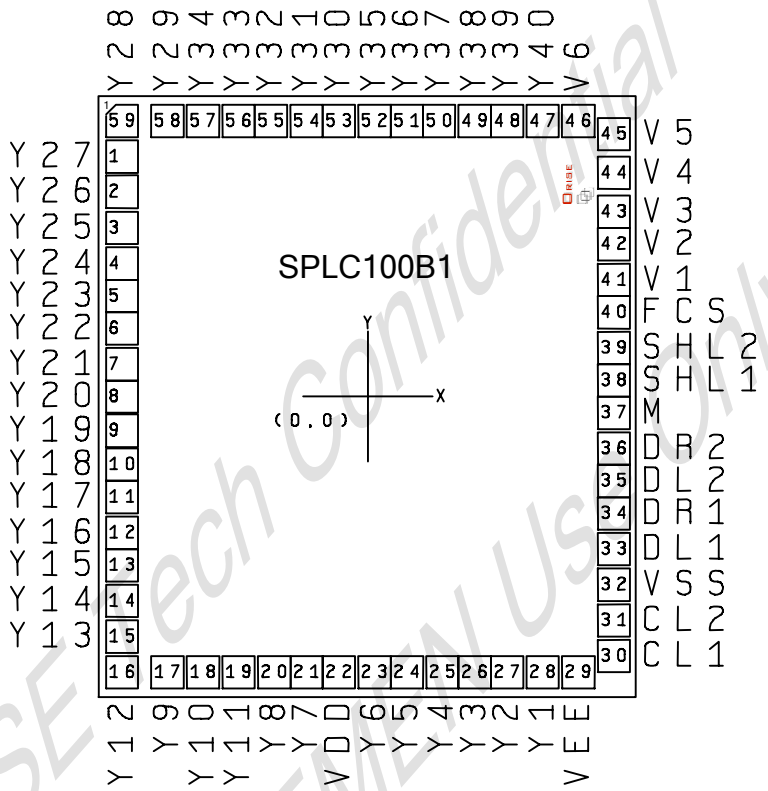


8.3. Segment / Common Driver



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 1816μm x 2026μm

PAD Size: 86μm X 86μm

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

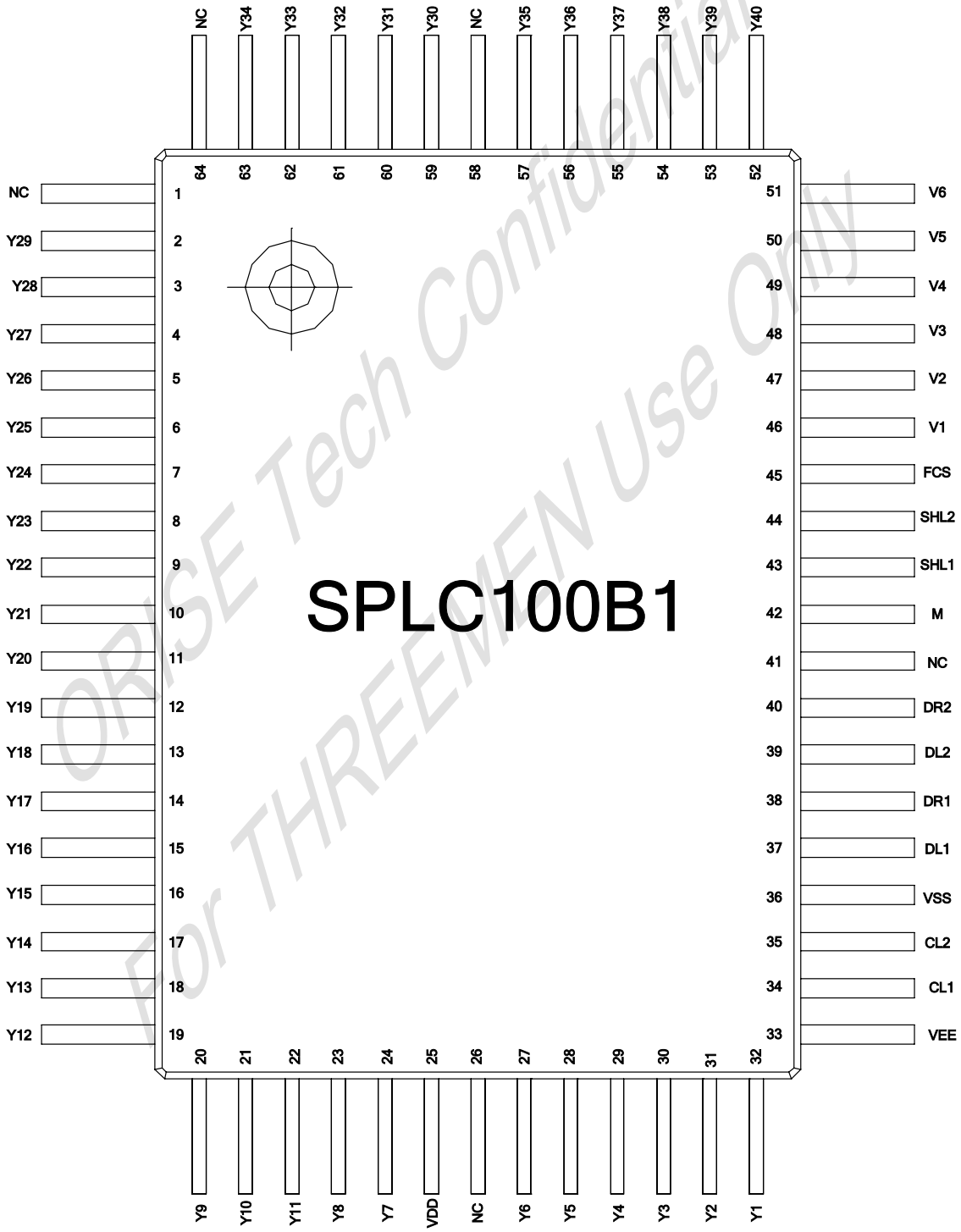
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	Pad Name	X	Y
1	Y27	-744	730	31	CL2	746	-620
2	Y26	-744	620	32	VSS	746	-510
3	Y25	-744	510	33	DL1	746	-405
4	Y24	-744	405	34	DR1	746	-300
5	Y23	-744	300	35	DL2	746	-200
6	Y22	-744	200	36	DR2	746	-100
7	Y21	-744	100	37	M	746	0
8	Y20	-744	0	38	SHL1	746	100
9	Y19	-744	-100	39	SHL2	746	200
10	Y18	-744	-200	40	FCS	746	300
11	Y17	-744	-300	41	V1	746	405
12	Y16	-744	-405	42	V2	746	510
13	Y15	-744	-510	43	V3	746	620
14	Y14	-744	-620	44	V4	746	730
15	Y13	-744	-730	45	V5	746	850
16	Y12	-744	-850	46	V6	626	850
17	Y9	-624	-850	47	Y40	516	850
18	Y10	-514	-850	48	Y39	406	850
19	Y11	-404	-850	49	Y38	301	850
20	Y8	-299	-850	50	Y37	201	850
21	Y7	-199	-850	51	Y36	101	850
22	VDD	-99	-850	52	Y35	1	850
23	Y6	1	-850	53	Y30	-99	850
24	Y5	101	-850	54	Y31	-199	850
25	Y4	201	-850	55	Y32	-299	850
26	Y3	306	-850	56	Y33	-404	850
27	Y2	416	-850	57	Y34	-514	850
28	Y1	526	-850	58	Y29	-624	850
29	VEE	646	-870	59	Y28	-744	850
30	CL1	746	-730				

9.3. PIN Assignment

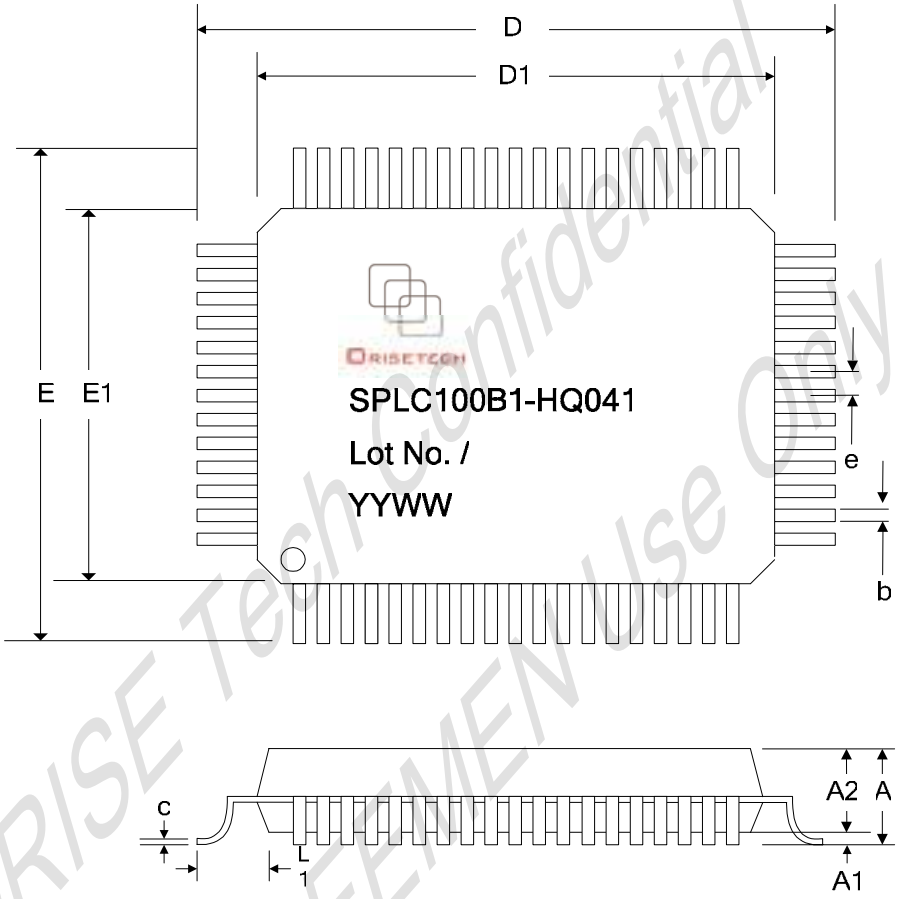
QFP 64L Top View



9.4. Package Information (QFP)

QFP 64L Outline Dimensions

Unit: Millimeter



Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		1.00 REF		Millimeter
b	0.35	0.40	0.50	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

10. LEAD FRAME PACKAGE PCB DESIGN AND MANUFACTURING GUIDELINES

10.1. Purpose

The purpose of this specification is to identify plastic surface mount devices (SMDs) those are sensitive to moisture-induced stress, so that they can be properly design PCB and assembly packaged, stored and handled to avoid subsequent mechanical damage during the assembly solder reflow attachment and /or repair operation.

10.2. Scope

10.2.1. PCB layout guideline

10.2.2. PCB process

10.2.3. Storage Condition and Period for Package

10.2.4. Recommended SMT Temperature Profile

10.3. Noun definition

10.3.1. NSMD: Non Solder Mask Defined

10.3.2. SMD: Solder Mask Defined

10.3.3. CSP: Chip scale Package

10.3.4. PCB :Printed Circuit Board

10.4. Responsibility unity:

ORISE Quality Assurance unity

10.5. Contents

10.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC-7525: Stencil Design Guidelines

J-STD-020: IPC/JEDEC Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Device

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-HDBK-001: Handbook & Guide to the Requirements of Soldered Electronic Assemblies with Amendment 1

IPC -6016: Qualification & Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-STD-003: Solderability Tests for Printed Boards

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

JESD22-B110: Subassembly Mechanical Shock

IPC-A-610: Acceptability of Electronic Assemblies

10.5.2. PCB layout guideline

PCB designer comply with IPC-SM-782 and IPC-7095 requirements is recommended

10.5.3. PCB process

10.5.3.1. Board material

The Glass transition temperature (Tg) of Board material greater than 170 degree C is recommended for Pb-free and Green package.

10.5.3.2. Surface Finishes

In order to achieve high assembly yields, use of a surface finish that is planar

And has good solderability performance is important. Below methods are all known to provide an acceptable land pad surface.

*OSP (Organic Solderability Preservative)

*Nihau (Electroplated nickel /gold)

*Immersion Ag

*Immersion Sn

10.5.3.3. Solder Paste: No clean flux is recommended.

10.5.3.4. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process

10.5.3.5. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package..

10.5.3.6. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green pack age.

10.5.3.7. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.

10.5.4. Storage condition and period for package

Orise technology evaluates all plastic surface mount devices (SMDs) to ICP/JEDEC J-STD-020A, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices, or refers to IPC JEDEC J-STD-033A Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

10.5.4.1. The primary facts for the package storage include oxidation, static, and therefore, the following rules are recommended to be applied for the storage.

10.5.4.2. The storage temperature should be 25℃ ± 5℃, and the humidity should be in the range of 50% ± 10% R.H. after opening the dry pack.

After the dry bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing.

10.5.4.3. Must be:

a. Mounted within 168 hours(Level 3) and 72 hours(Level 4) at factory conditions of ≦ 30℃/ 60% R.H. or

b. Stored at ≦ 20% R.H.

10.5.4.4. Devices require baking, before mounting, if:

a. Humidity Indicator Card shown warning message when read at 25℃±5℃, or

b. 10.5.4.3 is not met.

10.5.4.5. If baking is required. Devices may be baking for:

a. 192 hour at 40℃+5℃/-0℃ and <5% R.H. for low temperature device containers, or

b. 24 hours at 125±5℃ for high temperature device containers

10.5.4.6. The storage condition should be consistent with the operation condition to prevent dewing phenomena.

10.5.4.7. The storage location should be kept away from water and smoke; an isolated area with positive pressure control is preferred.

10.5.4.8. For a long-term storage, it is recommended to keep in a container with Nitrogen in it.

10.5.4.9. Avoid heavy objects stacked on the pack.

10.5.4.10. Avoid the static damage; use an anti-static bag for the package.

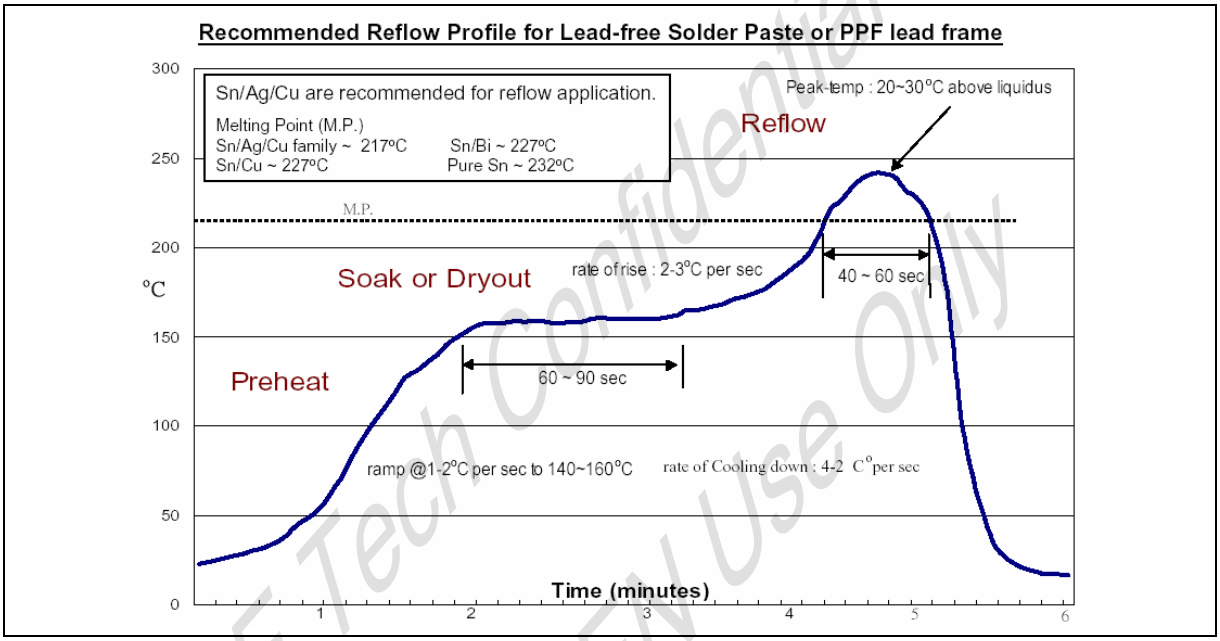
10.5.5. The classification of moisture sensitivity for Orise's product packages are shown in the following

(1) For Lead Free / Green Packages

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
QFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦ 30℃/ 60% R.H.	Yes

10.5.6. Recommended SMT Temperature Profile

This “Recommended” temperature profile is a rough guideline for SMT process reference. Most of ORISE leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



10.6. References

IPC:

http://www.ipc.org

*NEMI (National Electronics Manufacturing Initiative)

http://www.nemi.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

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12. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 21, 2007	0.1	Original	20