DATA SHEET

凌陽科技
SUNPLUS

SPLC086A

80ch Common/Segment Driver for Dot Matrix LCD

Preliminary

JAN. 11, 2002

Version 0.2

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80CH COMMON/SEGMENT DRIVER FOR DOT MATRIX LCD

1. GENERAL DESCRIPTION

The SPLC086A is an LCD driver LSI which is fabricated by low power CMOS high voltage process technology. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

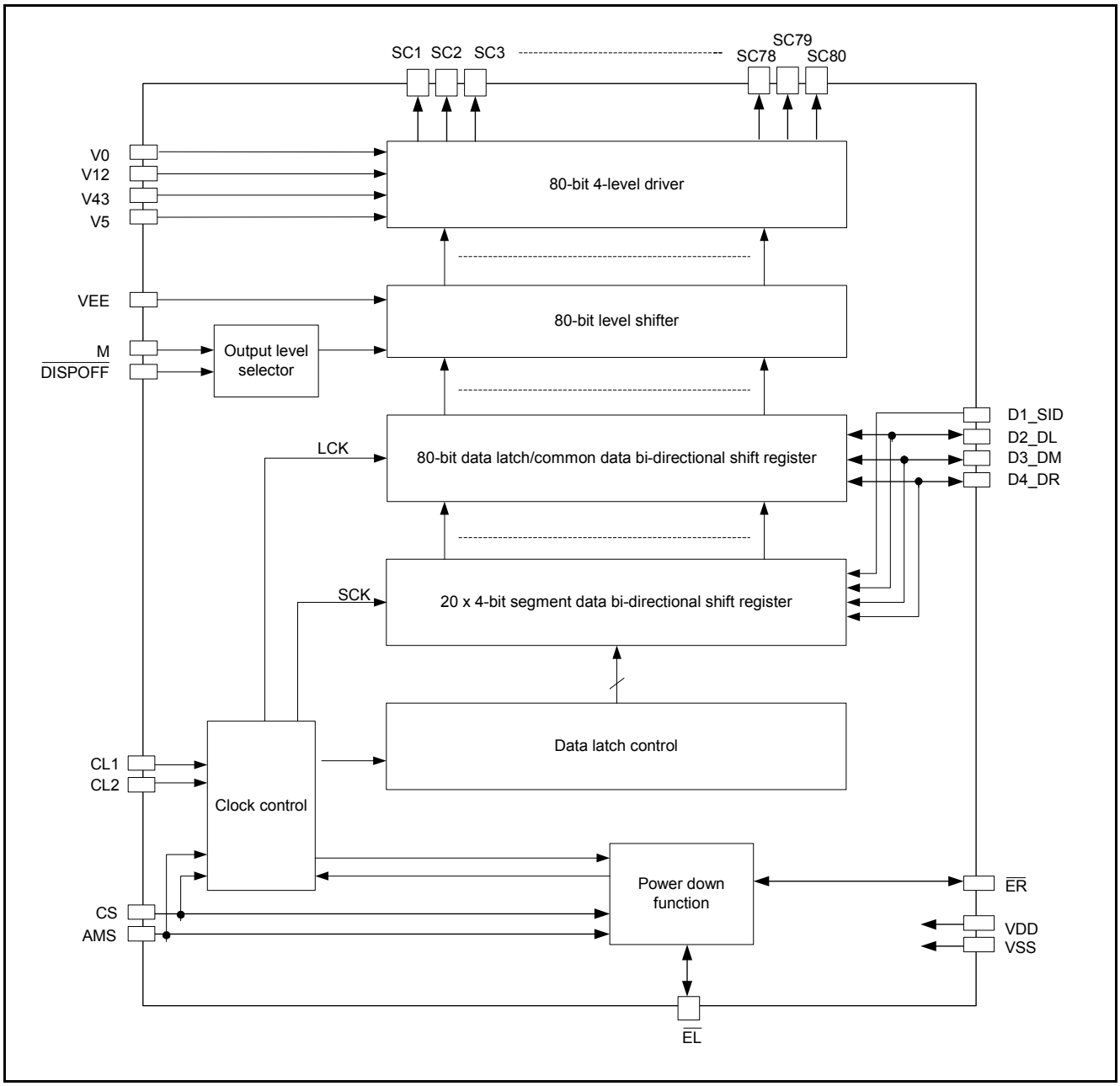
2. FEATURES

- Power supply voltage: +5.0V ± 10 %, +3.0V ± 10%
- Supply voltage for display: 6.0V to 28V (VDD-VEE)
- 4-bit parallel/1-bit serial data processing (in segment mode)
- Single mode operation/dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD Duty: 1/64 – 1/256
- Interface

Drivers	
COM (cascade)	**SEG (cascade)**
SPLC086A	SPLC086A

- High voltage CMOS process
- Available PKG type: bare die, 100 LQFP

3. BLOCK DIAGRAM



3.1. Block Descriptions

Name	Function	COM/SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin ($\overline{EL}$ or $\overline{ER}$). If enable input value is “Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and $\overline{DISPOFF}$) (refer to ***4. SIGNAL DESCRIPTIONS***).	COM/SEG
20x4-bit segment data bi-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch/ common data bi-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application, 1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to ***4.3 Data shift direction according to control signals***).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	COM/SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. And when in common driver application, this value becomes V1 or V4.	COM/SEG

4. SIGNAL DESCRIPTIONS

<table>
<tr><th>Mnemonic</th><th>Input/ Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3"></td><td rowspan="3"></td><td>Logical "High" input port (+5.0V ± 10%, +3.0V ± 10%)</td><td rowspan="3">Power</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>VEE</td><td>Logical "Low" for high voltage part</td></tr>
<tr><td>V0, V12
V43, V5</td><td>Input</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source (refer to <u>4.2 LCD Driving Voltage Application Circuit</u>).</td><td>Power</td></tr>
<tr><td>SC1 - SC80</td><td>Output</td><td>LCD driver output</td><td>Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to <u>4.1 Output level control</u>).</td><td>LCD</td></tr>
<tr><td>CL2</td><td>Input</td><td>Data shift clock</td><td>Clock pulse input for the bi-directional shift register.
1). In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift register at the falling edge of this clock pulse. The clock pulse, which was input when the enable bit ($\overline{EL}$ / $\overline{ER}$) is in not active condition, is invalid.
2). In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock. Hence, this clock pin is not used (Open or connect this pin to VDD).</td><td>Controller</td></tr>
<tr><td>M</td><td>Input</td><td>AC signal for LCD driver output</td><td>Alternate signal input pin for LCD driving.
Normal frame inversion signal is input in to this pin.</td><td>Controller</td></tr>
<tr><td>CL1</td><td>Input</td><td>Data latch clock</td><td>1). In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block.
2). In common driver application mode, CL1 is used as a shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>$\overline{DISPOFF}$</td><td>Input</td><td>Display off Control</td><td>Control input pin to fix the driver output (SC1 - SC80) to V0 level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS</td><td>Input</td><td>COM/SEG mode Control</td><td>When CS = "Low", SPLC086A is used as an 80-bit segment driver.
When CS = "High", SPLC086A is set to an 80-bit common driver.</td><td>VDD/VSS</td></tr>
<tr><td>AMS</td><td>Input</td><td>Application mode select</td><td>According to the input value of the AMS and the CS pin, application mode of SPLC086A differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM/SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode</td><td rowspan="2">SEG</td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode</td></tr>
<tr><td>1</td><td>0</td><td>Signal-type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>Dual-type application mode</td></tr>
</table></td><td>VDD/VSS</td></tr>
</table>

Mnemonic	Input/ Output	Name	Function	Interface
D1_SID D2_DL D3_DM D4_DR	I/O	Display data input/serial input data/left, right data input output	1). In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode: AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode: AMS = "High"). 2). In common driver application mode, the data is shifted from D2_DL (D4_DR) to D4_DR (D2_DL), when in single type interface mode (AMS = "Low"). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR (D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input (refer to ***4.3 Data Shift Direction According to Control Signals*** and ***4.4 Usage of Data PINs***)	Controller
SHL	Input	Shift direction control	When SHL = "Low", data is shifted from left to right. When SHL = "High", the direction is reversed. (refer to ***4.3 Data Shift Direction According to Control Signals***)	VDD/VSS
$\overline{EL}$ $\overline{ER}$	I/O	Enable data Input/output	1). In segment driver application mode, the internal operation is enabled only when enable input ($\overline{EL}$ or $\overline{ER}$) is "Low" (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below. 2). In common driver application mode, power down function is not used. Open these pins.	

SHL	Application mode	
	$\overline{EL}$	$\overline{ER}$
L	Output (open)	Input (VSS)
H	Input (VSS)	Output (open)

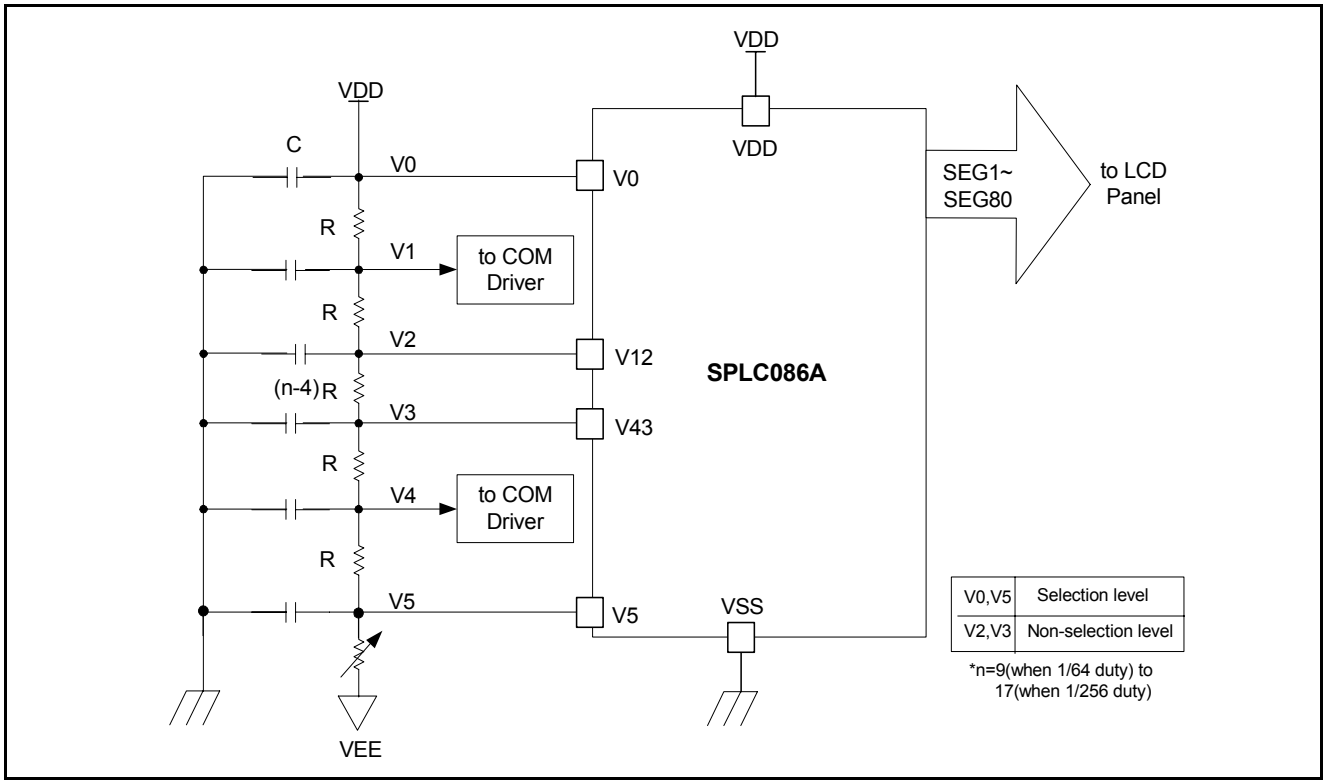
4.1. Output Level Control

M	Latched data	$\overline{DISPOFF}$	Output level (SC1 - SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V43 (V3)	V43 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

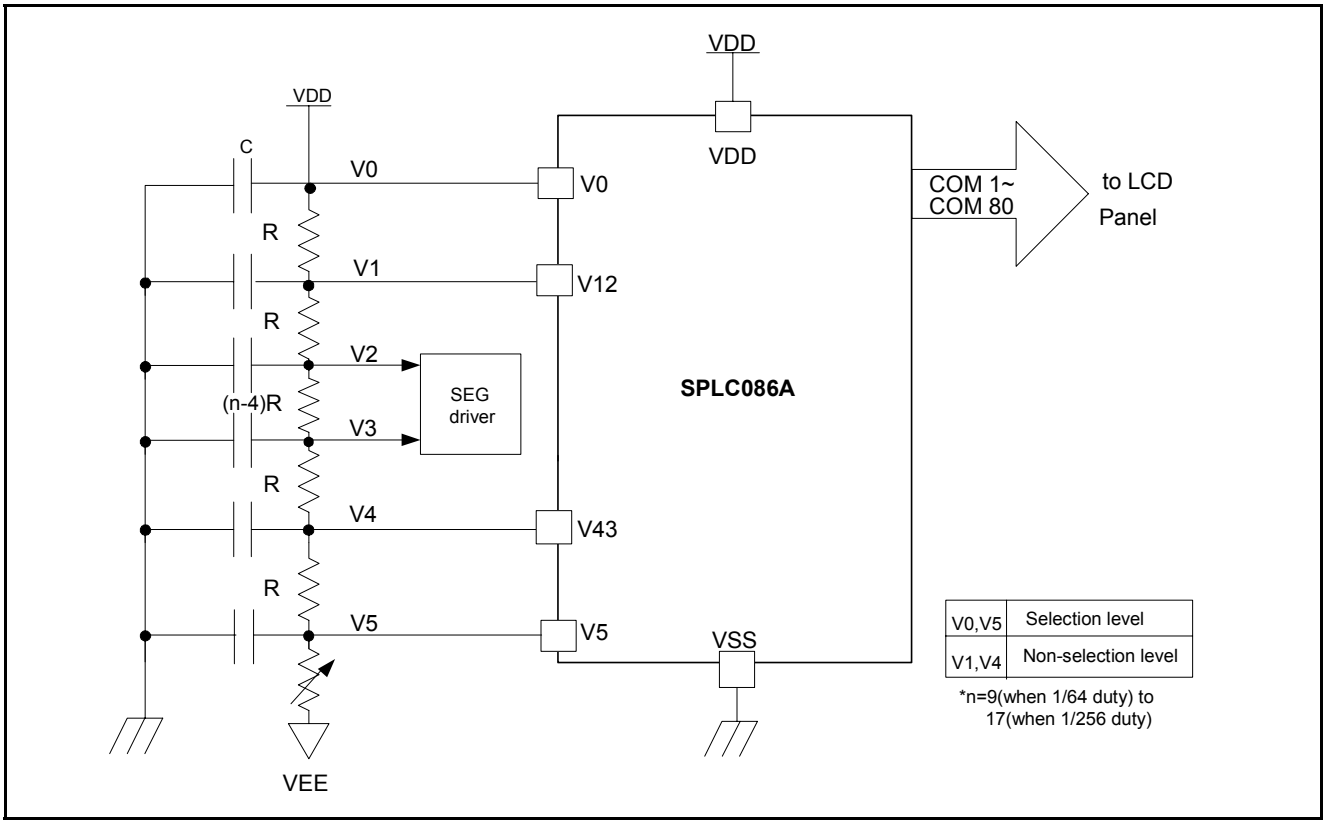
"X": don't care

4.2. LCD Driving Voltage Application Circuits

4.2.1. Segment driver application (CS = “Low”)

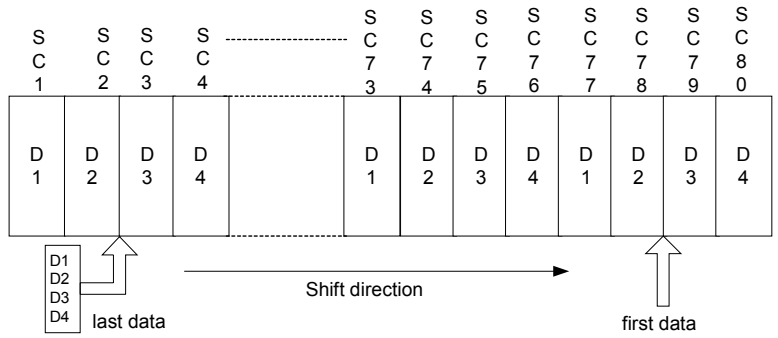
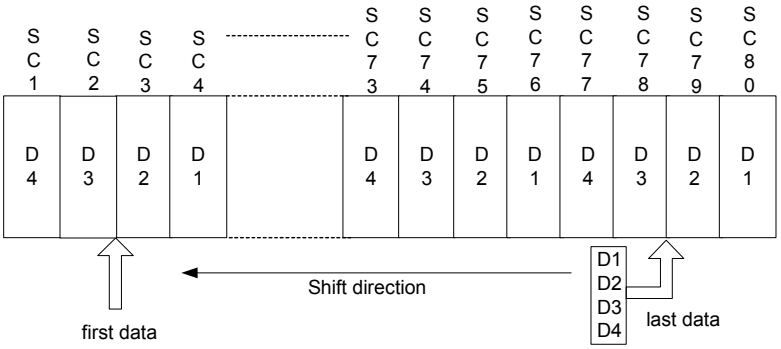
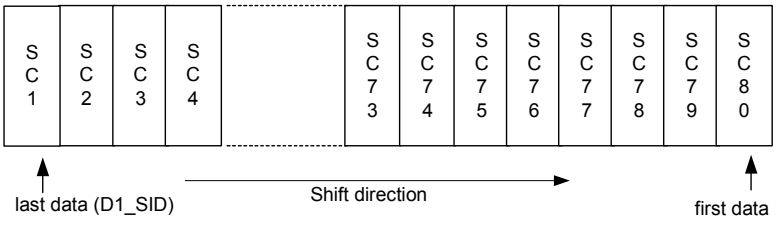
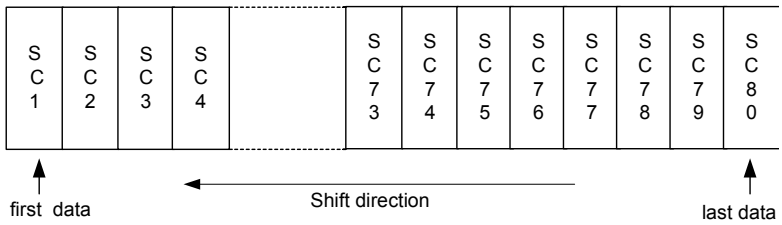


4.2.2. Common driver application (CS = “High”)

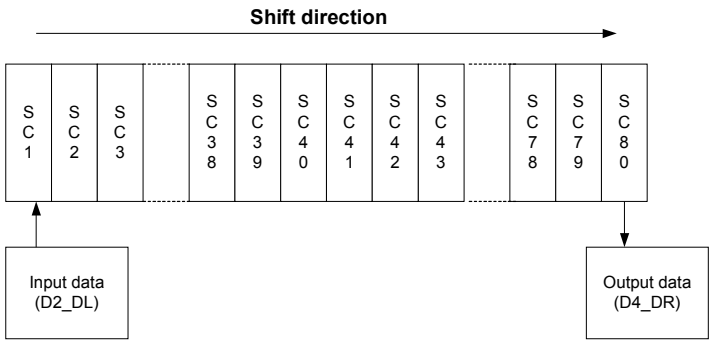
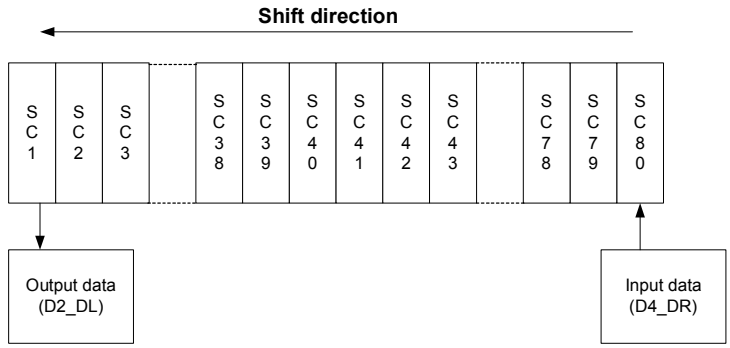
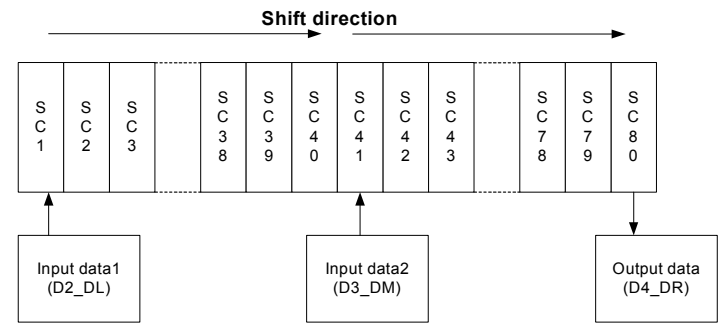
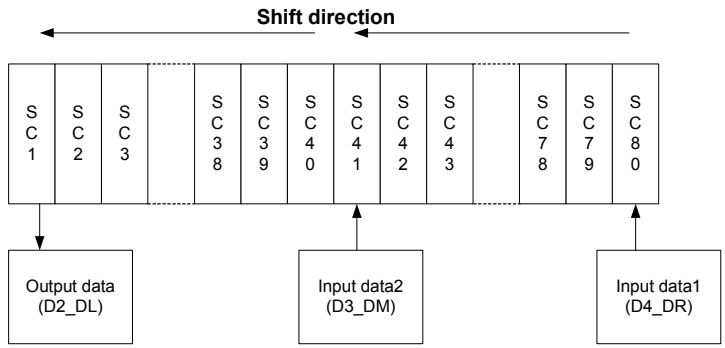


4.3. Data Shift Direction According to Control Signals

4.3.1. When CS = “Low” (segment driver application)

AMS	SHL	Application Mode	Data Direction	Input PIN
L	L	4-Bit Parallel Data Transfer Mode (SEG)		D1_SID, D2_DL, D3_DM, D4_DR,
	H			
H	L	1-Bit Serial Data Transfer Mode (SEG)		D1_SID
	H			

4.3.2. When CS = “High” (common driver application)

AMS	SHL	Application Mode	Data Direction	Input PIN
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL D3_DM
	H			D4_DR D3_DM

4.3.3. Usage of Data PINs

X = don't care

COM/SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS ="Low")	4-bit parallel interface mode (AMS = "Low")	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = "High")	X	SID (input)	Connect to VDD		
COM (CS = "High")	Single-type application mode (AMS = "Low")	L	Open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	Dual-type application mode (AMS = "High")	L	Open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

5. ELECTRICAL SPECIFICATIONS

5.1. Maximum Absolute Limit

Characteristic	Symbol	Value	Unit
Power supply voltage	VDD	-0.3 – +7.0	V
Driver supply voltage	V_{LCD}	0 – +30	
Input voltage	V_{IN}	-0.3 – VDD + 0.3	
Operating temperature	T_{OPR}	-30 – +85	°C
Storage temperature	T_{STG}	-55 – +150	

Note: Voltage greater than above may do damage to the circuit.

5.2. DC Characteristics

5.2.1. Segment driver application

(V_{SS} = 0V, T_A = - 30°C - +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating voltage1	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD - VEE		6.0	-	28	
Input voltage (1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = VDD to VSS		-10	-	10	μA
Input leakage current 2 (3)	I_{IL2}	V_{IN} = VDD to VEE		-25	-	25	
On resistance (4)	R_{ON}	I_{ON} = 100μA		-	2.0	4.0	KΩ
Supply current (5)	I_{STBY}	f_{CL1} = 32KHz M = VSS	VSS pin	-	-	100	μA
	I_{DD}	f_{CL1} = 32KHz f_M = 80Hz	VDD = 5.0V	-	-	5.0	mA
	I_{EE}		VDD = 3.0V	-	-	2.0	
			VDD = 5.0V	-	-	500	μA

Note1: Applied to CL1, CL2, $\overline{EL}$, $\overline{ER}$, D1_SID~D4_DR, SHL, $\overline{DISPOFF}$, M, CS, AMS pin

Note2: $\overline{EL}$, $\overline{ER}$ pin

Note3: V0, V12, V43, V5 pin

Note4: V_{LCD} = VDD - VEE, V0 = VDD = 5.0V, V5= VEE = -23V

V12 = VDD-2/n (V_{LCD}), V43 = VEE+2/n (V_{LCD}), n = 17 (1/256 duty, 1/17 bias)

Note5: V0 = VDD, V12 = 1.71V (VDD = 5.0V) or - 0.06V (VDD = 3.0V),

V43 = -19.71V (VDD = 5.0V) or -19.94V (VDD = 3.0V), V5 = VEE = -23V, no-load condition (1/256 duty, 1/17 bias) 4-bit parallel interface mode

I_{STBY}: VDD = 5.0V, f_{CL2} = 5.12MHz, SHL = VSS, $\overline{DISPOFF}$ = VDD, M = VSS, display data pattern = 0000

I_{DD} : VDD = 3.0V, f_{CL2} = 4.0MHz, display data pattern = 0101

VDD = 5V, f_{CL2} = 5.12MHz, display data pattern = 0101

I_{EE}: VDD = 5.0V, f_{CL2} = 5.12MHz, display data pattern = 0101, VEE pin

5.2.2. Common driver application

(VSS = 0V, T_A = - 30°C – +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating voltage	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD - VEE		6.0	-	28	
Input voltage (1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = VDD to VSS		-10	-	10	μA
Input leakage current 2 (2)	I_{IL2}	V_{IN} = 0V, VDD = 5.0V (PULL UP)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	V_{IN} = VDD to VEE		-25	-	25	
On resistance (5)	R_{ON}	I_{ON} = 100μA		-	2.0	4.0	KΩ
Supply current (6)	I_{STBY}	f_{CL1} = 32KHz	VSS pin	-	-	100	μA
	I_{DD}	f_{CL1} = 32KHz, f_M = 80Hz	VDD = 5.0V	-	-	200	
			VDD = 3.0V	-	-	120	
	I_{EE}		VDD = 5.0V	-	-	150	

Note1: Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, $\overline{DISPOFF}$, M, CS, AMS pin

Note2: Pull-up input pins: CL2, D1_SID, D3_DM (AMS = HIGH), $\overline{EL}$ (SHL = LOW), $\overline{ER}$ (SHL = HIGH)

Note3: D2_DL (SHL = HIGH), D4_DR (SHL = LOW) pin

Note4: V0, V12, V43, V5 pin

Note5: V_{LCD} = VDD-VEE, V0 = VDD = 5.0V, V5 = VEE = -23V
V12 = VDD-1/n(V_{LCD}), V43 = VEE+1/n(V_{LCD}), n = 17(1/256 duty, 1/17 bias)

Note6: V0 = VDD, V12 = 3.35V (VDD = 5.0V) or 1.47V (VDD = 3.0V),
V43 = -21.35V (VDD = 5.0V) or -21.47V (VDD = 3.0V), V5 = VEE = -23V, no-load condition (1/256 duty, 1/17 bias) single-type mode operation: AMS = VSS, SHL = VSS, $\overline{DISPOFF}$ = VDD
D1_SID = D3_DM = VDD, D4_DR = OPEN, $\overline{EL}$ = $\overline{ER}$ = OPEN,
I_{STBY}: VDD = 5.0V, M = VSS, D2_DL = VSS
I_{DD}: f_M = 80Hz, D2_DL = VDD
VDD = 3.0V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
VDD = 5.0V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
I_{EE}: f_M = 80Hz, D2_DL = VDD
VDD = 5.0V, current through VEE Pin, display data pattern = 10000000..., 01000000..., 00100000..., 00010000...

5.3. AC Characteristics

5.3.1. Segment driver application

(VSS = 0V, T_A = - 30°C – +85°C)

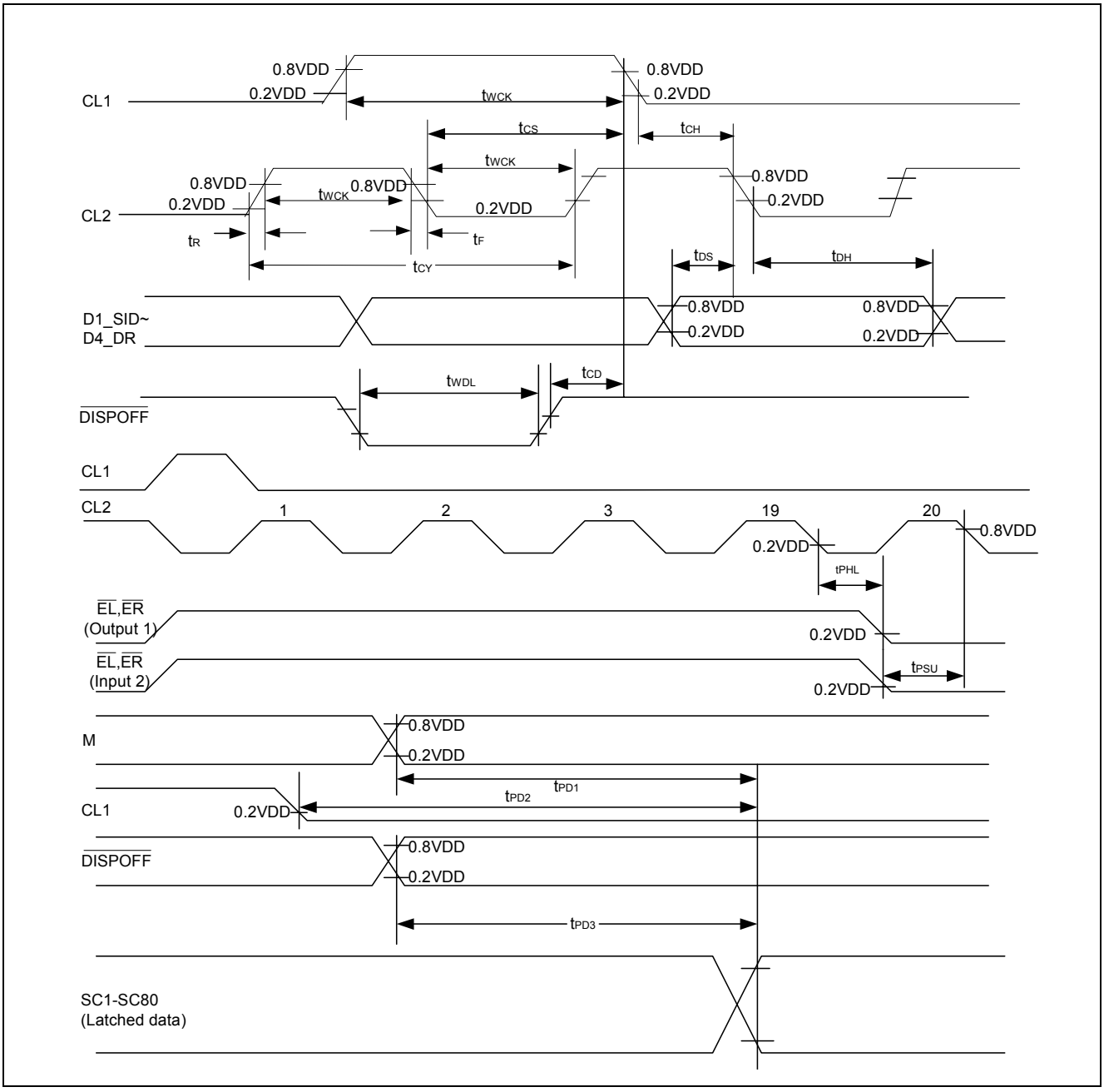
Characteristic	Symbol	Test Condition	(1) VDD = 5.0V ±10%			(2) VDD = 3.0V ±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	$\overline{EL}$ Output	-	-	60	-	-	125	
		$\overline{ER}$ Output			60			125	
$\overline{EL}$, $\overline{ER}$ set-up time	t_{PSU}	$\overline{EL}$ Input	30	-	-	65	-	-	
		$\overline{ER}$ Input	30			65			
$\overline{DISPOFF}$ low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
$\overline{DISPOFF}$ clear time	t_{CD}	-	100	-	-	100	-	-	ns
M – OUT propagation delay time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
$\overline{DISPOFF}$ - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-	

5.3.2. Common driver application

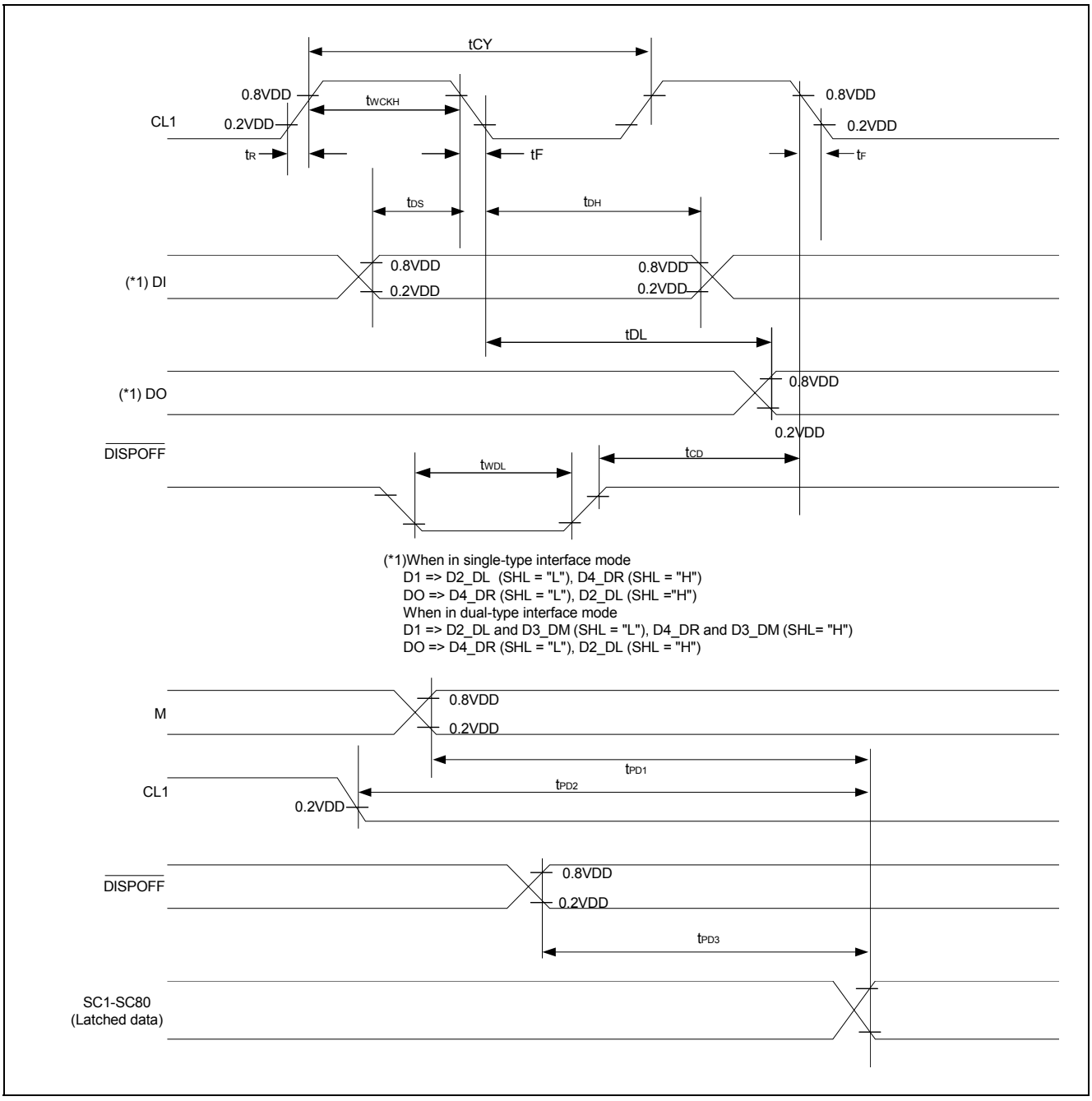
(VSS = 0V, T_A = - 30°C – +85°C)

Characteristic	Symbol	Test Condition	(1) VDD = 5.0V ±10%			(2) VDD = 3.0V ±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
$\overline{DISPOFF}$ low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
$\overline{DISPOFF}$ clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	C_L = 15pF	-	-	200	-	-	250	
M - OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
$\overline{DISPOFF}$ - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

5.3.3. Segment driver application timing



5.3.4. Common driver application timing

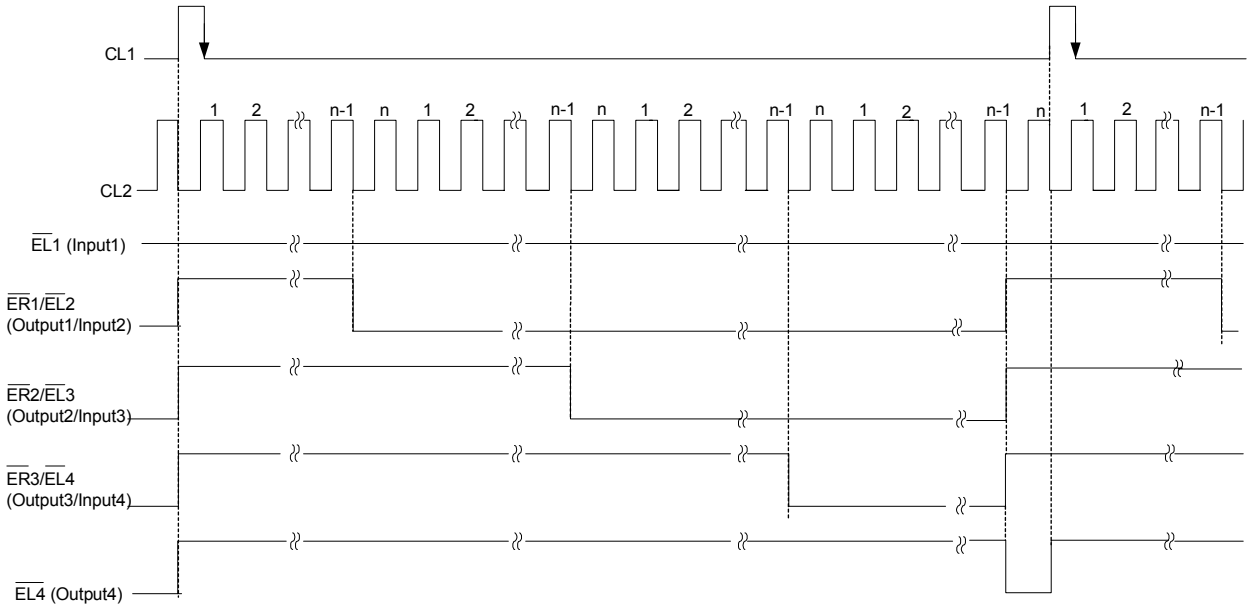


5.4. Power Down Function

In the case of cascade connection of segment mode drivers, power consumption. SPLC086A has a "power down function" in order to reduce the

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	$\overline{ER}$	$\overline{EL}$	While $\overline{ER}$ ="Low", current driver is enabled.	Disabled
H	$\overline{EL}$	$\overline{ER}$	While $\overline{EL}$ ="Low", current driver is enabled.	Disabled

Note: In the case of common driver application, power down function does not work.

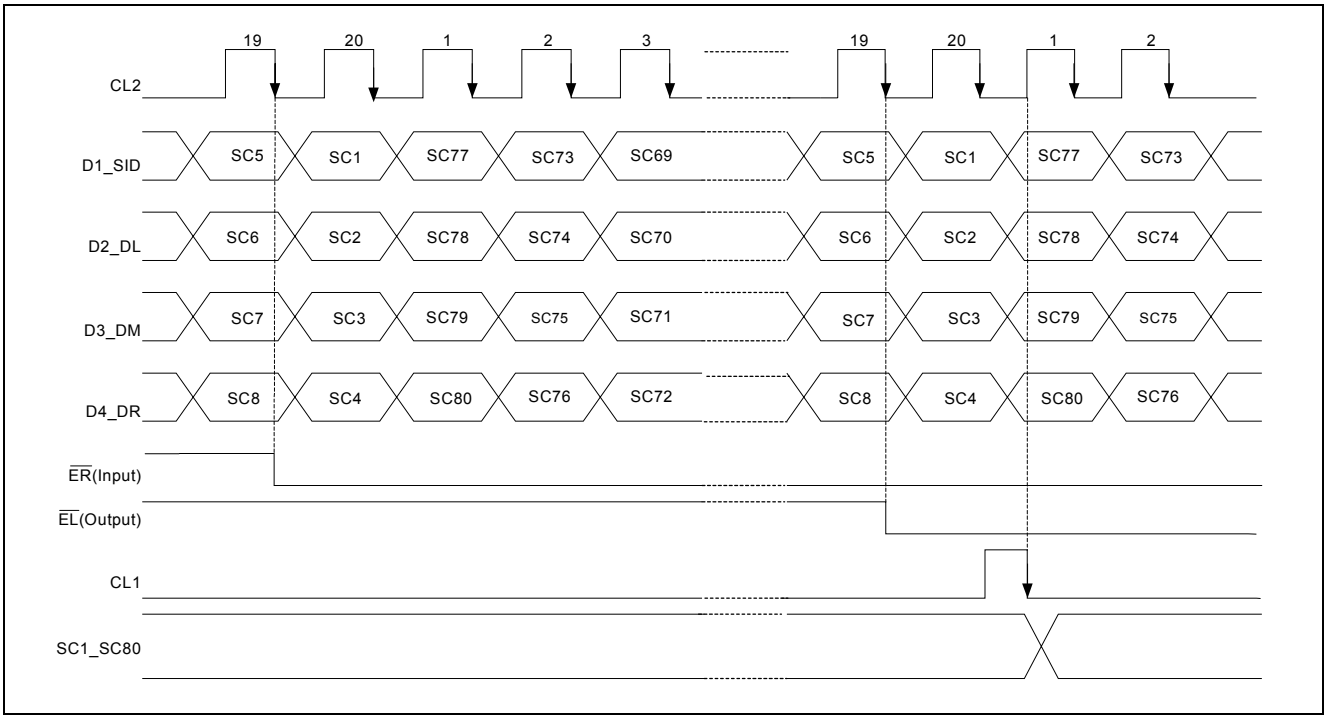


Note1: SHL = "High" ($\overline{EL}$ = Input, $\overline{ER}$ = Output)
Current SPLC086A's $\overline{ER}$ must be connected to the next SPLC086A's $\overline{EL}$.
Note2: When in 4-bit parallel interface mode: n = 20
When in 1-bit serial interface mode: n = 80

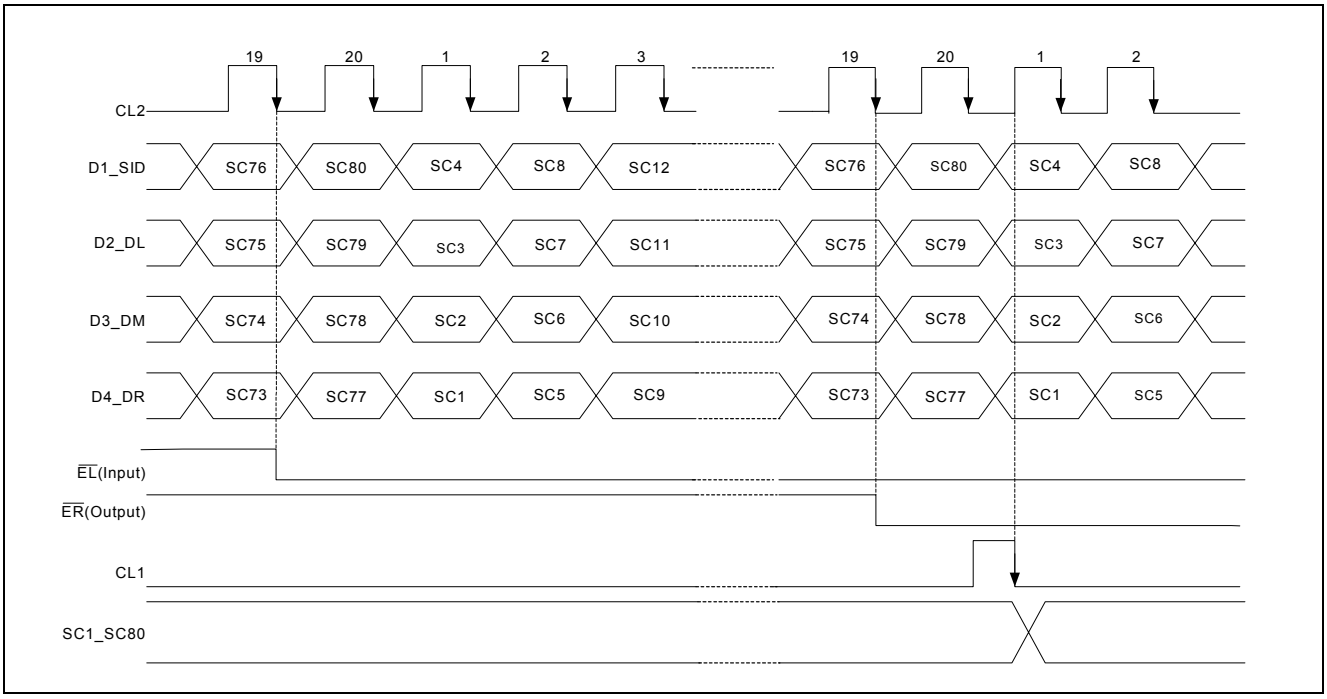
5.5. Operation Timing Diagram

5.5.1. 4-bit parallel mode interface segment driver

1.) When SHL = "Low"

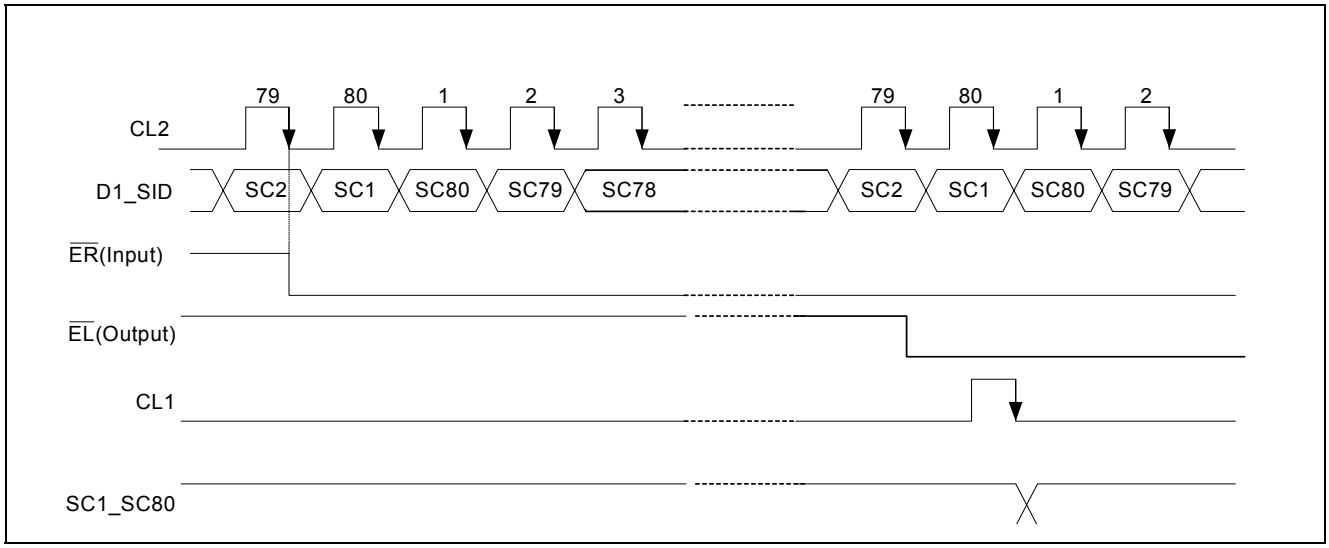


2.) When SHL = “High”

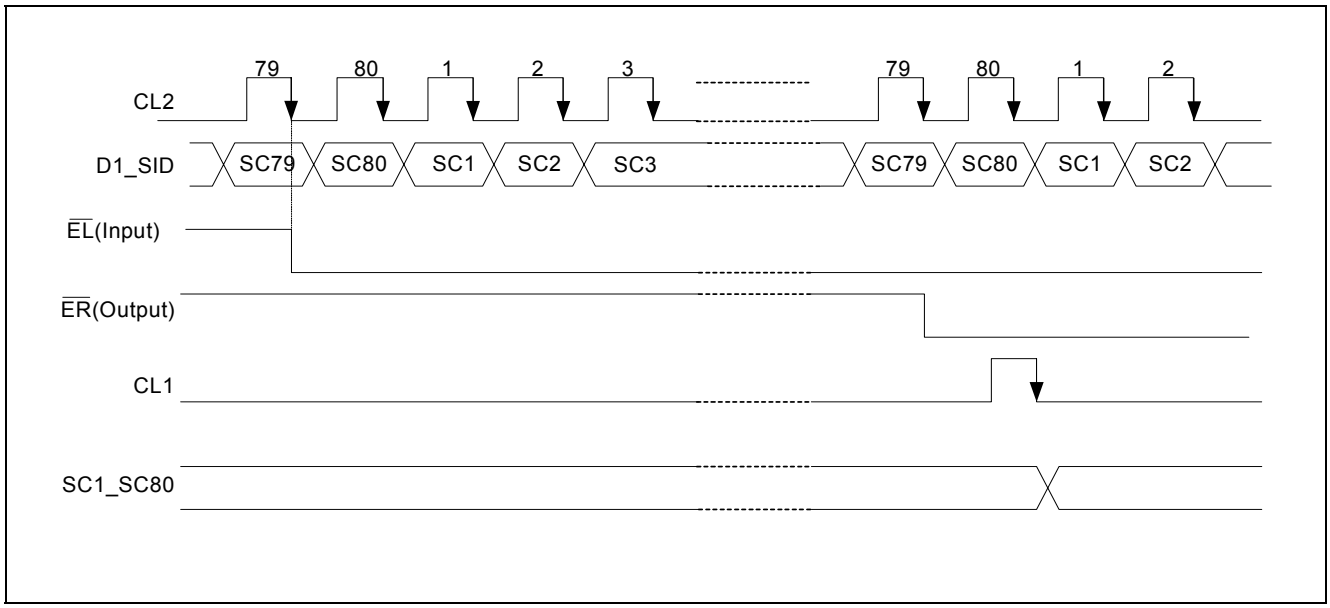


5.5.2. 1-bit serial mode interface segment driver

1.) When SHL = "Low"

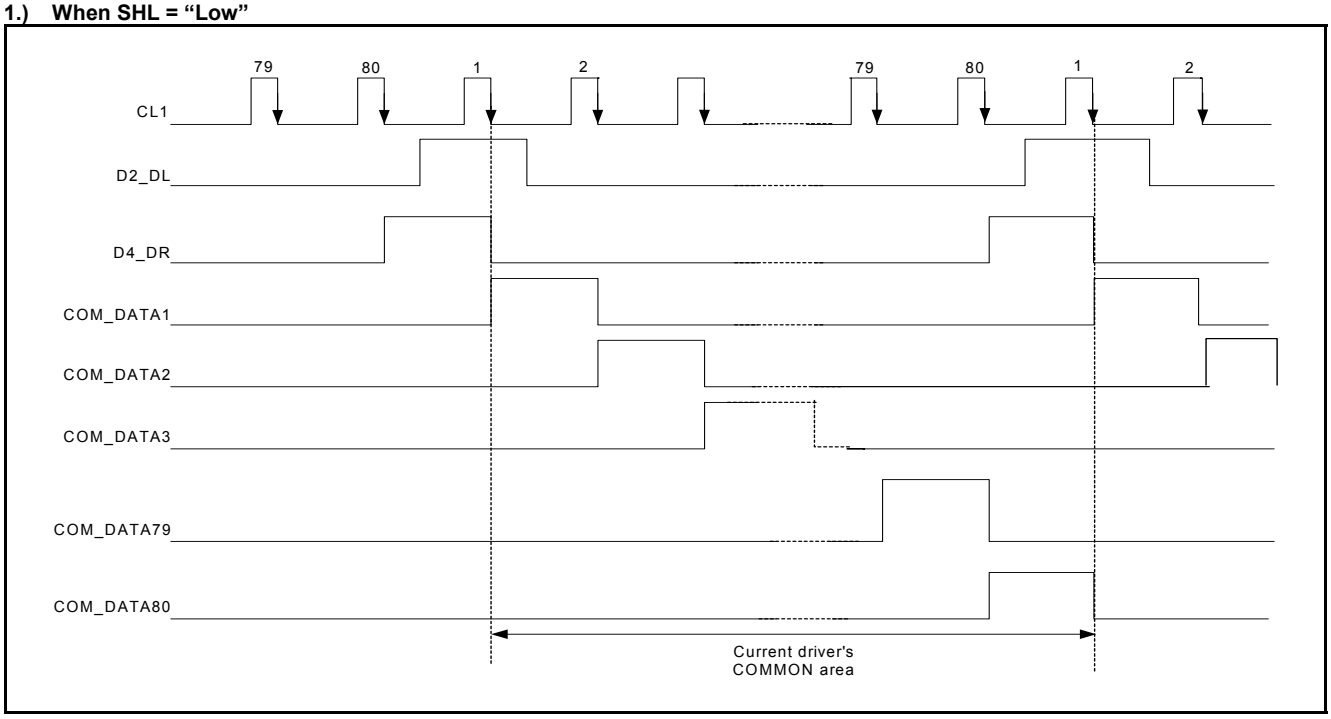


2.) When SHL = "High"

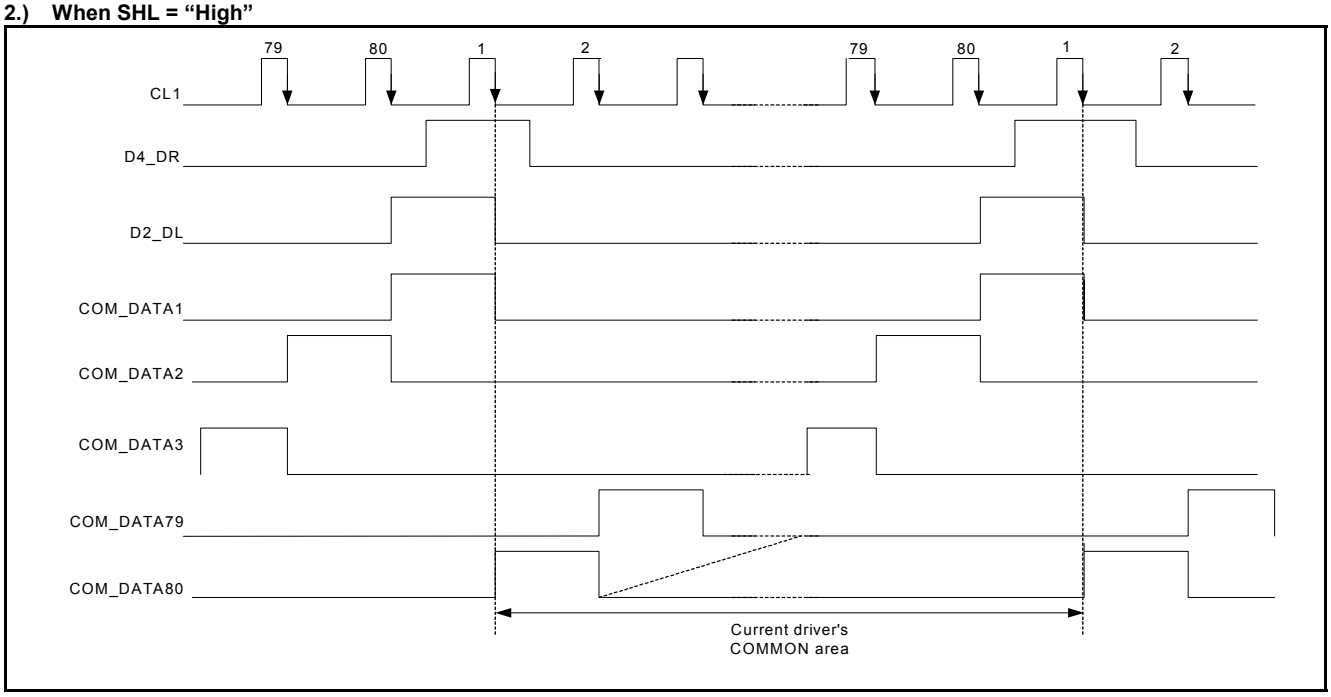


5.5.3. Single-type interface mode common driver

1.) When SHL = "Low"

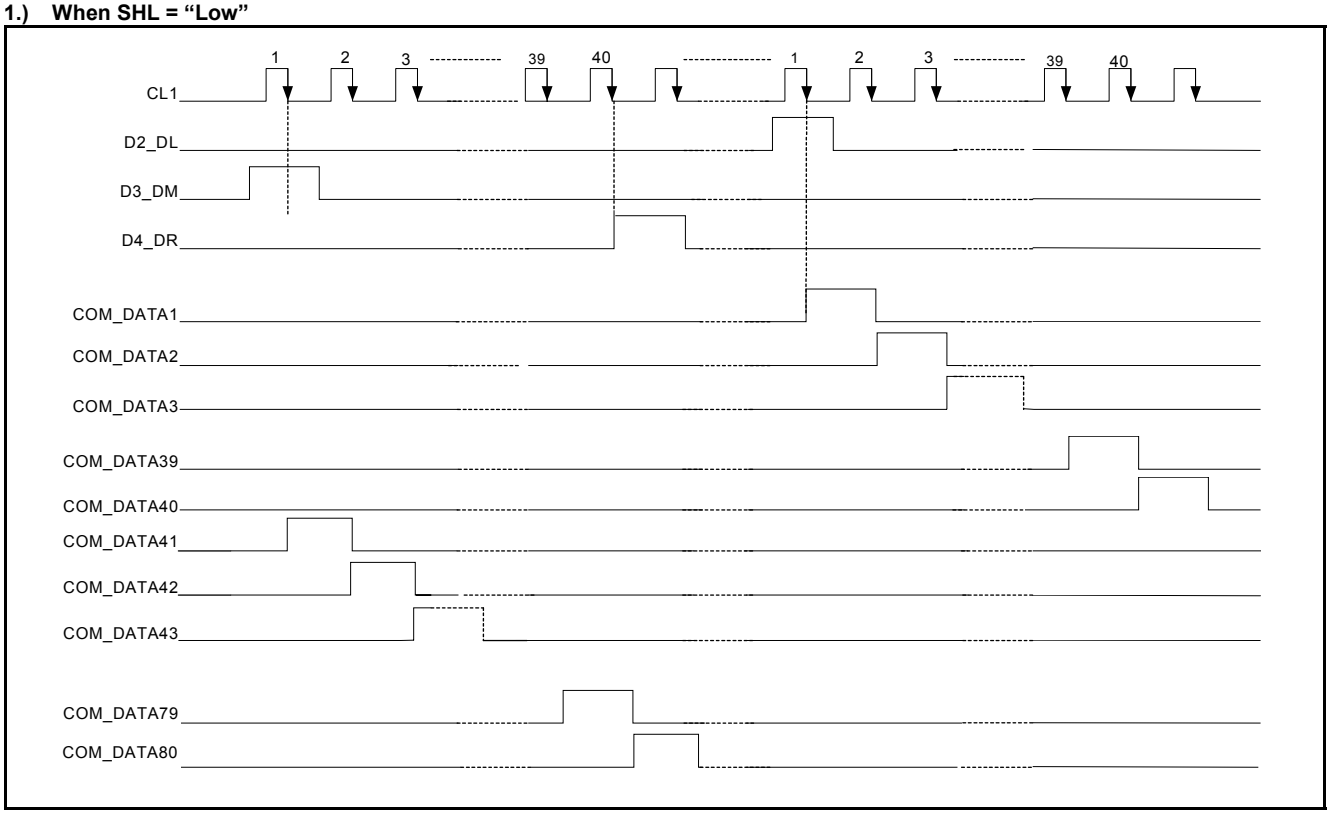


2.) When SHL = "High"

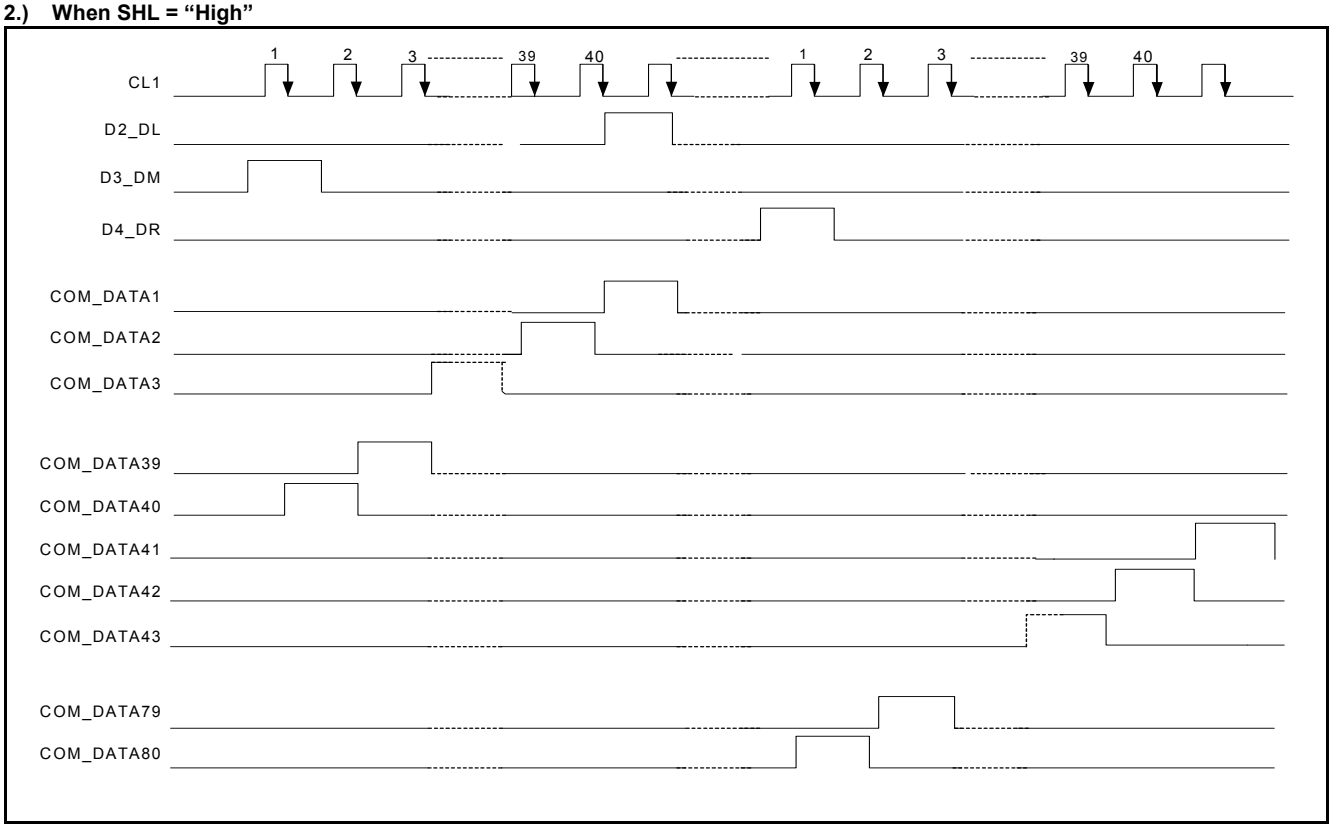


5.5.4. Dual-type interface mode common driver

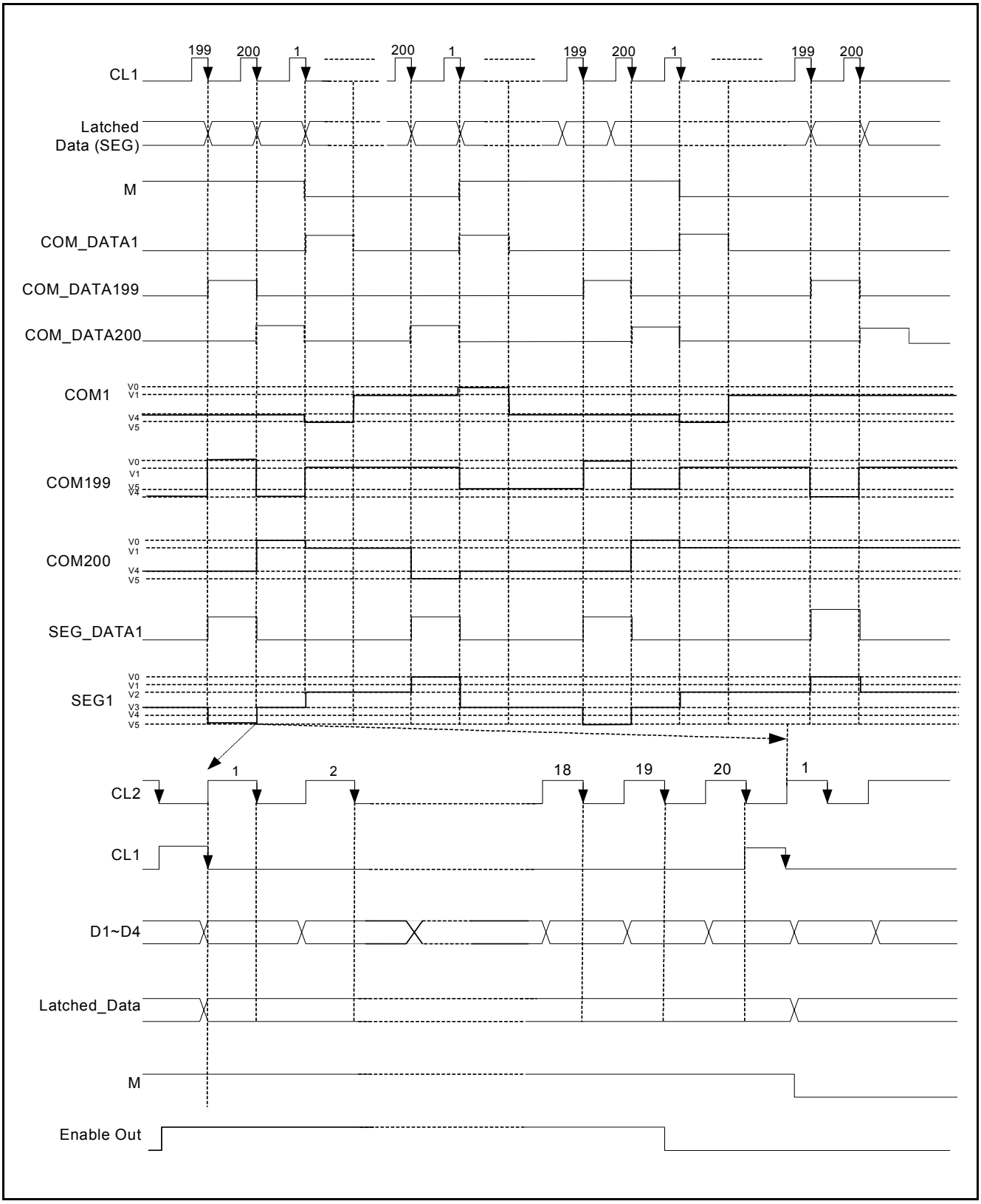
1.) When SHL = "Low"



2.) When SHL = "High"



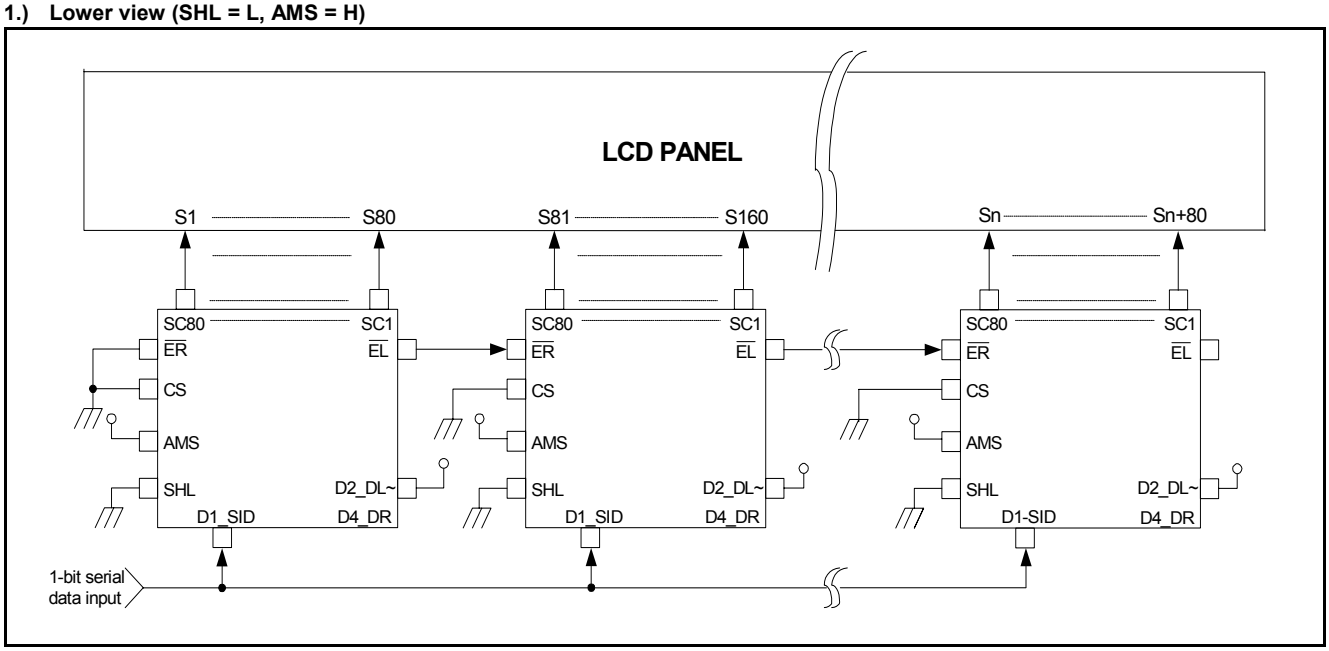
5.5.5. Common/segment driver timing (1/200 duty)



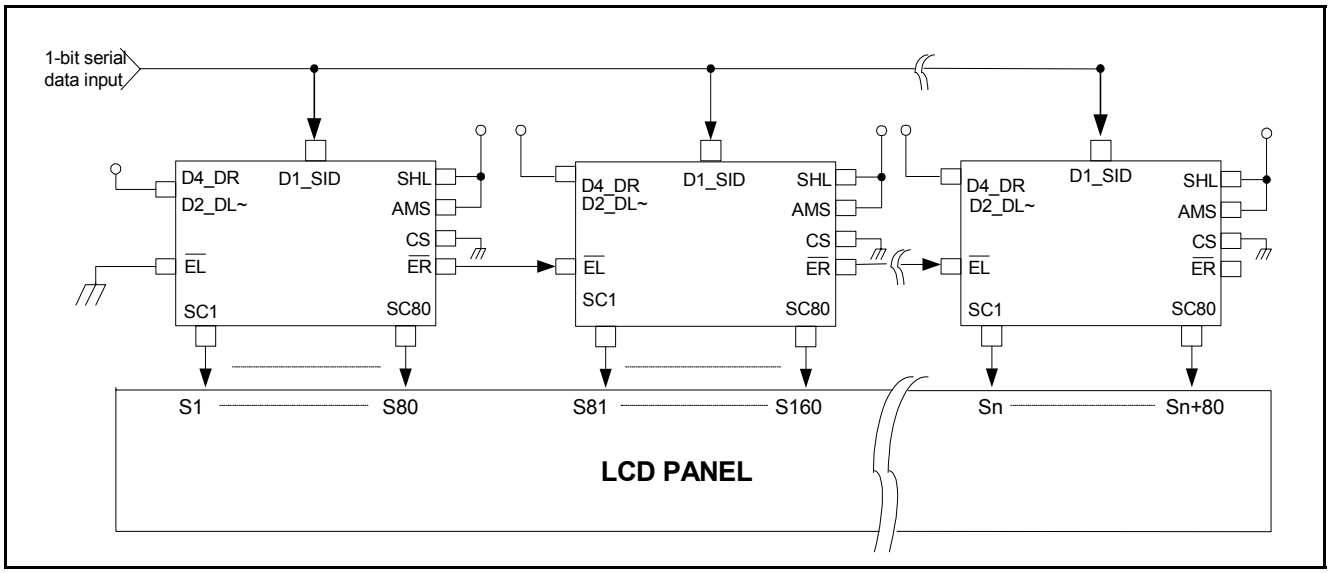
6. APPLICATION CIRCUITS

6.1. 1-Bit Serial Interface Mode (80-ch Segment Driver)

1.) Lower view (SHL = L, AMS = H)

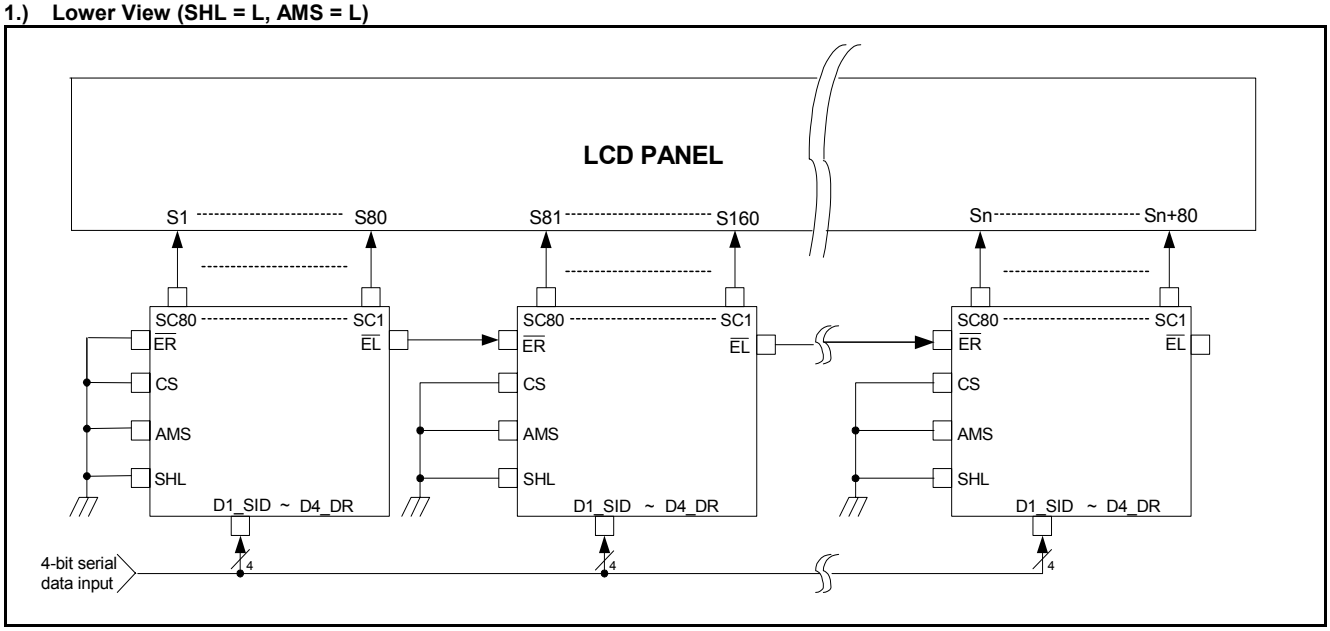


2.) Upper view (SHL = H, AMS = H)

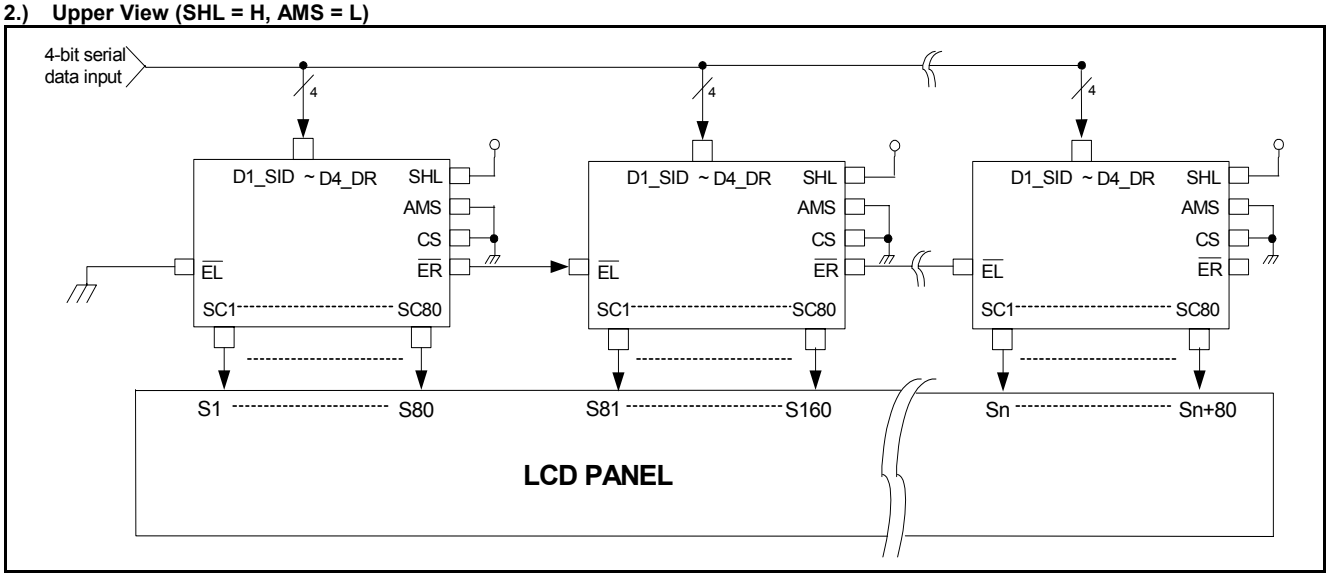


6.2. 4-Bit Parallel Interface Mode (80-ch Segment Driver)

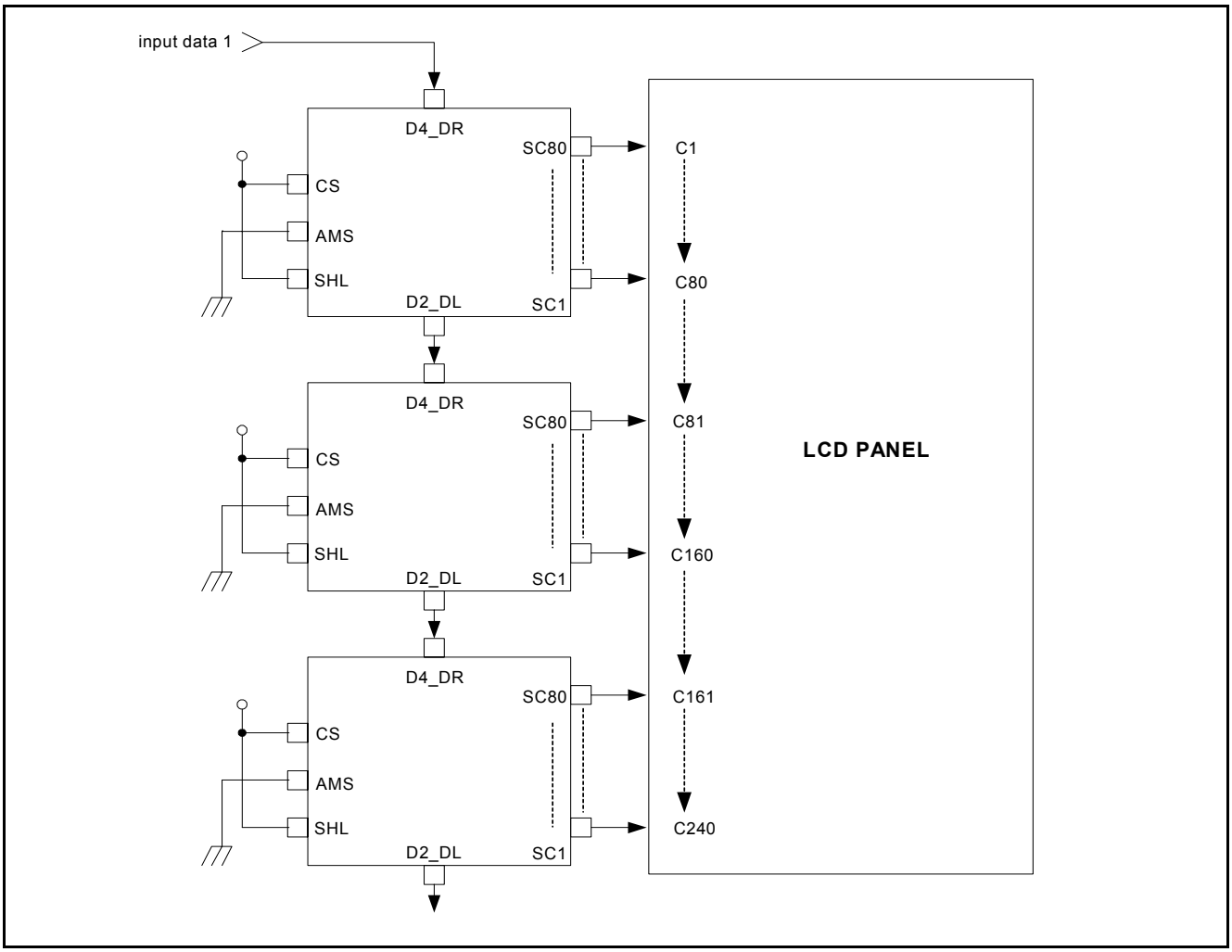
1.) Lower View (SHL = L, AMS = L)



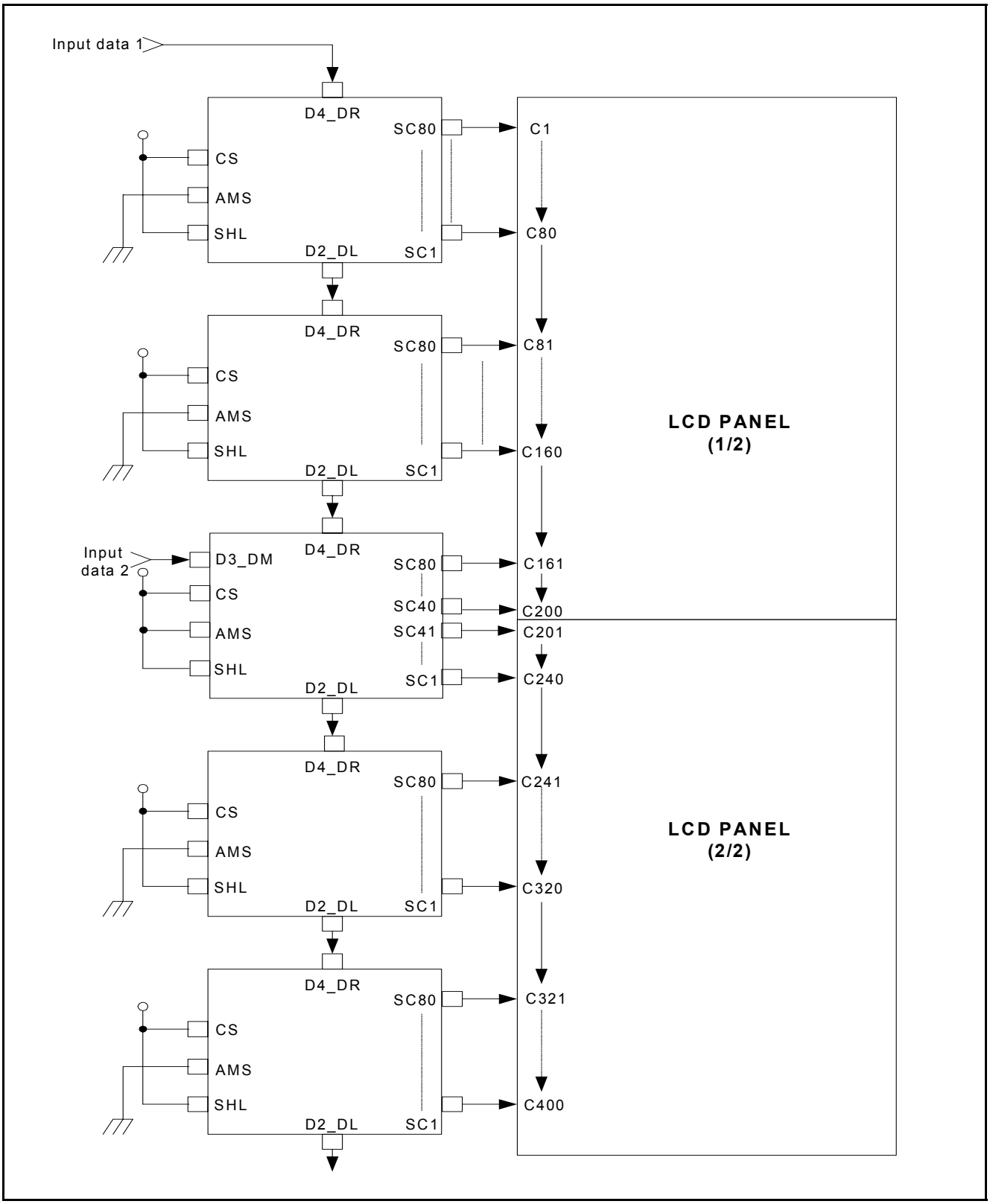
2.) Upper View (SHL = H, AMS = L)



6.3. Single-Type Interface Mode (80-ch Common Driver)

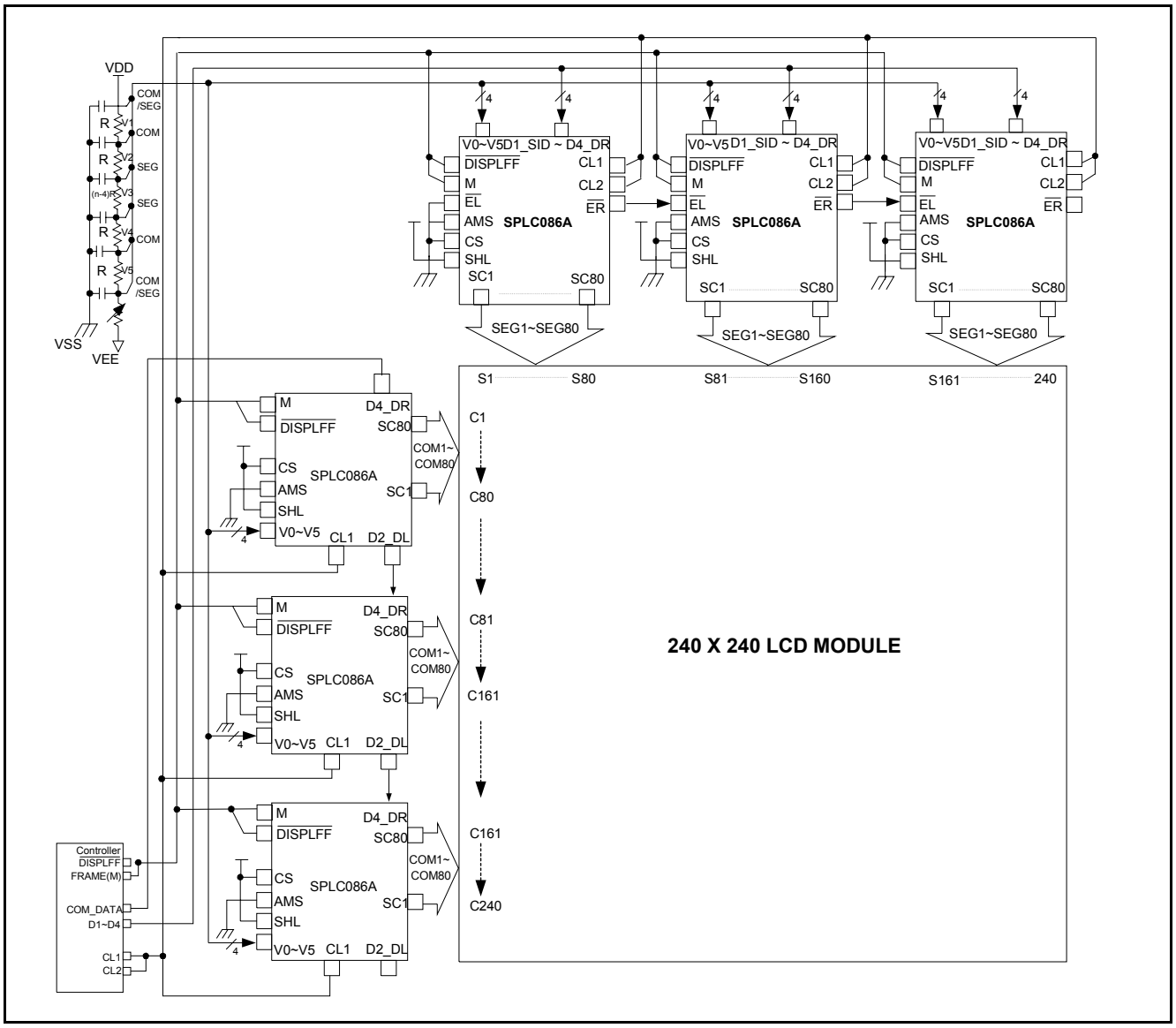


6.4. Dual-Type Interface Mode (40-ch + 40-ch Common Driver)



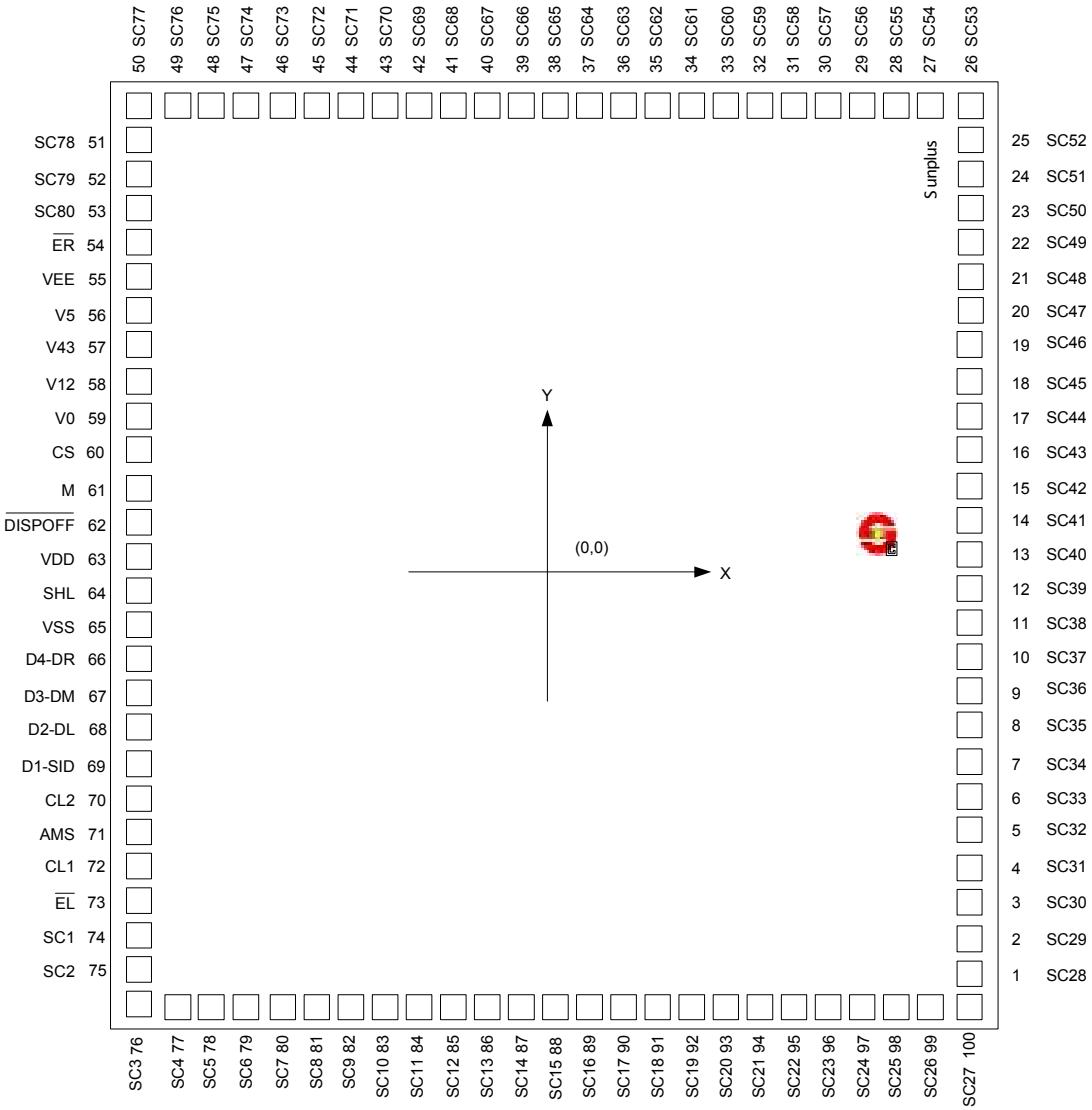
Note: Using this application mode (dual-type common mode), the duty ratio can be reduced to half. In case, 1/200 duty can be used to drive the 400 common LCD panel.

6.5. Application Circuit Example



7. PACKAGE/PAD LOCATIONS

7.1. PAD Assignment (SPLC086A)



Chip Size: 3190μm X 3260μm

PAD Size: 96μm X 96μm

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

7.2. Ordering Information

Product Number	Package Type
SPLC086A-nnnnV-C	Chip form
SPLC086A-nnnnV-PL08	Package form - 100LQFP

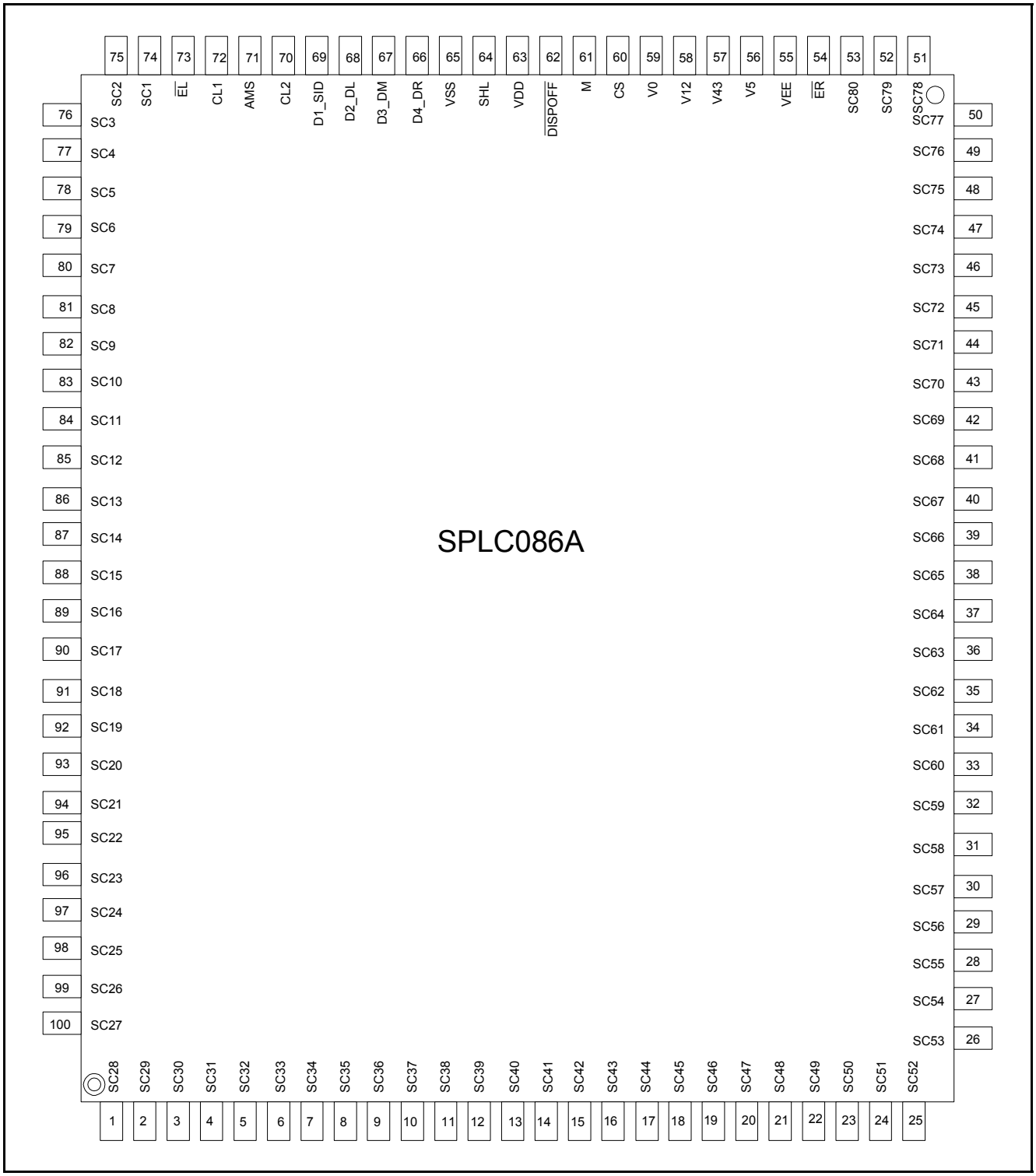
Note1: Code number (nnnV) is assigned for the customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

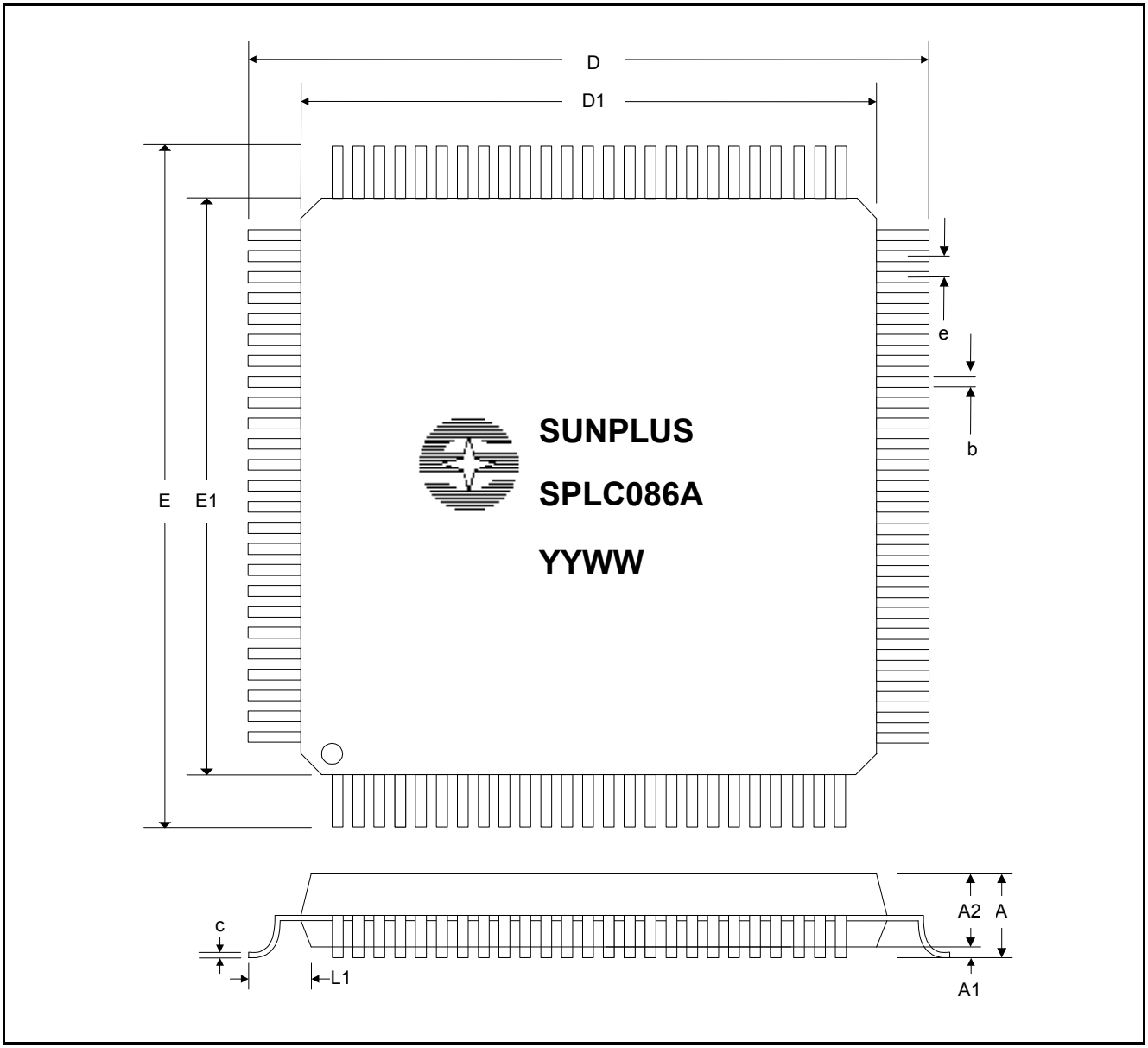
7.3. PAD Locations (SPLC086A)

PAD No.	PAD Name	Locations		PAD No.	PAD Name	Locations		PAD No.	PAD Name	Locations	
		X	Y			X	Y			X	Y
1	SC28	1445	-1360	35	SC62	353	1476	69	D1-SID	-1445	-659
2	SC29	1445	-1240	36	SC63	237	1476	70	CL2	-1445	-775
3	SC30	1445	-1120	37	SC64	121	1476	71	AMS	-1445	-890
4	SC31	1445	-1005	38	SC65	5	1476	72	CL1	-1445	-1005
5	SC32	1445	-890	39	SC66	-111	1476	73	$\overline{EL}$	-1445	-1120
6	SC33	1445	-775	40	SC67	-227	1476	74	SC1	-1445	-1240
7	SC34	1445	-659	41	SC68	-343	1476	75	SC2	-1445	-1360
8	SC35	1445	-549	42	SC69	-459	1476	76	SC3	-1445	-1480
9	SC36	1445	-439	43	SC70	-575	1476	77	SC4	-1308	-1480
10	SC37	1445	-329	44	SC71	-691	1476	78	SC5	-1180	-1480
11	SC38	1445	-219	45	SC72	-812	1476	79	SC6	-1054	-1480
12	SC39	1445	-109	46	SC73	-933	1476	80	SC7	-933	-1480
13	SC40	1445	1	47	SC74	-1054	1476	81	SC8	-812	-1480
14	SC41	1445	111	48	SC75	-1180	1476	82	SC9	-691	-1480
15	SC42	1445	221	49	SC76	-1308	1476	83	SC10	-575	-1480
16	SC43	1445	331	50	SC77	-1445	1476	84	SC11	-459	-1480
17	SC44	1445	441	51	SC78	-1445	1356	85	SC12	-343	-1480
18	SC45	1445	551	52	SC79	-1445	1236	86	SC13	-227	-1480
19	SC46	1445	661	53	SC80	-1445	1116	87	SC14	-111	-1480
20	SC47	1445	771	54	$\overline{ER}$	-1445	1001	88	SC15	5	-1480
21	SC48	1445	886	55	VEE	-1445	886	89	SC16	121	-1480
22	SC49	1445	1001	56	V5	-1445	771	90	SC17	237	-1480
23	SC50	1445	1116	57	V43	-1445	661	91	SC18	353	-1480
24	SC51	1445	1236	58	V12	-1445	551	92	SC19	469	-1480
25	SC52	1445	1356	59	V0	-1445	441	93	SC20	585	-1480
26	SC53	1445	1476	60	CS	-1445	331	94	SC21	701	-1480
27	SC54	1318	1476	61	M	-1445	221	95	SC22	822	-1480
28	SC55	1190	1476	62	$\overline{DISPOFF}$	-1445	111	96	SC23	943	-1480
29	SC56	1064	1476	63	VDD	-1445	1	97	SC24	1064	-1480
30	SC57	943	1476	64	SHL	-1445	-109	98	SC25	1190	-1480
31	SC58	822	1476	65	VSS	-1445	-219	99	SC26	1318	-1480
32	SC59	701	1476	66	D4-DR	-1445	-329	100	SC27	1445	-1480
33	SC60	585	1476	67	D3-DM	-1445	-439				
34	SC61	469	1476	68	D2-DL	-1445	-549				

7.4. SPLC086A LQFP Type (SPLC086A): 100LQFP



7.5. Package Information



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
D	15.85	16.00	16.15	Millimeter
D1	13.90	14.00	14.10	Millimeter
E	15.85	16.00	16.15	Millimeter
E1	13.90	14.00	14.10	Millimeter
L1	1.00 REF			Millimeter
b	0.17	0.22	0.27	Millimeter
c	0.09	-	0.20	Millimeter
e	0.50 BSC			Millimeter

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 15, 2001	0.1	Original	
JAN. 11, 2002	0.2	1. Add Sunplus logo in the "*7.1 PAD Assignment (SPLC086A)*" 2. Redefine "Product number" in the "*7.2 Ordering Information*" 3. Correct *"7.5 Package Information*" 4. Modify DISPOFFB to $\overline{\text{DISPOFF}}$, ERB to $\overline{\text{ER}}$ and ELB to $\overline{\text{EL}}$.	27 27 30