DATA SHEET

凌陽科技
SUNPLUS

SPL61A

80KB LCD Controller/Driver

AUG. 13, 2001

Version 1.2

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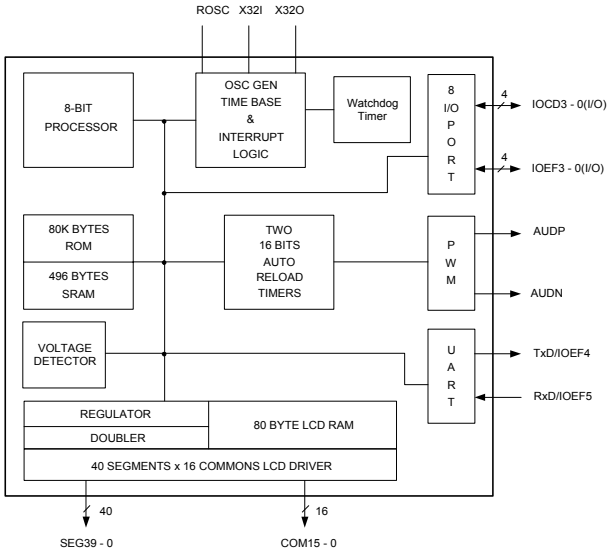
80KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPL61A, an 8-bit CMOS single chip microprocessor, contains RAM, ROM, I/Os, interrupt/wakeup controller, 8-bit PWM audio output, UART and automatic display controller/driver for LCD. With a dual channel PWM driver, attractive sound effects can be generated easily. A built-in UART speeds up data transmission between two chips. Furthermore, a software controllable standby switch is also built-in to save power consumption. The great amount of ROM can be used to store both program and audio data. (The speech duration is approximately 18 seconds at 7KHz sampling rate by using 4-bit ADPCM). The SPL61A is designed with state-of-the-art technology to fulfill the requirements of LCD applications especially hand-held products.

2. BLOCK DIAGRAM



Note1: IOAB3 - 0 can be enabled by mask option from Segment 39 - 36. Each I/O(segment) can be mask optioned individually.

Note2: TxD and RxD can be optioned to IOEF5 - 4 when UART is not used.

3. FEATURES

- Built-in 8-bit processor
  - 496 bytes SRAM
  - 80K bytes ROM
  - Max. operating speed: 3.0MHz @ 2.6V
  - CPU clock is software programmable, can be 1/2, 1/4, 1/8 or 1/16 of R-oscillator's clock frequency
  - Key wake-up
  - Provide 8 interrupt sources
- Asynchronous serial interface
  - Supports bit rates up to 115.2 Kbps
- Programmable LCD driver
  - Up to 40 segments, up to 16 commons, maximum 640 dots
  - 1/4 or 1/5 bias capability
  - 1/8, 1/12 or 1/6 duty
  - 80 bytes dedicated LCD RAM
  - LCD com/seg driving strength can be adjusted to compromise the display quality and current consumption
  - Built-in voltage doubler and voltage regulator to generate VLCD for LCD driver
  - 16-level VLCD adjustable (3.3V - 4.8V)
- Power saving SLEEP mode
- Low voltage detector
  - 2.6V and 2.4V detection
- Peripherals
  - 8 I/O pins (IOEF3 - 0, IOCD3 - 0)
  - 4 I/O pins shared with LCD segments (mask option)
  - Extra 2 I/O pins (IOEF5 - 4) when UART is not used (mask option)
  - Extra 2 I/O pins (IOEF7 - 6) when LCD is in 1/8 or 1/12 duty (mask option)
  - Built-in 32.768KHz oscillator circuit for real time clock function
  - Built-in R-oscillator (only one resistor is needed)
  - Internal time base generator
  - Two 16-bit reloadable timer/counters
  - 8-bit resolution, 2-channel PWM outputs (can drive speaker or buzzer directly)
  - Watchdog Timer for reliable operation
- Wide operating voltage:
  - 2.4V - 3.6V @ 1.0MHz
  - 3.6V - 5.5V @ 1.0MHz
- Low-power consumption:
  - 1mA typical @ 3.0V, F_{CPU} = 1.0MHz
  - <1μA typical standby current @ 3.0V

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG39 - 37 SEG36 SEG35 - 0	79 - 81 1 7 - 42	O	LCD driver segment output. SEG39 - 36 can be optioned to IOAB3 - 0. Port AB is a bi-directional I/O port.
COM15 - 14 COM13 - 0	67 - 68 56 - 43	O	LCD driver common output. COM15 - 14 can be optioned to IOEF7 - 6. Port EF is a bi-directional I/O port.
IOEF3 - 0	71 - 74	I/O	Port EF is a bi-directional I/O port, can be software programmed as wake up I/O.
IOCD3 - 0	75 - 78	I/O	Port CD is a bi-directional I/O port.
RxD	69	I	UART input. Can be optioned to IOEF5
TxD	70	O	UART output. Can be optioned to IOEF4
ROSC	66	I	ROSC input, connect to VDD through a resistor
RESET	60	I	System reset input, low active.
AUDP AUDN	2 4	O	PWM audio output
X32I	63	I	32.768KHz crystal input or connect to VDD through a resistor (option)
X32O	62	O	32.768KHz crystal output
TEST	61	I	Test input
VLCD	64	P	LCD voltage. Connect to VSS through a capacitor if voltage doubler is enabled.
HVLCD	59	P	LCD voltage generation. Connect to VSS through a capacitor if voltage regulator is enabled.
CUP1 CUP2	58 57	P	LCD voltage generation. Charge pump capacitor interconnection pins
VDD	65	P	Power supply voltage input
VSS	6	P	Ground reference
AVDD	3	P	Analog power
AVSS	5	P	Analog ground reference

Legend: I = Input, O = Output, P = Power

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area

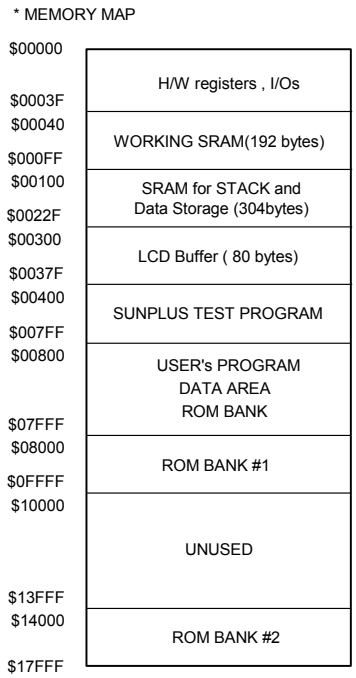
SPL61A is a large ROM based micro-controller with 640 dots LCD driver. The large ROM can be defined as program ROM, LCD fonts and audio data continuously without any limitation. To access the ROM area, users should first program the BANK SELECT Register ($07) and then access the bank#1 or bank#2 by addressing the higher bank address, $8000 - $FFFF, to fetch data.

5.2. Map of Memory and I/Os

*I/O PORT:
- PORT IOAB $0002
- PORT IOCD $0003
- PORT IOEF $0004
- I/O AB_CTRL $0001
- I/O CD_CTRL $0000
- I/O EF_CTRL $0006

*NMI SOURCE:
- INT1 (from TIMER 1)

*INT SOURCE:
- INT0 (from TIMER 0)
- INT1 (from TIMER 1)
- 2 KHz
- T2 Hz (2Hz / 1 Hz)
- T16 Hz (4Hz/8Hz/16Hz/32Hz)
- 128 Hz
- EXT INT (from IOCD0 pin)
- UART



Note: $7FFA - $7FFF in ROM bank#0, and $FFFA - $FFFF in bank#1 - 2 are reserved for reset vectors.
$7FF2 - $7FF7 in bank#0, and $FFF2 - $FFF7 in bank#1 - 2 are reserved for testing.

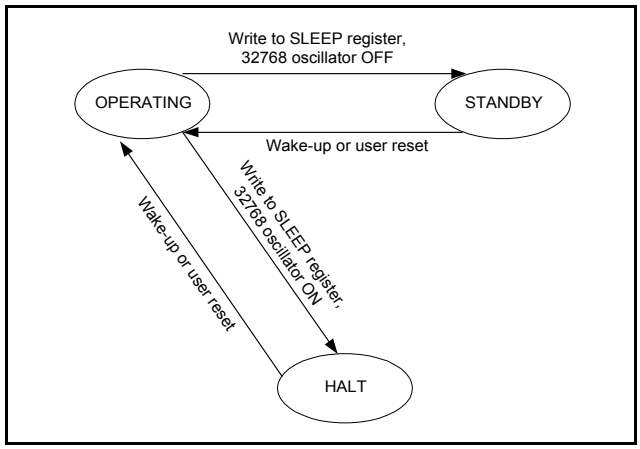
5.3. Operating States

The SPL61A supports three operating states: standby, halt, and operating. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating state, all modules (CPU, 32768 oscillator, timer/counter, LCD driver…) are activated. The halt/standby state is entered by writing to SLEEP register ($09). There are four wake-up sources in SPL61A: port IOEF wake-up, TIMR0 wake-up, 4Hz/8Hz/16Hz/32Hz wake-up and 2Hz/1Hz wake-up. If any wake-up event occurs, execution of the next instruction continues in the operating state.

When in standby, all modules will be shut down, and RAM and I/Os remain in their previous states. The current consumption is minimized in standby. By writing to SLEEP register but keeps 32768 oscillator running, the system is in halt state. In halt state, CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up. The 32768 related modules (timer/counter, LCD driver…) may remain active in the halt state. Following figure is a state diagram for the SPL61A.



State Diagram of SPL61A

5.4. Speech and Melody

Since SPL61A provides large ROM and wide range of CPU operating speed, it is the most appropriate IC for speech and melody synthesis. For speech synthesis, SPL61A provides several timer interrupts for precise sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound then can be played back in the sequence assigned by users' programs. Several algorithms are recommended for high fidelity and good compression of sound: such as PCM and ADPCM.

For melody synthesis, SPL61A provides the dual tone mode. Once in the dual tone mode, users only need to program the tone frequency of each channel by writing to timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically without users' care.

5.5. LCD Controller/Driver

SPL61A contains total of 640 dots LCD controller and driver. Programmers can set the LCD configuration (bias, duty, voltage doubler) by writing to LCD control register ($20). Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. The LCD driver in SPL61A is designed to fit most LCD specifications. It can either be programmed as 1/4 or 1/5 bias and the duty is also programmable as 1/8, 1/12, or 1/16 duty.

5.6. Voltage Doubler/Regulator

SPL61A also contains a built-in voltage doubler and a voltage regulator. The voltage regulator provides a reference voltage (HVLCD) for voltage doubler to generate VLCD (by charge-pumping). Users can get desired VLCD by changing the output reference voltage (writing to $23) of the voltage regulator. By enabling the voltage doubler and regulator, users can get a stable VLCD that will not be affected by VDD. The three possible configurations of voltage doubler and regulator are shown in the following table.

Regulator	Doubler	VLCD
OFF	OFF	VDD (not regulated)
OFF	ON	2*VDD (not regulated)
ON	OFF	N/A
ON	ON	3.3V - 4.8V adjustable

5.7. PWM Output

Internally, SPL61A has one pair of PWM outputs with two sound channels. Each channel can be set to play speech or tone individually. SPL61A uses Pulse Width Modulation that could directly drive speaker or buzzer without any buffer or amplification circuit.

5.8. Asynchronous Serial Interface

SPL61A supports 1-channel UART for serial communications. It supports bit rates up to 115.2kbps. UART operation is controlled by UART command registers $29 and $2A. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be set in command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt asserts when a byte is received or transmitted. By reading the status register $2A, users can tell whether the interrupt is generated by Rx or Tx. Framing, overrun and parity errors are detected as each byte is received. All error status can be read from status register $2A.

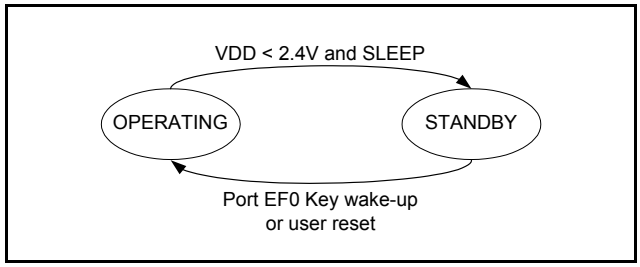
The UART supports clock auto calibration. If this clocking scheme is selected, standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to baud rate control registers $2E and $2F. The supported standard baud rates and their minimum R-oscillator clock frequency required are shown in the following table.

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration clocking scheme is not selected, users can get desired baud rates by writing appropriate values to prescaler registers, $2C and $2D. Non-standard baud rates can be obtained this way. When using non-calibration mode, one should aware that the frequency of R-oscillator may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

5.9. Low Voltage Detection

The SPL61A provides a 2.6V/2.4V voltage detector to detect a low voltage event. Users can turn on 2.6V detection and read bit1 of port $24 periodically to monitor if VDD is lower than 2.6V. In addition, if 2.4V detection is turned on and VDD drops below 2.4V, after a SLEEP command is issued, system will shut down all activities(LCD bias, LCD display, 32768 oscillator) and enters standby to reduce current consumption. This low voltage power down can be awakened by a PEF0 key change or RESET. Users can use this feature to implement low battery check/battery change function.



State Diagram of Low Voltage Power Down

5.10. Watch Dog Timer (WDT)

An on chip watchdog timer is available on SPL61A. The WDT is designed for recovering from system abnormal operation. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to $0F. Note that the WDT only works when 32768Hz clock is available.

5.11. Mask Options

5.11.1. 32768 oscillator

1). X'TAL
2). R-oscillator

5.11.2. Watchdog timer

1). Enable
2). Disable

5.11.3. TxD/RxD select

1). TxD as UART transmit output, RxD as UART receive input
2). TxD as I/O port EF4, RxD as I/O port EF5

5.11.4. Port EF Bit7 - 0 with 600KΩ pull-low

1). Each bit can be optioned to Enable/Disable individually.

5.11.5. I/O and LCD driver

1). COM15 -14 can be optioned to IOEF7 - 6 when LCD mode is 1/8 duty or 1/12 duty.
2). SEG39 - 36 can be optioned to IOAB3 - 0 individually.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics

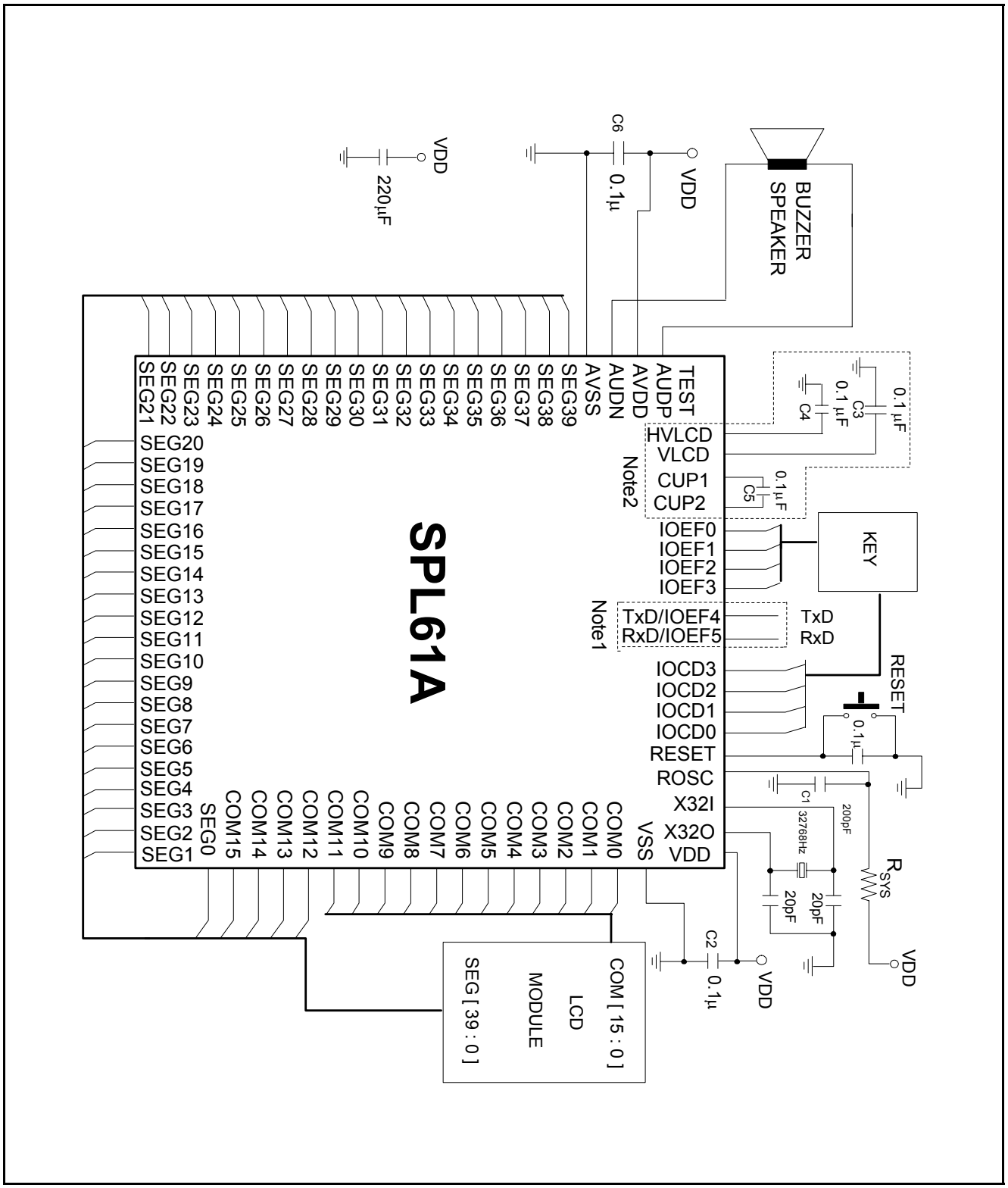
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-batter
Operating Current	I_{OP}	-	1.0	-	mA	F_{CPU} = 1.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	1.0	2.0	μA	VDD = 3.0V, 32768Hz OFF
Audio Output Current	I_{OH}	-	-20	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-40	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	25	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	50	-	mA	VDD = 3.0V, V_{OL} = 1.0V
VLCD Variation	V_{LCD_VAR}	-	±0.2	-	V	VDD = 2.6V - 5.0V VLCD = 4.5V LCD bias strength = $04, no LCD panel applied
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-	-800	-	μA	VDD = 3.0V V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	-	1000	-	μA	VDD = 3.0V V_{OL} = 0.8V
OSC Resistor	R_{OSC}	-	220K	-	ohm	F_{OSC2} = 2.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	3.0	MHz	F_{CPU} = F_{OSC2} /2 @ 2.6V

Note1: V_{LCD} variation is subject to change due to the variation of process, temperature, supply voltage and loadings.

Note2: When voltage regulator and voltage doubler are enabled, VDD should be lower than V_{LCD} to prevent forward biasing the p-n junction of I/O's output PMOS.

7. APPLICATION CIRCUITS

7.1. 640 Points LCD Driver, 40 Segments X 16 Commons, 32768 Mask Option X'TAL

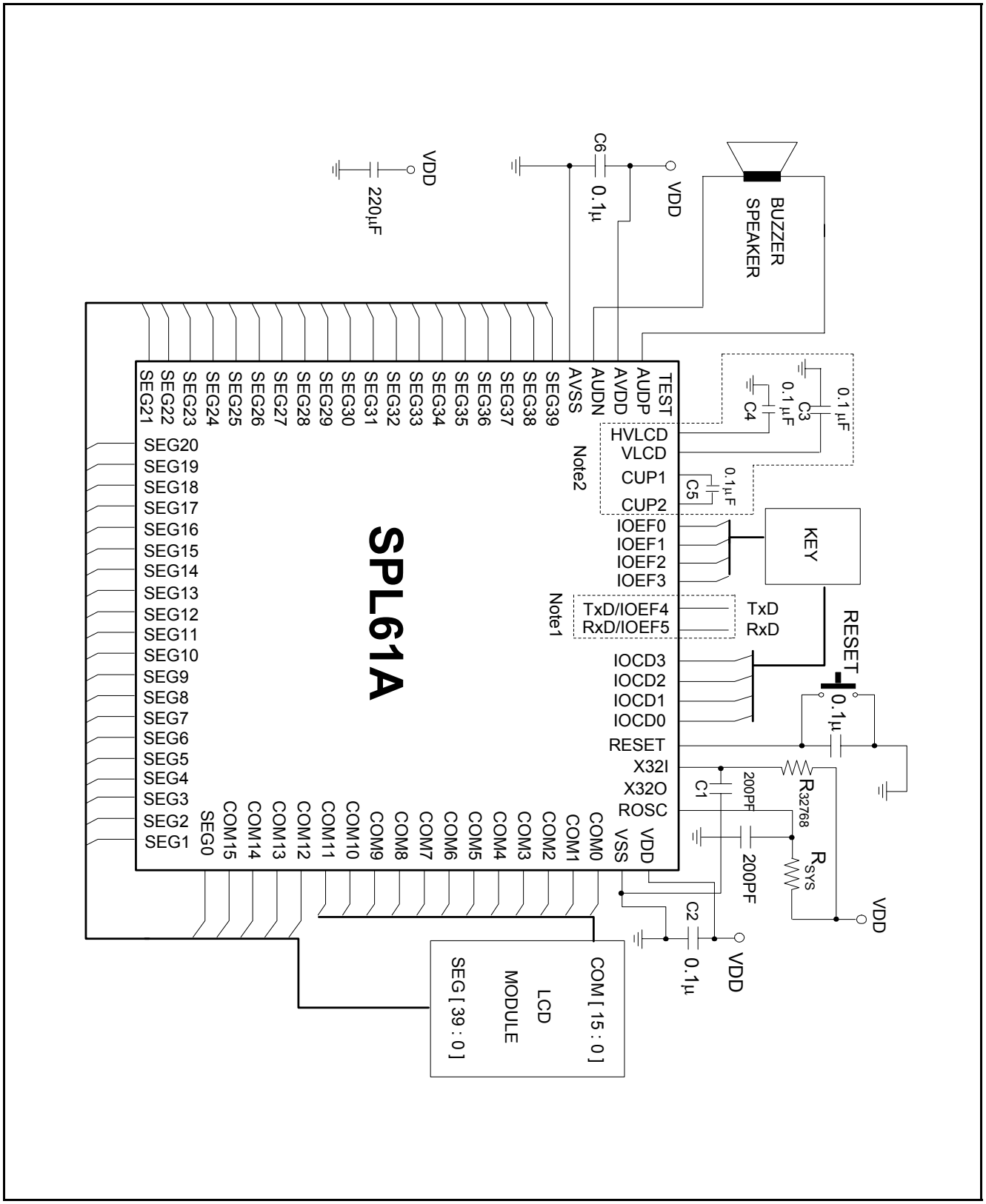


Note1: IOEF4, IOEF5 are shared with TxD, RxD(UART), if UART is not used, these two pins can be used as I/O ports

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

7.2. 640 Points LCD Driver, 40 Segments X 16 Commons, 32768 Mask Option R-Oscillator

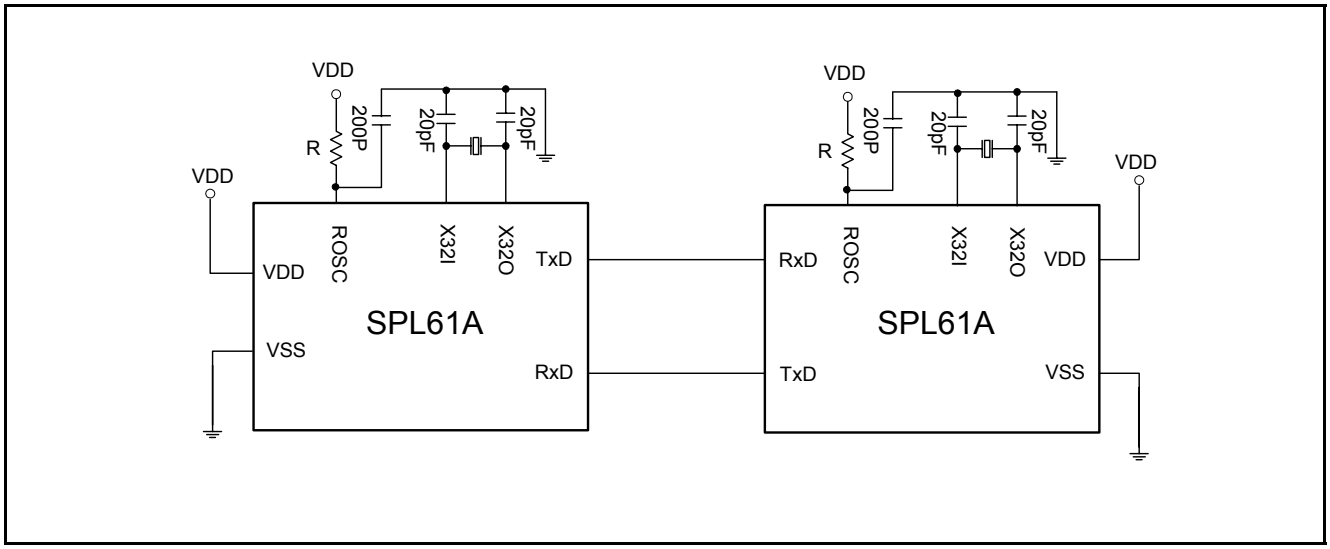


Note1: IOEF4, IOEF5 are shared with TxD, RxD(UART), if UART is not used, these two pins can be used as I/O ports

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

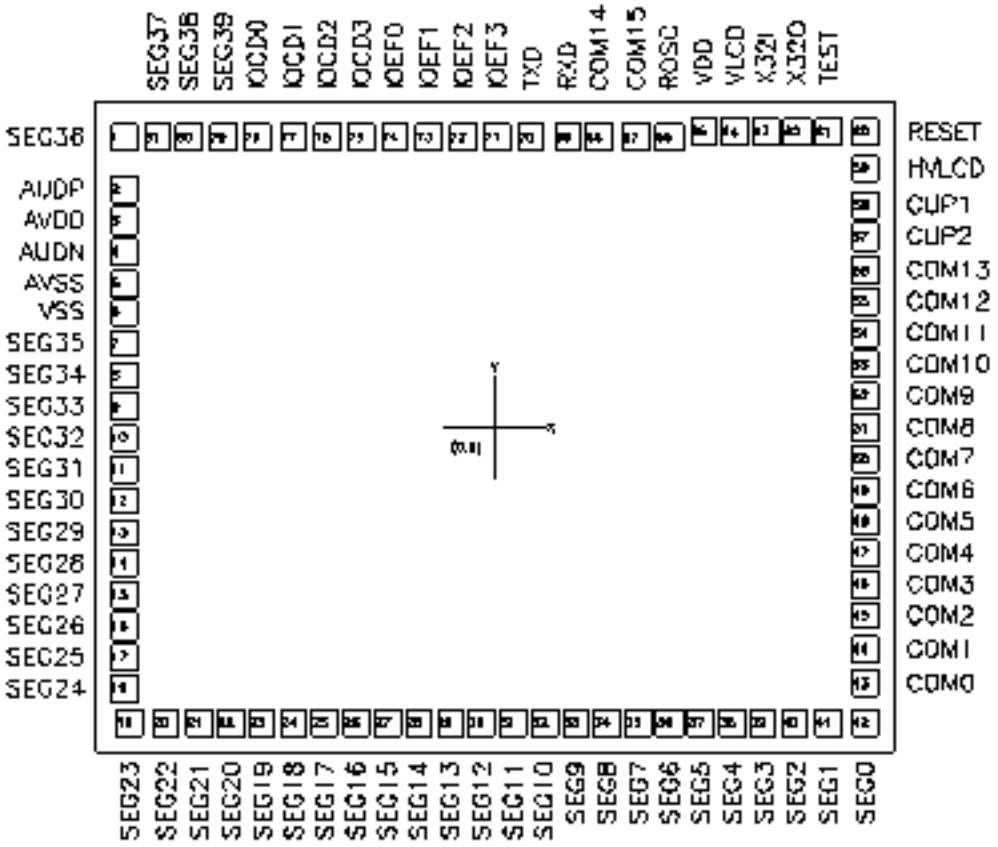
Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

7.3. Serial Communications between two SPL61As



8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



Chip Size: 3190μm x 2620μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
SPL61A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG36	-1420	1110	42	SEG0	1416	-1131
2	AUDP	-1416	905	43	COM0	1416	-986
3	AVDD	-1416	785	44	COM1	1416	-851
4	AUDN	-1416	665	45	COM2	1416	-724
5	AVSS	-1416	545	46	COM3	1416	-601
6	VSS	-1416	440	47	COM4	1416	-481
7	SEG35	-1416	320	48	COM5	1416	-361
8	SEG34	-1416	200	49	COM6	1416	-241
9	SEG33	-1416	80	50	COM7	1416	-121
10	SEG32	-1416	-40	51	COM8	1416	-1
11	SEG31	-1416	-160	52	COM9	1416	119
12	SEG30	-1416	-280	53	COM10	1416	239
13	SEG29	-1416	-400	54	COM11	1416	359
14	SEG28	-1416	-520	55	COM12	1416	479
15	SEG27	-1416	-640	56	COM13	1416	599
16	SEG26	-1416	-760	57	CUP2	1416	721
17	SEG25	-1416	-880	58	CUP1	1416	849
18	SEG24	-1416	-1000	59	HVLCD	1416	984
19	SEG23	-1401	-1131	60	RESET	1416	1129
20	SEG22	-1261	-1131	61	TEST	1276	1129
21	SEG21	-1133	-1131	62	X32O	1156	1129
22	SEG20	-1013	-1131	63	X32I	1036	1129
23	SEG19	-893	-1131	64	VLCD	916	1129
24	SEG18	-773	-1131	65	VDD	796	1129
25	SEG17	-653	-1131	66	ROSC	666	1110
26	SEG16	-533	-1131	67	COM15	539	1110
27	SEG15	-413	-1131	68	COM14	404	1110
28	SEG14	-293	-1131	69	RXD	277	1110
29	SEG13	-173	-1131	70	TXD	142	1110
30	SEG12	-53	-1131	71	IOEF3	15	1110
31	SEG11	67	-1131	72	IOEF2	-120	1110
32	SEG10	187	-1131	73	IOEF1	-247	1110
33	SEG9	307	-1131	74	IOEF0	-382	1110
34	SEG8	427	-1131	75	IOCD3	-509	1110
35	SEG7	547	-1131	76	IOCD2	-641	1110
36	SEG6	667	-1131	77	IOCD1	-768	1110
37	SEG5	787	-1131	78	IOCD0	-911	1110
38	SEG4	907	-1131	79	SEG39	-1038	1110
39	SEG3	1027	-1131	80	SEG38	-1166	1110
40	SEG2	1147	-1131	81	SEG37	-1293	1110
41	SEG1	1276	-1131				

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10. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 01, 1999	0.1	Original	
MAY. 28, 1999	0.2	1. Renew to a new document format 2. Modify ROM Size: 72K Bytes -> 80K Bytes 3. Modify SRAM Size: 704 Bytes -> 496 Bytes 4. Modify "*5.2 Map of Memory and I/Os*" 5. Add "*5.3 Operating States*" 6. Add "*5.6 Voltage Doubler/Regulator*" 7. Add "*5.8 Asynchronous Serial Interface*" 8. Add "*8.3. Serial Communications Between Two SPL61As*"	
DEC. 03, 1999	1.0	1. Delete "*PRELIMINARY*" 2. Renew to a new document format	
JUN. 01, 2001	1.1	1. Correct "*8.1 640 Points LCD Driver, 40 Segments X 16 Commons, 32768 Mask Option X'TAL*" RESET switch 0.1μF capacitor. 2. Add "Note**:** The 0.1μF capacitor between VDD and VSS…" 3. Renew to a new document format	8 11
AUG. 13, 2001	1.2	1. Correct chip size 2. Add Note1 in the "*8.1 PAD Assignment*" 3. Renew to a new document format	12 12