DATA SHEET

SAP3305
Dot Matrix STN LCD Controller

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1 GENERAL

1.1 Description

The SAP3305 series is a controller IC that can display text and graphics on LCD panel.

The SAP3305 series can display layered text and graphics , scroll the display in any direction and partition the display into multiple screens.

The SAP3305 series stores text , character codes and bitmapped graphics data in external frame buffer memory . Display controller functions include transferring dara from the controlling micropocessor to the buffer memory, reading memory data, converting data to dislay pixels and generating timing signals for the buffer memory , LCD panel.

The SAP3305 series has an internal character generator with 160,5 x 7 pixel characters in internal mask ROM. The characters generator support up to 64, 8 x 16 pixel character in external character generator RAM and up to 256, 8 x 6 pixel characters in external character generator ROM.

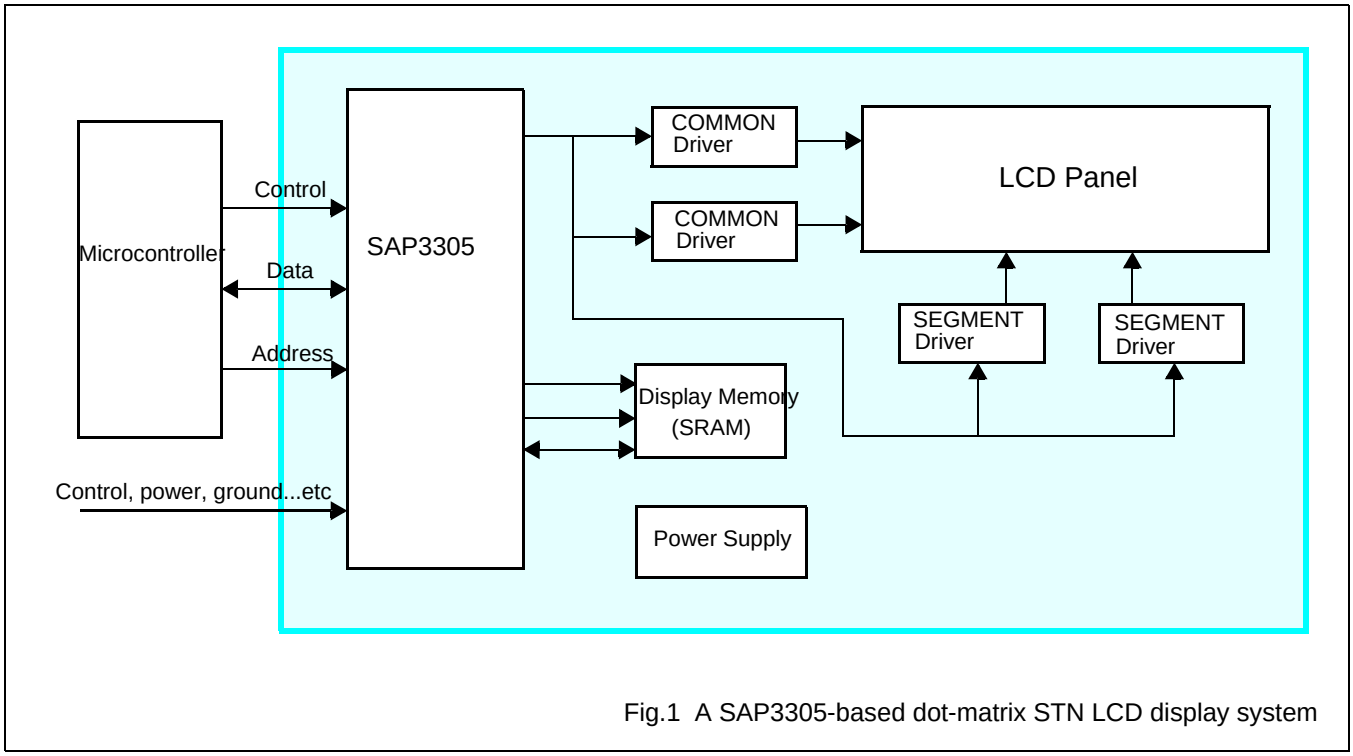


Fig.1 A SAP3305-based dot-matrix STN LCD display system

2 FEATURES

- Text,graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Up to 640 x 256 pixel LCD panel display resolution
- Programmable cursor control
- Smooth horizontal and vertical scrolling of all or part of the display
- 1/2-duty to 1/256-duty LCD drive
- Up to 640 x 256 pixel LCD panel display resolution memory
- 160, 5 x 7 pixel characters in internal mask-programmed character generator ROM
- Up to 64, 8 x 16 pixel characters in external character generator RAM
- Up to 256, 8 x 16 pixel characters in external character generator ROM
- 6800 and 8080 family microprocessor interfaces
- Low power consumption-3.5mA operating current (V_{DD}=3.5V), 0.05μA standby current
- Operating voltage range (control logic): 2.7 ~ 5.5 volts..
- Operating frequency range: 10 MHz, when V_{DD}= 5 volts.
- Operating temperature range: -20 to +70 °C.
- Storage temperature range: -55 to +125 °C.

3 ORDERING INFORMATION

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SAP3305-QFPG	QFP60 Pb-free package.

4 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

4.1 Funtional block diagram

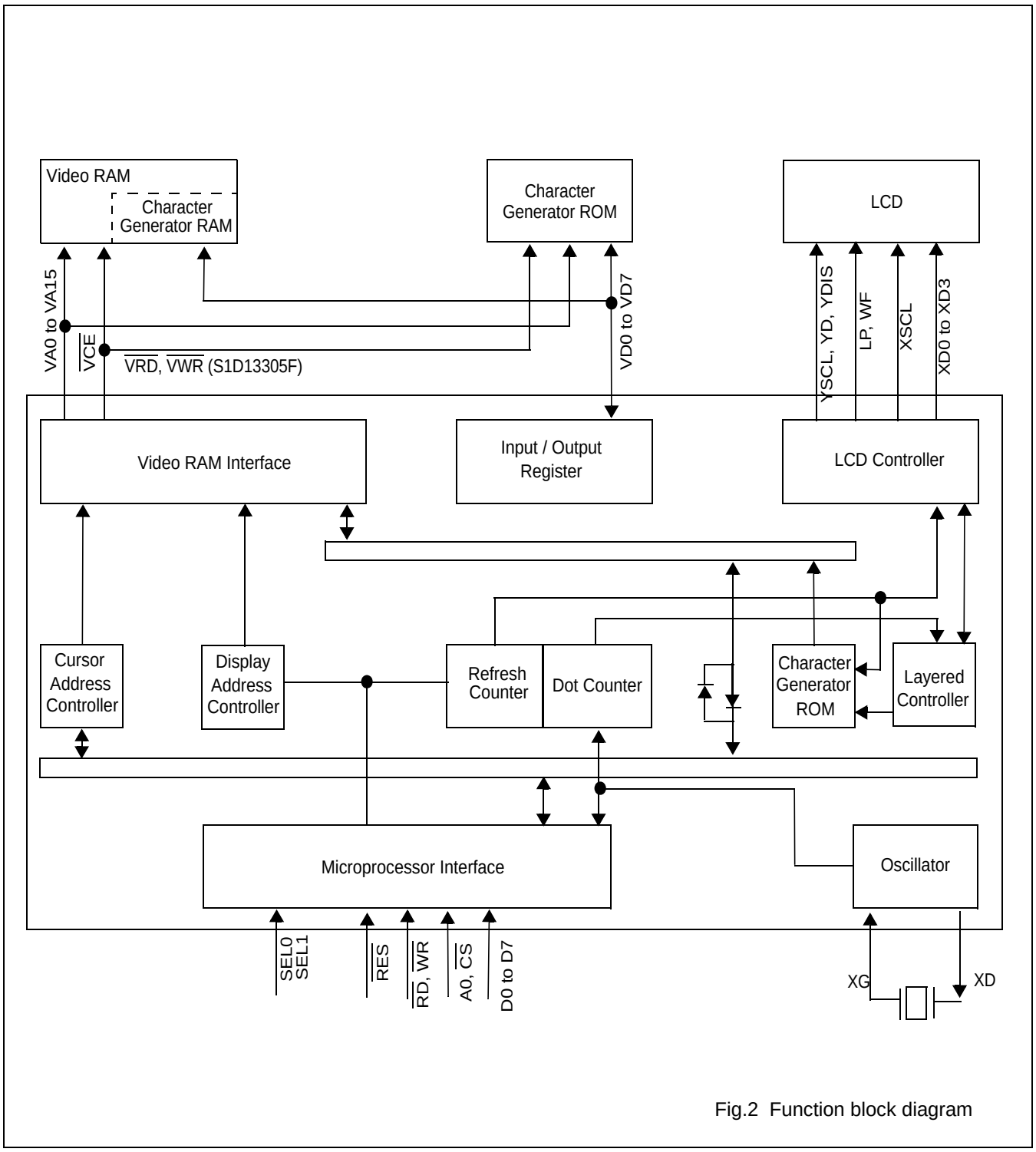


Fig.2 Function block diagram

5 PIN ASSIGNMENT, PAD PLACEMENT AND COORDINATES, SIGNAL DESCRIPTION

5.1 Pin assignment (QFP60)

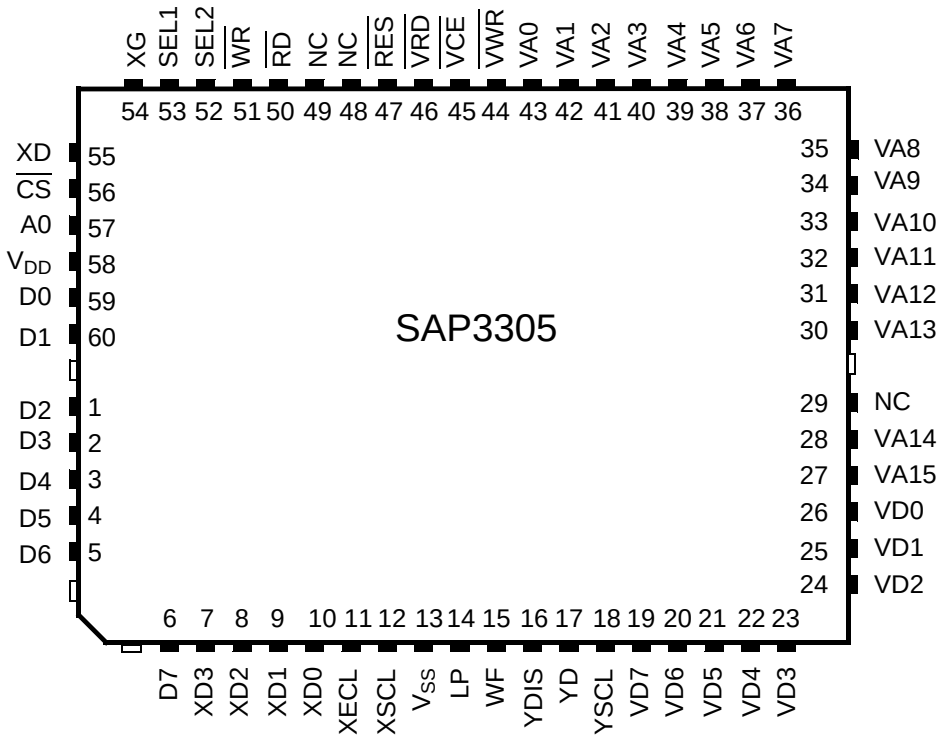
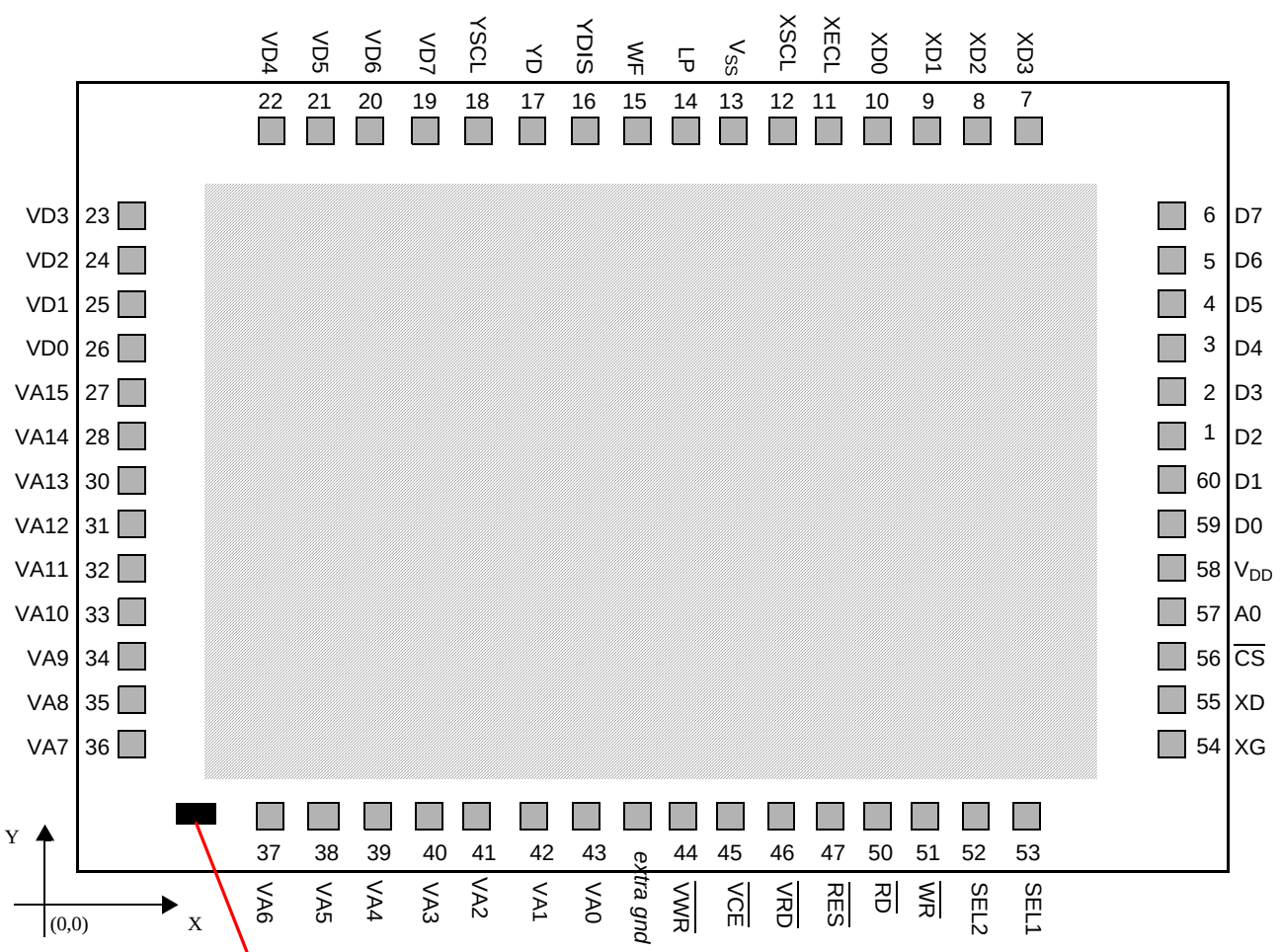


Fig.3 Pin assignment of the QFP60 package.

5.2 Pad Placement



Graphic logo

Note:

(1) A graphic logo, which looks like a flying bird, is placed at the lower left region of the chip's layout area.

(2) The *extra_gnd* pad at coordinate (1520, 56.3) is internally connected to pad 13, the Vss pad, at coordinate (1816, 2687). It is intended for extra ground bonding if your PCB layout has an extra ground bonding pad. Otherwise, it can be left unconnected.

(3) chip size : 3202 μm x 2755 μm.

(4) Bonding pad size: 86 μm x 86 μm.

Fig.4 Pad placement

5.3 Pad coordinates

Table 2 The SAP3305 pad coordinates (unit: mm)

PAD NO.	PAD NAME	X	Y
1	D2	3133	1520
2	D3	3133	1668
3	D4	3133	1816
4	D5	3133	1964
5	D6	3133	2112
6	D7	3133	2260
7	XD3	2704	2687
8	XD2	2556	2687
9	XD1	2408	2687
10	XD0	2260	2687
11	XECL	2112	2687
12	XSCL	1964	2687
13	V_{SS}	1816	2687
14	LP	1668	2687
15	WF	1520	2687
16	YDIS	1372	2687
17	YD	1224	2687
18	YSCL	1076	2687
19	VD7	930	2687
20	VD6	782	2687
21	VD5	634	2687
22	VD4	486	2687
23	VD3	55	2260.02
24	VD2	55	2112.02
25	VD1	55	1964
26	VD0	55	1816.03
27	VA15	55	1668
28	VA14	55	1520
29	NC		
30	VA13	55	1371.97
31	VA12	55	1224.6

PAD NO.	PAD NAME	X	Y
32	VA11	55	1076
33	VA10	55	928
34	VA9	55	780
35	VA8	55	632
36	VA7	55	484
37	VA6	484	56.3
38	VA5	632	56.3
39	VA4	780	56.3
40	VA3	928	56.3
41	VA2	1076	56.3
42	VA1	1224	56.3
43	VA0	1372	56.3
extra gnd (optional)		1520	56.3
44	$\overline{VWR}$	1668	56.3
45	$\overline{VCE}$	1816	56.3
46	$\overline{VRD}$	1964	56.3
47	$\overline{RES}$	2112	56.3
48	NC		
49	NC		
50	$\overline{RD}$	2260	56
51	$\overline{WR}$	2408	56
52	SEL2	2556	56
53	SEL1	2704	56
54	XG	3133	483.4
55	XD	3133	631.4
56	$\overline{CS}$	3133	780
57	A0	3133	928
58	V_{DD}	3133	1076
59	D0	3133	1224
60	D1	3133	1372

5.4 Signal description

Table 3 Pin Summary

Pin number	SYMBOL	I/O	DESCRIPTION
27~28 30~43	VA0 to VA15	output	VRAM address bus
44.	$\overline{VWR}$	output	VRAM write signal
45	$\overline{VCE}$	output	Memory control signal
46	$\overline{VRD}$	output	VRAM read signal
47	$\overline{RES}$	input	Reset
28,48,49	NC		No connection
50	$\overline{RD}$	input	8080 family: Read signal 6800 family: Enable clock(E)
51	$\overline{WR}$	input	8080 family: Write signal 6800 family: R/$\overline{W}$ signal
52	SEL2	input	8080 or 6800 family interface select
53	SEL1	input	8080 or 6800 family interface select
54	XG	input	Oscillator connection
55	XD	output	Oscillator connection
56	$\overline{CS}$	input	Chip select
57	A0	input	Data type select
58	VDD	Supply	2.7 to 5.5V supply
59~60 1~6	D0~D7	I/O	Data bus
7~10	XD0~XD3	output	X-driver data
11	XECL	output	X-driver enable chain clock
12	XSCL	output	X-driver data shift clock
13	VSS	Supply	Ground
14	LP	output	Latch pluse
15	WF	output	Frame signal
16	YDIS	output	Power-down signal when display is blanked
17	YD	output	Scan start pulse
18	YSCL	output	Y-driver shift clock
19~26	VDD~VD7	I/O	VRAM data bus

5.5 Pin Functions

5.5.1 POWER SUPPLY

Table 4

SYMBOL	DESCRIPTION
VDD	2.7 to 5.5V supply. This may be the same supply as the controlling microprocessor.
VSS	Ground

Note:

The peak supply current drawn by the SAP3305 series may be up to ten times the average supply current. The power supply impedance must be kept as low as possible by ensuring that supply lines are sufficiently wide and by placing 0.47 mF decoupling capacitors that have good high-frequency response near the device's supply pins.

5.5.2 OSCILLATOR

Table 5

SYMBOL	DESCRIPTION
$\overline{XG}$	Crystal connection for internal oscillator (See section 13).This pin can be driven by an external clock source that satisfies the timing specification of the EXT 0 signal (See section 6.36).
$\overline{XD}$	Crystal connection for internal oscillator .Leave this pin open when using an external clock source.

5.5.3 MICROPROCESSOR INTERFACE

Table 6

<table>
<tr><th>SYMBOL</th><th>DESCRIPTION</th></tr>
<tr><td>D0~D7</td><td>Tristate input/output pins.connect these pins to an 8- or 16-bit microprocessor bus.</td></tr>
<tr><td>SEL1,SEL2</td><td>Microprocessor interface select pin . The SAP3350 series supports both 8080 family processors (sch as the 8085 and Z80)and 6800 family processors (such as the 6802 and 6809).
<table>
<tr><th>SEL1</th><th>SEL2★</th><th>INTERFACE</th><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th></tr>
<tr><td>0</td><td>0</td><td>8080 family</td><td>A0</td><td>$\overline{RD}$</td><td>$\overline{WR}$</td><td>$\overline{CS}$</td></tr>
<tr><td>1</td><td>0</td><td>6800 family</td><td>A0</td><td>E</td><td>R/$\overline{W}$</td><td>$\overline{CS}$</td></tr>
</table></td></tr>
<tr><td>A0</td><td>8080 family interface.
<table>
<tr><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>FUNCTION</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Command write</td></tr>
</table>
6800 family interface
<table>
<tr><th>A0</th><th>R/$\overline{W}$</th><th>E</th><th>FUNCTION</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Command write</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$ or E</td><td>When the 8080 family interface is selected,this signal acts as the active-LOW read strobe.The SAP3305 series output buffers are enabled when this signal is active.
When the 6800 family interface is selected ,this signal acts as the sctive-HIGH enable clock.Data is read from or written to the SAP3305 series when this clock goes HIGH.</td></tr>
<tr><td>$\overline{WR}$ or R/$\overline{W}$</td><td>When the 8080 family interface is selected ,this signal acts as the active-LOW write strobe. The bus data is latched on the rising edge of this signal.
When the 6800 family isterface is selected,this signal acts as the read/write control signal.Data is read from the Sap3305 series if this signal is HIGH,and written to the SAP3305series if itis LOW.</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip select.This active-LOW input enables the SAP3305 series.It is usually connected to the output of an address decoder device that maps the SAP3305 series into the memory space of the controlling microprocessor.</td></tr>
<tr><td>$\overline{RES}$</td><td>This active-LOW input performs a hardware reset on the SAP3305 series.It is a Schmitt-trigger input for enhanced noise immunity;however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.</td></tr>
</table>

Note:

SEL1 should be tied directly to VDD or VSS to prevent noise. If noise does appear on SEL1,decouple it to ground using a capacitor placed as close to the pin as possible.

5.5.4 DISPLAY MEMORY CONTROL

The SAP3305 series can directly access static RAM and PROM.The designer may use a mixture of these two types of memory to achieve an optimum trade-off between low cost and low power consumption.

Table 7

SYMBOL	DESCRIPTION
VA0~VA15	16-bit display memory address . When acessing character generator RAM or ROM, VA0 to VA3,reflect the lower 4 bits of the SAP3305 series's row counter.
VD0~VD7	8-bit tristate display memory data bus. These pins are enabled when VR/W is LOW.
$\overline{\text{VWR}}$	Active-LOW display memory write control output.
$\overline{\text{VRD}}$	Active-LOW display memory read control output.
$\overline{\text{VCE}}$	Active-LOW static memory standby control signal. VCE can be used with CS.

5.5.5 LCD DRIVER SIGNALS

In order to provide effective low-power drive for LCD matrixes,the SAP3305 series can directly control both the X-and Y-drivers using an enable chain.

Table 8

SYMBOL	DESCRIPTION
XD0~XD3	4-bit X-driver(column drive)data outputs.Connect these outputs to the inputs of the X-driver chips.
XSCL	The fallng ede of XSCL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
XECL	The falling edge of XECL triggers the enable chain casade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
LP	LP latches the signal in the X-driver shift registers into the utput data latches.LP is a falling edge triggered signal .anf pulses once every fisplay line. Connect LP to the Y-drivers shift clock on modules.
WF	LCD panel AC drive output. The WF period is selected to be one of two values with SYSTEM ST command.
YSCL	The falling edge of YSCL latches the data on YD into the input shift resisters of the Y-drivers.YSCL is not used wth driver ICs with use LP as the Y-driver shift clock.
YD	YD is the data puoutput for the Y drivers.It is active during the last line of each frame,and is shifted through the Y drivers one by one (by YSCL),to scan the display's common connections.
YDIS	Power-down output signal.YDIS is HIGH while the display drive outputs are active. YDIS goes LOW one or two fames after the sleep command is written to the SAP3305 series.All Y-driver outputs are forced to an intermediate level (de-selecting the display segments)to blank the display. In order to implement power-down operation in the LCD unit,the LCD power drive supplies must also be disabled when the display is disabled by YDIS.

6 SPECIFICATIONS

6.1 Absolute maximum rating

Table 9

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	-0.3 to 7.0	V
V_{IN}	Input voltage range	-0.3 to VDD+0.3	V
P_D	Power dissipation	300	mW
T_{opg}	Operating temperature range	-20 to 75	°C
T_{stg}	Storage temperature range	-65 to 150	°C
T_{solder}	Soldering temperature (10 secnds).See note 1.	260	°C

Note:

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.
2. If the power supply has a high impedance, a large differential can occur between the input and supply voltages. Take appropriate care wth the power supply and the layout of the supply lines(see section 6.2)
3. All supply voltages are referenced to VSS= 0V.

6.2 DC characteristics

Table 10

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = −20°C to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{OH}	Register data retention voltage		2.0	-	6.0	V
I_{LI}	Input leakage current	V_I=V_{DD}.See note 5.	-	0.05	2.0	μA
I_{LO}	Output lrakage current	V_I=V_{DD}.See note 5.	-	0.10	5.0	μA
Iopr	Operating supply current	See note 4.	-	11	15	μA
I_Q	Quiescent supply current	Sleep mode, V_{OSC1}=$V_{\overline{CS}}$=$V_{\overline{RD}}$=V_{DD}	-	0.05	20.0	μA
f_{osc}	Oscillator frequency	Measured at crystal 47.5% duty cycle. See note 6.	1.0	-	10.0	MHz
f_{CL}	External clock frequency		1.0	-	10.0	MHz
R_f	oscillator feedback resistance		0.5	1.0	3.0	MΩ
TTL						
V_{IHT}	HIGH-level input voltage	See note 1.	0.5V_{DD}	-	V_{DD}	V
V_{ILT}	LOW-level input voltage	See note 1.	Vss	-	0.2V_{DD}	V
V_{OHT}	HIGH-level output voltage	I_{OH}=-5.0mA. See note 1.	2.4	-	-	V
V_{OLT}	LOW-level output voltage	I_{OL}=5.0mA. See note 1.	-	-	Vss+0.4	V
CMOS						
V_{IHC}	HIGH-level input voltage	See note 2.	0.8V_{DD}	-	V_{DD}	V
V_{ICT}	LOW-level input voltage	See note 2.	Vss	-	0.2V_{DD}	V
V_{OHC}	HIGH-level output voltage	I_{OH}=-2.0mA. See note 2.	V_{DD}-0.4	-	-	V
V_{OLC}	LOW-level output voltage	I_{OL}=1.6mA. See note 2.	-	-	Vss+0.4	V
Open-drain						
V_{OLN}	LOW-level output voltage	I_{OL}=6.0mA.	-	-	Vss+0.4	V
Schmitt-trigger						
V_{T+}	Rising-edge threshold volage	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
V_{T-}	Falling-edge threshold voltage	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Note:

1. D0 to D7,A0,$\overline{CS}$,$\overline{RD}$,$\overline{WR}$,VD0 to VD7,VA0 to VA15,$\overline{VRD}$,$\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1 is COMS-level inputs.YD,XD0 to XD3,XSCL,LP,WF,YDIS are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200ms, Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. fosc= 10 MHz, no load (no display memory),internal character generator,256 x 200 pixel display. The operating supply current can be reduced by approximately 1mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance,the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.

6. Because the oscilllator circuit input bias current is in the order of mA, design the printed circuit board so as to reduce leakage currents.

Table 11

V_{DD} = 2.7 V to 4.5V; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = -20°C to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		2.7	3.5	4.5	V
V_{OH}	LOW level input voltage		2.0	-	6.0	V
I_{LI}	HIGH level input voltage	V_I=V_{DD}.See note 5.	-	0.05	2.0	mA
I_{LO}	LOW level output voltage	V_I=V_{DD}.See note 5.	-	0.10	5.0	mA
Iopr	HIGH level output voltage	V_{DD}=3.5V.See note 4	-	3.5	-	mA
		See note 4.	-	-	7.0	
I_Q	Standby current at V_{DD}=5 volts	Sleep mode, V_{OSC1}=$V_{\overline{CS}}$=$V_{\overline{RD}}$=V_{DD}	-	0.05	20.0	mA
f_{osc}	Operating current at V_{DD}=5 volts	Measured at crystal 47.5% duty cycle. See note 6.	1.0	-	8.0	MHz
f_{CL}	Operating frequency		1.0	-	8.0	MHz
R_f	Internal pull-up resistor of input pins		0.7	-	3.0	MW
TTL						
V_{IHT}	Supply voltage	See note 1.	0.5V_{DD}	-	V_{DD}	V
V_{ILT}	LOW level input voltage	See note 1.	Vss	-	0.2V_{DD}	V
V_{OHT}	Supply voltage	I_{OH}=-3.0mA. See note 1.	2.4	-	-	V
V_{OLT}	LOW level input voltage	I_{OL}=3.0mA. See note 1.	-	-	Vss+0.4	V
CMOS						
V_{IHC}	Supply voltage	See note 2.	0.8V_{DD}	-	V_{DD}	V
V_{ICT}	LOW level input voltage	See note 2.	Vss	-	0.2V_{DD}	V
V_{OHC}	HIGH level input voltage	I_{OH}=-2.0mA. See note 2.	V_{DD}-0.4	-	-	V
V_{OLC}	HIGH level input voltage	I_{OL}=1.6mA. See note 2.	-	-	Vss+0.4	V
Open-drain						
V_{OLN}	Supply voltage	I_{OL}=6.0mA.	-	-	Vss+0.4	V
Schmitt-trigger						
V_{T+}	Supply voltage	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
V_{T-}	LOW level input voltage	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Note:

1. D0 to D7,A0,$\overline{CS}$,$\overline{RD}$,$\overline{WR}$,VD0 to VD7,VA0 to VA15,$\overline{VRD}$,$\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
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3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200μs, Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.

4. fosc= 10 MHz, no load (no display memory),internal character generator,256 x 200 pixel display. The operating supply current can be reduced by approximately 1mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance,the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscilllator circuit input bias current is in the order of μA, design the printed circuit board so as to reduce leakage currents.

6.3 Timing Diagrams

6.3.1 8080 FAMILY INTERFACE TIMING

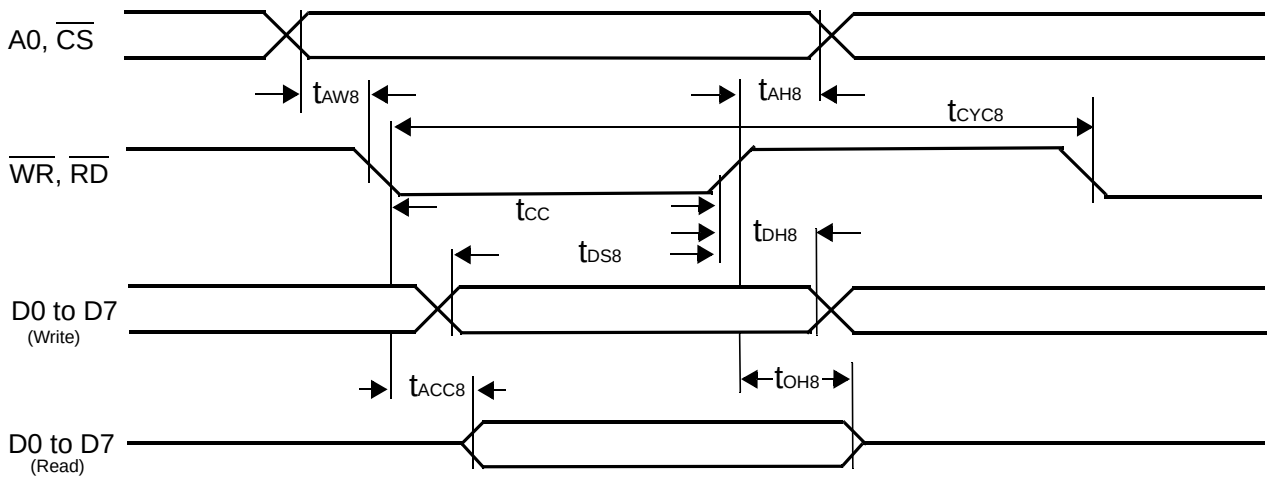


Fig.4 8080 family interface timing

Table 12

V_{SS} = 0 V; T_{amb} = -20 °C to +75°C

SIGNAL	SYMBOL	PARAMETER	VDD=4.5V TO 5.5V		VDD=2.7V TO 4.5V		UNIT	CONDITION
			MIN.	MAX.	MIN.	MAX.		
A0,$\overline{CS}$	t_{AH8}	Address hold time	10	-	10	-	ns	CL=100pF
	t_{AW8}	Address set-up time	0	-	0	-	ns	
$\overline{WR}$,$\overline{RD}$	t_{CYC8}	System cycle time	See note.	-	See note.	-	ns	
	t_{CC}	Strobe pulsewidth	120	-	120	-	ns	
D0 to D7	t_{DS8}	Data set-up time	120	-	120	-	ns	
	t_{DH8}	Data hold time	5	-	5	-	ns	
	t_{ACC8}	$\overline{RD}$ access time	-	50	-	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

Note:

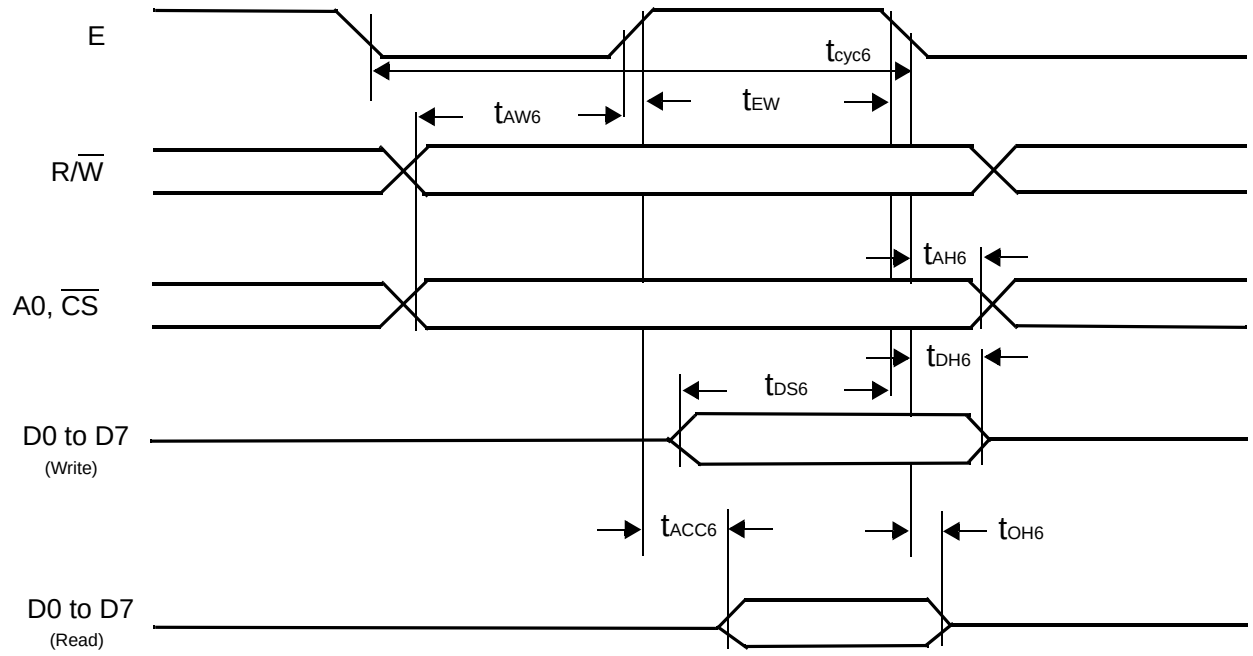
For memory control and system control commands:

t_{CYC8} =2tc + t_{CC} +t_{CEA} +75 > t_{ACV} +245

For all other commands:

t_{CYC8} =4tc + t_{CC} +t_{CE} +30

6.3.2 6800 FAMILY INTERFACE TIMING



Note: t_{cyc6} indicates the interval during which CS is LOW and E is HIGH

Fig.5 6800 family interface timing

Table 13

V_{SS} = 0 V; T_{amb} = -20 °C to +70°C

SIGNAL	SYMBOL	PARAMETER	VDD=4.5V TO 5.5V		VDD=2.7V TO 4.5V		UNIT	CONDITION
			MIN.	MAX.	MIN.	MAX.		
A0,CS,R/W	t_{CYC6}	System cycle time	See note.	-	See note.	-	ns	CL=100pF
	t_{AW6}	Address set-up time	0	-	10	-	ns	
	t_{AH6}	Address hold time	0	-	0	-	ns	
E	t_{EW}	Enable pulsewidth	120	-	150	-	ns	
D0 to D7	t_{DS6}	Data set-up time	100	-	120	-	ns	
	t_{DH6}	Data hold time	0	-	0	-	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	-	85	-	130	ns	

Note:

For memory control and system control commands:

$t_{CYC8} = 2tc + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4tc + t_{EW} + 30$

6.3.3 DISPLAY MEMORY READ TIMING

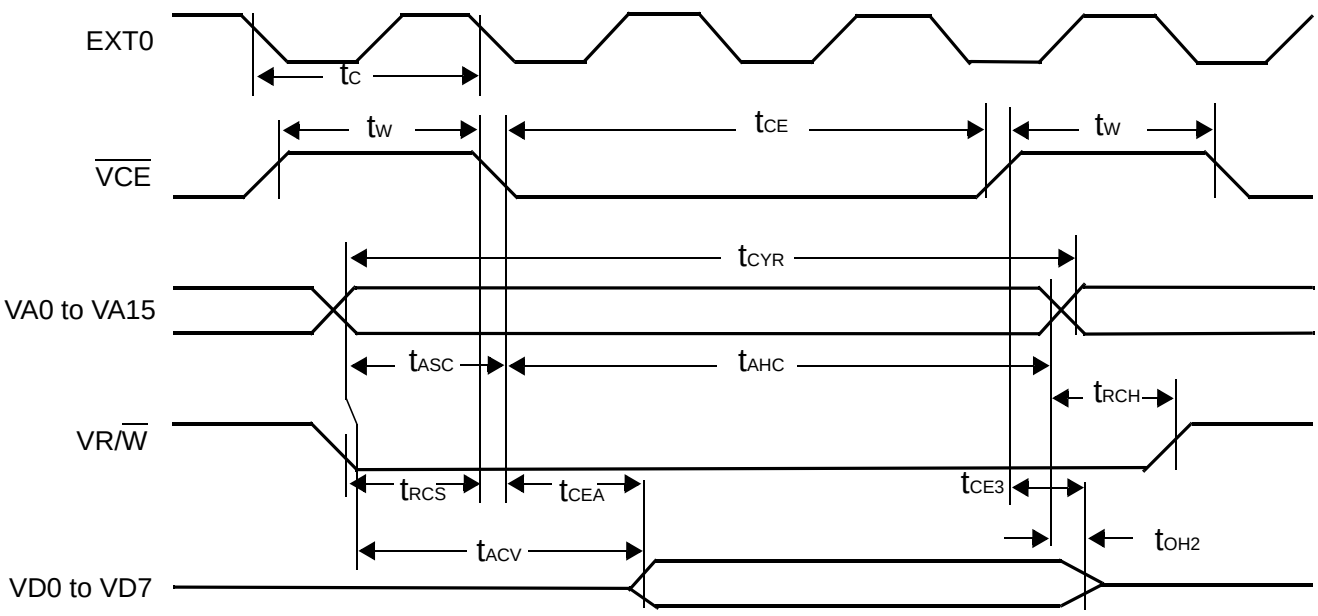


Fig.6 Display memory read timing

Table 14

V_{SS} = 0 V; T_{amb} = -20 °C to +75°C

SIGNAL	SYMBOL	PARAMETER	VDD=4.5V TO 5.5V		VDD=2.7V TO 4.5V		UNIT	CONDITION
			MIN.	MAX.	MIN.	MAX.		
EXT0	t_C	Clock period	100	-	125	-	ns	CL=100pF
VCE	t_W	$\overline{VCE}$ HIGH-level pulsewidth	t_C-50	-	t_C-50	-	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulsewidth	$2t_C$-30	-	$2t_C$-30	-	ns	
VA0 to VA15	t_{CYR}	Read cycle time	$3t_C$	-	$3t_C$	-	ns	
	t_{ASC}	Adress setup time to falling edge of $\overline{VCE}$	t_C-70	-	t_C-100	-	ns	
	t_{AHC}	Adress hold time from falling edge of $\overline{VCE}$	2_C-30	-	$2t_C$-40	-	ns	
VRD	t_{RCS}	Red cycle setup time to falling edge of $\overline{VCE}$	t_C-45	-	t_C-60	-	ns	
	t_{RCH}	Red cycle hold time from rising edge of $\overline{VCE}$	$0.5t_C$	-	$0.5t_C$	-	ns	
VD0 to VD7	t_{ACV}	Address access time	-	$3t_C$-100	-	$3t_C$-115	ns	
	t_{CEA}	$\overline{VCE}$ access time	-	$2t_C$-80	-	$2t_C$-90	ns	
	t_{OH2}	Output data hold time	0	-	0	-	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	-	0	-	ns	

6.3.4 DISPLAY MEMORY WRITE TIMING

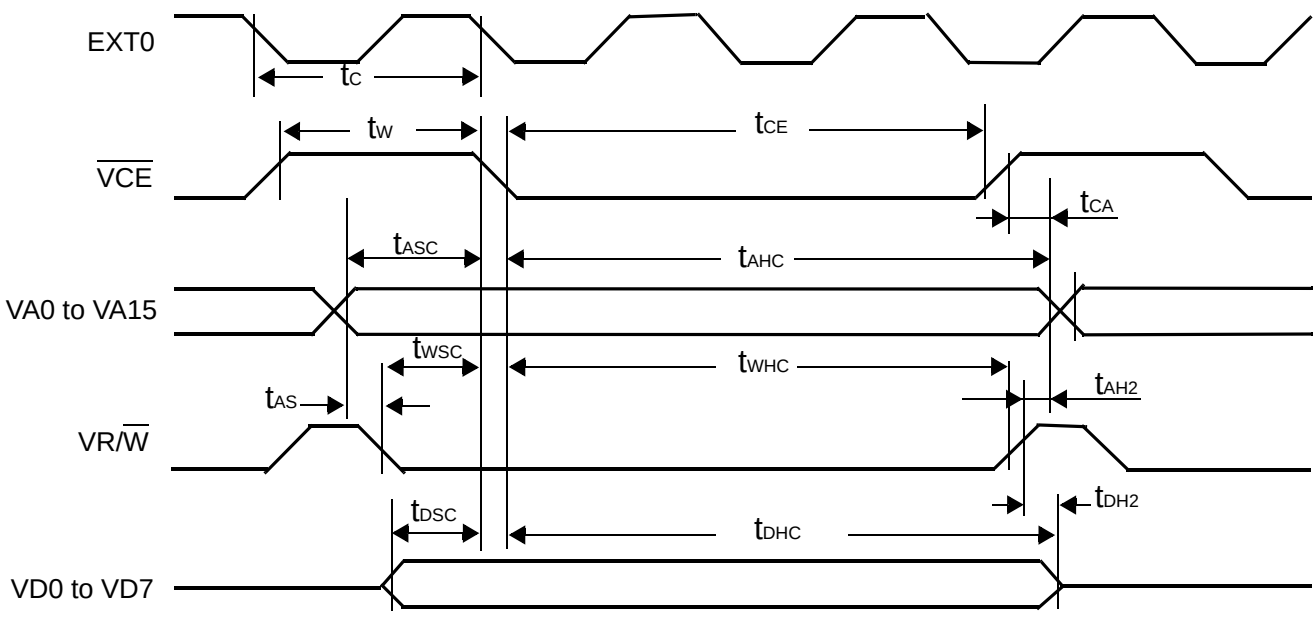


Fig.7 Display memory write timing

Table 15

V_{SS} = 0 V; T_{amb} = -20 °C to +75°C

SIGNAL	SYMBOL	PARAMETER	VDD=4.5V TO 5.5V		VDD=2.7V TO 4.5V		UNIT	CONDITION
			MIN.	MAX.	MIN.	MAX.		
EXT0	t_C	Clock period	100	-	125	-	ns	CL=100pF
VCE	t_W	$\overline{VCE}$ HIGH-level pulsewidth	t_C-50	-	t_C-50	-	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulsewidth	$2t_C$-30	-	$2t_C$-30	-	ns	
VA0 to VA15	t_{CYW}	Write cycle time	$3t_C$	-	$3t_C$	-	ns	
	t_{ASC}	Adress setup time to falling edge of $\overline{VCE}$	t_C-70	-	t_C-110	-	ns	
	t_{AHC}	Adress hold time from falling edge of $\overline{VCE}$	$2t_C$-30	-	$2t_C$-40	-	ns	
	t_{CA}	Adress hold time from rising edge of $\overline{VCE}$	0	-	0	-	ns	
	t_{AS}	Adress setup time to falling edge of $\overline{VWR}$	0	-	0	-	ns	
	t_{AH2}	Adress hold time from rising edge of $\overline{VWR}$	10	-	10	-	ns	
VWR	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	t_C-80	-	t_C-115	-	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	$2t_C$-20	-	$2t_C$-20	-	ns	
VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	t_C-85	-	t_C-125	-	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	$2t_C$-30	-	$2t_C$-30	-	ns	
	t_{DH2}	Data hold time from rising edge of $\overline{VCE}$	5	50	5	50	ns	

Note:

VD0 to VD7 are latching input/outputs. While the bus is high impedance , VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

6.3.5 SLEEP IN COMMAND TIMING

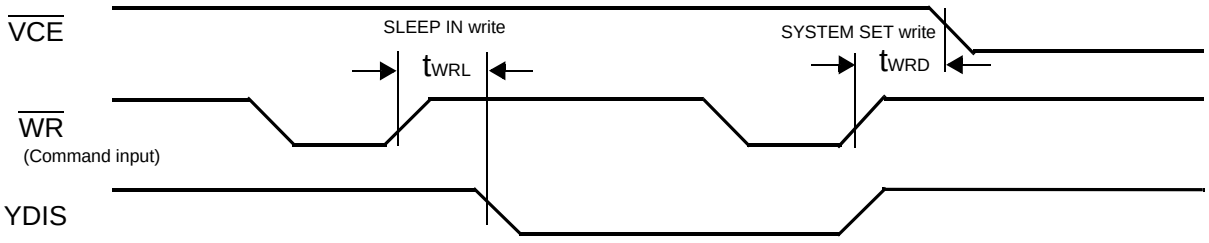


Fig.8 SLEEP IN command timing

Table 16

V_{SS} = 0 V; T_{amb} = -20 °C to +75°C

Signal	Symbol	Parameter	VDD=4.5V to 5.5V		VDD=2.7V to 4.5V		Unit	Condition
			MIN.	MAX.	MIN.	MAX.		
WR	t_{WRD}	$\overline{VCE}$ falling-edge delay time	See note1	-	See note1	-	ns	CL=100pF
	t_{WRL}	YDIS falling-edge delay time	-	See note2	-	See note2	ns	

Note:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C$ x [TC/R] x [L/F] + 70.

6.3.6 EXTERNAL OSCILLATOR TIMING

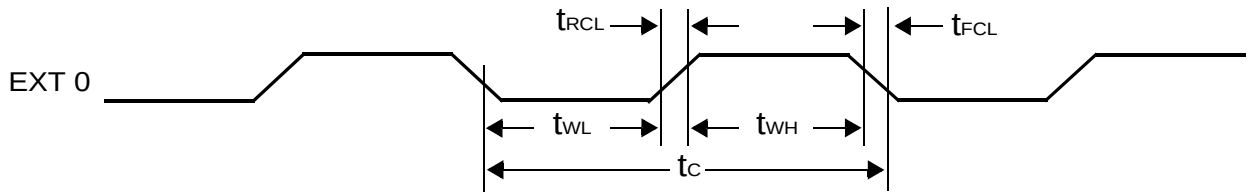


Fig.9 External oscillator signal timing

Table 17

V_{SS} = 0 V; T_{amb} = -20 °C to +75°C

Signal	symbol	parameter	VDD=4.5V to 5.5V		VDD=2.7V to 4.5V		Unit	Condition
			MIN.	MAX.	MIN.	MAX.		
EXTϕ0	t_{RCL}	External clock rise time	-	15	-	15	ns	
	t_{FCL}	External clock fall time	-	15	-	15	ns	
	t_{WH}	External clock HIGH-level pulsewidth	See note1	See note2	See note1	See note2	ns	
	t_{WL}	External clock LOW-level pulsewidth	See note1	See note2	See note1	See note2	ns	
	t_C	External clock period	100	-	125	-	ns	

Note:

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

6.3.7 LCD OUTPUT TIMING

The following characteristics are for a 1/64 duty cycle.

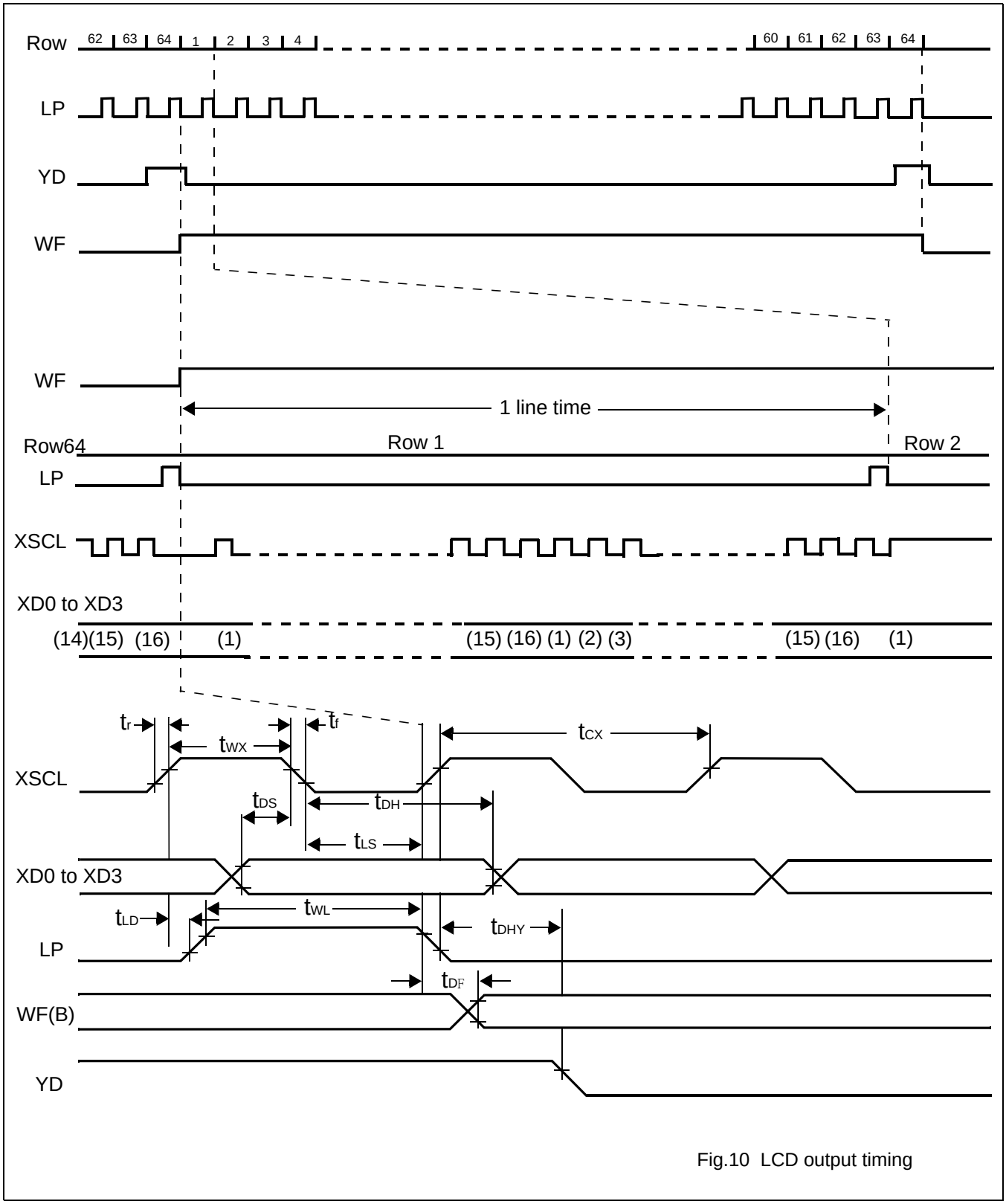


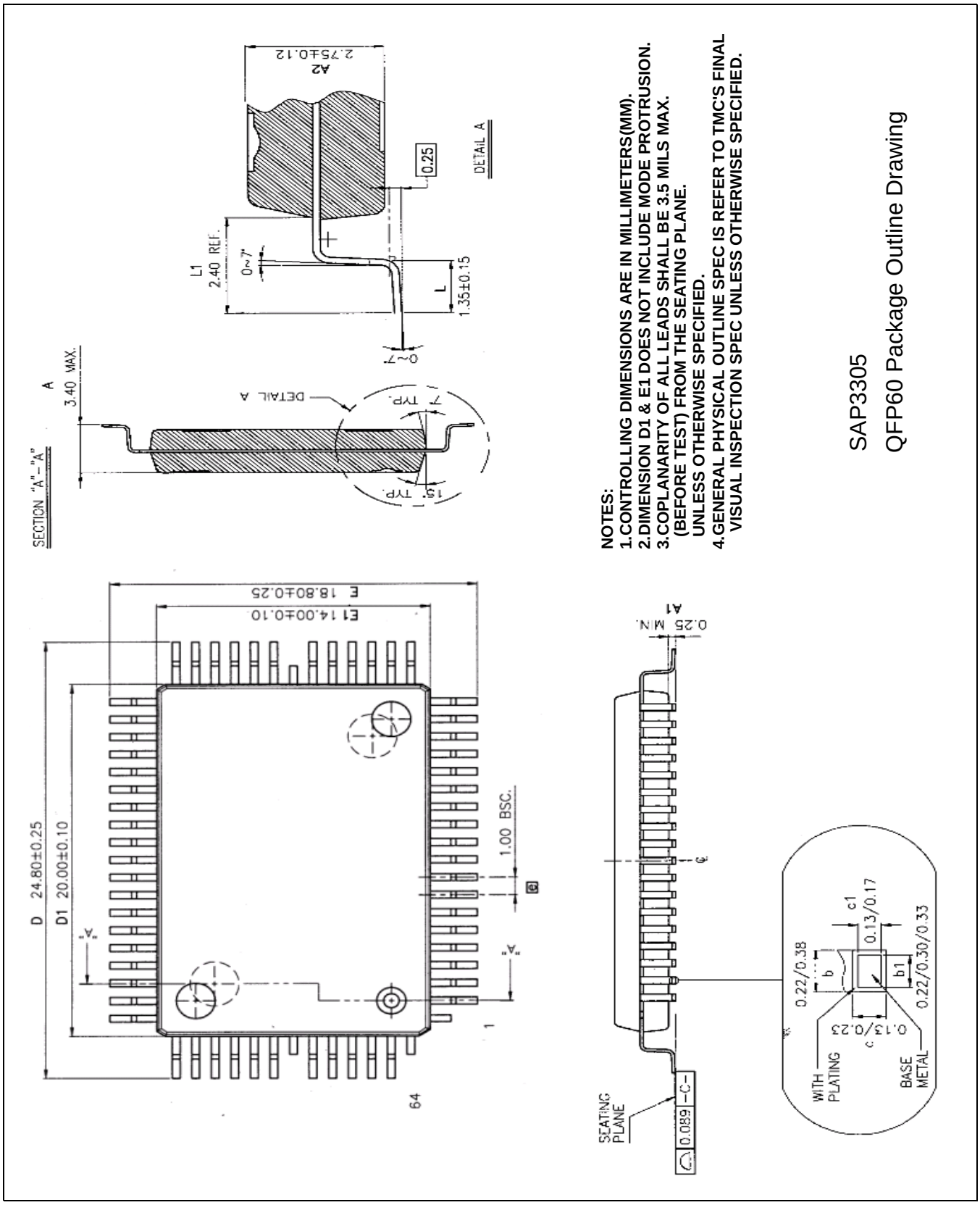
Fig.10 LCD output timing

Table 18

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -20 °C to +75°C

SIGNAL	SYMBOL	PARAMETER	VDD=4.5V TO 5.5V		VDD=2.7V TO 4.5V		UNIT	CONDITION
			MIN.	MAX.	MIN.	MAX.		
	t_r	Rising time	-	30	-	40	ns	CL=100pF
	t_f	Fall time	-	30	-	40	ns	
XSCL	t_{CX}	Shift clock pulsewidth	$4t_C$	-	$4t_C$	-	ns	
	t_{WX}	SCL clock pulsewidth	$2t_C$-60	-	$2t_C$-60	-	ns	
XD0 to XD3	t_{DH}	X data hld time	$2t_C$-50	-	$2t_C$-50	-	ns	
	t_{DS}	X data setup time	$2t_C$-100	-	$2t_C$-105	-	ns	
LP	t_{LS}	Latch data setup time	$2t_C$-50	-	$2t_C$-50	-	ns	
	t_{WL}	LP pulsewidth	$4t_C$-80	-	$4t_C$-120	-	ns	
	t_{LD}	LP delay time from XSCL	0	-	0	-	ns	
WF	t_{DF}	Permitted WF delay		50		50	ns	
YD	t_{DHY}	Y data hold time	$2t_C$-20	-	$2t_C$-20	-	ns	

7 PACKAGE INFORMATION



8 INSTRUCTION SET

8.1 The command set

Table 19

CLASS	COMMAND	CODE											HEX	COMMAND DESCRIPTION	COMMAND READ PARAMETERS	
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			NO.OF BYTES	SECT-ION
System control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	8.2.1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enable standby mode	0	8.2.2
Display control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	8.3.1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	8.3.2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	8.3.3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	8.3.6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C~ 4F	Set direction of crsor movement	0	8.3.4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	8.3.7
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	8.3.5
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	8.4.1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	8.4.2
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	-	8.5.1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	-	8.5.2

Note:

1. In general,the internal registers of the SAP3305 series are modified as each command parameter is input.However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters(where two bytes are treated as 1 data item) are handled as follows:
   a) CSRW,CSRR:Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
   b) SYSTEM SET,SCROLL,CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.
2. APL and APH are 2-byte paramters, but rae treated as two 1-byte parameters.

8.2 System control commands

8.2.1 SYSTEM SET

Initializes the device, sets the window sizes,and selects the LCD interface format.Since this command sets the basic operating parameters of the SAP3305 series,an incorrect SYSTEM SET command may cause other commands to operate incorrectly.

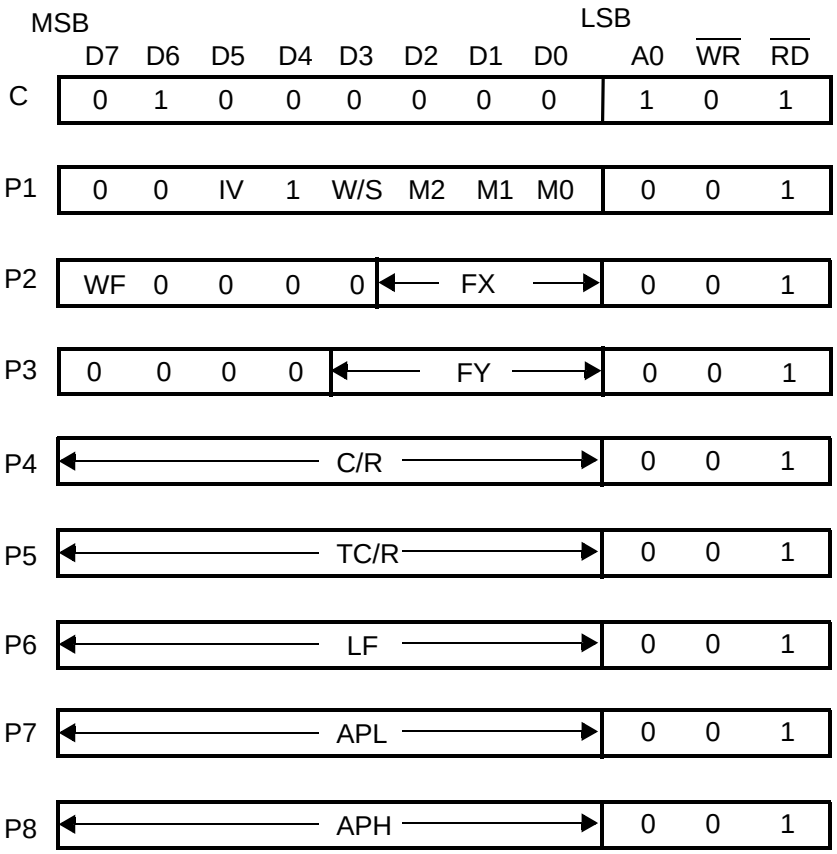


Fig.11 SYSTEM SET instruction

8.2.1.1 C

This control byte performs the following:

1. Resets the interal timing generator
2. Disables the display
3. Cancels sleep mode

Parameters following P1 are not needed if only can sleep mode.

8.2.1.2 M0

Selects the internal or external character generator ROM.The internal character generator ROM contains 160, 5x7 pixel characters ,as shown in figure 70. These characters are fixed at fabrication by the metallization mask. The external character generator ROM,on the other hand ,can contain up to 256 user-defined characters.

M0=0: Internal CG ROM

M0=1: External CG ROM

Note that if the CG ROM address space overlaps the display memory address space,that portion of the display memory cannot be written to.

8.2.1.3 M1

Selects the m for user-definable characters. The CG RAM codes select one of the 64 codes shoxn in figure 61.

M1=0: NNo D6 correction.

The CG RAM1 and CG RAM2

address spaces are not contiguous ,the CG RAM1 address space is treated as character generator RAM,and the CG RAM2 address space is treated as character generator ROM.

M1=1:D6 correction.

The CG RAM1 and CG RAM2 address spaces are contiguout and both treated as character generator RAM.

8.2.1.4 M2

Selects the height of the chaacter bitmaps.Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using thr SAP3305 series graphics mode to reposition them.

M2=0:8-pixel character height (2716 or equivalent ROM)

M2=1:16-pixel character height (2732 or equivalent ROM)

8.2.1.5 W/S

Selects the LCD drive method.

W/S=0:Single-panel drive

W/S=1:Dual-panel drive

)

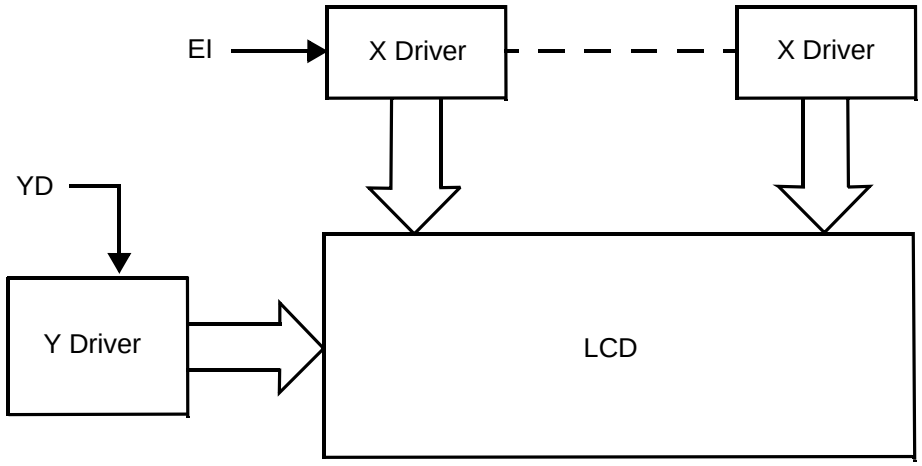


Fig.12 Single-panel display

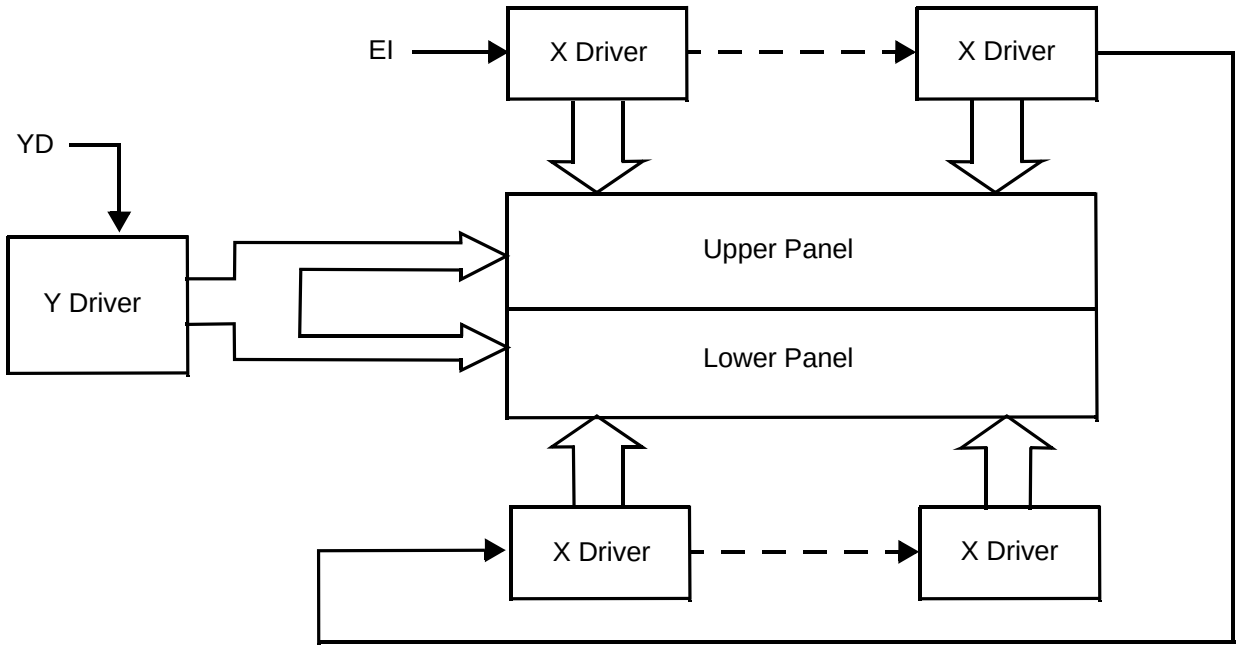


Fig.13 Above and below two-panel display

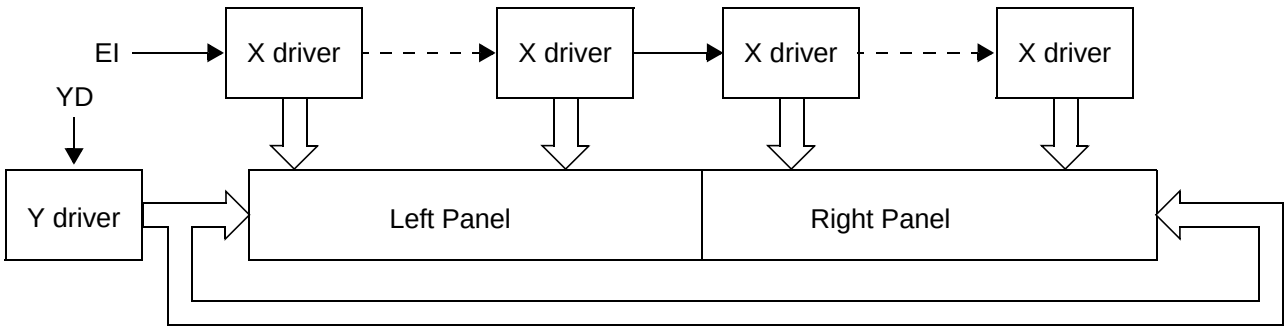


Fig.14 Left-and-right two -panel display

Note

There are no AVANT LCD units in the configuration shown in Figure 14.

Table 20 LCD parameters

PARAMETER	W/S=0		W/S=1	
	IV=1	IV=0	IV=1	IV=0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R(See note 1)	TC/R	TC/R
LF	LF	LF	LF	LF
SL1	00H to LF	00H to LF+1 (See note 2)	(LF)/2	(LF)/2
SL2	00H to LF	00H to LF+1 (See note 2)	(LF)/2	(LF)/2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth screen block
Cursor movement range	Continuous movement over whole screen		Above-and below configuaration: continuous movement over whole screen	

Note:

1. See table 45 for further details on setting the C/R and TC/R parameters when using the HDOT SCR command.
2. The value of SL when IV=0 is equal to the value of SL when IV=1,plus one.

8.2.1.6 IV

Screen origin compensation for inverse display.IV is usually set to 1.The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer.However,inverted characters at the top or left of the scteen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either aove or to the left of these characters.The IV flag causes the SAPP3305 series to offset the text screen against the graphics back layer by one vertical pixel.Use the horizontal pixel scroll function (HDOTSCR)to shift the text screen 1 to 7pixels to the right.Allcharacters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters.See Section 9.5 for information on scrolling.

IV=0:Screen top-line correction

IV=1:No screen top-line correction

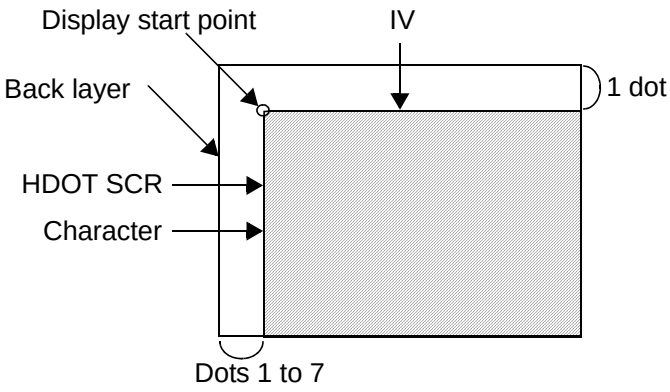


Fig.15 IV and HDOT SCR adjustment

8.2.1.7 FX

Define the horizontal charactersize. The character width in pixels is equal to FX+1,where FX can range from 00 to 07Hinclusive.If data bit 3 is set (FX is in the range 08 to 0FH)and an 8-pixel font is used ,a spac is inserted between characters.

Table 21 Horizontal character size selection

FX					[FX] character width (pixels)
HEX	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8

Since the SAP3305 series handles display data in 8-bit units, characters larger than 8-pixels wide must be formed from 8-pixel segments. As Figure 16 shows,the remainder of the second eight bits are not displayed . This also applies to the second screen layer.In graphics mode,the normal character field is also eight pixels.If a wider character field is used ,any remainder in the second eight bits is not displayed.

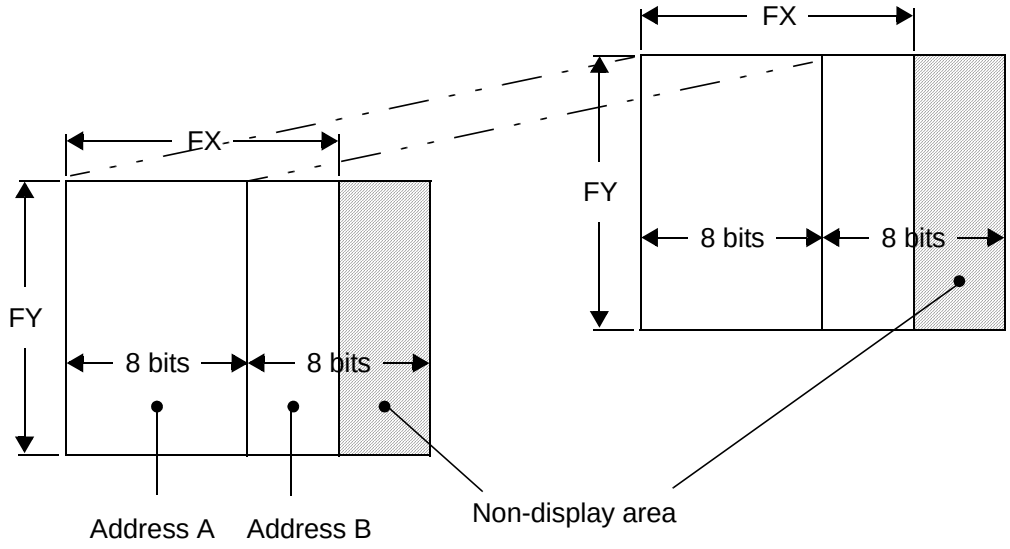


Fig.16 FX and FY display address

8.2.1.8 WF

Select the AC frame drive waveform period.WF is usually set to 1.

WF=0:16-line ACdrive

WF=1:wo-frame ACdrive

In two-frame AC drive,the WF period is twice the frame period.In 16-line AC drive gives a more readable display,horizontal lines may appear when using high LCD drive voltage or at high viewing angles.

8.2.1.9 FY

Sets the vertical character size .The height in pixels is equal to FY+1.FY can range from 00 to 0FH inclusive.Set FY to zero (vertical size equal one)when in graphics mode.

Table 22 Vertical character size selection

FY					[FX] CHARACTER HEIGHT (PIXELS)
HEX	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8
↓	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

8.2.1.10 C/R

Set the address range covered by one dispaly line ,that is,the nimber of characters less one ,multiplied by the number of horizontal bytes per character.C/R can range from 0 to 239.For example ,if the characterwidth is 10 pixels,then the address range is equal to twice the number of characters,less 2.See Section16.1.1 for the calculation of C/R.[C/R] cannot be set to a calue greater than the address range .It can,however,be set smaller than the address range ,in which case the excess display area is blank.The number of excess ixels musts not exceed 64.

Table 23 Display line address range

C/R									[C/R] BYTES PER DISPLAY LINE
HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	1	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

8.2.1.11 TC/R

Sets the length,including horizontal blanking,of one line .The line length is equal to TC/R+1,where TC/R can range from 0 to 255.TC/R must be greater than or equal to C/R+4.Provided this condition is satisfied,[TC/R]can be set accroding to the equation given in section 16.1.1 in order to hold the frame period constant and minimize jitter for any given main oscillator frequency,fosc.

Table 24 Linee length selection

TC/R									[TC/R] LINE LENGTH (BYTES)
HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	1	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	83
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

8.2.1.12 L/F

Set the height,in lines,of a frame.The height in lines is equal to L/F+1,where L/F can range from 0 to 255

Table 25 Frane height selection

L/F									[L/F] LINE PER FRAME
HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	1	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

If W/S is set to 1,selecting two-screen display,the number of lines must be even and L/F must, therefore,be an odd number.

8.2.1.13 AP

Defines the horizontal address range of the virtual screen.APL is the least significant byte of the address.

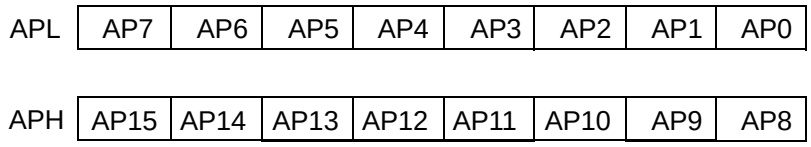


Fig.17 AP parameters

Table 26 Horizontal address range

HEX CODE				[AP] ADDRESSES
APH		APL		PER LINE
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	E	$2^{16} - 2$
F	F	F	F	$2^{16} - 1$

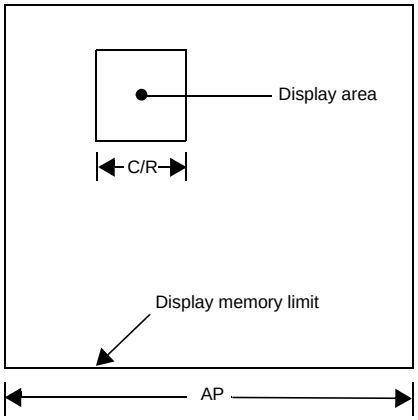


Fig.18 AP and C/R relationship

8.2.2 SLEEP IN

Places the system in standby mode.This command has no parameter bytes.At least one blank frame after receiving this command, the SAP3305 halts all internal operations ,including the oscillator,and enters the sleep stste.Blank data is sent to the X-dricer,and the Y-drivershave their bias supplies turned off by the YDIS signal to disable the Y-drivers guards against any spurious display.The internal registers of the SAP3306series maintain their values during the sleep state.The display memory control pins maintain their logic level to ensure that the display memory is not corrupted.The SAP3305 series can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter . The DISP ON command should be sent next to enable the display.

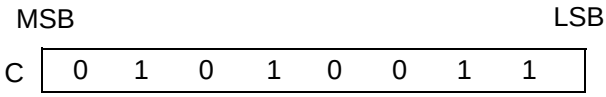


Fig.19 SLEEP IN instruction

1. The YDIS signal LOW between one and two frames after the SLEEP IN command is received.Since YDIS forces all dispaly driver outputs to go to the deselected output voltage,YDIS can be used as a power-down signal for the LCD unit.This can be done by having YDIS turn off the relatively high-power LCD drive supplies at the same time as it blanks the display.
2. Since all internal clocks in the SAP3305 series are halted while in the sleep state , a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on
3. Note that, although the bus lines become high impedance in the sleep state, pull-up or pull-down resistors on the bus will force these lines to a known state.

8.3 Display control commands

8.3.1 DISP ON/OFF

Turns the whole display on or off.The single-byte patameter enables and disables the cursor and layered screens,and sets the cursor and screen flash rates.The cursor can be set to flash over one character or over a whole line.

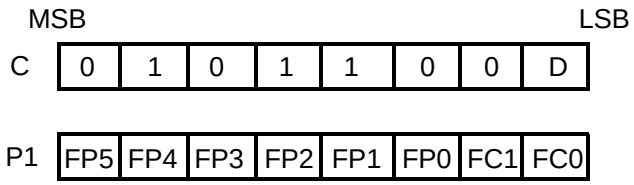


Fig.20 DISP ON/OFF parameters

8.3.1.1 D

Turns the display ON or OFF. The D bit takes precedance over the FP bits in the parameter.

D=0:Display OFF

D=1:Display ON

8.3.1.2 FC

Enables/disables the cursor and sets the flash rate. The cursor flashes wth a 70% duty cycle(ON/OFF).

Table 27 Cursor flash rate selection

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at f_{FR}/32Hz (approx. 2Hz)
1	1		Flash at f_{FR}/64Hz (approx. 1Hz)

Note:

As the MWRITE command always enables the cursor.the cursor position can be chcked even when performing consecutive write to display memory while the cursor is flashing.

8.3.1.3 FP

Each pair of bits in FP sets the attributes of one screen block, as follows.

The display attributes are as follows:

Table 28 Screen block attribute selection

FP1	FP0	First screen block(SAD1)	
FP3	FP2	Second screen block(SAD2，SAD4) See note.	
FP5	FP4	Third screen block(SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at f_{FR}/32Hz (approx. 2Hz)
1	1		Flash at f_{FR}/4Hz (approx. 1Hz)

Note:

If SAD4 is enabled by setting W/S to 1,FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently.

8.3.2 SCROLL

8.3.2.1 C

Sets the scroll start address anf the number of lines per scroll block. Parameters P1to P10 can be omitted if not required.The parameters must be entered sequentially as shown in Figure 11.

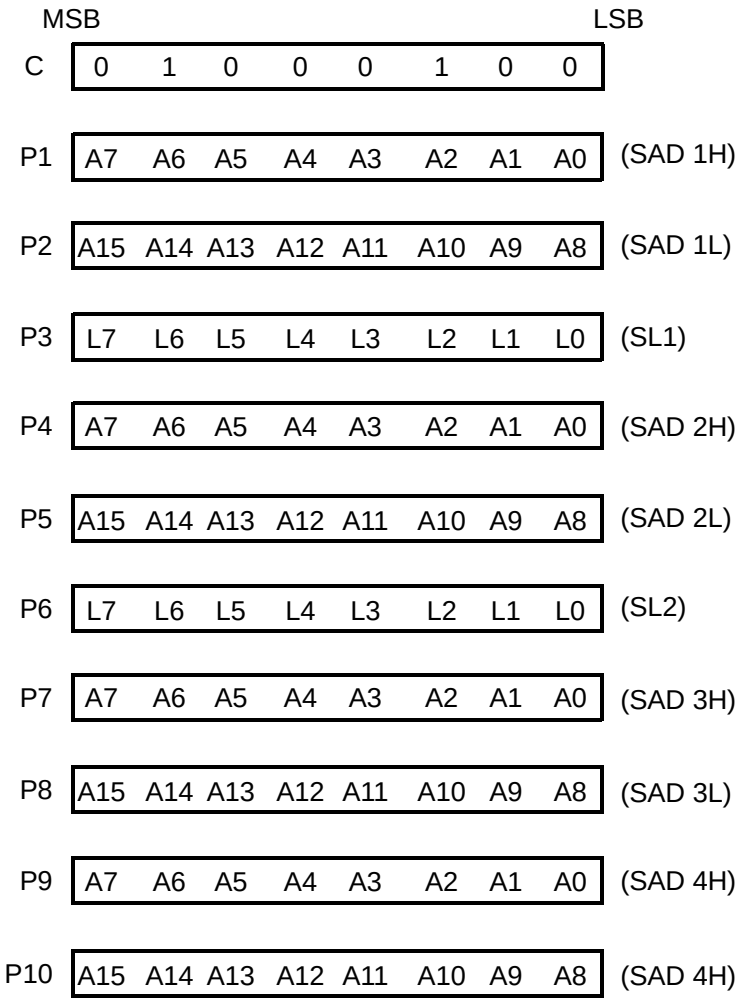


Fig.21 SCROLL instruction parameters

Note:

Set parameters P9 and P10 only if both two-screen drive (W/S=1) and two-layer configuration are selected.SAD4 is the fourth screen block display start address.

Table 29 Screen block start address selection

SL1,SL2									[SL] SCREEN LINE
HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	1	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

8.3.2.2 SL1,SL2

SL1 and SL2 set the number of lines per scrolling screen. The number of lines is SL1or SL2 plus one.The relationship between SAD,SL and the display mode is described below.

Table 30 Text display mode

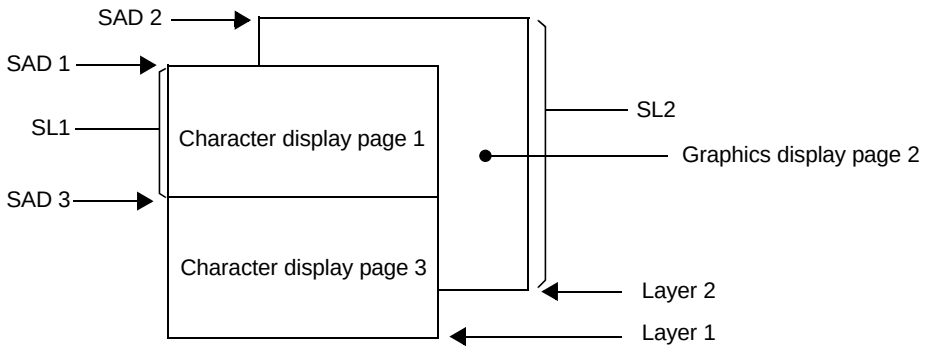
W/S	Screen	First Layer	Second Layer
0	First screen block	SAD1	SAD2
	Second screen block	SL1	SL2
	Third screen block(partitioned screen)	SAD3(see note 1) Set both SL1 and SL2 to L/F+1 if not using a partitioned screen	
			

Fig.22 Screen configuration example

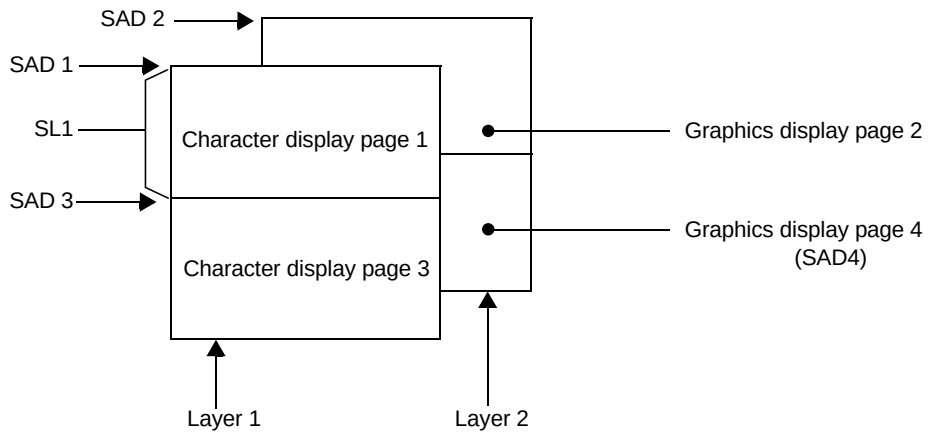
<table>
<tr><th>W/S</th><th>Screen</th><th>First Layer</th><th>Second Layer</th></tr>
<tr><td rowspan="4">1</td><td>Upper screen</td><td>SAD1
SL1</td><td>SAD2
SL2</td></tr>
<tr><td>Lower screen</td><td>SAD3
(see note 2)</td><td>SAD4
(see note 2)</td></tr>
<tr><td colspan="3">Set both SL1 and SL2 to (L/F) /2 +1).</td></tr>
<tr><td colspan="3"> 

Fig.23 Screen configuration example</td></tr>
</table>

Note:

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of line (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F,they do not have to be set in this mode.

Table 31 Graphics display mode

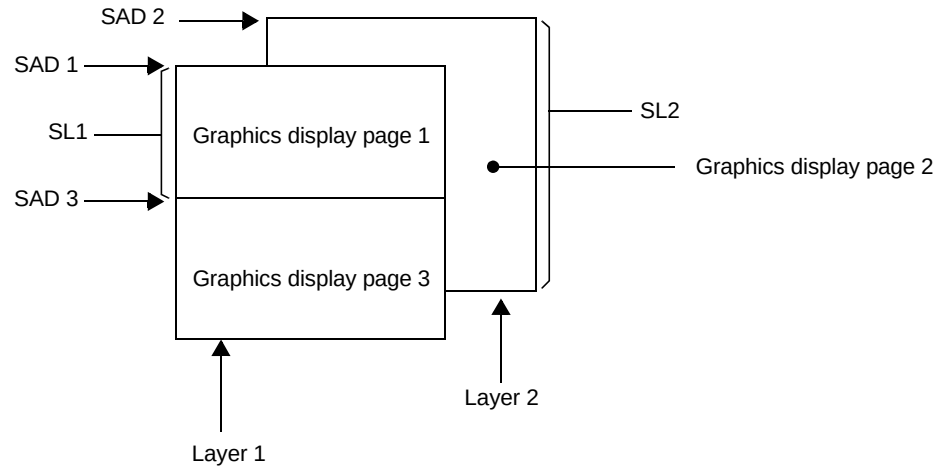
<table>
<tr><th>W/S</th><th>Screen</th><th>First Layer</th><th>Second Layer</th><th>Third Layer</th></tr>
<tr><td rowspan="3">0</td><td>Two-layer composition</td><td>SAD1
SL1</td><td>SAD2
SL2</td><td>-</td></tr>
<tr><td>Upper screen</td><td colspan="2">SAD3(see note 3)
Set both SL1 and SL2 to L/F+1
if not using a partitioned screen</td><td>-</td></tr>
<tr><td colspan="4"> 

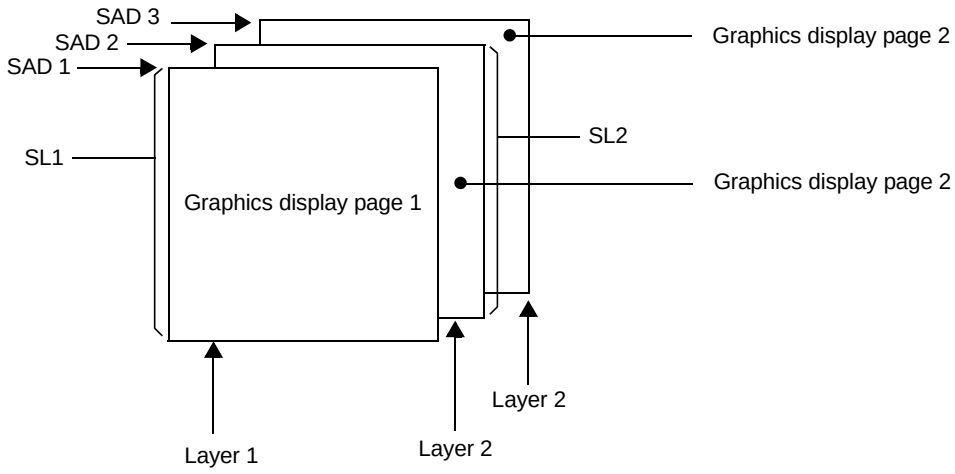
Fig.24 Screen configuration example</td></tr>
<tr><td rowspan="2">1</td><td>Three-layer configuration</td><td>SAD1
SL1= L/F+1</td><td>SAD2
SL2= L/F+1</td><td>SAD3
-</td></tr>
<tr><td colspan="4"> 

Fig.25 Screen configuration example</td></tr>
</table>

Table 32 Graphics display mode(continued)

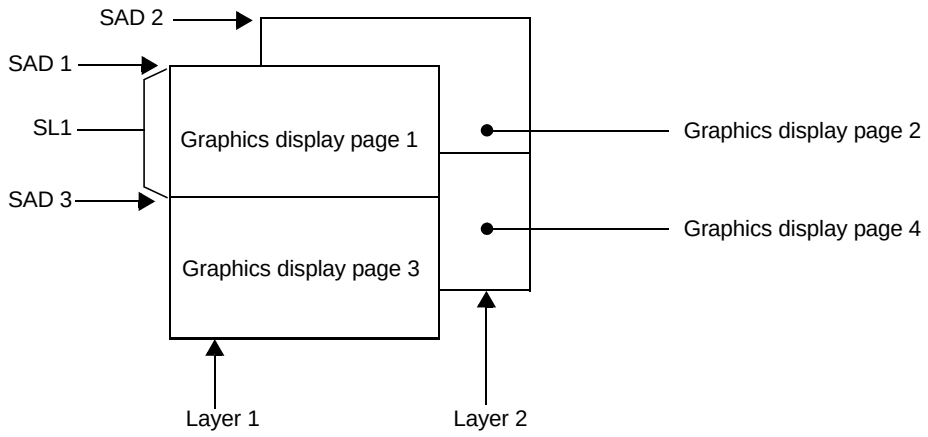
W/S	Screen	First Layer	Second Layer	Third Layer
1	Upper screen	SAD1 SL1	SAD2 SL2	-
	Lower screen	SAD3 (see note 2)	SAD4 (see note 2)	-
	Set both SL1 and SL2 to((L/F)/2+1)			
				

Fig.26 Screen configuration example(See note 3)

Note:

1. SAD3 has the same value as either SAD1or SAD2,whichever has the least number of lines(set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F,they do not have to be set.
3. If ,and only if,W/S=1,the differences between SL1 and (L/F+1)/2,and between SL2 and (L/F+1)/2,are blanked.

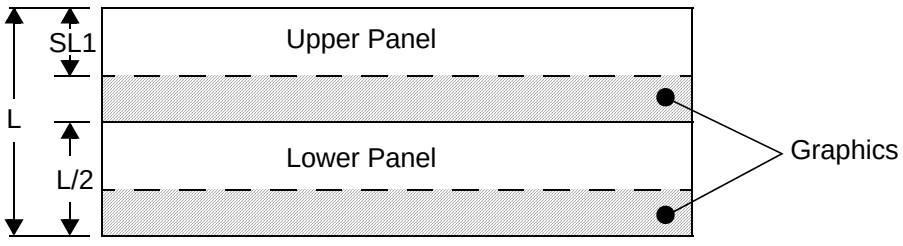


Fig.27 Two-panel dispaly height

8.3.3 CSRFORM

Sets the cursor size and shape. Although the cursor is normally only used in text displays,it may also e used in graphics displayswhen displaying special characters.

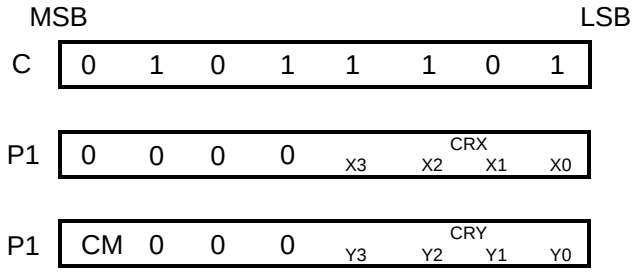


Fig.28 CSRFORM parameter bytes

8.3.3.1 CRX

Sets the horizontal size of the cursor from the character origin. CRX is equal to the cursor size less one.CRX must be less than or esqual to FX.

Table 33 Horizontal cursor size selection

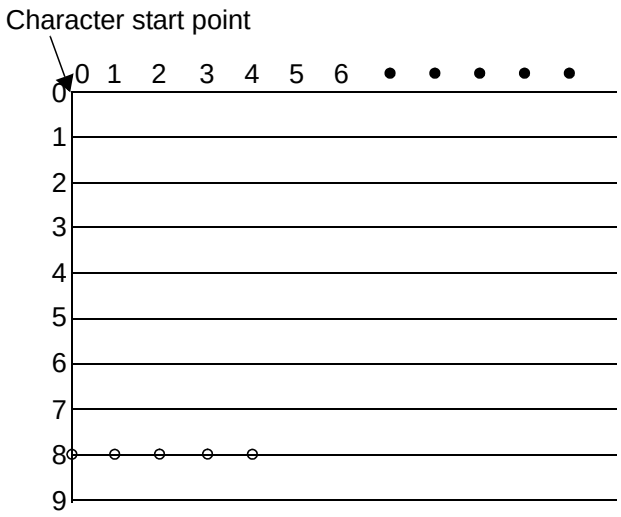
CRX					[CRX] cursor width
HEX	**X3**	**X2**	**X1**	**X0**	**(pixels)**
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↑	↓
4	0	1	0	0	9
↓	↓	↓	↓	↑	↓
E	1	1	1	0	15
F	1	1	1	1	16

8.3.3.2 CRY

Sets the location of an underscored cursor in lines,from the character origin.When using a block cursor,CRY sets the vertical size of the crsor from the character origin.CRY is equal to the number of line less one.

8.3.3.3 Cursor height selection

CRY					[CRY] cursor height
HEX	**X3**	**X2**	**X1**	**X0**	**(lines)**
0	0	0	0	0	Illegal
1	0	0	0	1	2
↓	↓	↓	↓	↑	↓
4	0	1	0	0	9
↓	↓	↓	↓	↑	↓
E	1	1	1	0	15
F	1	1	1	1	16



CRX = 5 dots

CRY = 9 dots

CM = 0

Fig.29 Cursor size and position

8.3.3.4 CM

Sets the cursor shape. Always set CM to 1 when in graphics mode.

CM=0:Underscore cursor

CM=1:Block cursor

8.3.4 CSRDIR

Sets the direction of automatic cursor increment.The cursor can move left or right one character, or up or down by the number of bytes specified by the assress pitch ,AP.When reading from and writing to display memory,this automatic cursor increment controls the display memory address increment on each read or write.

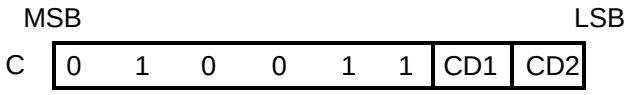


Fig.30 CSRDIR parameters

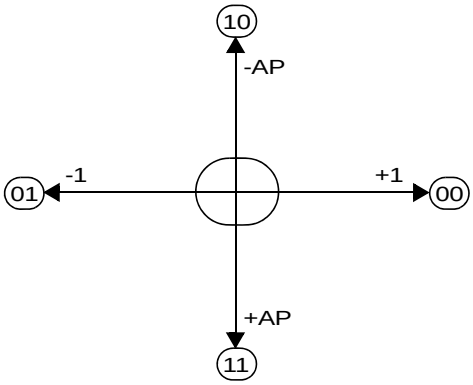


Fig.31 Cursor direction

Table 34 Cursor shift direction

C	CD1	CD2	Shift direction
4CH	0	0	Right
4DH	0	1	Left
4EH	1	0	Up
4FH	1	1	Down

Note:

Since the cursor moves in address units even if FXŠ 9,the cursor address increment must be preset for movement in character units .See Section 9.3.

8.3.5 OVLAY

Selects layered screen composition and screen text/graphics mode.

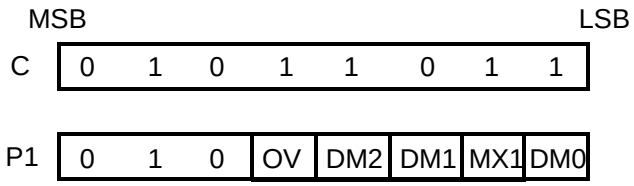


Fig.32 OVLAY parameters

8.3.5.1 MX0,MX1

MX0 and MX1 set the layered screen composition method, which can be either OR,AND, Exclusive-OR or Priority-OR.Since the screen composition is organized in layers and not by screen blocks different composition methods cannot be specified for the individual screen blocks.The Priority-OR mode is the same as the OR mode unless flashing of individual screens used.

Table 35 Cursor flash rate selection

MX1	MX0	Function	Composition Method	Applications
0	0	$L1 \cup L2 \cup L3$	OR	Underlining,rules,text and graphics
0	1	$(L1 \oplus L2) \cup L3$	Exclusive-OR	Inverted characters,flashing regions, underlining
1	0	$(L1 \cap L2) \cup L3$	AND	Simple,animation,threedmensional appearance
1	1	$L1 > L2 > L3$	Priority-OR	

Note:

L1: First layer(text or graphics).If text is selected ,layer L3 cannot be used.

L2: Second layer (graphics only)

L3: Third layer (graphics only)

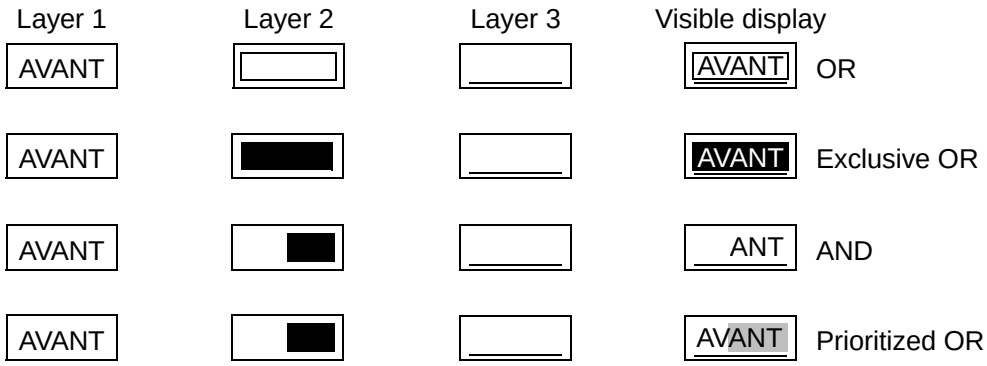


Fig.33 Combined layer display

Note:

L1: Not flashing

L2: Flashing at 1 Hz

L3: Flashing at 2 Hz

8.3.5.2 DM1,DM2

DM1 and DM2 specify the display mode of screen blocks 1 and 3,respectively.

DM1/2=0:Text mode

DM1/2=1:Graphics mode

Note 1:Screen blocks 2 and 4 can only display graphics.

Note2:DM1 and DM2 must be the same,regardless of the setting of W/S.

8.3.5.3 OV

Specifies two- or three-layer composition in graphics mode.

OV=0:Two-layer composition

OV=1:Three-layer composition

Set OV to 0 for mixed text and graphics mode.

8.3.6 CGRAM ADR

Specifies the CG RAM start address.

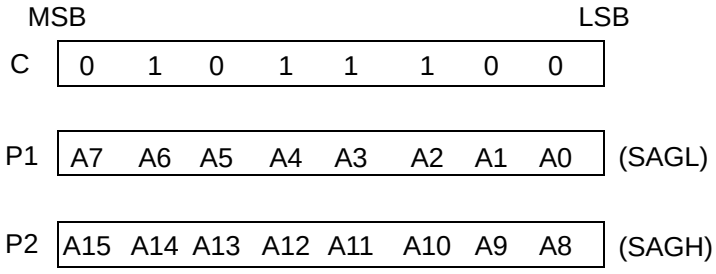


Fig.34 CGRAM ADR parameters

Note:

See section 10 for information on the SAG parameters.

8.3.7 HDOT SCR

While the SCROLL command only allows scrolling by characters,HDOT SCR allows the screen to be scrolled horizontally by pixels.HDOT SCR cannotbe used on individual layers.

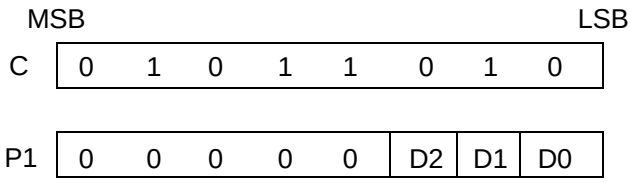


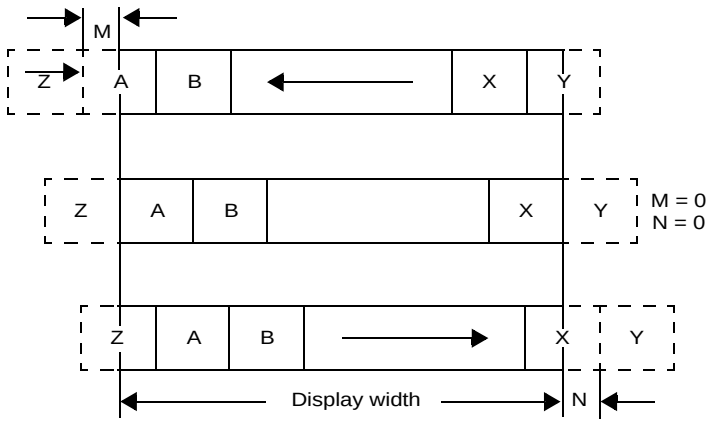
Fig.35 HDOT SCR parameters

8.3.7.1 D0 TO D2

Specifies the number of pixels to scroll.The C/R parameter has to be set to one morethan the number of horizontal characters before usingHDOT SCR.Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the SAP3305 series.See section 9.5 for more informationon on scrolling the display.

Table 36 Horizontal cursor size selection

P1				Number of pixels to scroll
HEX	**X2**	**X1**	**X0**	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
↓	↓	↓	↓	↓
06	1	1	0	6
07	1	1	1	7



M/N is the number of bits (dots) that parameter 1 (P1) is incremented/decremented by.

Fig.36 Horizontal scrolling

8.4 Drawing control commands

8.4.1 CSRW

The 16-bit cursor address register contains the display memory address of the data at thecursor position as shown in Figure 37.

Note that the microprocessor cannot directly access the display memory.The MREAD and MWRITE commands use the address in this register.

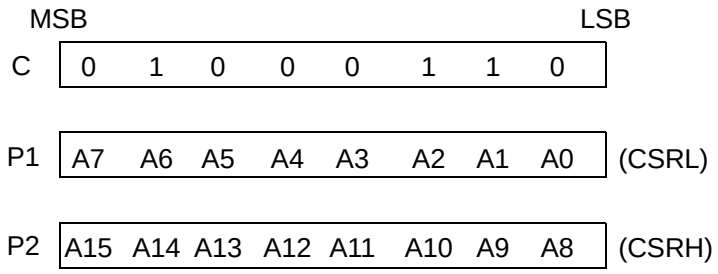


Fig.37 CSRW parameters

The cursor address register can only be mofified by the CSRW command. It is not affected by displayscrolling.If a new address is not set,displaymemory accesses will be from the last set address or the address after previous automatic increments.

8.4.2 CSRR

Reads from the cursor address register.After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.

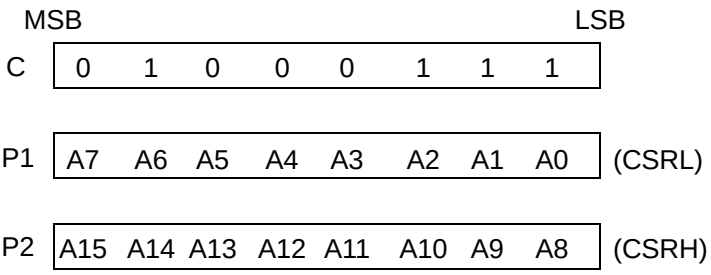


Fig.38 CSRR parameters

8.5 Memory control commands

8.5.1 MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the SAP3305 series. There is no need for further MWRITE commands or for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR,in preparation for the next data write.

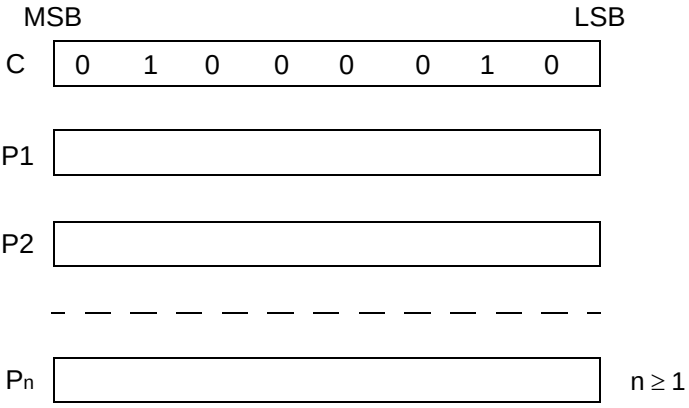


Fig.39 MWRITE parameters

Note:

P1,P2,...,Pin: display data.

8.5.2 MREAD

Puts the SAP3305 series into the data output state.Each time the microprocessor reads the buffer,the cursoraddress is incremented by the amount set by CSRDIR and the next data byte fetched from memory,so a sequence of data bytes may be read without further MREAD commands or by updating the cursor address register.If the cursor is displayed ,the read data will be from two positions ahead of the cursor.

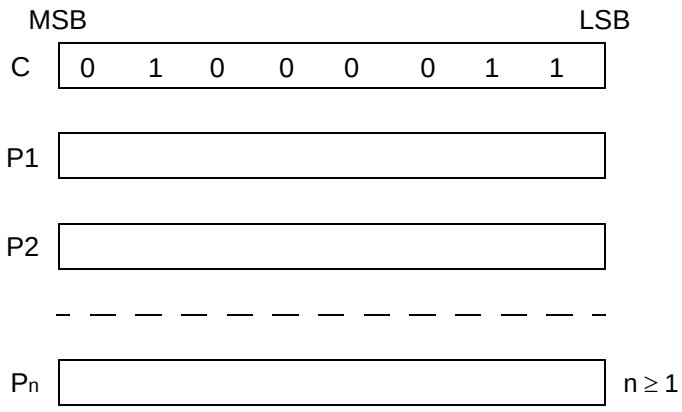


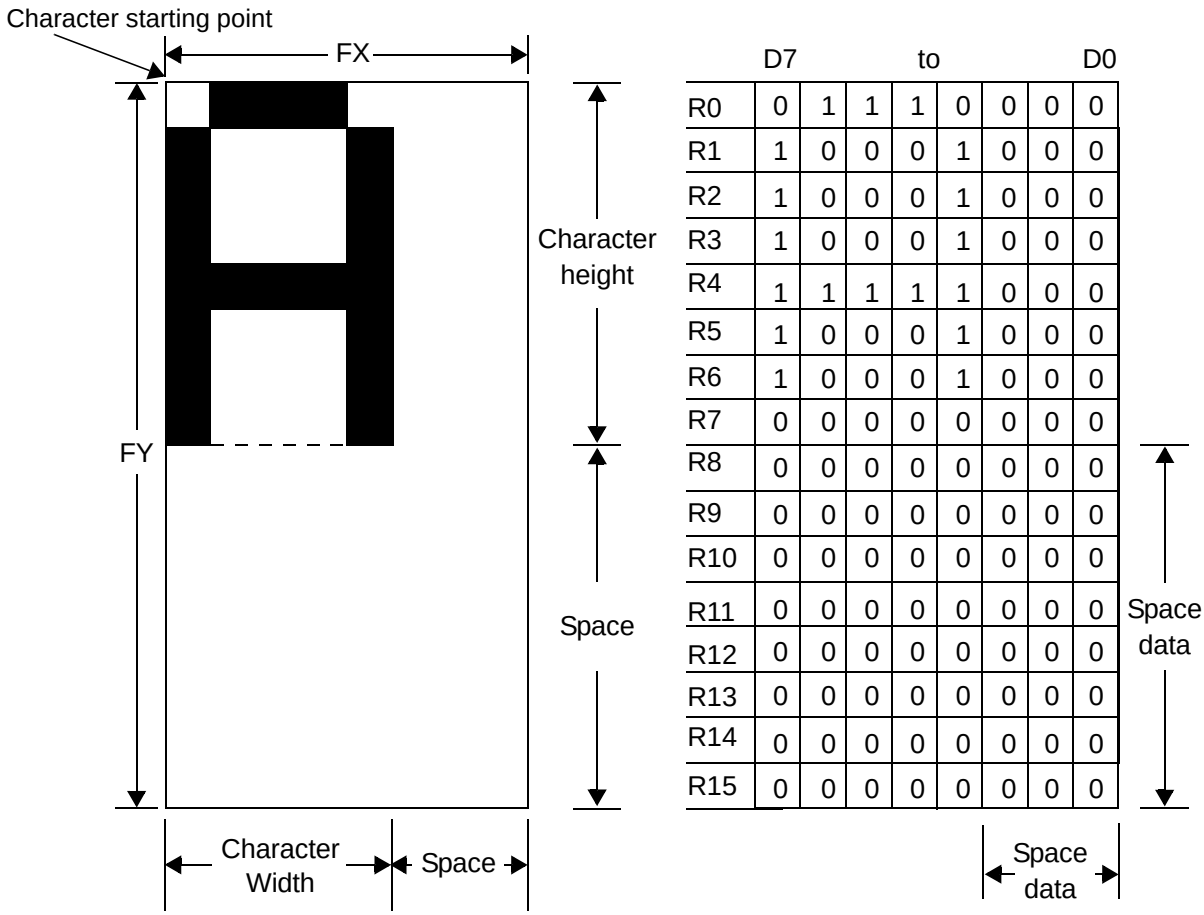
Fig.40 MREAD parameters

9 DISPLAY CONTROL FUNCTIONS

9.1 Chatacter configuration

The origin of each chaacter bitmap is in the top left comer as shown in Figure 44.Adjacent bits in each byte are horizontally adjacent in the corresponding character image.

Although the size of the bitmap is fixed by the character generator, the atual displayed size of the characterThe field can be varied in both dimensions.



	D7			to				D0
R0	0	1	1	1	0	0	0	0
R1	1	0	0	0	1	0	0	0
R2	1	0	0	0	1	0	0	0
R3	1	0	0	0	1	0	0	0
R4	1	1	1	1	1	0	0	0
R5	1	0	0	0	1	0	0	0
R6	1	0	0	0	1	0	0	0
R7	0	0	0	0	0	0	0	0
R8	0	0	0	0	0	0	0	0
R9	0	0	0	0	0	0	0	0
R10	0	0	0	0	0	0	0	0
R11	0	0	0	0	0	0	0	0
R12	0	0	0	0	0	0	0	0
R13	0	0	0	0	0	0	0	0
R14	0	0	0	0	0	0	0	0
R15	0	0	0	0	0	0	0	0

Fig.41 Example of chaacter display ($[FX] \leq 8$) and generator bitmap

If the area outside the character bitmap contains only zeros,the displayed character size can easily be increased by increasing FX and FY,as the zeros ensure that the extra space between displayed characters is blank.The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

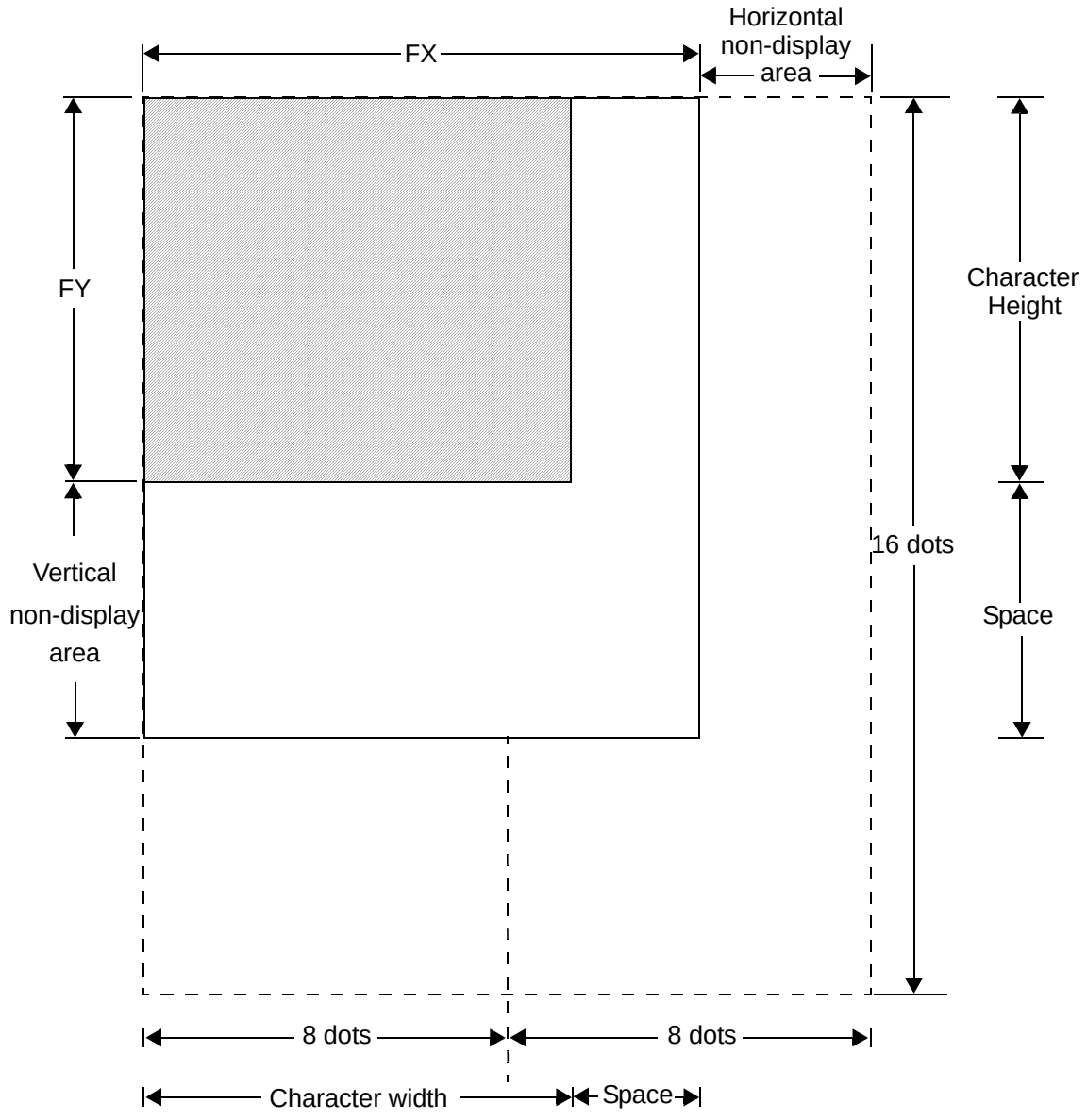


Fig.42 Character width greater than one byte wide ([FX]=9)

Note:

The SAP3305 series does not automatically insert spaces between characters.If the displayed character size is 8 pixels or less and the space between character origins is pixels or more, the bitmap must use two bytes per row,even thoug the character image requires only one.

9.2 Screen Configuration

9.2.1 SCREEN CONFIGURATION

The basic screen configuration of the SAP3305 series is as a single tezt screen or as overlapping text and graphics screens. The graphics screen uses eight times as much dsplay memory as the text screen.Figure 43 show the relationship between the virtual screen and the physical screen.

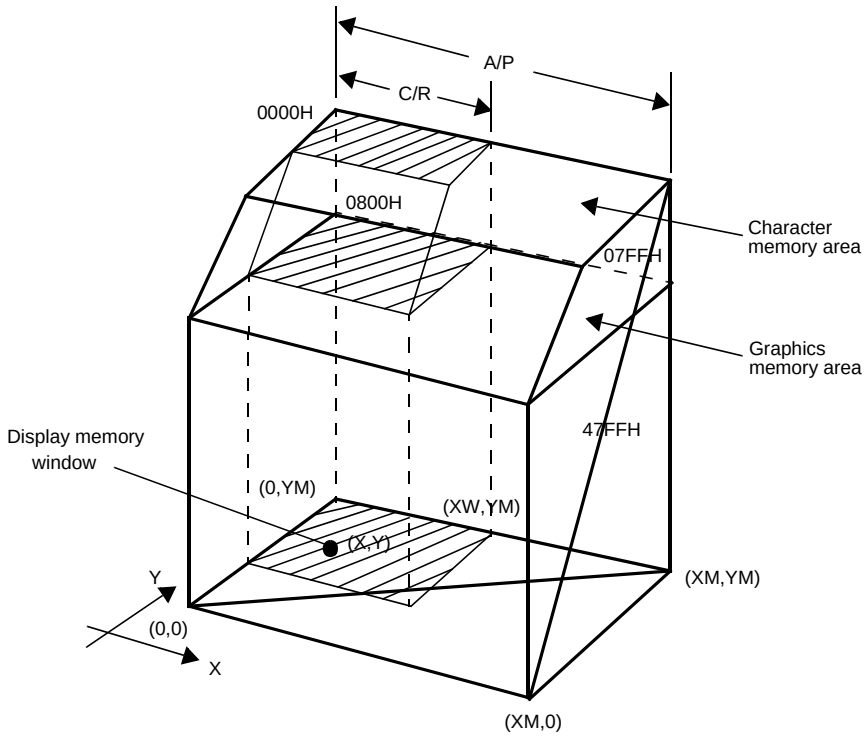


Fig.43 Virtual and physical screen relationship

9.2.2 DISPLAY ADDRESS SCANNING

The SAP3305 series until the address scans the display memory in the same way as a raster scan CRT screen .Each row is scanned from left to right untilthe address range equals C/R.Rows are scanned from top to bottom.In graphics mode, at the start of each line, the address counter is set to the address at the start of the previous line plus the address pitch,AP.

In text mode.the address counter is set to the same start address.and the same character data is read,for each row in the character bitmap.However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed , the address counter is set to the start address plus AP and the next line of text is displayed.

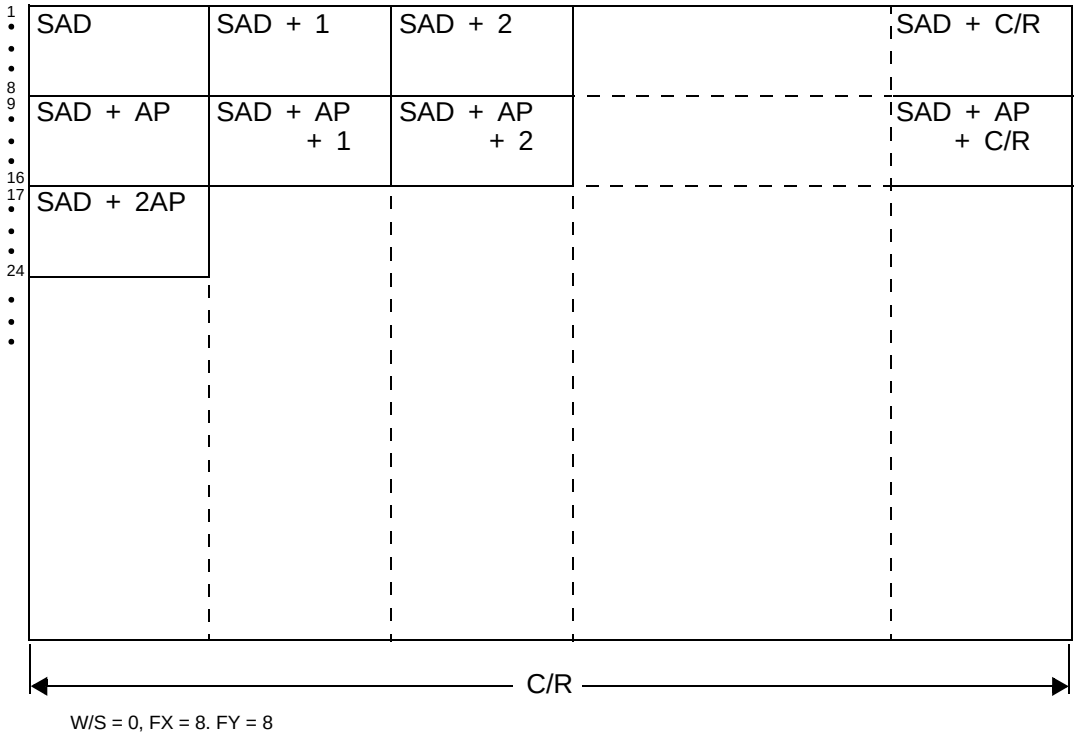


Fig.44 Character position parameters

Note: One byte of display memory corresponds to one character.

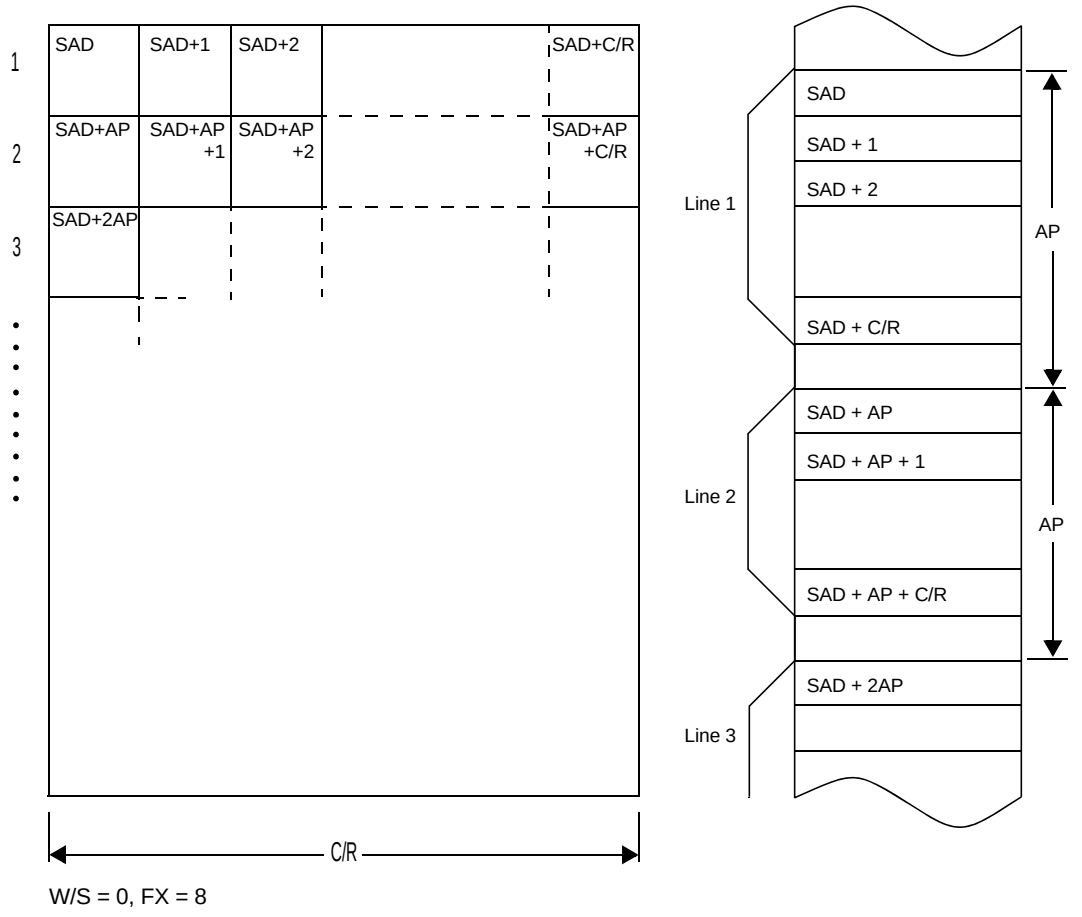
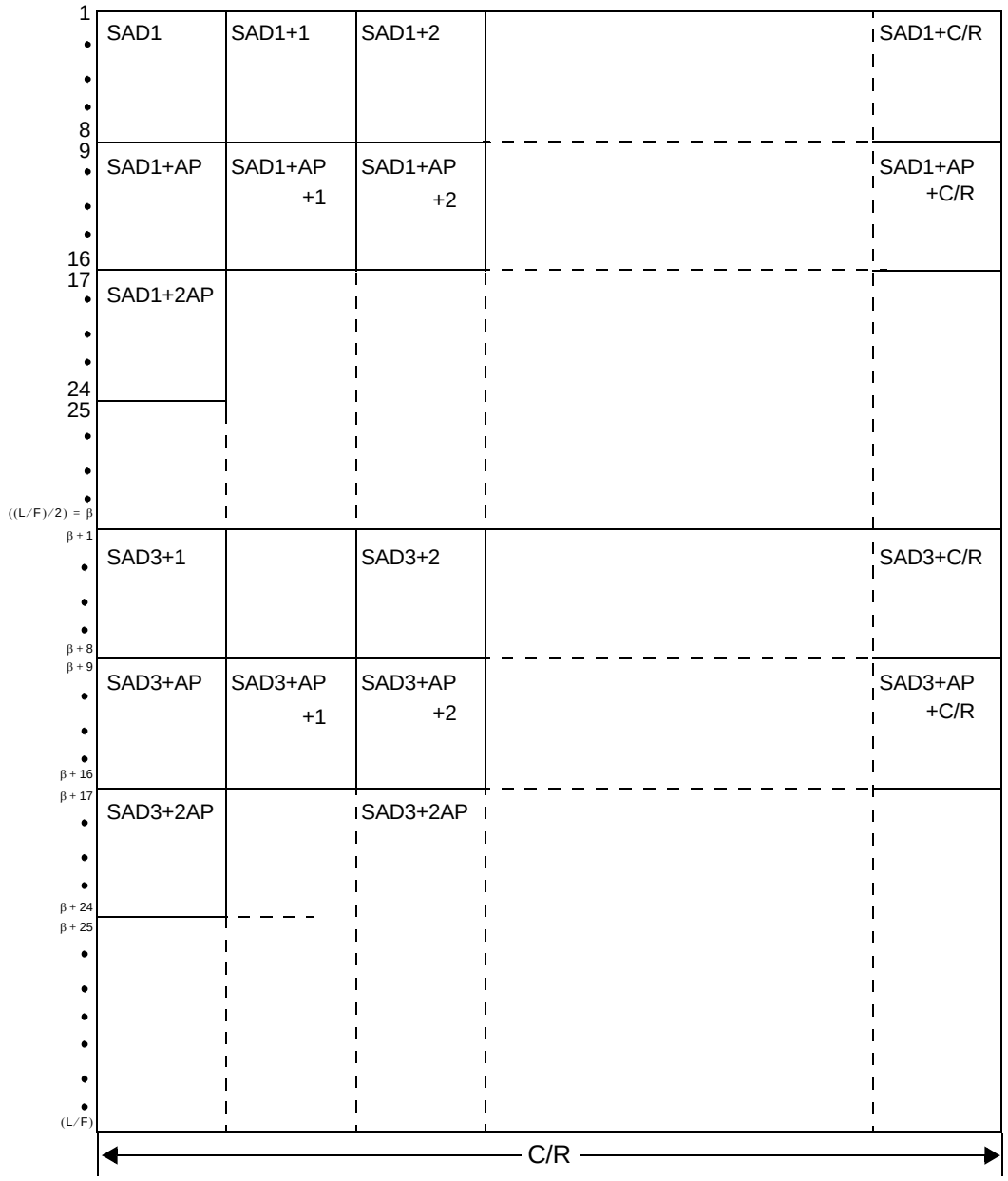


Fig.45 Character parameters vs. memory

Note:One bit of display memory corresponds to one pixel.



W/S = 1, FX = 8, FY = 8

Fig.46 Two-panel display address indexing

Note:

In two-panel drive,the SAP3305 series reads line 1 and line β +1 as one cycle. The upper and lower panels are thus read alternately, one line at a time.

9.2.3 DISPLAY SCAN TIMING

Figure 47 shows the basic timing of the SAP3305 series.One display memory read cycle takes nine periods of the system clock, $\phi 0$ (f_{OSC}).This cycle repeats(C/R+1)times per display line.

When reading,the display memory pauses at the end of each line for (TC/R-C/R) display memory read cycles.though the LCD drive signals are still generated.TC/Rmay be set to any value within the constraints imposed by C/R,fosc,f_{FR},and the size of the LCD panel,and it may be used to fine tune the frame frequency.The microprocessor may also use this pause to access the display memory data.

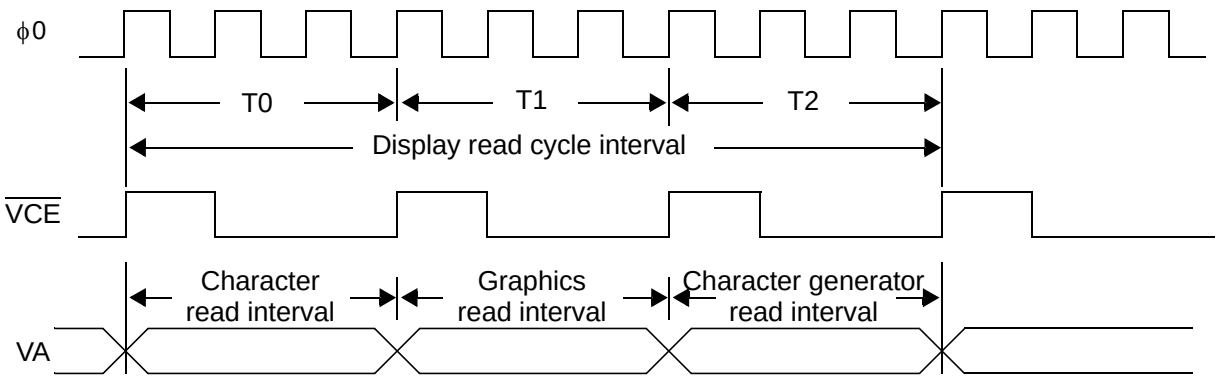


Fig.47 Display period memory basic read cycle

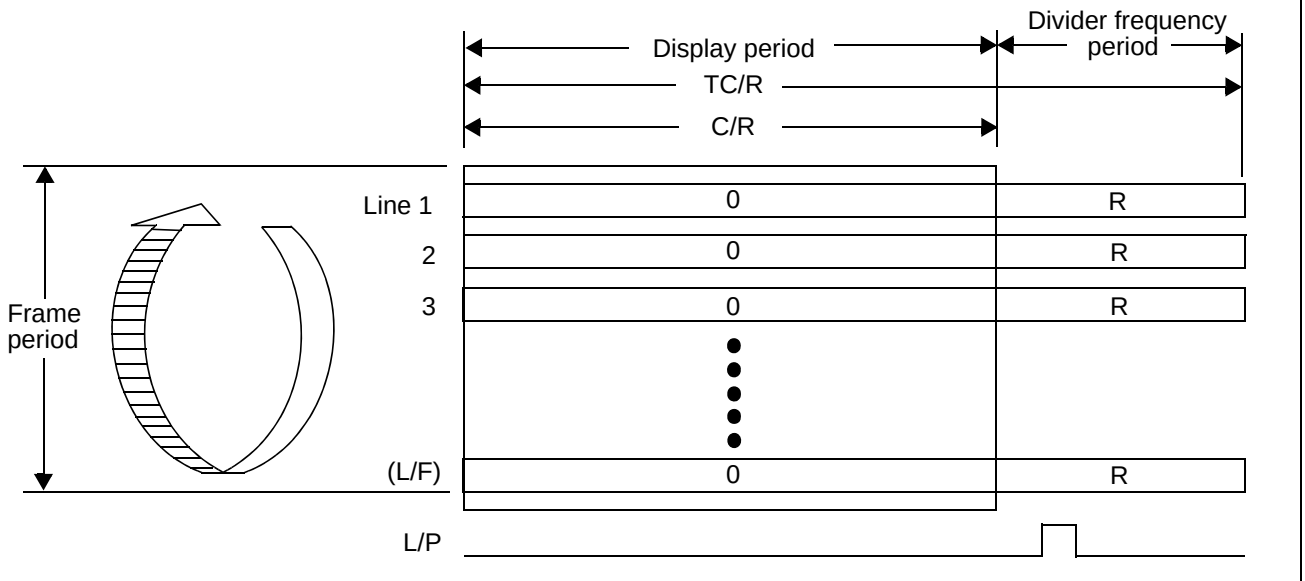


Fig.48 Relationship between TC/R and C/R

Note:

The divider adjustment interval(R) applies to both the upper and lower screens even if W/S=1. In this case,LP is active only at the end of the lower screen's display interval.

9.3 Cursor Control

9.3.1 CURSOR REGISTER FUNCTION

The SAP3305 series cursor address register functions as both the displayed cursor position address register and the display memory access address register.When accessing display memory outside the actual screen memory,the address register must be saved before accessing the memory and restored after memory access is complete.

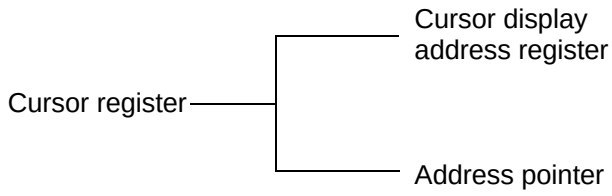


Fig.49 Cursor addressing

Note that the cursor may disappear from the display if the cursor address remains outdside the displayed screen memory for more than a few hundred milliseconds.

9.3.2 CURSOR MOVEMENT

On each memory access,the cursor address register changes by the amount previously specified with CSRDIR,automatically moving the cursor to the desired location.

9.3.3 CURSOR DISPLAY LAYERS

Althugh the SAP3305 series can display up to three layers,the cursor is displayed in only one of these layers:

Two-layer configuration:First layer(L1)

Three-layer configuration:Third layer(L3)

The cursor will note be displayed if it is moved outside the memory for is layer.Layers may be swapped or the crsor layer moved within the display memory if it is necessary to display the cursor on a layer other than the present cursor layer.

Although the cursor is normally displayed for character data, the SAP3305 series may also displaya dummy cursor for graphical characters.This is only possible if the graphics screen is displayed,the text screen is turned off and the icroprocessor ginerates the cursorcontrol address.

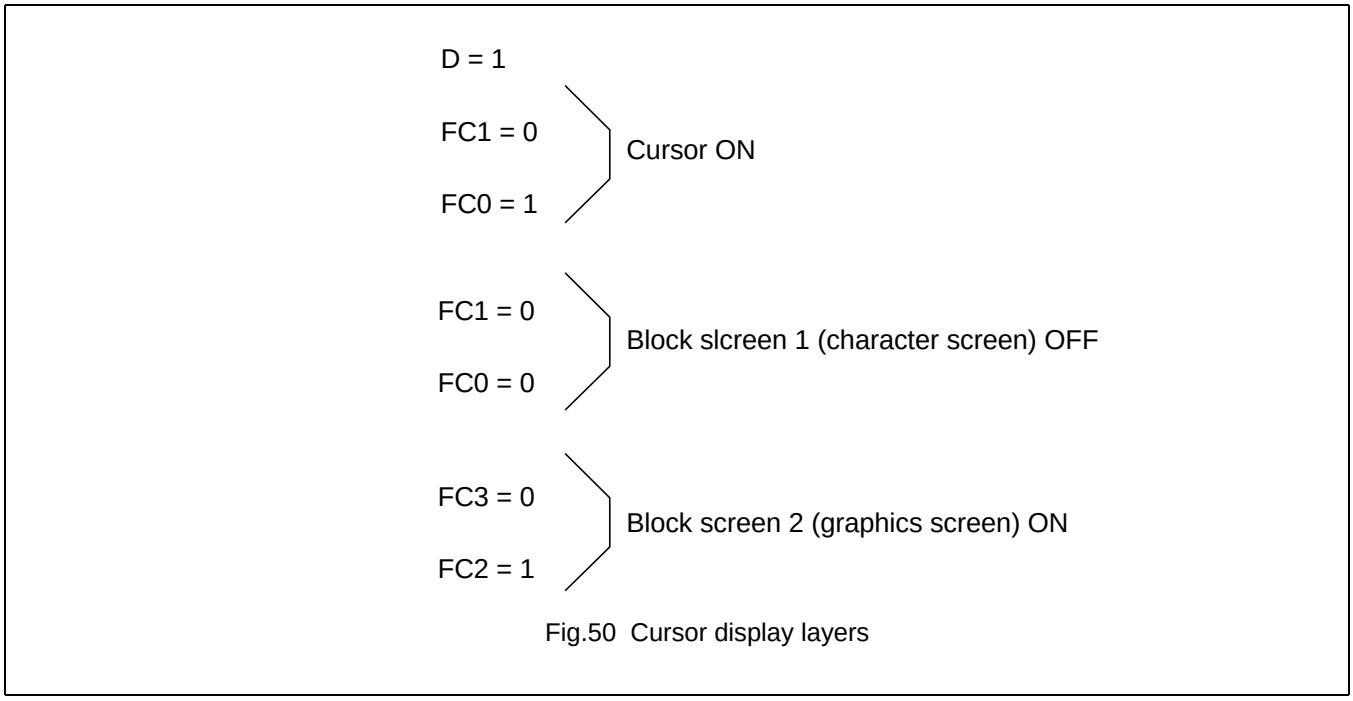


Fig.50 Cursor display layers

Consider the example of displaying Chinese characters on a graphics screen.To write the display data,the cursor address is set to the second screen block,but the cursor is not displayed. To display the cursor,the cursor address is set to an address within the blank text screen block.Since the autoatic cursor increment is in address unts,not character units,the controlling mcroprocessor must set the cursor address register when moving the cursor over the graphical characters.

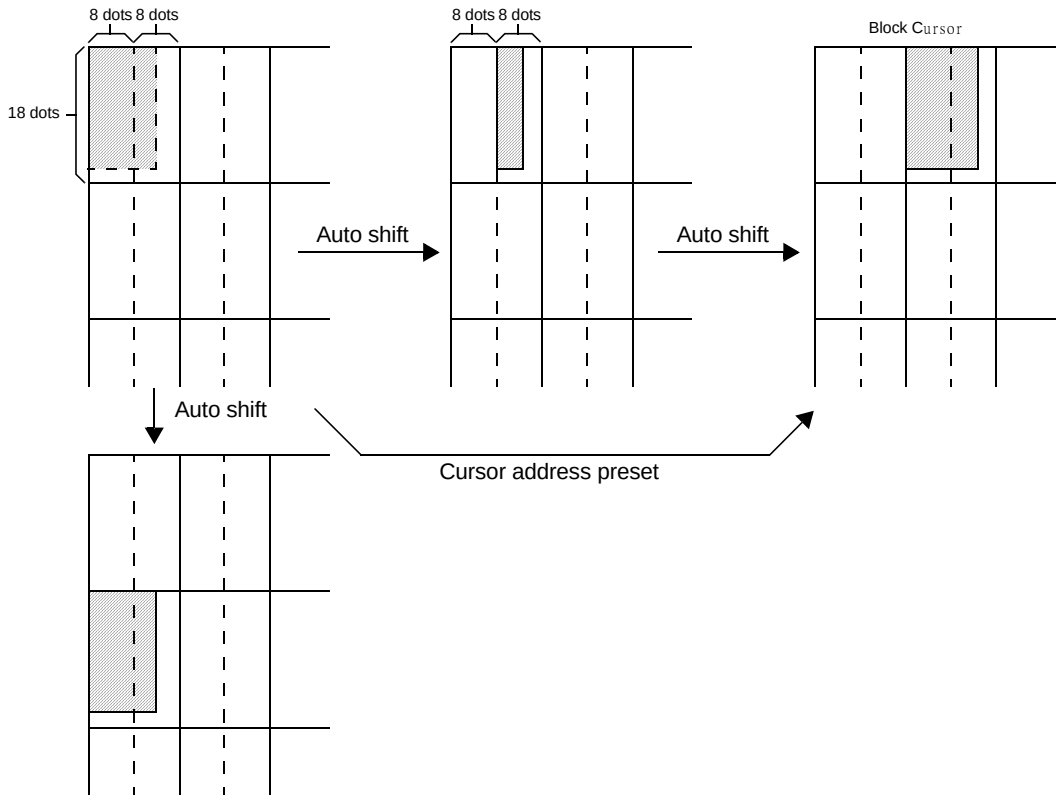


Fig.51 Cursor movement

If no text screen is displayed,only a bar cursor can be displayed at the cursor address.If the first layer is a mixed text and graphics screen and the cursor shape is set to a blockcursor,the SAP3305 series automaticlly decides which cursor shape to display.On the graphics screen,a bar cursor.

9.4 Memory to Display Relationship

The SAP3305 series supports virtual screens that are larger than the physical size of the LCD panel address range ,C/R.A layer os the SAP3305 series can be considered as a window in the large virtual screen held in display memory.This window can be divided into two blocks, with each block able to display a different portion of the virtual screen.This enables,for example,one block to dynamically scroll through a data area while the other acts as a status message display area. See Figure 52 and 53.

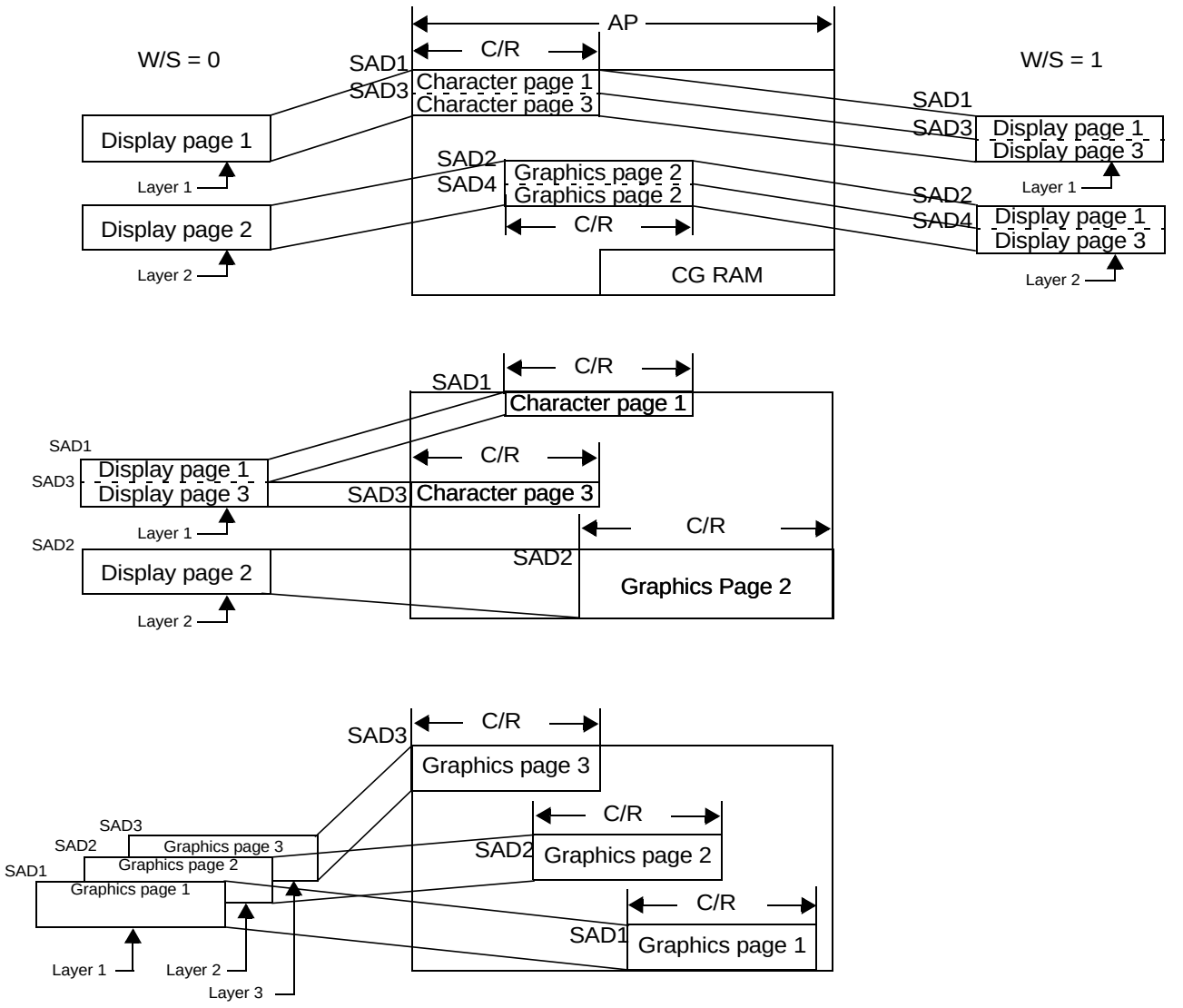


Fig.52 Display layers and memory

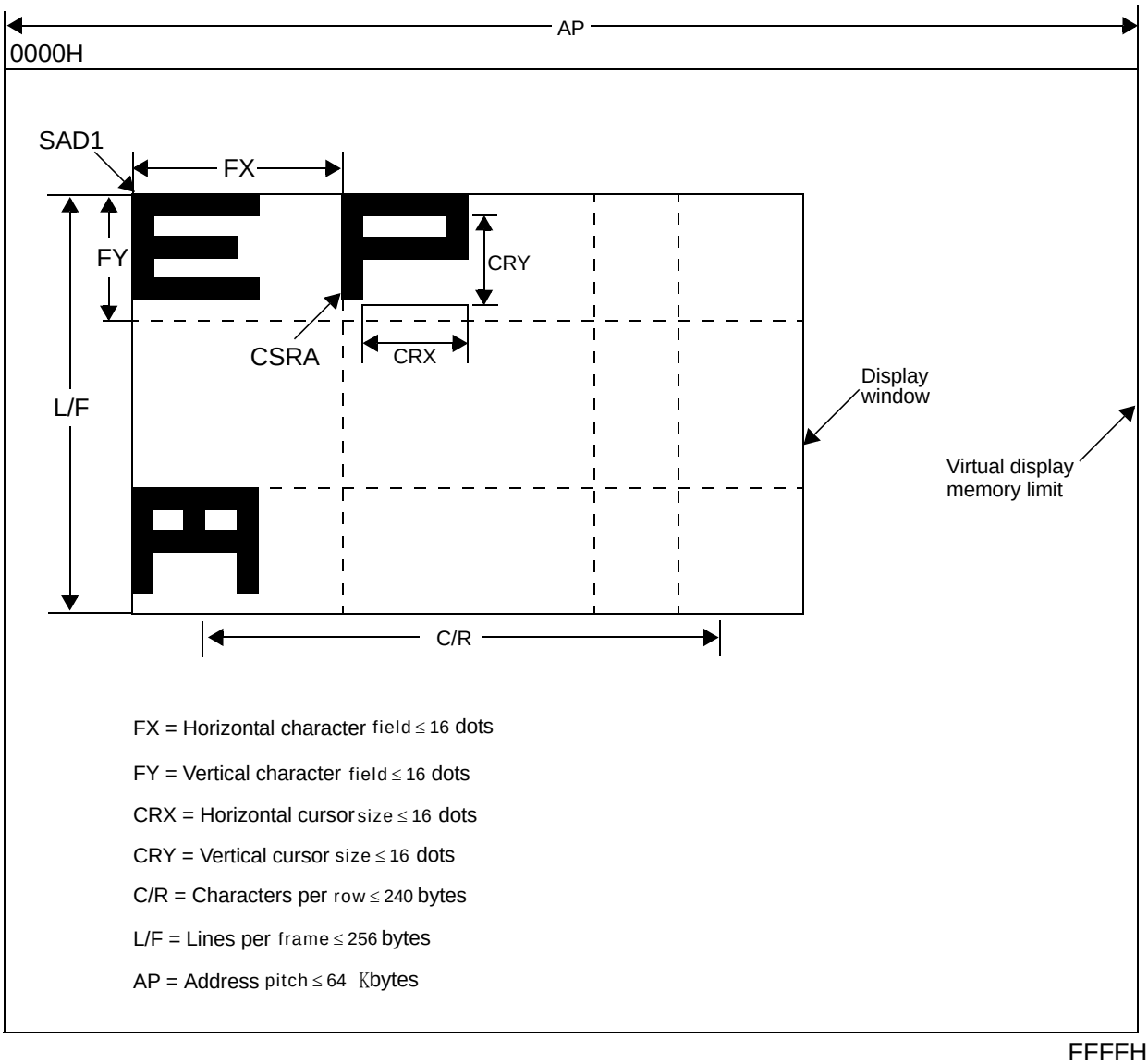


Fig.53 Display window and memory

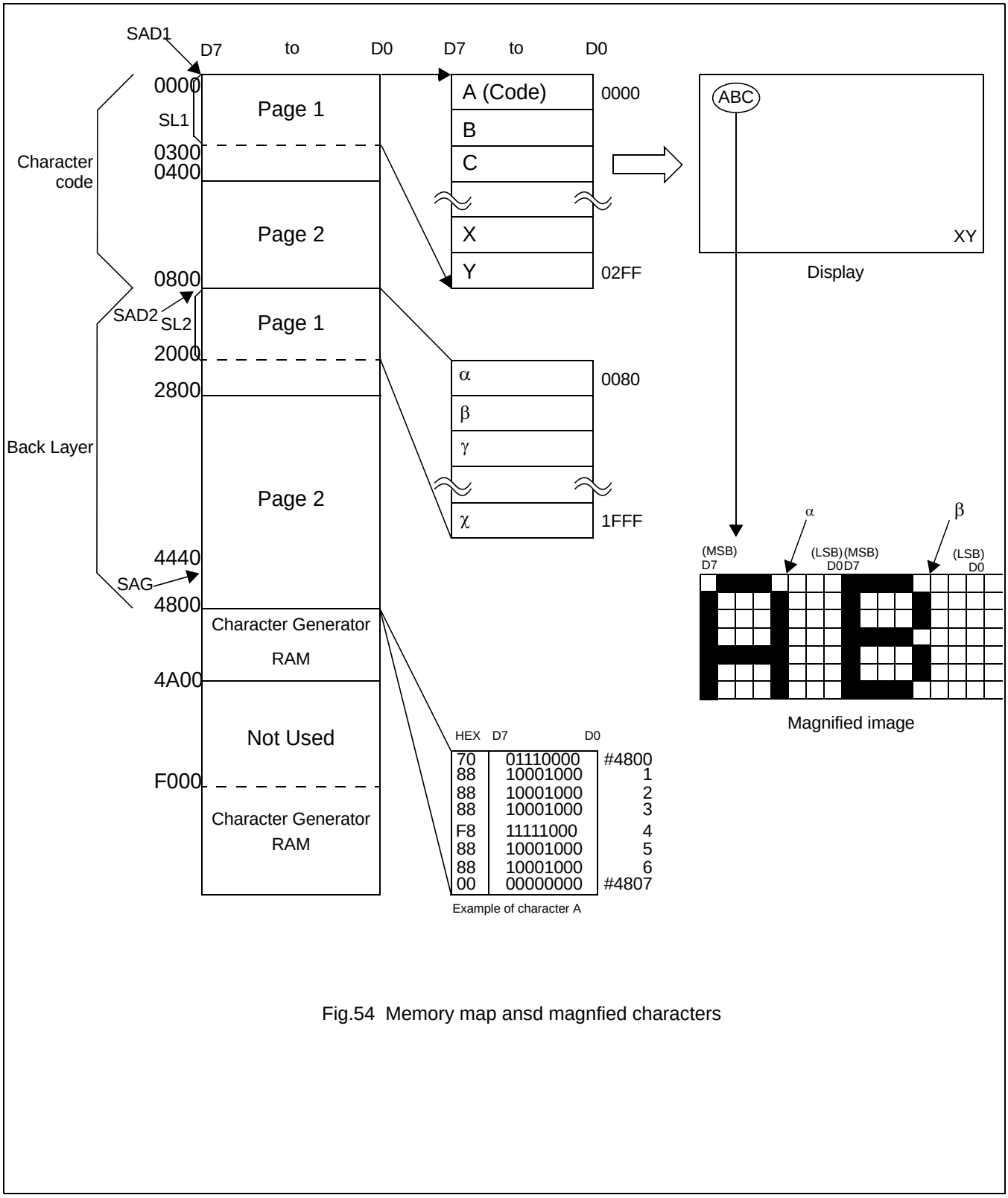


Fig.54 Memory map ansd magnfied characters

9.5 Scrolling

The controlling microprocessor can set the SAP3305 series scrolling modes by overwriting the scoll address registers SAD1 to SAD4,and by directly setting the scrolling mode and scrolling rate.

9.5.1 ON-PAGE SCROLLING

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line.Since the SAP3305 series does not automatically erase the bottom line ,it must be erased with blanking data when changing the scroll address register.

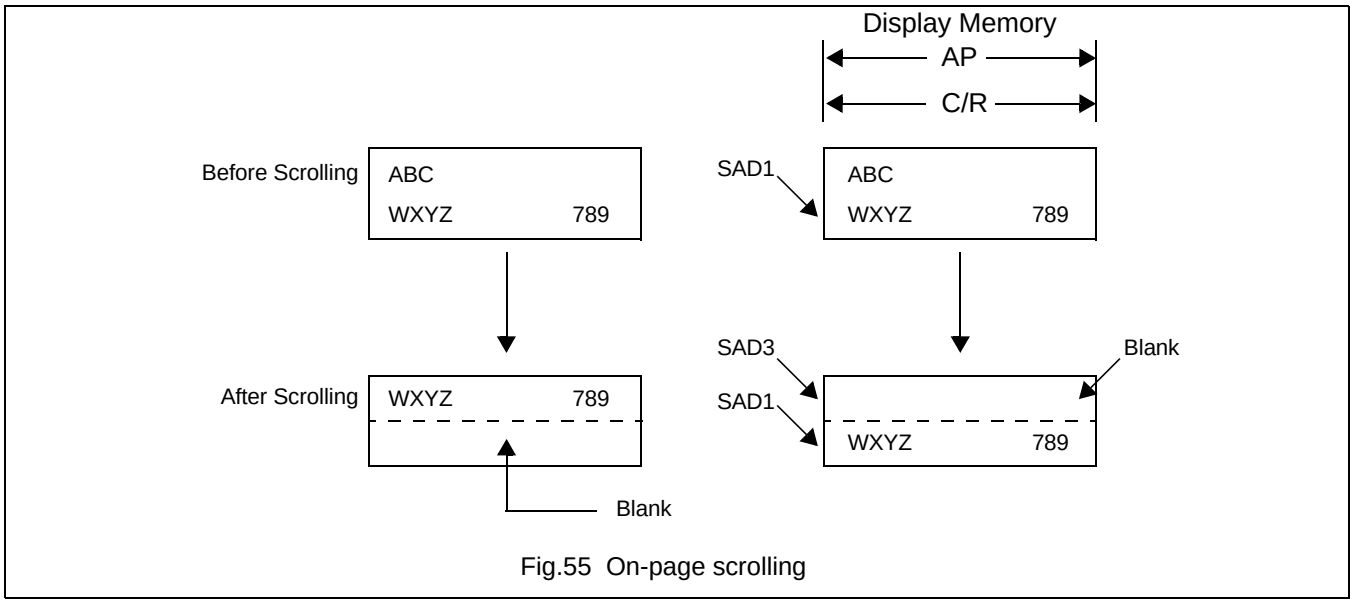


Fig.55 On-page scrolling

9.5.2 INTER-PAGE SCROLLING

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen.

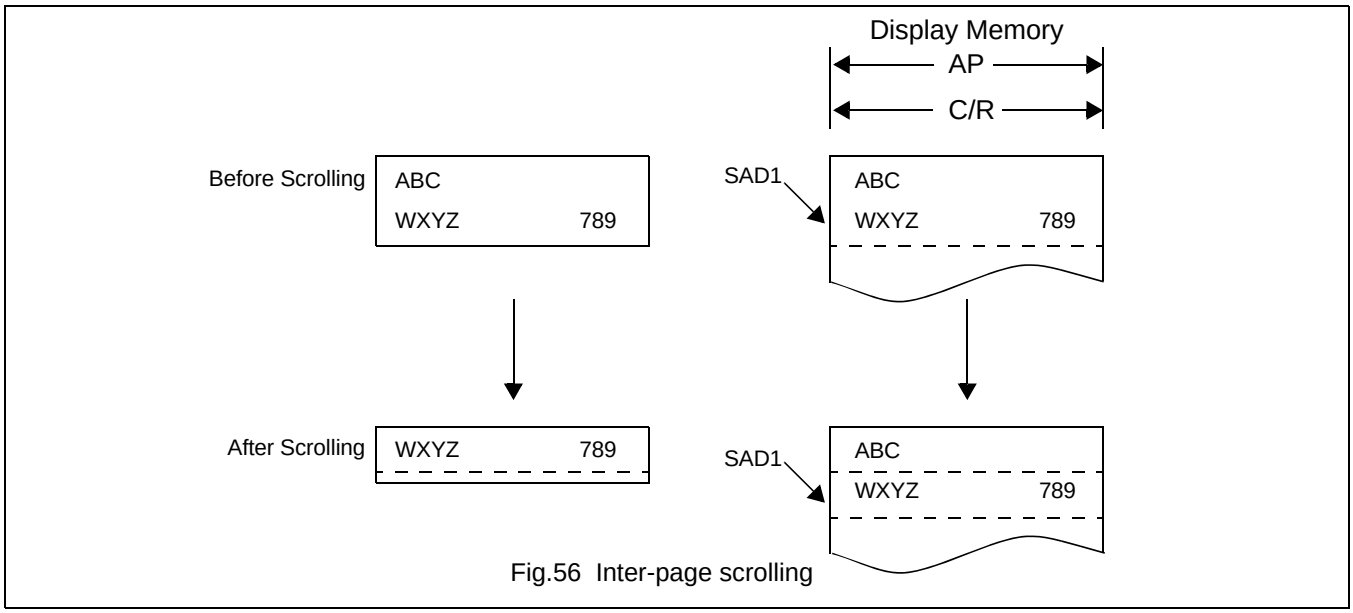


Fig.56 Inter-page scrolling

9.5.3 HORIZONTAL SCROLLING

The display can be scrolled horizontally in one-character units,regardless of the display memory capacity.

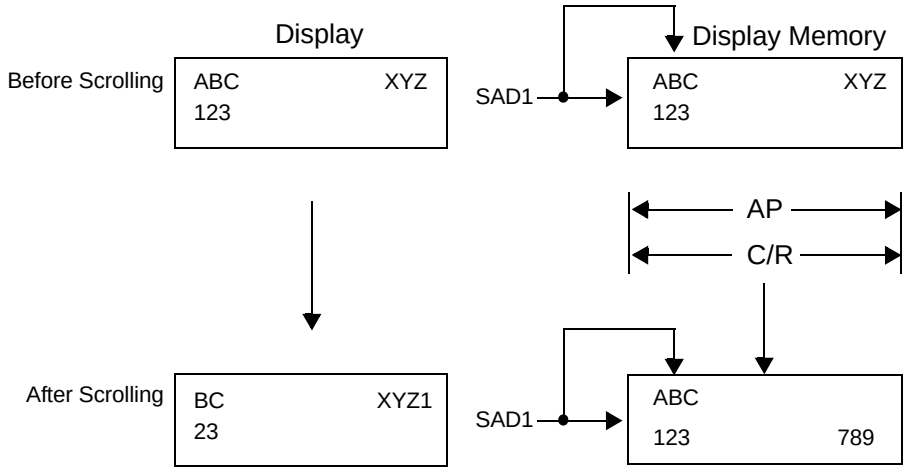


Fig.57 Horizontal wraparounf scrolling

9.5.4 BIDIRECTIONAL SCROLLING

Bidirectional scrolling can be performed only if the display memory is larger than the physical screen both horizontally and vertically.Although scrolling is normally done in single-character units,the HODOT SCR command can be used to scroll horizontally in ixel units.Single-pixel scrolling both horizontally and vertically can be performed by using the SCROLL and HDOT SCR commands. See Section 16.4

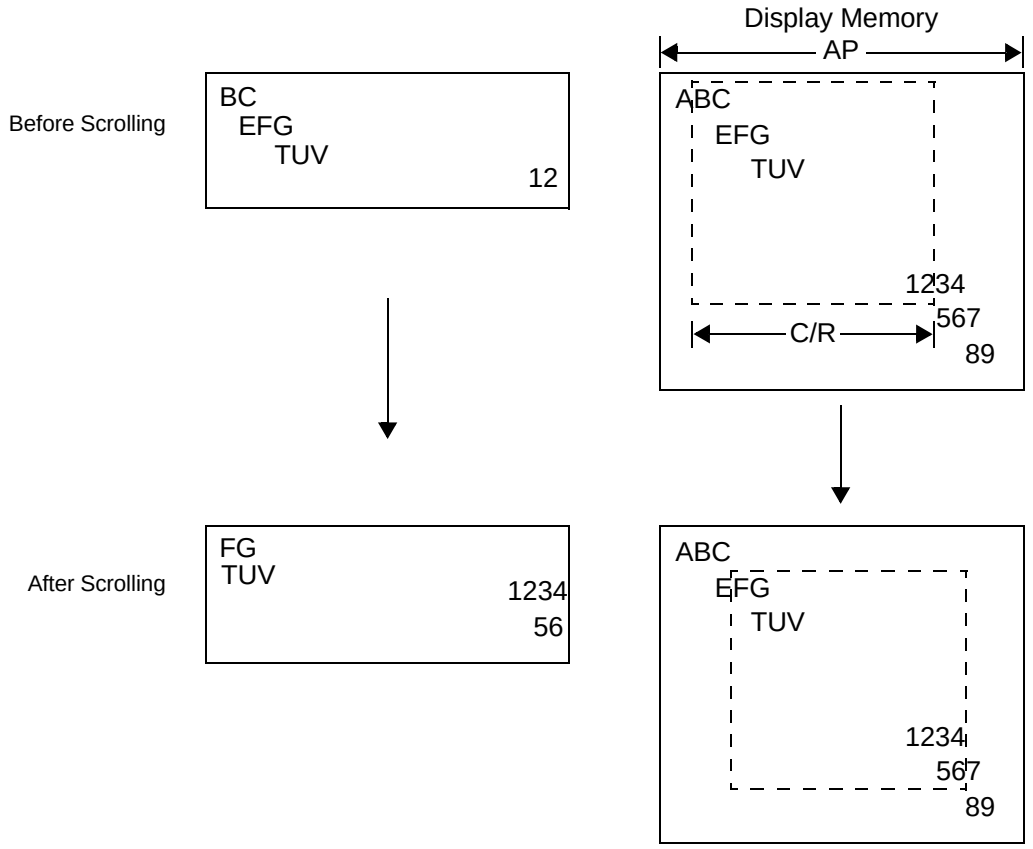


Fig.58 Birdirectional scrolling

9.5.5 SCROLL UNTS

Table 37 Scroll units

Mode	Vertical	Horizontal
Text	Characters	Pixels or characters
Graphics	Pixels	Pixels

Note:

That in a divided screen,each block cannot be independscroly scrolled horizontally in pixel unit.

10 CHARACTER GENERATOR

10.1 CG Characteristics

10.1.1 INTERNAL CHARACTER GENERATOR

The intermal character generator is recommended for minmum system configurations containing a SAP3305 series , display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5X7-pixel font (See Section 17.)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximun of 64 CG RAM characters)
- Can be automatically spaced out to 8X16 pixels

10.1.2 EXTERNAL CHARACTER GENERATOR ROM

The external CG ROM can be used when fonts other than those in the internal ROM are needed. Data is stored in the external ROM in the same format used in the internal ROM. (See Section 10.3.)

- Up to 8X8-pixel characters(M2=0)or 8X16-pixel characters(M2=1)
- Up to 256 characters(192 if used together with the internal ROM)
- Mapped into the display memory address space at F000H to F7FFH(M2=0) or F000H to FFFFH(M2=1)
- Characters can be up to 8X16-pixels;however, excess bits must be set to zero.

10.1.3 CHARACTER GENERATOR RAM

The user can freely use the character generator RAM for storing graphics characters.The character generator RAM can be mapped by the microprocessor anywhere in display memory, allowing effective use of unused address space.

- Up to 8X8-pixel characters(M2=0)or 8X16-pixel characters(M2=1)
- Up to 256 characters if mapped at F000H to FFFH (64 if used together with characters generator ROM)
- Can be mapped anywhere in display memory address space if used with the character generator ROM
- Mapped into the display memory address space at F000H to F7FFH if not used with the character generator ROM(more than 64 characters are in the CG RAM). Set SAG0 to F000H and M1 to zero when defining characters number 193 upwards.

10.2 CG Memory Allocation

Since the SAP3305 series uses 8-bit character codes,it can handle no more than 256 characters at a time. However, if a wider range of characters is required, character generator memory can be bank-switched using the CGRAM ADR command.

incremented by the amount set with CSRDIR,in preparation for the next data write.

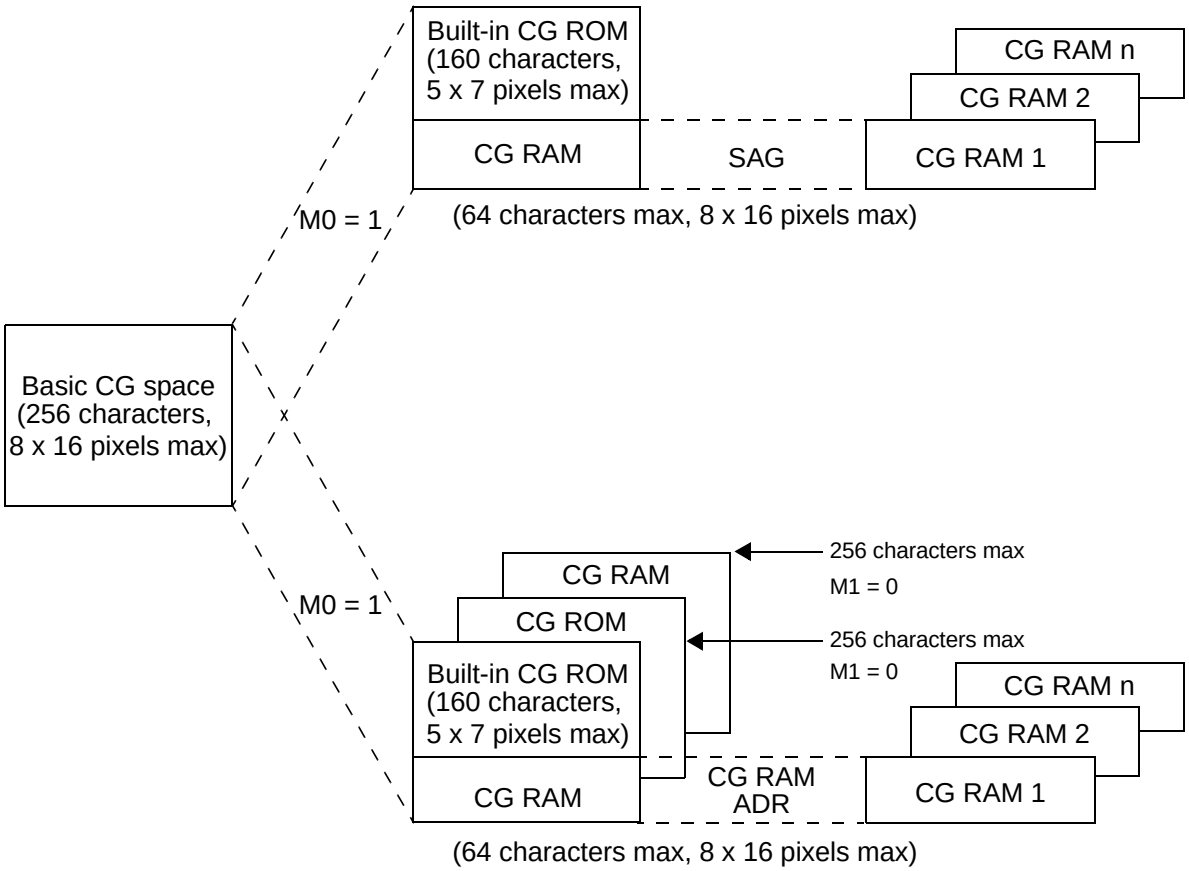


Fig.59 Internal and external character mapping

Note:

Note that there can be no more than 64 characters per bank.

Table 38 Character mapping

Item		Parameter	Remarks
Internal/external caracter generator selection		M0	
character field height	1 to 8 pixels	M2=0	
	9 to 16 pixels	M2=1	
	Greater than 16 pixels	Graphics mode (8 bit x 1 line)	
Internal CG ROM/RAM select External CG ROM/RAM select		Automatic	Determined by the character code
CG RAM bit 6 correction		M1	
CG RAM data storage address		Specified with CG RAM ADR command	Can be moved anywhere in the display memory address space
External CG ROM address	192 characters or less	Other than the area of Figure 49	
	More than 192 characters	Set SAG to F000H and overly SAG and the CG ROM table	

10.3 Setting the CharacterGenerator Address

The CG RAM address in the VRAM address space are not mapped directly from the address in the SAG register. The data to be displayed is at a CG RAM address caculated from SAG + character code + ROW select address. This mapping is shown in table 39 and 40.

Table 39 Character fonts, number of lines ≤ 8 (M2=0,M1=0)

SAG	**A15**	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Table 40 Character fonts, 9 ≤ number of lines ≤ 16 (M2=1, m1=0)

SAG	**A15**	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

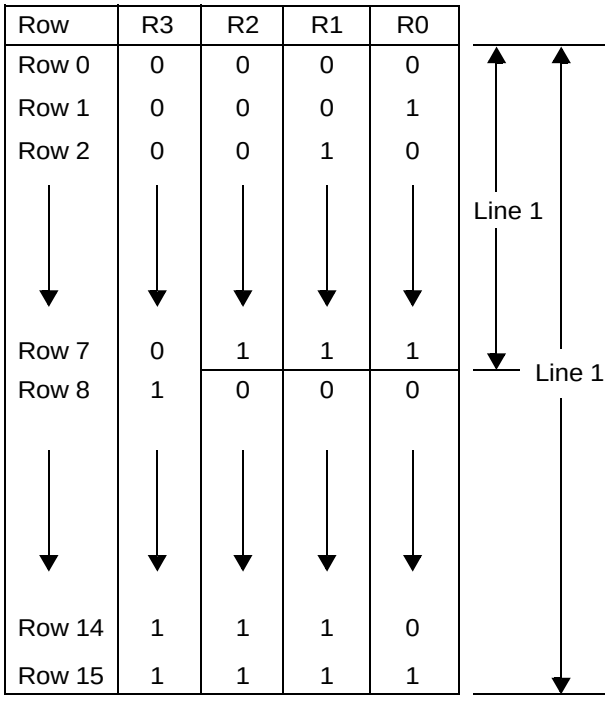


Fig.60 Row select address

Note:

LInes=1:lines in the character bitmap ≤ 8

Lines=2:lines in the character bitmap ≥ 9

10.3.1 M1=1

The SAP3305 series automatically converts all bits set in bit 6 of character code for CG RAM 2 to zero.Because of this, the CG RAM data areas become configuous in display memory.

When writing data to CG RAM:

- Calculate the address as for M1=0.
- Change bit 6 of the character code from "1" to "0".

10.3.2 CG RAM ADDRESSING EXAMPLE

- Define a patern for the "A" in Figure 26.
- The CG RAM table start address is 4800H.
- The character code for the defined pattern is 80H(the first character code in the CG RAM area).

As the character code table in Figure 61 shows, codes 80H to 9FH and E0H to FFH are allocated to the CG RAM and can be used as desired. 80H is thus the first code for CG RAM.AS characters cannot be used if only using graphics mode,there is no need to set the CG RAM data.

Table 41 Character data example

CGRAM AD	5CH	Horizontal
P1	00H	Reverse the CG RAM address calculation to calculate SAG
P2	40H	
CSRDIR	4CH	Set cursor shift direction to right
CSRW	46H	CG RAM start address is 4800H
P1	00H	
P2	48H	
MWRITE	42H	
P	70H	Write ROW 0 data
P2	88H	Write ROW 1 data
P3	88H	Write ROW 2 data
P4	88H	Write ROW 3 data
P5	F8H	Write ROW 4 data
P6	88H	Write ROW 5 data
P7	88H	Write ROW 6 data
P8	00H	Write ROW 7 data
P8	00H	Write ROW 8 data
↓	↓	↓
P16	00H	Write ROW 15 data

10.4 Character Codes

The following figure shows the character code and the codes allocated to CG RAM. All codes can be used by the CG RAM if not using the internal ROM.

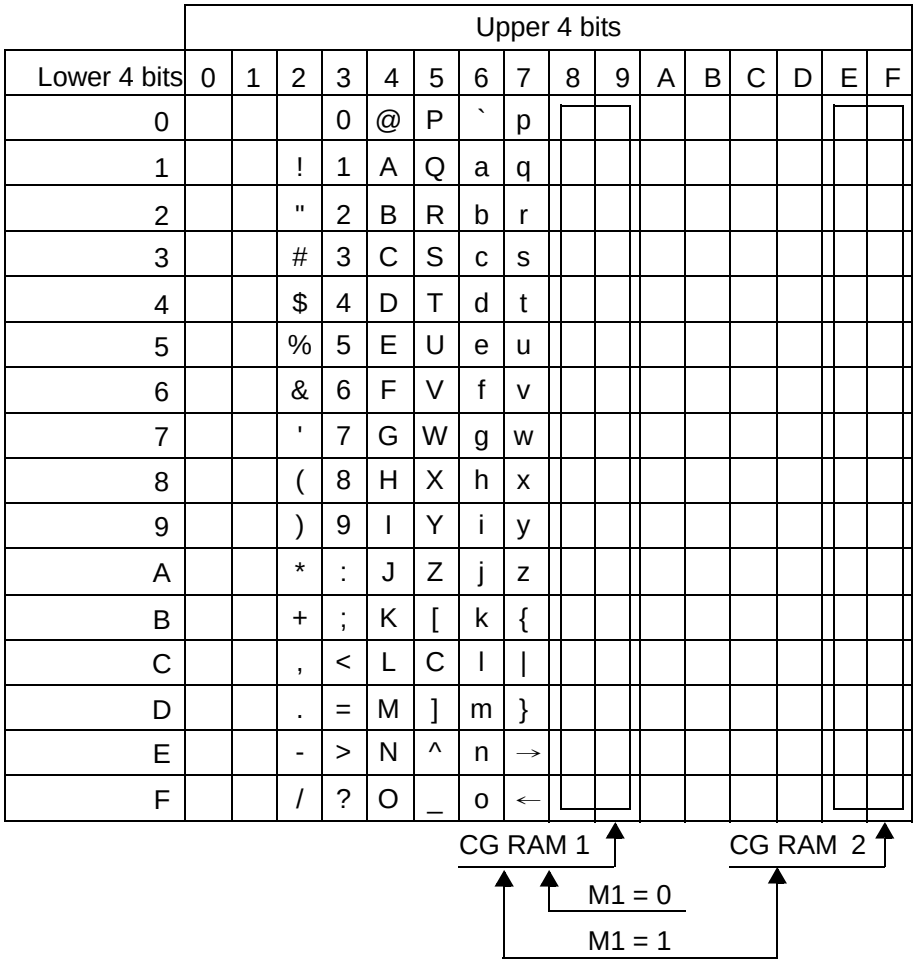


Fig.61 On-chip character codes

11 MICROPROCESSOR INTERFACE

11.1 System Bus Interface

SEL1,SEL2,A0,$\overline{RD}$,$\overline{WR}$ and $\overline{CS}$ are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the lowest bit of the system address bus. SEL1 and SEL2 change the operation of the $\overline{RD}$ and $\overline{WR}$ pins to enable interfacing to either an 8080 or 6800 fmily bus, and should have a pull-up or pull-down resistor.With microprocessor using an 8080 family interface,the SAP3305 series is normally mapped into the I/O address space.

11.1.1 8080 SERIES

Table 42 8080 series interface signals

A0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Status flag read
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

11.1.2 6800 SERIES

Table 43 6800 series interface signals

A0	R/$\overline{W}$	E	FUNCTION
0	1	1	Status flag read
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

11.2 Microprocessor Synchronization

The SAP3305 series interface operates at full bus speed,completing the execution of each command within the cycle time ,$t_{cyc.}$ The controlling microprocessor's performance is thus not hampered by polling or handshanking when accessing the SAP3305 series.

Display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame.The microprocessor can minimize this either by performing these accesses intermittently, or by continuously checking the status flag (D6)and waiting for it to become HIGH.

11.2.1 DISPLAY STATUS INDICATION OUTPUT

When CS,A0 and RD are LOW,D6 functions as the display status indication output.It is HIGH during the TV-mode vertical retrace period or the LCD-mode horizontal retrace period,and LOW, during the period the controller is writing to the dislay. By moitoring D6 and writing to the data memory only during retrace periods,the display can be updated without causing screen flicker.

11.2.2 INTERNAL REGISTER ACCESS

The SYSTEM SET and SLEEP IN commands can be used to perform input/output to the SAPP3305 series independly of the system clock frequency.These are the only commands that can be used while the SAP3305 series is in sleep mode.

11.2.3 DISPLAY MEMORY ACCESS

The SAP3305 series supports a form of pipelined processing,in which the microprcessor synchronizes its processing to the SAP3305 series timing. When writong, the microprocessor first issues the MWRITE command. It then repeatedly writes display data to the SAP3305 series using the system bus timing . This ensures that the microprocessor is not slowed down even if the display memory access times are slower than the system bus access times .See Figure 62.

When reading, the microprocessor first issues the MREAD command, which causes the SAP3305 series to load the first read data into its output buffer. The microprocessor then reads data from the SAP3305 series using the system bus timing . With each read, The SAP3305 series reads the next read access.See Figure 63.

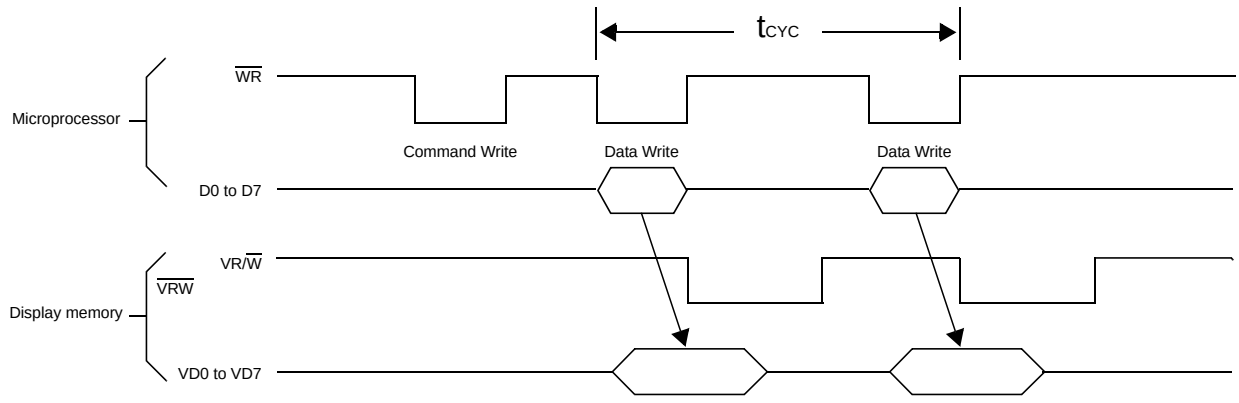


Fig.62 Display memory write cycle

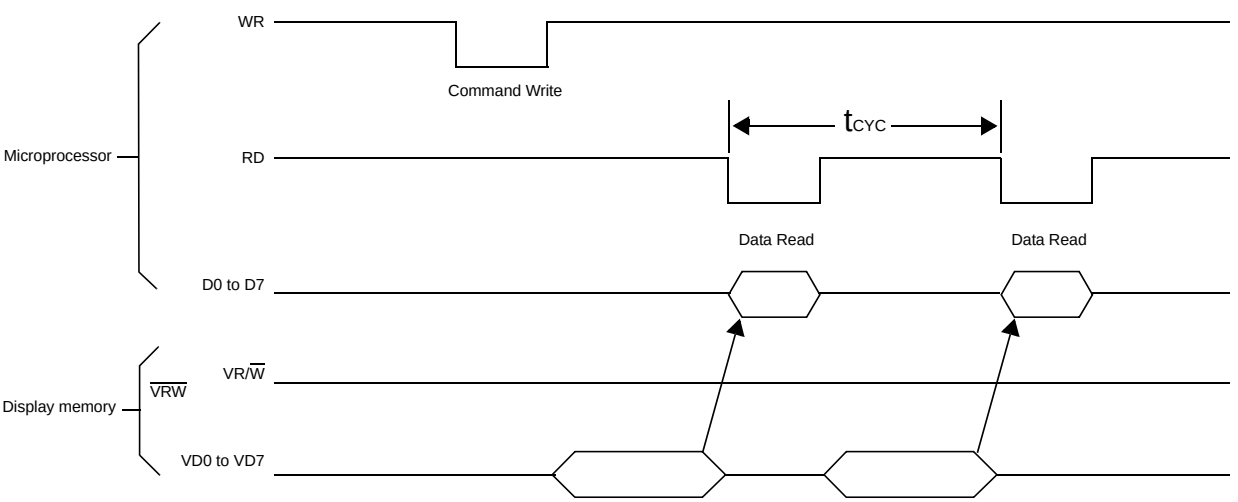


Fig.63 Display memory read cycle

Note:

A possible problem with the display memory read cycle is that the system bus access time, t_{ACC}, does not depend on the display memory access time, t_{ACV}. The microprocessor may only make repeated reads if the read loop time exceeds the SAP3305 series cycle time, t_{CYC}. If it does not, NOP instructions may be inserted in the program loop. t_{ACC}, t_{ACV} and t_{CYC} limits are given in section 6.3.

11.3 Interface Examples

11.3.1 Z80 TO SAP3305 SERIES INTERFACE

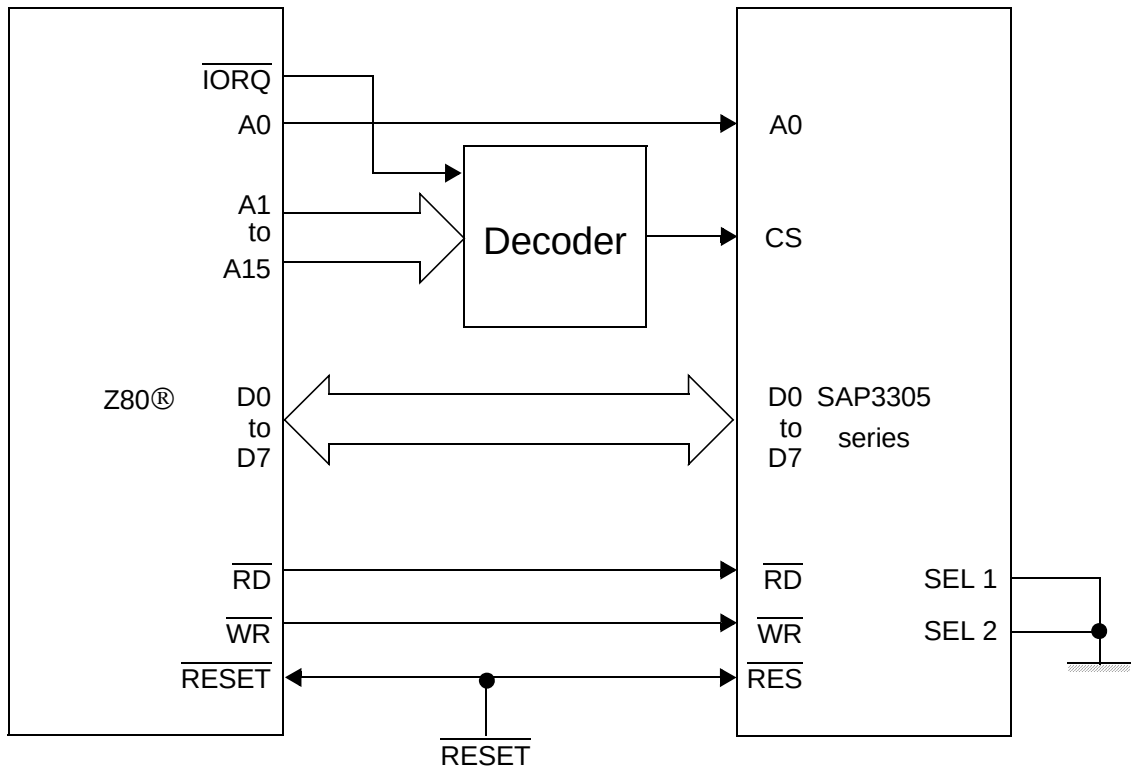


Fig.64 Z80® to SAP3305 series interface

Note:

Z80® is a registered trademark of Zilog Corporation

11.3.2 6802 TO SAP3305 SERIES INTERFACE

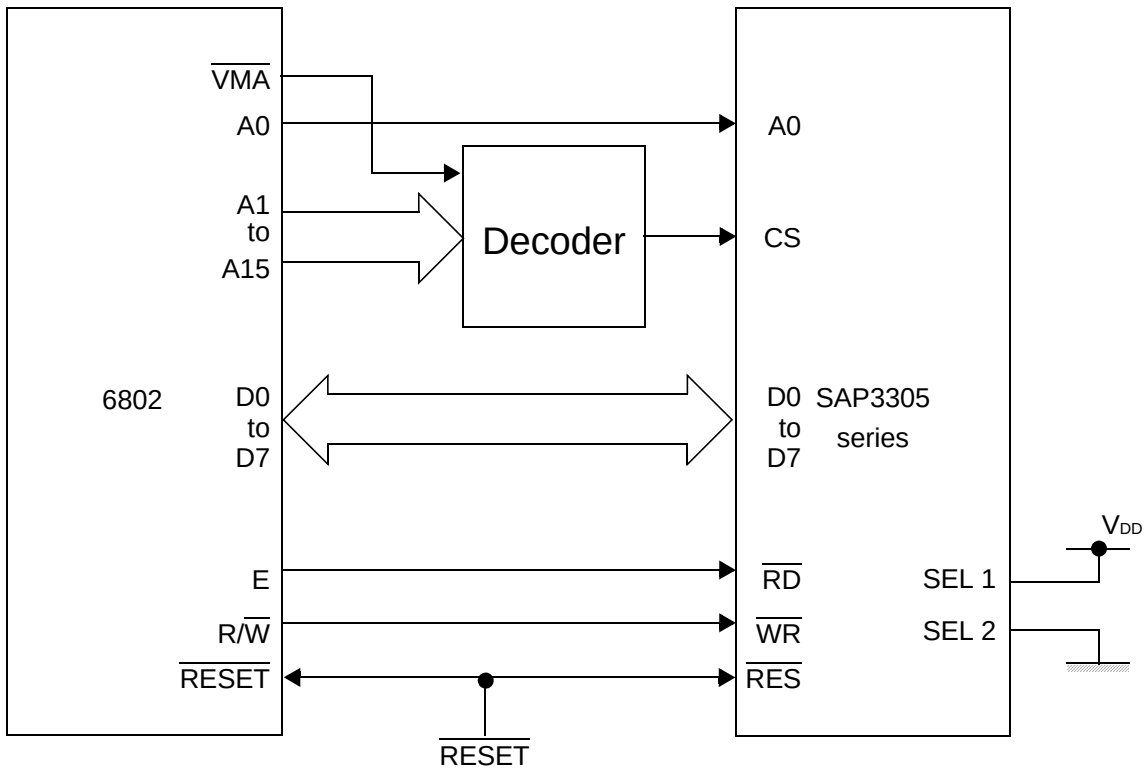


Fig.65 6802 to SAP3305 series interface

12 DISPLAY MEMORY INTERFACE

12.1 Static RAM

The figure below shows the interface between an 8K X 8 static RAM and the SAP3305 series. Note that bus buffers are required if the bus is heavily loaded.

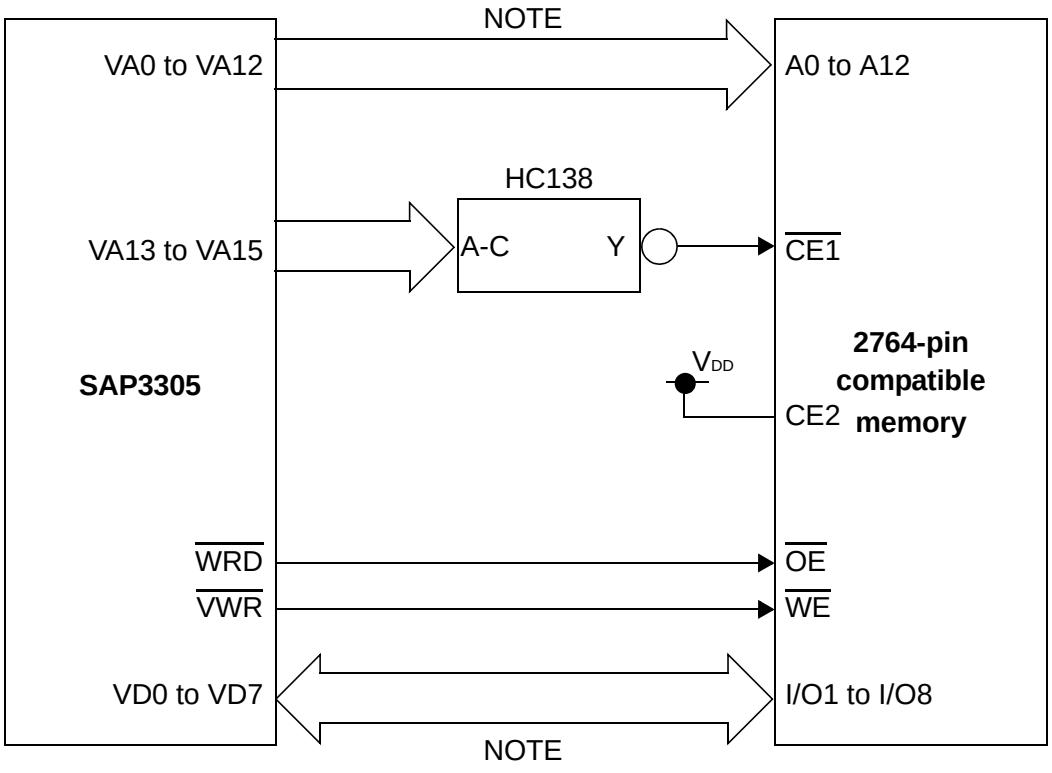


Fig.66 Static RAM interface

Note:

If the bus load is too much, use a bus buffer.

12.2 Supply Current during Display Memory Acess

The 24 address and data lines of the SAP3305 series cycle at one-third of the oscillator frequency, fosc .The charge and discharge current on these pins,I_{VOP} exeeeds I_{OPR}, it can be estimated by :

$$I_{VOP} \propto CVf$$

where C is the capacitance of the display memory bus, V is the operating voltage, and f is the operating frequency.

If VOPR =5.0V, f=1.0MHz, and the display memory bus capacitance is 1.0pF per line:

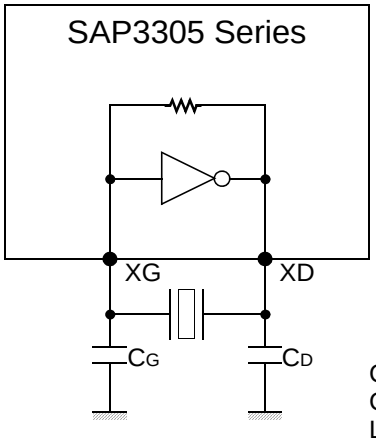
$$I_{VOP} \leq (120\mu A)/MHz \times pF$$

To reduce current flow during display memory accesses,it is important to use low-power memory , and to minimize both the number of devices and the parasitic capacitance.

13 OSCILLATOR CIRCUIT

The SAP3305 series incorporates an oscillator circuit. A stable oscillator can be constructed simply by connecting an AT-cut crystal and wo capacitors to XG and XD, as shown in the figure below. If the oscillator frequency is increased, C_D and C_G should be decreased proportionally.

Note that the circuit board lines to XG and XD must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.



C_G = 3 to 20 pF
C_D = 2 to 18 pF
Load impedance = 700Ω (max)

Fig.67 Crystal oscillator

14 STATUS FLAG

The SAP3305 series has a single bit status flag.

D6: X line standby

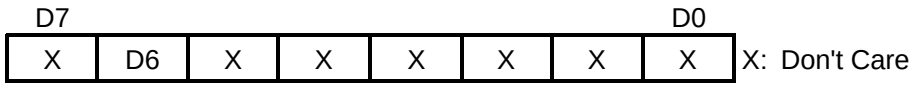


Fig.68 Status flag

The D6 status flag is HIGH for the TC/R-C/R cycles at the end of each line where the SAP3305 series is not reading the display memory. The microprocessor may use this period to update display memory without affecting the display, however it is recommended that the display be turned off when refreshing the whole display.

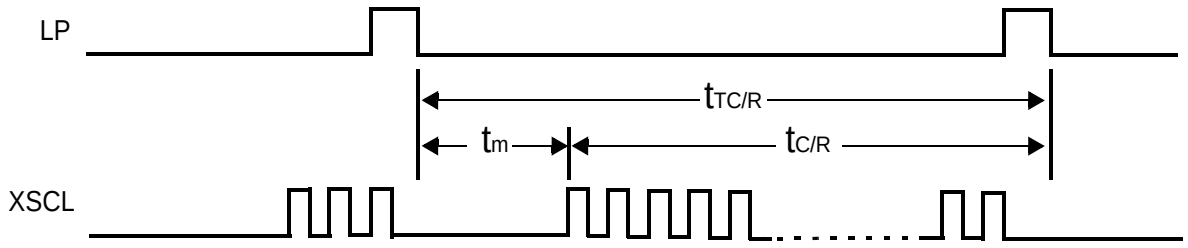


Fig.69 C/R to TC/R time difference

Table 44

$\overline{CS}$	A0	$\overline{RD}$	D6(FLAG)
0	0	0	0:Period of retrace lines 1:Period of display

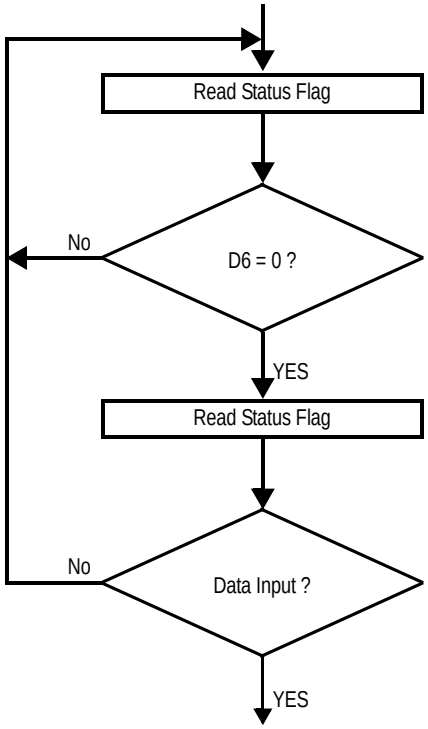


Fig.70 Flowchart for busy flag checking

- Precaution on the write timing to VRAM

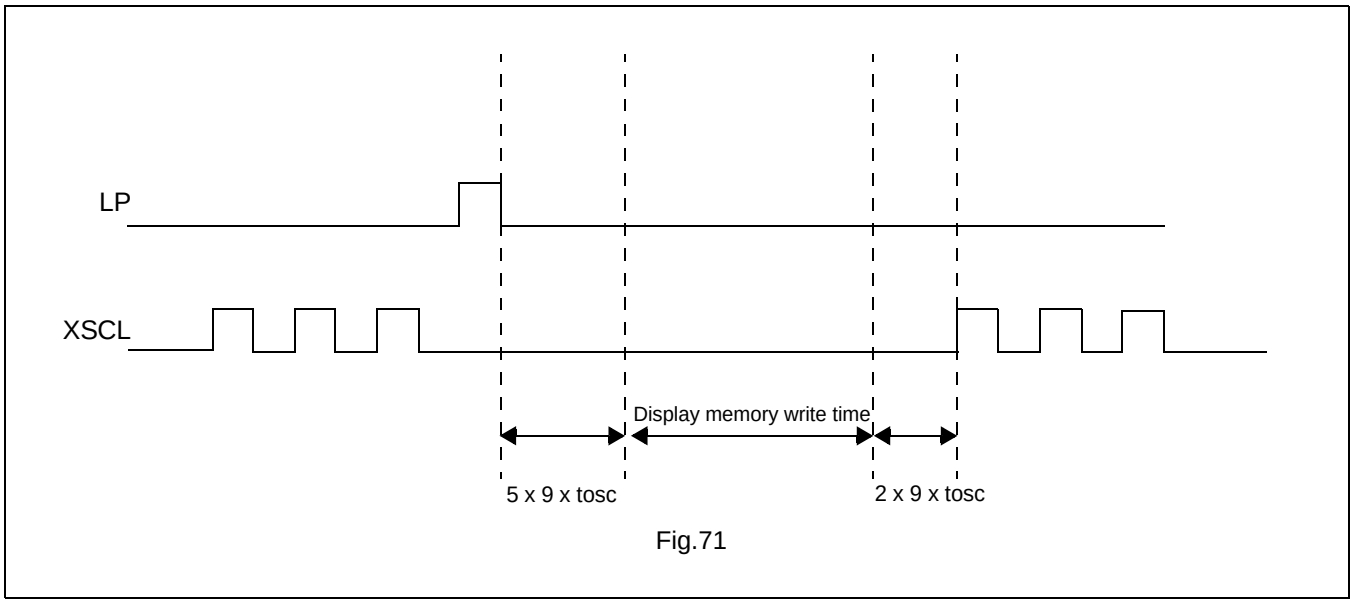


Fig.71

The allowable writing duration is since "5X9Xt_{OSC}" has elapsed(t_{OSC}=1/f_{OSC}: a cycle of the oscillation frequency)from the positive going edge of LP up to {(TCR)-(C/R)-7} X 9 X t_{OSC}.

Currently employed D6 status flag reading method does not idestify the timing when the read D6=Low took place. Thus, negative going edge of LP should be used as the interrupt signal when implementing the writing in above timing.

If you try to access the display memory in other timing than the above, flickering of the display screen will result.

15 RESET

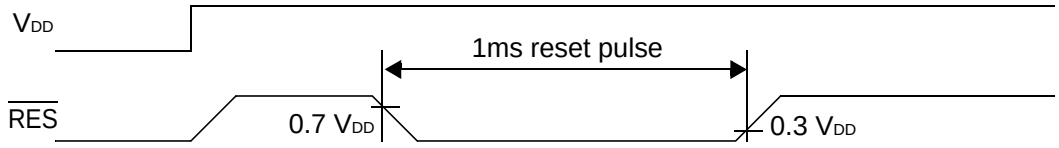


Fig.72 Reset timing

The SAP3305 series requires a reset pulse at least 1ms long after power-on in order to re-initialize its internal stste.

For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the SAP3305 series is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

The SAP3305 series cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset.During reset, the LCD drive signals XD, LP and FR are halted.

A delay of 3ms (maximum) is requires following the rising edges of both RES and V_{DD} to allow for system stabilization.

16 APPLICATION NOTES

16.1 Initialization Parameters

The parameters for the initialization commands must be determined first. Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example,[FX]=FX+1.

16.1.1 SYSTEM SET INSTRUCTION AND PARAMETERS

- FX

  The horizontal character field size is determined from the horizontal display size in pixels [VD]and the number of characters per line [VC].

  $[VD]/[VC] \leq [FX]$

- C/R

  C/R can be determned from VC and FX.

  $[C/R] = RND([FX]/8) \times [VC]$

  where RND(x) denotes X rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters.

- TC/R

  TC/R must satisfy the condition $[(TC)/R] \geq [C/R] + 4$.

- fOSC and fFR

  Once TC/R has been set, the frame frequency,fFR,and lines per frame [L/F] will also have been set. The lower limit on the oscillator frequency fOSC is given by:

  $f_{OSC} \geq ([(TC)/R] \times 9 + 1) \times [L/F] \times f_{FR}$

- If no standard crystal close to the calculated value of f_{OSC} exists, a higher frequency crystal can be used and the value of TC/R revised using the above equation.
- Symptoms of an ncorrect TC/R setting are listed below. If any of these appears, check the value of TC/R and modify it if necessary.
  - Vertical scanning halts and a high-contrast horizontal line appears.
  - All pixels are on or off.
  - The LP output signal is absent or corrupted.
  - The display is unstable.

Table 45 AVANT LCD unit example parameters

Product name and resolution(X x Y)	[FX]	[FY]	[C/R]	TC/R	f_{OSC}[MHz] See note 2.
256 x 64	[FX]=6 pixels: 256/6=42 remainder 4 =4 blank pixels	8 or 16, depending on the screen	[C/R]=42=2AH bytes: C/R=29H. When using HDOT SCR,[C/R]=43 bytes	2DH	1.85
512 x 64	[FX]=6 pixels: 512/6=85 remainder 2 =2 blank pixels	8 or 16, depending on the screen	[C/R]=85=55H bytes: C/R=54H. When using HDOT SCR,[C/R]=86 bytes	58H	3.59
256 x 128	[FX]=8 pixels: 256/8=32 remainder 0 =no blank pixels	8 or 16, depending on the screen	[C/R]=32=20H bytes: C/R=19H. When using HDOT SCR,[C/R]=33bytes	22H	2.90
512 x 128	[FX]=10 pixels: 512/10=51 remainder 2 =2 blank pixels	8 or 16, depending on the screen	[C/R]=102=66H bytes: C/R=65H. When using HDOT SCR,[C/R]=103 bytes	69H	8.55

Note:

1. The remainder pixels on the right-hand side of the display are automatically blanked by the SAP3305.There is no need to zero the display memory corresponding to these pixels.
2. Assuming a frame frequency of 60 Hz.

16.1.2 INITIALIZATION EXAMPLE

The initialization example shown in Figure 73 is for a SAP3305 series with an 8-bit microprocessor interface bus and an Epson EG4810S-AR display unit(512x128 pixels).

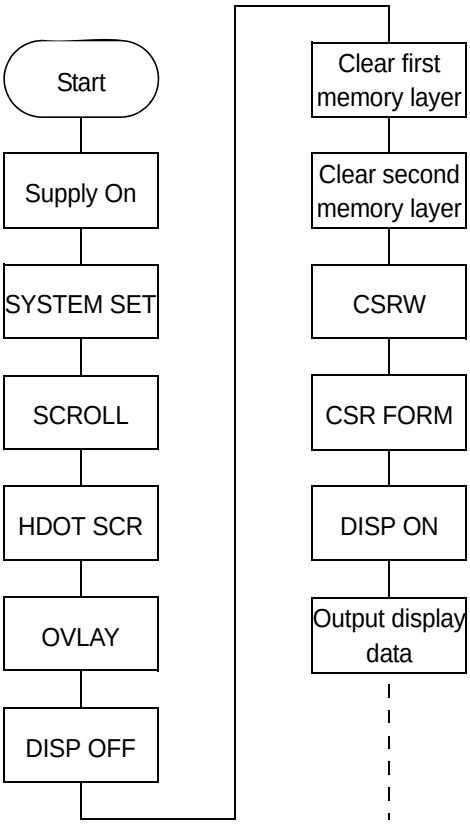


Fig.73 Initialization procedure

Note:

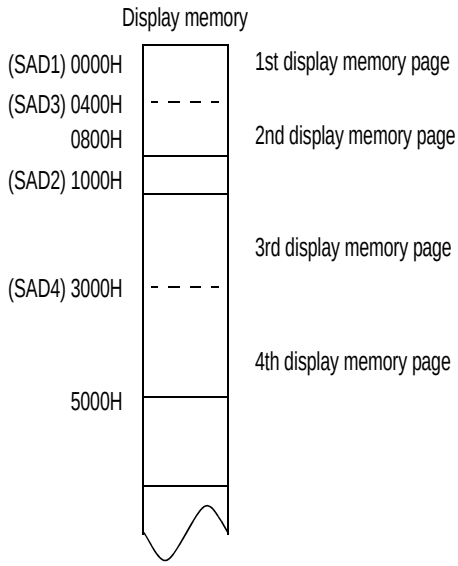
Set the cursor address to the start of each screen's layer memry, and use MWRITE to fill the memory with space characters, 20H(text screen only) or 00H(graphics screen only).Determining which memory to clear is explained in section 16.1.3.

Table 46 Initialization procedure

NO.	Command	Operation
1	Power-up	
2	Supply	
3	SYSTEM SET	
	C=40H	
	P1=38H	M0:Internal CG ROM
		M1:CG RAM is 32 characters maximum
		M2:8 lines per character
		W/S:Two-panel drive
		IV:No top-line compensation
	P2=87H	FX:Horizontal character size=8 pixels
		WF:Two-frame AC drive
	P3=07H	FY:Vertical character size=8 pixels
	P4=3FH	C/R:64 display address per line
	P5=49H	TC/R: Total address range per line =90
		f_{OSC}=6.0 MHz, f_{FR}=70Hz
	P6=7FH	L/F: 128 display lines
	P7=80H	AP:Virtual screen horizontal size is 128 address
	P8=00H	
4	SCROLL	
	C=44H	
	P1=00H	First screen block start address
	P2=00H	Set to 0000H
	P3=40H	Display lines in first screen block=64
	P4=00H	Second screen block start address
	P5=10H	Set to 1000H
	P6=40H	Display lines in second screen block=64
	P7=00H	Third screen block start address
	P8=04H	Set to 0400H
	P9=00H	Fourth screen block start address
	P10=30H	Set to 3000H

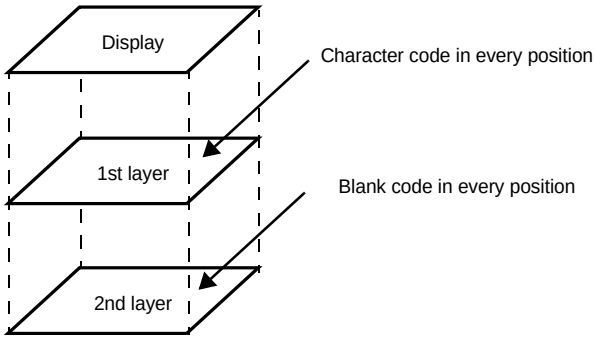
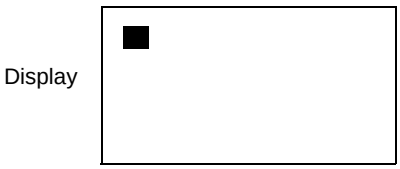
(continued)

Table 47 Initialization procedure(continued)

NO.	Command	Operation
		
		Fig.74 Display memory
5	HDOT SCR	
	C=5AH	
	P1=00H	Set horizontal pixel shift to zero
6	OVLAY	
	C=5BH	
	P1=01H	MX 1,MX 0:Inverse video superposition
		DM 1:First screen block is text mode
		DM 2:Third screen block is text mode
7	DISP ON/OFF	
	C=58H	D:Display OFF
	P1=56H	FC1,FC0:Flash cursor at 2 Hz
		FP1,FP0:First screen block ON
		FP3,FP2:Second and fourth screen blocks ON
		FP5,FP4:Third screen block ON
8	Clear data in first layer	Fill first screen layer memory with 20H(space charcter)

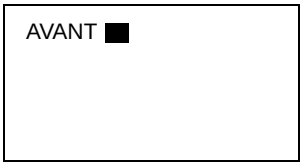
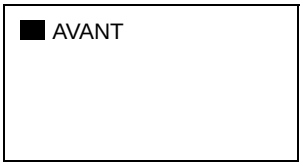
(continued)

Table 48 Initialization procedure(continued)

NO.	Command	Operation
9	Clear data in second layer	Fill second screen layer memory with 00H(blank data)
		
		Fig.75 Fill second screen layer memory with 00H(blank data)
10	CSRW	
	C=46H	
	P1=00H	Set cursor to start of first screen block
	P2=00H	
11	CSR FORM	
	C=5DH	
	P1=04H	CRX:Horizontal cursor size = 5 pixels
	P2=86H	CRY:Vertical cursor size = 7 pixels
		CM:Block cursor
12	DISP ON/OFF	
	C=59H	Display ON
		
		Fig.76
13	CSR DIR	
	C=4CH	Set cursor shift direction to right

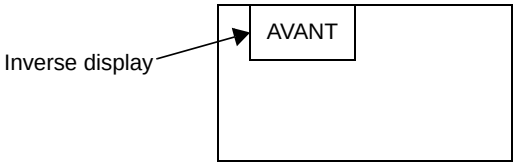
(continued)

Table 49 Initialization procedure(continued)

NO.	Command	Operation
14	MWRITE	
	C=42H	
	P1=20H	' '
	P2=45H	'A'
	P3=50H	'V'
	P4=53H	'A'
	P5=4FH	'N'
	P6=4EH	'T'
		 Fig.77
15	CSRW	
	C=46H	
	P1=00H	Set cursor to start of second screen block
	P2=00H	
16	CSR DIR	
	C=4FH	Set cursor shift direction to down
17	MWRITE	
	C42H	
	P1=FFH	Fill in a square to the left of the 'A'
	↓	
	P9=FFH	 Fig.78
18	CSRW	
	C=46H	
	P1=01H	Set cursor address to 1001H
	P2=10H	
19	MWRITE	
	C=42H	

(continued)

Table 50 Initialization procedure(continued)

NO.	Command	Operation
	P1=FFH	Fill in the second screen block in the second column of line 1
	↓	
	P9=FFH	
20	CSRW	Repeat operations 18 and 19 to fill in the background under
↓		'AVANT'
29	MWRITE	
		
		Fig.79
30	CSRW	
	C=46H	
	P1=00H	Set cursor to line three of the first screen block
	P2=01H	
31	CSR DIR	
	C=4CH	Set cursor shift direction to right
32	MWRITE	
	C42H	
	P1=44H	'D'
	P2=6FH	'o'
	P3=74H	't'
	P4=20H	' '
	P5=4DH	'M'
	P6=61H	'a'
	P7=74H	't'
	P8=72H	'r'
	P9=69H	'i'
	P10=78H	'x'
	P11=20H	' '
	P12=4CH	'L'
	P13=43H	'C'
	P14=44H	'D'

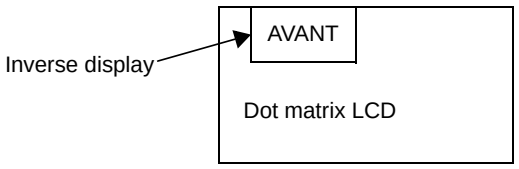


Fig.80

16.1.3 DISPLAY MODE SETTING EXAMPLE 1: COMBINING TEXT AND GRAPHICS

- Condictions
  - 320 x 200 pixels,single-panel drie (1/200 duty cycle)
  - First layer: text display
  - Second layer : gtaphics display
  - 8 x 8-pixel chaacter font
  - CG RAM not required
- Display memory allocation
  - First layer (text): 320/8 =40 characters per line,200/8=25 lines. Required memory size =40x25=1000 bytes.
  - Second layer (graphics):320/8=40 characters per line, 200/1 =200 lines. Required memory size =40x200=8000 bytes.

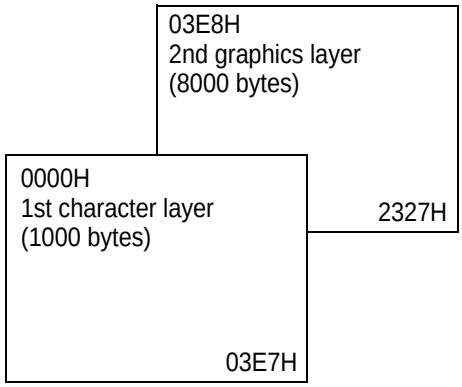


Fig.81 Character over graphics layers

● Register setup procedure

SYSTEM SET TC/R calculation
C = 40H
P1= 30H fOSC = 6 MHz
P2= 87H fFR = 70 Hz
P3= 07H
P4= 27H (1/6)x9x[TC/R]x200 = 1/70
P5= 2FH [TC/R]= 48, so TC/R= 2FH
P6= C7H
P7= 28H
P8= 00H

SCROLL
C = 44H
P1= 00H
P2= 00H
P3= C8H
P4= E8H
P5= 03H
P6= C8H
P7= XH
P8= XH
P9= XH
P10= XH

CSR FORM
C = 5DH
P1= 04H
P2= 86H

HDOT SCR
C = 5AH
P1= 00H

OVLAY
C = 5BH
P1= 00H

DISP ON/OFF
C = 59H
P1= 16H
X = Don't care

16.1.4 DISPLAY MODE SETTING EXAMLE 2: COMBINING GRAPHICS AND GRAPHICS

- Condictions
  - 320 x 200 pixels, single-panel drive(1/200 duty cycle)
  - First layer: graphics display
  - Second layer: graphics display
- Display memory allocation
  - First layer(graphics):320/8 =40 characters per line, 200/1 =200 lines. Required memory size= 40x200= 8000 bytes.
  - Second layer(graphics):320/8= 40 characters per line, 200/1 =200 lines. Required memory size = 8000 bytes.

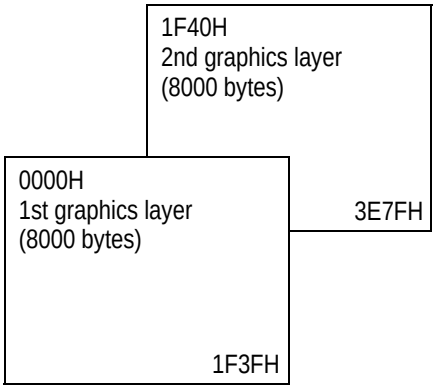


Fig.82 Two-layer graphics

● Register setup procedure

SYSTEM SET TC/R calculation
C = 40H
P1= 30H fOSC = 6 MHz
P2= 87H fFR = 70 Hz
P3= 07H
P4= 27H (1/6)x9x[TC/R]x200 = 1/70
P5= 2FH [TC/R]= 48, so TC/R= 2FH
P6= C7H
P7= 28H
P8= 00H

SCROLL
C = 44H
P1= 00H
P2= 00H
P3= C8H
P4= 40H
P5= 1FH
P6= C8H
P7= XH
P8= XH
P9= XH
P10= XH

CSR FORM
C = 5DH
P1= 07H
P2= 87H

HDOT SCR
C = 5AH
P1= 00H

OVLAY
C = 5BH
P1= 00H

DISP ON/OFF
C = 59H
P1= 16H
X = Don't care

16.1.5 DISPLAY MODE SETTING EXAMLE 3: COMBINING THREE GRAPHICS LAYERS

- Condictions
  - 320 x 200 pixels, single-panel drive(1/200 duty cycle)
  - First layer: graphics display
  - Second layer: graphics display
  - Third layer: graphics display
- Display memory allocation
  - All layer(graphics):320/8 =40 characters per line, 200/1 =200 lines. Required memory size= 40x200= 8000 bytes.

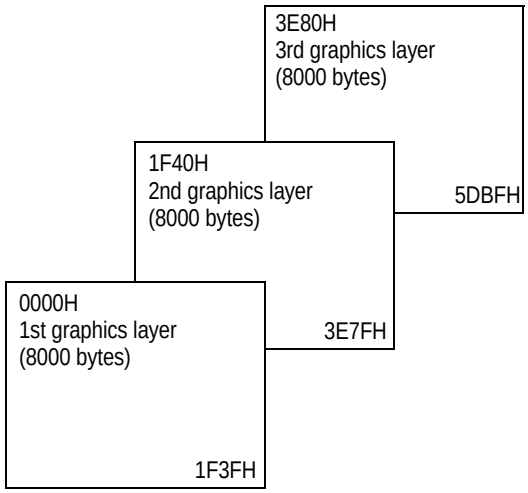


Fig.83 Three-layer graphics

● Register setup procedure

SYSTEM SET TC/R calculation
C = 40H
P1= 30H fOSC = 6 MHz
P2= 87H fFR = 70 Hz
P3= 07H
P4= 27H (1/6)x9x[TC/R]x200 = 1/70
P5= 2FH [TC/R]= 48, so TC/R= 2FH
P6= C7H
P7= 28H
P8= 00H

SCROLL
C = 44H
P1= 00H
P2= 00H
P3= C8H
P4= 40H
P5= 1FH
P6= C8H
P7= XH
P8= XH
P9= XH
P10= XH

CSR FORM
C = 5DH
P1= 07H
P2= 87H

HDOT SCR
C = 5AH
P1= 00H

OVLAY
C = 5BH
P1= 00H

DISP ON/OFF
C = 59H
P1= 16H
X = Don't care

16.2 System overview

Figure 61 shows the SAP3305 series in a typical system.The microprocessor issues instructions to the SAP3305 series, and the SAP3305 series drives the LCD panel and may have up to 64KB of display memory .Since all of the LCD control circuits are integrated onto the SAP3305 series, few external components are required to construct a complete medium-resolution liquid crystal display.

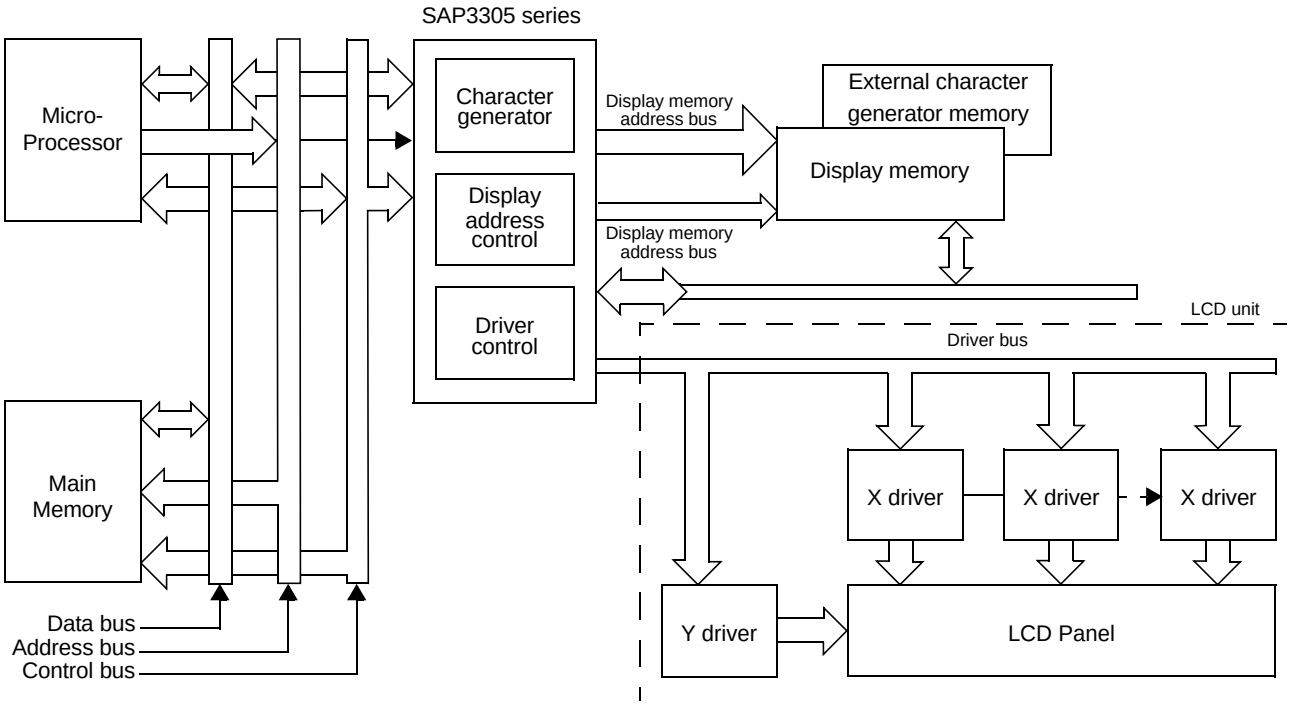


Fig.84 System block diagram

16.3 System interconnection

16.3.1 SAP3305

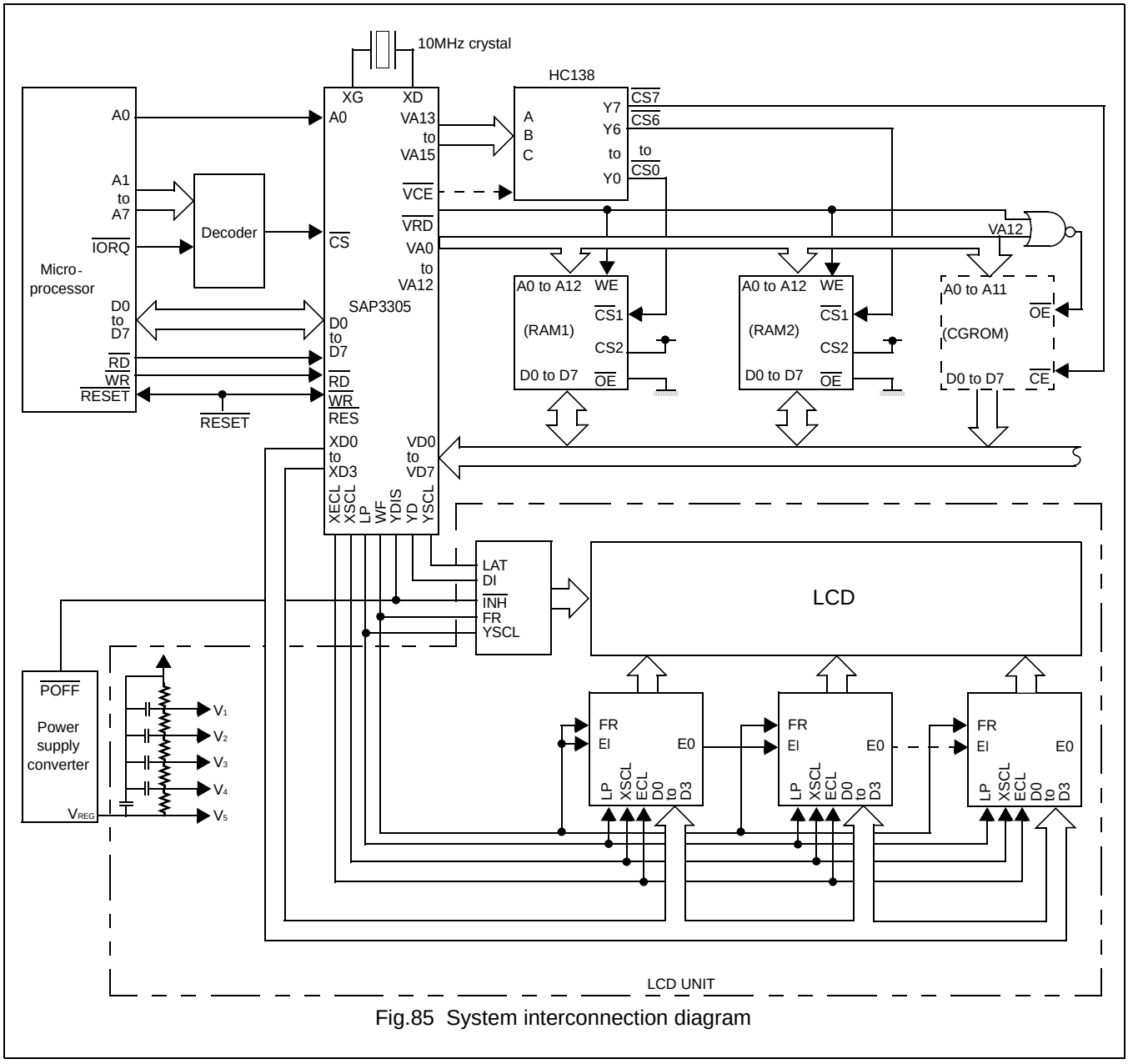


Fig.85 System interconnection diagram

The SAP3305 series layeres screens and flexible scrolling facilities support a range of display functions and reduces the load on the controlling microprocessor when displaying unferlining, inverse display, text overlaid on graphics or simple animation. These facilities are supported by the SAP3305 series ability to drivde display memory into up to four different areas.

- Character code table
  - Contains character codes for text display
  - Each character requires 8 bits
  - Table mapping can be changedby using the scroll start function
- Graphics data table

  - Contains graphics bitmaps
  - Word length is 8 bits
  - Table mapping can be changed
- CG RAM table
  - Character generator memory can be modified by the external microprocessor
  - Character sizes up to 8 x 16-pixels(16 bytes per charcter)
  - Maxinum of 64 characters
  - Table mapping can be changed
- CG ROM table
  - Used when the internal character generator is not adequate
  - Can be used in conjunction with the internal character generator and external character generator RAM
  - Character size up to 8 x 16-pixels(16 bytes per character)
  - Maximum of 256 characters
  - Fixed mapping at F000H to FFFFH

16.4 Smooth Horizontal Scrolling

Figure 86 illustrates smooth display scrolling to the left.When scrolling left, the screen is effectively moving to the right, overthe larger virtual screen. Instead of changing the display start address SAD and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the pixel-shift parameter of the HDOT SCR command. When the display has been scrolled seven pixels, the HDOT SCR pixel-shift parameter is reset to zero and SAD incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling.

To scroll the display to the right, the reverse procedure is followed.

When the edge of the virtual screen is reached, the microprocessor must take approriate steps so that the display is not corrupted. The scroll must be stopped or the display modified.Note that the HDOT SCR command cannot be used to scroll indivdual layers.

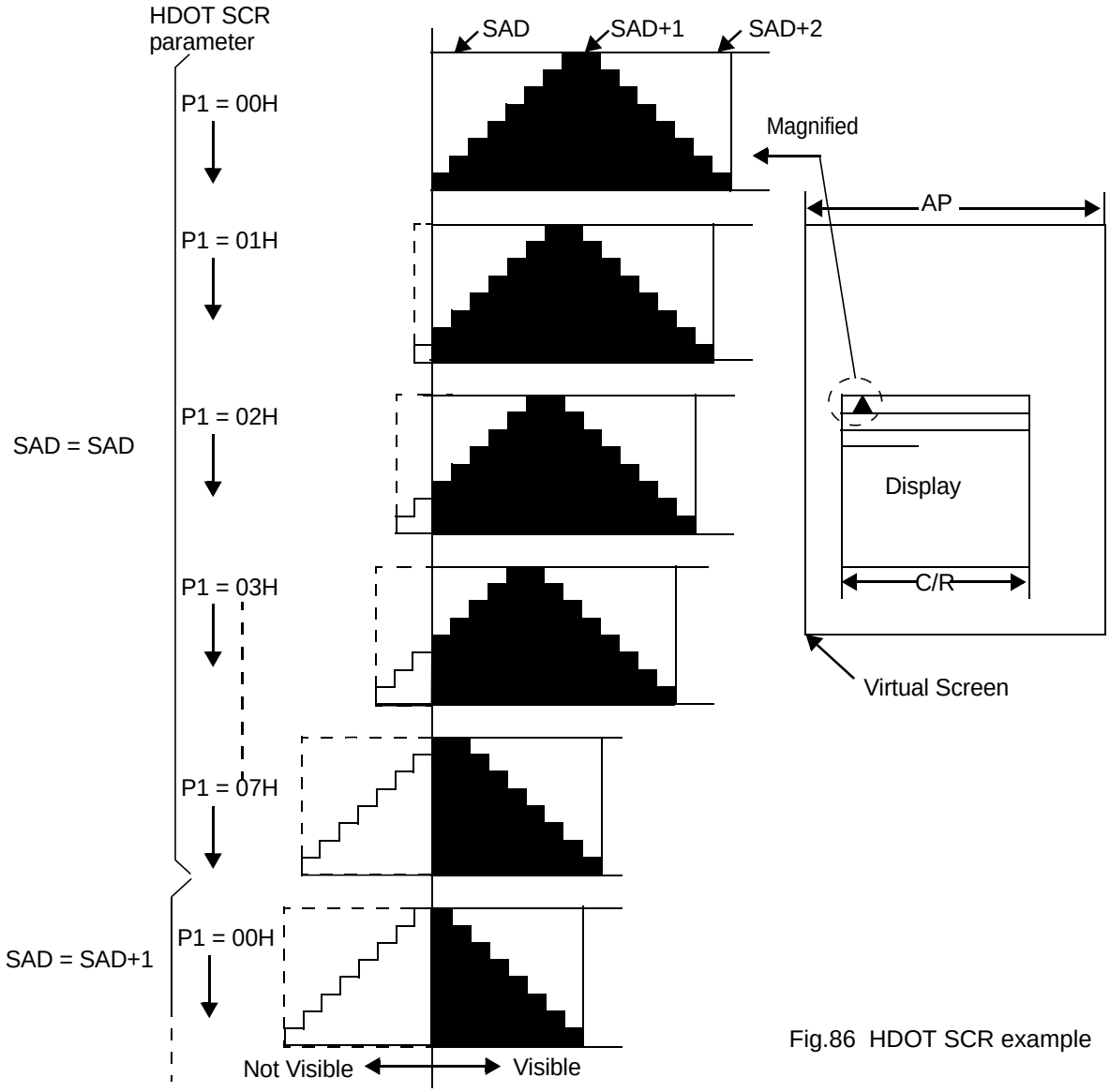


Fig.86 HDOT SCR example

Note: The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

16.5 Layered Display Attributes

SAP3305 series incorporates a number of functions for enhanced displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas.These functions are controlled by the OVLAY and DISP ON/OFF commands.

Attribute	MX1	MX0	Combined layer display	1st layer display	2nd layer display
Reverse	0 1	1 1	IV AVANT	IV AVANT	
Half-tone	0 1	0 1	ME Yes, No	ME Yes, No	
Local flashing	0 0	0 1	BL Error	BL	Error
Ruled line	0 0 1	0 1 1	LINE RL LINE	LINE RL LINE	

Fig.87 Layer synthesis

A number of means can be used to achieve these effects, depending on the display configuration. These are listed below. Note, however, that not all of these can be used in the one layer at the same time.

16.5.1 INVERSE DISPLAY

The first layer is text, the second layer is graphics.

1. CSRW, CSDIR, MWRITE

   Write is into the graphics screen at the area to be inverted.

2. OVLAY:MX0=1,MX1=0

   Set the combination of the two layers to Exclusive-OR.

3. DISP ON/OFF:FP0=FP1=1,FP1=FP3=0.

   Turn on layers 1 and 2.

16.5.2 HALF-TONE DISPLAY

The FP parameter can be used to generate half-intensity display by flashing the display at 17 Hz. Note that this mode of operation may cause flicker problems with certain LCD panels.

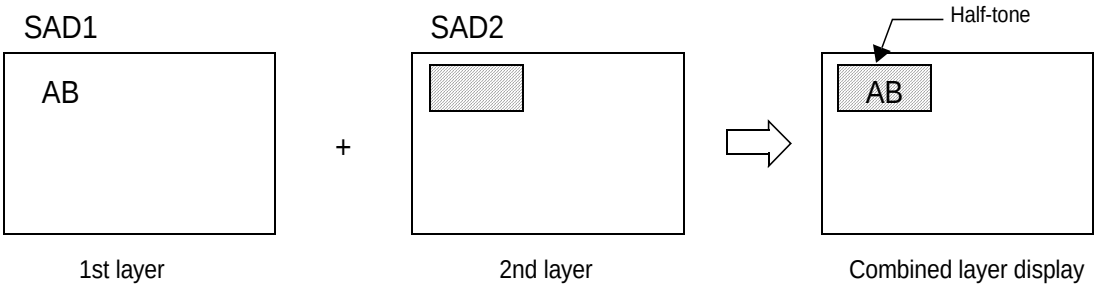


Fig.88 Half-tone character and graphics

16.5.2.1 Menu pad display

Turn flashing off for the first layer, on at 17 Hz for the second layer, and combine the screens using the OR function.

1. OVLAY:P1=00H
2. DISP ON/OFF:P1=34H

16.5.2.2 Graph display

To present two overlaid grahs on the screen, configure the display as for the menu bar display and put one graph on each screen layer. The difference in contrast between the half-and full-intensity displays will make it easy to distinguish between the two graphs and help create an attractive display.

1. OVLAY:P1=00H
2. DISP ON/OFF:P1=34H

16.5.3 FLASHING AREAS

16.5.3.1 Small area

To flash selected characters, the MPU can alternately write the character as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

16.5.3.2 Large area

Divide both layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.

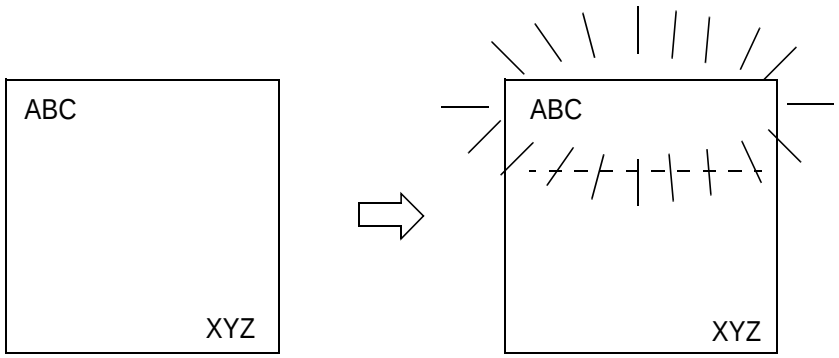


Fig.89 Localized flashing

16.6 16x16-dot Graphic Display

16.6.1 COMMAND USAGE

This example shows how to display 16 x 16-pixel characters. The command sequence is as follows:

CSRW : Set the cursor address.

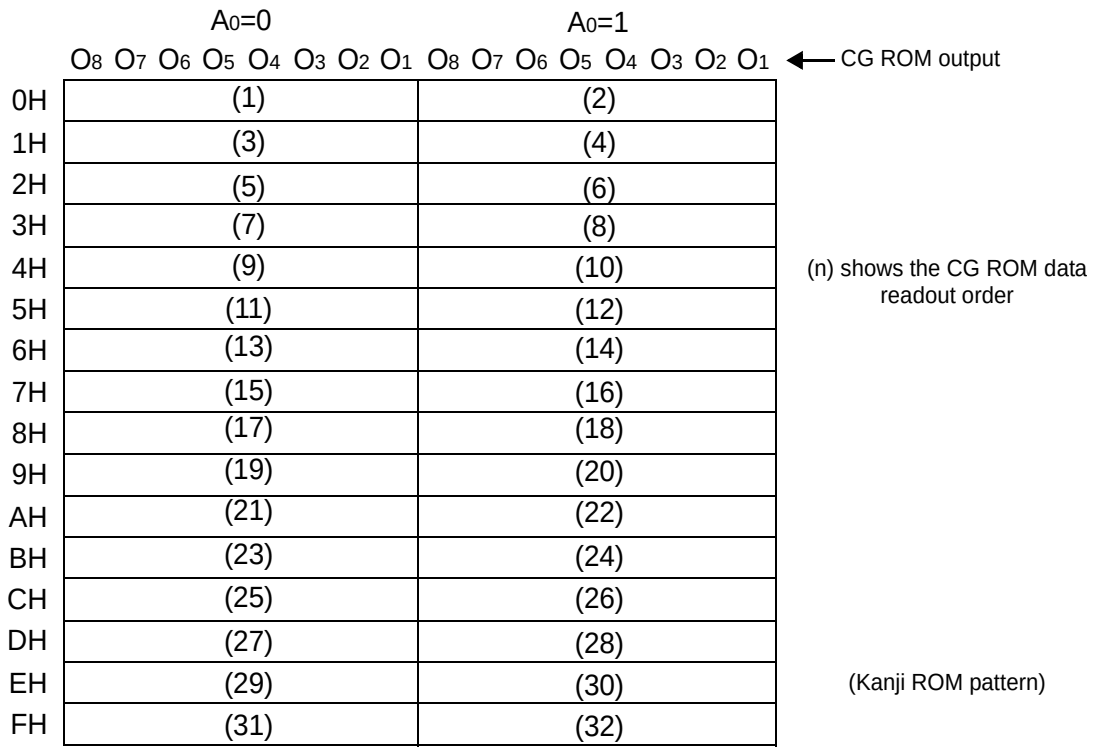
CSDIR : Set the cursor auto-increment direction.

MWRITE : Write to the display memory.

16.6.2 KANJI CHARACTER DISPLAY

The program for writing large characters operates as follows:

1. The microprocessor reads the character data from its ROM.
2. The microprocessor sets the display address and writes to the VARM. The flowchart is shown in Figure 92.



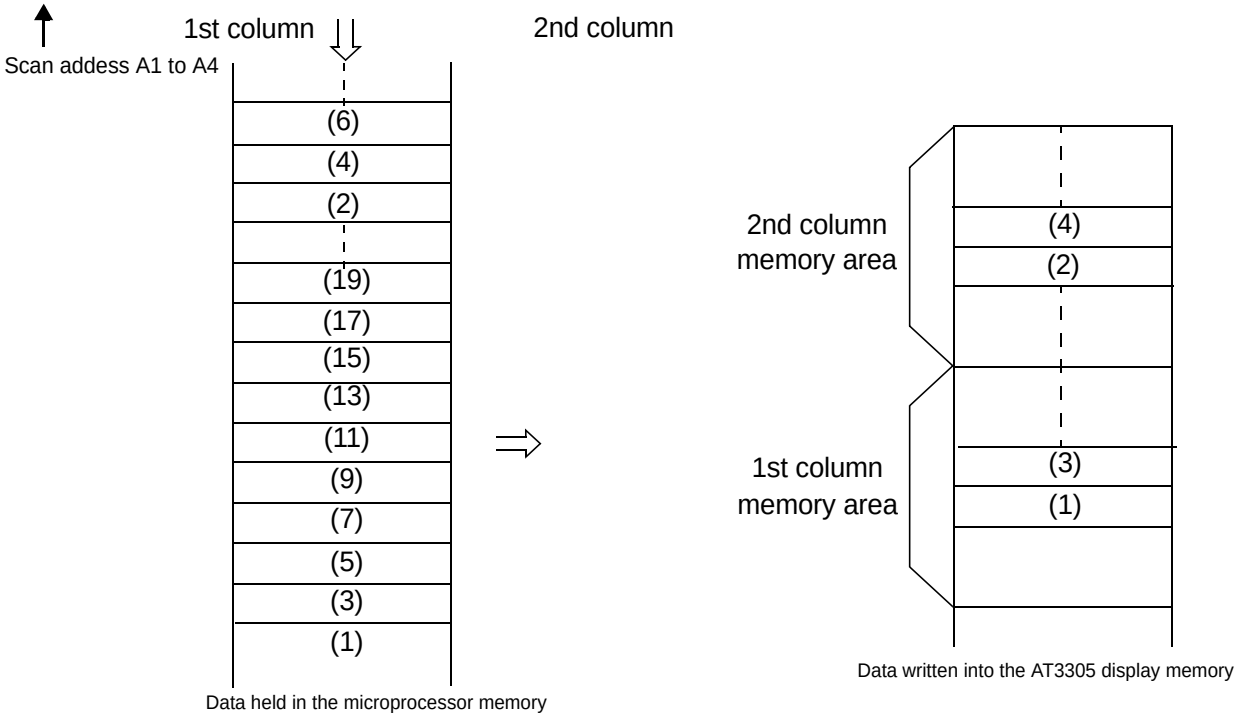
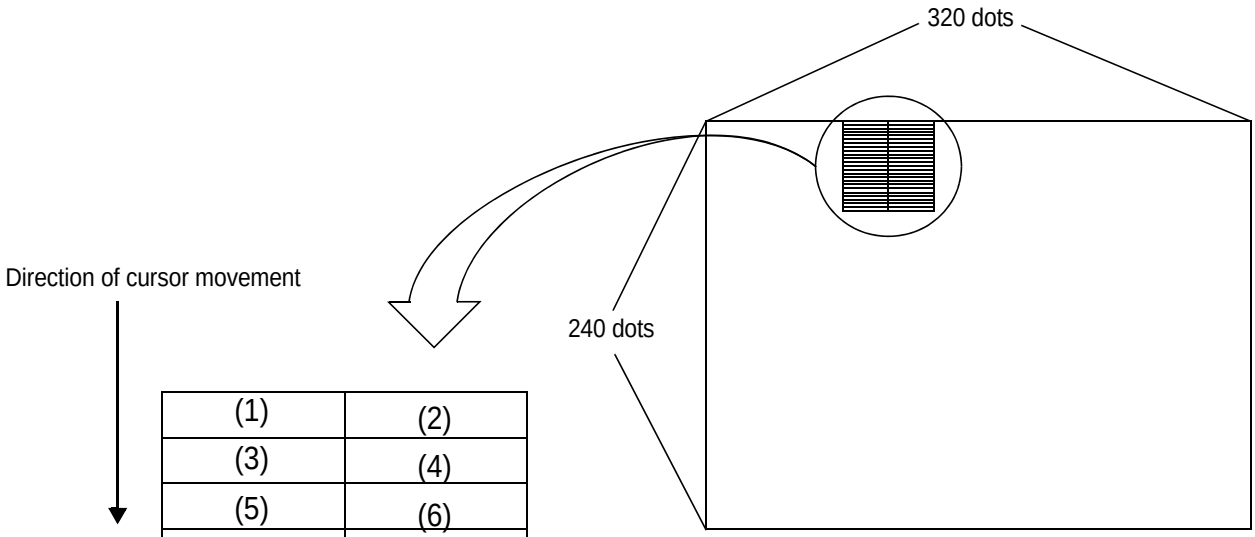


Fig.90 Graphics address indexing



(1)	(2)
(3)	(4)
(5)	(6)
(7)	(8)
(9)	(10)
(11)	(12)
(13)	(14)
(15)	(16)
(17)	(18)
(19)	(20)
(21)	(22)
(23)	(24)
(25)	(26)
(27)	(28)
(29)	(30)
(31)	(32)

Fig.91 Graphics bit map

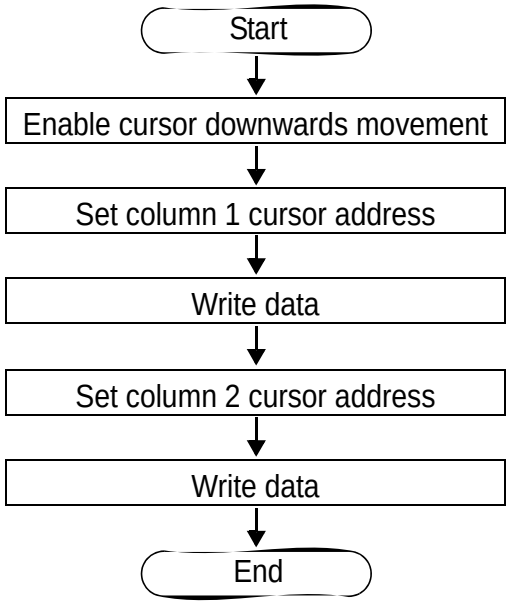


Fig.92 16 x16-dot display flowchart

Using an external character generator ROM, and 8 x 16-pixel font can be used, allowing a 16 x 16-pixel character to be displayed in two segments. The external CG ROM EPROM data format is described in Section 9.1. This will allow the display of up to 128, 16 x 16-pixel characters and 32 bank-switchable characters can also be supported.

17 INTERNAL CHARACTER GENERATOR FONT

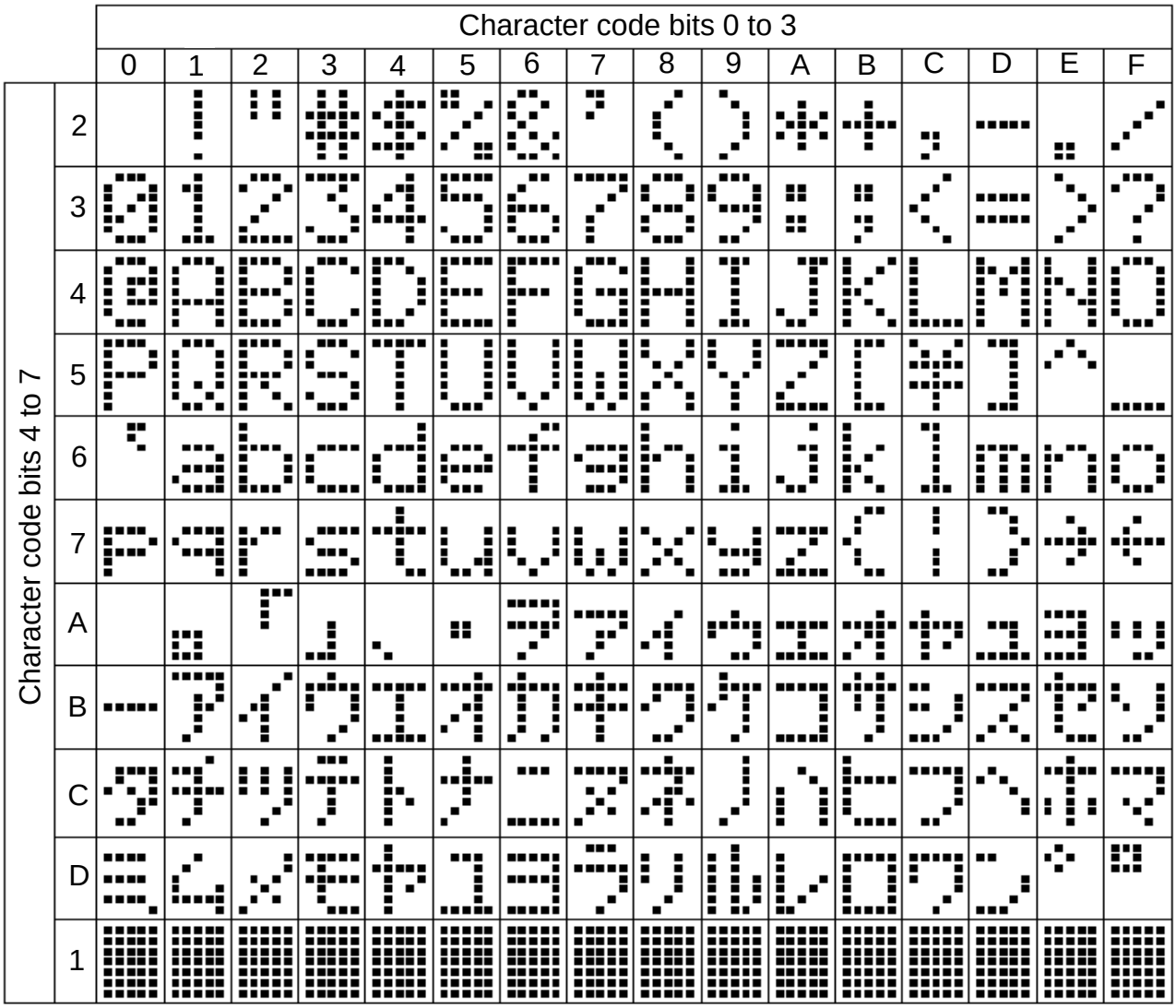


Fig.93 On-chip character set

Note

The shaded positions indicate chatacters that hace the whole 6 x 8 bitmap blackened.

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

18.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

18.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 LIFE SUPPORT APPLICATIONS

Avant's products, unless specifically specified, are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling Avant's products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.