EPSON
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S1D15722D01B000
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.1

NOTICE

Configuration of product number

●DEVICES

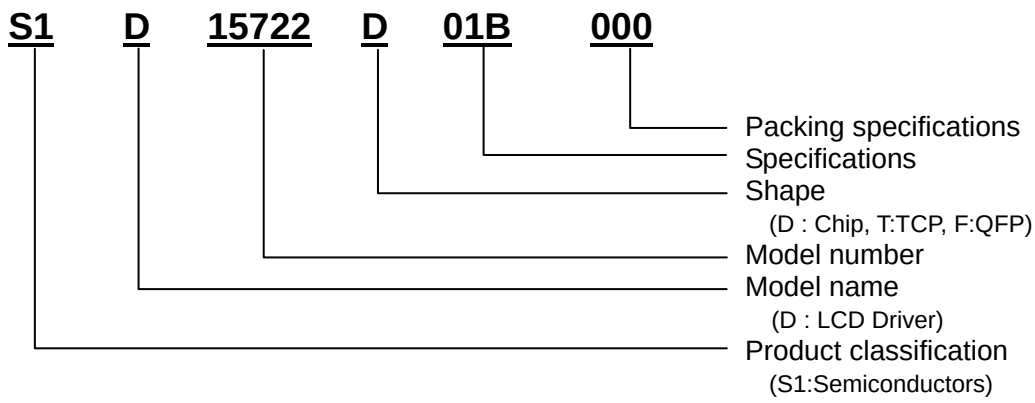


Table of Contents

1. DESCRIPTION

The S1D15722 series is a MLS drive system dot matrix LCD driver that can be directly connected to the microcomputer bus. An 8-bit parallel or serial display data sent from the microcomputer is stored in the built-in display data RAM and LCD drive signal is generated independently of the microcomputer. (Required external LCD bias voltages input.)

The S1D15722 series provides both FRM 4-grayscale display and binary display. With display data RAM 224 × 184 × 2 bits incorporated, for 4-grayscale display, 2 bits of built-in RAM correspond to 1 dot of pixel, and for binary display, 1 bit of the built-in RAM corresponds to 1 dot of pixel.

The S1D15722 series contains 184 circuits of common output and 224 circuits of segment output. This allows display of a maximum of 224 × 184 dots per chip.

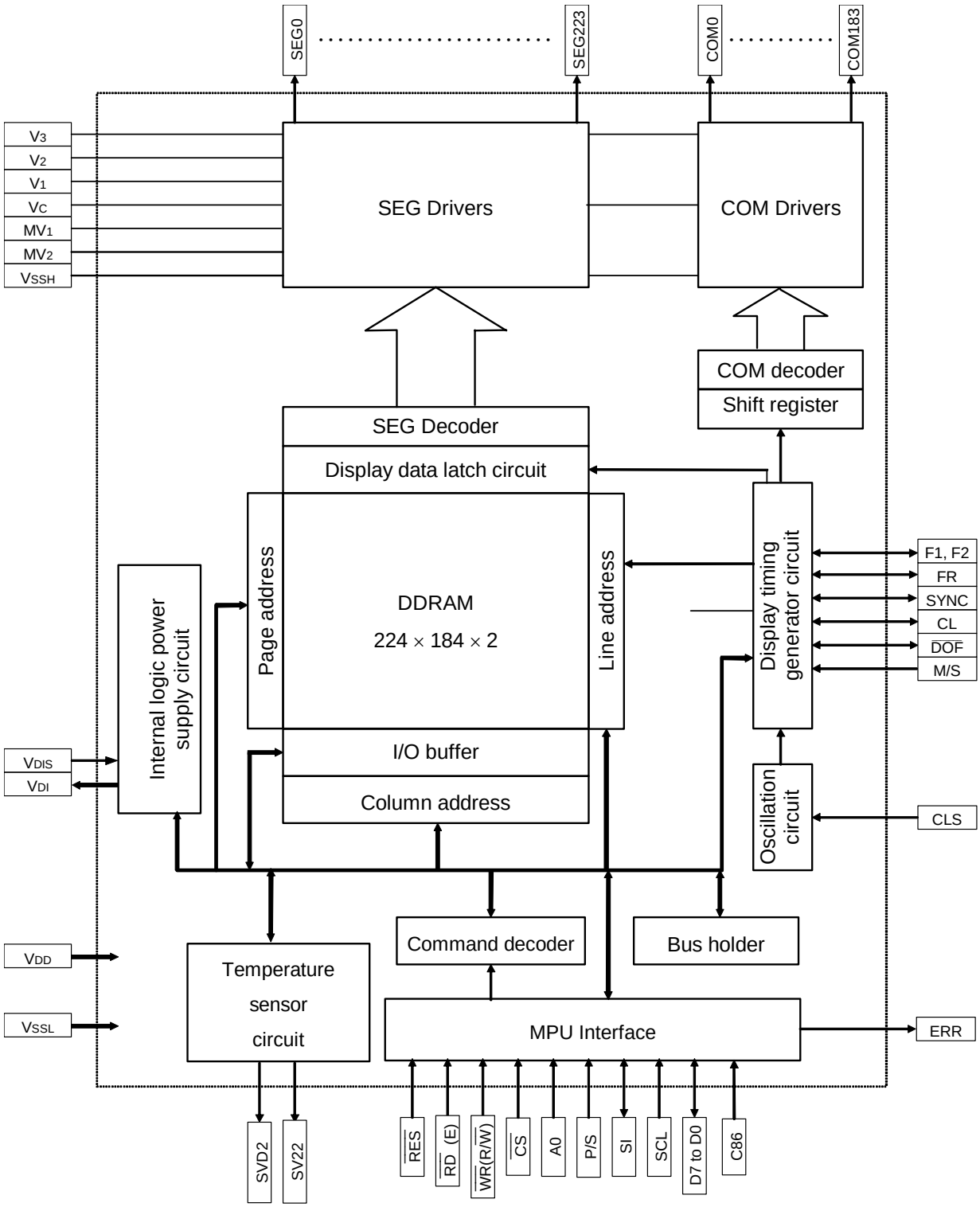
Read/write operation from microcomputer to display data RAM does not require external operation clock.

2. FEATURES

- Direct display of RAM data with display data RAM
  - For 4-grayscale display (normally white, normal display mode)
    RAM bit data (higher and lower)
    (1, 1): Level 3 of gray scale Black
    (1, 0): Level 2 of gray scale
    (0, 1): Level 1 of gray scale
    (0, 0): Level 0 of gray scale White
  - For binary display (Normally White, normal display mode)
    RAM bit data
    "1": ON Black
    "0": OFF White
- RAM capacity
  $184 \times 224 \times 2 = 82{,}432$ bits
- Liquid crystal drive circuit
  184 common output and 224 segment output
- Provides a high-speed 8-bit MPU interface (can be directly connected to MPU of both 80 and 68 series)/serial interface.
- Extensive command functions
  Display lines set, n-line inversion, display data RAM address control, gray scale control, display ON/OFF, display in forward/reverse direction, full display lighting ON/OFF, display clock built-in oscillation circuit control, select common output status, etc.
- Required external LCD bias voltages input
- Built-in high precision voltage adjustment function
  - Built-in high precision CR oscillation circuit
- Power supply:
  Logic power supply : V_{DD} - V_{SSL} = 3.0V to 5.5V
  (Internal logic is operated by V_{DI}-V_{SSL} ・・・ 2.85V typ.)
  LCD drive power supply: V_3 - V_{SSH} = 15V to 25V

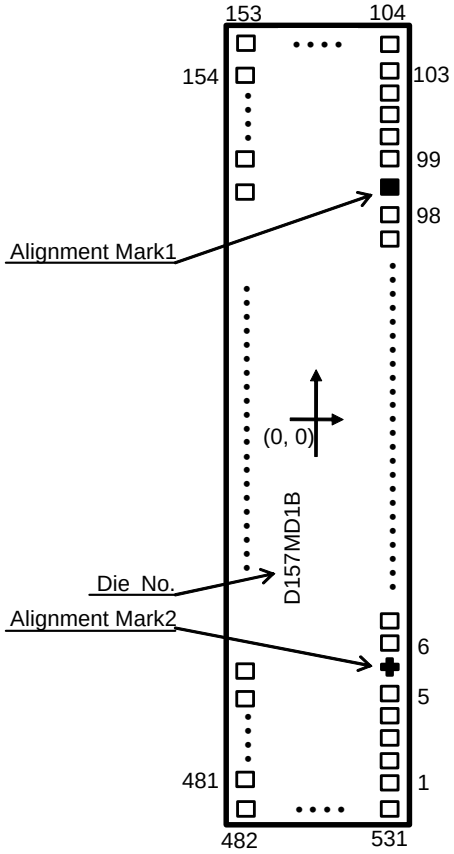
  (V_{SSL} = V_{SSH} = GND)
- Wide temperature range: - 40 to +90°C
- CMOS Process
- Shipping form: bare chip
- No anti-radiation and light resistance design

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT

4.1 Chip Assignment



Item		Size X		Size Y	Unit
Chip size		3.31	×	21.00	mm
Chip thickness		0.625			mm
Bump pitch		62 (Min.)			μm
Bump size PAD No.	1 to 5	45	×	85	μm
	6 to 17, 19 to 44, 83, 85 to 98	90	×	109	μm
	18, 48 to 82, 84	90	×	60	μm
	45 to 47	90	×	45	μm
	99 to 153	45	×	85	μm
	154 to 481	90	×	35	μm
	482 to 531	45	×	85	μm
Bump height		Typ. 17			μm

4.2 Alignment mark

Alignment coordinate

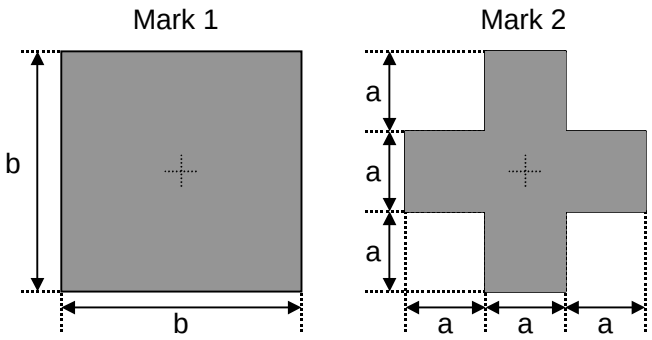
1 (1500.0, 9380.0) μm

2 (1500.0, -9380.0) μm

Mark size

a = 15 μm

b = 45 μm



4.3 Pad Center Coordinates

Unit : μm

PAD No.	Pin Name	X	Y
1	NC	1539.7	-10204.05
2	NC	1539.7	-10075.5
3	NC	1539.7	-9946.5
4	NC	1539.7	-9817.5
5	NC	1539.7	-9688.5
6	TEST3	1517.2	-9238.5
7	TEST3	↓	-9112.5
8	TEST4	↓	-8788.5
9	TEST4	↓	-8662.5
10	TEST5	↓	-8338.5
11	TEST5	↓	-8212.5
12	TEST6	↓	-7888.5
13	TEST6	↓	-7762.5
14	TEST7	↓	-7438.5
15	TEST7	↓	-7312.5
16	TEST8	↓	-6988.5
17	TEST8	↓	-6862.5
18	TEST9	↓	-6530.0
19	TEST10	↓	-6348.5
20	TEST10	↓	-6222.5
21	TEST11	↓	-5898.5
22	TEST11	↓	-5772.5
23	TEST12	↓	-5448.5
24	TEST12	↓	-5322.5
25	TEST9	↓	-4998.5
26	TEST9	↓	-4872.5
27	V_{DD2}	↓	-4510.7
28	V_{DD2}	↓	-4384.7
29	V_{DD2}	↓	-4258.7
30	V_{DD}	↓	-3926.7
31	V_{DD}	↓	-3800.7
32	V_{DD}	↓	-3674.7
33	V_{SSH}	↓	-3362.1
34	V_{SSH}	↓	-3236.1
35	V_{SSH}	↓	-3110.1
36	V_{SSH}	↓	-2984.1
37	V_{SSL}	↓	-2821.1
38	V_{SSL}	↓	-2695.1
39	V_{SSL}	↓	-2569.1
40	V_{SSL}	↓	-2443.1
41	V_{DI}	↓	-2280.1
42	V_{DI}	↓	-2154.1
43	V_{DD}	↓	-1841.5
44	V_{DD}	↓	-1715.5
45	TEST2	↓	-1440.0
46	SV22	↓	-1050.0
47	SVD2	↓	-800.0
48	V_{DIS}	↓	-600.0
49	V_{SSL}	↓	-510.0
50	SYNC	↓	-420.0

PAD No.	Pin Name	X	Y
51	FR	1517.2	-150.0
52	CL	↓	-60.0
53	$\overline{DOF}$	↓	210.0
54	F1	↓	300.0
55	F2	↓	570.0
56	V_{SSL}	↓	660.0
57	$\overline{CS}$	↓	750.0
58	$\overline{RES}$	↓	1020.0
59	A0	↓	1110.0
60	V_{SSL}	↓	1290.0
61	$\overline{WR}$,R/$\overline{W}$	↓	1380.0
62	$\overline{RD}$, E	↓	1650.0
63	VDD	↓	1740.0
64	SI	↓	1830.0
65	SCL	↓	2100.0
66	D0	↓	2190.0
67	D1	↓	2460.0
68	D2	↓	2550.0
69	D3	↓	2820.0
70	D4	↓	2910.0
71	D5	↓	3180.0
72	D6	↓	3270.0
73	D7	↓	3540.0
74	V_{DD}	↓	3630.0
75	M/S	↓	3720.0
76	CLS	↓	3990.0
77	VSSL	↓	4080.0
78	TEST	↓	4260.0
79	C86	↓	4350.0
80	P/S	↓	4620.0
81	V_{DD}	↓	4710.0
82	ERR	↓	4800.0
83	V_{SSH}	↓	5051.5
84	TEST13	↓	5210.0
85	TEST14	↓	5371.5
86	TEST15	↓	5701.5
87	TEST15	↓	5827.5
88	TEST16	↓	6159.5
89	TEST16	↓	6285.5
90	TEST17	↓	6613.5
91	TEST17	↓	6739.5
92	V_3	↓	7061.5
93	V_2	↓	7405.5
94	V_1	↓	7749.5
95	V_C	↓	8093.5
96	MV_1	↓	8437.5
97	MV_2	↓	8781.5
98	V_{SSH}	↓	9111.5
99	NC	1539.7	9688.5
100	NC	↓	9817.5

PAD No.	PIN Name	X	Y
101	NC	1539.7	9946.5
102	NC	1539.7	10075.5
103	NC	1539.7	10204.5
104	NC	1519.0	10364.7
105	NC	1457.0	↓
106	COM91	1395.0	↓
107	COM90	1333.0	↓
108	COM89	1271.0	↓
109	COM88	1209.0	↓
110	COM87	1147.0	↓
111	COM86	1085.0	↓
112	COM85	1023.0	↓
113	COM84	961.0	↓
114	COM83	899.0	↓
115	COM82	837.0	↓
116	COM81	775.0	↓
117	COM80	713.0	↓
118	COM79	651.0	↓
119	COM78	589.0	↓
120	COM77	527.0	↓
121	COM76	465.0	↓
122	COM75	403.0	↓
123	COM74	341.0	↓
124	COM73	279.0	↓
125	COM72	217.0	↓
126	COM71	155.0	↓
127	COM70	93.0	↓
128	COM69	31.0	↓
129	COM68	-31.0	↓
130	COM67	-93.0	↓
131	COM66	-155.0	↓
132	COM65	-217.0	↓
133	COM64	-279.0	↓
134	COM63	-341.0	↓
135	COM62	-403.0	↓
136	COM61	-465.0	↓
137	COM60	-527.0	↓
138	COM59	-589.0	↓
139	COM58	-651.0	↓
140	COM57	-713.0	↓
141	COM56	-775.0	↓
142	COM55	-837.0	↓
143	COM54	-899.0	↓
144	COM53	-961.0	↓
145	COM52	-1023.0	↓
146	COM51	-1085.0	↓
147	COM50	-1147.0	↓
148	COM49	-1209.0	↓
149	COM48	-1271.0	↓
150	COM47	-1333.0	↓

4. PIN ASSIGNMENT

Unit : μm

PAD No.	Pin Name	X	Y
151	COM46	-1395.0	10364.7
152	NC	-1457.0	
153	NC	-1519.0	
154	NC	-1517.2	10137.0
155	NC		10075.0
156	COM45		10013.0
157	COM44		9951.0
158	COM43		9889.0
159	COM42		9827.0
160	COM41		9765.0
161	COM40		9703.0
162	COM39		9641.0
163	COM38		9579.0
164	COM37		9517.0
165	COM36		9455.0
166	COM35		9393.0
167	COM34		9331.0
168	COM33		9269.0
169	COM32		9207.0
170	COM31		9145.0
171	COM30		9083.0
172	COM29		9021.0
173	COM28		8959.0
174	COM27		8897.0
175	COM26		8835.0
176	COM25		8773.0
177	COM24		8711.0
178	COM23		8649.0
179	COM22		8587.0
180	COM21		8525.0
181	COM20		8463.0
182	COM19		8401.0
183	COM18		8339.0
184	COM17		8277.0
185	COM16		8215.0
186	COM15		8153.0
187	COM14		8091.0
188	COM13		8029.0
189	COM12		7967.0
190	COM11		7905.0
191	COM10		7843.0
192	COM9		7781.0
193	COM8		7719.0
194	COM7		7657.0
195	COM6		7595.0
196	COM5		7533.0
197	COM4		7471.0
198	COM3		7409.0
199	COM2		7347.0
200	COM1		7285.0

PAD No.	Pin Name	X	Y
201	COM0	-1517.2	7223.0
202	NC		7161.0
203	NC		7099.0
204	NC		7037.0
205	NC		6975.0
206	SEG0		6913.0
207	SEG1		6851.0
208	SEG2		6789.0
209	SEG3		6727.0
210	SEG4		6665.0
211	SEG5		6603.0
212	SEG6		6541.0
213	SEG7		6479.0
214	SEG8		6417.0
215	SEG9		6355.0
216	SEG10		6293.0
217	SEG11		6231.0
218	SEG12		6169.0
219	SEG13		6107.0
220	SEG14		6045.0
221	SEG15		5983.0
222	SEG16		5921.0
223	SEG17		5859.0
224	SEG18		5797.0
225	SEG19		5735.0
226	SEG20		5673.0
227	SEG21		5611.0
228	SEG22		5549.0
229	SEG23		5487.0
230	SEG24		5425.0
231	SEG25		5363.0
232	SEG26		5301.0
233	SEG27		5239.0
234	SEG28		5177.0
235	SEG29		5115.0
236	SEG30		5053.0
237	SEG31		4991.0
238	SEG32		4929.0
239	SEG33		4867.0
240	SEG34		4805.0
241	SEG35		4743.0
242	SEG36		4681.0
243	SEG37		4619.0
244	SEG38		4557.0
245	SEG39		4495.0
246	SEG40		4433.0
247	SEG41		4371.0
248	SEG42		4309.0
249	SEG43		4247.0
250	SEG44		4185.0

PAD No.	PIN Name	X	Y
251	SEG45	-1517.2	4123.0
252	SEG46		4061.0
253	SEG47		3999.0
254	SEG48		3937.0
255	SEG49		3875.0
256	SEG50		3813.0
257	SEG51		3751.0
258	SEG52		3689.0
259	SEG53		3627.0
260	SEG54		3565.0
261	SEG55		3503.0
262	SEG56		3441.0
263	SEG57		3379.0
264	SEG58		3317.0
265	SEG59		3255.0
266	SEG60		3193.0
267	SEG61		3131.0
268	SEG62		3069.0
269	SEG63		3007.0
270	SEG64		2945.0
271	SEG65		2883.0
272	SEG66		2821.0
273	SEG67		2759.0
274	SEG68		2697.0
275	SEG69		2635.0
276	SEG70		2573.0
277	SEG71		2511.0
278	SEG72		2449.0
279	SEG73		2387.0
280	SEG74		2325.0
281	SEG75		2263.0
282	SEG76		2201.0
283	SEG77		2139.0
284	SEG78		2077.0
285	SEG79		2015.0
286	SEG80		1953.0
287	SEG81		1891.0
288	SEG82		1829.0
289	SEG83		1767.0
290	SEG84		1705.0
291	SEG85		1643.0
292	SEG86		1581.0
293	SEG87		1519.0
294	SEG88		1457.0
295	SEG89		1395.0
296	SEG90		1333.0
297	SEG91		1271.0
298	SEG92		1209.0
299	SEG93		1147.0
300	SEG94		1085.0

Unit : μm

PAD No.	Pin Name	X	Y
301	SEG95	-1517.2	1023.0
302	SEG96		961.0
303	SEG97		899.0
304	SEG98		837.0
305	SEG99		775.0
306	SEG100		713.0
307	SEG101		651.0
308	SEG102		589.0
309	SEG103		527.0
310	SEG104		465.0
311	SEG105		403.0
312	SEG106		341.0
313	SEG107		279.0
314	SEG108		217.0
315	SEG109		155.0
316	SEG110		93.0
317	SEG111		31.0
318	SEG112		-31.0
319	SEG113		-93.0
320	SEG114		-155.0
321	SEG115		-217.0
322	SEG116		-279.0
323	SEG117		-341.0
324	SEG118		-403.0
325	SEG119		-465.0
326	SEG120		-527.0
327	SEG121		-589.0
328	SEG122		-651.0
329	SEG123		-713.0
330	SEG124		-775.0
331	SEG125		-837.0
332	SEG126		-899.0
333	SEG127		-961.0
334	SEG128		-1023.0
335	SEG129		-1085.0
336	SEG130		-1147.0
337	SEG131		-1209.0
338	SEG132		-1271.0
339	SEG133		-1333.0
340	SEG134		-1395.0
341	SEG135		-1457.0
342	SEG136		-1519.0
343	SEG137		-1581.0
344	SEG138		-1643.0
345	SEG139		-1705.0
346	SEG140		-1767.0
347	SEG141		-1829.0
348	SEG142		-1891.0
349	SEG143		-1953.0
350	SEG144	↓	-2015.0

PAD No.	Pin Name	X	Y
351	SEG145	-1517.2	-2077.0
352	SEG146		-2139.0
353	SEG147		-2201.0
354	SEG148		-2263.0
355	SEG149		-2325.0
356	SEG150		-2387.0
357	SEG151		-2449.0
358	SEG152		-2511.0
359	SEG153		-2573.0
360	SEG154		-2635.0
361	SEG155		-2697.0
362	SEG156		-2759.0
363	SEG157		-2821.0
364	SEG158		-2883.0
365	SEG159		-2945.0
366	SEG160		-3007.0
367	SEG161		-3069.0
368	SEG162		-3131.0
369	SEG163		-3193.0
370	SEG164		-3255.0
371	SEG165		-3317.0
372	SEG166		-3379.0
373	SEG167		-3441.0
374	SEG168		-3503.0
375	SEG169		-3565.0
376	SEG170		-3627.0
377	SEG171		-3689.0
378	SEG172		-3751.0
379	SEG173		-3813.0
380	SEG174		-3875.0
381	SEG175		-3937.0
382	SEG176		-3999.0
383	SEG177		-4061.0
384	SEG178		-4123.0
385	SEG179		-4185.0
386	SEG180		-4247.0
387	SEG181		-4309.0
388	SEG182		-4371.0
389	SEG183		-4433.0
390	SEG184		-4495.0
391	SEG185		-4557.0
392	SEG186		-4619.0
393	SEG187		-4681.0
394	SEG188		-4743.0
395	SEG189		-4805.0
396	SEG190		-4867.0
397	SEG191		-4929.0
398	SEG192		-4991.0
399	SEG193		-5053.0
400	SEG194	↓	-5115.0

PAD No.	PIN Name	X	Y
401	SEG195	-1517.2	-5177.0
402	SEG196		-5239.0
403	SEG197		-5301.0
404	SEG198		-5363.0
405	SEG199		-5425.0
406	SEG200		-5487.0
407	SEG201		-5549.0
408	SEG202		-5611.0
409	SEG203		-5673.0
410	SEG204		-5735.0
411	SEG205		-5797.0
412	SEG206		-5859.0
413	SEG207		-5921.0
414	SEG208		-5983.0
415	SEG209		-6045.0
416	SEG210		-6107.0
417	SEG211		-6169.0
418	SEG212		-6231.0
419	SEG213		-6293.0
420	SEG214		-6355.0
421	SEG215		-6417.0
422	SEG216		-6479.0
423	SEG217		-6541.0
424	SEG218		-6603.0
425	SEG219		-6665.0
426	SEG220		-6727.0
427	SEG221		-6789.0
428	SEG222		-6851.0
429	SEG223		-6913.0
430	NC		-6975.0
431	NC		-7037.0
432	NC		-7099.0
433	NC		-7161.0
434	COM92		-7223.0
435	COM93		-7285.0
436	COM94		-7347.0
437	COM95		-7409.0
438	COM96		-7471.0
439	COM97		-7533.0
440	COM98		-7595.0
441	COM99		-7657.0
442	COM100		-7719.0
443	COM101		-7781.0
444	COM102		-7843.0
445	COM103		-7905.0
446	COM104		-7967.0
447	COM105		-8029.0
448	COM106		-8091.0
449	COM107		-8153.0
450	COM108	↓	-8215.0

4. PIN ASSIGNMENT

Unit : μm

PAD No.	Pin Name	X	Y
451	COM109	-1517.2	-8277.0
452	COM110		-8339.0
453	COM111		-8401.0
454	COM112		-8463.0
455	COM113		-8525.0
456	COM114		-8587.0
457	COM115		-8649.0
458	COM116		-8711.0
459	COM117		-8773.0
460	COM118		-8835.0
461	COM119		-8897.0
462	COM120		-8959.0
463	COM121		-9021.0
464	COM122		-9083.0
465	COM123		-9145.0
466	COM124		-9207.0
467	COM125		-9269.0
468	COM126		-9331.0
469	COM127		-9393.0
470	COM128		-9455.0
471	COM129		-9517.0
472	COM130		-9579.0
473	COM131		-9641.0
474	COM132		-9703.0
475	COM133		-9765.0
476	COM134		-9827.0
477	COM135		-9889.0
478	COM136		-9951.0
479	COM137		-10013.0
480	NC		-10075.0
481	NC		-10137.0
482	NC	-1519.0	-10364.7
483	NC	-1457.0	
484	COM138	-1395.0	
485	COM139	-1333.0	
486	COM140	-1271.0	
487	COM141	-1209.0	
488	COM142	-1147.0	
489	COM143	-1085.0	
490	COM144	-1023.0	
491	COM145	-961.0	
492	COM146	-899.0	
493	COM147	-837.0	
494	COM148	-775.0	
495	COM149	-713.0	
496	COM150	-651.0	
497	COM151	-589.0	
498	COM152	-527.0	
499	COM153	-465.0	
500	COM154	-403.0	

PAD No.	Pin Name	X	Y
501	COM155	-341.0	-10364.7
502	COM156	-279.0	
503	COM157	-217.0	
504	COM158	-155.0	
505	COM159	-93.0	
506	COM160	-31.0	
507	COM161	31.0	
508	COM162	93.0	
509	COM163	155.0	
510	COM164	217.0	
511	COM165	279.0	
512	COM166	341.0	
513	COM167	403.0	
514	COM168	465.0	
515	COM169	527.0	
516	COM170	589.0	
517	COM171	651.0	
518	COM172	713.0	
519	COM173	775.0	
520	COM174	837.0	
521	COM175	899.0	
522	COM176	961.0	
523	COM177	1023.0	
524	COM178	1085.0	
525	COM179	1147.0	
526	COM180	1209.0	
527	COM181	1271.0	
528	COM182	1333.0	
529	COM183	1395.0	
530	NC	1457.0	
531	NC	1519.0	

5. PIN DESCRIPTION

5.1 Power Supply Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Power supply</td><td>IC system power supply. Also, use this pin together with the MPU power supply pin V_{CC}.</td><td>8</td></tr>
<tr><td>V_{DD2}</td><td>Power supply</td><td>Connect to V_{DD}.</td><td>3</td></tr>
<tr><td>V_{SSL}</td><td>Power supply</td><td>0V pin connected to the system ground.</td><td>8</td></tr>
<tr><td>V_{SSH}</td><td>Power supply</td><td>High-voltage resistance circuit negative power supply pin. Short-circuit to V_{SSL} outside the LCD module.</td><td>6</td></tr>
<tr><td>V_{DI}</td><td>Power supply</td><td>Power supply pin for internal circuit. It is made from V_{DD}.
This pin is required to connect external capacitance between this pin and V_{SS} to stabilize the voltage.
The V_{DI} generator can select valid/invalid by V_{DIS} pin.
For single chip usage, the V_{DI} generator must be ON (V_{DIS} = HIGH).
Prohibit to supply V_{DI} externally.
For multi chip usage, each V_{DI} of chips are must be same, therefore set master's V_{DIS} = HIGH and slave's V_{DIS} = LOW to supply V_{DI} voltage from master chip to slave chip(s).</td><td>2</td></tr>
<tr><td>V_{DIS}</td><td>I</td><td>This pin is used for making the V_{DI} generating circuit valid or invalid.
V_{DIS} = HIGH : The V_{DI} generating circuit is valid. (Master chip)
V_{DIS} = LOW : The V_{DI} generating circuit is invalid. (Slave chip)
When the V_{DIS} pin is used by changing from LOW to HIGH, it should be initialized by the pin after changing it.
Only the V_{DIS} pin controls operation of the V_{DI} generating circuit and the circuit operates independently of the save power command.</td><td>1</td></tr>
<tr><td>V_3, V_2, V_1, V_C, MV_1, MV_2</td><td>Power supply</td><td>Multi-level, liquid crystal drive power supply pins. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operational amplifier and applied.
The following magnitude correlation should be followed:
$V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq V_{SSH}$ (=V_{SSL})
The following voltages are example in case of Bias 1/13 to 8. Input externally symmetrical voltages against VC.
<table>
<tr><th>Bias</th><th>1/13</th><th>1/12</th><th>1/11</th><th>1/10</th><th>1/9</th><th>1/8</th></tr>
<tr><td>V_2</td><td>8.5/13 · V_3</td><td>8/12 · V_3</td><td>7.5/11 · V_3</td><td>7/10 · V_3</td><td>6.5/9 · V_3</td><td>6/8 · V_3</td></tr>
<tr><td>V_1</td><td>7.5/13 · V_3</td><td>7/12 · V_3</td><td>6.5/11 · V_3</td><td>6/10 · V_3</td><td>5.5/9 · V_3</td><td>5/8 · V_3</td></tr>
<tr><td>V_C</td><td>6.5/13 · V_3</td><td>6/12 · V_3</td><td>5.511 · V_3</td><td>5/10 · V_3</td><td>4.5/9 · V_3</td><td>4/8 · V_3</td></tr>
<tr><td>MV_1</td><td>5.5/13 · V_3</td><td>5/12 · V_3</td><td>4.5/11 · V_3</td><td>4/10 · V_3</td><td>3.5/9 · V_3</td><td>3/8 · V_3</td></tr>
<tr><td>MV_2</td><td>4.5/13 · V_3</td><td>4/12 · V_3</td><td>3.5/11 · V_3</td><td>3/10 · V_3</td><td>2.5/9 · V_3</td><td>2/8 · V_3</td></tr>
</table>
</td><td>each 1</td></tr>
</table>

5.2 System Bus Connection Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0</td><td>I/O</td><td>8-bit bi-directional data bus; connected to the standard 8-bit or 16-bit MPU data bus.
When serial interface is selected (P/S = LOW), if chip select is inactive or the state of operation is other than reading or writing, D0 to D7 are set to High-impedance (Hi-Z).</td><td>total 8</td></tr>
<tr><td>SI</td><td>I/O</td><td>Serial data input/output pin when the serial interface is selected (P/S = LOW)
When serial interface is selected, read status is enabled, but read display data RAM is not enabled.</td><td>1</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial clock input pin when serial interface is selected (P/S = LOW) . Data is read at the rising edge of clock.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>The least significant bit (LSB) of the standard MPU address bus is connected and a distinction is made between data and command.
A0 = HIGH : D0 to D7 is display data or command parameter.
A0 = LOW : D0 to D7 is control command.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Setting $\overline{RES}$ to LOW resets the device.
Reset operation depends on the signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal Active when $\overline{CS}$ = LOW, enabling input or output of data/command. When $\overline{CS}$ = HIGH, data bus are set to Hi-Z.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When MPU of the 80 series is connected. Active LOW
This pin connects $\overline{RD}$ signal of 80 series MPU. Data bus enters a state of output while this signal is set to LOW.
• When MPU of the 68 series is connected. Active HIGH
Becomes enable clock input pin of the 68 series MPU.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When MPU of the 80 series is connected. Active LOW
This pin connects the 80 series MPU signal. Signals on the data bus are latched at the trailing edge of Signal $\overline{WR}$.
• When the 68 series MPU is connected:
Becomes input pin of read/write control signal.
R/$\overline{W}$ = HIGH : Read
R/$\overline{W}$ = LOW : Write</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Select pin between parallel interface and serial interface
P/S = HIGH : Parallel interface
P/S = LOW : Serial Interface:
Sets as shown in the table below depending on the state of P/S.
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>A0</td><td>SI</td><td>Write
Read status</td><td>SCL</td></tr>
</table>
When P/S = LOW, D0 to D7 are Hi-Z. For D0 to D7, it may be set to HIGH, LOW or open. However, set $\overline{RD}$(E) and $\overline{WR}$ (R/$\overline{W}$) to HIGH or LOW.
When serial interface is selected, read status is enabled, but read display data RAM is not enabled.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>C86</td><td>I</td><td>Pin for switching MPU interface.
C86 = HIGH : 68 series MPU interface
C86 = LOW : 80 series MPU interface
When serial interface is selected, set to LOW.</td><td>1</td></tr>
<tr><td>ERR</td><td>O</td><td>Pin for monitoring the operating state of IC.
ERR = LOW : Normal operating state
ERR = HIGH : Initial state or error detection
Becomes ERR = HIGH in the initial state following resetting.
Becomes ERR = LOW after resetting.
If a bit-flip occurs in the register which is part of internal logic because of external noise or similar reason, becomes ERR = HIGH. When ERR = HIGH, re-write all commands. After resetting, returns to WRR = LOW. At this time it is also recommended to re-write data to display data RAM.</td><td>1</td></tr>
</table>

5.3 Display Timing Signal Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>M/S</td><td>I</td><td>Pin for selecting master/slave operation.
Master operation outputs timing signal required for LCD display and slave operation inputs timing signal required for LCD display. This causes synchronization in LCD display system.
M/S = HIGH : Master operation
M/S = LOW : Slave operation
Sets as shown in the table below depending on the state of M/S and CLS.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillation circuit</th><th>CL</th><th>FR, $\overline{DOF}$, F1, F2, SYNC</th></tr>
<tr><td rowspan="2">HIGH</td><td>HIGH</td><td>Enabled</td><td>Output</td><td>Output</td></tr>
<tr><td>LOW</td><td>Disabled</td><td>Input</td><td>Output</td></tr>
<tr><td rowspan="2">LOW</td><td>HIGH</td><td>Disabled</td><td>Input</td><td>Input</td></tr>
<tr><td>LOW</td><td>Disabled</td><td>Input</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>Pin for selecting enable/disable built-in oscillation circuit for display clock.
CLS = HIGH : Built-in oscillation circuit enabled
CLS = LOW : Built-in oscillation circuit disabled (external input)
When CLS = LOW, display clock is input from the CL pin.
To use this IC on master or slave, set each CLS pin to the same level.
<table>
<tr><th>Display clock</th><th>Master</th><th>Slave</th></tr>
<tr><td>Use of built-in oscillation circuit</td><td>HIGH</td><td>HIGH</td></tr>
<tr><td>External input</td><td>LOW</td><td>LOW</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin. Sets as shown in the table below depending on the state of M/S and CLS.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td rowspan="2">HIGH</td><td>HIGH</td><td>Output</td></tr>
<tr><td>LOW</td><td>Input</td></tr>
<tr><td rowspan="2">LOW</td><td>HIGH</td><td>Input</td></tr>
<tr><td>LOW</td><td>Input</td></tr>
</table>
To use this IC on master/slave, connect each CL pin.</td><td>1</td></tr>
</table>

Pin name	I/O	Description	Number of pins
FR	I/O	Liquid crystal alternating-current signal input/output pin. M/S = HIGH : Output M/S = LOW : Input To use this IC on master/slave, connect each FR pin.	1
F1, F2, SYNC	I/O	Liquid crystal synchronization signal input/output pin. M/S = HIGH : Output M/S = LOW : Input To use this IC on master/slave, connect each F1, F2 or SYNC pin.	1 for each
$\overline{DOF}$	I/O	Pin for controlling blanking of liquid crystal display. M/S = HIGH : Output M/S = LOW : Input To use this IC on master/slave, connect each $\overline{DOF}$ pin.	1

5.4 Liquid Crystal Drive Pins

Pin name	I/O	Description	Number of pins
SEG0 to SEG223	O	Liquid crystal segment drive output pin. One level is selected from V_2, V_1, V_C, MV_1, and MV_2 by combining display RAM and FR, F1 and F2 signals.	224 in total
COM0 to COM183	O	Liquid crystal common drive output pin. One level is selected from V_3, V_C, and V_{SSL} (= V_{SSL}) by combining scan data and FR, F1 and F2 signals.	184 in total

5.5 Temperature Sensor Pins

Pin name	I/O	Description	Number of pins
SV_{D2}	O	Temperature sensor analog voltage output pin.	1
SV_{22}	O	Pin for testing temperature sensor. Sets to open.	1

5.6 Test Pins

Pin name	I/O	Description	Number of pins
TEST	I	Pin for testing IC chip. Set to LOW.	1
TEST2	O	Pin for testing IC chip. Set to open.	1
TEST3 to TEST17	I	Pin for testing IC chip. Set to open.	1

6. FUNCTIONAL DESCRIPTION

6.1 MPU Interface

6.1.1 Selecting Interface Type

This IC allows data transfer through 8-bit bi-directional data bus (D7 to D0) or serial data input (SI). Selecting HIGH or LOW for polarity of P/S pin allows selection of 8-bit parallel data input or serial data input as shown in Table 6.1.

Table 6.1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D7～D0
HIGH : Parallel input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	—	—	D7～D0
LOW : Serial input	$\overline{CS}$	A0	—	—	—	SI	SCL	(HZ)

— : Set - to HIGH or LOW. HZ is in the state of high impedance.

6.1.2 Parallel interface

When parallel interface is selected (P/S = HIGH), setting the C86 pin to HIGH or LOW allows direct connection to the MPU bus of either 80 series or 68 series as shown in Table 6.2.

Table 6.2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7～D0
HIGH : 68 series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7～D0
LOW : 80 series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7～D0

Data bus signal is identified by combination of A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) as shown in Table 6.3.

Table 6.3

Common	68 series	80 series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data reading, reads status.
1	0	1	0	Status data writing, writes command parameter.
0	0	1	0	Writes a command.

6.1.3 Serial Interface

When serial interface is selected (P/S = LOW), the chip is active ($\overline{CS}$ = LOW) and can accept serial data input (SI) and serial clock input (SCL). Serial interface is comprised of an 8-bit shift register and 3-bit counter. Serial data is captured from serial data input pin in order from D7, D6 to D0 on the rising edge of the serial clock and converted into 8-bit parallel data on the rising edge of the 8th serial clock and then processed.

Whether serial data input is display data, command parameter or command is determined by A0 input. For A0 = HIGH, display data or command parameter, for A0 = LOW, command. A0 input is read and determined on the 8xn-th rising edge of the serial clock after the chip goes into the active state.

Using the status read command enables read status and read data, respectively, even when serial interface is selected. However, it should be noted that the $\overline{CS}$ signal is handled differently from the time of serial data input. Read from display data RAM is not enabled. Signal chart of serial interface is shown in Fig.6.1.

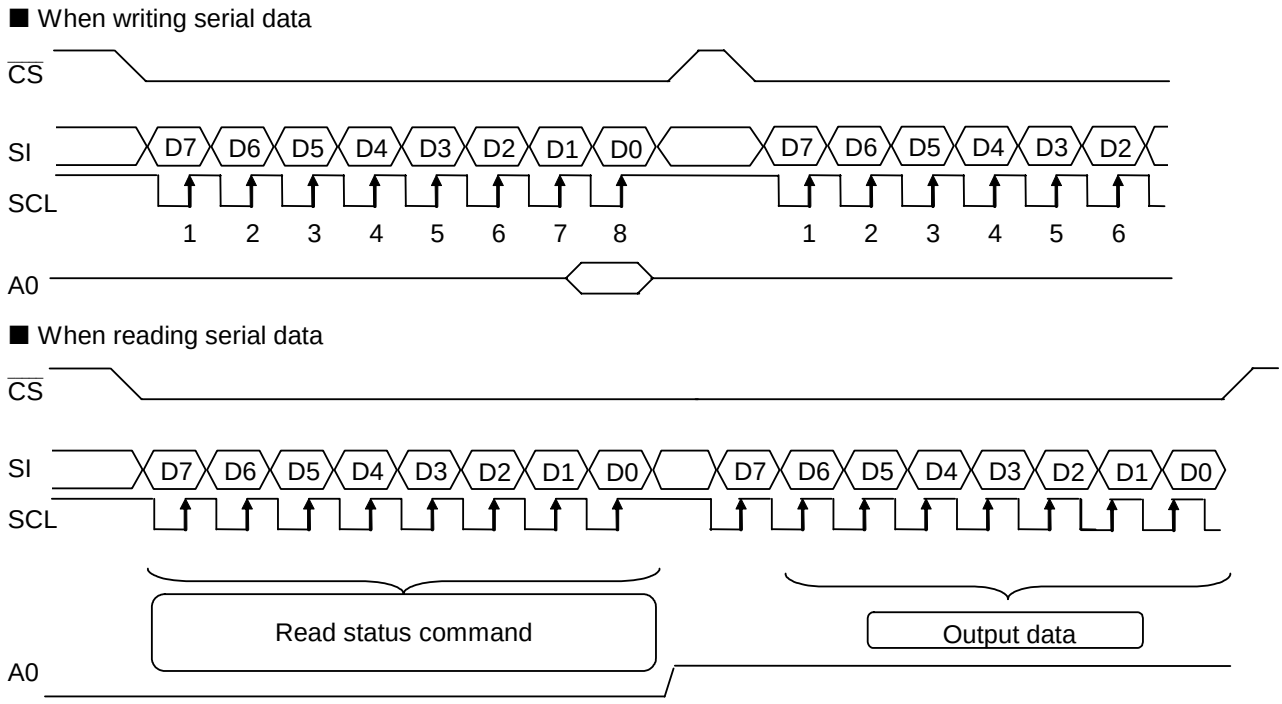


Fig.6.1 Signal Chart of Serial Interface

* When the chip is inactive, the counter is reset to the initial state. Continuous serial clock input is possible, however, it is recommended to clear the counter by setting $\overline{CS}$ = HIGH for every 8 bits of serial clock at the time of serial data input so that malfunction caused by external noise can be prevented. When reading serial data, continuously read data by entering serial clock from the SCL pin with the setting left $\overline{CS}$ = LOW instead of setting $\overline{CS}$ = HIGH after the read command. After getting the read data, to set $\overline{CS}$ = HIGH is necessary.
* For serial interface, read from display data RAM is not enabled.
* For SCL signal, great care should be taken for wiring termination reflection and external noise. It is recommended to check operation using the actual equipment.

6.1.4 Chip Select

Since this IC has chip select pin, parallel interface or serial interface is enabled when $\overline{CS}$ = LOW is set.

When the chip select is inactive, D0 to D7 are in the state of high impedance and input of A0, $\overline{RD}$, $\overline{WR}$, SI, and SCL is disabled. When serial interface is selected, shift register and counter are reset.

6.1.5 Accessing Display Data RAM and Internal Register

Since this IC is accessed as a kind of pipeline processing between LSIs via bus holder coming with internal data bus, wait time is not necessary if the cycle time is satisfied, enabling high-speed data transmission.

For example, if MPU writes data to display data RAM, data is temporarily held in the bus holder and written to the display data RAM by the next data write cycle. When MPU reads display data RAM, read data is held in the bus holder in the first data read cycle (dummy) and read on the system bus from the bus holder in the next data read cycle.

Therefore, read sequence of display data RAM is subject to constraints. In the data read immediately after the display data read command, the specified address data is not output (dummy read), but it is output at the 2nd data read session.

This relationship is shown in Fig.6.2.

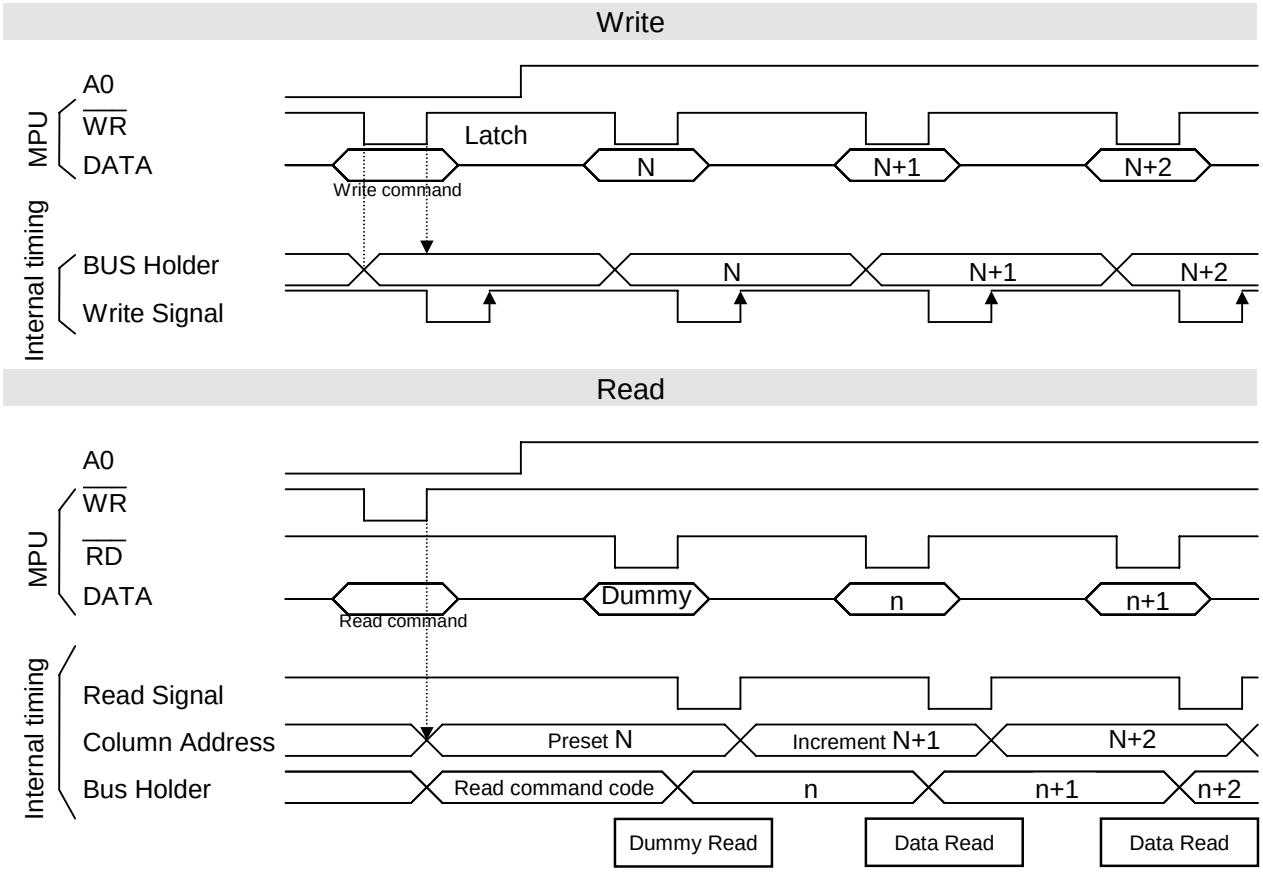


Fig.6.2 Read Sequence of Display Data RAM

6.2 Display Data RAM

6.2.1 Display Data RAM

This RAM for storing display dot data is comprised of 184 × 224 × 2 bits. The desired bit is accessible by specifying page address and column address.

When 4 gray scales are selected with the set display mode command, the input display data is processed as a pair of 2 bits each. Combination is

RAM bit data (higher bit, lower bit) = (D1, D0), (D3, D2), (D5, D4), (D7, D6)
= (1, 1): Gray scale 3 Black (in normal display mode)
= (1, 0): Gray scale 2
= (0, 1): Gray scale 1
= (0, 0): Gray scale 0 White (in normal display mode)

When RAM bit data is gray scales 1 and 2, gray scale display will be provided according to parameters of set gray scale pattern command.

When binary display is selected with the set display mode command, 1-bit of built-in RAM corresponds to 1 dot of pixel. When RAM bit data is "1", black display appears. When RAM data is "0", white display appears.

RAM bit data
"1": ON Black (in normal display mode)
"0": OFF White (in normal display mode)

Since display data D7 to D0 from MPU corresponds to the common direction of LCD as shown in Fig.6.3 and Fig.6.4, higher degree of freedom is achieved in configuring display with less constraints on display data transfer if the S1D15722 series is used for the multi-chip.

Read/write from MPU to RAM is performed via I/O buffer, which is controlled independently of liquid crystal drive RAM. Therefore, even if MPU makes an asynchronous access to RAM during liquid crystal display, it does not have an adverse effect on the display.

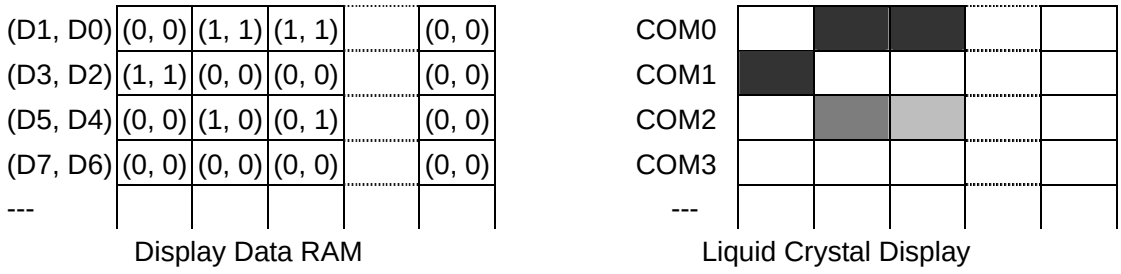


Fig.6.3 4-Gray Scale Display

Fig.6.4 Binary Display

6.2.2 Gray Scale Display

When 4-gray scale is displayed with the set display mode command, the display is expressed by controlling FRM (frame gray scale) based on the gray scale data written to the display data RAM.

Density of gray level (gray scale 2, gray scale 1) of four gray scales is specified with the set gray scale pattern command. The density of gray scale can be selected from 14 levels.

6.2.3 Page Address Circuit/Column Address Circuit

Use the set page address command and set column address command to specify display data RAM address to be accessed as shown in Fig.6.5 and Fig.6.6.

The address increment direction can be selected between the column direction and page direction using the select display data input direction command. In both directions, an increment by +1 takes place following read or write operation.

When the address increment direction is column, the column address increments by +1 each time read or write operation takes place. After the column address has made an access to DFH, the page address increments by +1 and the column address moves to 0H.

When the address increment direction is page, the page address increments with the column address fixed. After the page address has made an access to Page45, the column address increments by +1 and the page address moves to Page0.

In both address increment directions, moves to the page address Page0 and the column address 0H after an access to the column address DFH of the page address Page 45 is made.

As shown in Table 6.4, the correspondence between the column address of the display data RAM and segment output can be reversed with the direction of setting column address command. Therefore, IC arrangement comes to be less restricted when the LCD module is assembled.

Table 6.4

Direction of setting column address Command register value		**Correspondence between RAM column address and SEG output**		
		SEG0	→	**SEG223**
D0 = "0"	Column address: normal rotation	0(H)	→	DF(H)
D0 = "1"	Column address: reversal	DF(H)	←	0(H)

6.2.4 Line Address Circuit

For the line address, specify the line address corresponding to the COM output when the display data RAM is displayed as shown in Fig.6.5 and Fig.6.6. Normally, specify the top line on display (in the state of common output .. for normal rotation, COM0 output, for inverted, COM183 output) using the set display start line command. The display area corresponds to the lines specified in the incremental direction from the specified display start line address to the line address, using the number of display lines set command.

The display start line address is set every four lines of display. Dynamically changing the line address using the set display start line command enables screen scrolling and page turning.

6.2.5 I/O Buffer Circuit

Bi-directional buffer for reading or writing display data RAM from the side of MPU. Since read or write of display data RAM from the side of MPU is controlled independently of data output from the display data RAM to the display data clutch circuit, an asynchronous access made to the display data RAM during crystal liquid display does not have an adverse effect on display, including flickering.

6.2.6 Display Data Latch Circuit

The display data latch circuit is a latch for temporarily storing data to be output to the liquid crystal drive circuit from the display data RAM. Since the display normal/inverted, display ON/OFF, and display full lighting ON/OFF commands control data in this latch, data in the display data RAM will not change.

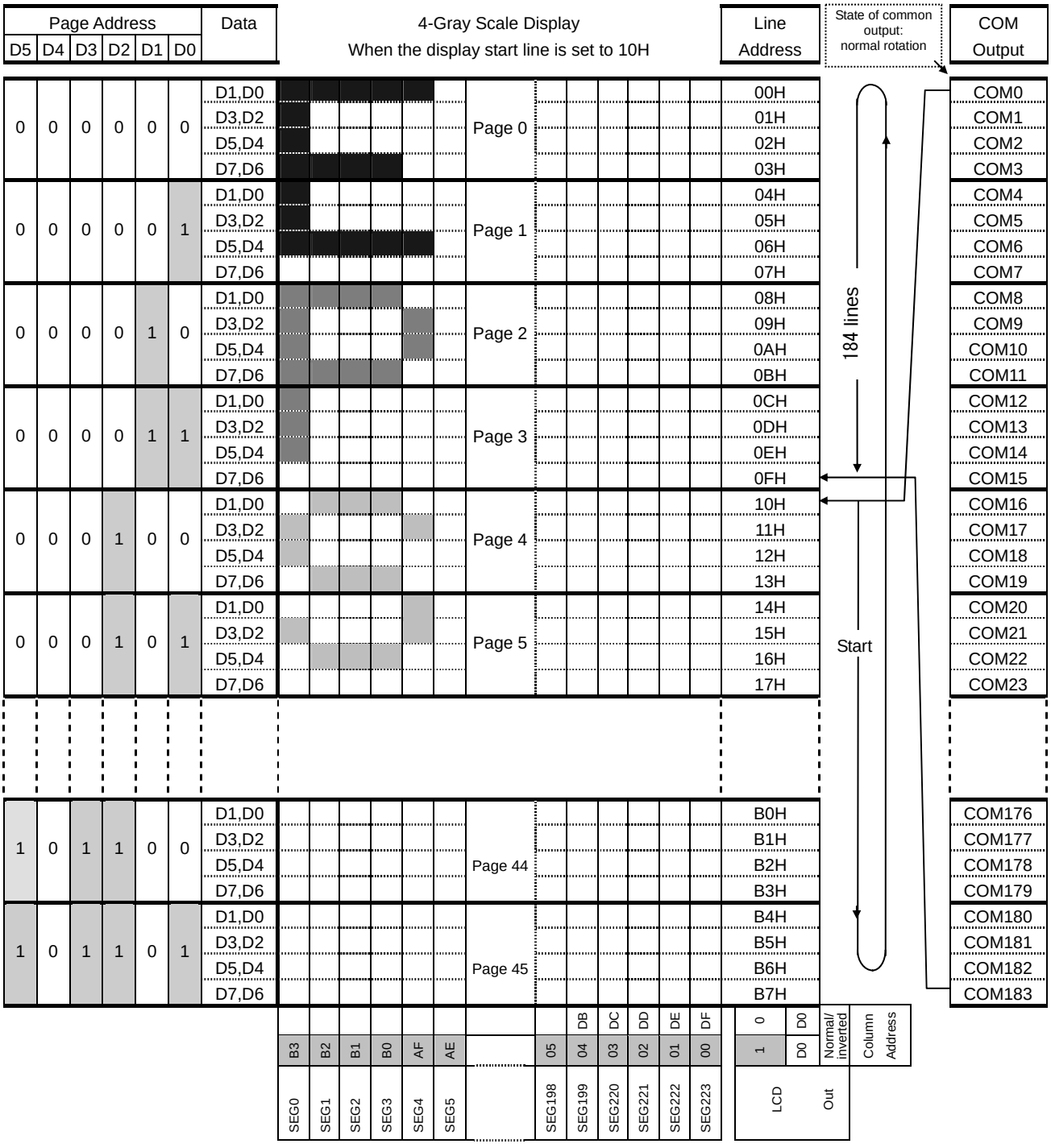


Fig.6.5 4-Gray Scale Display

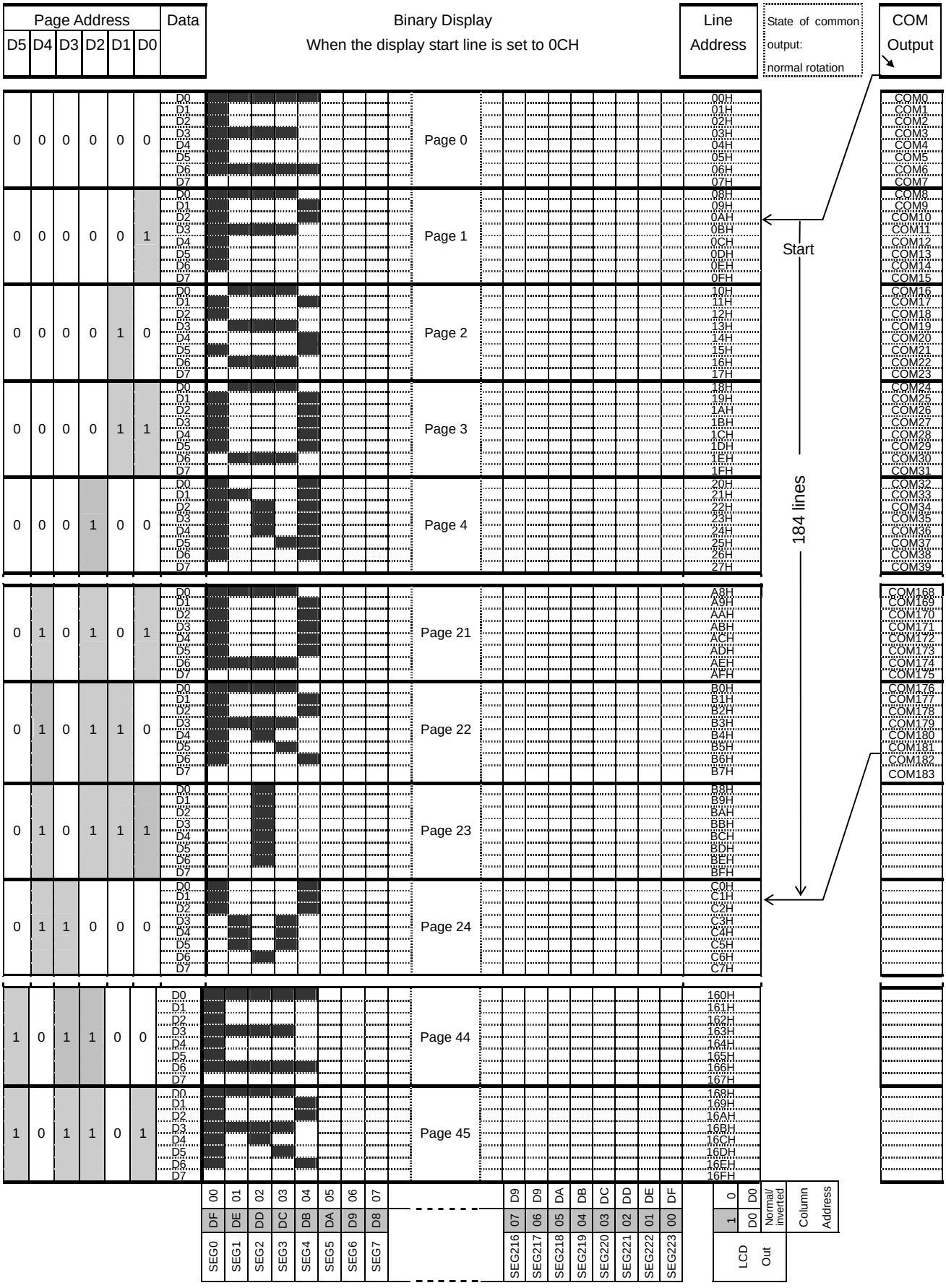


Fig.6.6 Binary Display

6.3 Oscillation Circuit

This CR-type oscillator generates internal clocks and display clocks. The oscillation circuit is enabled only when set to M/S = HIGH and CLS = HIGH. Oscillation starts following input of the built-in oscillation circuit ON command.

When set to CLS = LOW, oscillation stops and display clock is input from the CL pin.

6.4 Display Timing Signal Generator

Based on the built-in oscillation circuit or external clock, display timing signals (FR, SYNC, F1, F2, CL, and DOF) are generated.

The FR normally generates 2-frame alternating drive system drive waveform to the liquid crystal drive circuit. FR normally generates. Setting data a for the n-line inverted drive register generates n-line inversion alternating drive waveform for each 4 × (a+1) line. When the display quality such as cross talk presents a problem, it may be improved by using the n-line inverted alternating drive. Determine the number of lines n for AC drive through actual liquid crystal display.

When this IC is shared by multiple chips, supply the display timing signals (FR, SYNC, F1, F2, CL, and DOF) to the slave from the master and synchronize the master and the slave.

The state of FR, SYNC, F1, F2, CL, and DOF is shown in Table 6.5.

Table 6.5

Operating Mode		CL	FR, SYNC, F1, F2, DOF
Master (M/S = HIGH)	Built-in oscillation circuit enabled (CLS = HIGH)	Output	Output
	Built-in oscillation circuit disabled (CLS = LOW)	Input	Output
Slave (M/S = LOW)	Built-in oscillation circuit enabled (CLS = HIGH)	Input	Input
	Built-in oscillation circuit disabled (CLS = LOW)	Input	Input

6.5 Operating State Detector Circuit

This circuit detects an error if the state of a specific command register was changed because of excessive external noise. The circuit can determine the state at the level output from the pin ERR or read the state from the data bus using the read status command.

Relationship between the output level from the pin ERR and the internal state is shown in Table 6.6.

Table 6.6

Output	Descriptions
LOW	Error was not detected.
HIGH	Bit-flip occurred in part of the command register.

When the level is set to HIGH, display operation may not be normal because of bit-flip in the command register. Monitor the level of the pin ERR or execute the read status command regularly to check the operating state of the IC. When an error is detected, reset all the commands. It is also recommended to rewrite to all the bits of the display data RAM concurrently with the above operation.

This circuit detects specific error modes. It does not support all command registers. For command registers to be supported and expanded information, see 7.1 Command Description (30) Read Status. The initial state after resetting is ERR = HIGH. This function is enabled after resetting.

6.6 Liquid Crystal Drive Circuit

6.6.1 Segment Driver

This SEG output circuit selects from five values of V_2, V_1, V_C, MV_1 and MV_2 using the driver control signal determined by the decoder and outputs them.

6.6.2 Common Driver

This COM output circuit selects from three values of V_3, V_C and V_{SSH} using the driver control signal determined by the decoder and outputs them.

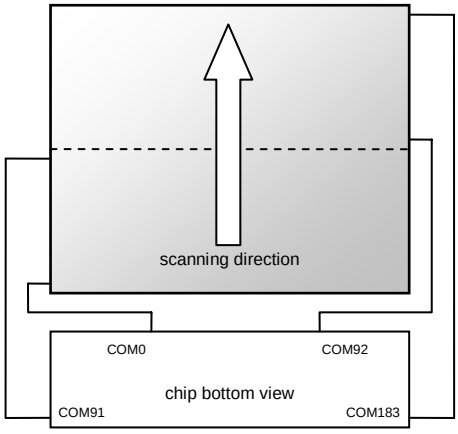
This IC can set the COM output scanning direction and select normal drive or interlace drive using the select common output status command (See Table 6.7.). Therefore, IC arrangement comes to be less restricted when the LCD module is assembled.

Table 6.7

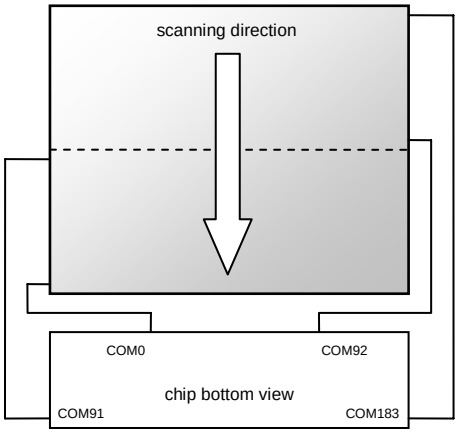
Status	Drive system	COM scanning direction
State 1	Normal drive/normal scan direction	COM(0,1,2,3) → COM(4,5,6,7) →⋯ → COM(176,177,178,179) → COM(180,181,182,183)
State 2	Normal drive/invert scan direction	COM(183,182,181,180) → COM(179,178,177,176) →⋯ → COM(7,6,5,4) → COM(3,2,1,0)
State 3	Interlace drive pattern A (Scanning start position: COM0) - Normal scan direction	COM(0,1,2,3) → COM(92,93,94,95) (⋯ (COM(44,45,46,47) (COM(136,137,138,139) (⋯ (COM(88,89,90,91) (COM(179,181,182,183)
State 4	Interlace drive pattern A (Scanning start position: COM183) - Invert scan direction	COM(183,182,181,180) (COM(91,90,89,88) (⋯ (COM(139,138,137,136) (COM(47,46,45,44) (⋯ (COM(95,94,93,92) (COM(3,2,1,0)
State 5	Interlace drive pattern B (Scanning start position: COM92) - Normal scan direction	COM(92,93,94,95) (COM (0,1,2,3) (⋯ (COM(136,137,138,139) (COM(44,45,46,47) (⋯ → COM(179,181,182,183) → COM (88,89,90,91)
State 6	Interlace drive pattern B (Scanning start position: COM91) - Invert scan direction	COM(91,90,89,88) → COM (183,182,181,180) →⋯ (COM(47,46,45,44) (COM(139,138,137,136) (⋯ (COM(3,2,1,0) (COM((95,94,93,92)

* Four lines in parentheses ( ) indicate those of COM to be selected at a time.

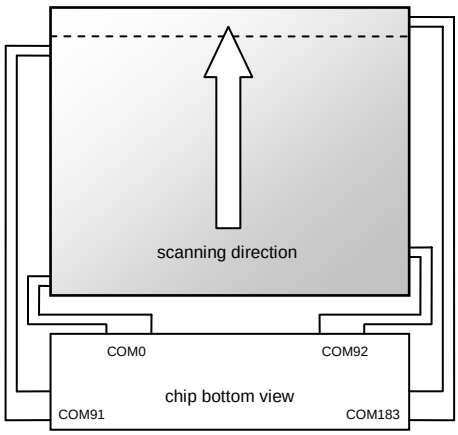
State 1: Normal drive/normal rotation of scanning direction
(Scan start position: COM0)



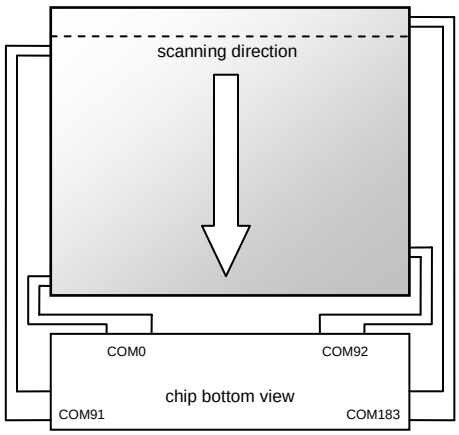
State 2: Normal drive/inverted scanning direction
(Scan start position: COM183)



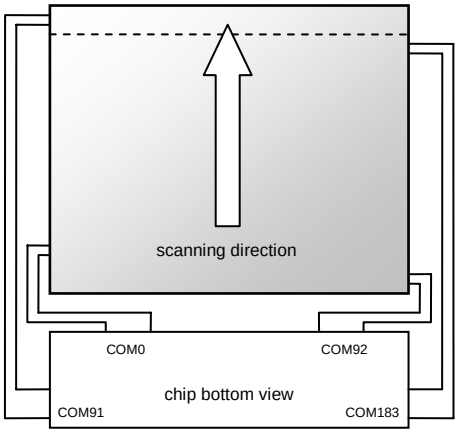
State 3: Interlace drive pattern A/
normal rotation of scanning direction
(Scan start position: COM0)



State 4: Interlace drive pattern A/
inverted scanning direction
(Scan start position: COM183)



State 5: Interlace drive pattern B/
normal rotation of scanning direction
(Scan start position: COM92)



State 6: Interlace drive pattern B/
inverted scanning direction
(Scan start position: COM91)

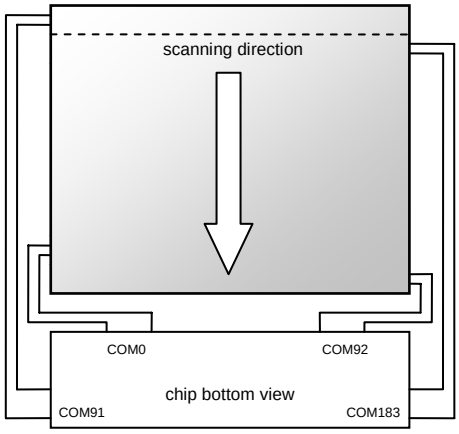


Fig. 6.7 Relationship between Select Common Output Status Command and LCD Panel Connection

6.7 Temperature Sensor Circuit

This IC incorporates the temperature sensor circuit that consists of analog voltage output that changes on the temperature gradient of -5.06 mV/°C (typ.). Liquid crystal display of appropriate contrasting density is available in the wide temperature range by inputting the electronic volume register value according to the temperature sensor output value from MPU and controlling the liquid crystal display voltage V_3.

6.7.1 Analog Voltage Output

Inputting the temperature sensor ON command causes the analog voltage to be output from the SVD2 pin, which varies according to the temperature. To control liquid crystal drive voltage with higher accuracy, configure the system which can reduce variations in output voltage by allowing the MPU to give the feedback of values of the output voltage sampled under certain temperature and store them as reference voltage.

6.7.2 Precautions

(1) Noise influence

The temperature sensor circuit operates in the SV22 voltage generated in the regulator operating in the V_{DI} system which is IC's logic operating voltage. The circuits of the SV22 voltage are configured so that steady variations in the V_{DI} power supply system do not have an effect on them. However, if logic is operated at high speed for writing to RAM, for example, power supply noise may be caused in the V_{DI} voltage and the SV22 voltage may also be influenced similarly.

To perform temperature detection accurately, be sure to stop access from the MPU when capturing the temperature sensor output and comply with operating conditions specified at the AC timing.

(2) Influence of mounting

The temperature sensor circuit analog output SVD2 is specified using the output voltage value for the IC's board potential V_{SS}. When measuring the SVD2 potential in the actual system, attention should be paid to the relationship between the IC's board potential and the system ground's potential.

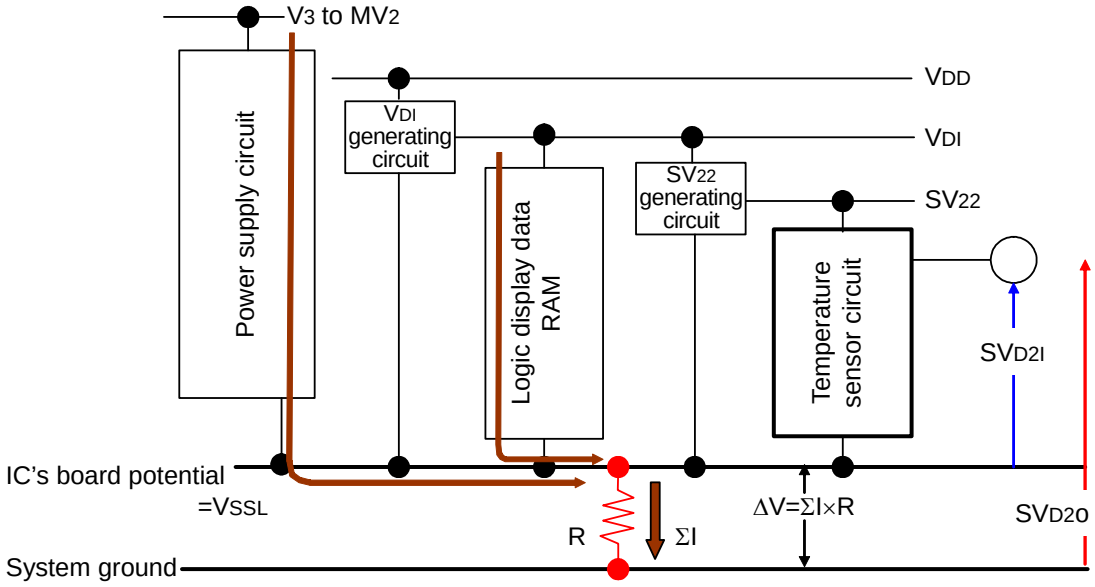


Fig.6.8 Influence of Resistance R between System Ground and V_{SS}

If there is a resistance component R between the system ground and IC's VSS pin, the IC's board potential VSS viewed from the system ground experiences fall of potential of

$\Delta V = \sum I \times R$ (where $\sum$I: IC is the total amount of the current consumed by IC)

Therefore, the temperature sensor output (Fig.6.22: SVD20) viewed from the system ground is also influenced similarly. That is, ΔV has an impact on the temperature sensor output (Fig.6.22: SVD21) viewed from the IC's VDD defined in the specifications.

To eliminate the impact of ΔV as much as possible, adopt the design and usage with consideration given to three points below:

- Decrease the resistance value between the system ground and IC's VSS pin as low as possible, including ITO resistance when mounting COG.
- Measure the temperature sensor output voltage with the current consumed by IC reduced as much as possible by placing the IC in the power-saving mode.
- Minimize the impact caused by the IC's external circuits by leaving the system to be used under certain temperature and allowing the system to store the SVD2 voltage measured while operating the system as the reference voltage.

6.8 Reset Circuit

When the $\overline{RES}$ input reaches LOW, this IC enters the state of initial settings. The state of initial settings is as follows:

1 Display: OFF
2 Display: normal rotation
3 Full display lighting: OFF
4 Common output state: normal drive, scanning direction in normal rotation
5 Display start line: set on the 1st line
6 Page address: set to page 0.
7 Column address: set to address 0.
8 Display data input direction: column direction
9 Column address direction: normal rotation
10 n line alternating inverted drive: Off (inverted drive for each frame)
11 n line inverted drive register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0)
12 Display mode: 4-gray scale display
13 Gray scale pattern register: (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 1, 0, 1, 0, 0, 1, 0)
14 FRM pallet: Pallet 0
15 Display line number set register: (D5, D4, D3, D2, D1, D0) = (1, 0, 1, 1, 0, 1) (184 lines)
start point (block) register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0) (COM0 ~ COM3)
*: COM output state: Normal drive, Normal scan direction.
16 Read-modify-write: OFF
17 Built-in oscillation circuit: stop
18 Clock frequency register: (D3, D2, D1, D0) = (0, 1, 0, 0)
19 TEST1 register: (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
20 Discharge: ON (at the $\overline{RES}$ = LOW level only)
21 Power-saving: reset (OFF)
23 Data in the register in the serial interface: clear
24 Temperature sensor: OFF
25 MLS drive select register: (D4, D3) = (0, 1) (N-line frame inversion overlap OFF, Non-dispersive drive)

When the power is turned on, this circuit requires initialization using the $\overline{RES}$ pin. After being initialized by the pin, each input pin should be controlled successfully.

If the impedance of the control signal from the MPU is high, an over current may flow into the IC. After power is turned on, remedies for high impedance of input pin must be prescribed.

This IC discharges V_{OUT1} to V_{SSL}, and V_{OUT2}, V_{20}, V_{OUT3} and liquid crystal drive voltages V_3, V_2, V_1, V_C, MV_1, and MV_2 to V_{SSH} at the $\overline{RES}$ pin = LOW level. Prevent the V_{SSL} and V_{SSH} from being high impedance during discharge. When using the external power supply for liquid crystal drive, do not supply external power but set high impedance during the pin $\overline{RES}$ = LOW to prevent shorting in the external power supply and V_{SSH} and apply the specified voltage after canceling reset.

7. COMMAND

This IC identifies data bus signal by combination of A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$). Since the command is interpreted and executed at the internal timing only without relying on the external clock, high-speed processing is possible.

For the 80 series MPU interface, entering low pulse in the $\overline{RD}$ pin during read and low pulse in the pin during write starts the command. When HIGH is entered in the R/$\overline{W}$ pin, the 68 series MPU interface goes into the state of read. When LOW is entered, it goes into the state of write. Entering high pulse in the E pin starts the command (For timing, see 10. TIMING CHARACTERISTICS.) Consequently, the 68 series MPU interface is different from the 80 series MPU interface in the point that $\overline{RD}$(E) becomes "1(H)" during display data read in the command description and command table. Command description is shown below by taking the 80 series MPU interface as an example.

When serial interface is selected, sequentially input data from D7.

7.1 Command Description

(1) Display ON/OFF

This command allows specification of display ON/OFF. Liquid crystal display is performed in synchronization with display clock input from the built-in oscillation circuit or external source. Do not stop clock frequency input from the built-in oscillation circuit or external source during display ON.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Output level
0	1	0	1	0	1	0	1	1	1	0	Display OFF
										1	Display ON

* After resetting by the $\overline{RES}$ pin, the display is set to OFF.

(2) Display normal/inverted

This command allows inversion of display lighting/non-lighting without rewriting display data RAM. At this time the contents of the display data RAM are held.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data HIGH LCD ON voltage level (normal display)
										1	RAM data LOW LCD ON voltage level (inverted display)

* After resetting by the $\overline{RES}$ pin, the display is set to normal display.

(3) Full display lighting ON/OFF

This command allows to forcefully place full display in the state of lighting irrespective of the contents of the display data RAM. At this time the contents of the display data RAM are held. In combination with the invert the display command, all-white display is also available.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	State of normal display
										1	Full display lighting

* After resetting by the $\overline{RES}$ pin, the full display lighting is set to OFF.

(4) Select common output state

This command allows selection of the scanning direction of the COM output pin. For more information, see 6.6.2 Common Driver in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	1	0	0	0	1	0	0	Mode set
1	1	0	*	*	*	*	*	P2	P1	P0	Register set

Note: An asterisk (*) denotes invalid bit.

Note: After resetting by the $\overline{RES}$ pin, it is set to normal drive/normal scanning direction.

P2 Normal/interlace drive switching	P1 Interlace A/B switching	P0 Scanning normal/inverted switching	Status
0	0	0	Normal drive, normal scanning direction
0	0	1	Normal drive, inverted scanning direction
1	0	0	Interlace drive pattern A/normal scanning direction
1	0	1	Interlace drive pattern A/inverted scanning direction
1	1	0	Interlace drive pattern B/normal scanning direction
1	1	1	Interlace drive pattern B/inverted scanning direction

(5) Set display start line

With the parameter following this command, specify the display start line address of the display data RAM shown in Figs.6.5 and 6.6.

The display area appears in the incremental direction of the line address from the specified line address. Dynamically changing the line address using this command allows lengthwise screen scrolling and page turning. For more information, see 6.2.4 Line Address Circuit in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	0	1	0	Mode set
1	1	0	*	P6	P5	P4	P3	P2	P1	P0	Register set

Note: An asterisk (*) denotes invalid bit.

Set display start line/set register

The display start line address can be set every four lines of display. The address range that can be specified in the 4-gray scale display in the display mode differs from that in the binary display.

Relationship between the register value with the set register and line address is shown below.

(I) In the 4-gray scale display mode

P6	P5	P4	P3	P2	P1	P0	Line address
*	0	0	0	0	0	0	00H (4 × 0)
*	0	0	0	0	0	1	04H (4 × 1)
			↓				↓
*	1	0	1	1	0	0	B0H (4 × 44)
*	1	0	1	1	0	1	B4H (4 × 45)

Note: After resetting by the $\overline{RES}$ pin, the line address is set to 00H.
Note: An asterisk (*) denotes invalid bit.
Note: Register setting at (1, 0, 1, 1, 1, 0) or higher is not allowed.

(II) In the binary display mode

P6	P5	P4	P3	P2	P1	P0	Line address
0	0	0	0	0	0	0	00H (4 × 0)
0	0	0	0	0	0	1	04H (4 × 1)
			↓				↓
0	1	0	1	1	0	0	B0H (4 × 44)
0	1	0	1	1	0	1	B4H (4 × 45)
			↓				↓
1	0	1	1	0	1	0	168H (4 × 90)
1	0	1	1	0	1	1	16CH (4 × 91)

Note: After resetting by the $\overline{RES}$ pin, the line address is set to 00H.
Note: Register setting at (1, 0, 1, 1, 1, 0, 0) or higher is not allowed.

Sequence of setting display start line

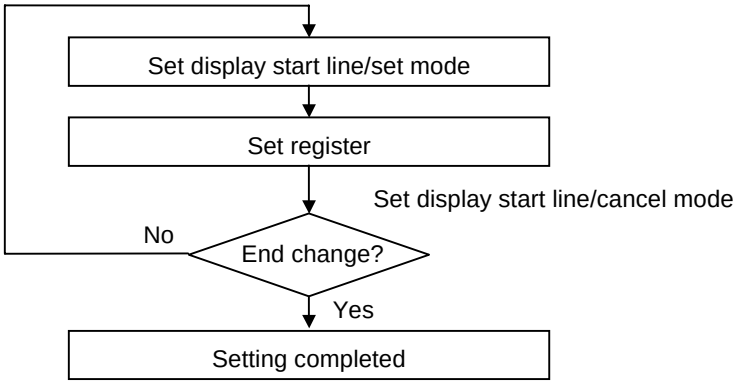


Fig.7.1 Sequence of Setting Display Start Line

(6) Set page address

This command specifies the page address that corresponds to the row address when making an access to the display data RAM shown in Figs.6.5 and 6.6 from the side of MPU.

For more information, see 6.2.3 Page Address Circuit/Column Address Circuit in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	1	1	0	0	0	1	Set mode
1	1	0	*	*	P5	P4	P3	P2	P1	P0	Set register

Note: An asterisk (*) denotes invalid bit.

Relationship between the register value with set register and page address is shown below.

P5	P4	P3	P2	P1	P0	Page address
0	0	0	0	0	0	00H (Page 0)
0	1	0	0	1	1	01H (Page 1)
			↓			↓
1	0	1	1	0	0	2CH (Page 44)
1	0	1	1	0	1	2DH (Page 45)

Note: After resetting by the $\overline{RES}$ pin, the address is set to 00H.
Note: Register setting at (1, 0, 1, 1, 1, 0) or higher is not allowed.

(7) Set column address

This command specifies the column address of the display data RAM shown in Figs.6.5 and 6.6. For more information, see 6.2.3 Page Address Circuit/Column Address Circuit in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	0	1	0	0	1	1	Set mode
1	1	0	P7	P6	P5	P4	P3	P2	P1	P0	Set register

Relationship between the register value with the set register and column address is shown below.

P7	P6	P5	P4	P3	P2	P1	P0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				↓				↓
1	1	0	1	1	1	1	0	DEH
1	1	0	1	1	1	1	1	DFH

Note: After resetting by the $\overline{RES}$ pin, the address is set to the column 00H.
Note: Register setting at (1, 1, 1, 0, 0, 0, 0, 0) or higher is not allowed.

(8) Write display data

This command allows writing 8-bit data to the specified address of the display data RAM. Using the select display data input direction after writing automatically increments the column address or page address by 1. So MPU can write data on display continuously.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	1
1	1	0	Write data							

(9) Read display data

This command allows reading 8-bit data from the specified address of the display data RAM Using the select display data input direction after reading automatically increments the column address or page address by 1. So MPU can read data of multiple words continuously.

Immediately setting the column address or page address, one-shot dummy read is required. For more information, see 6.1.5 Description of Access to Display Data RAM and Internal Register. When serial interface is used, the display data RAM cannot be read.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	0
1	0	1	Read data							

(10) Select display data input direction

This command allows setting of the direction of automatic increment of the display RAM address.

For more information, see 6.2.3 Page Address Circuit/Column Address Circuit in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Direction
0	1	0	1	0	0	0	0	1	0	0	Column
										1	Page

Note: After resetting by the $\overline{RES}$ pin, the direction is set to column.

(11) Direction of setting column address

This command allows reversal of correspondence between the column address of the display RAM data shown in Figs.6.5 and 6.6 and segment driver output. Therefore, the order of the segment driver output pins can be reversed using the command.

The column address is incremented by +1 according to the column address in Figs.6.5 and 6.6 as display data is written and read. For more information, see 6.2.3 Page Address Circuit/Column Address Circuit in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reversal

Note: After resetting by the $\overline{RES}$ pin, the direction is set to normal of setting the column address.

(12) Set n line inverted drive register

This command allows setting the number of inverted lines of the liquid crystal AC drive and starting of the line inverting drive. The number of lines that can be set is 4 to 184 (45 states for 4 lines each). For more information, see 6.4 Display Timing Signal Generator in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	1	0	1	1	0	Set mode
1	1	0	*	*	P5	P4	P3	P2	P1	P0	Set register

Note: An asterisk (*) denotes invalid bit.

Relationship between the register value with set register and the number of inverted lines is shown below.

P5	P4	P3	P2	P1	P0	Number of inverted lines
0	0	0	0	0	0	4 (1 × 4)
0	0	0	0	0	1	8 (2 × 4)
		↓				↓
1	0	1	1	0	0	180 (45 × 4)
1	0	1	1	0	1	184 (46 × 4)

Note: After resetting by the $\overline{RES}$ pin, the number of inverted lines is set to 4.
Note: Register setting at (1, 0, 1, 1, 1, 0) or higher is not allowed.

(13) n line inverted drive ON/FF

This command allows ON/OFF of the n line inverted drive.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	N line inverted drive
0	1	0	1	1	1	0	0	1	0	0	OFF
										1	ON

Note: After resetting by the $\overline{RES}$ pin, the n line inverted drive is set to OFF.

(14) Set display mode

This command allows setting of the normal display mode. Structure of display data RAM in the 4-gray scale display differs from that in the binary display. For more information, see 6.2 Display RAM FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	0	1	1	0	Set mode
1	1	0	*	*	*	*	*	*	P1	P0	Set register

Note: An asterisk (*) denotes invalid bit.

Relationship between the register value with set register and display mode is shown below.

P1	P0	Display mode
0	0	4-gray scale display
0	1	Binary display

Note: After resetting by the $\overline{RES}$ pin, the display is set to 4-gray scale.

(15) Set gray scale pattern

This command allows setting of the density of gray scale.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	1	1	0	0	1	Set mode
1	1	0	P7	P6	P5	P4	P3	P2	P1	P0	Set register

Select the density of (P7, P6, P5, P4): gray scale bit (1,0).

Select the density of (P3, P2, P1, P0): gray scale bit (0, 1).

For the gray scale pattern, one state can be selected from 14 states of gray level. Register value with set register, density of gray scale, and setting range are shown below.

Density of gray level	Gray scale bit (1, 0) P7	P6	P5	P4	Gray scale bit (0, 1) P3	P2	P1	P0	Setting range (1,0)	(0,1)
Level 1 (light)	Setting disabled				0	0	0	1	—	▲
	0	0	1	0	0	0	1	0	▲	▲
	0	0	1	1	0	0	1	1	▲	▲
	0	1	0	0	0	1	0	0	▲	▲
↓		⋮				⋮			▲	▲
	1	0	1	1	1	0	1	1	▲	▲
	1	1	0	0	1	1	0	0	▲	▲
	1	1	0	1	1	1	0	1	▲	▲
Level 14 (dark)	1	1	1	0	Setting disabled				▼	—

Note: Set so that the density of gray scale bits (1, 0) and (0, 1) will not be reversed.

Note: After resetting by the $\overline{RES}$ pin, the density is set to gray scale bit (1,0): (0, 1, 0, 1) and gray scale bit (0, 1): (0, 0, 1, 0).

(16) Select FRM Pallet

This command is used to switch FRM pattern group (pallet).

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	1	1	1	1	1	1	0	Set mode
1	1	0	*	*	*	*	*	*	*	P0	Set register

Note: An asterisk (*) denotes invalid bit.

Relationship between the register value with the set register and pallet is shown below.

P0	Pallet
0	Pallet 0
1	Pallet 1

Note: After resetting by the $\overline{RES}$ pin, the number is set to Pallet 0.

Relationship between density of gray level setting with the set gray scale pattern command and pallet is shown below.

Density of gray level	Set register value with the set gray scale pattern command	Density	
		Pallet 0	Pallet 1
Level 1 (light)	01h	1 / 10 = 10%	1 / 6 = 17%
Level 2	02h	1 / 7 = 14%	1 / 5 = 20%
Level 3	03h	1 / 5 = 20%	1 / 4 = 25%
Level 4	04h	1 / 4 = 25%	1 / 3 = 33%
Level 5	05h	3 / 10 = 30%	2 / 5 = 40%
Level 6	06h	3 / 8 = 38%	3 / 7 = 43%
Level 7	07h	3 / 7 = 43%	2 / 4 = 50%
Level 8	08h	2 / 4 = 50%	4 / 7 = 57%
Level 9	09h	4 / 7 = 57%	3 / 5 = 60%
Level 10	0Ah	5 / 8 = 63%	2 / 3 = 67%
Level 11	0Bh	2 / 3 = 67%	5 / 7 = 71%
Level 12	0Ch	3 / 4 = 75%	3 / 4 = 75%
Level 13	0Dh	5 / 6 = 83%	4 / 5 = 80%
Level 14 (dark)	0Eh	9 / 10 = 90%	5 / 6 = 83%

(17) Set display lines

This command allows change of display lines. Setting the start point (block) displays in the desired location on the panel (continuous COM pin in 4 lines).

Be sure to set both parameters continuously, because this command uses both parameters of the display lines and start point (block) in a pair.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	1	1	0	1	Set mode
1	1	0	*	*	P15	P14	P13	P12	P11	P10	Display lines Set register
1	1	0	*	*	P25	P24	P23	P22	P21	P20	Set start point Set register

Note: An asterisk (*) denotes invalid bit.

Set display line register

The number of display lines can be set from 4 to 184 in steps of 4 lines. Adjust the crystal liquid drive voltage that attains optimal display contrast by adjusting to the change of the number of display lines.

Relationship between the register value with set register and the number of display lines is as follows:

P15	P14	P13	P12	P11	P10	Number of display lines
0	0	0	0	0	0	4
0	0	0	0	0	1	8
		↓				↓
1	0	1	1	0	0	180
1	0	1	1	0	1	184

Note: After resetting by the $\overline{RES}$ pin, the number is set to 184 lines.
Note: Register setting at (1, 0, 1, 1, 1, 0) or higher is not allowed.

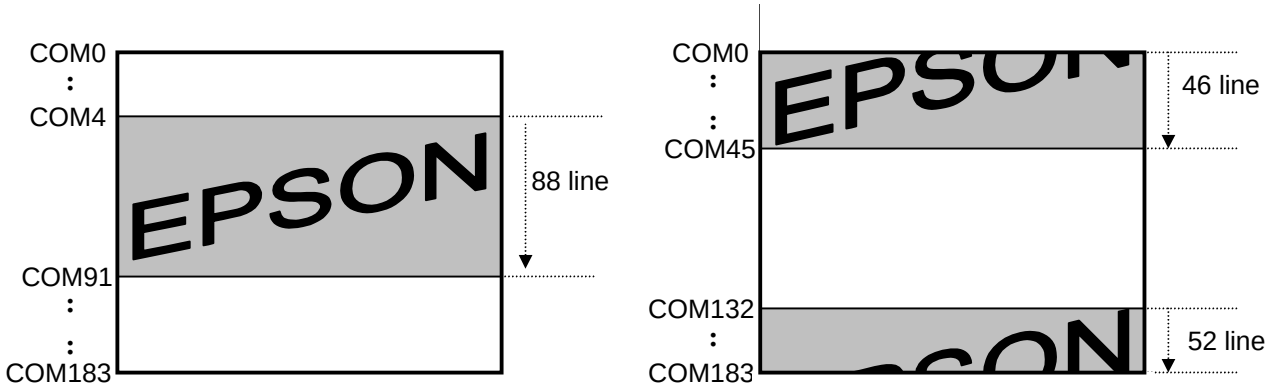
Set start point (block) register

Setting 8-bit data in the start point (block) register with this parameter takes one block out of 45 start point blocks. To scroll display, use (5) Set display start line command instead of this command.

P25	P24	P23	P22	P21	P20	Set start point	
						Common Output State: Normal Drive, Normal scan direction	Common Output State: Normal Drive, Reverse scan direction
0	0	0	0	0	0	0 (COM0～3)	45 (COM183～180)
0	0	0	0	0	1	1 (COM4～7)	44 (COM179～176)
0	0	0	0	1	0	2 (COM8～11)	43 (COM175～172)
		↓				↓	↓
1	0	1	1	0	0	44 (COM176～179)	1 (COM7～4)
1	0	1	1	0	1	45 (COM180～183)	0 (COM3～0)

* After reset by RES pin, the start point is below.
・Common output state: Normal driving, Normal scan direction, Block 0.
* Prohibit (1, 0, 1, 1, 1, 0) or upper value.

[Setup example of set the number of display line command]
Setup example 1: Select common output state: normal drive, normal scanning direction
When the display is set to 88 lines and the start point is to 1 (COM4 to 7), the display of 88 lines appears from COM4.
Setup example 2: Select common output state: normal drive, normal scanning direction
When the display is set to 88 lines and the start point is to 33 (COM132 to 135), the display of 88 lines appears from COM132. COM183 is followed by COM0.



Setup example 1 Setup example 2

Fig.7.2 Image of Correspondence between COM Output and the Number of Display Lines

(18) Read-modify-write

This command is used with the end command in a pair. Once this command is input, the column address will not be changed with the read display data command but incremented by +1 only with the write display data. This state is held until the end command is input.

Inputting the end command returns the column address to the address at the time of inputting the read-modify-write command. This function lessens the load from MPU when repeatedly changing data in the specific display area like blinking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

The command other than read/write display command can be used even in the read-modify-write mode. The page address set command and column address set command.

Sequence of cursor display

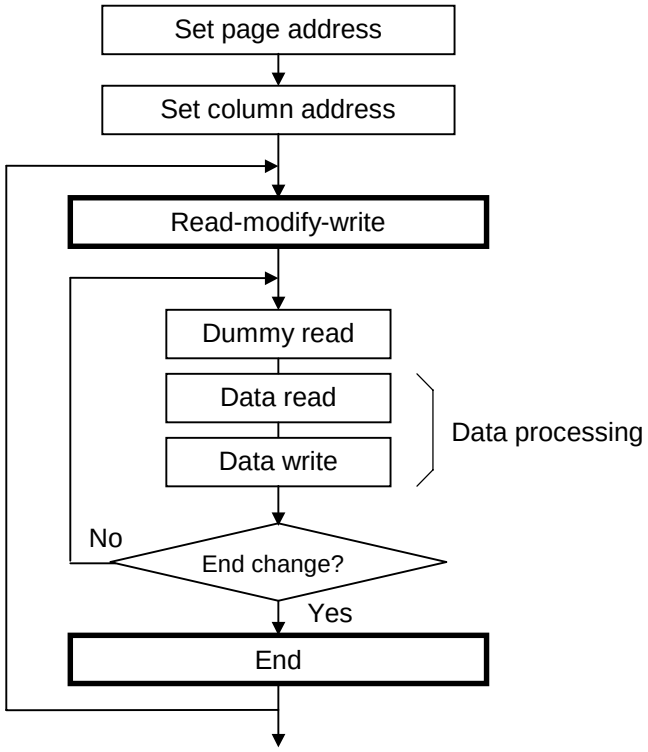


Fig.7.3 Sequence of Cursor Display

(19) End

This command clears the read-modify-write mode and returns the page address and column address to the initial address of the mode.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

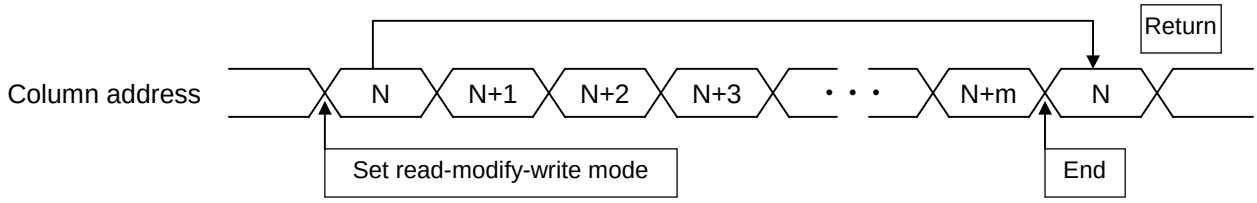


Fig.7.4 Addressing During Read-Modify-Write

(20) Built-in oscillation circuit ON/OFF

This command starts operation of the built-in oscillation circuit. This command is enabled on when the master operation (M/S = HIGH) and built-in oscillation circuit enabled (CLS = HIGH).

The liquid crystal display circuit operate in synchronization with the built-in oscillation circuit. To turn off the built-in oscillation circuit, stop the built-in power supply circuit and liquid crystal display circuit using the set power control command and display OFF command and then discharge the capacitor using the discharge ON command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Built-in oscillation circuit
0	1	0	1	0	1	0	1	0	1	0	OFF
										1	ON

(21) Select clock frequency

This command sets the dividing ratio of the internal clock f_{CL} to the built-in oscillation circuit frequency f_{OSC}. Enabled only when the built-in oscillation circuit is ON.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	0	1	1	1	1	1	Set mode
1	1	0	*	*	*	*	P3	P2	P1	P0	Set register

Note: An asterisk (*) denotes invalid bit.

Relationship between the register value with the set register and internal clock frequency when the built-in oscillation circuit is used is as follows:

Target value

P3	P2	P1	P0	Internal clock frequency	Frame frequency f_{FR} [Hz]			
				f_{CL} [kHz]	184 lines	160 lines	128 lines	96 lines
0	0	0	0	80.0	217	250	313	417
0	0	0	1	71.1	193	222	278	370
0	0	1	0	64.0	174	200	250	333
0	0	1	1	58.2	158	182	227	303
0	1	0	0	53.3	145	167	208	278
0	1	0	1	49.2	134	154	192	256
0	1	1	0	45.7	124	143	179	238
0	1	1	1	42.7	116	133	167	222
1	0	0	0	40.0	109	125	156	208
1	0	0	1	35.6	97	111	139	185
1	0	1	0	32.0	87	100	125	167
1	0	1	1	29.1	79	91	114	152
1	1	0	0	26.7	72	83	104	139
1	1	0	1	24.6	67	77	96	128
1	1	1	0	22.9	62	71	89	119
1	1	1	1	21.3	58	67	83	111

* After resetting by the $\overline{RES}$ pin, it is set to (0, 1, 0, 0).
* Indicates the typical value at 25°C.

(22) Discharge ON/OFF

This command allows the capacitor connected to the power supply circuit to be discharged, which is required for the following instances.

- When turning off the system power supply V_{DD}-V_{SS}
- When changing the number of display lines

See (4) When changing the number of display lines and (5) Power supply OFF in 7.3 Setup Example of Instructions (Reference Example).

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	1	0	1	0	1	0	Discharge OFF
										1	Discharge ON

*: Set to discharge ON during reset by the $\overline{RES}$ pin and set to discharge OFF after clearing reset.

This command short-circuits each liquid crystal drive voltages to V_{SSH} with switching elements. Be sure to execute this command after turning off the external power supply to avoid possible breakdown caused by over current.

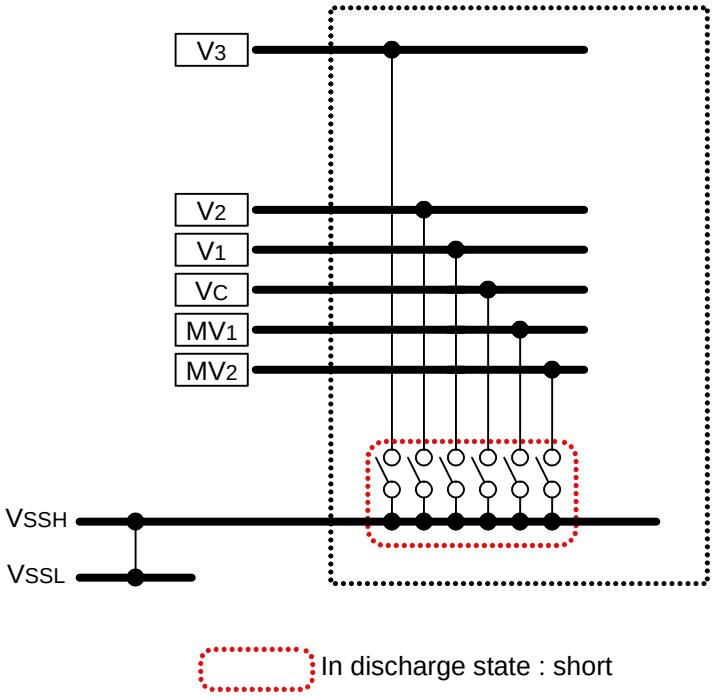


Fig.7.5 Location of Switching Elements for Discharge

(23) Power-saving

This commands places the IC in the power-saving mode. When all operations of the LCD system are stopped and there is no access from the MPU, current consumption can be reduced to the value close to static current.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Power-saving mode
0	1	0	1	0	1	0	1	0	0	0	OFF
										1	ON

*: After resetting by the $\overline{RES}$ pin, it is set to power-saving OFF.

In the power-saving condition, display data and operating state before starting power save command is held and display data RAM is accessible from MPU.

The power save OFF command is used to cancel the power-saving condition and reset to the state prior to starting power save command.

In the power-saving mode,

- The built-in oscillation circuit is stopped.
- All the liquid crystal drive circuits are stopped (V_C level is output from all SEG/COM.)
- The temperature sensor circuit and V_{DI} generation circuit operate.

It is recommended to stop the function of the external power supply circuit when starting the power save function. For example, if each level of the liquid crystal drive voltage is provided in the external resistive division circuit, it is recommended to add a circuits that cuts current flowing into the resistive division circuit when starting the power save function. It is recommended to quit the power saving-state, goes power-saving OFF after turing the external power circuit ON and stabilized it.

Power-save ON/OFF sequence

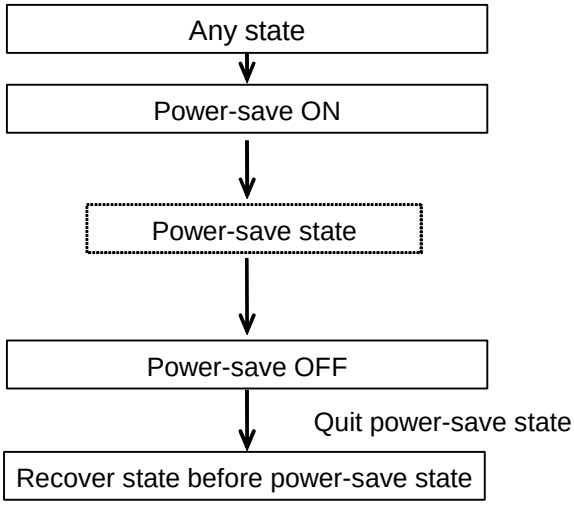


Fig.7.6 Power-save ON/OFF sequence

* In power-save state, it is recommended to stop external power supply circuit. For example, in case of input LCD Bias voltages by external ladder resistances, it is recommended to add cut-off circuit to the ladder resistances. To recover from power-save state to normal state, quit power-save state after external power supply circuit ON and stable.

(24) Read status

This command allows detection of bit error of the specific command register, caused by excessive external noise or the like.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	1	1	0	Set mode
1	0	1	*	*	*	*	*	*	*	P0	Register read

*: An asterisk (*) denotes invalid bit.

Description of the register value P0 that were read is given below:

Results of reading	Description
LOW	Error not detected.
HIGH	A bit-flip of part of the command register occurred, which could be a cause of disabled normal display. Re-execute all the commands.

The commands that support error detection of the register are

- Display ON/OFF
- Built-in oscillation circuit ON/OFF
- Full display lighting ON/OFF
- Display normal/inverted
- TEST1 set

The five commands above can be used to detect an error when a bit-flip occurred in any of the specified registers. When those five commands are executed and operated normally, LOW is output.

When the IC is placed in the reset condition because of external noise or the like, it can also be detected as an error. So the register P0 will be set to HIGH after resetting by a pin. Therefore, in normal operation sequence, the above five commands must be set in the register again before executing read status.

For example, even if the built-in oscillation circuit is not used, execute the "built-in oscillation circuit OFF command". Perform read status after executing all the five commands above (for the function not to be used, execute the OFF command).

This command is used to conduct self-check on a specific error mode, but not used to detect all errors. Even if the result of read status is "normal" because of an influence of excessive external noise, it could have gone into malfunction mode of some sort that is not detected by this command. It is recommended to refresh the state regularly instead of relying on the result of read status. Moreover, garbled bit data of display data RAM may have been caused when an error was detected. So it is also recommended to refresh the data of the display data RAM.

Since the register P0 level is output from the pin ERR, the operating state can be checked without executing a command. For ERR output operating conditions and precautions, conform to the above read status command.

(25) Temperature sensor ON/OFF

This command allows specification of the temperature sensor ON/OFF. For more information, see 6.10 Temperature Sensor Circuit in FUNCTIONAL DESCRIPTION.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	1	0	0	0	Temperature sensor OFF
										1	Temperature sensor ON

*: After resetting by the $\overline{RES}$ pin, the temperature sensor is set to OFF.

Setting the temperature sensor to ON is no problem when the temperature sensor is not use. However, operating current of the temperature sensor is steadily consumed.

The temperature sensor circuit is controlled independently of the power save command. To reduce current consumption during power saving, set the temperature sensor to OFF using this command.

(26) Select MLS drive

This command is used for selecting the MLS drive and method of AC drive. It should be selected according to display quality on actual display patterns.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	1	1	0	0	1	1	1	Set mode
1	1	0	0	0	0	P4	P3	0	1	1	Set register.

P4	P3	-	-	-	MLS drive
0	-	-	-	-	N-line/frame inversion overlap OFF
1	-	-	-	-	N-line/frame inversion overlap ON
-	0	-	-	-	Dispersion drive
-	1	-	-	-	Non-dispersion drive

*: After resetting by the $\overline{RES}$ pin, it is set to N-line frame in version overlap OFF and non-dispersion drive.

◆ N-line frame inversion overlap ON / OFF

This function is controlled by parameter P4. It is valid only in "n-line inverted drive ON".

It may cause dark / light stripes on the display due to occur AC drive deflection depend on combination of number of display lines and number of n-line inverted drive. This function reduces the AC drive defledction therefore reduce the dark / light stripes.

◆ Dispersion / Non-dispersion drive

This function is controlled by parameter P3. The S1D15722 uses 4 line MLS drive method, and common

output pins output 4 lines of select-signal at once, 4 times / 1frame.
When non-dispersion drive is selected, the common outputs output select-signal 4 times continuously. If display content is changed frequently, it is recommended to use the non-dispersion drive.
When dispersion drive is selected, the common outputs output select-signal 4 times dispersively in one frame. The dispersion drive can get higher contrast than non-dispersion drive in theory, however the dispersion drive may cause a flicker in case to display moving pictures.

Anyway, it is recommended to decide above both functions ON/OFF after evaluate display quality totally like as flicker, crosstalk and so on, with actual display patterns.
Optimum frame frequency may be changed depend on these function ON/OFF, therefore display quality evaluation with various frame frequency is also recommended. Frame frequency can be changed by "Select clock frequency" command or external clock frequency.

(27) NOP

Command for Non-Operation.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(28) TEST1

Command for IC chip testing. Do not use. If this command is executed, the IC goes into test mode. If the IC goes into test mode by mistake, execute the NOP command to clear test mode.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	0	0	1	0	1	Set mode
1	1	0	0	0	0	0	0	0	0	0	Set register

*: It is set to (0,0,0,0,0,0,0,0) after reset by RESET pin.

(29) TEST2

Command for IC chip testing. Do not use. If this command is executed, the IC goes into test mode. If the IC goes into test mode by mistake, execute the NOP command to clear test mode.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	1	1	1	0	*	*	*	Set mode
0	1	0	1	1	1	1	1	1	1	1	Set register

*: An asterisk (*) denotes invalid bit.

(30) TEST3

Command for IC chip testing. Do not use. If this command is executed, the IC goes into test mode. If the IC goes into test mode by mistake, execute the NOP command to clear test mode.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	1	1	1	Set mode

7.2 Command Table

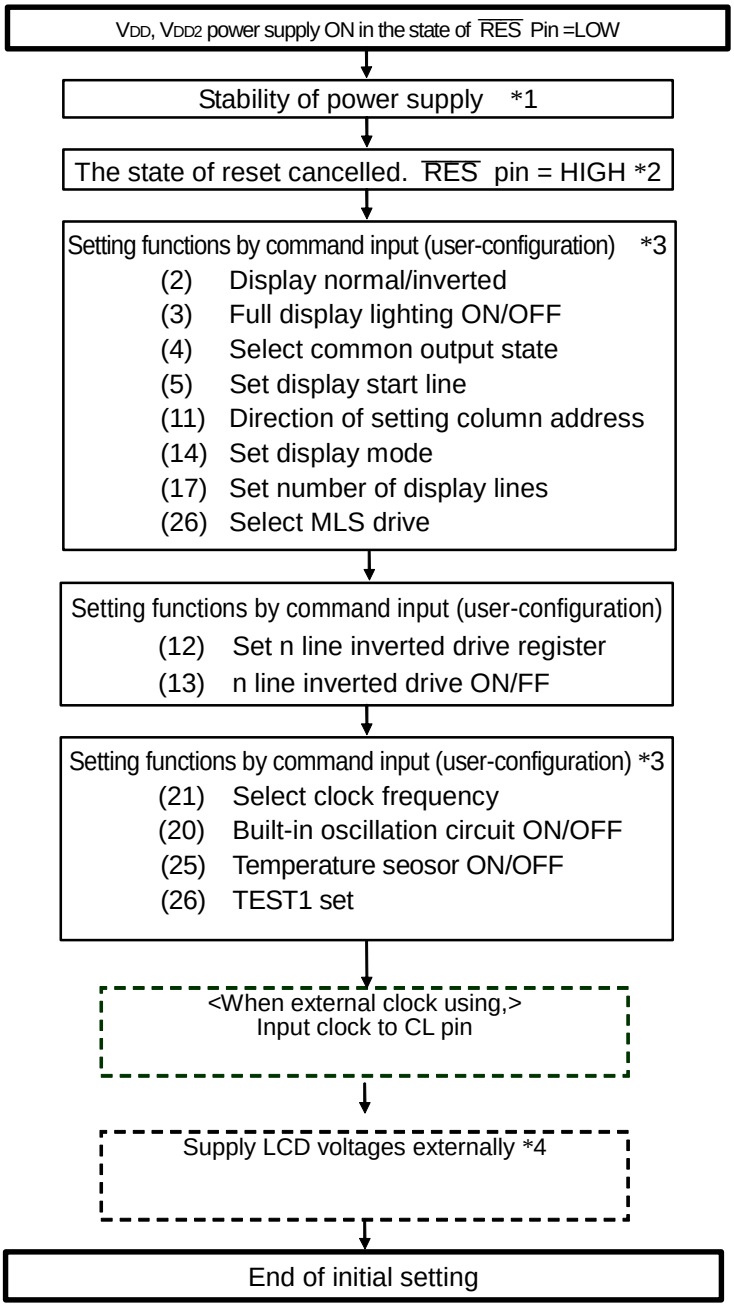
Table 7.1

Command	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD ON/OFF 0: OFF, 1: ON
(2) Display normal/inverted	0	1	0	1	0	1	0	0	1	1	0 1	LCD normal/inverted 0: Normal, 1: Inverted
(3) Full display lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Full display lighting 0: Normal display, 1: Full ON
(4) Select common output state	0 1	1 1	0 0	1	1	0	0	0	1 Output state	0	0	Selects COM output method.
(5) Set display start line	0 1	1 1	0 0	1 *	0	0 Display start line address	0	1	0	1	0	Sets the display start line.
(6) Set page address	0 1	1 1	0 0	1 *	0 *	1	1 Page address	0	0	0	1	Sets the display RAM page address.
(7) Set column address	0 1	1 1	0 0	0	0	0 Set column address	1	0	0	1	1	Sets the display RAM column address.
(8) Write display data	0 1	1 1	0 0	0	0	0	1 Write data	1	1	0	1	Writes to display RAM.
(9) Read display data	0 1	1 0	0 1	0	0	0	1 Read data	1	1	0	0	Reads to display RAM.
(10) Select display data input direction	0	1	0	1	0	0	0	0	1	0	0 1	Display RAM data input direction 0: Column direction, 1: Page direction
(11) Direction of setting column address	0	1	0	1	0	1	0	0	0	0	0 1	Supports SEG output of the display RAM column address 0: Normal, 1: Inverted
(12) Set n line inverted drive register	0 1	1 1	0 0	0 *	0 *	1 Number of inverted lines	1	0	1	1	0	Set the number of lines of n line inverted drive
(13) n line inverted drive ON/FF	0	1	0	1	1	1	0	0	1	0	0 1	n line inverted drive ON/FF 0: OFF, 1: ON
(14) Set display mode	0 1	1 1	0 0	0 *	1 *	1 *	0 *	0 *	1 *	1 Mode	0	Select 4-gray scale display/binary display 00: 4-gray scale, 01: binary
(15) Set gray scale pattern	0 1	1 1	0 0	0	0	1 Gray scale pattern	1	1	0	0	1	Selects the density of the gray scale bits (1,0), (0,1)
(16) Select FRM Pallet	0 1	1 1	0 0	1 *	1 *	1 *	1 *	1 *	1 *	1 *	0 PL	Selects FRM Pallet PL=0: Pallet 0 PL=1: Pallet 1
(17) Set display line	0 1 1	1 1 1	0 0 0	0 * *	1 *	1 Number of display lines Start point	0	1	1	0	1	Sets the number of display lines and start address.
(18) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. When writing: +1, when reading: 0
(19) End	0	1	0	1	1	1	0	1	1	1	0	Cancels read-modify-write
(20) Built-in oscillation circuit ON/OFF	0	1	0	1	0	1	0	1	0	1	0 1	Operation of the built-in CR oscillation circuit 0: OFF, 1: ON
(21) Select clock frequency	0 1	1 1	0 0	0 *	1 *	0 *	1 *	1 Frequency value	1	1	1	Sets the dividing ratio of the internal clock frequency f_{OSC}.
(22) Discharge ON/OFF	0	1	0	1	1	1	0	1	0	1	0 1	Discharges the capacitor connected to the power supply circuit 0: OFF, 1:ON
(23) Power save ON/OFF	0	1	0	1	0	1	0	1	0	0	0 1	Power save 0: OFF, 1: ON
(24) Read status	0 1	1 0	0 1	1 *	0 *	0 *	0 *	1 *	1 *	1 *	0 ST	Outputs the result of detecting bit error to ERR bus
(25) Temperature sensor ON/OFF	0	1	0	0	1	1	0	1	0	0	0 1	Operation of the temperature sensor 0: OFF, 1: ON

Command	Command Code										Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(26) Select MLS drive	0	1	0	1	1	1	0	0	1	1	1	P4/ N-line frame inv. Overlap 0:OFF 1:ON
	1	1	0	0	0	0	P4	P3	0	1	1	P3/ 0: Dispersion, 1: Non-dispersion
(27) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for Non-Operation.
(28) TEST1	0	1	0	0	0	1	0	0	1	0	1	Command for testing IC chip.
	0	1	0	0	0	0	0	0	0	0	0	(Prohibit)
(29) TEST2	0	1	0	1	1	1	1	0	*	*	*	Command for testing IC chip.
	0	1	0	1	1	1	1	1	1	1	1	(Prohibit)
(30) TEST3	0	1	0	1	0	0	0	1	1	1	1	Command for testing IC chip. (Prohibit)

7.3 Example of Setting Instructions (Reference Example)

(1) Initial setting



Numbers in parentheses correspond to those in the item of command description.

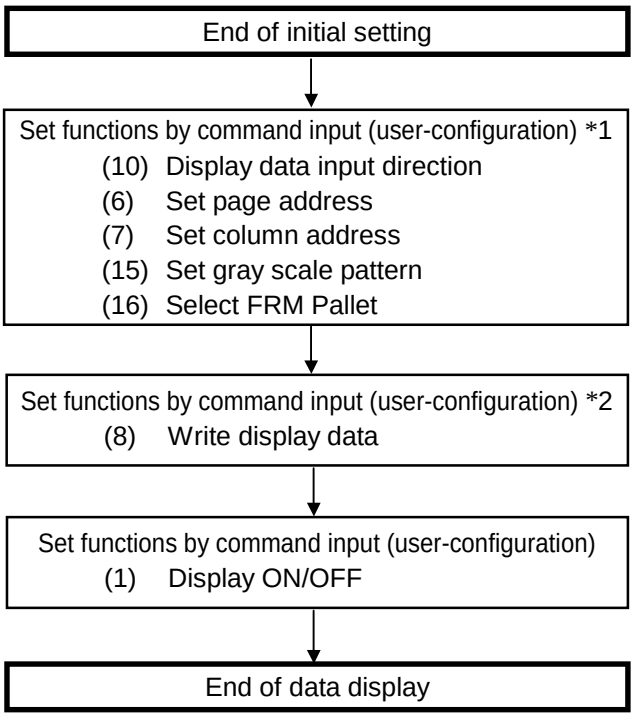
*1: Consideration must be given to the wait time until the internal generation V_{DI} voltage is stabilized. The wait time varies with external circuit, depending on the capacity between V_{DI} and V_{SS}. Therefore, evaluate and set with sufficient margin.
Reference: When V_{DD} = 5V and V_{DI} stabilizing capacity at 4.7 μF, the wait time = 5 mS.
(The wait time is inversely proportional to the V_{DD} voltage, but proportional to the V_{DI} stabilizing capacity.)

*2: The contents of the display data RAM are undefined even in the state of initial setting following reset.

*3: Execute the OFF command when performing initial setting and refreshing even if it is set to non-use of each function, so that a recovery can be made from a sudden change of internal state resulted from excessive external noise.
Likewise, for the command used for setting the register value, reset the register when performing initial setting and refreshing even if default values after reset are used as they are.

*4: LCD voltages (V_3 to MV_2) are sure to supply all at the same timing.

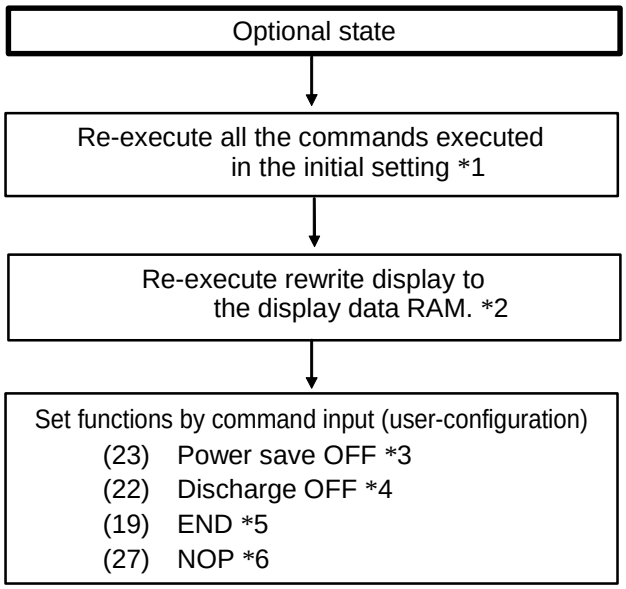
(2) Data display



*1 Reset the register when performing initial setting and refreshing even if it is set to use default values as they are, so that a recovery can be made from a sudden change of internal state resulted from excessive external noise.

*2 The contents of the display data RAM are undefined after completion of initial setting. Write data all the display data RAMs to be used for display.

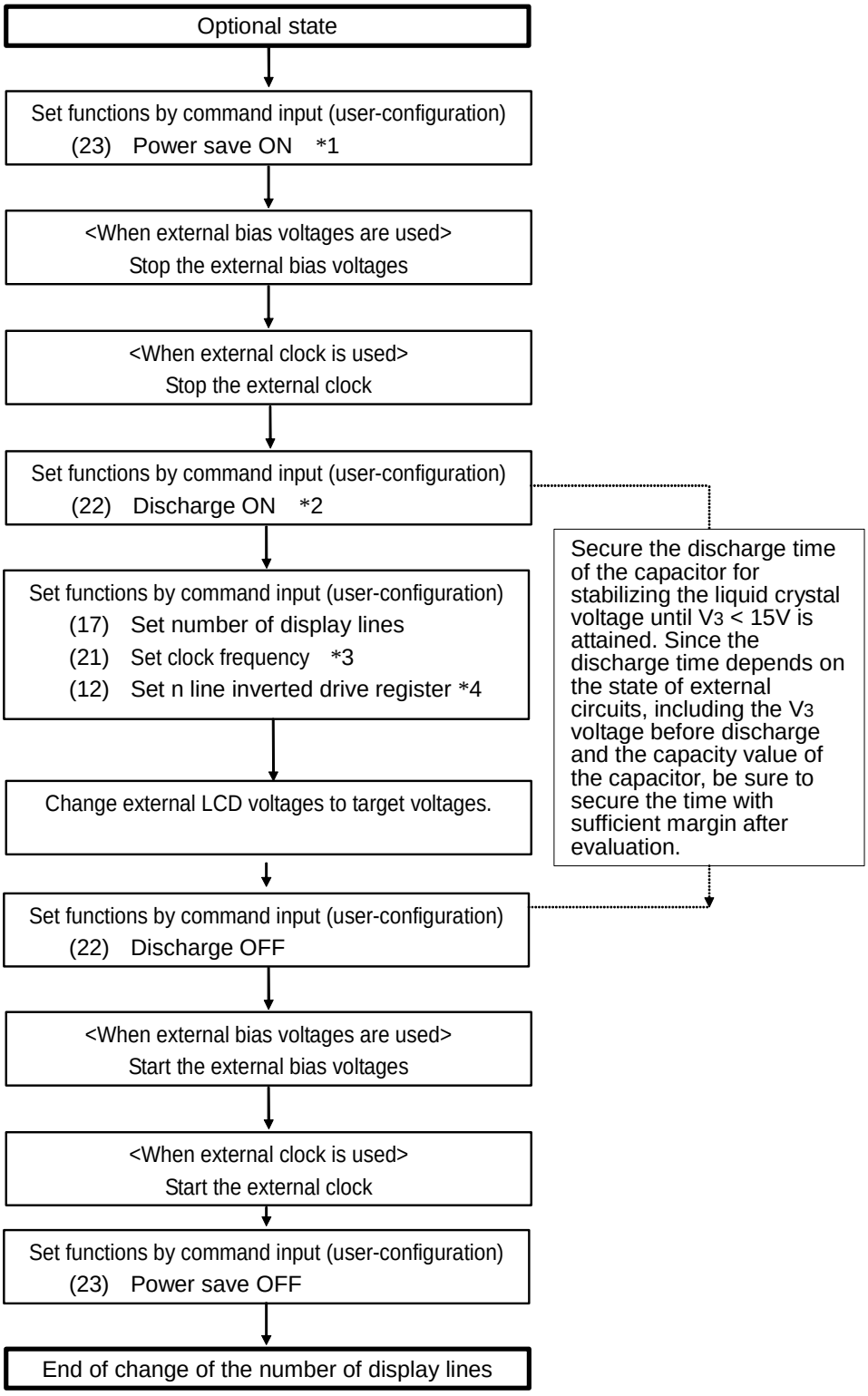
(3) Refresh



This IC holds the operating state by a command, however, it may change the internal state when excessive external noise enters. Measures are required to prevent noise generation or influence in terms of mounting and the system itself. To provide for a sudden, excessive external noise, it is recommended to refresh the operating state and the contents of display regularly.

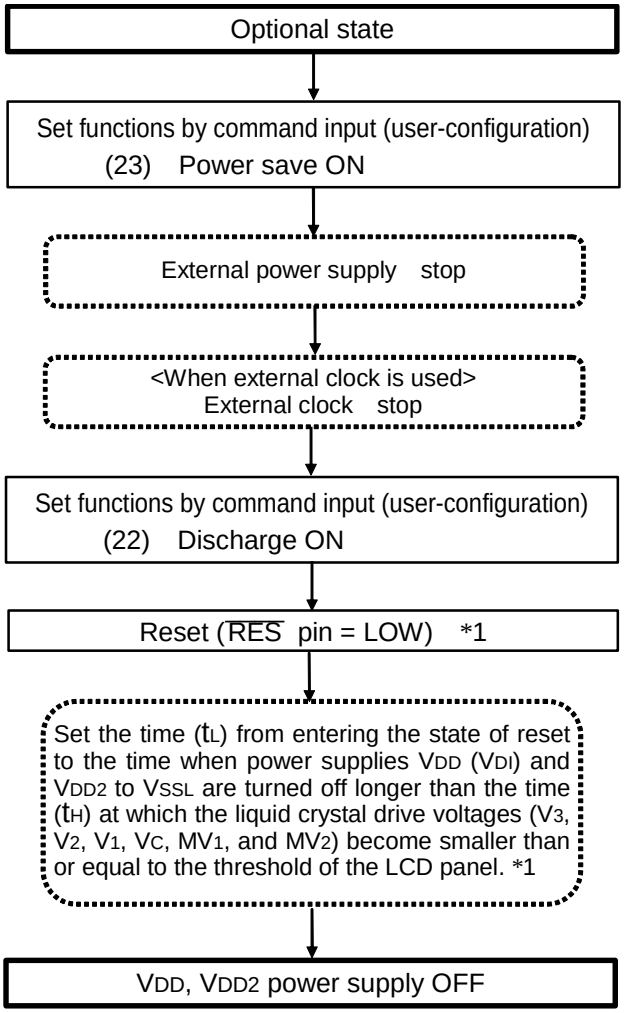
*1: (1) Initial setting reference
*2: (2) Data display reference
*3: When the IC chip enters the power-saving mode, the power save OFF command can be used to exit.
*4: When the IC chip goes into power-saving mode, the discharge OFF command can be used to exit.
*5: When the IC chip goes into read-modify-write mode, the end command can be used to exit.
*6: When the IC chip goes into test mode, the NOP command can be used to exit.

(4) When changing the number of display lines



*1: When the number of liquid crystal display lines is changed, the liquid crystal drive voltage from which optimal contrast is obtained changes. To avoid the problem of the display, for example, the display turns black for an instant, place in the power save mode in the above sequence and turn off the display once. Then set to obtain the optimal liquid crystal drive voltage before displaying again.
*2: To change the liquid crystal drive voltage, discharge the capacitor for holding the voltage once.
*3: Set to the number of frame frequency that won't cause display problem such as a flicker.
*4: Set to the number of n line inversions that won't cause display problem such as a flicker.

(5) Power supply OFF



This IC controls the circuits of the liquid crystal drive power supply system in the VDD, VDD2 to VSSL, and VSSH power supply circuits. If VDD, VDD2 to VSSL, and VSSH power supplies are cut off with the voltage remaining in the liquid crystal drive power supply system, the voltage that is not controlled will be output from the SEG and COM pins, which could cause display problem. Be sure to follow the above power supply OFF sequence.

*1: The threshold voltage of the LCD panel 1[V] serves as an index. Prevent VDD and VDD2 from becoming high impedance during discharge (reset).

8. ABSOLUTE MAXIMUM RATINGS

If not specified, particularly, $V_{SSL} = V_{SSH} = 0V$

Table 8.1

Item	Symbol	Standard value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to +6.0	V
Power supply voltage (2)	V_{DD2}	V_{DD} to +6.0	
Power supply voltage (3) during external input	V_{DI}	-0.3 to +4.0	
Power supply voltage (4)	V_3	-0.3 to +42.0	
Power supply voltage (5)	V_2, V_1, V_C, MV_1, MV_2	-0.3 to V_3	
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	
Output voltage	V_O	-0.3 to V_{DD}+0.3	
Operating temperature	T_{OPR}	-40 to +90	°C
Storage temperature Bare chip	T_{STR}	-55 to +125	

1: For the V_3, V_2, V_1, V_C, MV_1 and MV_2 voltages, be sure to satisfy the following conditions: $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq V_{SSL}, V_{SSH}$.

2: The use of IC exceeding the absolute maximum rating can cause permanent damage to the IC. During normal operation, electrical characteristics conditions should be observed. Failure to do so can cause malfunction of the IC and have adverse effect on the reliability of IC.

9. DC CHARACTERISTICS

If not specified, particularly: V_{SSL}, V_{SSH} = 0V, V_{DD} = 5.0V ± 10%, T_a = - 40 to 90°C

Table 9.1

Item		Symbol	Conditions		Standard value			Unit	Applicable pin
					Min.	Typ.	Max.		
Operating voltage (1)	Operable	V_{DD}	—		3.0	—	5.5	V	V_{DD} *1
Operating voltage (2)	Operable	V_{DD2}	—		3.0	—	5.5		V_{DD2}
Operating voltage (3)	Operable	V_{DI}	during slave external input T_a=25°C		—	2.85	—		V_{DI}
Operating voltage (4)	Operable	V_3	—		15.0	—	25.0		V_3 *2
High level input voltage		V_{IHC}	V_{DD}=3.0V to 5.5V		0.8xV_{DD}	—	V_{DD}		*3
Low level input voltage		V_{ILC}			V_{SSL}	—	0.2xV_{DD}		*3
High level output voltage		V_{OHC}	V_{DD}=3.0V	I_{OH}=-25µA	0.8xV_{DD}	—	V_{DD}		*4
Low level output voltage		V_{OLC}	to 5.5V	I_{OL}= 25µA	V_{SSL}	—	0.2xV_{DD}		*4
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		-1	—	1	µA	*5
Output leak current		I_{LO}			-1	—	1		*6
Liquid crystal driver ON resistance		R_{ON}	T_a=25°C	V_3= 15.0V	—	2.0	6.0	kΩ	SEGn
				V_3= 25.0V	—	0.6	3.0		COMn *7
Static power consumption		I_{DDQ}	T_a=25°C	V_{DD} = 3.0V	—	0.3	3	µA	V_{DD} *8
		I_{3Q}		V_3 = 16.0V	—	0.3	3		V_3
Input pin capacitance		C_{IN}	Ta=25°C, f=1MHz		—	4	12	pF	—
Oscillation frequency	Built-in oscillation	f_{OSC}	T_a = 25°C at maximum frequency		608	640	672	kHz	*9
	External input	f_{CLO}			—	—	160		

[References marked with an asterisk (*)]

*1 The IC operations are not guaranteed when rapid voltage fluctuations are observed during access from MPU.

*2 For operating voltage range of V_{DI} series and V_3 series, see Fig.9.4.

*3 A0, D0 to D7, SCL, SI, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS}$, CLS, CL, FR, F1, F2, SYNC, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, TEST pins

*4 D0 to D7, FR, $\overline{DOF}$, CL, F1, F2, SYNC, ERR, SI TEST2 pins

*5 A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), CLS, M/S, C86, P/S, RES, SCL, TEST pins

*6 Apply when D0 to D7, SI, CL, FR, $\overline{DOF}$, F1, F2, SYNC, ERR TEST2 pins are in the state of high impedance.

*7 Resistance value when the voltage of 0.1 V is applied between output pin SEGn or COMn and each power supply pin (V_3, V_2, V_1, V_C, MV_1, MV_2, V_{SSH}).
R_{ON} = 0.1V/ΔI (where ΔI is current flowing when 0.1 V is applied between power supply On.)

*8 Current value at V_{SIS} = LOW

*9 For relationship between the oscillation frequency and the frame frequency, see Table 9.7. The internal oscillation items indicates manufacturing variations in the built-in oscillation circuit while the external input item indicates the maximum operability.

9.1 Dynamic Current Consumption Value

9.1.1 When in normal operation.

Current value consumed by the entire IC at T_a = 25[°C] when the external power supply is use.

- Display mode 4-gray scale, f_{FR} = 80 Hz, no n line inversion, 1/13 bias, non-dispersion drive

Table 9.2 Display all white

V_{DD}	Booster magnification	V_3 voltage	Standard value				Unit	Remarks
			1/184 Duty		1/132 Duty			
			Typ.	Max.	Typ.	Max.		
5V	—	20	125	210	112	190	μA	*10
3V	—	20	110	185	100	170		

Table 9.3 Display Heavy Load Pattern

V_{DD}	Booster magnification	V_3 voltage	Standard value				Unit	Remarks
			1/184Duty		1/132 Duty			
			Typ.	Max.	Typ.	Max.		
5V	—	20	159	265	140	235	μA	*11
3V	—	20	148	250	130	220		

- Display mode binary, f_{FR} = 80 Hz, no n line inversion, 1/13 bias, non-dispersion drive

Table 9.4 Display all white

V_{DD}	Booster magnification	V_3 voltage	Standard value				Unit	Remarks
			1/184 Duty		1/132 Duty			
			Typ.	Max.	Typ.	Max.		
5V	—	20	133	225	114	190	μA	*10
3V	—	20	117	195	100	170		

Table 9.5 Display Heavy Load Pattern

V_{DD}	Booster magnification	V_3 voltage	Standard value				Unit	Remarks
			1/184 Duty		1/132 Duty			
			Typ.	Max.	Typ.	Max.		
5V	—	20	210	350	167	280	μA	*11
3V	—	20	200	335	159	265		

[References marked with an asterisk (*)]

*10 The built-in oscillation circuit is used and “0” is written to all the bits of the display data RAM and displayed. Current consumed by a single IC. Current related to LCD panel capacity and wiring capacity is not included. Applicable when no access is made from MPU.

*11 The built-in oscillation circuit is used and display data that makes current consumption maximum is written and displayed. Current consumed by a single IC. Current related to LCD panel capacity and wiring capacity is not included. Applicable when no access is made from MPU.

9.2 Current Consumption in the Power-saving Mode

- V_{DD} = 5V, T_a = 25°C

Table 9.6

Item	Symbol	Conditions	Standard value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	V_{DIS}= HIGH	—	36	72	μA	—
		V_{DIS}= LOW	—	0.3	3		

9.3 Reference Data

9.3.1 When in normal operation.

- V_{DD} = 5.0 V, Display mode 4-gray scale, f_{FR} = 100 Hz, no n line inversion, 1/13 bias, non-dispersion drive, T_a = 25°C.

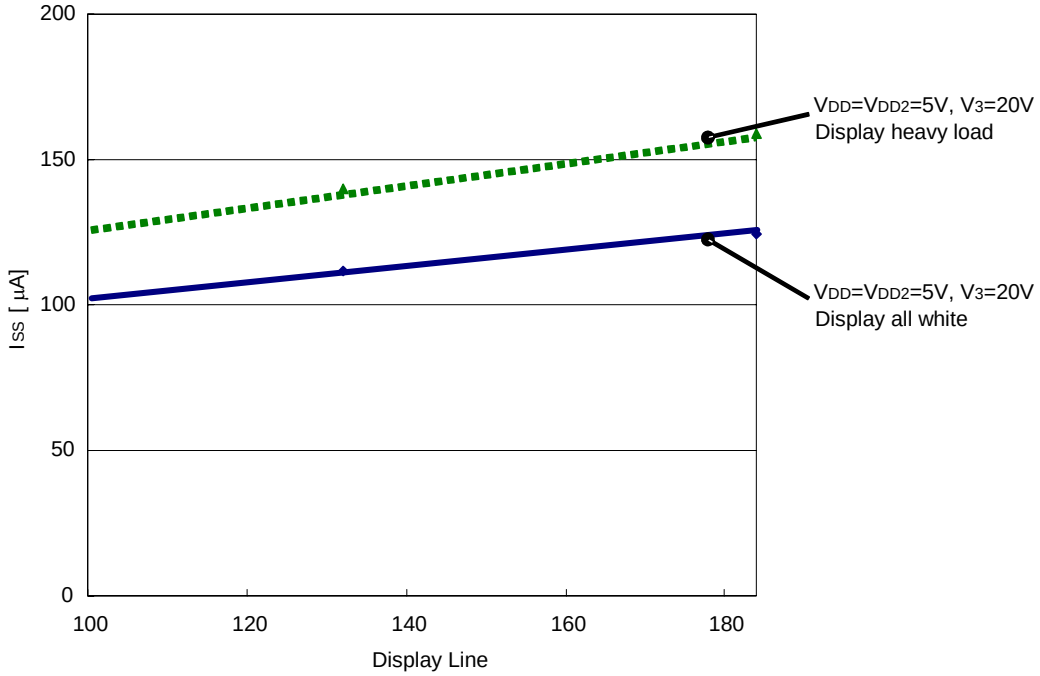


Fig.9.1

- V_{DD} = 5.0 V, Display mode binary, f_{FR} = 100 Hz, no n line inversion, 1/13 bias, non-dispersion drive, T_a = 25°C.

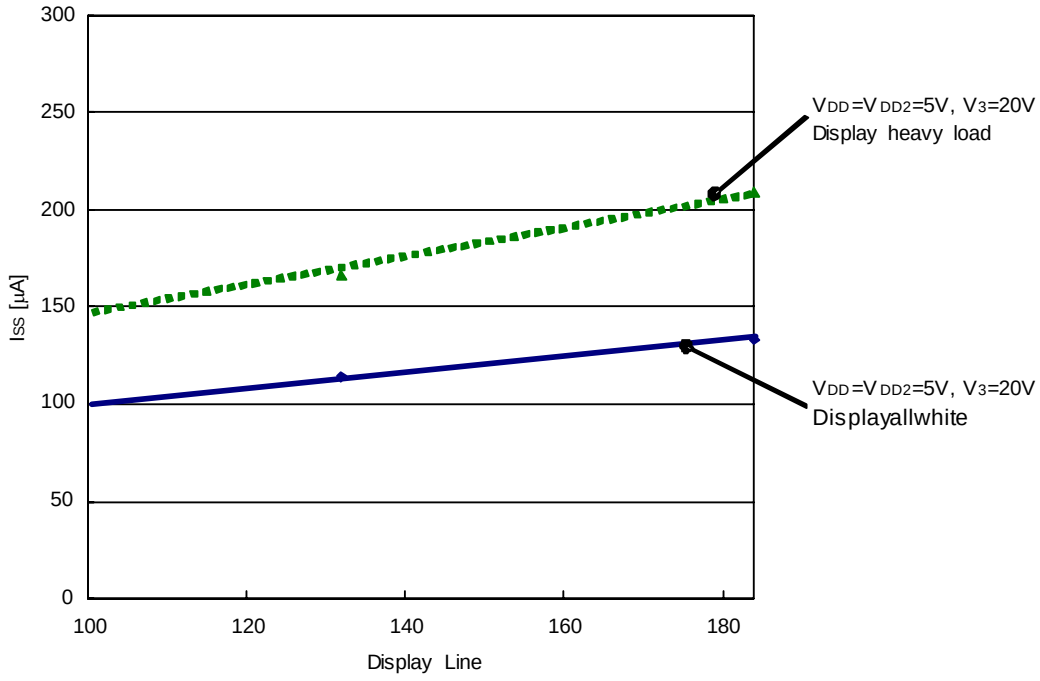


Fig.9.2

9.3.2 During MPU access

- Current consumption by a single IC when the display heavy load pattern is written in f_{CYC}.
  V_{DD} = 5V, V_3 = 25V, f_{FR} = 100 Hz, no n line inversion, built-in power supply OFF, 1/13 bias, non-dispersion drive, display ON, T_a = 25°C.

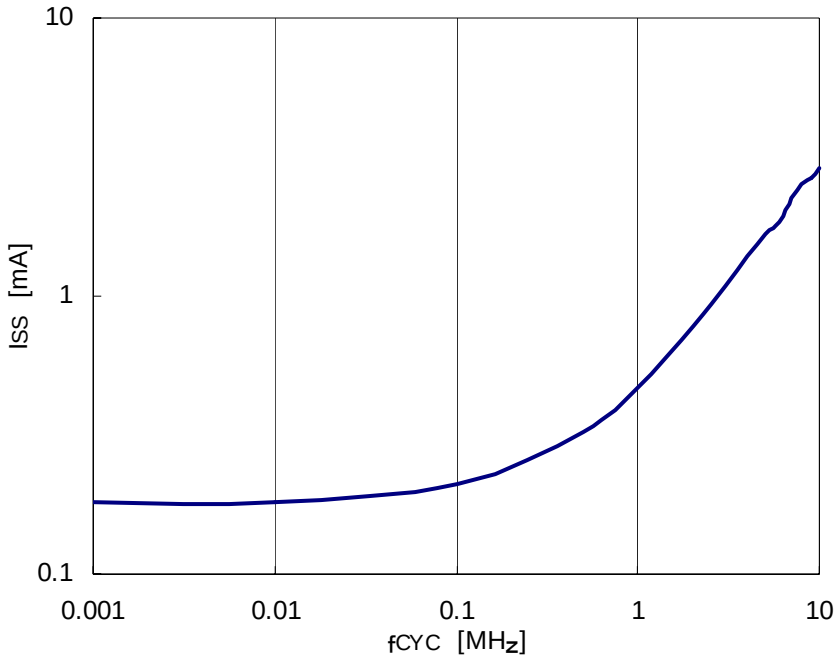


Fig.9.3

9.3.3 Operating Voltage Rage of V_{DI} Series and V_3 Series

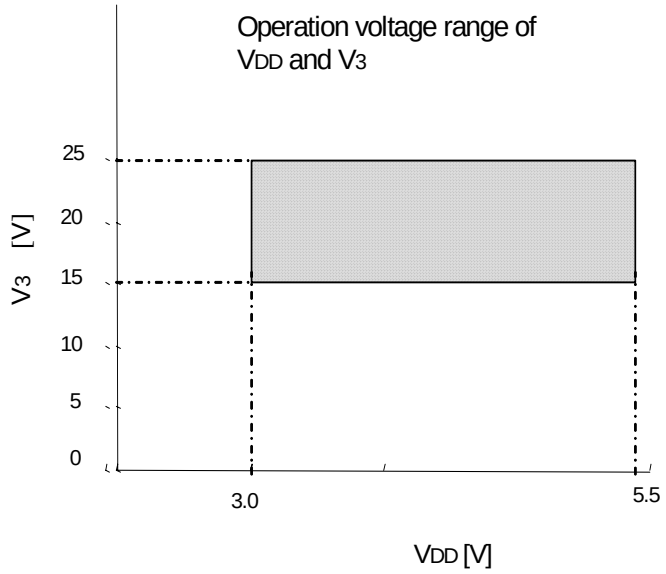


Fig.9.4

9.3.4 Liquid Crystal Frame Frequency f_{FR}

- When the number of display lines is set to *1*

Table 9.7

Item	Display clock frequency f_{CL}	Frame frequency f_{FR}
Built-in oscillation circuit is used.	See command#21.	$f_{FR} = \frac{f_{CL}/2}{1}$
Built-in oscillation circuit is not used.	External input (f_{CL})	

- 2 CL clock correspond to 1 common line scanned period.
- Frame frequency indicates the frequency that rewrites 1 frame, but it does not indicate a signal (= a cycle of AC drive) from the FR pin.

9.4 Temperature Sensor Characteristics

9.4.1 Analog Voltage Output Characteristics

Table 9.8

Item	Symbol	Conditions	Standard value			Unit	Applicable pin
			Min.	Typ.	Max.		
Operating Voltage range	V_{SV}	—	3.0	—	5.5	V	V_{DD} *16
Operating temperature range	Ta	—	-40	—	90	°C	
Temperature accuracy	T_{ACCA}	TBD to TBD°C	-5	—	+5	°C	SVD2 *12, *13
Output voltage	V_{SVD2}	-40°C 25°C 90°C	1.490 1.185 0.857	1.467 1.160 0.831	1.444 1.136 0.805	V	SVD2 *12, *13
Output voltage temperature gradient	V_{GRA}	*14	—	-5.06	—	mV/°C	SVD2 *12, *13
Output voltage setup time	t_{SEN}	*15	100	—	—	ms	SVD2 *12, *15
Operating current	I_{SEN}	25°C	—	100	250	μA	V_{DD} *16

[References marked with an asterisk (*)]

*12: To obtain an accurate output voltage value, it should be noted that current path and capacity must not be provided between the SVD2 and V_{DD}, V_{DI}, V_{DD2}.

*13: The curve of the sensor analog output voltage SVD2 is approximated by the following expression.

$$V_{SVD2} = -2.641\times10^{-6} \bullet T^2 - 4.763\times10^{-3} \bullet T + 1.281[V] \qquad \text{(Expression 9.1)}$$

The accuracy is ±5 °C at -40 to 90 °C.

*14: It is temperature gradient of V_{SVD2} output approximation strait line. Accuracy of analog sensor output is caliculated as following.

$\Delta V_{SVD2} = \pm(5.06 \times 5) \cong \pm 25[mV]$

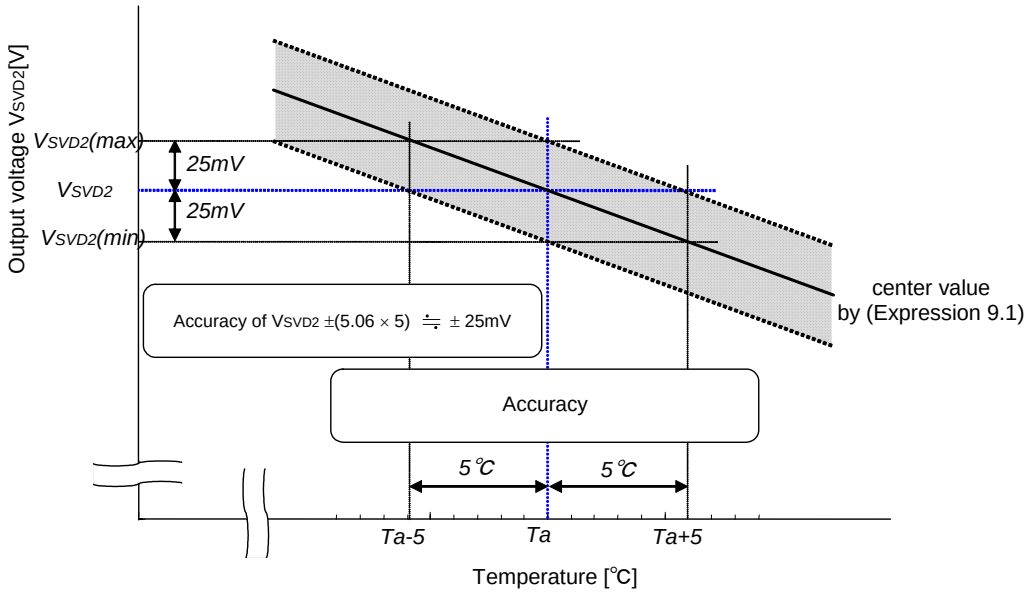


Fig.9.5

*15: The wait time after inputting the temperature sensor ON command until the output voltage can be monitored steadily. It is applied not to connect capacitance to SVD2 pin. Be sure to sample the output voltage after a fixed wait time or longer.

*16: Include operating current of built-in V_{DI} generating circuit.

10. TIMING CHARACTERISTICS

10.1 System Bus Read/Write Characteristics 1 (80 Series MPU)

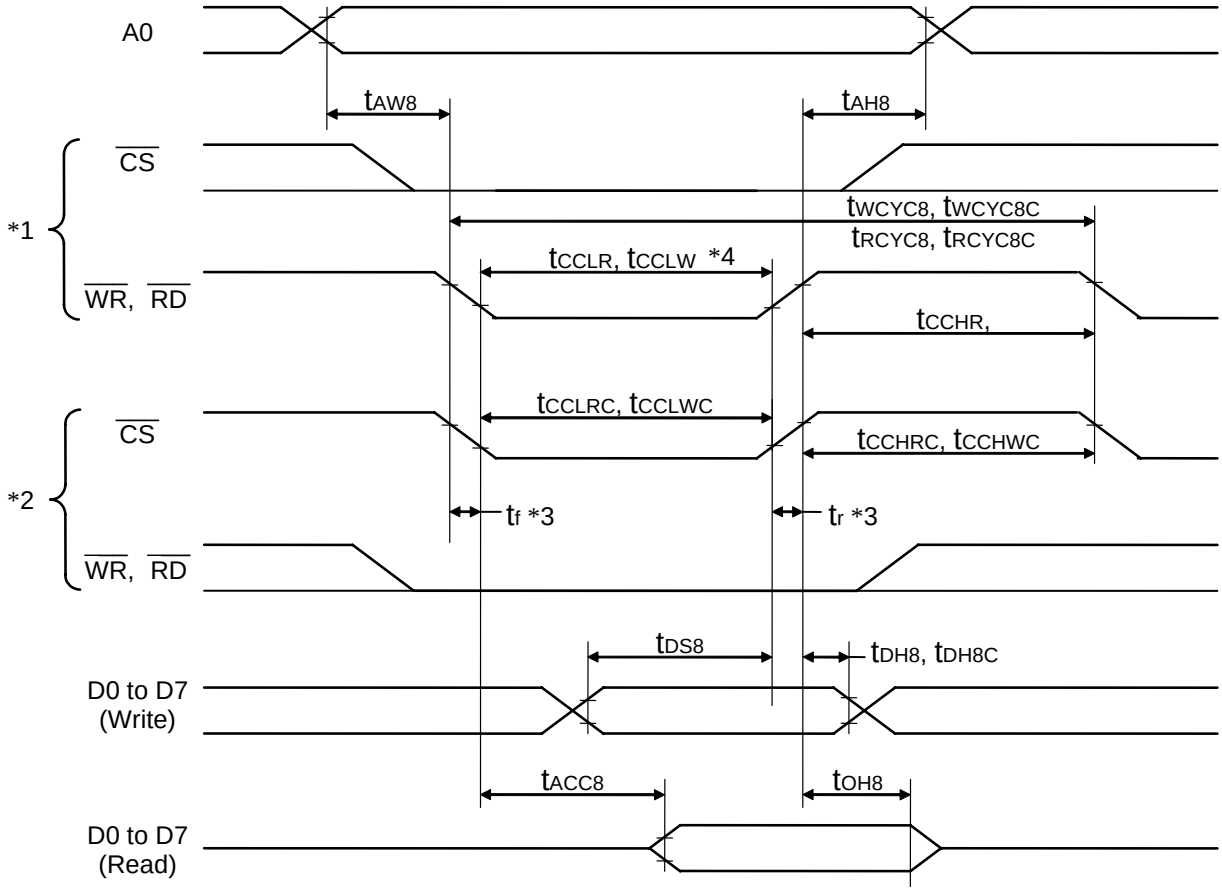


Fig.10.1

10. TIMING CHARACTERISTICS

Table 10.1

[V_{DD}=3.0V to 5.5V, T_a= -40 to +90°C]

Item	Signal	Symbol	Conditions	Standard value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		150	—	
System write cycle time	$\overline{WR}$	t_{WCYC8}		1000	—	
System write cycle time	$\overline{CS}$	t_{WCYC8C}		1600	—	
System read cycle time	$\overline{RD}$	t_{RCYC8}		1600	—	
System read cycle time	$\overline{CS}$	t_{RCYC8C}		1600	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		650	—	
Control L pulse width ($\overline{CS}$)	$\overline{CS}$	t_{CCLWC}		1000	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		1000	—	
Control L pulse width ($\overline{CS}$)	$\overline{CS}$	t_{CCLRC}		1000	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		350	—	
Control H pulse width ($\overline{CS}$)	$\overline{CS}$	t_{CCHWC}		600	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		600	—	
Control H pulse width ($\overline{CS}$)	$\overline{CS}$	t_{CCHRC}		600	—	
Data setup time	D0 to D7	t_{DS8}		600	—	
Data hold time ($\overline{WR}$)		t_{DH8}		30	—	
Data hold time ($\overline{CS}$)		t_{DH8C}		100	—	
$\overline{RD}$ access time		t_{ACC8}	Cload=100pF	—	1000	
Output disable time		t_{OH8}		50	600	

*1. Accessed by $\overline{WR}$ and $\overline{RD}$ at $\overline{CS}$ = LOW.
*2. Accessed by $\overline{CS}$ at $\overline{WR}$, $\overline{RD}$ = LOW.
*3. The rising and trailing times (t_r and t_f) of the input signal are below 15 ns. When the system cycle time is used at high speed, stipulated at $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.
*4. t_{CCLW} and t_{CCLR} are stipulated by the overlap period when $\overline{CS}$ is at LOW and $\overline{WR}$ and $\overline{RD}$ are at the LOW level.
*5. All timings are stipulated on the basis of 20% and 80% of V_{DD}.

10.2 System Bus Read/Write Characteristics 2 (68 Series MPU)

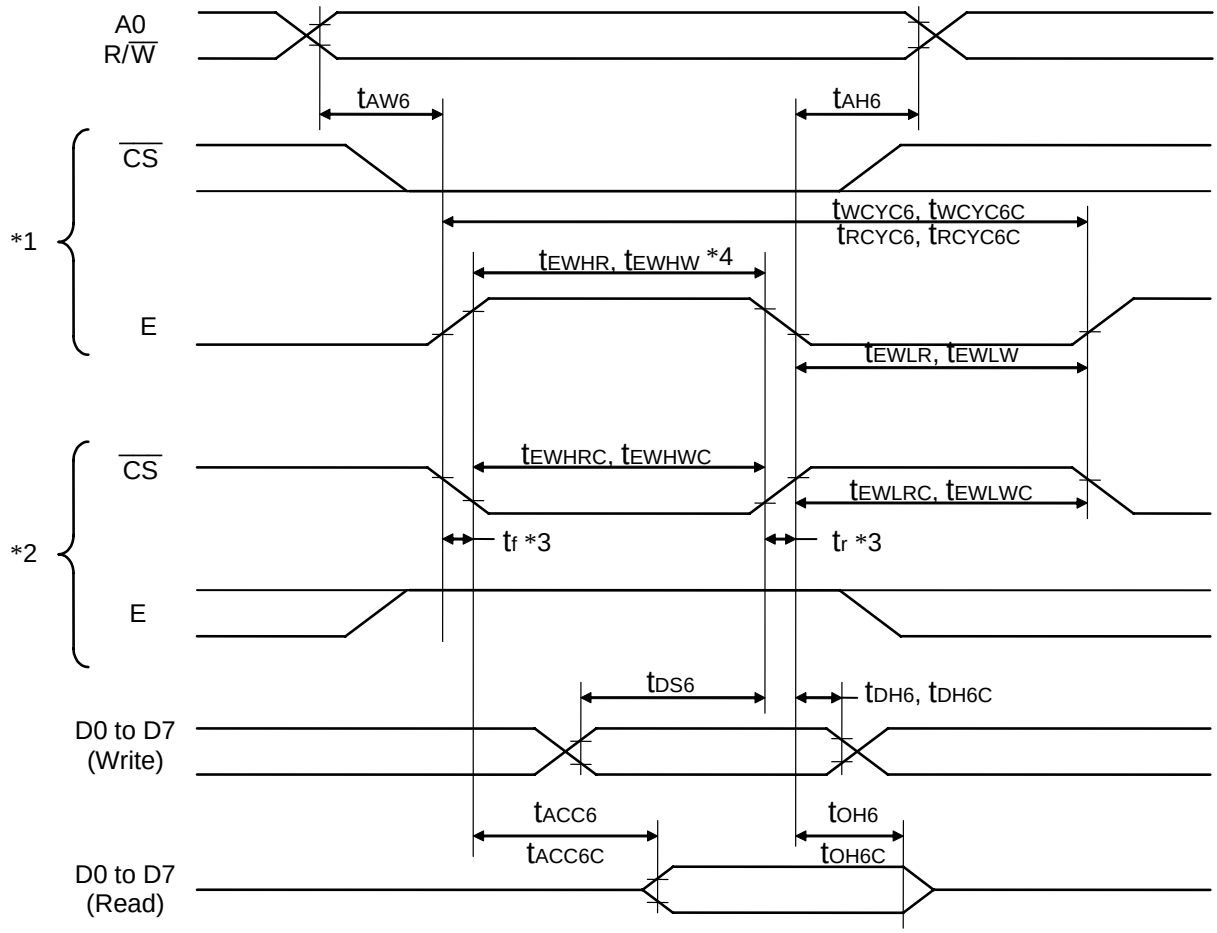


Fig.10.2

10. TIMING CHARACTERISTICS

Table 10.2

[V_{DD}=3.0V to 5.5V, T_a= -40 to +90°C]

Item		Signal	Symbol	Conditions	Standard value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0		ns
Address setup time			t_{AW6}		350		
System write cycle time		E	t_{WCYC6}		1600		
System write cycle time		$\overline{CS}$	t_{WCYC6C}		1600		
System read cycle time		E	t_{RCYC6}		1600		
System read cycle time		$\overline{CS}$	t_{RCYC6C}		1600		
Data setup time		D0 to D7	t_{DS6}		450		
Data hold time (E)			t_{DH6}		600		
Data hold time ($\overline{CS}$)			t_{DH6C}		100		
Access time			t_{ACC6}	Cload=100pF	—	600	
			t_{ACC6C}		—	1000	
Output disable time			t_{OH6}		100	1000	
			t_{OH6C}		50	600	
Enable H pulse width	Read	E	t_{EWHR}		600		
	Read	$\overline{CS}$	t_{EWHRC}		1000		
	Write	E	t_{EWHW}		600		
	Write	$\overline{CS}$	t_{EWHWC}		1000		
Enable L pulse width	Read	E	t_{EWLR}		1000		
	Read	$\overline{CS}$	t_{EWLRC}		600		
	Write	E	t_{EWLW}		1000		
	Write	$\overline{CS}$	t_{EWLWC}		600		

*1. Accessed by E at $\overline{CS}$ = LOW.
*2. Accessed by $\overline{CS}$ at E = HIGH.
*3. The rising and trailing times (t_r and t_f) of the input signal are below 15 ns. When the system cycle time is used at high speed, stipulated at $(t_r + t_f) \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $(t_r + t_f) \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.
*4. t_{EWHW} and t_{EWHR} are stipulated by the overlap period when $\overline{CS}$ is at LOW and E is at the HIGH level.
*5. All timings are stipulated on the basis of 20% and 80% of V_{DD}.

10.3 Serial Interface

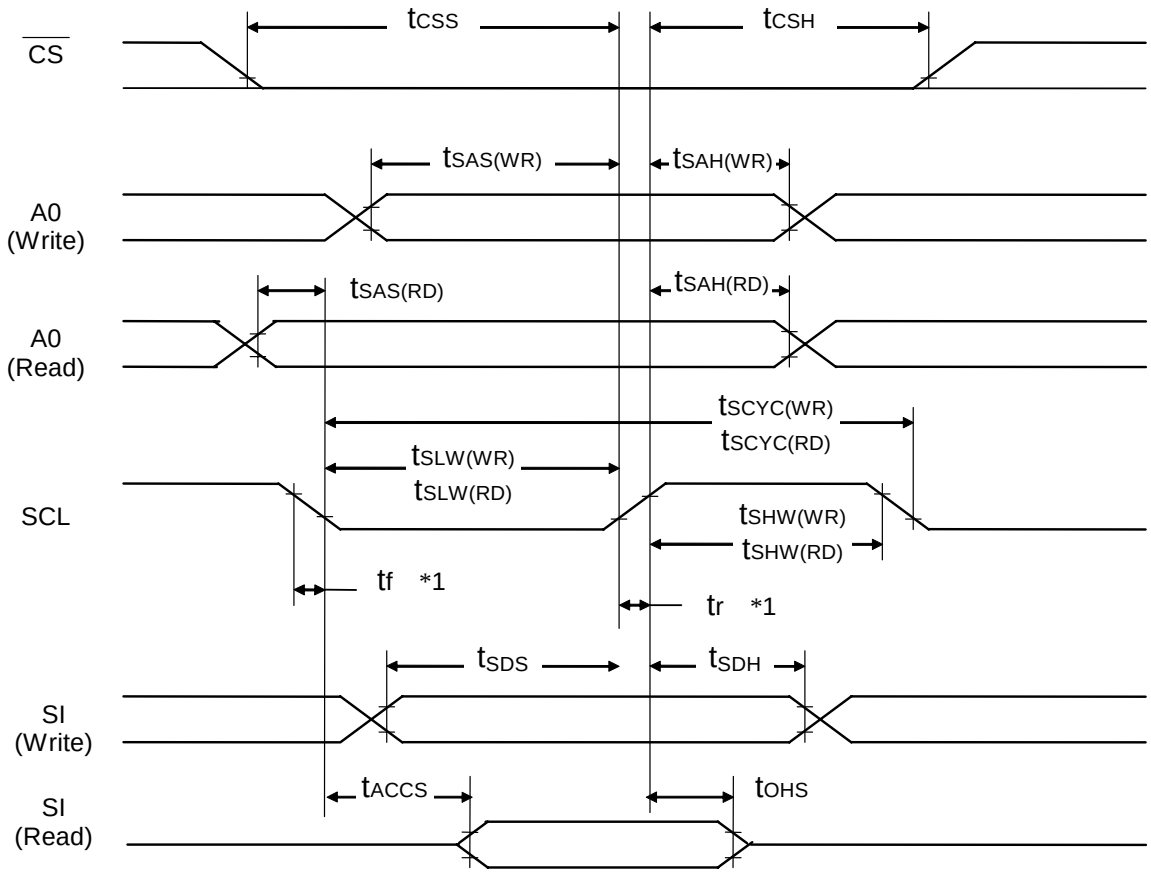


Fig.10.3

Table 10.3

[V_{DD}=3.0V to 5.5V, T_a= -40 to +90°C]

Item		Signal	Symbol	Conditions	Standard value		Unit
					Min.	Max.	
Serial clock cycle	Write	SCL	t_{SCYC}(WR)		250	—	ns
	Read		t_{SCYC}(RD)		450	—	
SCL HIGH pulse width	Write		t_{SHW}(WR)		50	—	
	Read		t_{SHW}(RD)		250	—	
SCL LOW pulse width	Write		t_{SLW}(WR)		150	—	
	Read		t_{SLW}(RD)		150	—	
Address setup time	Write	A0	t_{SAS}(WR)		50	—	
	Read		t_{SAS}(RD)		50	—	
Address hold time	Write		t_{SAH}(WR)		50	—	
	Read		t_{SAH}(RD)		50	—	
Data setup time		SI	t_{SDS}		50	—	
Data hold time		(Write)	t_{SDH}		50	—	
$\overline{CS}$-SCL time		$\overline{CS}$	t_{CSS}		50	—	
			t_{CSH}		150	—	
$\overline{RD}$ access time		SI	t_{ACCS}	Cloud = 100pF	150	—	
Output disable time		(Read)	t_{OHS}		30	250	

*1. The rising and trailing times (t_r and t_f) of the input signal are below 15 ns.
*2. All timings are stipulated on the basis of 20% and 80% of V_{DD}.

10.4 Display Control I/O Timing

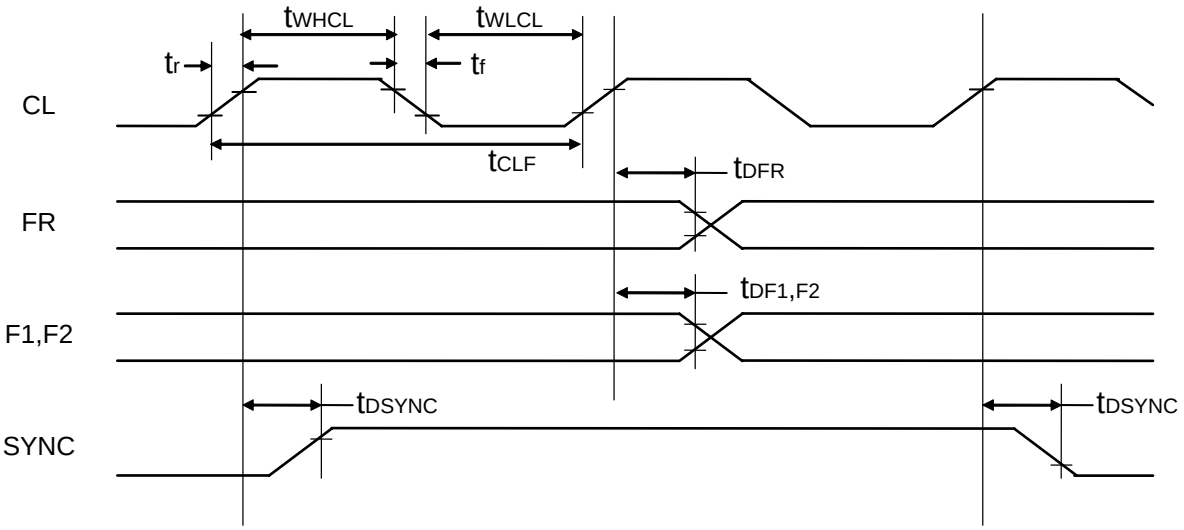


Fig.10.4

Table 10.4 Output timing

[V_{DD}=3.0V to 5.5V, T_a= -40 to +90°C]

Item		Signal	Symbol	Conditions	Standard value			Unit
					Min.	Typ.	Max.	
Use of built-in oscillation circuit (CLS = HIGH)	FR delay time	FR	t_{DFR}	CL = 50pF	-200	—	200	ns
	F1 and F2 delay time	F1,F2	$t_{DF1,F2}$		-200	—	200	
	SYNC delay time	SYNC	t_{DSYNC}		-200	—	200	
External input (CLS = LOW)	FR delay time	FR	t_{DFR}		0	—	500	
	F1 and F2 delay time	F1,F2	$t_{DF1,F2}$		0	—	500	
	SYNC delay time	SYNC	t_{DSYNC}		0	—	500	

Table 10.5 Input Timing

[V_{DD}=3.0V to 5.5V, T_a= -40 to +90°C]

Item	Signal	Symbol	Conditions	Standard value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		-1.25	—	1.25	µs
F1 and F2 delay time	F1,F2	$t_{DF1,F2}$		-1.25	—	1.25	µs
SYNC delay time	SYNC	t_{DSYNC}		-1.25	—	1.25	µs
Input clock duty ratio *2	CL	t_{CLD}		20	—	80	%
Input clock cycle		t_{CLF}		6.25	—	—	µs
Input clock rise time (20% to 80%) *3		t_r		—	—	15	ns
Input clock fall time (20% to 80%) *3		t_f		—	—	15	ns
Low level pulse width		t_{WLCL}		1.25	—	—	µs
High level pulse width		t_{WHCL}		1.25	—	—	µs

*1: All timings are stipulated on the basis of 20% and 80% of V_{DD}.

*2: The CL duty ratio is stipulated by $t_{CLD} = \frac{t_{WHCL}}{t_{CLF}} \times 100[\%]$ or $t_{CLD} = \frac{t_{WLCL}}{t_{CLF}} \times 100[\%]$.

*3 A signal beyond the specification has no problem for the functionality, but t_{CLF}, t_{WLCL} and t_{WHCL} always should be kept.

10.5 Reset Input Timing

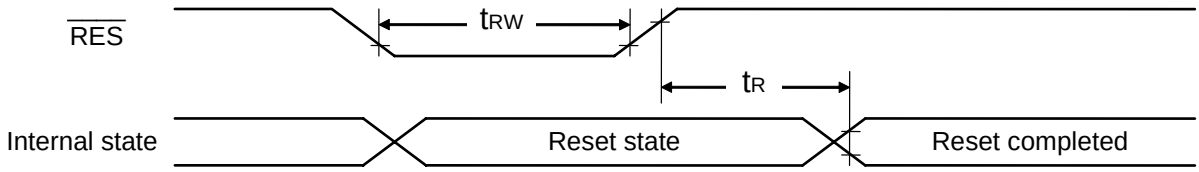


Fig.10.5

Table 10.6

[V_{DD}=3.0V to 5.5V, T_a= -40 to +90°C]

Item	Signal	Symbol	Conditions	Standard value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—			1	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		2			µs

*1: All timings are stipulated on the basis of 20% and 80% of V_{DD}.

10.6 Temperature Sensor Measuring Timing

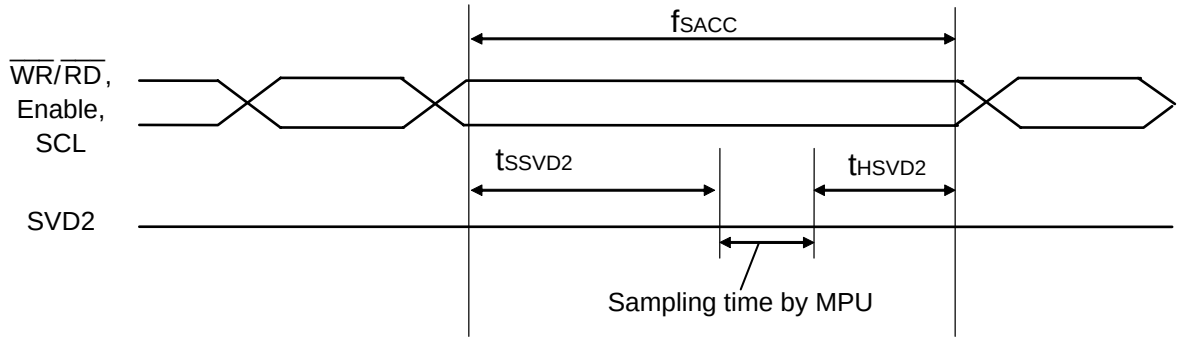


Fig.10.6

Table 10.7

[V_{DD}=3.0V to 5.5V, T_a=-40 to +90°C]

Item	Signal	Symbol	Conditions	Standard value			Unit
				Min.	Typ.	Max.	
MPU access cycle	$\overline{WR}$ or $\overline{RD}$ (80 series MPU) Enable (68 series MPU) SCL (Serial interface)	f_{SACC}	—	—	—	0	Hz
Sampling setup time	SVD2	t_{SSVD2}		100	—	—	ms
Sampling hold time	SVD2	t_{HSVD2}		0	—	—	ms

*1: Stop an access from MPU (for 80 series MPU: input from the $\overline{WR}$ or $\overline{RD}$ pin, for 68 series MPU: input from the Enable pin, and for the serial interface: input from the SCL pin) during detection of the SVD2 output.

*2: Wait time until SVD2 sampling is enabled after stopping access from MPU. Apply when the temperature sensor is set to ON beforehand. T o set the temperature sensor to ON after stopping access from MPU, provide a given output voltage setup time.

*3: Wait time until access from MPU can be started after completion of SVD2 sampling by MPU.

11. POWER CIRCUIT (REFERENCE EXAMPLE)

V_{DD} > 3.0V, VDIS=H”

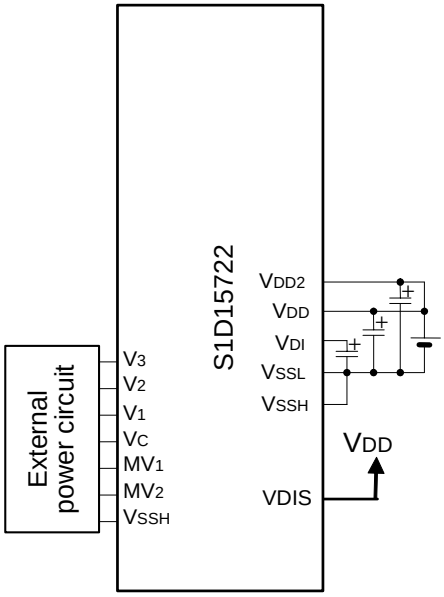


Fig.11.1

12. MPU INTERFACE (REFERENCE EXAMPLE)

This IC can be directly connected to the 80 series MPU and 68 series MPU. Using the serial interface operates with fewer signal lines.

Sharing this IC with multiple chips enlarges the display area. In such cases, the IC that makes an access individually using the chip select signal can be selected.

After being initialized by the pin, each input pin should be controlled successfully.

(1) 80 series MPU

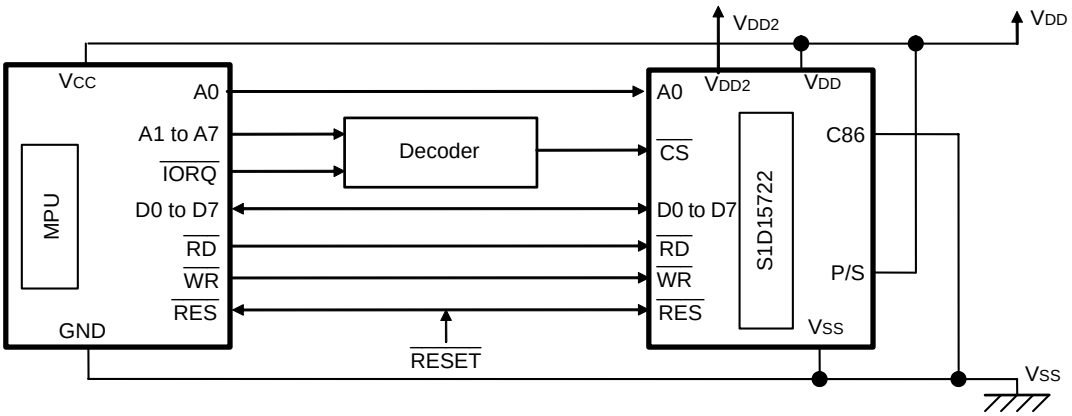


Fig.11.1 80 Series

(2) 68 series MPU

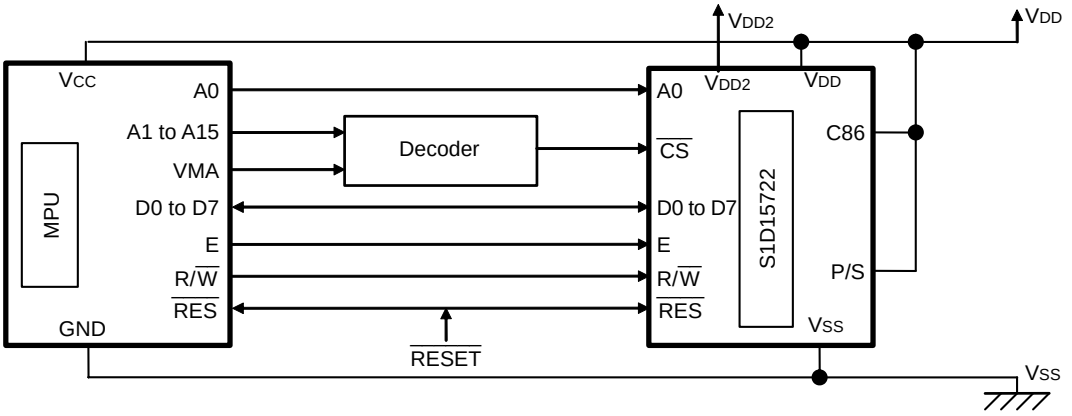


Fig.11.2 68 Series

(3) Serial Interface

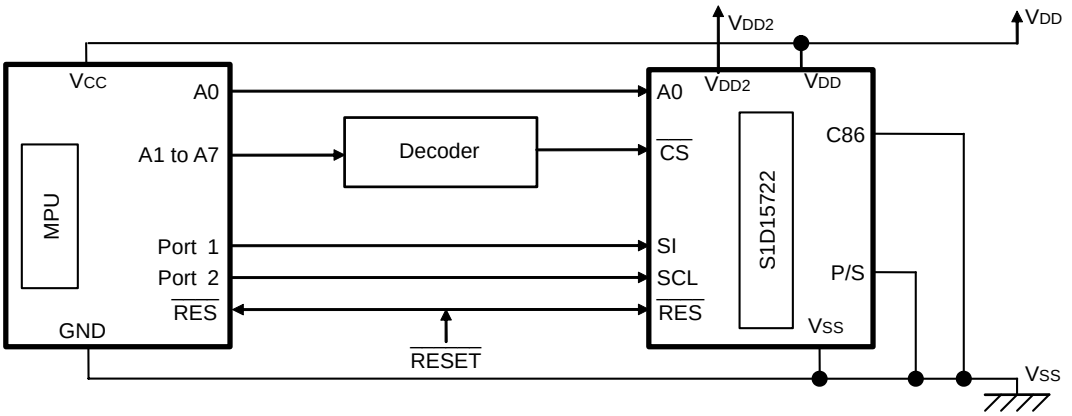


Fig.11.3 Serial Control

13. CONNECTION BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

Sharing this IC with multiple chips makes it easy to enlarge the liquid crystal display area. Set both master and slave the same number of display line using the command.

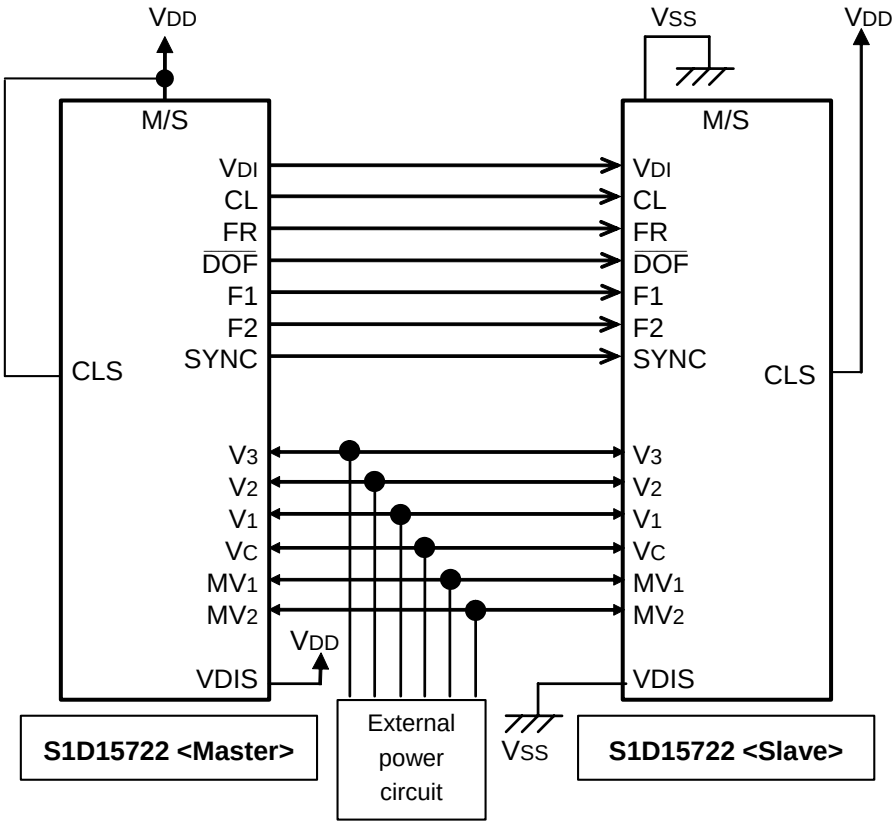


Fig 13.1 Connection between Master and Slave

Set V_{DIS} of master = HIGH, V_{DIS} of slave = Low, to supply V_{DI} generated by master to slave.

14. LCD PANEL CONNECTION (REFERENCE EXAMPLE)

Sharing this IC with multiple chips makes it easy to enlarge the liquid crystal display area.

(1) Example of 1 chip configuration

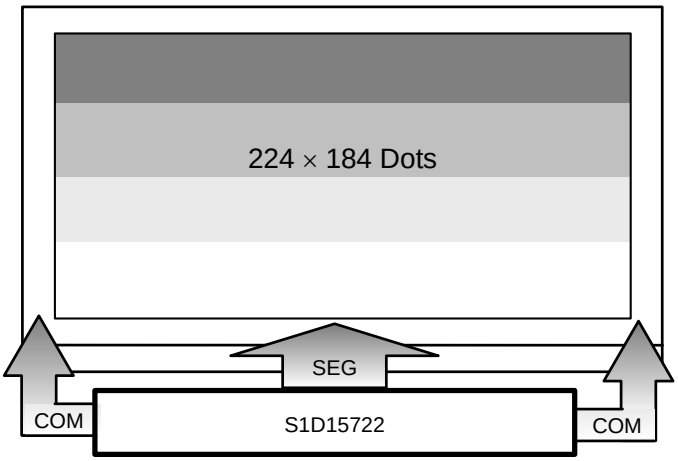


Fig.14.1 Example of 1 Chip Drive

(2) Example of 2-chip configuration

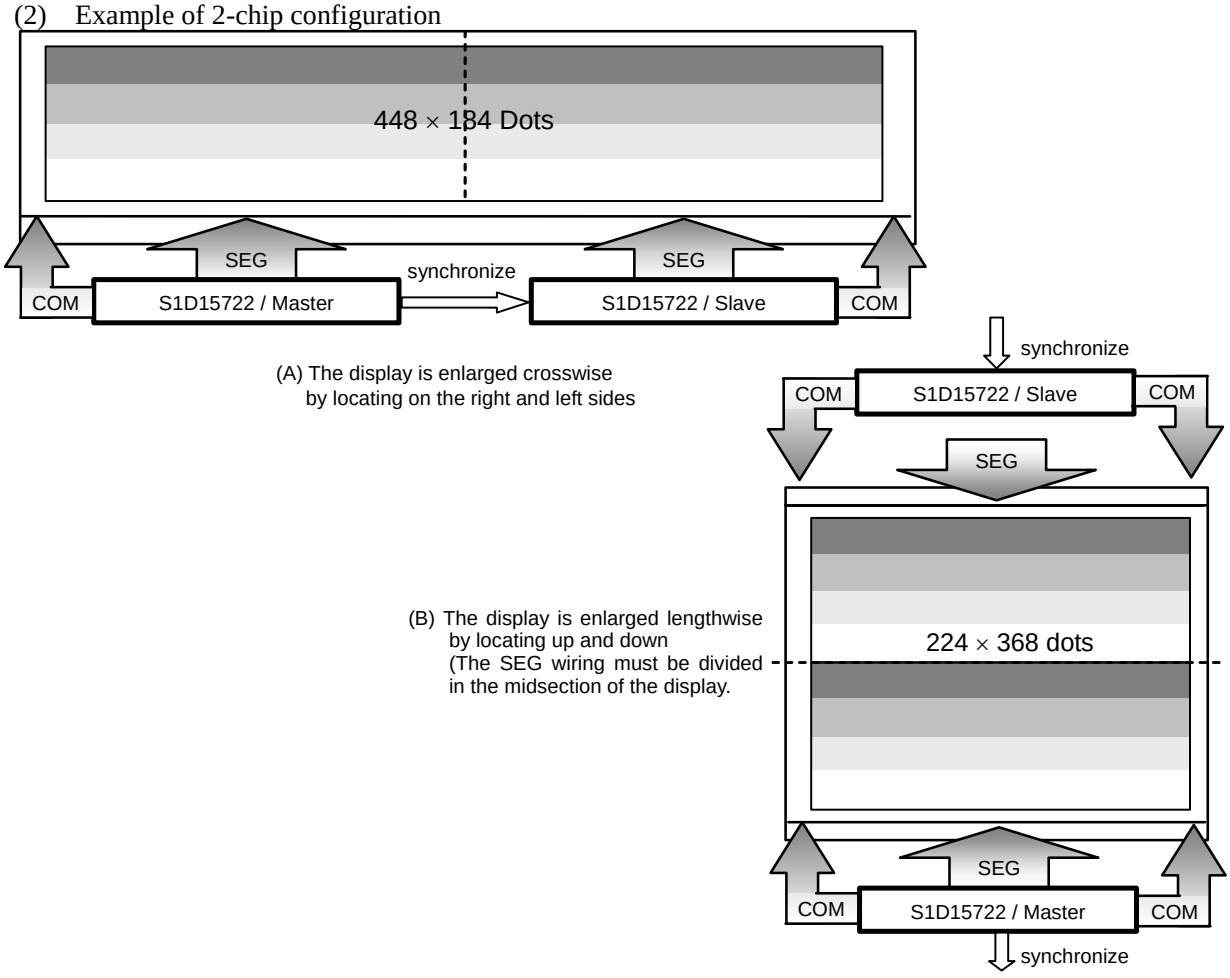


Fig.14.2 Example of 2-chip Drive

15. PRECAUTIONS

When using this development specification, the following points should be noted.

1. This development specification is subject to change without notice for improvement.
2. This development specification does not permit and guarantee the implementation and/or use of the patent properties and other intellectual property rights the third party or SEIKO EPSON owns.
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When using semiconductor chips, the following points should be noted.

[Precautions in Handling the IC against the Light]

If semiconductor chips are exposed to the strong light, their characteristics may change. Therefore, the IC may malfunction if exposed to the light. To protect the ICs, the following general requirements must be satisfied for IC mount boards and products.

(1) Do not expose the ICs to the light before they are mounted in the board design and IC mounting phases.
(2) Also, do not expose the ICs to the light in the inspection phase.
(3) Take all surfaces, top, bottom and sides, of the IC chip into consideration when blocking out light.

REVISION HISTORY

Date	Rev.	Page	Type	Description
2008/1/9	1.0	All	new	New enactment.
2008/6/11	1.1	P3	Corrected	In 3. Blockdiagram, change arrow direction at VDI pin from bi-directional to one-way.
		P27	added	In 6.8 Reset circuit, add bit “D4” at MLS driving select register.
		P42 to 43	Added	IIn 7. Command at (26) “Select MLS drive” command, add bit P4 and the description. P4=0: n-line frame inversion overlap OFF P4=1: n-line frame inversion overlap ON
		P45	Added	In 7.2 Command table, at (26) Select MLS Drive command, add a bit P4.

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