EPSON
EXCEED YOUR VISION

S1D15719 Series
Technical Manual

SEIKO EPSON CORPORATION

Rev.2.0a

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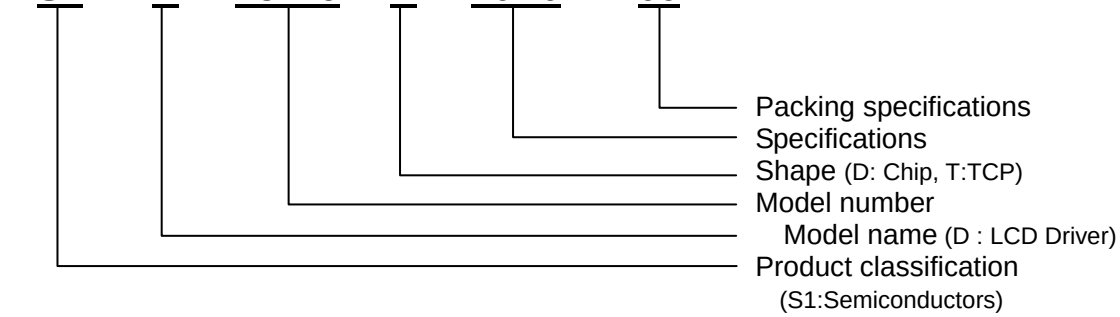
Configuration of product number

●DEVICES

S1 D 15719 D 10B0 00



CONTENTS

1. DESCRIPTION

S1D15719 Series is a single chip MLS driver for dot matrix liquid crystal displays which can be directly connected to the microcomputer bus. It accepts the 8-bit parallel or serial display data from the microcomputer to store the data in the on-chip display data RAM, and issues liquid crystal drive signals independently of the microcomputer.

The S1D15719 Series provides both 4 gray-scale display and binary display. It incorporates a display data RAM (180 × 132 × 2 bits). In the case of 4 gray-scale display, 2 bits of the on-chip RAM respond to one-dot pixels, while in the case of binary display, 1 bit of the on-chip RAM respond to one-dot pixels.

The S1D15719 Series features 132 common output circuits and 180 segment output circuits. A single chip provides a display of 11 characters by 8 lines with 180 × 132 dots (16 × 16 dots) and display of 15 characters by 11 lines by the 12 × 12 dot character font.

S1D15719 Series can be used to constitute a system to provide optimum LCD contrast throughout a wide temperature range without need for use of supplementary parts such as the thermistor, under controls of a microcomputer.

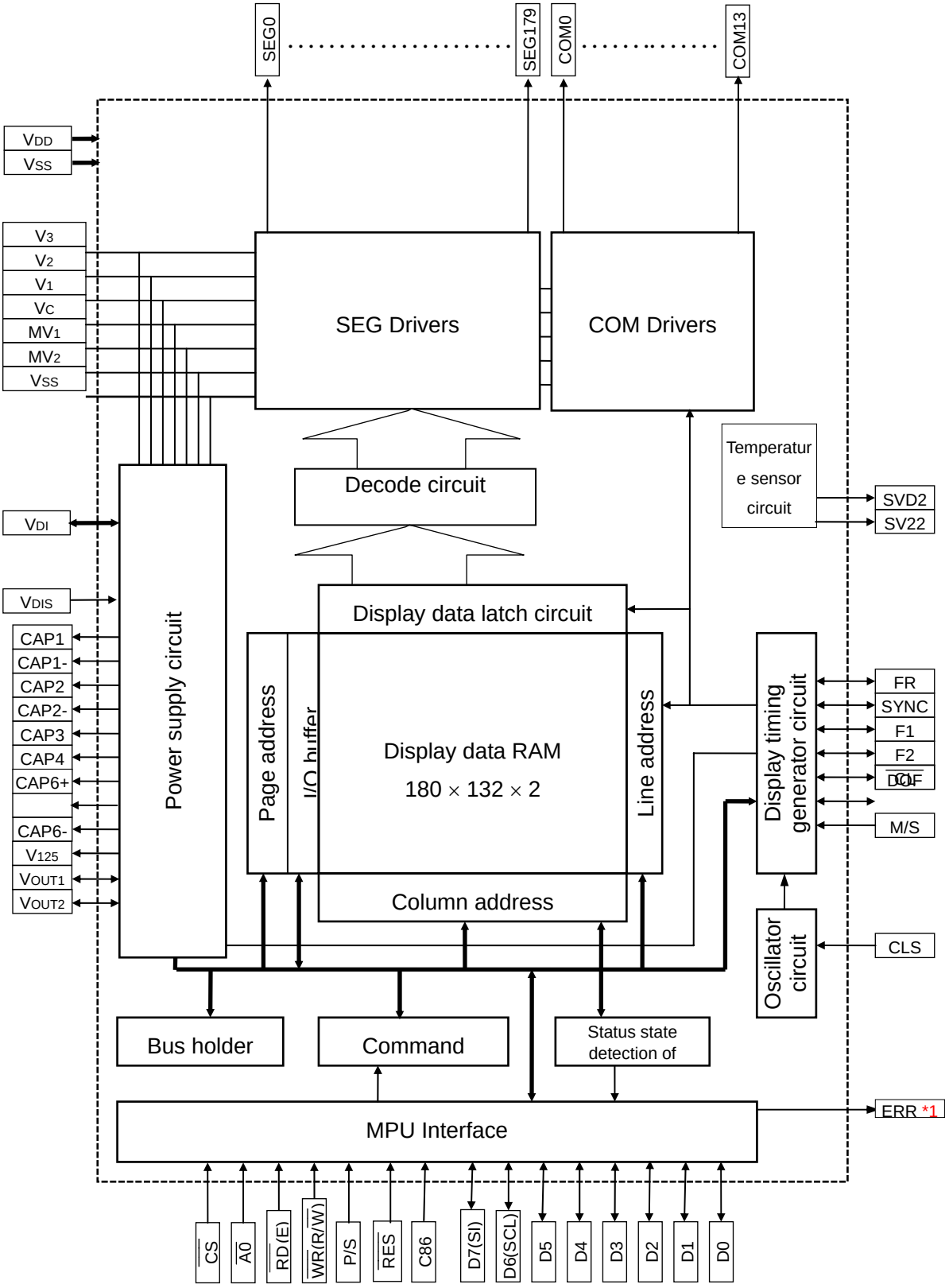
2. FEATURES

- Direct RAM data display by display data RAM
  4 gray-scale display (Normally white in normal display mode)
  RAM bit data (MSB, LSB)
    (1,1): gray-scale 3, black
    (1,0): gray-scale 2
    (0,1): gray-scale 1
    (0,0): gray-scale 0, white
- Binary display (Normally white display is in normal mode)
  RAM bit data
    "1": On and black
    "0": Off and white
- RAM capacity
  132 × 180 × 2 = 47,520 bits
- Liquid crystal drive circuit
  132 common outputs and 180 segment outputs
- High-speed 8-bit MPU interface (directly connectable to the MPUs of both 80/68 series) / serial interface possible
- A variety of command functions
  Duty set, n-line reversal, display data RAM address control, contrast control, display ON/OFF, display normal/reverse rotation, display all lighting ON/OFF, liquid crystal drive power supply circuit control, display clock built-in oscillator circuit control
- MLS drive technology
  Built-in high precision voltage regulation function
- High precision CR oscillator circuit incorporated
- Low power consumption
- Built-in temperature sensor circuit
- Power supply
  Logic power supply 1: V_{DI}-V_{SS}= 2.7V to 3.3V
  Logic power supply 2: V_{DD}-V_{SS}= 2.7V to 5.5V
  Booster power supply: V_{DD2}-V_{SS}= V_{DD} to 5.5V
  Liquid crystal drive power supply: V_3-V_{SS}= 11V to 25V
- Wide operation temperature range: -40 to +85°C (S1D15719D10B000)
  -40 to +95°C (S1D15719D11B000,S1D15719D12B000)
- CMOS process
- Shipping form: Bare chips
- Light and radiation proof measures are not taken in designing.

Series Specification

Product name	Shipping form	Die thickness	COM output	Schumidt trigger input	Noise filter input	Operating temperature
S1D15719D10B000	Bare chip	0.625mm	Interlace out	-	$\overline{RES}$	-40 to 85°C
S1D15719D11B000	Bare chip	0.625mm	Interlace out	*1	$\overline{RES}$	-40 to 95°C
S1D15719D12B000	Bare chip	0.625mm	Interlace out	*1	*1	-40 to 95°C

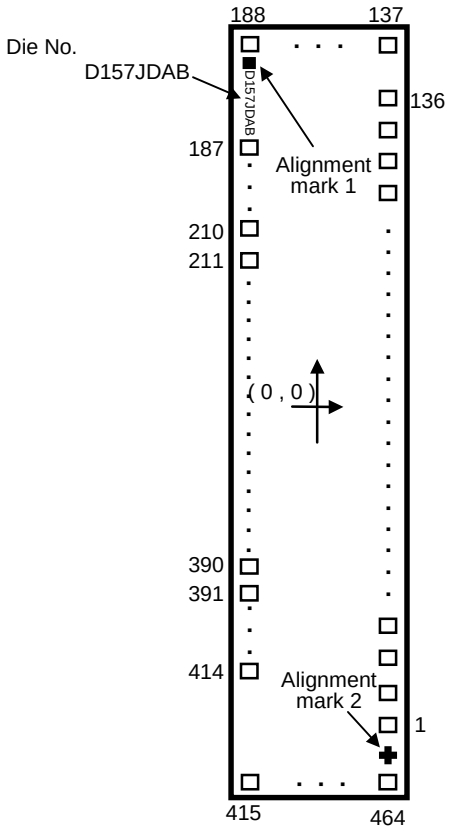
3. BLOCK DIAGRAM



*1: ERR pin is NC pin in case of S1D15719D11B000/1D15719D12B000.

4. PIN ASSIGNMENT

4.1 Chip Assignment



Top View (from bump side)

Item		Size X		Size Y	Unit
Chip size		3.03	×	17.27	mm
Chip thickness		0.625			mm
Bump pitch		Min.50			µm
Bump size					
PAD No.	1 to 136	85	×	85	µm
	137 to 186	33	×	106	µm
	187 to 210	106	×	33	µm
	211 to 390	106	×	52	µm
	391 to 414	106	×	33	µm
	415 to 464	33	×	106	µm
Bump height		Typ.17			µm

Die number	Parts number
D157JDAB	S1D15719D10B000
D157JDBB	S1D15719D11B000
D157JDCB	S1D15719D12B000

4.2 Alignment mark

Alignment coordinate

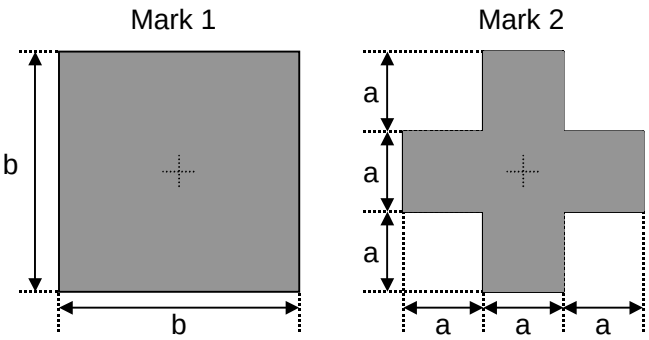
1 (-1365, 8055) µm

2 (1365, -8252) µm

Mark size

a = 15 µm

b = 45 µm



4.3 Pad Center Coordinates (COM interlace output type)

Unit: μm

PAD No.	Pin Name	X	Y
1	NC	1361	-8100
2	NC		-7980
3	V_{DD}		-7860
4	V_{DIS}		-7740
5	V_{SS}		-7620
6	SYNC		-7500
7	FR		-7380
8	CL		-7260
9	$\overline{DOF}$		-7140
10	F1		-7020
11	F2		-6900
12	V_{SS}		-6780
13	ERR*1		-6660
14	NC		-6540
15	$\overline{CS}$		-6420
16	$\overline{RES}$		-6300
17	A0		-6180
18	V_{SS}		-6060
19	$\overline{WR}$, R/$\overline{W}$		-5940
20	$\overline{RD}$, E		-5820
21	V_{DD}		-5700
22	D7, SI		-5580
23	D6, SCL		-5460
24	D0		-5340
25	D1		-5220
26	D2		-5100
27	D3		-4980
28	D4		-4860
29	D5		-4740
30	D6, SCL		-4620
31	D7, SI		-4500
32	V_{DD}		-4380
33	M/S		-4260
34	CLS		-4140
35	V_{SS}		-4020
36	TEST1		-3900
37	C86		-3780
38	P/S		-3660
39	V_{DD}		-3540
40	V_{SS}		-3420
41	V_{SS}		-3300
42	V_{SS}		-3180
43	V_{SS}		-3060
44	V_{SS}		-2940
45	V_{SS}		-2820
46	TEST2		-2700
47	V_{DI}		-2580
48	V_{DI}		-2460
49	V_{DI}		-2340
50	V_{DD}		-2220
51	V_{DD}	1361	-2100
52	V_{DD}		-1980
53	V_{DD}		-1860
54	V_{DD2}		-1740
55	V_{DD2}		-1620
56	V_{DD2}		-1500
57	V_{DD2}		-1380
58	V_{OUT1}		-1260
59	V_{OUT1}		-1140
60	V_{OUT1}		-1020
61	V_{OUT1}		-900
62	CAP1+		-780
63	CAP1+		-660
64	CAP1+		-540
65	CAP1+		-420
66	CAP1-		-300
67	CAP1-		-180
68	CAP1-		-60
69	CAP1-		60
70	CAP3+		180
71	CAP3+		300
72	CAP3+		420
73	CAP3+		540
74	CAP5+		660
75	CAP5+		780
76	CAP5+		900
77	CAP5+		1020
78	V_{OUT1}		1140
79	CAP4+		1260
80	CAP4+		1380
81	CAP4+		1500
82	CAP4+		1620
83	CAP2-		1740
84	CAP2-		1860
85	CAP2-		1980
86	CAP2-		2100
87	CAP2+		2220
88	CAP2+		2340
89	CAP2+		2460
90	CAP2+		2580
91	V_{OUT1}		2700
92	V_{OUT2}		2820
93	V_{OUT2}		2940
94	V_{OUT2}		3060
95	V_{OUT2}		3180
96	V_{125}		3300
97	V_{125}		3420
98	CAP6+		3540
99	CAP6+		3660
100	CAP6+		3780
101	CAP6+	1361	3900
102	CAP6-		4020
103	CAP6-		4140
104	CAP6-		4260
105	CAP6-		4380
106	V_3		4500
107	V_3		4620
108	V_3		4740
109	V_2		4860
110	V_2		4980
111	V_2		5100
112	V_1		5220
113	V_1		5340
114	V_1		5460
115	V_C		5580
116	V_C		5700
117	V_C		5820
118	MV_1		5940
119	MV_1		6060
120	MV_1		6180
121	MV_2		6300
122	MV_2		6420
123	MV_2		6540
124	V_{SS}		6660
125	V_{SS}		6780
126	TESTA		6900
127	TESTB		7020
128	TESTB		7140
129	TEST3		7260
130	TEST4		7380
131	V_{DI}		7500
132	SVD2		7620
133	SV22		7740
134	TEST5		7860
135	NC		7980
136	NC		8100
137	NC	1224	8469
138	COM129	1174	
139	COM128	1124	
140	COM123	1074	
141	COM122	1024	
142	COM121	974	
143	COM120	924	
144	COM115	874	
145	COM114	824	
146	COM113	774	
147	COM112	724	
148	COM107	674	
149	COM106	624	
150	COM105	574	

*1: ERR pin is NC pin in case of S1D15719D11B000/1D15719D12B000

Unit: μm

PAD No.	Pin Name	X	Y
151	COM104	524	8469
152	COM99	475	
153	COM98	425	
154	COM97	375	
155	COM96	325	
156	COM91	275	
157	COM90	225	
158	COM89	175	
159	COM88	125	
160	COM83	75	
161	COM82	25	
162	COM81	-25	
163	COM80	-75	
164	COM75	-125	
165	COM74	-175	
166	COM73	-225	
167	COM72	-275	
168	COM67	-325	
169	COM66	-375	
170	COM65	-425	
171	COM64	-475	
172	COM59	-524	
173	COM58	-574	
174	COM57	-624	
175	COM56	-674	
176	COM51	-724	
177	COM50	-774	
178	COM49	-824	
179	COM48	-874	
180	COM43	-924	
181	COM42	-974	
182	COM41	-1024	
183	COM40	-1074	
184	COM35	-1124	
185	COM34	-1174	
186	NC	-1224	
187	NC	-1350	7956
188	NC		7906
189	COM33		7856
190	COM32		7806
191	COM27		7756
192	COM26		7706
193	COM25		7656
194	COM24		7606
195	COM19		7556
196	COM18		7506
197	COM17		7457
198	COM16		7407
199	COM11		7357
200	COM10		7307

PAD No.	Pin Name	X	Y
201	COM9	-1350	7257
202	COM8		7207
203	COM3		7157
204	COM2		7107
205	COM1		7057
206	COM0		7007
207	NC		6957
208	NC		6907
209	NC		6857
210	NC		6807
211	SEG0		6713
212	SEG1		6638
213	SEG2		6563
214	SEG3		6488
215	SEG4		6413
216	SEG5		6338
217	SEG6		6263
218	SEG7		6188
219	SEG8		6113
220	SEG9		6038
221	SEG10		5963
222	SEG11		5888
223	SEG12		5813
224	SEG13		5738
225	SEG14		5663
226	SEG15		5588
227	SEG16		5513
228	SEG17		5438
229	SEG18		5363
230	SEG19		5288
231	SEG20		5213
232	SEG21		5138
233	SEG22		5063
234	SEG23		4988
235	SEG24		4913
236	SEG25		4838
237	SEG26		4763
238	SEG27		4688
239	SEG28		4613
240	SEG29		4538
241	SEG30		4463
242	SEG31		4388
243	SEG32		4313
244	SEG33		4238
245	SEG34		4163
246	SEG35		4088
247	SEG36		4013
248	SEG37		3938
249	SEG38		3863
250	SEG39		3788

PAD No.	Pin Name	X	Y
251	SEG40	-1350	3713
252	SEG41		3638
253	SEG42		3563
254	SEG43		3488
255	SEG44		3413
256	SEG45		3338
257	SEG46		3263
258	SEG47		3188
259	SEG48		3113
260	SEG49		3038
261	SEG50		2963
262	SEG51		2888
263	SEG52		2813
264	SEG53		2738
265	SEG54		2663
266	SEG55		2588
267	SEG56		2513
268	SEG57		2438
269	SEG58		2363
270	SEG59		2288
271	SEG60		2213
272	SEG61		2138
273	SEG62		2063
274	SEG63		1988
275	SEG64		1913
276	SEG65		1838
277	SEG66		1763
278	SEG67		1688
279	SEG68		1613
280	SEG69		1538
281	SEG70		1463
282	SEG71		1388
283	SEG72		1313
284	SEG73		1238
285	SEG74		1163
286	SEG75		1088
287	SEG76		1013
288	SEG77		938
289	SEG78		863
290	SEG79		788
291	SEG80		713
292	SEG81		638
293	SEG82		563
294	SEG83		488
295	SEG84		413
296	SEG85		338
297	SEG86		263
298	SEG87		188
299	SEG88		113
300	SEG89		38

Unit: μm

PAD No.	Pin Name	X	Y
301	SEG90	-1350	-38
302	SEG91		-113
303	SEG92		-188
304	SEG93		-263
305	SEG94		-338
306	SEG95		-413
307	SEG96		-488
308	SEG97		-563
309	SEG98		-638
310	SEG99		-713
311	SEG100		-788
312	SEG101		-863
313	SEG102		-938
314	SEG103		-1013
315	SEG104		-1088
316	SEG105		-1163
317	SEG106		-1238
318	SEG107		-1313
319	SEG108		-1388
320	SEG109		-1463
321	SEG110		-1538
322	SEG111		-1613
323	SEG112		-1688
324	SEG113		-1763
325	SEG114		-1838
326	SEG115		-1913
327	SEG116		-1988
328	SEG117		-2063
329	SEG118		-2138
330	SEG119		-2213
331	SEG120		-2288
332	SEG121		-2363
333	SEG122		-2438
334	SEG123		-2513
335	SEG124		-2588
336	SEG125		-2663
337	SEG126		-2738
338	SEG127		-2813
339	SEG128		-2888
340	SEG129		-2963
341	SEG130		-3038
342	SEG131		-3113
343	SEG132		-3188
344	SEG133		-3263
345	SEG134		-3338
346	SEG135		-3413
347	SEG136		-3488
348	SEG137		-3563
349	SEG138		-3638
350	SEG139	↓	-3713

PAD No.	Pin Name	X	Y
351	SEG140	-1350	-3788
352	SEG141		-3863
353	SEG142		-3938
354	SEG143		-4013
355	SEG144		-4088
356	SEG145		-4163
357	SEG146		-4238
358	SEG147		-4313
359	SEG148		-4388
360	SEG149		-4463
361	SEG150		-4538
362	SEG151		-4613
363	SEG152		-4688
364	SEG153		-4763
365	SEG154		-4838
366	SEG155		-4913
367	SEG156		-4988
368	SEG157		-5063
369	SEG158		-5138
370	SEG159		-5213
371	SEG160		-5288
372	SEG161		-5363
373	SEG162		-5438
374	SEG163		-5513
375	SEG164		-5588
376	SEG165		-5663
377	SEG166		-5738
378	SEG167		-5813
379	SEG168		-5888
380	SEG169		-5963
381	SEG170		-6038
382	SEG171		-6113
383	SEG172		-6188
384	SEG173		-6263
385	SEG174		-6338
386	SEG175		-6413
387	SEG176		-6488
388	SEG177		-6563
389	SEG178		-6638
390	SEG179		-6713
391	NC		-6807
392	NC		-6857
393	NC		-6907
394	NC		-6957
395	COM4		-7007
396	COM5		-7057
397	COM6		-7107
398	COM7		-7157
399	COM12		-7207
400	COM13	↓	-7257

PAD No.	Pin Name	X	Y
401	COM14	-1350	-7307
402	COM15		-7357
403	COM20		-7407
404	COM21		-7457
405	COM22		-7506
406	COM23		-7556
407	COM28		-7606
408	COM29		-7656
409	COM30		-7706
410	COM31		-7756
411	COM36		-7806
412	COM37		-7856
413	NC		-7906
414	NC	↓	-7956
415	NC	-1224	-8469
416	COM38	-1174	
417	COM39	-1124	
418	COM44	-1074	
419	COM45	-1024	
420	COM46	-974	
421	COM47	-924	
422	COM52	-874	
423	COM53	-824	
424	COM54	-774	
425	COM55	-724	
426	COM60	-674	
427	COM61	-624	
428	COM62	-574	
429	COM63	-524	
430	COM68	-475	
431	COM69	-425	
432	COM70	-375	
433	COM71	-325	
434	COM76	-275	
435	COM77	-225	
436	COM78	-175	
437	COM79	-125	
438	COM84	-75	
439	COM85	-25	
440	COM86	25	
441	COM87	75	
442	COM92	125	
443	COM93	175	
444	COM94	225	
445	COM95	275	
446	COM100	325	
447	COM101	375	
448	COM102	425	
449	COM103	475	
450	COM108	524	↓

Unit: μm

PAD No.	Pin Name	X	Y
451	COM109	574	-8469
452	COM110	624	
453	COM111	674	
454	COM116	724	
455	COM117	774	
456	COM118	824	
457	COM119	874	
458	COM124	924	
459	COM125	974	
460	COM126	1024	
461	COM127	1074	
462	COM130	1124	
463	COM131	1174	
464	NC	1224	

5. PIN DESCRIPTION

5.1 Power Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Power supply</td><td>System power supply for IC.
Connect to system MPU power supply pin V_{CC}</td><td>8</td></tr>
<tr><td>V_{SS}</td><td>Power supply</td><td>0V pin connected to the system ground.</td><td>12</td></tr>
<tr><td>V_{DD2}</td><td>Power supply</td><td>Boosting power supply pin. Short-circuit it to the V_{DD} if the built-in booster circuit is not used.</td><td>4</td></tr>
<tr><td>V_{DI}</td><td>Power supply</td><td>Power pin for internal logic. $V_{DD} \geq V_{DI}$ as well as $3.3V \geq V_{DI} \geq 2.7V$ must be maintained.
This IC contains the circuit for generating V_{DI} power. In accordance with the voltage relations between the maximum voltage of V_{DD} and V_{DI}, make them valid or invalid with the V_{DIS} pin.
1. When selecting V_{DD}Max.>3.3V and V_{DI} generation circuit enable (V_{DIS}=HIGH):
Supply the power for the internal logic circuit from the built-in V_{DI} generation circuit. Connect the capacitor across V_{DI} pin and V_{SS} pin.
2. When selecting V_{DD}Max.>3.3V and V_{DI} generation circuit disable (V_{DIS}=LOW):
Input the power for the internal logic circuit externally via V_{DI} pin.
The power for the logic circuit is externally entered in the range of $V_{DD} \geq V_{DI}$ and $3.3V \geq V_{DI} \geq 2.7V$.
3. When selecting V_{DD}Max. $\leq$ 3.3V:
Select V_{DI} generation circuit disable (V_{DIS}=LOW) and then short-circuit V_{DI} pin and V_{DD} pin ($V_{DI}=V_{DD}$).
When using this IC in multi-chip (master and slave) configuration, keep the same V_{DI} voltage on each chip. When using the built-in V_{DI} generating circuit, set V_{DIS}=HIGH for the master chip only. Set V_{DIS}=LOW for the slave chip and supply the V_{DI} voltage from the master chip.</td><td>4</td></tr>
<tr><td>V_{DIS}</td><td>I</td><td>It is used to enable or disable V_{DI} generation circuit.
V_{DIS} = HIGH:V_{DI} generation circuit is enabled
V_{DIS} = LOW:V_{DI} generation circuit is disabled
Whenever switching V_{DIS} pin from LOW to HIGH, it must be once initialized with $\overline{RES}$ pin after the switching.
Operation of V_{DI} generation circuit is controlled by V_{DIS} pin alone. Namely its operation is independent of the power save command. When you want to reduce current consumption during the power save mode, turn on the control by V_{DIS} pin externally.</td><td>1</td></tr>
<tr><td>V_3, V_2, V_1, V_C, MV_1, MV_2</td><td>Power supply</td><td>A liquid crystal drive multi-level power supply. The voltages determined by the liquid crystal cell are impedance-converted by resistive divider and operational amplifier for application.
The following order must be maintained:
$V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq V_{SS}$
Master operation: When power supply is turned on, the following voltage is applied to each pin by the built-in power supply circuit.
Selection of voltage is done with the bias set command.
<table>
<tr><td>V_2</td><td>7.5/11・V_3</td><td>7/10・V_3</td><td>6.5/9・V_3</td><td>6/8・V_3</td></tr>
<tr><td>V_1</td><td>6.5/11・V_3</td><td>6/10・V_3</td><td>5.5/9・V_3</td><td>5/8・V_3</td></tr>
<tr><td>V_C</td><td>5.5/11・V_3</td><td>5/10・V_3</td><td>4.5/9・V_3</td><td>4/8・V_3</td></tr>
<tr><td>MV_1</td><td>4.5/11・V_3</td><td>4/10・V_3</td><td>3.5/9・V_3</td><td>3/8・V_3</td></tr>
<tr><td>MV_2</td><td>3.5/11・V_3</td><td>3/10・V_3</td><td>2.5/9・V_3</td><td>2/8・V_3</td></tr>
</table></td><td>3 each</td></tr>
</table>

5.2 LCD Power Supply Current Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	This pin connects the positive side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP1- pin.	4
CAP1-	O	This pin connects the negative side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP1+ pin.	4
CAP2+	O	This pin connects the positive side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP2- pin.	4
CAP2-	O	This pin connects the negative side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP2+ pin.	4
CAP3+	O	This pin connects the positive side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP1- pin.	4
CAP4+	O	This pin connects the positive side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP2- pin.	4
CAP5+	O	This pin connects the positive side of the booster capacitor for the 1st booster circuit. It connects the capacitor across CAP1- pin.	4
CAP6+	O	This pin connects the positive side of the booster capacitor for the 2nd booster circuit. It connects the capacitor across CAP6- pin.	4
CAP6-	O	This pin connects the negative side of the booster capacitor for the 2nd booster circuit. It connects the capacitor across CAP6+ pin.	4
V_{OUT1}	I/O	This pin is used to output the voltage after being boosted on the 1st booster circuit. The capacitor is connected across V_{DD2}. When both the 1st and 2nd booster circuits are not used, select $V_{OUT1}=V_{125}=V_{OUT2}$ or OPEN.	6
V_{125}	I/O	It is the power supply pin on the 2nd booster circuit. Set it to OPEN or connect the capacitor across V_{DD2} or V_{SS}. When the 1st booster circuit is used but the 2nd booster circuit is not used: Select $V_{125}=V_{OUT1}=V_{OUT2}$. When both the 1st and 2nd booster circuits are not used: Select $V_{125}=V_{OUT1}=V_{OUT2}$ or OPEN.	2
V_{OUT2}	I/O	This pin is used to output the voltage after boosted on the 2nd booster circuit. It connects the capacitor across V_{DD2} or V_{SS}. When the 1st booster circuit is used but the 2nd booster circuit is not used: Select $V_{125}=V_{OUT1}=V_{OUT2}$. When both the 1st and 2nd booster circuits are not used: Supply the voltage externally if V_3 voltage adjusting circuit is used. When V_3 voltage adjusting circuit is not used, select $V_{OUT2}=V_3$ or OPEN.	4

5.3 System Bus Connection Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0

(SI)
(SCL)</td><td>I/O</td><td>Connects to the 8-bit or 16-bit MPU data bus via the 8-bit bi-directional data bus. When the serial interface is selected (P/S = LOW), D7 serves as the serial data input (SI) and D6 serves as the serial clock input (SCL), In this case, D0 through D5 go to a high impedance state. When the Chip select is inactive, D0 through D7 go to a high impedance state.</td><td>total 10</td></tr>
<tr><td>A0</td><td>I</td><td>Normally, the least significant bit MPU address bus is connected to distinguish between data and command.
A0 = HIGH : indicates that D0 to D7 are display data or command parameters.
A0 = LOW : indicates that D0 to D7 are control commands.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When the $\overline{RES}$ is LOW, in initialization is achieved.
Resetting operation is done on the level of the $\overline{RES}$ signal.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>A chip select signal. When $\overline{CS}$ = LOW, signals are active, and data/command input/output are enabled.
When $\overline{CS}$ = High, the data bus is caused to high impedance.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected. (active LOW)
A pin for connection of the $\overline{RD}$ signal of the 80 series MPU.
When this signal is LOW, the data bus of the S1D15719 Series is in the output state.
• When the 68 series MPU is connected. (active HIGH)
Serves as a 68 series MPU enable clock input pin.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected. (active LOW)
A pin for connection of the $\overline{WR}$ signal of the 80 series MPU.
Signals on the data bus are latched at the leading edge of the $\overline{WR}$ signal.
• Serves as a read/write control signal input pin when the 68 series MPU is connected. (active HIGH)
R/$\overline{W}$ = HIGH : Read
R/$\overline{W}$ = LOW : Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>A MPU interface switching pin.
C86 = HIGH : 68 series MPU interface
C86 = LOW : 80 series MPU interface
LOW is selected when the serial interface is selected.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel data input/serial data input select pin
P/S = HIGH : Parallel data input
P/S = LOW : Serial data input
The following Table shows the summary:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write status read</td><td>SCL (D6)</td></tr>
</table>
When P/S = LOW, D0 to D5 high impedance.
D0 to D5 can be HIGH, LOW or open.
$\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) are fixed to HIGH or LOW.
When serial data is input, read status and read temperature sensor output are enabled, but read display data RAM is not enabled.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>A pin used to select Enable/Disable state of the built-in oscillator circuit for display clock.
CLS = HIGH : Built-in oscillator circuit Enabled
CLS = LOW : Built-in oscillator circuit Disabled (External input)
When CLS is LOW, display clock is input from the CL pin. When the S1D15719 Series is used in the master/slave mode, each CLS pins must be set to the same level.
<table><tr><th>Display clock</th><th>Master</th><th>Slave</th></tr><tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr><tr><td>External input</td><td>LOW</td><td>LOW</td></tr></table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>A pin used to select the master/slave operation for S1D15719 Series.
Liquid crystal display system is synchronized when the master operation outputs the timing signal required for liquid crystal display, while the slave operation inputs the timing signal required for liquid crystal display.
M/S = HIGH : Master operation
M/S = LOW : Slave operation
The following Table shows the relation in conformance to the M/S and CLS :
<table><tr><th>M/S</th><th>CLS</th><th>Oscillation circuit</th><th>Power circuit</th><th>CL</th><th>FR, DOF, F1, F2, SYNC</th></tr><tr><td>HIGH</td><td>HIGH
LOW</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td></tr><tr><td>LOW</td><td>HIGH
LOW</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td></tr></table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
The following Table shows the relation in conformance to the M/S and CLS state:
<table><tr><th>M/S</th><th>CLS</th><th>CL</th></tr><tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Input</td></tr><tr><td>LOW</td><td>HIGH
LOW</td><td>Input
Input</td></tr></table>When you want to use the S1D15719 Series in the master/slave mode, connect each CL pin.</td><td>1</td></tr>
<tr><td>ERR</td><td>O</td><td>This pin is used to monitor operating mode of IC.
ERR = LOW:Normal operating mode
ERR = HIGH:IC is in the initial state or an error is detected in its operation
When ERR=HIGH, bits are potentially garbled on the display data RAM and some registers of the internal logic due to, for instance, excessive incoming noises. In this case, you must reset the command and send the data to the display data RAM again. In the initial state after the reset, ERR=HIGH will be indicated.
*:ERR pin is NC pin in case of S1D15719D11B000/D15719D12B000</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>A liquid crystal alternating current input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15719 Series in the master/slave mode, connect each FR pin.</td><td>1</td></tr>
</table>

Pin name	I/O	Description	Number of pins
F1, F2, SYNC	I/O	A liquid crystal sync signal input/output pin. M/S = HIGH : Output M/S = LOW : Input When you want to use the S1D15719 Series in the master/slave mode, connect each F1, F2 and SYNC pins.	1 each
$\overline{DOF}$	I/O	A liquid crystal blanking control pin. M/S = HIGH : Output M/S = LOW : Input When you want to use the S1D15719 Series in the master/slave mode, connect each $\overline{DOF}$ pin.	1

5.4 Liquid Crystal drive pin

Pin name	I/O	Description	Number of pins
SEG0 to SEG179	O	Liquid crystal segment drive output pins. One of the V_2, V_1, V_C, MV_1, and MV_2 levels is selected by a combination of the display RAM content and FR/F1/F2 signals.	total 180
COM0 to COM131	O	Liquid crystal common drive output pins. One of the V_3, V_C, V_{SS} levels is selected by a combination of the scan data and FR/F1/F2 signals.	total 132

5.5 Thermal sensor pins

Pin name	I/O	Description	Number of pins
SV_{D2}	O	Analog voltage output pin for thermal sensor.	1
SV_{22}	O	Thermal sensor test pin. Set to OPEN.	1

5.6 Pin for Test

Pin name	I/O	Description	Number of pins
TEST 1, 4	I	IC chip testing pin. Fix it to LOW.	1 each
TEST 2, 5	O	IC chip testing pin. Set it to OPEN.	1 each
TEST 3	I	IC chip testing pin. Fix it to HIGH.	1
TESTA	I	IC chip testing pin. Fix it to HIGH.	1
TESTB	I	Connect to V_{DI} pin	2

* If it is difficult to set each TEST pin as shown above due to constraints on tape carrier package (TCP) implementation, etc., you can set
  TEST3=V_{DI}, TEST4= V_{DI}, TESTA= V_{DI}, TESTB= V_{DI}
  However, since this setting can change output state of the built-in V_3 voltage adjusting circuit due to an unexpected factor such as excessive external noise, the following commands must be issued when performing initial setting and periodical setting.

	$\overline{E}$	R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	1	1	0	0

  If the built-in V_3 voltage adjusting circuit is not used, it is not required to issue the above commands when performing initial setting and periodical setting.

6. FUNCTIONAL DESCRIPTION

6.1 MPU interface

6.1.1 Selection of Interface Type

S1D15719 Series allows data to be sent via the 8-bit bi-directional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to HIGH or LOW, you can select either 8-bit parallel data input or serial data input, as shown in Table 6.1.

Table 6.1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH : Parallel input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW : Serial input	$\overline{CS}$	A0	—	—	—	SI	SCL	(HZ)

— : Fixed to HIGH or LOW HZ: High impedance state

6.1.2 parallel Interface

When the parallel interface is selected (P/S = HIGH), direction connection to the MPU bus of either 80 series MPU or 68 series MPU is performed by setting the 86 pin to either HIGH or LOW, as shown in Table 6.2.

Table 6.2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH : 68 series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW : 80 series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

The data bus signals are identified by a combination of A0, $\overline{RD}$ (E), and $\overline{WR}$ (R/$\overline{W}$) signals as shown in Table 6.3.

Table 6.3

Common	68 series	80 series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data read, status read, temperature sensor output read
1	0	1	0	Display data write, status write
0	0	1	0	Command write

6.1.3 Serial Interface

When the serial interface is selected (P/S=LOW), the chip is active ($\overline{CS}$=LOW), and reception of serial data input (SI) and serial clock input (SCL) is enabled. Serial interface comprises a 8-bit shift register and 3-bit counter. The serial data are latched by the rising edge of serial clock signals in the order of D7, D6, …. and D0 starting from the serial data input pin. On the rising edge of 8th serial clock signal, they are converted into 8-bit parallel data to be processed. Whether serial data input is a display data or command is identified by A0 input. A0 = HIGH indicates display data or command parameter, while A0 = LOW shows command. The A0 input is read and identified at every 8 × n-th rising edge of the serial clock after the chip has turned active.
Using the read status command and temperature sensor output read command enable read serial data, even when serial interface is selected. However, it should be noted that the $\overline{CS}$ signal is handled differently from the case of serial data input. Read from display data RAM is not enabled.
Fig.6.1 shows the serial interface signal chart.

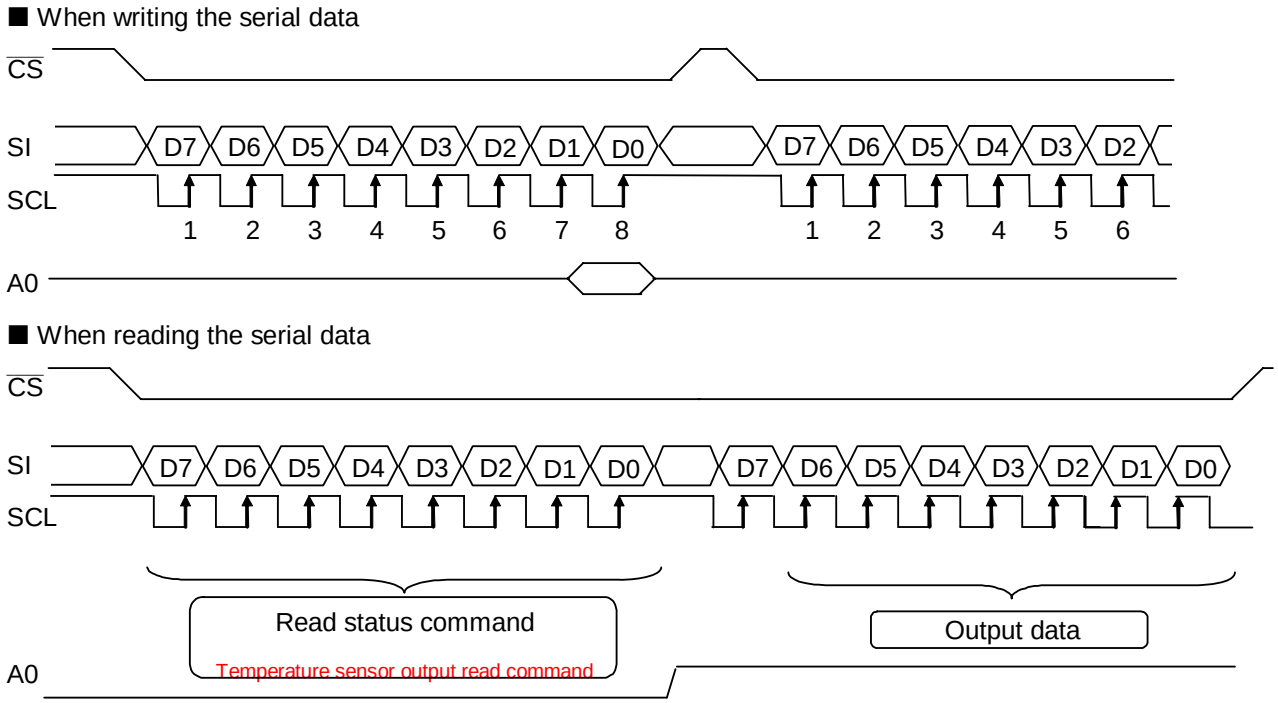


Fig.6.1 Signal Chart of Serial Interface

* When the chip is inactive, the counter is reset to the initial state. Although consecutive input of serial clocks is available, it is recommended to clear the counter for every 8 bits of serial clocks by selecting $\overline{CS}$=HIGH in order to prevent malfunctioning due to incoming noises.
* When the serial interface is used, reading data from RAM becomes unavailable.
* For the SCL signal, a sufficient care must be taken against terminal reflection of the wiring and external noise. Recommend to use an actual equipment to verify the operation.

6.1.4 Chip Selection

The S1D15719 Series has chip selection pin. Parallel interface or serial interface is enabled only when $\overline{CS}$ = LOW.
When the chip select pin is inactive, D0 to D7 are in the state of high impedance, while A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When serial interface is selected, the shift register and counter are reset.

6.1.5 Access to display data RAM and Internal register

Access to S1D15719 Series viewed from the MPU side is enabled only if the cycle time requirements are kept. This does not required waiting time; hence, high-speed data transfer is allowed.
Furthermore, at the time of data transfer with the MPU, S1D15719 Series provides a kind of inter-LSI pipe line processing via the bus holder accompanying the internal data bus.
For example, when data is written to the display data RAM by the MPU, the data is once held by the bus holder. It is written to the display data RAM before the next data write cycle comes.
On the other hand, when the MPU reads the content of the display data RAM, it is read in the first data read cycle (dummy), and the data is held in the bus holder. Then it is read onto on the system bus from the bus holder in the next data read cycle. Restrictions are imposed on the display data RAM read sequence. When the address has been set, specified address data is not output to the Read command immediately after that. The specified address data is output in the second data reading. This must be carefully noted. Therefore, one dummy read operation is mandatory subsequent to address setting or write cycle. Fig.6.2 illustrates this relationship.

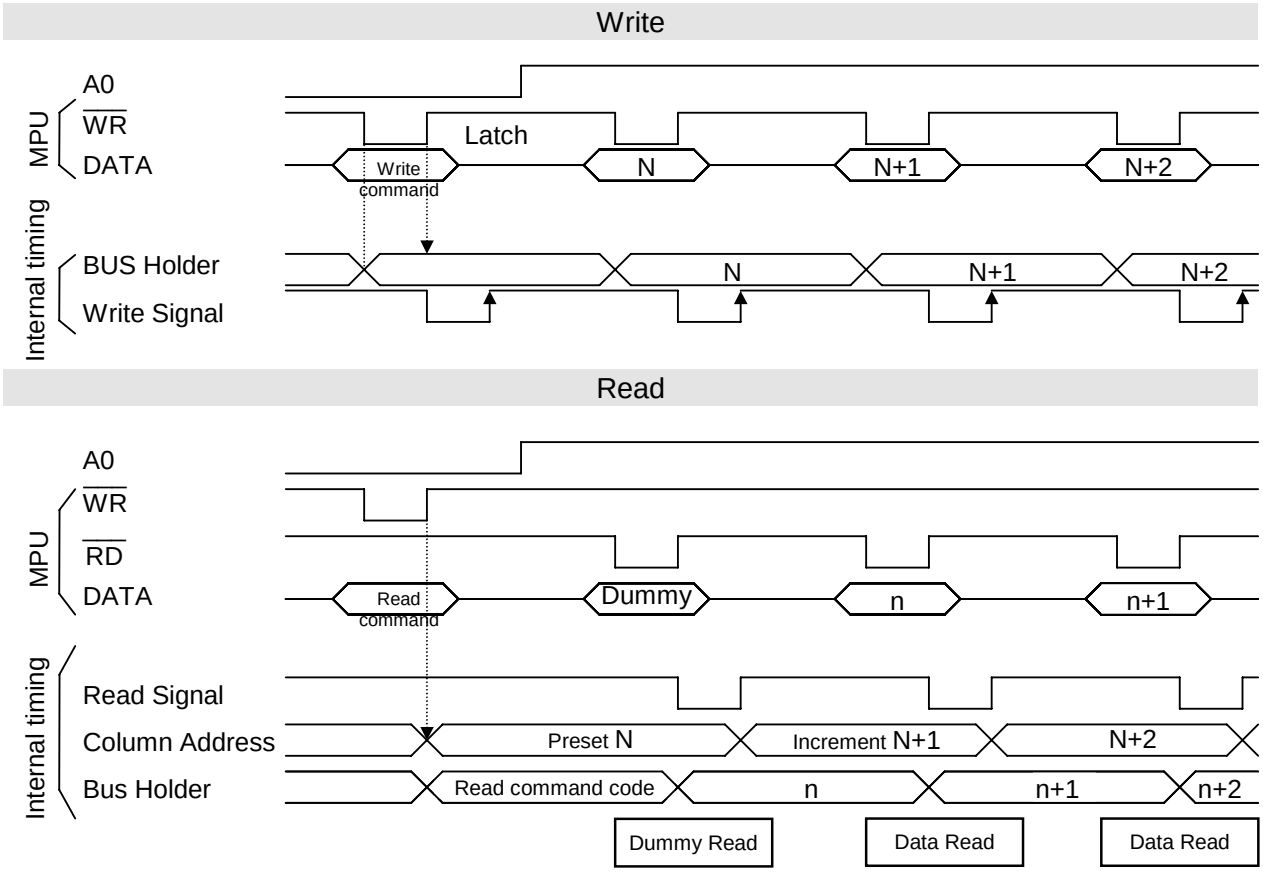


Fig.6.2 Display data RAM read sequence

6.2 Display data RAM

6.2.1 Display data RAM

This is a RAM to store the display dot data, and comprises 180 × 132 × 2 bits. Access to the desired bit is enabled by specifying the page address and column address. When the 4 gray-scale is selected by the Display Mode Set command, display data input for gray-scale display are processed as a two-bit pair. Combination is as follows:

(MSB, LSB) = (D1, D0), (D3, D2), (DS, D4), (D7, D6)

When the RAM bit data is gray-scale 1 and 2, gray-scale display is realized according to the parameter of the Gray-scale Pattern Set command.

RAM bit data (high order and low order)
(1,1): gray-scale 3 Black (when display is in normal mode)
(1,0): gray-scale 2
(1,1): gray-scale 1
(1,1): gray-scale 0 White (when display is in normal mode)

When binary display is selected by the Display Mode Set command, the RAM 1 bit built in the one-dot pixel responds to it. When the RAM bit data is “1”, the display is black. If it is “0”, the display is given in white.

RAM bit data
“1”: Light On Black (when display is in normal mode)
“0”: Light Off White (when display is in normal mode)

Display data D7 to D0 from the MPU correspond to LCD common direction, as shown in Fig.6.3 and 6.4. Therefore, less restrictions when multi-chip usage.
Furthermore, read/write operations from the MPU to the RAM are carried out via the input/output buffer. The read operation from Display data RAM is designed as an independent operation. Accordingly, even if the MPU accesses the RAM asynchronously during LCD display, no adverse effect is given to display.

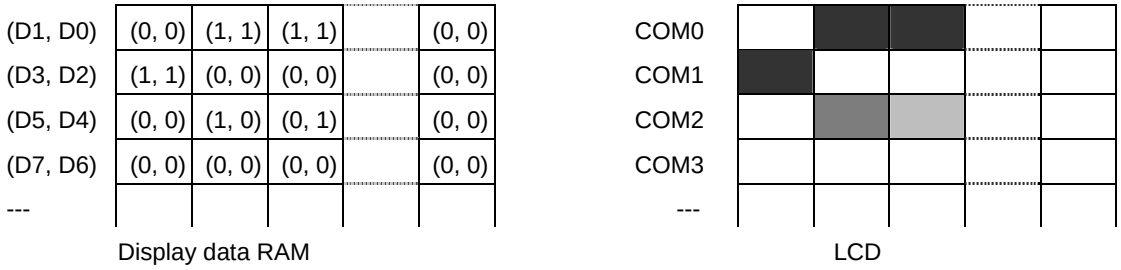


Fig.6.3 4 gray-scale

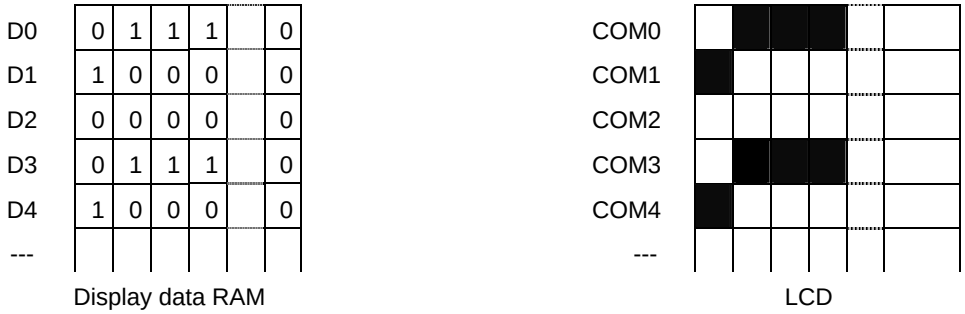


Fig.6.4 Binary

6.2.2 Display of gray-scale

When the 4 gray-scale are selected with the Display Mode Set command, gray-scales are represented through FRM (frame gray-scale) control, which is performed based on the gray-scale data written to the display data RAM.
Density of intermediate gray-scales (gray-scales 2 and 1) is specified by use of the gray-scale pattern set command. Density of the gray-scale is selectable from nine levels.

6.2.3 Page address circuit and column address circuit

Address of the target display data RAM of access is specified with the page address set command and the column address set command as shown in Fig.6.5 and 6.6.
Using the Display Data Input Direction Select command allows you to increase the address either in the column or page direction. In both cases, the address is incremented by +1 after the reading or writing operation.

When you chose to increase the address in the column direction, the column address is incremented by +1 for every write or read operation. After up to B3H of the column address has been accessed, the page address is incremented by +1 and the column address is shifted to 0H.
When you chose to increase the address in the page direction, the page address is incremented for every write or read operation while the column address being fixed to the current state. After up to Page32 of the page address has been accessed, the column address is incremented by +1 and the page address is shifted to Page0.

Whichever you may choose for the address increment direction, the page address and column address are returned to Page0 and 0H, respectively, after you have accessed the column address B3H of the page address Page32.

Using the column address set direction command allows you to reverse the correspondence between the display data RAM's column address and the segment output as shown in Table 6.4. This arrangement can alleviate the restrictions on IC layout in assembling the LCD module.

Table 6.4

Register value of column address set direction command		**Correspondence between RAM column address and SEG output**		
		SEG0	**→**	**SEG179**
D0 = "0"	Column addresses: Normal	0(H)	→	B3(H)
D0 = "1"	Column address: Reverse	B3(H)	←	0(H)

6.2.4 Line address circuit

The line address circuit is used to specify the line address corresponding to COM output when displaying contents of the display data RAM. See Fig.6.5 and 6.6. You should normally specify the top display line (state of the common output, namely COM0 output for the normal mode and COM131 output for the reverse) with the Display Start Line Set command. The display area covers from the specified display start line up to the line specified with the number of display lines set command in the line address increasing direction.

It is required to specify the display start line address for every four-display line. Dynamic change of the line address by use of the Display Start Line Set command allows screen scrolling as well as changing of pages.

6.2.5 Display data latch circuit

The display data larch circuit is a latch to temporarily latch the display, data output from then display data RAM to the liquid crystal drive circuit. Display normal/reverse, display ON/OFF, and display all lighting ON/OFF commands control the data in this latch, without the data in the display data RAM being controlled.

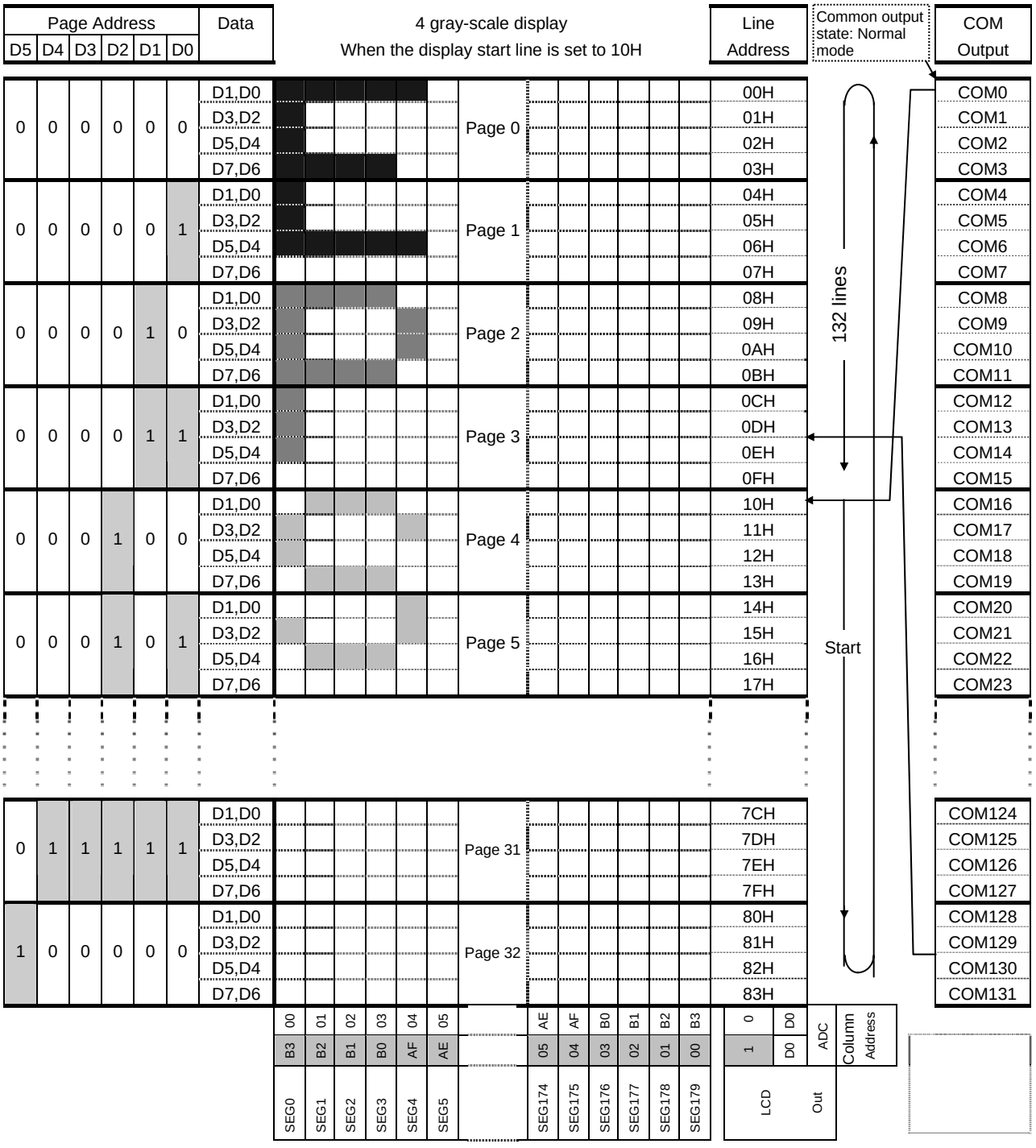


Fig.6.5 4 Gray-scale Display

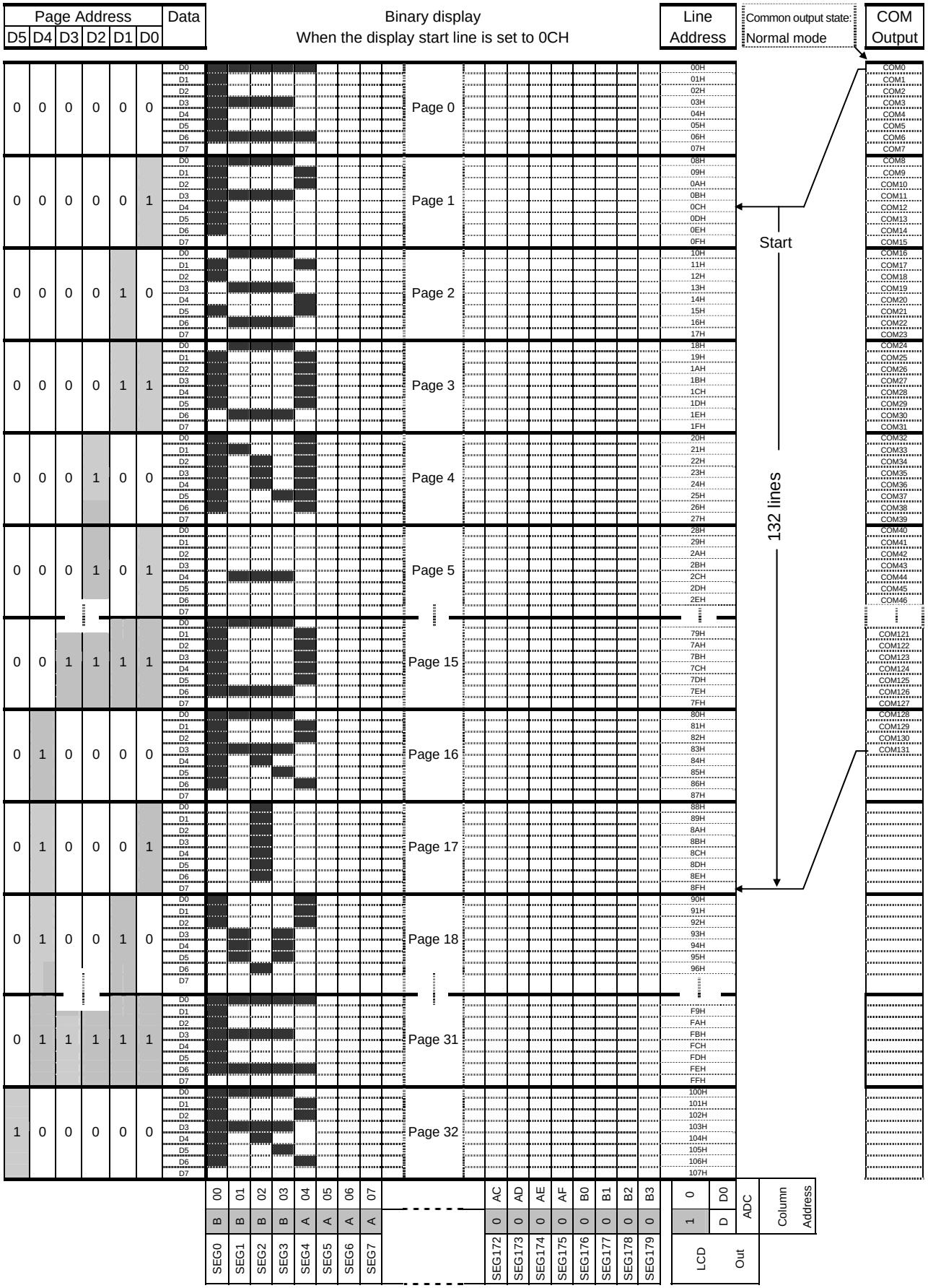

Page Address
D5 D4 D3 D2 D1 D0
Data
Binary display
When the display start line is set to 0CH
Line Address
Common output state:
Normal mode
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 15
Page 16
Page 17
Page 18
Page 31
Page 32
Start
132 lines
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG172
SEG173
SEG174
SEG175
SEG176
SEG177
SEG178
SEG179
LCD Out
ADC
Column Address

Fig.6.6 Binary Display

6.3 Oscillator circuit

A display clock is generated by the CR oscillator. The oscillator circuit is enabled only when M/S = HIGH and CLS = HIGH. Oscillation starts after input of the built-in oscillator circuit ON command input.
When CLS = LOW, oscillation stops, and display clock is input from the CL pin.

6.4 Display timing generation circuit

Timing signals are generated from the display clock to the line address circuit and display data latch circuit. Synchronized with display clock, display data is latched in display data latch circuit, and is output to the segment drive output pin. Reading of the display data into the LCD drive circuit is completely independent of access from the MPU to the display data RAM. Accordingly, asynchronous access to the display data RAM during LCD display does not give any adverse effect; like as flicker.
Furthermore, the display clock generates internal common timing, liquid crystal alternating signal (FR), field start signal (SYNC) and drive pattern signal (F1 and F2).
The FR normally generates 2-frame alternating drive system drive waveform to the liquid crystal drive circuit. The n-line reverse alternating drive waveform is generated for each 4 × (a+1) line by setting data on the n-line reverse drive register. When there is a display quality problem including crosstalk, the problem may be solved using the n-line reverse alternating drive.
Execute liquid crystal display to determine the number of lines "n" for alternation.
When you want to use the S1D15719 Series in multi-chip configuration, supply display timing signal (FR, SYNC, F1, F2, CL, $\overline{DOF}$) to the slave side from the master side. Table 6.5 shows the statuses or FR, SYNC, F1, F2, CL, $\overline{DOF}$.

Table 6.5

Operating mode		CL	FR, SYNC, F1, F2, $\overline{DOF}$
Master (M/S = HIGH)	Built-in oscillator circuit enabled (CLS = HIGH)	Output	Output
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Output
Slave (M/S = LOW)	Built-in oscillator circuit enabled (CLS = HIGH)	Input	Input
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Input

6.5 Operating mode detection circuit

If state of the display data RAM or a command register is changed by excessive incoming noises, this circuit detects such change and warns an error. The output level from the pin ERR allows you to know whether or not the error is developing. You can also determine existence of the error by reading the state from the data bus using the status read command.
Table 6.6 shows the relation between the internal state and output level from the pin ERRS.(S1D15719D10B).
Concerning S1D15719D11B and S1D15719D12B, the ERR pin is NC.(The register read by Status read command is possible.)

Table 6.6

Output	Descriptions
LOW	Operation is done normally.
HIGH	Garbling of bits on the display data RAM or some command registers is suspected.

When the level is HIGH, you may suspect that inappropriate information is displayed because of garbled bits on the display data RAM or display operation is not normally carried out due to garbled bits on a command register. In order to avoid above trouble, you should monitor the output level from the pin ERR or check operating mode of IC on a regular basis by use of the status read command. If the error is detected, recover the normal display operation by rewriting every bit on the display data RAM and also setting every command again.

This circuit is used to detect the specific error modes alone and also is not intended to support all the command registers. For the supportable command registers and supplementary explanation, refer to 7.1 Command Description (29) Status read.

6.6 Liquid crystal drive circuit

6.6.1 SEG Drivers

This is a SEG output circuit. It selects the five values of V_2, V_1, V_C, MV_1 and MV_2 using the driver control signal determined by the decoder, and output them.

6.6.2 COM Drivers

This is a COM output circuit. It selects three values of V_3, V_C and V_{SS} using the driver control signal determined by the decoder, and output them.
S1D15719 Series allows the COM output scanning direction to be set by the common output status select command. (See Table 6.7). This will reduce restrictions on IC layout during LCD module assembling.

Table 6.7

Status	Direction of COM scanning		
Normal	COM 0	→	COM131
Reverse	COM 131	→	COM 0

6.6.3 Dummy Selection Period

Immediately after COM scanning has been completed, the selection period equivalent to 4 lines of display is provided as dummy. Therefore, the relationship between the number of display lines l set up by the set the number of display line command and display duty (1 selection period length of liquid crystal line sequential drive for frame cycle) is

$$duty = 1 / (l + 4)$$

Some liquid crystal display patterns allow reduction of cross talk by changing the SEG output during dummy selection period using the set the display mode command

6.7 Power Supply Circuit

This low-power consumption power supply circuit is used to generate the voltage necessary to drive liquid crystal. It comprises the 1st booster circuit, 2nd booster circuit, V_3 voltage regulating circuit and LCD voltage generating circuit.

The 1st booster circuit, 2nd booster circuit, V_3 voltage regulating circuit and LCD-voltage generating circuit on the power supply circuit are turned on or off with the power control set command. It allows using part of functions of the external and internal power supplies in parallel.

Table 6.8 shows the functions controlled by 4-bit data of the power control set command.

Table 6.8 Target of control of respective bits of power control set command

Item		Bits "1"	Bits "0"
D3	2nd booster circuit control bit	ON	OFF
D2	1st booster circuit control bit	ON	OFF
D1	V_3 voltage regulating circuit control bit	ON	OFF
D0	LCD voltage generating circuit control bit	ON	OFF

6.7.1 Blocks of power supply circuit and combinations of their operations

Fig.6.7 shows relation among the blocks of the power supply circuit with respect to their potential and Table 6.9 summarizes functions of these blocks.

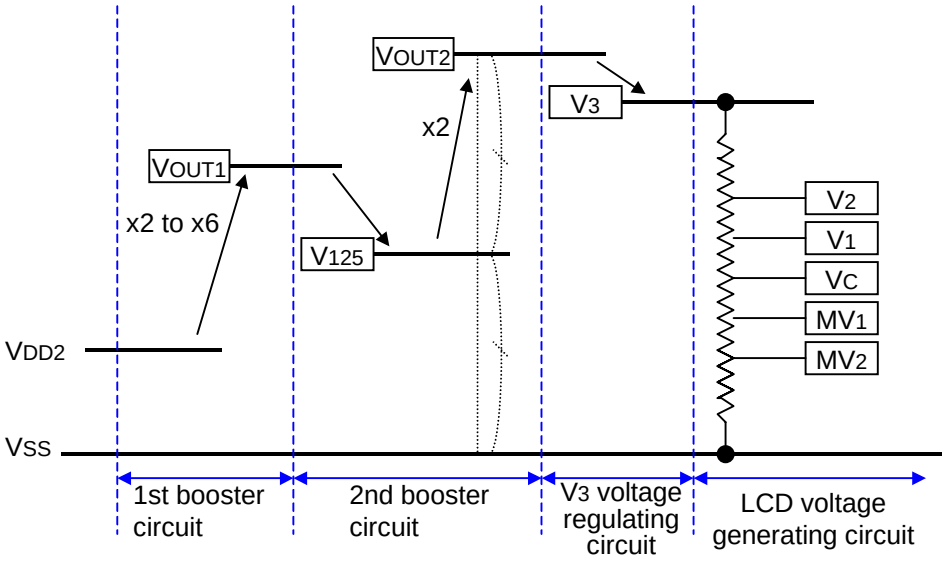


Fig.6.7 Relation among Power Supply Circuit Blocks with respect to their Potential

Table 6.9

Item	Input voltages	Functions	Output voltages
1st booster circuit	V_{DD2}	It generates V_{OUT1} by stepping up the voltage across V_{DD2}-V_{SS} by use of the charge pump. When connected to an external booster capacitor, it can boost the voltage in the range of 2 to 6 times.	V_{OUT1}
2nd booster circuit	V_{OUT1}	It comprises the voltage regulating circuit and the double-boosting circuit. The former operates on V_{OUT1} voltage system and is used to generate V_{125}, the base voltage of the voltage regulating circuit. The latter doubles V_{125} to generate V_{OUT2}.	V_{125}, V_{OUT2}
V_3 voltage regulating circuit	V_{OUT2}	It operates on V_{OUT2} voltage system and is used to generate LCD voltage V_3.	V_3
LCD voltage generating circuit	V_3	It resistively divide the voltage across V_3-V_{SS} with the bias ratio and then generates LCD voltages V_2, V_1, V_C, MV_1 and MV_2 on the impedance conversion circuit, which is operated on V_3 voltage system.	V_2, V_1, V_C, MV_1, MV_2

Following five types of functional combinations of the power supply circuit blocks become available depending on the register value set with the power control set command.

① Using every built-in power supply circuits - 1st and 2nd booster circuits, V_3 voltage regulating circuit and LCD voltage generating circuit
Above is applicable when the external supply of V_{OUT1} and V_3 voltage is not available. Every voltage necessary to drive liquid crystal is generated from V_{DD2}.

② Using the 1st booster circuit, V_3 voltage generating circuit and LCD-voltage generating circuit (2nd booster circuit is not used)
Above is applicable when the external supply of V_{OUT1} and V_3 voltage is not available. Every voltage necessary to drive liquid crystal is generated from V_{DD2} voltage.

Stopping operation of the 2nd booster circuit allows reducing the number of the booster capacitors used. Since the V_3 voltage regulating circuit, which was originally intended for V_{OUT2} voltage system, is operated on V_{OUT1} voltage system in this case, you must short- circuit V_{OUT1}, V_{125} and V_{OUT2} respectively.

Turn on or off the 2nd booster circuit taking into consideration of the following factors:
- Output impedance of the 1st booster circuit (it depends on V_{DD2} voltage, number of step-ups, capacitor capacity and wiring resistance.)
- Volume of current consumed on the panel.
- Level of V_3 voltage necessary to ensure an appropriate contrast.

For the detail, refer to Fig.6.8.

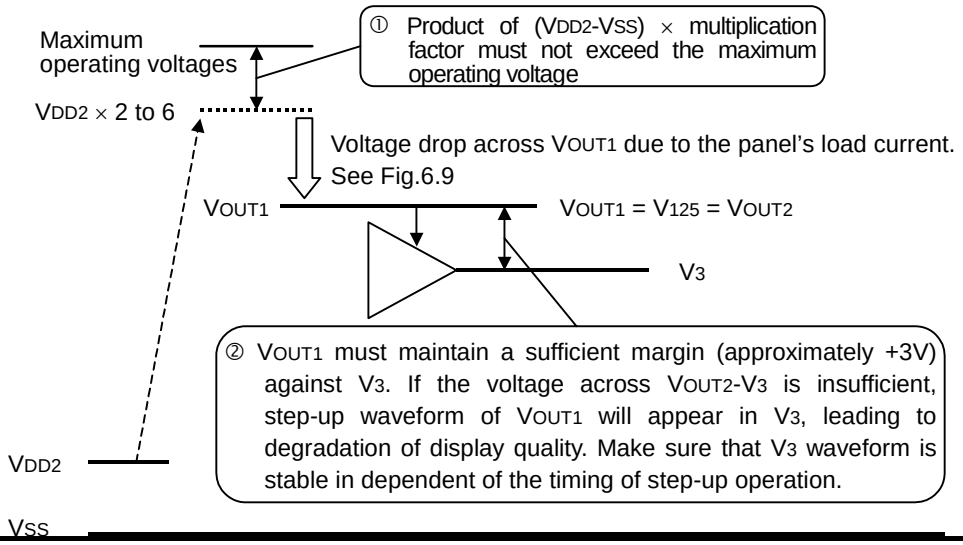


Fig.6.8 When 1st booster circuit alone is sufficient for the Operation

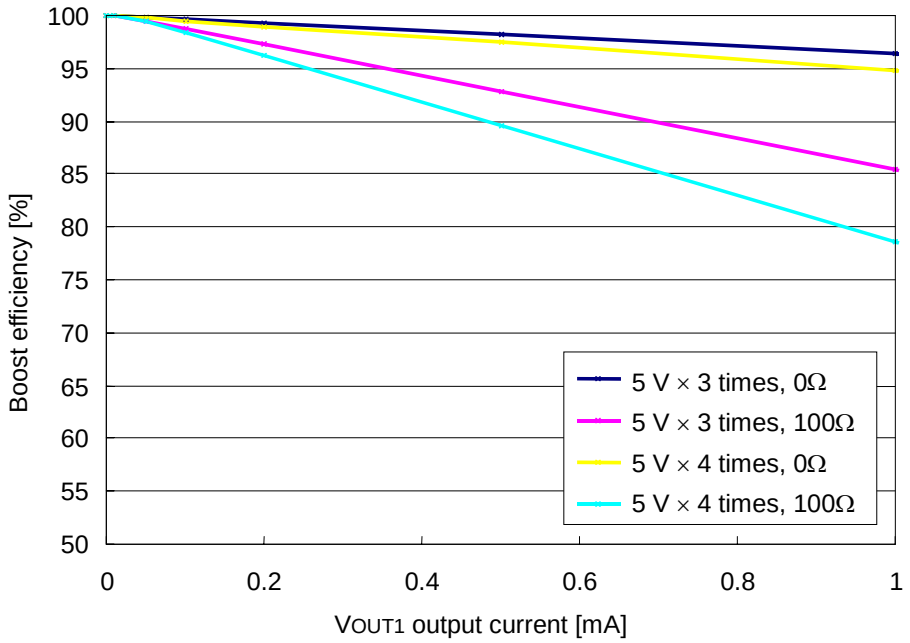


Fig.6.9 1st Booster Circuit Load Current Characteristics

* Load current characteristics of the built-in 1st booster circuit when there is no resistance or there is a 100-ohm resistance between each CAP pin and capacitor at the 1st boosting system. ITO wiring resistance is assumed.
  The reference data indicates to what extent the voltage is dropped when current is drawn from the V_{OUT1} pin where the V_{OUT1} voltage is 100 % at 0 mA of load current. If the 2nd booster circuit is not used, current load of V_{OUT1} becomes equal to current consumption in the V3 series.
  [Measurement conditions] V_{DD} = V_{DD2} = 5V, series resistor of 50 ohm is added between the capacitor for boosting of 4.7 µF, V_{DD}, and V_{SS} and the respective power supplies.

When the primary step-up alone is not sufficient to secure the voltage margin across V_{OUT1}-V_3, use the 2nd booster circuit in parallel. In such a case, it should be noted that current load twice as high as current consumption of the V_3 series is applied to V_{OUT1}. Fig.10 lists the points to be kept in mind when using the 2nd booster circuit.

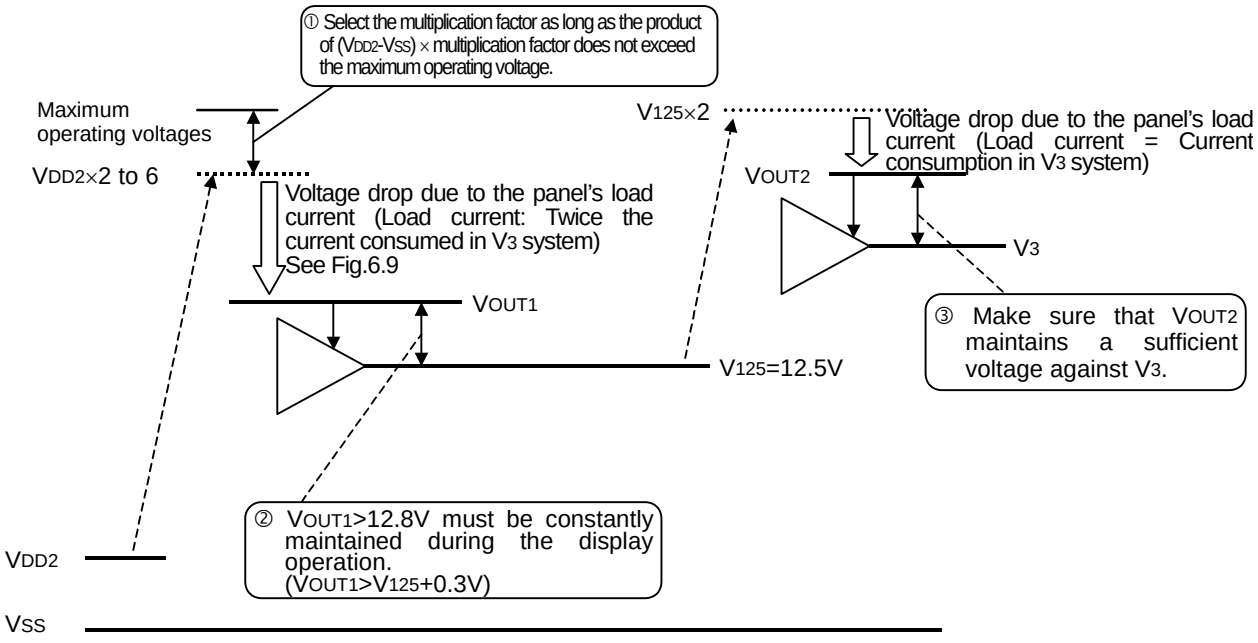


Fig.6.10 Precautions for use of 2nd booster circuit

③ Use of the second booster circuit, V_3 voltage adjusting circuit, liquid crystal drive voltage generation circuit only (1st booster circuit not used)

Available if the V_{OUT1} voltage can be supplied externally. The 1st booster circuit is not used when connecting with the external circuit, however, set it to "use" in the command setting.

If there is supply power voltage exceeding V_{DD2} maximum operating voltage value where the double boosting is admissible to generate the specified V_3 voltage, supply the V_{OUT1} voltage without connecting the capacitor to the 1st booster circuit. Also, even if V_{OUT1} voltage of the external supply is below 12.5V, do not supply it from V_{125}.

Precautions when not using the 1st booster circuit are shown in Fig.6.11.

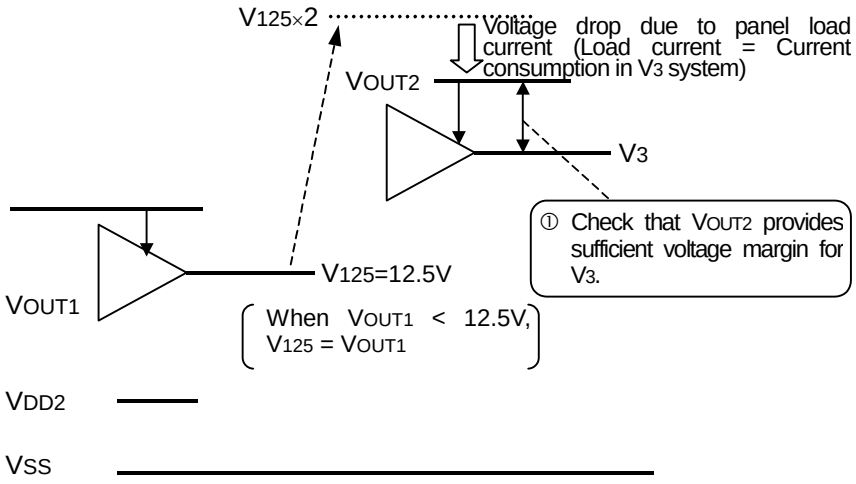


Fig.6.11 Precautions when not using the 1st booster circuit

When the current value consumed by the panel is so large that you can't secure the necessary voltage margin across V_{OUT2}-V_3 by use of the 2nd booster circuit, stop using the 2nd booster circuit. And then select one of the following approaches of ③, ④ or ⑤ to drive the panel.

④ Using the V_3 voltage regulating circuit and LCD-voltage generating circuit

Above is applicable when external supply of V_{OUT2} voltage is available. In this case, V_3, V_2, V_1, V_C, MV_1 and MV_2 voltages are generated and output from the built-in V_3 voltage regulating circuit and the built-in LCD voltage generating circuit. Connect the voltage holding capacitor to the respective LCD voltages.

V_3 voltage becomes adjustable with the V_3 voltage select command as well as the electronic volume command. The V_3 voltage regulating circuit operates on V_{OUT2} voltage. In order to maintain the operating margin, the V_{OUT2} supplied must meet the following requirement: $V_{OUT2} \geq V_3 + 0.3V$.

⑤ Using the LCD voltage generating current alone

Above is applicable when external supply of V_3 voltage is available. Connect the voltage holding capacitor to the respective internally generated LCD voltages.

⑥ Using external power supply alone (all internal power supplies are turned OFF)

Above is applicable when external supply of V_3, V_2, V_1, V_C, MV_1 and MV_2 are available.

Table 6.10

Circuit used	D3	D2	D1	D0	2nd booster circuit	1st booster circuit	V_3 voltage regulating circuit	LCD voltage generating circuit	Externally input power
① All built-in power supplies	1	1	1	1	Enable	Enable	Enable	Enable	—
② 1st booster circuit, V_3 voltage regulating circuit and LCD-voltage generating circuit	0	1	1	1	Disable	Enable	Enable	Enable	—
③ 2nd booster circuit, V_3 voltage adjusting circuit and liquid crystal drive voltage generation circuit (1st booster circuit is ON in setting)	1	1	1	1	Enable	Enable	Enable	Enable	V_{OUT1}
④ V_3 voltage regulating circuit and LCD-voltage generating circuit	0	0	1	1	Disable	Disable	Enable	Enable	V_{OUT2}
⑤ LCD-voltage generating circuit	0	0	0	1	Disable	Disable	Disable	Enable	V_3
⑥ External power supply alone	0	0	0	0	Disable	Disable	Disable	Disable	V_3, V_2, V_1, V_C, MV_1, MV_2

* Combinations listed in above table alone are usable.

6.7.2 1st booster circuit

This circuit allows amplifying the voltage across V_{DD2}-V_{SS} by sextuple, quintuple, quadruple, triple and double booster.

① For sextuple boosting
Connect capacitor C1 across CAP1+ ⇔ CAP1-, CAP2+ ⇔ CAP2-, CAP3+ ⇔ CAP1-, CAP4+ ⇔ CAP2- and V_{DD2} ⇔ V_{OUT1}.

② For quintuple boosting
Connect capacitor C1 across CAP1+ ⇔ CAP1-, CAP2+ ⇔ CAP2-, CAP3+ ⇔ CAP1-, CAP4+ ⇔ CAP2- and V_{DD2} ⇔ V_{OUT1}. Then short-circuit CAP5+ and V_{OUT1} pin.

③ For quadruple boosting
Connect capacitor C1 across CAP1+ ⇔ CAP1-, CAP2+ ⇔ CAP2-, CAP3+ ⇔ CAP1-, V_{DD2} ⇔V_{OUT1}. Then short-circuit CAP5+, CAP4+ and V_{OUT1} pin.

④ For triple boosting
Connect capacitor C1 across CAP1+ ⇔ CAP1-, CAP2+ ⇔ CAP2- and V_{DD2} ⇔ V_{OUT1}. Then short-circuit CAP5+, CAP4+, CAP3+ and V_{OUT1} pin.

⑤ For double boosting
Connect capacitor C1 across CAP1+ ⇔ CAP1- and V_{DD2} ⇔ V_{OUT1} pin and set CAP2- to OPEN. Then short-circuit CAP5+, CAP4+, CAP3+, CAP2+ and V_{OUT1} pin.

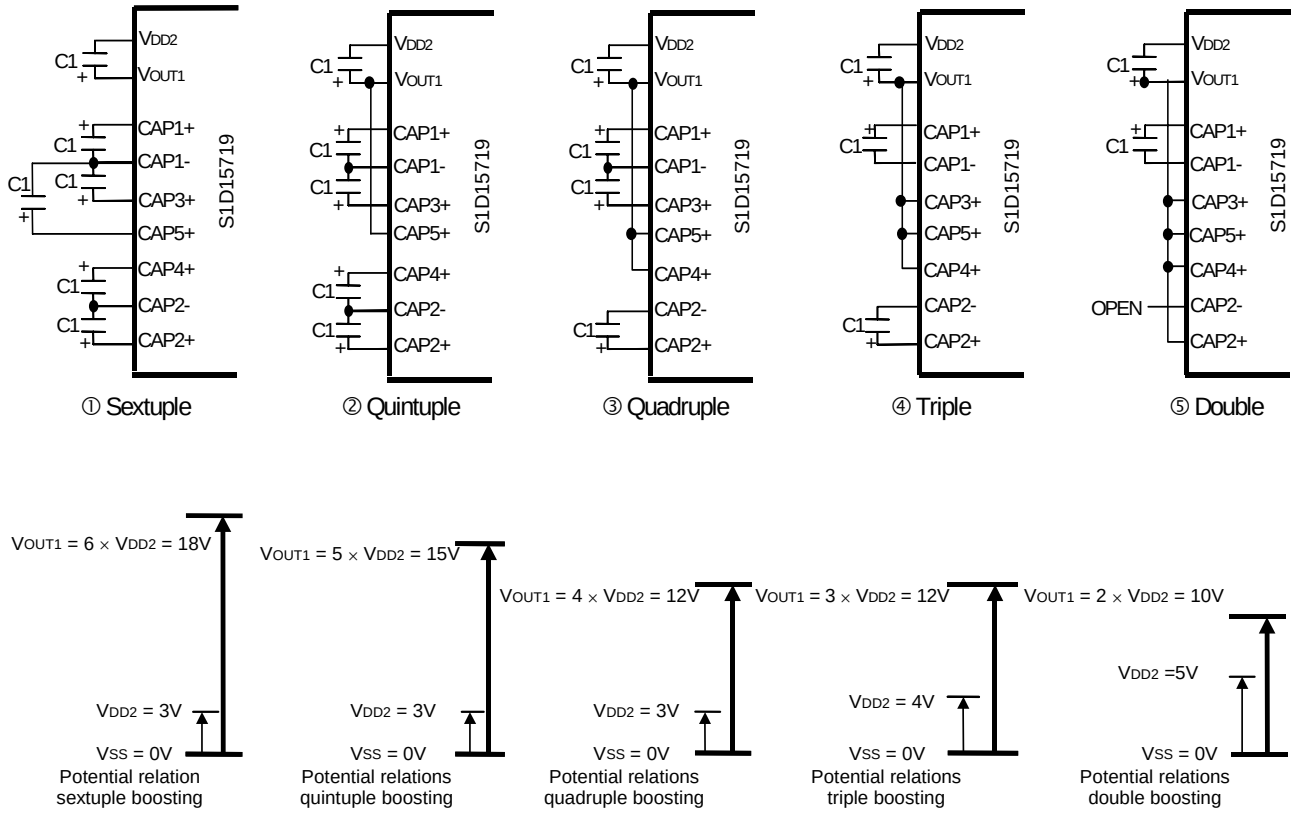


Fig.6.12 1st booster circuit - Capacitor Connection and Potential Relation

Voltage span of V_{DD2} must be set so that the voltage on V_{OUT1} pin does not exceed the maximum operating voltage.

Example) When V_{DD2}+10% is specified as the maximum margin of fluctuation of V_{DD2} (V_{DD2}Max.):

[For sextuple boosting]

Since V_{DD2}Max. × 6 ≤ Maximum operating voltage (V_{OUT1}-V_{SS}=25[V]), the voltage must be set within the following span:

$V_{DD2} \leq 3.7[V]+10\%$

[For quintuple boosting]

Since V_{DD2}Max. × 5 ≤ Maximum operating voltage (V_{OUT1}-V_{SS}=25[V]), the voltage must be set within the following span:

$V_{DD2} \leq 4.5[V]+10\%$

[For quadruple boosting]

Since V_{DD2}Max. × 4 ≤ Maximum operating voltage (V_{OUT1}-V_{SS}=25[V]), resulting span becomes $V_{DD2} \leq$ 5.6[V]+10%. In this case, however, following operable range of V_{DD2} is employed:

$V_{DD2} \leq 5.0[V]+10\%$

[For triple boosting]

Since V_{DD2}Max. × 3 ≤ Maximum operating voltage (V_{OUT1}-V_{SS}=25[V]), resulting span becomes $V_{DD2} \leq$ 7.5[V]+10%. In this case, however, following operable range of V_{DD2} is employed:

$V_{DD2} \leq 5.0[V]+10\%$

[For double boosting]

Since V_{DD2}Max. × 2 ≤ Maximum operating voltage (V_{OUT1}-V_{SS}=25[V]), resulting span becomes $V_{DD2} \leq$ 11.3[V] ±10%. In this case, however, following operable range of V_{DD2} is employed:

$V_{DD2} \leq 5.0[V]\pm10\%$

6.7.3 2nd booster circuit

6.7.3.1 Voltage regulating circuit

This regulator operates on V_{OUT1} power generated in the 1st booster circuit and is used to generate input voltage for the double-boosting circuit (to be described later).
Since the output V_{125} of the regulator is 12.5V at maximum, the output V_{OUT2} after amplification by two times does not exceed the maximum operating voltage 25.0[V].

6.7.3.2 Double-boosting circuit

It generates V_{OUT2} by doubling the voltage across V_{125}-V_{DD2} or V_{SS}.
Used by connecting the capacitors C1 between CAP6+ and CAP6- and V_{OUT2} and V_{SS}.
As for V_{125}, connect the capacitors C1 between V_{DD2} or V_{SS} and itself. If not affect the evaluation result display, this can be set to OPEN.

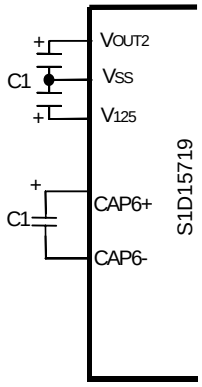


Fig.6.13 Connection Diagram of Capacitor of the 2nd Booster Circuit

When operating V_3 regulating circuit with output V_{OUT1} from the 1st booster circuit while turning off the 2nd booster circuit, V_{125} and V_{OUT2} are short-circuited to V_{OUT1}.
Also, it is possible not to use the 1st booster circuit but only use the 2nd booster circuit by inputting the V_{OUT1} voltage externally. In this case, use the 1st booster circuit in set power control command setting (register D2="1").

6.7.4 V_3 voltage regulating circuit

V_{OUT2}, which is externally entered or generated on the step-up circuit, is output from the voltage regulating circuit as the LCD voltage V_3. The voltage regulating circuit is controlled with the V_3 voltage regulating command and the electronic volume command.
Being equipped with the high-precision constant voltage source, this IC contains the function for switching the LCD voltage in eight levels as well as the 128-step electronic volume function. Thus, you can adjust the LCD voltage accurately by use of the commands alone without adding external parts.

6.7.4.1 V_3 voltage output range

Using the V_3 voltage adjusting command, you can choose one of the eight different V_3 voltage ranges from the 3-bit register. Table 6.11 determines V_3 voltage by use of the V_3 voltage adjusting command and the electronic volume command. The precision is ±3% maximum at 25°C. Set not to fall below 11.0V that is a lower limit of the V_3 operating voltage range.

Table 6.11

V_3 voltage select command register value			V_3 voltage output range [V]	V3 voltage calculating formula [V] (α = 0 to 127)
D2	D1	D0		
0	0	0	10.49 to 17.35	$10.489 + 0.054 \times \alpha$
0	0	1	10.97 to 18.21	$10.966 + 0.057 \times \alpha$
0	1	0	11.49 to 19.11	$11.488 + 0.060 \times \alpha$
0	1	1	12.06 to 20.06	$12.063 + 0.063 \times \alpha$
1	0	0	12.70 to 21.08	$12.697 + 0.066 \times \alpha$
1	0	1	13.40 to 22.17	$13.403 + 0.069 \times \alpha$
1	1	0	14.19 to 23.59	$14.191 + 0.074 \times \alpha$
1	1	1	15.08 to 24.98	$15.078 + 0.078 \times \alpha$

* Above is applicable at T_a = 25°C

6.7.4.2 Electronic volume

In Formula 6.1 represents the register value of the electronic volume command. You can select one of 128 states by setting data on the 7-bit electronic volume register. Table 6.12 shows the value of α corresponding to the setting on the electronic volume register.

Table 6.12

D6	D5	D4	D3	D2	D1	D0	α	V_3 voltage
0	0	0	0	0	0	0	0	Small
0	0	0	0	0	0	1	1	↑
0	0	0	0	0	1	0	2	↑
			⋮				⋮	↑
1	1	1	1	1	0	1	125	↑
1	1	1	1	1	1	0	126	↓
1	1	1	1	1	1	1	127	Large

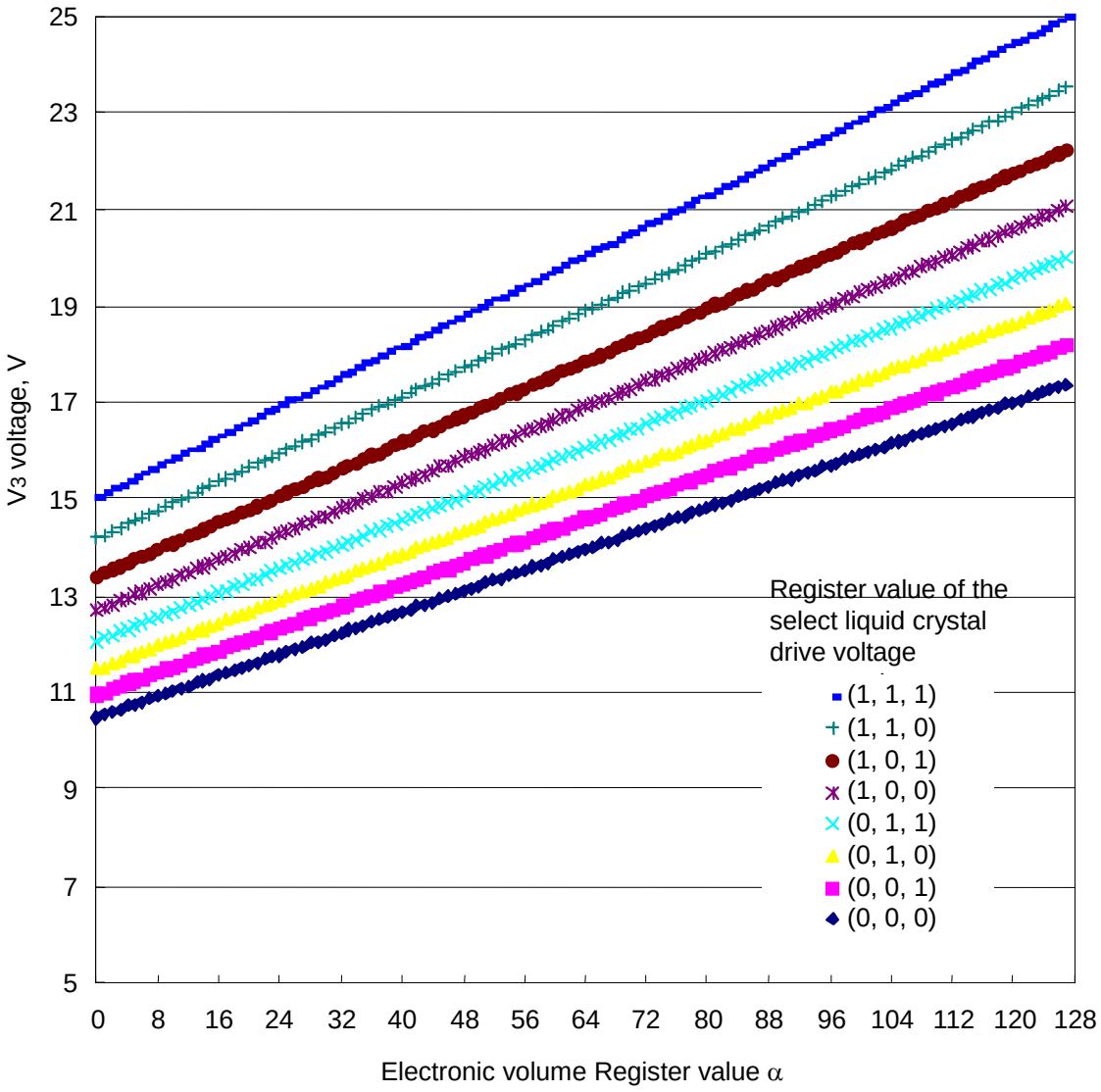

25
23
21
19
17
15
13
11
9
7
5
V3 voltage, V
0
8
16
24
32
40
48
56
64
72
80
88
96
104
112
120
128
Electronic volume Register value α
Register value of the select liquid crystal drive voltage
(1, 1, 1)
(1, 1, 0)
(1, 0, 1)
(1, 0, 0)
(0, 1, 1)
(0, 1, 0)
(0, 0, 1)
(0, 0, 0)

Fig.6.14

6.7.5 Liquid crystal drive voltage generation circuit

Voltages V_3 is converted by resistive divider to produce V_2, V_1, V_C, MV_1 and MV_2 voltages. V_2, V_1, V_C, MV_1 and MV_2 voltages are impedance - converted by the voltage follower, and is supplied to the liquid crystal drive circuit. A bias ratio is chosen by the bias set command.

Table 6.13

Potential	LCD bias set command register value (D1, D0)			
	(0, 0) 1/11 Bias	(0, 1) 1/10 Bias	(1, 0) 1/9 Bias	(1, 1) 1/8 Bias
V_2	7.5/11・V_3	7/10・V_3	6.5/9・V_3	6/8・V_3
V_1	6.5/11・V_3	6/10・V_3	5.5/9・V_3	5/8・V_3
V_C	5.5/11・V_3	5/10・V_3	4.5/9・V_3	4/8・V_3
MV_1	4.5/11・V_3	4/10・V_3	3.5/9・V_3	3/8・V_3
MV_2	3.5/11・V_3	3/10・V_3	2.5/9・V_3	2/8・V_3

6.7.6 Temperature gradient selection circuit

This circuit is used to select the temperature gradient characteristics of V_3 voltage. You can set one of the eight types of temperature gradient characteristics by use of the temperature gradient set command. Since you can select a type of temperature characteristics suitable for the liquid crystal used, you don't have to resort to external devices for compensating V_3 voltage's temperature characteristics when developing a system.

Voltage range of V_3 deviates from Table 6-11 by the ambient temperature-dependent temperature gradient.
Example) When V_3 voltage select command register value is (D2, D1, D0 = 0, 1, 1), Table 6-11 gives following V_3 voltage range.
12.06 to 20.06 [V]
If you select -0.06%/°C as the temperature gradient, volume of temperature change of V_3 at 35°C is determined by the following equation.

$$\Delta V_3 = V_3 \times (35°C - 25°C) \times \frac{(-0.06\ \% / °C)}{100}\ [V]$$

Voltage range of V_3, therefore, becomes 11.99V to 19.94V.

6.8 Examples of peripheral circuits of power supply circuit

6.8.1 S1D15719D10B000

6.8.1.1 An example of when using every built-in power supply

An example of sextuple boosting

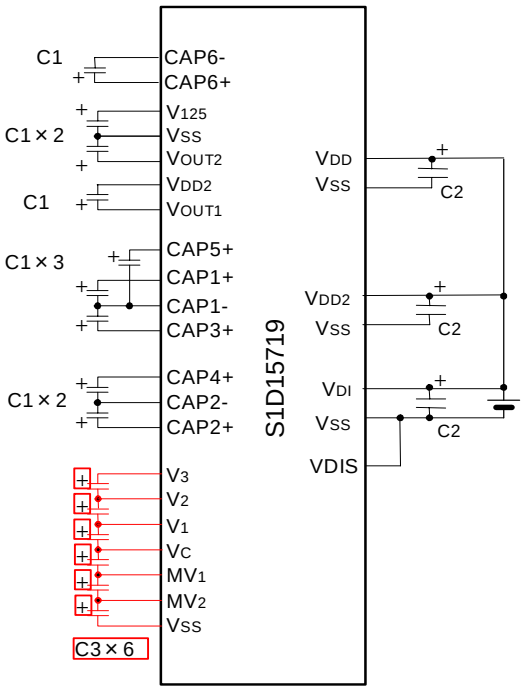


Fig.6.16

6.8.1.2 When using the 2nd booster circuit, V3 voltage regulating circuit and LCD-voltage generating circuit (1st booster circuit is turned off)

An example of VDD=VDD2, internal VDI circuit

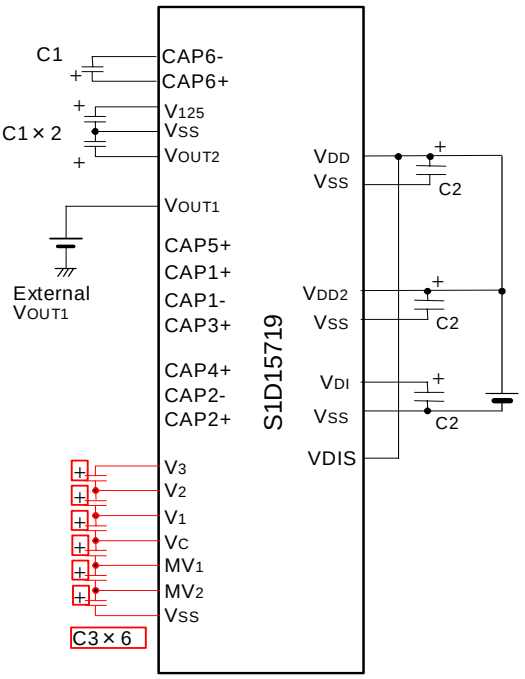


Fig.6.17

6.8.1.3 When using the 1st booster circuit, V3 voltage regulating circuit and LCD-voltage generating circuit (2nd booster circuit is turned off)

An example quintuple boosting

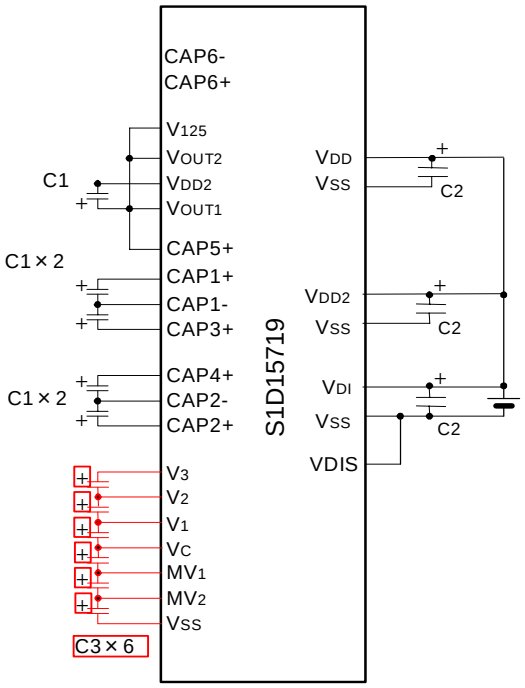


Fig.6.18

An example triple boosting

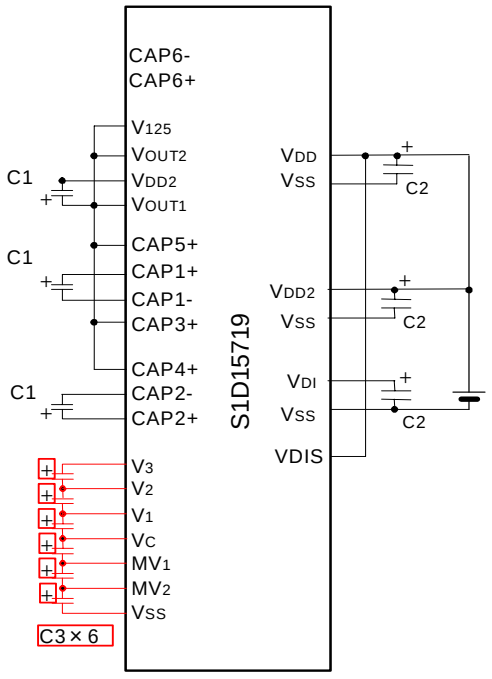


Fig6.19

6.8.1.4 When using V_3 voltage regulating circuit and LCD-voltage generating current

(1st and 2nd booster circuits are turned off)

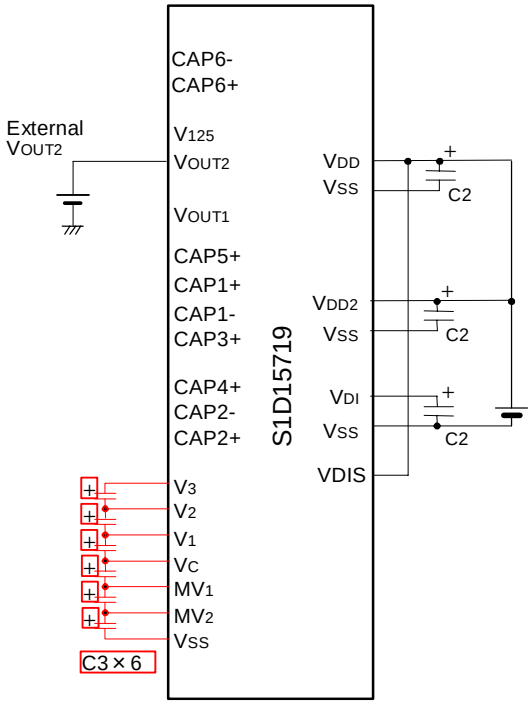


Fig.6.20

6.8.1.5 When using LCD voltage generating circuit

(1st and 2nd booster circuits and V_3 voltage regulating circuit are turned off)

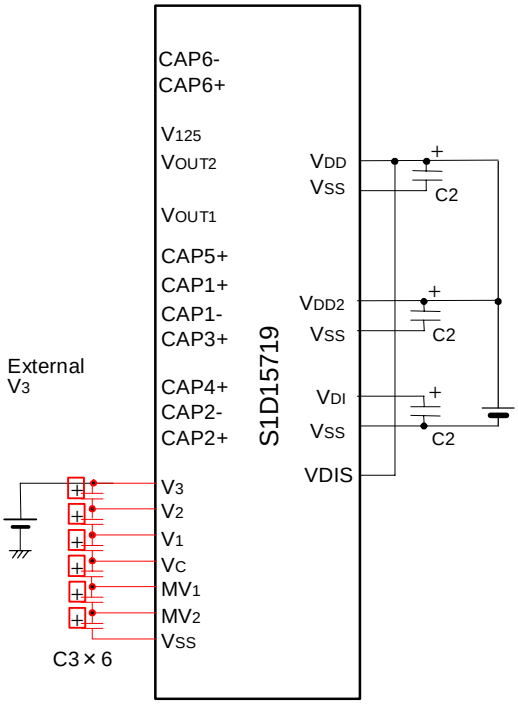


Fig.6.21

6.8.1.6 All internal power supplies are turned off

(All necessary voltages including LCD voltage are externally supplied)

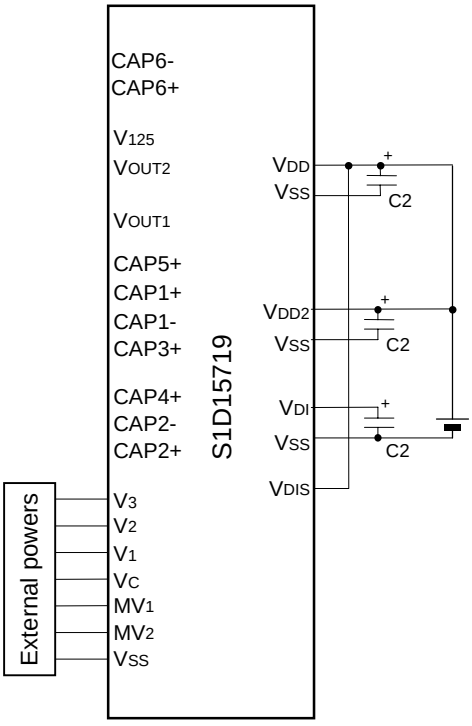
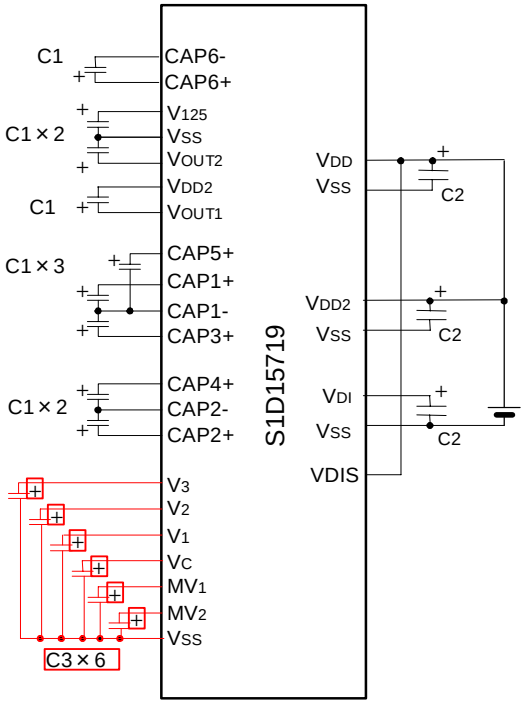


Fig.6.22

6.8.1.7 Another example of connecting capacitor for LCD voltage

(when all internal power supplies are used for sextuple boosting)



*Above is also usable in the connection examples shown in 6.8.1.1 to 6.8.1.5

Fig.6.23

*: About Capacitor connection between V3, V2, V1,VC, MV1 and MV2

In case to use S1D15719D10B, Values of capacitors connected V3, V2, V1, VC, MV1 and MV2 are recommend inverse number of BIAS ratio.
Refer to Fig 6-24 and below setting example.
And C7 and C6 capacitances are recommend to stabilize bias voltage level.

Example) in case of 1/11 Bias

Each Bias voltage ratio is;
V3 : V2 : V1 : VC : MV1 : MV2 = 11/11 : 7.5/11 : 6.5/11 : 5.5/11 : 4.5/11 : 3.5/11
Each voltage difference ratio is;
V3-V2 : V2-V1 : V1-VC : VC-MV1 : MV1-MV2 : MV2-VSS
= 3.5/11 : 1/11 : 1/11 : 1/11 : /11 : 3.5/11
Each Capacitance value is;
V3-V2 : V2-V1 : V1-VC : VC-MV1 : MV1-MV2 : MV2-VSS
= 1 : 3.5 : 3.5 : 3.5 : 3.5 : 1
Actual value example;
C4=0.68µF, C5=2.2µF, C6=4.7µF, C7=6.8µF

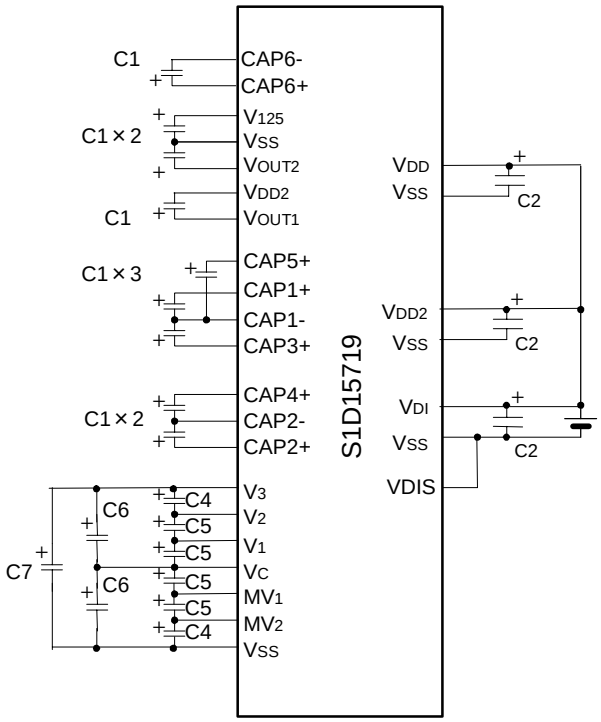


Fig. 6-24

6.8.2 When using S1D15719D11B000/ S1D15719D12B000

6.8.2.1When using every built-in power supply

An example of x6 boosting

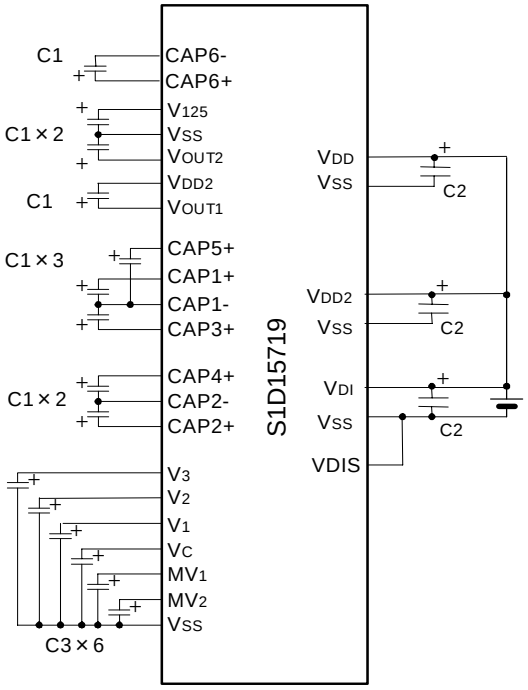


Fig 6-25

6.8.2.2When using 2nd booster circuit, V3 voltage regulator circuit and LCD-voltage generating circuit(1st booster circuit is turned off)

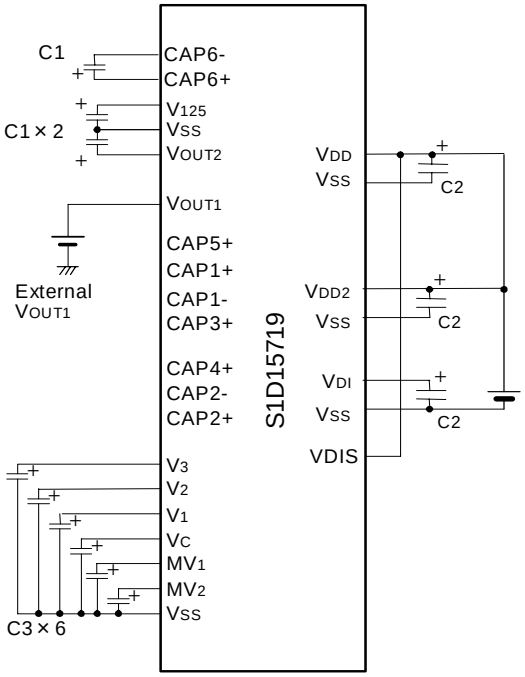


Fig 6-26

6.8.2.3 When using the 1st booster circuit, V3 voltage regulating circuit and LCD-voltage generating circuit (2nd booster circuit is turned off)

An example of x5 boosting, VDD=VDD2=VDI (External input)

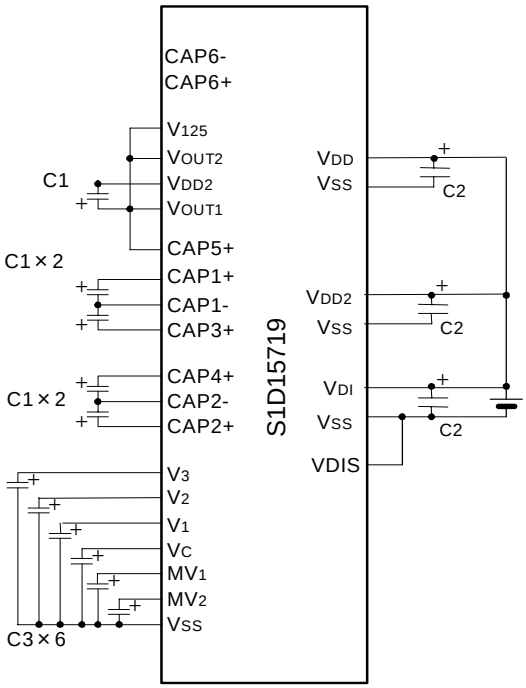


Fig 6-27

An example of x3 boosting, VDD=VDD2, built-in VDI Circuit used.

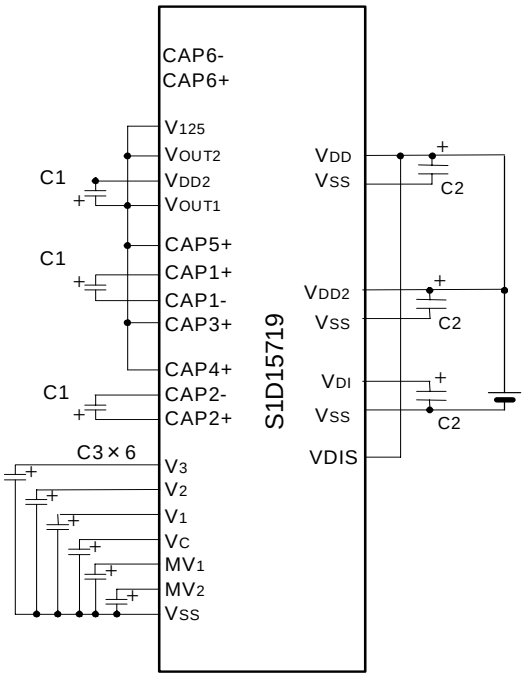


Fig 6-28

6.8.2.4 When using V3 voltage regulating circuit and LCD-voltage generationg circuit(1st and 2nd booster circuits are turned off)

An example of using V_{DD}=V_{DD2}, V_{DI} circuit.

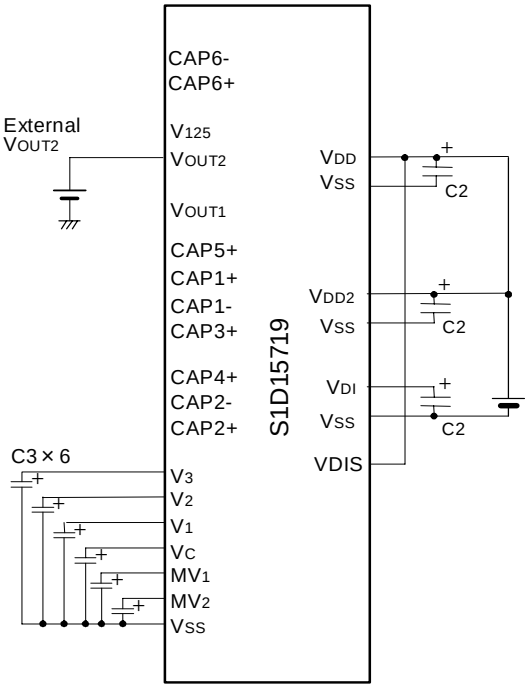


Fig 6-29

6.8.2.5 When using LCD voltage generating circuit(1st and 2nd booster circuits and V3 voltage regulating circuit are turned off)

An example of using V_{DD}=V_{DD2}, V_{DI} circuit.

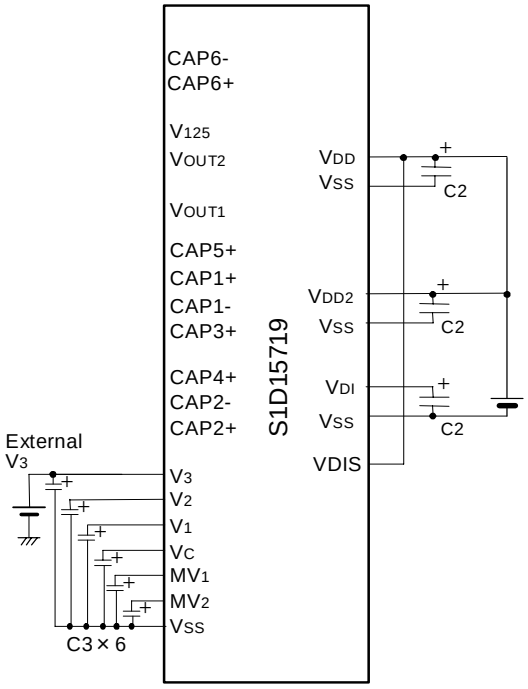


Fig. 6-30

6.8.2.6 All internal power supplies are turned off (All LCD voltages are external supplied)

An example of V_{DD}=V_{DD2}, built-inV_{DI} used

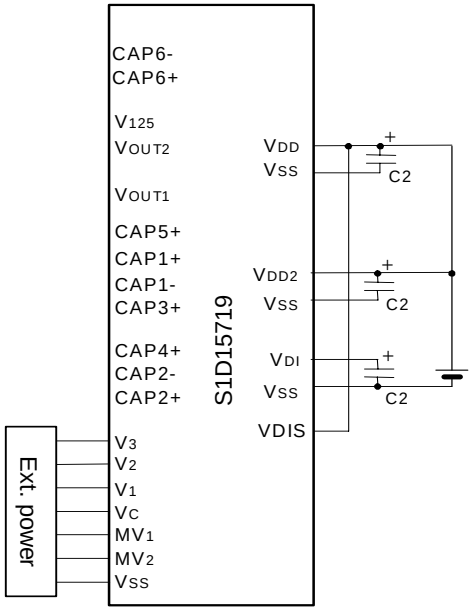
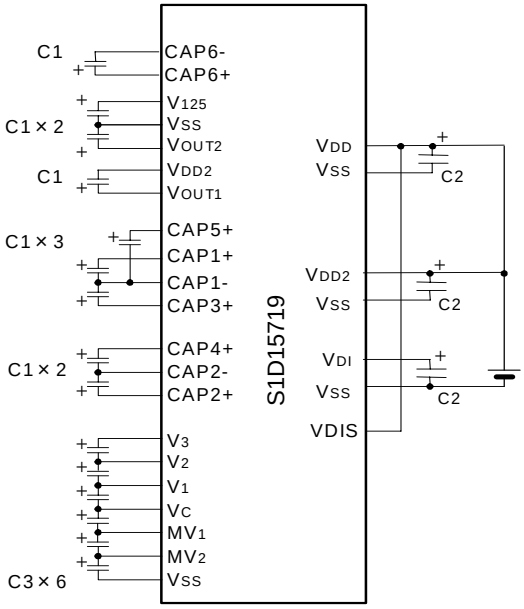


Fig. 6-31

6.8.2.7 Anoter example of using C3(All internal power supplies are used, x6 boosting)

V_{DD}=V_{DD2}, built-in V_{DI} used



*: It is applicable to 6.8.2.1 to 6.8.2.5 connection. Refer to 6.8.1 about capacitance value.

Fig. 6-32

6.8.3 Reference values for capacitor setup

The optimum value of C1, C2 and C3 shown in the examples of peripheral circuits depends on the size of liquid crystal panel to be driven. When determining the value, display a pattern with large load and then find the value where the LCD voltage becomes stable referencing Table 6.14.

Table 6.14

Item	Descriptions	Reference setting value [µF]
C1	Capacity for step-up circuits	1.0 to 4.7
C2	Capacity for supply voltage regulation	1.0 to 4.7
C3	Capacity for LCD voltage stabilization (smoothing)	0.47 to 4.7
C4	Capacity for LCD voltage stabilization (smoothing)	0.68 to 1.0
C5	Capacity for LCD voltage stabilization (smoothing)	2.2
C6	Capacity for LCD voltage stabilization (smoothing)	4.7
C7	Capacity for LCD voltage stabilization (smoothing)	6.8

*:Non Polarity capacitance can be applicable.

When size of a display panel is large and desired display quality is unavailable by adjusting values of above C1 to C7, turn off the built-in power supply circuit and then supply the LCD voltage externally referencing 6.7.1.6 to 6.7.2.6.

6.8.4 Precautions of V_{DD2} power supply circuits

This IC discharges the capacitor connected to outside of the IC by Discharge ON command or $\overline{RES}$ pin = V_{SS}. At this time, V_{OUT} is discharged to V_{DD2} and V_3 - MV_2 to V_{SS}.
To prevent the V_{DD2} potential from exceeding the absolute maximum rating due to the charge flowing in from the V_{OUT1}, V_{OUT2} power, if necessary, connect the zener diode between V_{DD2} and V_{SS} upon sufficient evaluation.

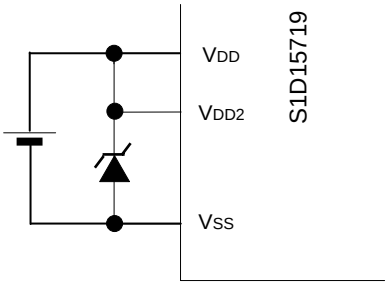


Fig.6.19 Example based on the assumption V_{DD} = V_{DD2}

6.9 Precautions on using COG

When COG is installed, resistance component due to ITO wiring appears across IC and external connection parts (capacitors and resisters) as well as across the power supply. This component could degrade display quality of liquid crystal or cause malfunctioning of IC. Whenever design a module, you must take into consideration of the following three points and, after developing the module, you should verify its function under actual operating conditions.

(1) Wiring resistance of pins in step-up system

The step-up circuits of this IC employ transistors with very low ON resistance for switching. When COG is installed, wiring resistance of ITO is applied in series to the switching transistor, resulting in governing the step-up capability. Thus, care must be exercised in wiring to booster capacitors (employing thicker ITO wires, for instance, may be considered).

(2) Wiring resistance of power terminal

Momentary voltage drop can occur on the supply voltage synchronizing with generation of momentary current at, for instance, switching of the display clock. In this case, if resistance of ITO wiring on the power terminal is high, supply voltage in IC can be significantly fluctuated, resulting in malfunctioning. In order to supply stable power to IC, wiring impedance of the power supply line must be kept as low as possible.

(3) Preparation of module samples with varied sheet resistances

It is recommended to test the samples with varied ITO wiring resistances and uses the one with sheet resistance of a larger operating margin.

6.10 Temperature sensor circuit

This IC contains an analog temperature sensor circuit that changes with the temperature gradient of -4.70 mV/°C(typ.) And the latter outputs digital values corresponding to the changing analog voltages through the data bus. This circuit receives from MPU the electronic volume register value corresponding the thermal sensor's output value to control the LCD voltage V_3. Appropriate shading has been enabled in wide temperature gradient area thanks to this arrangement.

6.10.1 Analog voltage output element

Responding to the thermal sensor ON command, SVD2 pin outputs analog voltage that changes according to the temperature. In order to ensure high-accuracy control of LCD voltage, the system you develop must be capable of absorbing fluctuations in the output voltage. Above can be done by, for instance, sampling the output voltage values under a specific temperature level and then feeding them back to MPU so that the voltage to be used as the reference may be stored on it.

6.10.2 Digital converter element

This element samples analog voltage V_{SVD2} and output 7bit digital value by Temperature sensor output read command.

In case using serial interface, it is possible to read the data. After input Temerature sensor output read, change A0=HIGH and input clock to SCL pin, and read the digital value from SI pin. Between Temperature sensor output read command and Output data read operation, don't change CS to HIGH(keep LOW). Refer to timing chart Fig. 6.1.

When correct V_3 voltage by the digital value, It is recommend to have hysteresis characteristics to temperature in order not to change V3 voltage continuasly at switching temperature and not to cause flicker.

6.10.3 Precautions

(1) Noise influence

The temperature sensor circuit operates in the SV_{22} voltage generated in the regulator operating in the V_{DI} system which is IC's logic operating voltage. The circuits of the SV_{22} voltage are configured so that steady variations in the V_{DI} power supply system do not have an effect on them. However, in cases such as logic is operated at high speed for writing to RAM, for example, power supply noise may be caused in the V_{DI} voltage and the SV_{22} voltage may also be influenced similarly.

To perform temperature detection accurately, be sure to stop access from the MPU when capturing the temperature sensor output and comply with operating conditions specified at the AC timing.

(2) Influence of mounting

The temperature sensor circuit output SV_{D2} is specified using the output voltage value for the IC's board potential V_{SS}. When measuring the SV_{D2} potential in the actual system, attention should be paid to the relationship between the IC's board potential and the system ground's potential.

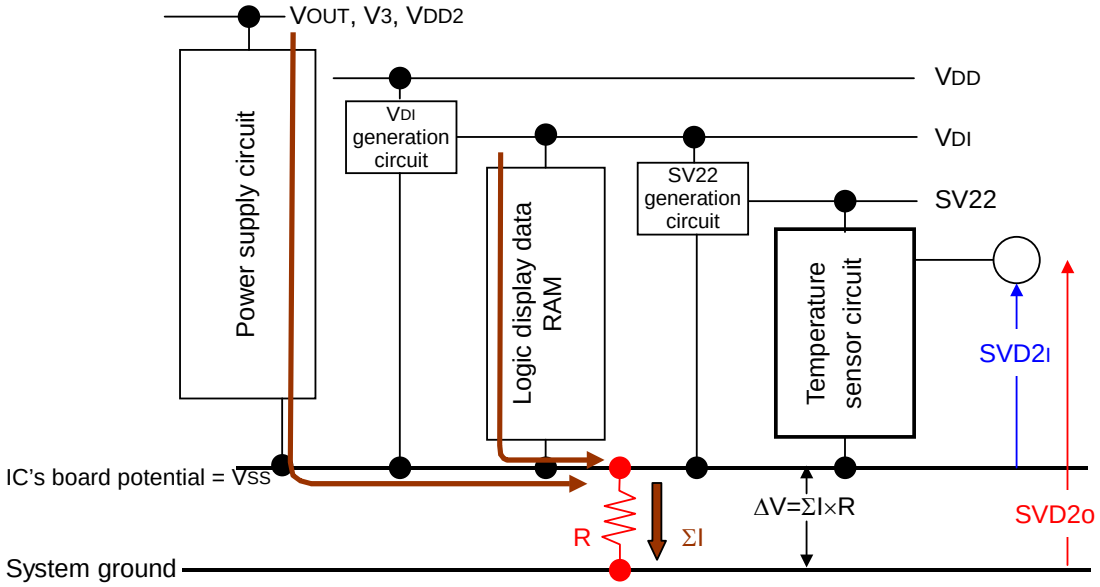


Fig.6.34 Influence of Resistance R between System Ground and V_{SS}

If there is a resistance component R between the system ground and IC's V_{SS} pin, the IC's board potential V_{SS} viewed from the system ground experiences fall of potential of

$$\Delta V = \sum I \times R$$ (where Σ is the total amount of the current consumed by IC)

Therefore, the temperature sensor output ($SVD2_O$ in Fig.6.34) viewed from the system ground is also influenced similarly. That is, ΔV has an impact on the temperature sensor output ($SVD2_I$ in Fig.6.34) viewed from the IC's V_{SS} defined in the specifications.

To eliminate the impact of ΔV as much as possible, adopt the design and usage with consideration given to three points below.

- Decrease the resistance value between the system ground and IC's V_{SS} pin as low as possible, including ITO resistance when mounting COG.
- Measure the temperature sensor output voltage with the current consumed by IC reduced as much as possible by placing the IC in the power-saving mode.
- Minimize the impact caused by the IC's external circuits by leaving the system to be used under certain temperature and allowing the system to store the SV_{D2} voltage measured while operating the system as the reference voltage.
- The digital value is not affected by the resistance R.

6.11 Reset circuit

When the $\overline{RES}$ input becomes LOW, this LSI is set to the initialized state.
The following shows the initially set state:

1. Display : OFF
2. Display : normal mode
3. Display all lighting : OFF
4. Common output states : normal
5. Display start line: Set to 1st line
6. Page address: Set to 0 page
7. Column address: Set to 0 address
8. Display data input direction: Column direction
9. Column address direction : forward
10. n-line a.c. reverse drive: OFF (reverse drive for each frame)
11. n-line reverse drive register: (D5, D4, D3, D2, D1, D0)=(0, 0, 0, 0, 0, 0)
12. Display mode: All ON during dummy selection period; 4 gray-scale display
13. Gray-scale pattern register: (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 1, 0, 1, 0, 0, 1, 0)
14. Number of display lines setting register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0, 0) (132 lines)
    Start spot (block) register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0) (COM0)
15. Read modify write: OFF
16. Built-in oscillation circuit: stop
17. Oscillation frequency register: (D3, D2, D1, D0) = (0, **1**, 0, 0)
18. Power control register: (D3, D2, D1, D0) = (0, 0, 0, 0)
19. Step-up clock frequency: (D1, D0) = (0, 0)
20. V_3 voltage adjusting register: (D2, D1, D0) = (0, 0, 0)
21. LCD bias set register: (D1, D0) = (0, 0)
22. Electronic volume resister: (D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0)
23. Discharge: ON (only for when $\overline{RES}$ = LOW)
24. Power save: OFF
25. Temperature gradient register: (D2, D1, D0) = (0, 0, 0) (-0.06% / °C)
26. Register data in the serial interface: Clear
27. Thermal sensor: OFF
28. MLS drive selecting register: (D4, D3)=(0, 1) (n-line inversion, frame inversion overlap OFF, and non-dispersion drive)

When power is turned on, initialization by the $\overline{RES}$ pin is necessary. After initialization by the $\overline{RES}$ pin, each input pin must be controlled correctly.
Furthermore, when control signals from the MPU have a high impedance, the excessive current may flow to the IC.
This IC sets discharges V_{OUT1} and V_{OUT2} to V_{DD2}, and liquid crystal drive voltage (V_3, V_2, V_1, V_C, MV_1, and MV_2) to V_{SS} by setting the $\overline{RES}$ pin to LOW level or execution of discharge ON command. When using the external power supply for liquid crystal drive, do not supply external power $\overline{RES}$ during pin = LOW or execution of discharge ON command to prevent external power supply from shorting with V_{DD2} or V_{SS}. At this time, in some power supply peripheral circuitry, the charge flowing in from the V_{OUT1} and V_{OUT2} power increases the power voltage shorted with the V_{DD2} and V_{DD2}. Care should be taken not to allow these power supplies to exceed the absolute maximum ratings.

7. COMMAND

The S1D15719 Series identifies data bus signals by a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$). Interpretation and execution of the command are executed by the internal timing alone which is independent of the external clock. This allows high-speed processing.
The 80 series MPU interface allows the command to be started by entering the low pulse in the $\overline{RD}$ pin during reading and by entering the low pulse in the $\overline{WR}$ pin during writing.
The 68 series MPU interface allows a read state to occur by entering HIGH in the R/$\overline{W}$ pin, and permits a write state to occur by entering LOW. It also allows the command to be started by entering the high pulse in the pin E. (For timing, see the description of "10. Timing characteristics").

Accordingly, the 68 series MPU interface is different from 80 series MPU interface in that $\overline{RD}$(E) is "1(H)" in the case of display data/read shown in the Command Description and Command Table. The following describes the commands, based on the example of the 80 series MPU interface:
When the serial interface is selected, enter data sequentially starting from D7.

7.1 Command Description

(1) Display ON/OFF
This command is used to turn ON or OFF the display. Display of liquid crystal is performed synchronized with the built-in oscillation circuit or the externally entered display clock. Be sure not to stop the internal oscillation circuit or the external operation clock as long as the display is turned ON.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Output level
0	1	0	1	0	1	0	1	1	1	0	Display OFF
										1	Display ON

After reset is done from the $\overline{RES}$, the display is set to OFF.

(2) Display Normal/Reverse
This command allows the display ON/OFF state to be reversed, without having to rewrite the contents of the display data RAM. In this case, contents of the display data RAM are maintained.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data = HIGH LCD ON Voltage (normal)
										1	RAM data = LOW LCD ON Voltage (reverse)

After reset is done from the $\overline{RES}$, the display is set to REVERSE.

(3) Display All Lighting ON/OFF
This command forces all the displays to be turned on independently of the contents of the display data RAM. In this case, the contents of the display data RAM are maintained. Fully white display can also be made by a combination of the Display Reverse command.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display status
										1	Display all lighting

After reset is done from the $\overline{RES}$, the display all lighting is set to OFF.

(4) Common Output Status Select

This command allows the scanning direction of the COM output pin to be selected. For details, see the description of "6.5.2 COM Drivers" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	1	0	0	Normal	COM0 → COM131
										1	Reverse	COM131 → COM0

After reset is done from $\overline{RES}$ pin, the common output status is set to normal.

(5) Display Start Line Set

The parameter following this command specifies the display start line address of the display data RAM shown in Fig.6.5 and 6.6.

The display area is indicated in the direction where line address numbers are incremented, starting from the specified line address. If a dynamic change of the line address is made by this command, smooth scrolling in the longitudinal direction and page breaking are enabled. For details, see the description of "6.2.4 Line address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	0	1	0	Mode setting
1	1	0	*	P6	P5	P4	P3	P2	P1	P0	Register setting

*: denote invalid bits

Display Start Line Set command parameter

(i) When the display model is a 4 gray-scale mode:

The one-byte parameter is used to specify the address.

P6	P5	P4	P3	P2	P1	P0	Line address
*	0	0	0	0	0	0	00H (4 × 0)
*	0	0	0	0	0	1	01H (4 × 1)
			↓				↓
*	0	1	1	1	1	1	7CH (4 × 31)
*	1	0	0	0	0	0	80H (4 × 32)

After reset is done from RES pin, the line address is set to 00H.

*: Denotes invalid bits

(ii) When the display mode is binary

P6	P5	P4	P3	P2	P1	P0	Line address
0	0	0	0	0	0	0	00H (4 × 0)
0	0	0	0	0	0	1	01H (4 × 1)
			↓				↓
0	0	1	1	1	1	1	1FH (4 × 31)
0	1	0	0	0	0	0	20H (4 × 32)
			↓				↓
1	0	0	0	0	0	0	40H (4 × 64)
1	0	0	0	0	0	1	41H (4 × 65)

After reset is done from RES pin, the line address is set to 00H

Register setting at 42H or higher is not allowed.

Sequence of Display Start Line Set

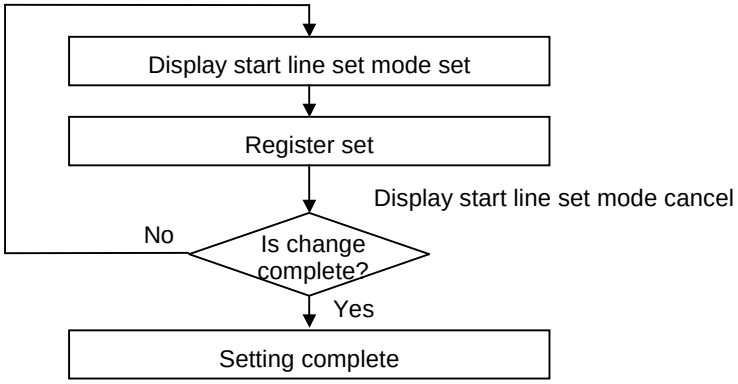


Fig.7.1 Sequence of Display Start Line Set

(6) Page Address Set

This command specifies the page address corresponding to row address when MPU access to the display data RAM shown in Fig.6.5 and 6.6. For details, see the description of "6.2.3 Page address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	1	1	0	0	0	1	Mode setting
1	1	0	*	*	P5	P4	P3	P2	P1	P0	Register setting

*: denote invalid bits.

P5	P4	P3	P2	P1	P0	Page address
0	0	0	0	0	0	00H (Page 0)
0	0	0	0	0	1	01H (Page 1)
			↓			↓
0	1	1	1	1	1	1FH (Page 31)
1	0	0	0	0	0	20H (Page 32)

After reset is done from $\overline{RES}$ pin, the page address set to 00H.
Register setting at 21H or higher is not allowed.

(7) Column Address Set

This command sets the display data RAM column address given in Fig.6.5 and 6.6. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	0	1	0	0	1	1	Mode setting
1	1	0	P7	P6	P5	P4	P3	P2	P1	P0	Register setting

Relationship between the register value with the set register and column address is shown below.

P7	P6	P5	P4	P3	P2	P1	P0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				↓				↓
1	0	1	1	0	0	1	0	B2H
1	0	1	1	0	0	1	1	B3H

After reset is done from $\overline{RES}$ pin, the column address is set to column 00H.
Register setting at B4H or higher is not allowed.

(8) Display Data Write

This command allows the 8-bit data to be written to the address specified by the display data RAM. After writing, column address or page address is automatically incremented +1 by the Display Data Input Direction Select command.
This enables the MPU to write the display data continuously.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	1
1	1	0	Write Data							

(9) Display Data Read

This command allows the 8-bit data to be read from the address specified by the display data RAM. After reading, column address or page address is automatically incremented +1 by the Display Data Input Direction select command. This enables the MPU to read multiple word data continuously.
It should be noted that one dummy reading is essential immediately after the column address or page address has been set. For details, see the description of "6.1.5 Access to display data RAM and internal register" in the Function Description. When the serial interface is used, display data cannot be read.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	0
1	0	1	Read Data							

(10) Display Data Input Direction Select

This command sets the direction where the display RAM address number is automatically incremented. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Direction
0	1	0	1	0	0	0	0	1	0	0	Column
										1	Page

$\overline{RES}$ After resetting by the $\overline{RES}$ pin, the direction is set to column.

(11) Column Address Set Direction

This command can reverse the relationship between the display RAM data column address and segment driver output shown in Fig.6.5 and 6.6. So you can reverse the sequence of segment driver output pins using this command. When the display data is written or read, the column address is incremented by (+1) according to the column address given in Fig.6.4 and 6.5. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

$\overline{RES}$ After resetting by the $\overline{RES}$ pin, the direction is set to normal rotation of setting the column address.

(12) n-line Inversion Drive Register Set

This command sets the liquid crystal alternating drive reverse line count in the register to start line reverse driving operation. The line count to be set is 4 to 132 (33 steps for each 4 lines). For details, see the description of "6.4 Display timing generation circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	1	0	1	1	0	Mode setting
1	1	0	*	0	P5	P4	P3	P2	P1	P0	Register setting

*: denote invalid bits.

Relationship between the register value with set register and the number of inverted lines is shown below.

P5	P4	P3	P2	P1	P0	Reverse line count
0	0	0	0	0	0	4 (1 × 4)
0	0	0	0	0	1	8 (2 × 4)
			↓			↓
0	1	1	1	1	1	128 (32 × 4)
1	0	0	0	0	0	132 (33 × 4)

* $\overline{RES}$ After resetting by the $\overline{RES}$ pin, the number of inverted lines is set to 4. Register setting at 21H or higher is not allowed.

(13) n-line Inversion Drive ON/OFF

This command provides ON/OFF control of n-line inverting drive.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	n-line Inversion Drive
0	1	0	1	1	1	0	0	1	0	0	OFF
										1	ON

* $\overline{RES}$ After resetting by the $\overline{RES}$ pin, the n line inverted drive is set to OFF.

(14) Display Mode Set

This command allows selection between the 4-gray scale display and the binary display and setting of the SEG output state during dummy selection period. Structure of display data RAM in the 4-gray scale display differs from that in the binary display. For more information, see 6.2 and Display Data RAM in FUNCTIONAL DESCRIPTION.

When the dummy selection period and display all lighting ON is selected, the same level as in display all lighting ON is output from all SEG during dummy selection. When the dummy selection period and display all lighting OFF is selected, the same level as in display all lighting OFF is output. Determine after adjusting to the display pattern of the liquid crystal panel and comparing the display quality.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	0	1	1	0	Mode setting
1	1	0	*	*	*	*	*	*	P1	P0	Register setting

*: denote invalid bias.

Relationship between the register value with the set register and display state is shown below.

P1	P0	Display state
0		Dummy selection period Display all lighting ON
1		Dummy selection period Display all lighting OFF
	0	4-gray scale display
	1	Binary display

* RES After resetting by the pin, the setting is made to dummy selection period and display all lighting ON and 4-gray scale.

(15) Gray-scale Pattern Set
This command sets the level of gray-scale.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	1	1	0	0	1	Mode setting
1	1	0	P7	P6	P5	P4	P3	P2	P1	P0	Register setting

*: denote invalid bias.

(P7, P6, P5, P4): Used to select density of gray-scale bits (1, 0)
(P.3, P2, P1, P0): Used to select density of gray-scale bits (0, 1)
One of the 9 states of intermediate gray-scales is respectively selectable as the gray-scale pattern. Following shows the register value and gray-scale density set with the register set command as well as their settable range.

Density of intermediate gray-scale	Gray-scale bits (1,0) P7	P6	P5	P4	Gray-scale bits (0,1) P3	P2	P1	P0	Settable ranges (1,0)	(0,1)
Levels 1 (Light)	Not settable				0	0	0	1	—	▲
	Not settable				0	0	1	0	▲	▲
	Not settable				0	0	1	1	▲	▲
	0	1	0	0	0	1	0	0	▲	▲
↓	0	1	0	1	0	1	0	1	▲	▲
	0	1	1	0	0	1	1	0	▲	▲
	0	1	1	1	0	1	1	1	▲	▲
	1	0	0	0	1	0	0	0	▲	▲
Level 9 (Dark)	1	0	0	1	Not settable				▼	—

Care must be used in the setting so that that the gray-scale bits (1, 0) and (0, 1) may not be inverted.
After reset is done from $\overline{RES}$ pin the gray-scale bits (1, 0) are set to (0, 1, 0, 1) and (0, 1) are set to (0, 0, 0, 1).
Gray scale bit (1, 0) at 3h or lower and Ah or higher, and gray scale bit (0, 1) at 9H or higher are not allowed.

(16) Number of Display Lines Set

Liquid crystal drive at a lower power consumption is ensured by using this command to change the duty. Use of this command also allows display at a desired position on the panel (continuous COM pins on a 4-line basis). This command is used with a pair of the duty set parameter and start point (block) parameter, so be sure to set both parameters so that one of them will immediately follow the other.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	1	0	1	1	0	1	Mode setting
1	1	0	*	*	P15	P14	P13	P12	P11	P10	Number of Display Line Register setting
1	1	0	*	*	P25	P24	P23	P22	P21	P20	Start point set Register setting

*: denote invalid bits.

Number of Display Lines Register Set

You can set number of display lines in the range of 4 to 132 line in multiple of 4 lines. After changing the number of display lines, be sure to adjust the LCD voltage to ensure an optimum display contrast.
Following shows the relation between the register values specified with the register set command and number of display lines.

P15	P14	P13	P12	P11	P10	Number of display lines
0	0	0	0	0	0	4
0	0	0	0	0	1	8
			↓			↓
0	1	1	1	1	1	128
1	0	0	0	0	0	132

After reset is done from $\overline{RES}$ pin, the number is set to 132 lines.
Register setting at 21H or higher is not allowed.

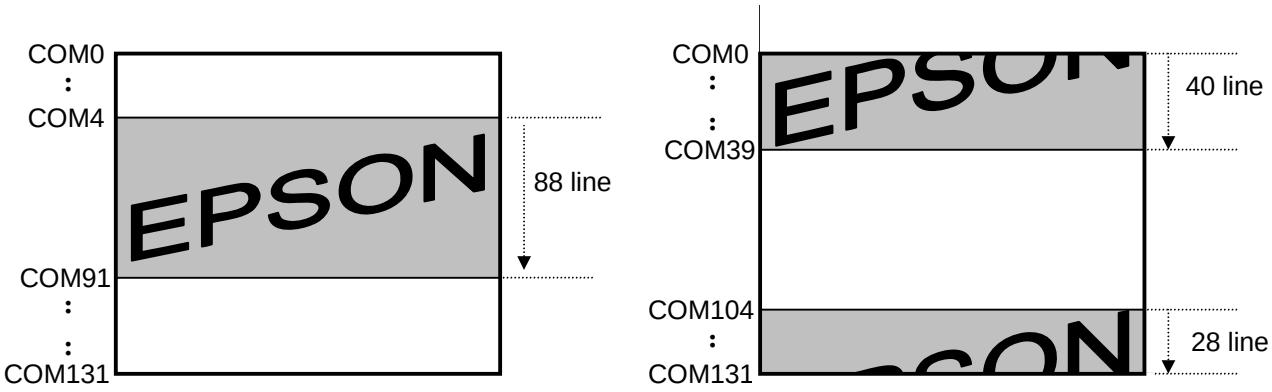
Start Point (Block) Register Set

You can specify one of the 33 starting point blocks by setting 6-bit data on the start point (block) register using this parameter. When you want to scroll the display, use (6) Display Start Line Set Command rather than this command.

P25	P24	P23	P22	P21	P20	Start point set
0	0	0	0	0	0	0 (COM0 to 3)
0	0	0	0	0	1	1 (COM4 to 7)
0	0	0	0	1	0	2 (COM8 to 11)
			↓			↓
0	1	1	1	1	1	31 (COM124 to 127)
1	0	0	0	0	0	32 (COM128 to 131)

After reset is done from $\overline{RES}$ pin, 0 (COM0 to 3) will be selected.
Register setting at 21H or higher is not allowed.

[Example of settings done by use of Number of Display Lines Set Command]
Setting example 1: When 88 display lines and start point 1 (COM4 to 7) are set, 88 lines worth data are displayed starting from COM4.
Setting example 2: When 68 display lines and start point 26 (COM104 to 107) are set, 68 lines worth data are displayed starting COM104. After COM131 has been reached, COM0 is then selected.



Setting examples 1 Setting examples 2

Fig.7.2 Correspondence between COM Output and Number of Display Lines

Relation between the number of display lines "ι" and display duty "duty" (duration of a single operation in the sequential drive of liquid crystal lines compared against the frame cycle) is described by the following equation.

$$duty = 1/(l + 4) \qquad \text{(Equation 7.1)}$$

Example 1: When 132 are selected for the number of display lines, display duty becomes 1/136.
Example 2: When 88 are selected for the number of display lines, display duty becomes 1/92.

Care is required if COM pin is not used commonly between the master and slave (such as when 180 lines are specified for SEG and 80 lines +80 lines for COM) when multiple chips are operated in the master/slave arrangement. In this case, if there is a difference in the number of display lines driven by the master and slave, a different density will result in the display area driven the master chip and that driven by the slave chip. Thus, you must make sure to specify the same number of display lines for both the master and the slave chips.

(17) Read Modify Write

This command is paired with end command for use. If this command is entered, the column address is not changed by the Display Data Read command. It can be incremented +1 by the Display Data Read command alone. This states retained until the End command is input. If the End command is input, the column address goes back to the address when the Read Modify Write command is input. This function reduces the MPU loads when changing the data repeated in the specific display area such as blinking cursor.

	$\overline{E}$	R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	0	0	0	0

A command other than display data Read/Write command can be used in the Read Modify Write mode. However, you cannot use the page address set command or the column address set command.

Sequence for cursor display

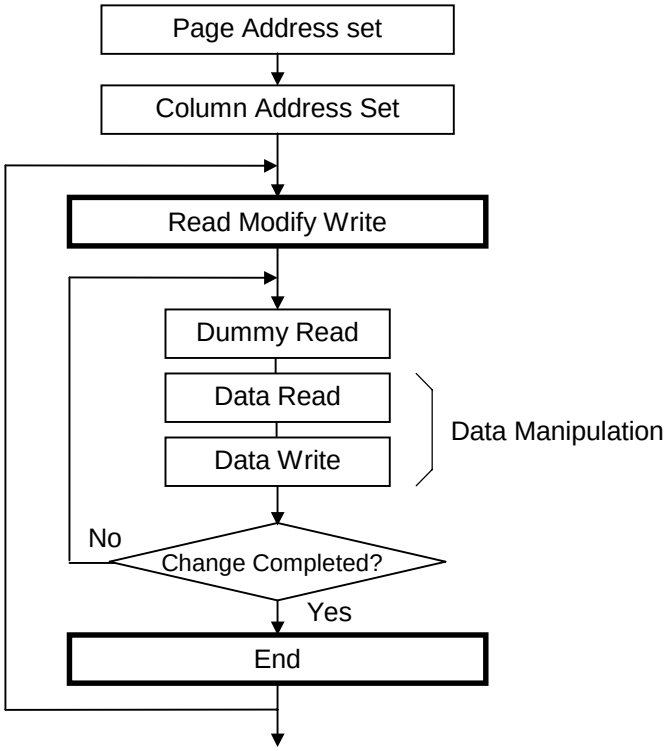


Fig.7.3 Sequence for cursor display

(18) End

This command releases the read modify write mode and gets page address and column address back to the initial address of the mode.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

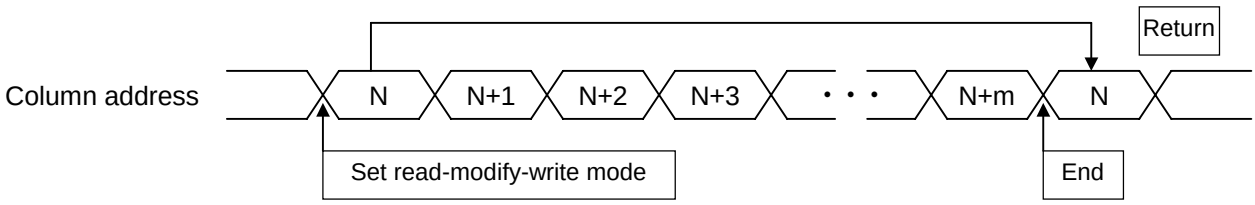


Fig.7.4 Addressing at the time of a lead modify light

(19) Built-in Oscillator Circuit ON/OFF

This command starts the built-in oscillator circuit operation. It is enabled only in the master operation mode (M/S=HIGH) when built-in oscillator circuit is valid (CLS=HIGH).

When the built-in power supply is used, the Oscillator Circuit ON command must be executed before the Power Control Set command. (See the description of "(21) power control command"). If the built-in oscillator circuit is turned off when the built-in power supply is used, display failure may occur.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Built-in oscillator circuit
0	1	0	1	0	1	0	1	0	1	0	OFF
										1	ON

(20) Operation Clock Frequency Select

This command is used to specify the dividing ratio of the internal operation clock f_{CL} to the built-in oscillation frequency fuss. This command is enabled only when the built-in oscillation circuit is turned on. When the built-in oscillation circuit is turned on, the external clock focal entered to CL pin is used as the internal operation clock.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	0	1	1	1	1	1	Mode set
1	1	0	*	*	*	*	P3	P2	P1	P0	Register set

*: Denotes invalid bits.

Following shows the relation between the dividing ratio and the register value set with the register set command.

Following also shows the relation between the internal operation clock f_{CL} and the display operation clock f_{DCLK}.

P3	P2	P1	P0	Internal operation clock f_{CL} Dividing ratios	Internal operation clock f_{CL} Frequency [kHz]	Display operation clock f_{DCLK} Dividing ratios	Display operation clock f_{DCLK} Frequency [kHz]
0	0	0	0	fosc/4	1224	f_{CL}/45	27.2
0	0	0	1	fosc/5	980		21.8
0	0	1	0	fosc/6	816		18.1
0	0	1	1	fosc/7	700		15.5
0	1	0	0	fosc/8	612		13.6
0	1	0	1	fosc/10	490		10.9
0	1	1	0	fosc/12	408		9.1
0	1	1	1	fosc/14	350		7.8
1	0	0	0	fosc/16	306		6.8
1	0	0	1	fosc/20	245		5.4
1	0	1	0	fosc/24	204		4.5
1	0	1	1	fosc/28	175		3.9
1	1	0	0	fosc/32	153		3.4
1	1	0	1	fosc/40	122		2.7
1	1	1	0	fosc/48	102		2.3
1	1	1	1	fosc/56	87		1.9

After reset is done from RES pin, (0, 1, 0, 0) are set.
Typical value at 25°C.

[Definition of Symbols]
f_{OSC}: Oscillation frequency of the built-in oscillation circuit.
f_{CL}: Internal operation clock. It is the basic clock used by the synchronous circuit of IC. This clock is obtained by dividing f_{OSC}.
f_{OCL}: It is the external clock provided from CL pin when the built-in oscillation circuit is turned off. In this case, internal operation clock = external operation clock ($f_{CL} = f_{OCL}$).
f_{DCLK}: Display operation clock. It is used to specify a single duration in the sequential drive of liquid crystal. It constantly meets the relation of $f_{CL}/45$ independent of the value of the operation clock frequency select command. The relationship will not change even when the external clock is used.

Display duty expressed as shown below when the number of display lines is *l*.

$$\text{duty} = 1/(l+4) \quad \text{(see Equation 7.1)}$$

Thus, the frame frequency (frequency for rewriting the display-screen) for LCD is described as shown below.

$$f_{FR} = \frac{f_{DCLK}}{1/\text{duty}} = \frac{f_{DCLK}}{l+4} = \frac{f_{CL}/45}{l+4} \qquad \text{(Equation 7.2)}$$

Following shows the frame frequencies used in typical number of display lines when the n line inversion drive is turned off.

P3	P2	P1	P0	f_{CL} [kHz]	f_{DCLK} [kHz]	Frame frequencies f_{FR} [Hz] 132 lines	96 lines	64 lines	32 lines
0	0	0	0	1224	27.2	200	272	400	756
0	0	0	1	980	21.8	160	218	320	604
0	0	1	0	816	18.1	133	181	267	504
0	0	1	1	700	15.5	114	155	229	432
0	1	0	0	612	13.6	100	136	200	378
0	1	0	1	490	10.9	80	109	160	302
0	1	1	0	408	9.1	67	91	133	252
0	1	1	1	350	7.8	57	78	114	216
1	0	0	0	306	6.8	50	68	100	189
1	0	0	1	245	5.4	40	54	80	151
1	0	1	0	204	4.5	33	45	67	126
1	0	1	1	175	3.9	29	39	57	108
1	1	0	0	153	3.4	25	34	50	94
1	1	0	1	122	2.7	20	27	40	76
1	1	1	0	102	2.3	17	23	33	63
1	1	1	1	87	1.9	14	19	29	54

(21) Power Control Set

This command sets the built-in power supply circuit function. For details, see the description of "6.6 Power supply circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	0	1	0	0	1	0	1	Mode set
1	1	0	*	*	*	*	P3	P2	P1	P0	Register set

*: Denote invalid bits.

Following shows the register values set with the register set command and the functions.

P3	P2	P1	P0	Selected state
0				2nd booster circuits: OFF
1				2nd booster circuit: ON
	0			1st booster circuits: OFF
	1			1st booster circuits: ON
		0		V_3 voltage regulating circuit:OFF
		1		V3 voltage regulating circuit: ON
			0	LCD voltage generation circuit: OFF
			1	LCD voltage generation circuit: ON

After reset is done from RES pin, (0, 0, 0, 0) <all-internal power supplies OFF> are set.

An internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside.
If the built-in oscillator circuit is used, execute the built-in oscillator circuit ON command before the power control set command. If an external oscillator circuit is used, operate the external oscillator circuit before the power control set command.
If the internal clock is cut off during the operation of the built-in power supply circuit, display failure may occur. To avoid this, do not cut it off.

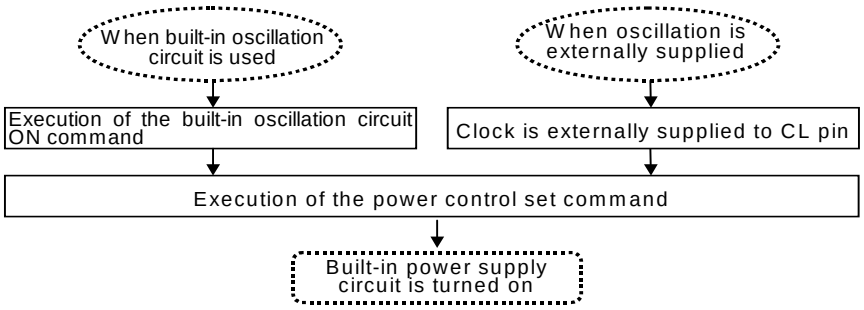


Fig.7.5 Clock Input and Execution Sequence of Power Control Set Command

(22) Step-up Clock Frequency Select
This command is used to choose one of the four step-up frequencies for the 1st and 2nd booster circuits.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	0	1	0	1	0	1	Mode set
1	1	0	*	*	*	*	*	*	P1	P0	Register set

*: Denotes invalid bits

Following shows the relation between the register values selected with the register set command and the step-up frequency when the built-in oscillation circuit or external clock f_{OCL} is used.

P1	P0	Step-up clock frequency	
		When built-in oscillation circuit is used [kHz]	When external clock is used
0	0	9.6	f_{OCL}/64
0	1	4.8	f_{OCL}/128
1	0	2.4	f_{OCL}/256
1	1	1.2	f_{OCL}/512

After reset is done from $\overline{RES}$ pin, (0, 0) are set.

(23) V_3 Voltage Regulation Circuit

The liquid crystal drive voltage range issued from the liquid crystal drive voltage regulating circuit is selected from 8 states by this command. V_3 voltage output ranges are Typ. values at 25°C.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	V_3 voltage output range
0	1	0	0	0	1	0	1	0	1	1	Command
1	1	0	*	*	*	*	*	P2	P1	P0	Register

*: denote invalid bits.

P2	P1	P0	V_3 voltage output range
0	0	0	10.49 to 17.35
0	0	1	10.97 to 18.21
0	1	0	11.49 to 19.11
0	1	1	12.06 to 20.06
1	0	0	12.70 to 21.08
1	0	1	13.40 to 22.17
1	1	0	14.19 to 23.59
1	1	1	15.08 to 24.98

After reset is done from $\overline{RES}$, (0, 0, 0) are set.

(24) LCD Bias Set

With this command, the bias ratio of voltage required for a liquid crystal drive is chosen.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Bias ratio
0	1	0	1	0	1	0	0	0	1	0	Command
1	1	0	*	*	*	*	*	*	P1	P0	Register set

*: denote invalid bits.

P1	P0	Bias ratio
0	0	1/11
0	1	1/10
1	0	1/9
1	1	1/8

After reset is done from $\overline{RES}$, (0, 0) are set.

(25) Electronic Volume

This command controls liquid crystal drive voltage V_3 issued from the built-in liquid crystal power supply voltage regulating circuit, and adjusts the liquid crystal display density. For details, see the description of "6.6.2 Voltage Regulating Circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	0	0	0	1	Command
1	1	0	*	P6	P5	P4	P3	P2	P1	P0	Register

*: denote invalid bits.

Electronic Volume Register Set

When a 7-bit data to the electronic volume register set by this command, liquid crystal drive voltage V_3 assumes one state out of voltage values in 128 states.

After this command is input, and the electronic volume register is set, the electronic volume mode is reset.

P6	P5	P4	P3	P2	P1	P0	V_3
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	
0	0	0	0	0	1	0	
			↓				↓
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	Larger

$\overline{RES}$ After resetting by the $\overline{RES}$ pin, it is set to (0, 0, 0, 0, 0, 0, 0).

(26) Discharge ON/OFF

This command is used to discharge the capacitors connected to the power supply circuits. This command becomes necessary when:

- Turning off the system power supply V_{DD}-V_{SS}
- Changing number of display lines

Refer to (4) When changing number of display lines and (5) Power supply OFF in the 7.3 instruction setting examples.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	1	0	1	0	1	0	Discharge OFF
										1	Discharge ON

$\overline{RES}$ Set to discharge ON during reset by the $\overline{RES}$ pin and set to discharge OFF after resetting.

This command short-circuits the output pins in the step-up system and V_{DD2} as well as respective LCD voltages and V_{SS} by use of the switching device. When V_{OUT1} or LCD voltages are externally supplied, be sure to turn them off before executing this command. Otherwise, damages due to overcurrent can result.

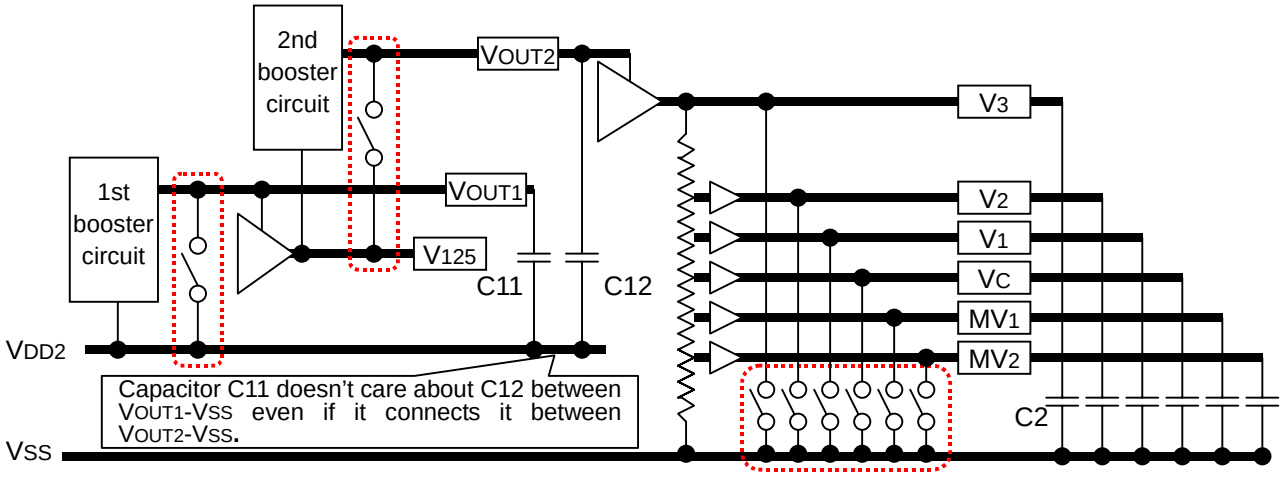


Fig.7.6 Positions of Switching Devices for Discharge

Capacitors C11 and C12 being connected to V_{OUT1} and V_{OUT2} are discharged to V_{DD2} potential by the switching devices provided across V_{OUT1}-V_{DD2} and V_{OUT2}-V_{125}. Capacitor C2 for voltage retention is discharged to V_{SS} potential by the switching device provided across the LCD voltages V_3 to MV_2 and V_{SS}.

(27) Power Saving

This command establishes the power save mode, thereby ensuring a substantial reduction of current consumption.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Power save mode
0	1	0	1	0	1	0	1	0	0	0	OFF
										1	ON

$\overline{RES}$ After resetting by the $\overline{RES}$ pin, it is set to power-saving OFF.

In the power save mode, display data and operation before power saving are maintained. Access to the display data RAM from the MPU is also possible. The current consumption is reduced to the value close to static current if all operations of the LCD display system are stopped and there is no access from the MPU.

The Power Save OFF command is used to cancel the Power Save mode and reset to the status prior to starting the Power Save mode.

If the built-in power supply is used, it is started following the execution of Power Save OFF command and the display is started with a certain delay until the output voltage is stabilized.

[Internal state while the power save mode is turned on]

(1) Built-in oscillation circuit is turned off
(2) Built-in power supply circuit is turned off
(3) Every LCD circuit is turned off (every SEG and COM outputs V_C level)
(4) The VDI generating circuit and the temperature sensor circuit operate.

If an external oscillator circuit is used, the built-in booster (amp) circuit operates even in the Power Save mode. To reduce the current consumption during power saving by turning off the built-in booster circuit:

(i) Turn off the external oscillator circuit, or
(ii) Turn off the built-in booster circuit by using the Power Control Set command.

IMPORTANT: Before issuing the Power Save OFF command, activate the external clock in Step (i) and activate the built-in booster circuit by using the Power Control Set command in Step (ii).

When the external power supply is used, it is recommend to stop the external power supply circuit function in the power save mode. For example, when each level of the liquid crystal drive voltage is given from the external resistive divider circuit, it is recommended to add a circuit to cut off the current flowing to the resistive divider circuit when power save function is started. The S1D15719 Series has a liquid crystal display blanking control control pin DOF, and the level goes LOW when power save function is started. You can use the DOF output to stop the external power supply circuit function.

(28) Temperature Gradient Set

The 3-bit data of this command is used to set the temperature gradient characteristics of the liquid crystal drive voltage output from the built-in power supply circuit from eight states to one state. The temperature gradient of the liquid crystal drive voltage can be set according to the liquid crystal temperature gradient to be used. This eliminates the need of a temperature characteristics regulating circuit to be installed outside this IC.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	0	1	0	0	1	1	1	0	Mode set
1	1	0	*	*	*	*	*	P2	P1	P0	Register set

*: denote invalid bits.

P2	P1	P0	Temperature gradient (Reference)[%/°C]
0	0	0	-0.06
0	0	1	-0.08
0	1	0	-0.10
0	1	1	-0.11
1	0	0	-0.13
1	0	1	-0.15
1	1	0	-0.17
1	1	1	-0.18

$\overline{RES}$ After resetting by the $\overline{RES}$ pin, it is set to (0, 0, 0).

(29) Status Read

This command reads out the temperature gradient select bit set on the register.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	1	1	0	Mode set
1	0	1	*	*	*	*	*	*	P1	P0	Register set

*: denote invalid bits.

Following describes contents of register values P1 and P0 being read with the command.

Register	Result of reading	Descriptions
P1 *1	LOW	Display data RAM is normally operating.
	HIGH	Part of the bits of the display data RAM is probably garbled. Rewrite every bit of the display data RAM.
P0 *2	LOW	IC is normally operating.
	HIGH	Part of the bits of the command register is probably garbled. Normal display operation is disabled. Execute every command again.

*1: Note on register P1

After the system power is turned on and before the rewriting is completed, “1” can be sometimes indicated as the result of reading. Execution of this command must take place after every bit of the display data RAM has

been rewritten.
*2: Note on register P2
Following commands support the register error detection:

- Display ON/OFF
- Built-in Oscillation Circuit ON/OFF
- Power Control Set
- Display All Lighting ON/OFF
- All Display Normal/Reverse

You can detect the error if bits are garbled on the register specified with one of above five commands. When the register specified with the command is operating normally, LOW will be output.

After reset is done from $\overline{RES}$ pin, register P0 is set to HIGH. This arrangement is employed in order to detect reset of IC being caused by incoming noises as an error, too. In the normal operation sequence, therefore, above five commands must be set on the register before executing the status read.
You must execute, for instance, the built-in oscillation circuit OFF command even when this circuit is not used. Namely, all of above five commands must be executed (including the "OFF command" for the function not used) before the status read.

This command is intended for the self-check of a specific error mode and does not support detection of every error. Even when result of the status read done with this command was "normal", an error mode of some kind or another can be turned on due to excessive incoming noises, etc. Thus, not only the status read but also refreshing should be implemented on a regular basis.

ERR pin outputs ORed level of registers P1 and P0 independent of execution of the status read command, enabling to check the operating mode without using the command. Output operating conditions and precautions on use of the status read command are usable as that for ERR pin, too.

(30) Temperature sensor ON/OFF

The ON/OFF of the temperature sensor is set by this command. For more information, see 6.10 Temperature Sensor Circuit in FUNCTIONAL DESCRIPTION.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	1	1	0	1	0	0	0	Temperature sensor OFF
										1	Temperature sensor ON

The temperature sensor is set to OFF after performing reset.

When the built-in temperature sensor is used, this command is used to set the thermal sensor to ON. The temperature sensor setting to ON when it is not used, has no problem except for occurrence of approximately 10μA current consumption.

(31) MLS/drive method select

This command is used to select MLS drive method and liquid crystal AC drive method. Select the most suitable drive method for the display pattern.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	1	1	0	0	1	1	1	Mode set
1	1	0	*	*	*	P4	P3	0	1	1	Register set

* represents an invalid bit.

P4	P3	—	P1	P0	Drive method
0		—			n line inversionFrame inversion overlap OFF
1		—			n line inversionFrame inversion overlap ON
	0	—			MLS dispersion drive
	1	—			MLS non-dispersion drive

After resetting, (P4, P3) is set to (0, 1).

- n line inversion Frame inversion overlap ON/OFF

Controlled by the parameter P4. Enabled only when n line inversion drive is ON.
Deviation can be produced in liquid crystal AC drive, depending on combination of the number of display lines and the number of lines of n line inversion, which could cause dark and light stripes. This function reduces deviation in liquid crystal AC drive and dark and light stripes of display by overlapping the n-line inversion with the frame inversion.

- MLS dispersion drive / non-dispersion drive

Controlled by the parameter P3.
For this IC, the 4-line simultaneous selection MLS dispersion drive method has been adopted. The common output pin outputs a signal at the same time when the display lines are selected four times in 1 frame in 4 lines.
For non-dispersion drive, the common output pin outputs a signal by selecting four times continuously. It is recommended to use this drive if the display is frequently changed.
For dispersion drive, the common output pin outputs a signal by selecting four times at equal intervals in a frame. Compared to non-dispersion drive, higher contrast can be obtained basically, however, the display flicker may be caused in the drive in which animation is displayed.

In either function, determine to turn ON/OFF after evaluating the display quality in a comprehensive manner, including actual display pattern flicker and cross talk. The frame frequency from which optimal frequency can be obtained may be switched when the function is turned ON/OFF. Use the operation clock frequency select command or change the clock frequency supplied externally to drive at an appropriate frame frequency.

(32) NOP
This is a Non-Operation command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(33) Temperature sensor output read
This command convert analog voltage of temperature sensor SVD2 to digital value internally, and output the digital value to data bus. Refer to 6.10 Temperature sensor circuit.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Command
0	1	0	1	0	0	0	1	1	1	1	Mode set
0	1	0	*	P6	P5	P4	P3	P2	P1	P0	Register read

* represents an invalid bit.

7.2 Table of Commands

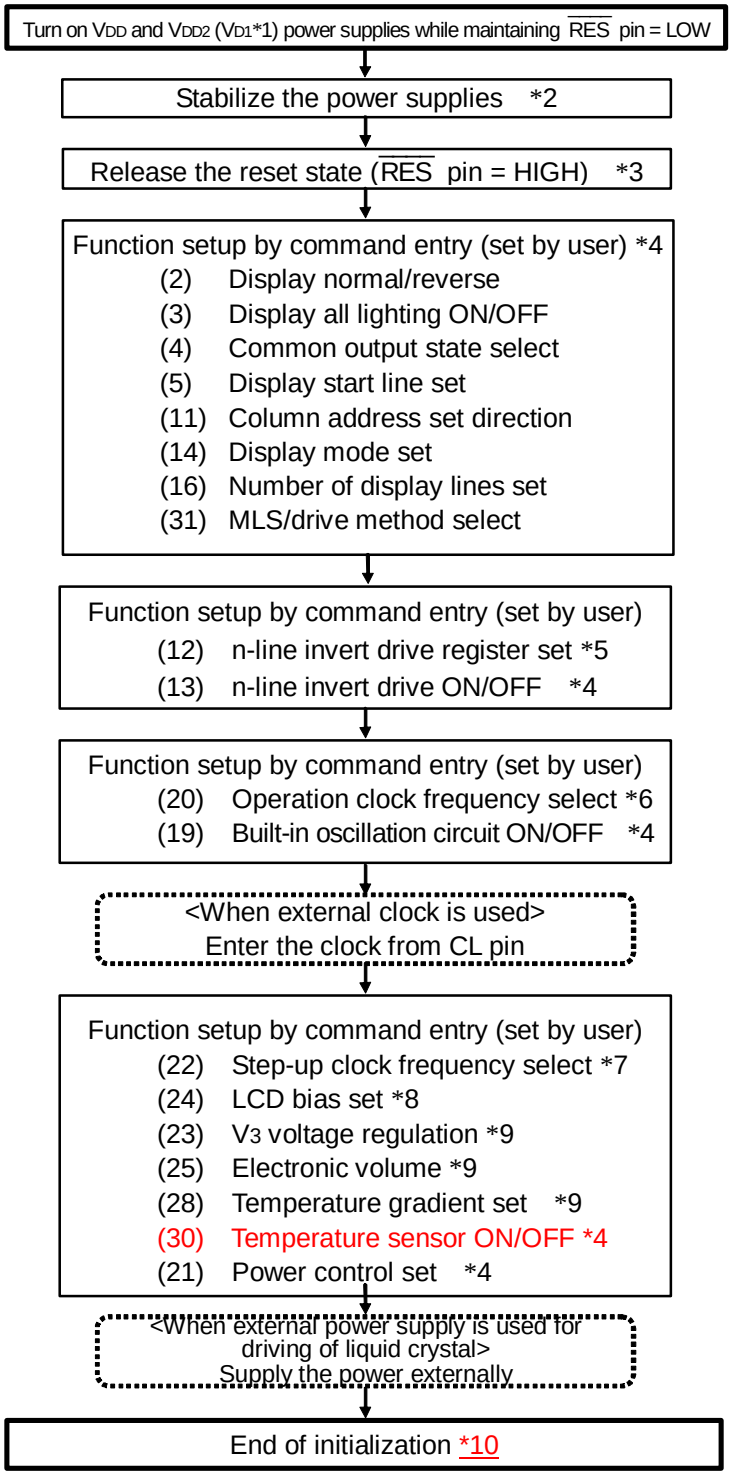
Table 7.1 Table of commands in S1D15719 series

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF control.
											1	0: OFF, 1: ON
(2) Display Normal /Reverse	0	1	0	1	0	1	0	0	1	1	0	LCD display normal/reverse
											1	0: Normal, 1: Reverse
(3) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display All Lighting
											1	0: Normal display, 1: All ON
(4) Common Output Status Select	0	1	0	1	1	0	0	0	1	0	0	Selects COM output scan direction.
											1	0: Normal, 1: Reverse
(5) Display Start Line Set	0	1	0	1	0	0	0	1	0	1	0	Sets display start line.
	1	1	0	*	Display start line address							
(6) Page Address Set	0	1	0	1	0	1	1	0	0	0	1	Sets the display RAM page address.
	1	1	0	*	*	Page address						
(7) Column Address Set	0	1	0	0	0	0	1	0	0	1	1	Sets the display RAM column address.
	1	1	0	Column Address Set								
(8) Display Data Write	0	1	0	0	0	0	1	1	1	0	1	Writes data to the display RAM.
	1	1	0	Writes data								
(9) Display Data Read	0	1	0	0	0	0	1	1	1	0	0	Reads data to the display RAM.
	1	0	1	Reads data								
(10) Display Data Input Direction Select	0	1	0	1	0	0	0	0	1	0	0	Display RAM data input direction
											1	0: Column direction, 1: Page direction
(11) Column Address Set Direction	0	1	0	1	0	1	0	0	0	0	0	Compatible with display RAM address SEG output
											1	0: Normal 1: Reverse
(12) n-line Inversion Drive Register Set	0	1	0	0	0	1	1	0	1	1	0	n-line invert drive.
	1	1	0	*	0	Invert line count						Sets the line count.
(13) n-line Inversion Drive ON/OFF	0	1	0	1	1	1	0	0	1	0	0	Resets the n-line invert drive.
											1	0: n-line OFF, 1: n-line ON
(14) Display Mode Set	0	1	0	0	1	1	0	0	1	1	0	Switches between dummy selection in the state of display and 4-gray scale display / binary display
	1	1	0	*	*	*	*	*	*	Mode		
(15) Gray-scale Pattern Set	0	1	0	0	0	1	1	1	0	0	1	Selects the contrast of gray-scale bit (1,0) (0,1).
	1	1	0	Gray-scale pattern								
(16) Number of Display Set	0	1	0	0	1	1	0	1	1	0	1	Sets the number of display lines and start address.
	1	1	0	*	*	Duty count						
	1	1	0	*	*	Static spot (block)						
(17) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. Write: +1, Read: 0
(18) End	0	1	0	1	1	1	0	1	1	1	0	Resets read modify write functions.
(19) Built-in Oscillator Circuit ON/OFF	0	1	0	1	0	1	0	1	0	1	0	Built-in oscillator circuit operation
											1	0: OFF, 1: ON
(20) Operation Clock Frequency Select	0	1	0	0	1	0	1	1	1	1	1	Sets the dividing ratio of the internal clock frequency f_{OSC}
	1	1	0	*	*	*	*	Frequency				
(21) Power Control Set	0	1	0	0	0	1	0	0	1	0	1	Selects built-in power supply operation state.
	1	1	0	*	*	*	*	Operation state				
(22) Step-up Clock Frequency Select	0	1	0	0	1	0	1	0	1	0	1	Step-up Clock Frequency Select
	1	1	0	*	*	*	*	Frequency				
(23) V_3 Voltage Select	0	1	0	0	0	1	0	1	0	1	1	Sets the V_3 voltage range.
	1	1	0	*	*	*	*	*	V_3 range			

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(24) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Selects the bias ratio of the liquid
	1	1	0	*	*	*	*	*	*	bias		crystal drive voltage.
(25) Electronic Volume Mode Set	0	1	0	1	0	0	0	0	0	0	1	V_3 output voltage is set to the
	1	1	0	*	Electronic volume							electronic volume register. 128 states
(26) Discharge ON/OFF	0	1	0	1	1	1	0	1	0	1	0	Discharges Power supply circuit
											1	connection capacitor.
												0: OFF (normal), 1:ON
(27) Power Save ON/OFF	0	1	0	1	0	1	0	1	0	0	0	Power Save 0: OFF, 1: ON
											1	
(28) Temperature Gradient Set	0	1	0	0	1	0	0	1	1	1	0	Sets the temperature gradient of the
	1	1	0	*	*	*	*	*	Temperature gradient			liquid crystal drive voltage
(29) Status Read	0	1	0	1	0	0	0	1	1	1	0	Outputs the result of detecting bit
	1	0	1	*	*	*	*	*	*	STAT		error to ERR bus
(30) Thermal sensor ON/OFF	0	1	0	0	1	1	0	1	0	0	0	Thermal sensor
											1	0: OFF (normal), 1: ON
(31) MLS/drive method select	0	1	0	1	1	1	0	0	1	1	1	Sets the MLS drive method and liquid
	1	1	0	*	*	*	0	MLS	0	1	1	crystal AC drive method
(32) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation command
(33) Temperature sensor output read	0	1	0	1	0	0	0	1	1	1	1	Bus output of emperature sensor digital value
	0	1	0	*	Digital read value							

7.3 Instruction Setup Example (Reference)

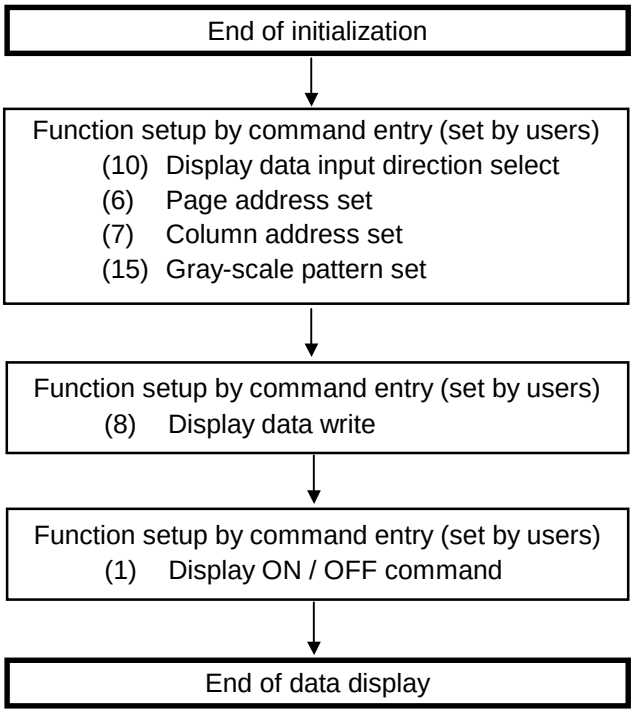
(1) Initial setup



Numbers in parentheses correspond to that used in description of the commands.

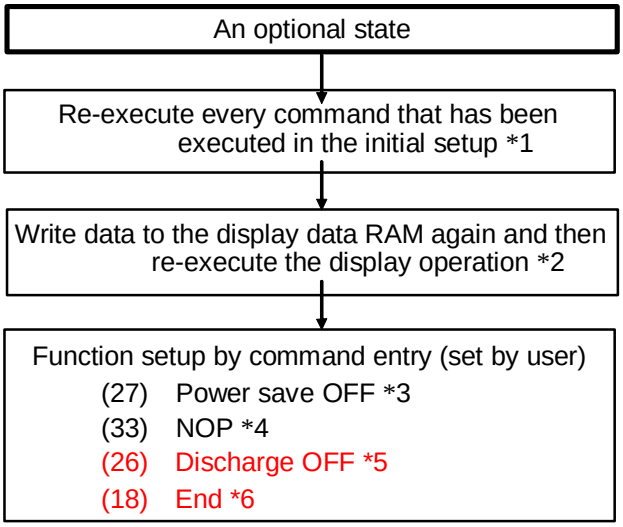
*1: When supplying V_{DI} power externally, be sure to turn it on at the same timing as V_{DD} is turned on.
*2: When the built-in V_{DI} generating circuit is used, the waiting time for stabilization must be set taking into consideration of not only V_{DD} and V_{DD2} but also the internally generated V_{DI} voltage. Necessary waiting time depends on the external circuit (such as capacity across V_{DI}-V_{SS}). Be sure to provide sufficient margin to the time.
*Reference: When V_{DD} = 5V, Capacitance to V_{DI} = 4.7µF, wait time = 30ms.
(The wait time is inverse proportional to V_{DD}, and proportional to Capacitance to V_{DI}.)
*3: In the initial state after the reset, contents of the display data RAM are uncertain.
*4: Execute each OFF commands or set the default value when performing initial setting and refreshing even if it is set to use the default value after reset or set to non-use of each function, so that a recovery can be made from a sudden change of internal state resulted from excessive external noise.
When the TEST pin is held by setting TEST3=V_{DI}, TEST4= V_{DI}, TESTA= V_{DI}, TESTB= V_{DI} due to constraints on implementation,
the command ECh (D7-D0: 11101100) must be issued. 5. See Test Pin in 5.6 PIN DESCRIPTION.
*5: It is not necessary to set if n-line inverted drive is not used.
*6: It is not necessary when the built-in oscillation circuit is not used.
*7: It is not necessary when the built-in step-up circuits are not used.
*8: It is not necessary when the built-in liquid drive voltage generating circuit (voltage follower) is not used.
*9: It is not necessary when the built-in V_3 voltage regulating circuit is not used.
*10: It is recommend not to access to this IC during rising LCD voltages up. The rising time is 24 frame period. When fFR = 80Hz, 24 frame period is around 300ms. It may be over 24 frame period according to external circuit, capacitors and wiring resistance. Therefore evaluate enough and set the wait time.

(2) Data display



Note: * DDRAM contents are not determined after end of initialization. Write data to all the DDRAM used for display. See “9. Display data write” in the “7. Command Description”.

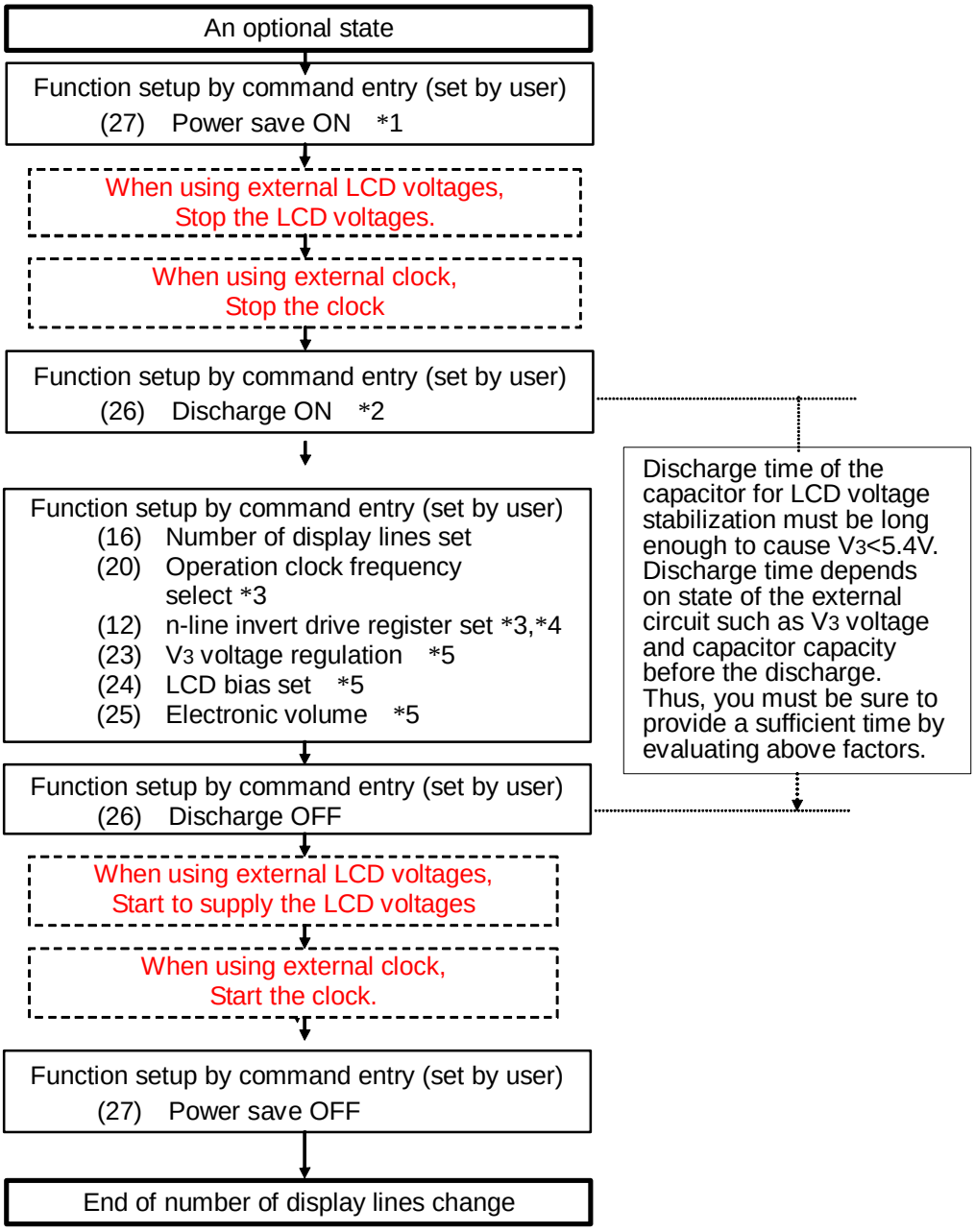
(3) Refresh



Although this IC retains a command-specified operating mode, the internal state can be altered by excessive incoming noises. You should make sure that the equipment or system is immune to noises or you should provide measures for suppressing generation of noises. It is recommended to refresh the operating mode and display contents on a regular basis in order to cope with excessive incoming noises.

*1: Refer to (1) Initial setup.
*2: Refer to (2) Data display.
*3: When IC chip is forced to the power save mode, you can turn the mode off by use of power save OFF command.
*4: When IC chip is forced to the test mode, you can turn the mode off by use of NOP command.
*5: When IC chip is forced to discharge state, you can quit the state by use of Discharge OFF command.
*6: When IC chip is forced to Read-Modify-Write state, quit the state by use of End command.

(4) When changing number of display lines



*1: As you change the number of display lines of liquid crystal, the LCD voltage currently selected for the optimum contrast is also modified. Thus, in order to avoid troubles such as momentary blacking of the screen, following operations should be implemented. Turn on the power save mode in the above sequence to turn off the display once, set the optimum LCD voltage and then turn on the display operation.

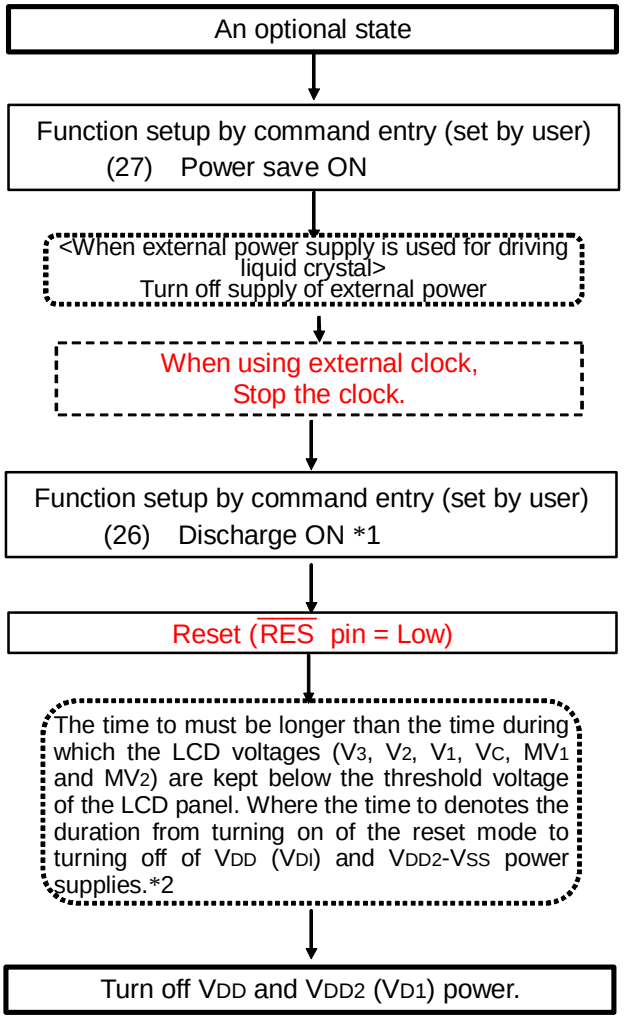
*2: Before changing the LCD voltage, the capacitor for retaining the voltage must be once discharged.

*3: You must make sure that the number of inverted n-lines and frame frequency you have selected do not cause troubles such as flicker.

*4: It is not necessary when the n-line invert drive is not employed.

*5: When the LCD voltage is externally supplied, specify the necessary items taking into consideration of the functions of the built-in power supply.

(5) Power OFF



This IC controls the circuits in the LCD system circuits by use of the power supply system circuits V_{DD} (V_{D1}) and V_{DD2}-V_{SS}. If V_{DD} (V_{D1}) and V_{DD2}-V_{SS} are turned off while voltage is remained on the LCD power supply system, uncontrolled voltage can be output from SEG and COM pins, potentially leading to display troubles. Thus, above powering off sequence must be strictly observed.

*1: This IC discharge external capacitor connected to the V_{OUT}, each CAP pin, V_3, V_2, V_1, V_C, MV_1 and MV_2 to V_{DD2} and V_{SS} by Discharge command ON. At this time, in some circuit configurations around the power supply, V_{DD2} and the power potential shorted with V_{DD2} go up by discharge current. To make sure that the potential of the V_{DD2} and power supply shorted with the V_{DD2} do not exceed its absolute maximum rating, take the following measures.

- Use the power supply circuit that can absorb the discharge intensity to the V_{DD2} pin
- Connect the zener diode between V_{DD2} and V_{SS}
- Use the smaller capacity values for each capacitor (trade-off with the display quality)
- Add the external resistance for discharge between the V_{OUT} and V_{SS}, and the V_3 and V_{SS} to limit the discharge flowing into the V_{DD2} power

*2: Threshold voltage of LCD panel is approximately 1[V].

8. ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V unless otherwise specified.

Table 8.1

Item		Symbol	Specified value	Unit
Power voltage (1)		V_{DD}	-0.3 to +6.0	V
Power voltage (2)		V_{DD2}	V_{DD} to +6.0	
Power voltage (3) (requires external input)		V_{DI}	-0.3 to +3.6	
Power voltage (4)		V_3, V_{OUT1}, V_{OUT2}	-0.3 to +27.0	
Power voltage (5)		V_2, V_1, V_C, MV_1, MV_2	-0.3 to V_3	
Input voltage		V_{IN}	-0.3 to V_{DD}+0.3	
Output voltage		V_O	-0.3 to V_{DD}+0.3	
Operating temperature	*1	T_{OPR}	-40 to +85	°C
	*2	T_{OPR}	-40 to +95	
Storage temperature	bare chip	T_{STR}	-55 to +125	

*1: S1D15719D10B000
*2: S1D15719D11B000, S1D15719D12B000

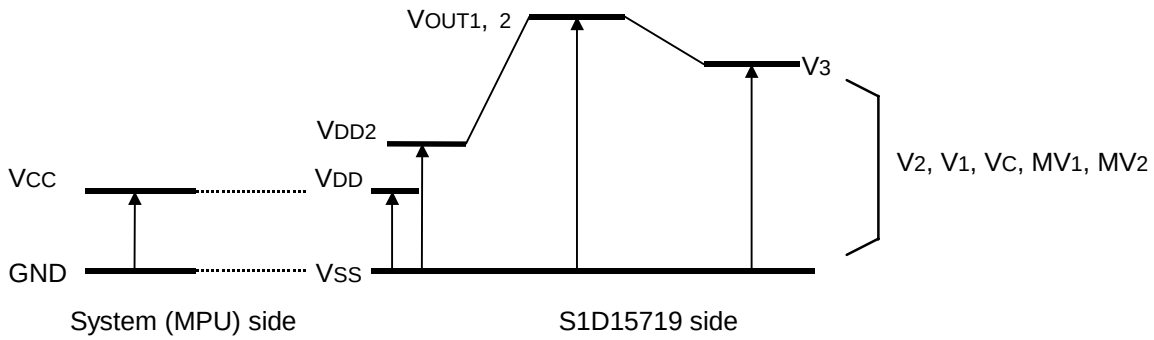


Fig.8.1

Notes: 1. Voltages V_3, V_2, V_1, V_C, MV_1 and MV_2 must always meet the conditions of
$V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq V_{SS}$

2. Voltage of V_{OUT1} and V_{OUT2} must be constantly in compliance with the requirement $V_{OUT2} \geq V_{OUT1} \geq V_{DD2} \geq V_{DD}$. When V_{OUT2} is externally supplied, the requirement $V_{OUT2} \geq V_3$+0.3V becomes applicable.
In case to supply V_{OUT1} and V_{OUT2} externally, the make V_{OUT1} and V_{OUT2} high-impedance during period from power-on VDD and VDD2 to power-on V_{OUT1} and V_{OUT2}.

3. If the LSI has been used in excess of the absolute maximum rating, it may be subjected to permanent breakdown. So in the normal operation, the LSI preferred to be used under the condition of electrical characteristics. If this condition is not met, LSI operation error may occur and LSI reliability may be deteriorated.

9. DC CHARACTERISTICS

V_{SS}=0V, V_{DD}=5.0V ±10% and Ta=-10 to +85°C unless otherwise specified.
Ta = -40 to 85°C (S1D15719D10B000)
Ta = -40 to 95°C (S1D15719D12B000/ S1D15719D11B000)

Table 9.1

Item		Symbol	Conditions		Specified value Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)	Operation enabled	V_{DD}	—		2.7	—	5.5	V	V_{DD} *1
Operating voltage (2)	Operation enabled	V_{DD2}	—		2.7	—	5.5		V_{DD2}
Operating voltage (3)	Operation enabled	V_{DI}	requires external input		2.7	—	3.3		V_{DI}
Operating voltage (4)	Recommended operations	$V_{OUT1,2}$	—		V_{DD2}	—	25.0		$V_{OUT1,2}$
Operating voltage (5)	Operation enabled	V_3	—		11.0	—	25.0		V_3 *2
High-level input voltage		V_{IHC}	V_{DD}=2.7V to 5.5V		0.8xV_{DD}	—	V_{DD}		*3
Low-level input voltage		V_{ILC}			V_{SS}	—	0.2xV_{DD}		*3
Hysteresis voltage		V_H	V_{DD}= 5.0V		0.5	0.9		V	*4
High-level output voltage		V_{OHC}	V_{DD}=2.7V	I_{OH}=-25µA	0.8xV_{DD}	—	V_{DD}		*5
Low-level output voltage		V_{OLC}	to 5.5V	I_{OL}= 25µA	V_{SS}	—	0.2xV_{DD}		*5
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		-1.0	—	1.0	µA	*6
Output leak current		I_{LO}			-3.0	—	3.0		*7
LCD driver ON resistance		R_{ON}	Ta=25°C	V_3= 12.0V	—	2.5	6.0	kΩ	SEGn
				V_3= 20.0V	—	0.8	2.0		COMn *8
Static current consumption		I_{DDQ}	Ta=25°C	V_{DD} = 3.0V	—	0.3	1.0	µA	V_{DD} *9
		I_{3Q}		V_3 = 16.0V	—	0.3	1.0		V_3
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		—	8	15	pF	—
Oscillation frequency	Built-in oscillation	f_{OSC}	Ta=25°C Max. frequency		4749	4896	5043	kHz	*10
	External input	f_{CL}	S1D15719D10B000		—	—	1300		*11
			S1D15719D11B000		—	—	1300		
			S1D15719D12B000		—	—	1250		

Table 9.2

Item	Symbol	Conditions	Specified value Min.	Typ.	Max.	Unit	Applicable pin
Input voltage to 1st booster circuit	V_{DD2}	Double boosting	2.7	—	5.5	V	V_{DD2}
	V_{DD2}	Triple boosting	2.7	—	5.5		
	V_{DD2}	Quadruple boosting	2.7	—	5.5		
	V_{DD2}	Quintuple boosting	2.7	—	5.0		
	V_{DD2}	Sextuple boosting	2.7		4.1		
Output voltages from 1st booster circuit	V_{OUT1}		—	—	25.0		V_{OUT1} *12
Output voltage from 2nd booster circuit	V_{OUT2}		—	—	25.0		V_{OUT2} *13
Voltage regulating circuit operating voltage	V_3		11.0	—	25.0		V_3

[Asterisked references]

*1. Does not guarantee if there is an abrupt voltage variation during MPU access.

*2. For V_{DI} and V_3 system operating voltage range, see Fig.9.2.

3. A0, D0 to D5, D6(SCL), D7(SI), RD(E), WR(R/W), CS, CLS, CL, FR, F1, F2, SYNC, M/S, C86, P/S, DOF, RES, V_{DIS}, TEST

*4 Apply to S1D15719D11B, S1D15719D12B. A0, D6(SCL), D7(SI), RD(E), WR(R/W), CS, CL, RES pins.

*5. D0 to D7, FR, DOF, CL, F1, F2, SYNC, ERR and TEST5 pins. (Except ERR pin of the S1D15712D12B)

6: A0, RD(E), WR(R/W), CS, CLS, MS, C86, P/S, RES, V_{DIS} and TEST pins

*7: It is applicable when D0 to D5, D6(SCL), FR, DOF, F1, F2, SYNC and TEST5 pins are caused to the high impedance.

*8: It is the resistance value resulting from applying 0.1V across the output pin SEGn or COMn and respective power terminals (V_2, V_1, V_C, MV_1 and MV_2).
R_{ON} = 0.1V/ΔI (ΔI represents the current being conducted when 0.1V is applied while the power supply is turned on)

*9: It is the current value at V_{DIS} = LOW.

*10: For the relation between the oscillation frequency and frame frequency, refer to Table 9.13 The internal oscillation item indicates the manufacturing process-dependant variations in frequency of the built-in oscillation circuit. And the external input item represents the maximum operating voltage.

*11: Maximum external clock frequency is depend on model. Refer table 10-12, 10-15, 10-18.

*12: When using the 2nd booster circuit is used, you must decide the amplification factor and voltage the requirement V_{OUT1}>12.8V may be met. When the 2nd booster circuit is not used, select the amplification factor and voltage so that the relation V_{OUT1}=V_{125}=V_{OUT2}>V_3+0.3V may be constantly maintained.

*13: When the 1st and 2nd booster circuits are not used and V_{OUT2} voltage is externally supplied, the voltage supplied must constantly meet the requirement V_{OUT2}>V_3+0.3V.

9.1 Dynamic current consumption value

9.1.1 When the built-in power supplied is turned OFF

- Indication mode: f_{FR}=100Hz, No line reversion 1/11 bias, undivided drive

Table 9.3 Indications: All white indications *14

V_{DD}	1st booster factor	V_3 voltage	1/136 Duty		1/68 Duty		Unit	Remark
			Typ.	Max.	Typ.	Max.		
5V	—	16.0	1889	3780	1034	2070	μA	*14
		11.0	1887	3780	1031	2060		
3V	—	16.0	1760	3520	976	1960		
		11.0	1760	3520	976	1960		

Table 9.4 Indications: Heavy load indications *15

V_{DD}	1st booster factor	V_3 voltage	1/136 Duty		1/68 Duty		Unit	Remark
			Typ.	Max.	Typ.	Max.		
5V	—	16.0	2002	4000	1089	2180	μA	*15
		11.0	1998	4000	1087	2180		
3V	—	16.0	1865	3730	1030	2060		
		11.0	1865	3730	1030	2060		

Display mode in binary at f_{FR}=80Hz, No line reversion, 1/11 bias, undivided drive

Table 9.5 Display: entirely in white *14 Code: ISS (1)

V_{DD}	1st booster factor	V_3 voltage	1/136 Duty		1/68 Duty		Unit	Remarks
			Typ.	Max.	Typ.	Max.		
5V	—	16.0	1492	2990	836	1670	μA	*14
		11.0	1491	2990	835	1670		
3V	—	16.0	1403	2800	797	1600		
		11.0	1403	2800	797	1600		

Table 9.6 Display: Heavy load display *15 Code: ISS (1)

V_{DD}	1st booster factor	V_3 voltage	1/136 Duty		1/68 Duty		Unit	Remarks
			Typ.	Max.	Typ.	Max.		
5V	—	16.0	1582	3160	881	1760	μA	*15
		11.0	1580	3160	880	1760		
3V	—	16.0	1488	2970	840	1680		
		11.0	1488	2970	840	1680		

9.1.2 When the built-in power supply is turned ON

T_a = 25°C. The current value consumed by entire IC including the built-in power supply.

- 4 gray-scale display mode, f_{FR}=100Hz, n-line inversion, 1st and 2nd booster circuits are, V_{DD}=V_{DD2}, 1/11 bias and undivided drive.

Table 9.7 Display: Entirely in white

V_{DD} [V]	1st booster factor	V_3 [V]	Specified value 1/136 Duty Typ.	1/136 Duty Max.	1/68 Duty Typ.	1/68 Duty Max.	Units	Remarks
5V	4	16.0	2476	4950	1617	3240	µA	*14
		11.0	2470	4841	1564	3130		
3V	5	16.0	2444	4890	1659	3320		
		11.0	2377	4750	1591	3180		

Table 9.8 Display: Heavy load display

V_{DD} [V]	1st booster factor	V_3 [V]	Specified value 1/136 Duty Typ.	1/136 Duty Max.	1/68 Duty Typ.	1/68 Duty Max.	Units	Remarks
5V	4	16.0	2732	5470	1736	3470	µA	*15
		11.0	2598	5200	1648	3300		
3V	5	16.0	2747	5500	1802	3600		
		11.0	2579	5160	1689	3380		

[*: Refer to P79]

-
- Binary display mode, f_{FR}=80Hz, no n-line inversion, 1st and 2nd booster circuits are used, 1/11 bias and undivided drive.

Table 9.9 Display: Entirely in white

V_{DD} [V]	1st booster factor	V_3 [V]	Specified value 1/136 Duty Typ.	1/136 Duty Max.	1/68 Duty Typ.	1/68 Duty Max.	Units	Remarks
5V	4	16.0	2078	4160	1419	2840	µA	*14
		11.0	2023	4050	1369	2740		
3V	5	16.0	2080	4160	1472	2940		
		11.0	2015	4031	1409	2820		

Table 9.10 Display: Heavy load display

V_{DD} [V]	1st booster factor	V_3 [V]	Specified value 1/136 Duty Typ.	1/136 Duty Max.	1/68 Duty Typ.	1/68 Duty Max.	Units	Remarks
5V	4	16.0	2283	4570	1514	3030	µA	*15
		11.0	2167	4330	1430	2860		
3V	5	16.0	2324	4650	1583	3170		
		11.0	2177	4350	1481	2960		

9.2 Current Consumption under Power Saving Mode

- V_{DD} = 5V, T_a = 25°C

Table 9.11

Item	Symbol	Condition	Specified value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	VDIS = HIGH	—	24.0	48.0	μA	—

- V_{DD} = 3V, V_{DI} = 3V,T_a = 25°C

Table 9.12

Item	Symbol	Condition	Specified value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS2}	VDIS = LOW	—	0.3	1.0	μA	—

[Remarks on * marked item]

*14: It is the case when the display was turned on by use of the built-in oscillation circuit after writing "0" every bit of the display data RAM. The current indicated represents the one consumed by IC alone and does not include that for the LCD panel and wiring capacity. Above case is applicable when access from MPU is absent.

*15. It is the case when the display was turned on by use of the built-in oscillation circuit after writing the display data that requires the maximum current consumption. The current indicated is the one consumed by IC alone and does not include that for the LCD panel and wiring capacity. Above case is applicable when access from MPU is absent.

9.3 Reference Data

9.3.1 While access from MPU is taking place

- The current consumed by IC alone while constant writing of heavy load display patterns is continued by use of f_{CYC}.
  V_{DD}= 5V, V_3=16V, f_{FR}=100Hz, no n-line inversion, built-in power supply turned off, 1/11 bias, undivided drive and display ON. T_a=25°C.

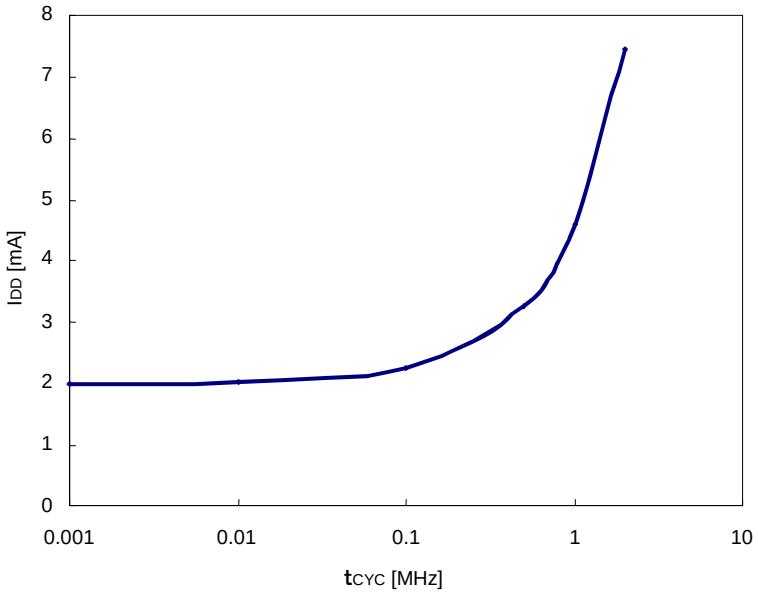


Fig.9.1

9.3.2 Operating voltage rang of V_{DI} system and V_3 system

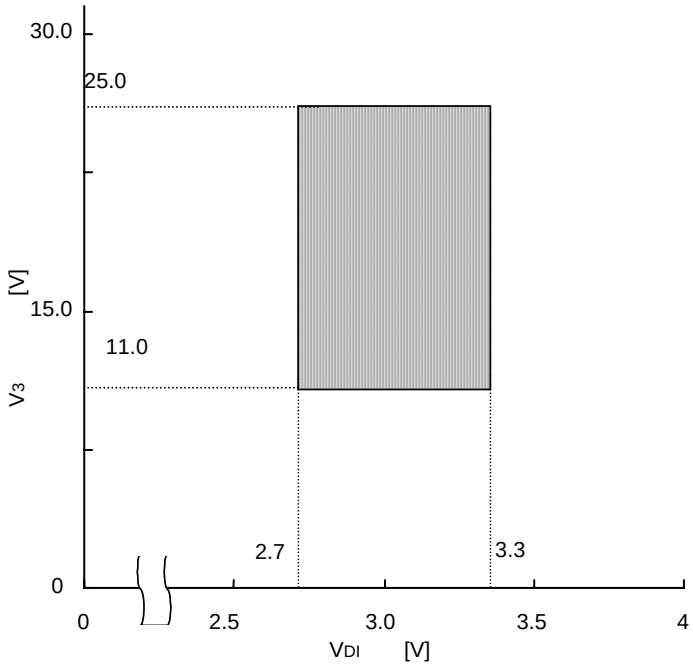


Fig.9.2

9.3.3 Liquid crystal frame frequency f_{FR}

- When l is specified for the number of display lines

Table 9.13

Item	Internal operation clock frequency f_{CL}	Display operation clock frequency f_{DCLK}	Frame frequency f_{FR}
When built-in oscillation circuit is used	See page 47	$f_{CL}/45$	$f_{FR} = \frac{f_{DCLK}}{l+4} = \frac{f_{CL}/45}{l+4}$
When built-in oscillation circuit is not used	External input (f_{CL})		

- Display operation clock f_{DCLK} represents the duration of a single operation in the sequential selection of lines of liquid crystal.
- Display duty is expressed as $\text{duty} = 1/(l+4)$.
- Frame frequency denotes the frequency used to rewrite a single screen. It does not represent the signal from FR pin (= cycle of alternated drive).

9.4 Characteristics of Thermal Sensor

9.4.1 Analog voltage output characteristics

Table 9.14

Item	Symbol	Condition	Specified value			Unit	Applicable pins
			Min.	Typ.	Max.		
Operating voltage range	V_{SV}	—	2.7	—	5.5	V	V_{DD}
Operating temperature range	Ta	—	-40	—	85	°C	
Temperature accuracy	T_{ACCA}	-40 to 85°C	-5.0	—	5.0	°C	SV_{D2} *1
Output voltage	V_{SVD2}	-40°C 25°C 85°C	1.472 1.176 0.887	1.496 1.200 0.911	1.520 1.224 0.935	V	SV_{D2} *1, *4
Temperature gradient of output voltage	V_{GRA}	*2	—	-4.70	—	mV/°C	SV_{D2} *2
Output voltage setup time	t_{SEN}		100	—	—	mS	SV_{D2} *3
Operating current	I_{SEN}	25°C	—	15	30	μA	V_{DI} *5

[Remarks on * marked item]

*1 The typ. value of the sensor analog output voltage SVD2 when ambient temperature is Ta [°C] is approximated by the following expression.
It should be noted that the (equation 9-1) uses the unit of mV.

$$V_{SVD2} = -0.002 \bullet Ta^{2} - 4.590 \bullet Ta + 1316[mV] \qquad \text{(Equation 9-1)}$$

The sensor analog output voltage is output with accuracy of ±5°C of temperature conversion at -40 to 85°C.

*2 Approximate linear gradient of the VSVD2 output within the specified temperature range. Apply to all the operating temperature range.
Based on the temperature accuracy of ±5°C and temperature variation of the sensor analog voltage of -4.70 mV/°C, the accuracy of the sensor analog output has variations of

$$\Delta V_{SVD2} = \pm(4.70 \times 5) \cong \pm 24[mV]$$

when centering around the value determined by (Equation 9-1) at at any ambient temperature Ta [°C]. The relationship between the accuracy of the sensor analog output and temperature is shown in Figure.

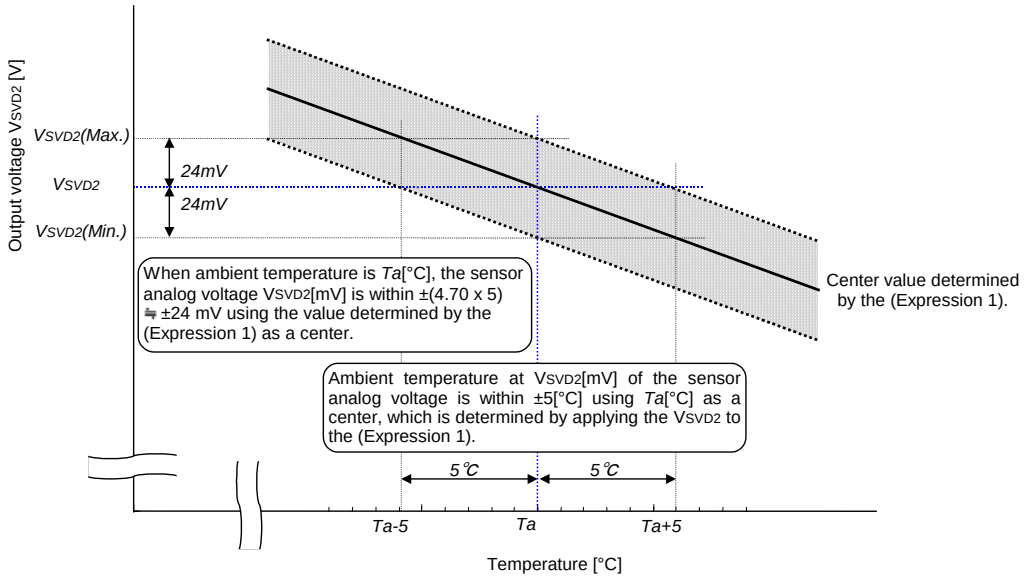


Fig.9.3

*3 until the output voltage is stabilized, allowing the monitoring. Be sure to provide the specified waiting time at minimum before starting sampling of output voltages.

*4 Set the load capacity CL of the sensor analog voltage output pin to 100pF or lower and Load resistance RL to 1MΩ or higher. To obtain an accurate output voltage value, it should be noted that current path must not be provided between the VDD or VDI.
If SVD2 voltage waveforms are unstable, some stabilizing capacity can be added between SVD2 and VSS. In such case, as explained in 6.10.3 Paragraph (2) “Influence of mounting” of Subsection 6.10.2 “Notes,” the voltage drop (ΔV) at VSS is smoothed by the stabilizing capacity and it is used as an offset to SVD2 voltage.
Make sure that the SVD2 voltage difference between the time when the system is operated normally and the time when only the temperature sensor circuit is operated is acceptable for the required temperature control.

*5 It is current consumption of the temperature sensor only. When temperature sensor is turned on during operation, this current consumption is added.

9.4.2 Digital conversion characteristics

Table 9-15

Item	Symbol	Condition	Specified value			Unit	Applicable pins
			Min.	Typ.	Max.		
Operating temperature range	Ta	—	-40		85	°C	
Temperature accuracy	TACCD	-40 to 85°C	-5	—	5	°C	
Digital output value	DSVD2	-40°C 25°C 80°C	— — —	3 65 125	— — —	—	D7 to D0 *1
Digital conversion delay time	tDDL	—	—	128		Frame	*2

*1 Approximate equation of the digital output voltage D_{SVD2} is following. Unit of Equation 9-2 is digital value by decimal.

$$DSVD2 = 0.001 * Ta^2 * 0.978*Ta+40.20 \quad \text{(Equation 9-2)}$$

The digital value have +/-5°C accuracy in -40 to 85°C tempareture range.
Output value is 0 to 127, however it may overflow or underflow in case of 0 or 127, therefore the value is invalid. Actual valid digital value is 1 to 126.

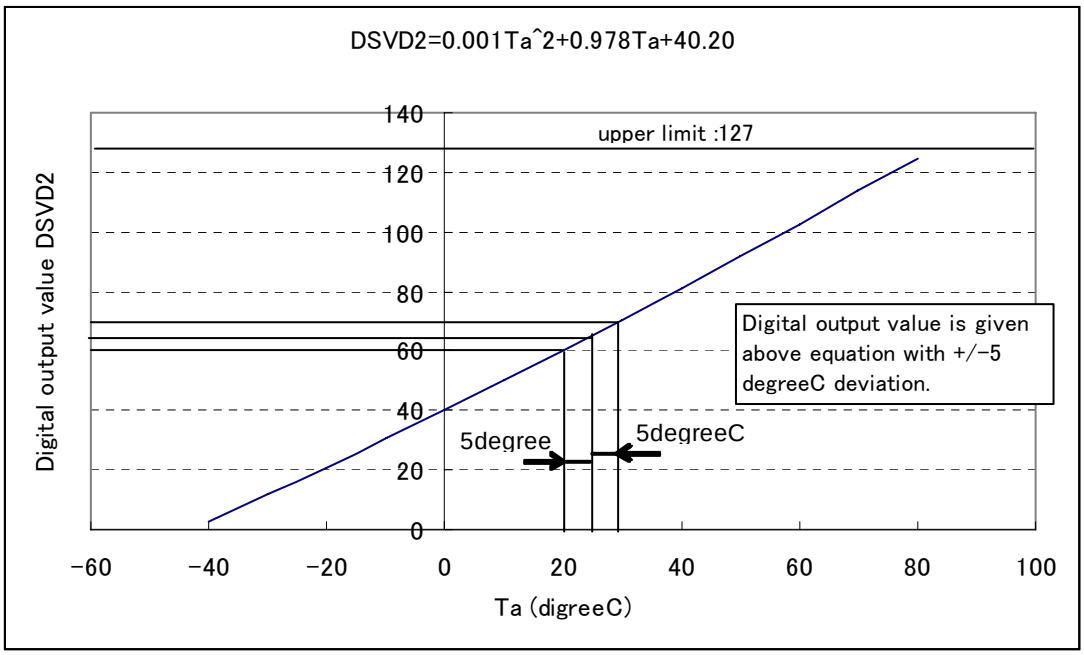


Fig. 9.4 relation between Digital output value and temperature

*2 Sensor output value is updated by constant cycle. The update cycle is 1 frame period. Refer to 9.3.3 LCD frame frequency f_{FR}.

(1 frame period is $1/f_{FR}$)

10. TIMING CHARACTERICTICS

10.1 System path read/write characteristics 1 (80 system MPU)

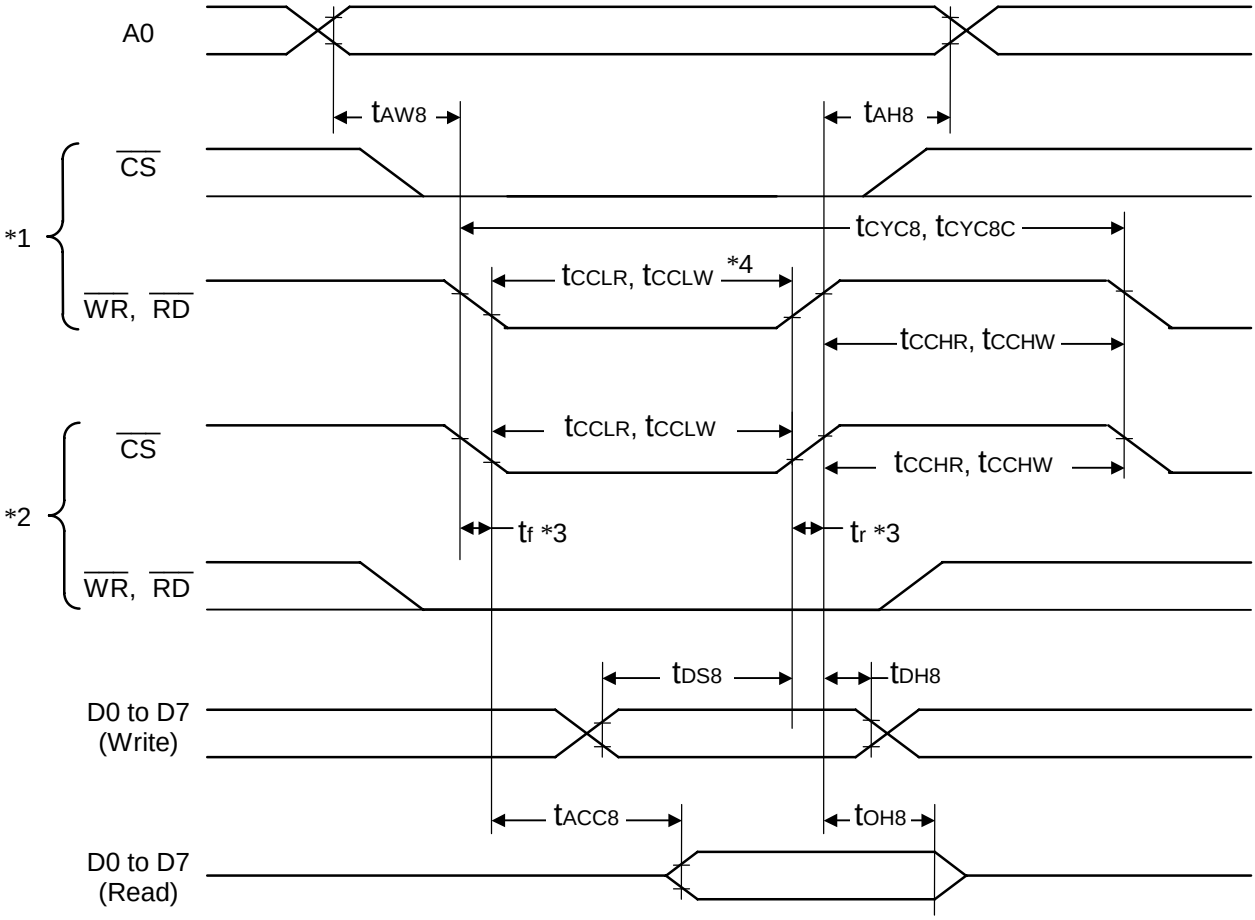


Fig.10.1

10.1.1 S1D15719D10B000

Table 10.1

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Item	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$, $\overline{CS}$	t_{WCYC8}		1100	—	
System read cycle time	$\overline{RD}$, $\overline{CS}$	t_{RCYC8}		2000	—	
Control Low-pulse width ($\overline{WR}$, $\overline{CS}$)	$\overline{WR}$, $\overline{CS}$	t_{CCLW}		500	—	
Control Low-pulse width ($\overline{RD}$, $\overline{CS}$)	$\overline{RD}$, $\overline{CS}$	t_{CCLR}		950	—	
Control High-pulse width ($\overline{WR}$, $\overline{CS}$)	$\overline{WR}$, $\overline{CS}$	t_{CCHW}		500	—	
Control High-pulse width ($\overline{RD}$, $\overline{CS}$)	$\overline{RD}$, $\overline{CS}$	t_{CCHR}		500	—	
Data setup time	D0 to D7	t_{DS8}		200	—	
Data hold time ($\overline{WR}$)		t_{DH8}		30	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	950	
Output disable time		t_{OH8}		5	200	

10.1.2 S1D15719D11B000

Table 10.2

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Item	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		50	—	ns
Address setup time		t_{AW8}		50	—	
System write cycle time	$\overline{WR}$, $\overline{CS}$	t_{WCYC8}		1350	—	
System read cycle time	$\overline{RD}$, $\overline{CS}$	t_{RCYC8}		2100	—	
Control Low-pulse width ($\overline{WR}$, $\overline{CS}$)	$\overline{WR}$, $\overline{CS}$	t_{CCLW}		550	—	
Control Low-pulse width ($\overline{RD}$, $\overline{CS}$)	$\overline{RD}$, $\overline{CS}$	t_{CCLR}		1000	—	
Control High-pulse width ($\overline{WR}$, $\overline{CS}$)	$\overline{WR}$, $\overline{CS}$	t_{CCHW}		700	—	
Control High-pulse width ($\overline{RD}$, $\overline{CS}$)	$\overline{RD}$, $\overline{CS}$	t_{CCHR}		700	—	
Data setup time	D0 to D7	t_{DS8}		250	—	
Data hold time ($\overline{WR}$)		t_{DH8}		80	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	1000	
Output disable time		t_{OH8}		15	250	

10.1.3 S1D15719D12B000

Table 10.3

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Item	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		50	—	ns
Address setup time		t_{AW8}		50	—	
System write cycle time	$\overline{WR}$, $\overline{CS}$	t_{WCYC8}		1350	—	
System read cycle time	$\overline{RD}$, $\overline{CS}$	t_{RCYC8}		2100	—	
Control Low-pulse width ($\overline{WR}$, $\overline{CS}$)	$\overline{WR}$, $\overline{CS}$	t_{CCLW}		550	—	
Control Low-pulse width ($\overline{RD}$, $\overline{CS}$)	$\overline{RD}$, $\overline{CS}$	t_{CCLR}		1150	—	
Control High-pulse width ($\overline{WR}$, $\overline{CS}$)	$\overline{WR}$, $\overline{CS}$	t_{CCHW}		700	—	
Control High-pulse width ($\overline{RD}$, $\overline{CS}$)	$\overline{RD}$, $\overline{CS}$	t_{CCHR}		700	—	
Data setup time	D0 to D7	t_{DS8}		250	—	
Data hold time ($\overline{WR}$)		t_{DH8}		300	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	1150	
Output disable time		t_{OH8}		50	400	

*1. This is in case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS}$ = LOW.
*2. This is in case of making the access by $\overline{CS}$, setting the $\overline{WR}$, $\overline{RD}$ = LOW.
*3. Input signal rise and fall time (t_r, t_f) must not exceed 15ns. When the system cycle time is used at a high speed, it is specified by $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$
*4. t_{CCLW} and t_{CCLR} are specified in terms of the overlapped period when $\overline{CS}$ is at LOW level and $\overline{WR}$ and $\overline{RD}$ are at LOW level.
*5. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

10.2 System path read/write characteristics 2 (68 system MPU)

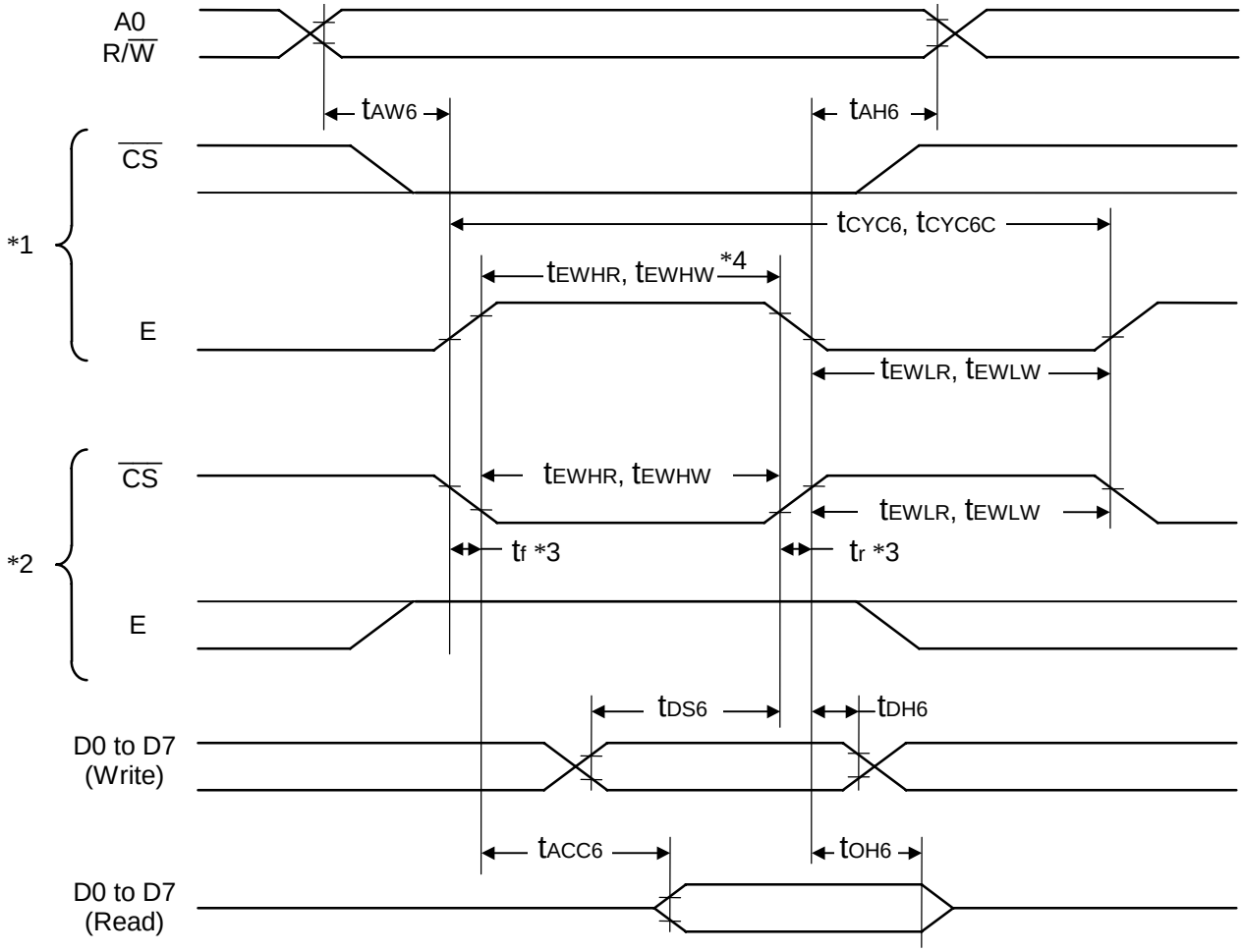


Fig.10.2

10.2.1 S1D15719D10B000

Table 10.4

[V_{DD}=2.7V to 5.5V, Ta= -40 to +85°C]

Item		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System write cycle time		E, $\overline{CS}$	t_{WCYC6}		1100	—	
System read cycle time		E, $\overline{CS}$	t_{RCYC6}		2000	—	
Data setup time		D0 to D7	t_{DS6}		200	—	
Data hold time (E)			t_{DH6}		30	—	
Access time			t_{ACC6}	C_L=100pF	—	950	
Output disable time			t_{OH6}		5	200	
Enable HIGH-pulse width	Read	E, $\overline{CS}$	t_{EWHR}		950	—	
	Write	E, $\overline{CS}$	t_{EWHW}		500	—	
Enable LOW-pulse width	Read	E, $\overline{CS}$	t_{EWLR}		500	—	
	Write	E, $\overline{CS}$	t_{EWLW}		500	—	

10.2.2 S1D15719D11B000

Table 10.5

[V_{DD}=2.7V to 5.5V, Ta= -40 to +95°C]

Item		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		50	—	ns
Address setup time			t_{AW6}		50	—	
System write cycle time		E, $\overline{CS}$	t_{WCYC6}		1350	—	
System read cycle time		E, $\overline{CS}$	t_{RCYC6}		2100	—	
Data setup time		D0 to D7	t_{DS6}		250	—	
Data hold time (E)			t_{DH6}		80	—	
Access time			t_{ACC6}	C_L=100pF	—	1000	
Output disable time			t_{OH6}		15	250	
Enable HIGH-pulse width	Read	E, $\overline{CS}$	t_{EWHR}		1000	—	
	Write	E, $\overline{CS}$	t_{EWHW}		550	—	
Enable LOW-pulse width	Read	E, $\overline{CS}$	t_{EWLR}		700	—	
	Write	E, $\overline{CS}$	t_{EWLW}		700	—	

10.2.2 S1D15719D12B000

Table 10.6

[V_{DD}=2.7V to 5.5V, Ta= -40 to +95°C]

Item		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		50	—	ns
Address setup time			t_{AW6}		50	—	
System write cycle time		E, $\overline{CS}$	t_{WCYC6}		1350	—	
System read cycle time		E, $\overline{CS}$	t_{RCYC6}		2100	—	
Data setup time		D0 to D7	t_{DS6}		250	—	
Data hold time (E)			t_{DH6}		300	—	
Access time			t_{ACC6}	C_L=100pF	—	1150	
Output disable time			t_{OH6}		50	400	
Enable HIGH-pulse width	Read	E, $\overline{CS}$	t_{EWHR}		1150	—	
	Write	E, $\overline{CS}$	t_{EWHW}		550	—	
Enable LOW-pulse width	Read	E, $\overline{CS}$	t_{EWLR}		700	—	
	Write	E, $\overline{CS}$	t_{EWLW}		700	—	

*1. This is in case of making the access by E, setting the $\overline{CS}$ = LOW.
*2. This is in case of making the access by $\overline{CS}$, setting the E = HIGH.
*3. The rise time and the fall time (t_r & t_f) of the input signals should be set to 15ns or less. When it is necessary to use the system cycle time at high speed, the rise time and the fall time should be so set to conform to ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) or ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLR} – t_{EWHR}$)
*4. t_{EWLW}, t_{EWLR} should be set to the overlapping zone where the $\overline{CS}$ is at LOW level and where the E is on the HIGH level.
*5. All the timing should basically be set to 20% or 80% of the V_{DD}.

10.3 Serial Interface

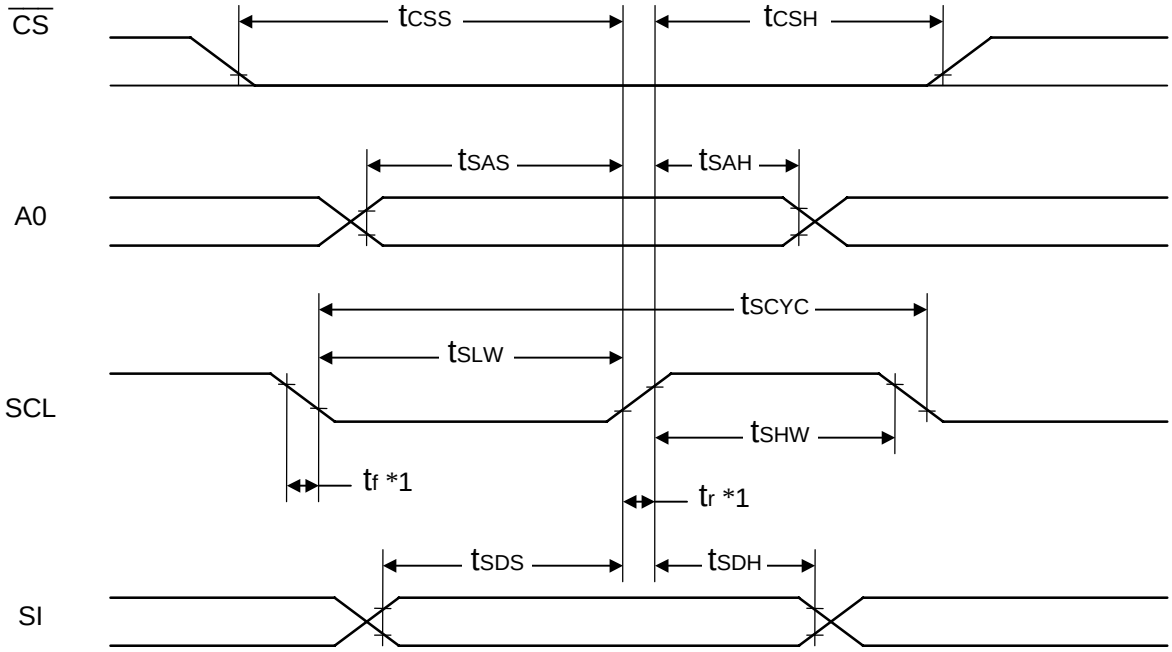


Fig.10.3

10.3.1 S1D15719D10B000

Table 10.7

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		350	—	ns
SCL H pulse width		t_{SHW}		150	—	
SCL L pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		200	—	
Address hold time		t_{SAH}		200	—	
Data setup time	SI	t_{SDS}		150	—	
Data hold time		t_{SDH}		150	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		200	—	
		t_{CSH}		200	—	

10.3.2 S1D15719D11B000

Table 10.8

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		650	—	ns
SCL H pulse width		t_{SHW}		300	—	
SCL L pulse width		t_{SLW}		300	—	
Address setup time	A0	t_{SAS}		200	—	
Address hold time		t_{SAH}		200	—	
Data setup time	SI	t_{SDS}		300	—	
Data hold time		t_{SDH}		300	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		400	—	
		t_{CSH}		200	—	

10.3.3 S1D15719D12B000

Table 10.9

[V_{DD}=2.7V to 5.5V, Ta= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		250	—	ns
SCL H pulse width		t_{SHW}		100	—	
SCL L pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		150	—	
		t_{CSH}		150	—	

*1. Input signal rise and fall time (t_r, t_f) must not exceed 15ns. If the operation timing exceeds the limit, t_{SCYC}, t_{SHW} and t_{SLW} standard width shall be provided.
*2. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

10.4 Display Control Input and Output Timing

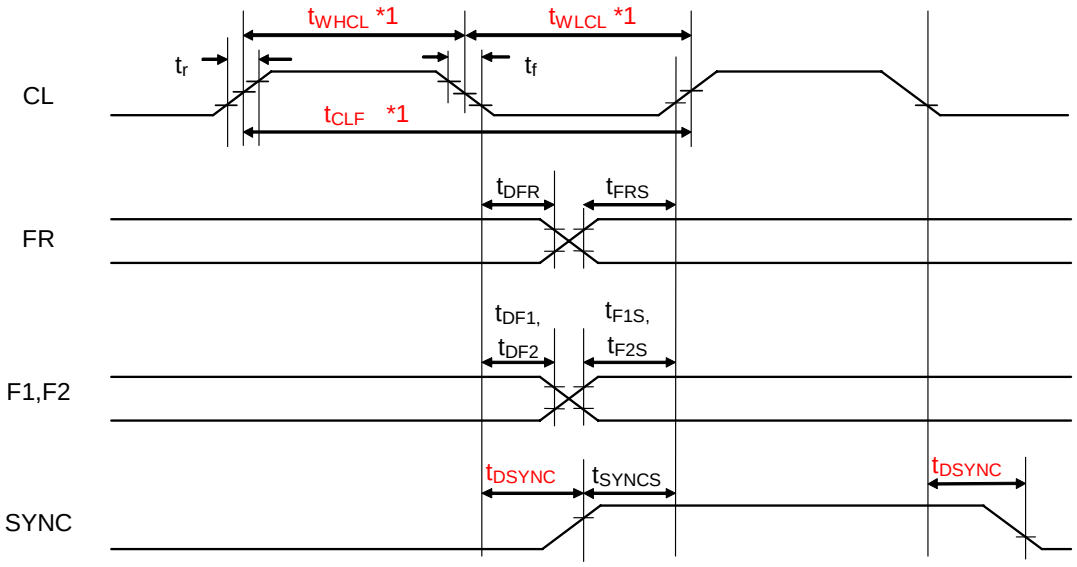


Fig.10.4

10.4.1 S1D15719D10B000

Table 10.10 output Timing (in case of using built-in oscillator)

[V_{DD}=2.7V to 5.5V, Ta= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-200	—	200	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		-200	—	200	ns
SYNC delay time	SYNC	t_{DSYNC}		-200	—	200	ns

Table 10.11 output Timing (in case of using external clock)

[V_{DD}=2.7V to 5.5V, Ta= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-200	—	200	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		-200	—	200	ns
SYNC delay time	SYNC	t_{DSYNC}		-200	—	200	ns

Table 10.12 Input Timing

[V_{DD}=2.7V to 5.5V, Ta= -40 to 85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		0	—	t_{WLCL} + 200	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		0	—	t_{WLCL} + 200	ns
SYNC delay time	SYNC	t_{DSYNC}		0	—	t_{WLCL} + 200	ns
Input clock duty ratio *2	CL	t_{CLD}		20	—	80	%
Input clock rise time (20% to 80%)		t_r		—	—	15	ns
Input clock fall time (20% to 80%)		t_f		—	—	15	ns
Input clock cycle(1)		t_{CLF}	1chip usage	770	—	—	ns
Input clock L pulse width(1)		t_{WLCL}		200	—	—	ns
Input clock H pulse width(1)		t_{WHCL}		200	—	—	ns
Input clock cycle(2)		t_{CLF}	Master/slave usage	770	—	—	ns
Input clock L pulse width(2)		t_{WLCL}		200	—	—	ns
Input clock H pulse width(2)		t_{WHCL}		200	—	—	ns

10.4.2 S1D15719D11B000

Table 10.13 output Timing (in case of using built-in oscillator)

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-600	—	200	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		-600	—	200	ns
SYNC delay time	SYNC	t_{DSYNC}		-600	—	200	ns

Table 10.14 output Timing (in case of using external clock)

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	50	—	700	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		50	—	700	ns
SYNC delay time	SYNC	t_{DSYNC}		50	—	700	ns

Table 10.15 Input Timing

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		0	—	t_{WLCL}	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		0	—	t_{WLCL}	ns
SYNC delay time	SYNC	t_{DSYNC}		0	—	t_{WLCL}	ns
Input clock duty ratio *2	CL	t_{CLD}		20	—	80	%
Input clock rise time (20% to 80%)		t_r		—	—	15	ns
Input clock fall time (20% to 80%)		t_f		—	—	15	ns
Input clock cycle(1)		t_{CLF}	1chip usage	770	—	—	ns
Input clock L pulse width(1)		t_{WLCL}		200	—	—	ns
Input clock H pulse width(1)		t_{WHCL}		200	—	—	ns
Input clock cycle(2)		t_{CLF}	Master/slave usage	1400	—	—	ns
Input clock L pulse width(2)		t_{WLCL}		700	—	—	ns
Input clock H pulse width(2)		t_{WHCL}		700	—	—	ns

10.4.3 S1D15719D12B000

Table 10.16 output Timing (in case of using built-in oscillator)

[V_{DD}=2.7V to 5.5V, Ta= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	-600	—	200	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		-600	—	200	ns
SYNC delay time	SYNC	t_{DSYNC}		-600	—	200	ns

Table 10.17 output Timing (in case of using external clock)

[V_{DD}=2.7V to 5.5V, Ta= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50pF	100	—	900	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		100	—	900	ns
SYNC delay time	SYNC	t_{DSYNC}		100	—	900	ns

Table 10.18 Input Timing

[V_{DD}=2.7V to 5.5V, Ta= -40 to 95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		0	—	t_{WLCL}	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{DF2}		0	—	t_{WLCL}	ns
SYNC delay time	SYNC	t_{DSYNC}		0	—	t_{WLCL}	ns
Input clock duty ratio *2	CL	t_{CLD}		20	—	80	%
Input clock rise time (20% to 80%)		t_r		—	—	15	ns
Input clock fall time (20% to 80%)		t_f		—	—	15	ns
Input clock cycle(1)		t_{CLF}	1chip usage	800	—	—	ns
Input clock L pulse width(1)		t_{WLCL}		400	—	—	ns
Input clock H pulse width(1)		t_{WHCL}		400	—	—	ns
Input clock cycle(2)		t_{CLF}	Master/slave usage	1800	—	—	ns
Input clock L pulse width(2)		t_{WLCL}		900	—	—	ns
Input clock H pulse width(2)		t_{WHCL}		900	—	—	ns

*1: The timing t_{CLF}, t_{WLCL}, t_{WHCL} is defined based on 50% of V_{DD} or V_{DI}.

*2: All the timing except t_{CLF}, t_{WLCL}, t_{WHCL} is defined based on 20% and 80% of V_{DD} or V_{DI}. CL output / input voltage is between V_{DD} and V_{SS}, FR, F1, F2 and SYNC output / input is between V_{DI} and V_{SS}.

*3: CL duty ratio is defined as $t_{CLD} = \frac{t_{WHCL}}{t_{CLF}} \times 100[\%]$ or $t_{CLD} = \frac{t_{WLCL}}{t_{CLF}} \times 100[\%]$.

It is necessary to meet t_{WLCL} and t_{WHCL} specification in any case.

*4: A signal beyond the specification has no problem for the functionality, but t_{CLF}, t_{WLCL} and t_{WHCL} always should be kept.

10.5 Reset Input timing

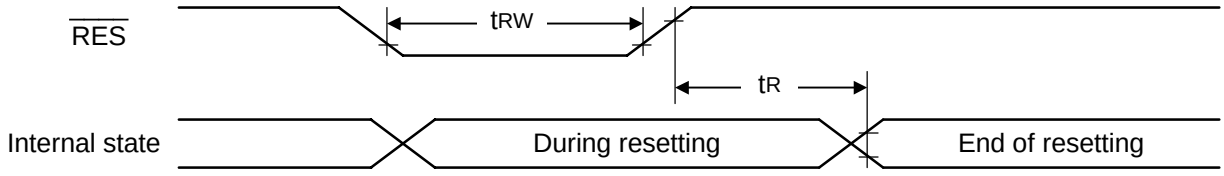


Fig.10.5

10.5.1 S1D15719D10B000

Table 10.19

[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	—	1	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1	—	—	

10.5.2 S1D15719D11B000

Table 10.20

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	—	1	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1	—	—	

10.5.3 S1D15719D12B000

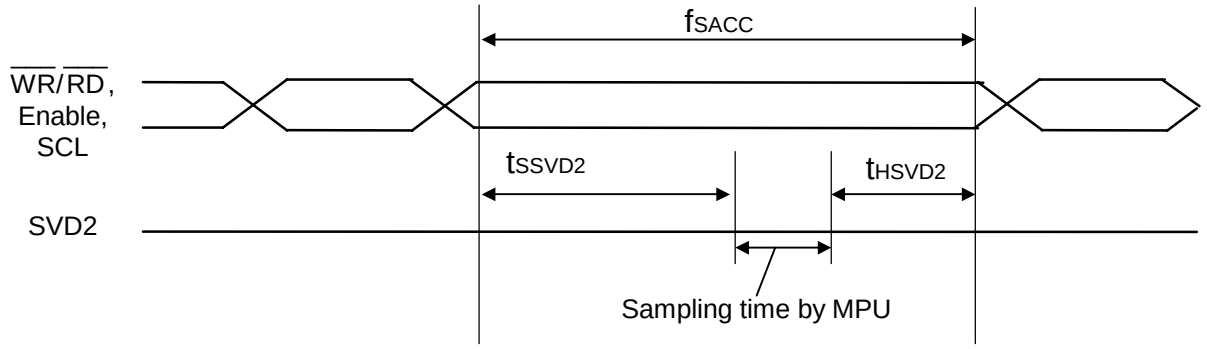
Table 10.21

[V_{DD}=2.7V to 5.5V, T_a= -40 to +95°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	—	1	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1	—	—	

*1: Timing is entirely specified with reference to 20% and 80% of V_{DD}.

10.6 Temperature Sensor Measuring Timing



[V_{DD}=2.7V to 5.5V, T_a= -40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
MPU access cycle *1	$\overline{WR}/\overline{RD}$ (80 series MPU) Enable (68 series MPU) SCL (Serial interface)	f_{SACC}		—	—	0	Hz
Sampling setup time *2	SVD2	t_{SSVD2}		1	—	—	ms
Sampling hold time *3	SVD2	t_{HSVD2}		0	—	—	ms

*1: Stop an access from MPU (for 80 series MPU: input from the $\overline{WR}$ or $\overline{RD}$ pin, for 68 series MPU: input from the Enable pin, and for the serial interface: input from the SCL pin) during detection of the SVD2 output.

*2: Wait time until SVD2 sampling is enabled after stopping access from MPU. Apply when the temperature sensor is set to ON beforehand. When setting the temperature sensor to ON after stopping access from MPU, provide a given output voltage setup time.

*3: Wait time until access from MPU can be started after completion of SVD2 sampling by MPU.

11. MPU INTERFACE (Reference Example)

The S1D15719 Series can be connected to the 80 series MPU and 68 series MPU. Use of a serial interface allows operation with a smaller number of signal lines.
You can expand the display area using the S1D15719 Series as a multi-chip. In this case, the IC to be accesses can be selected individually by the chip select signal. After initialization by the $\overline{RES}$ pin, each input terminal of the S1D15719 Series must be placed under normal control.

(1) 80 series MPU

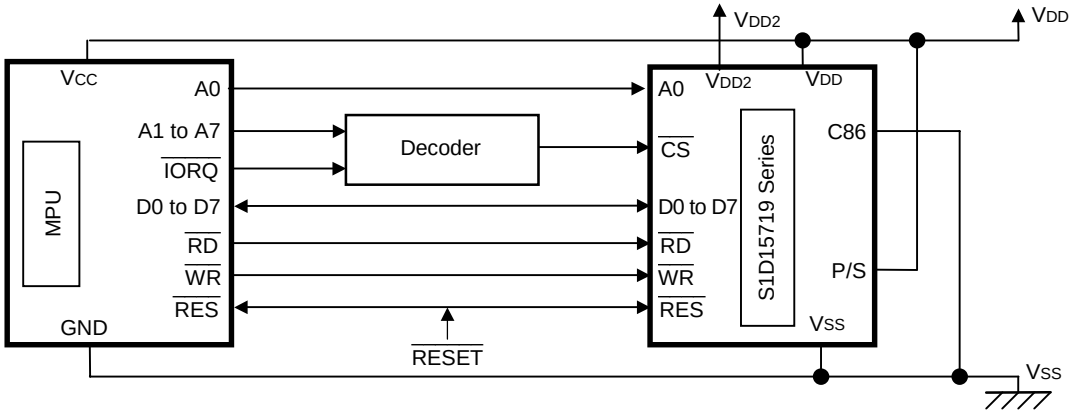


Fig.11.1 80 series

(2) 68 series MPU

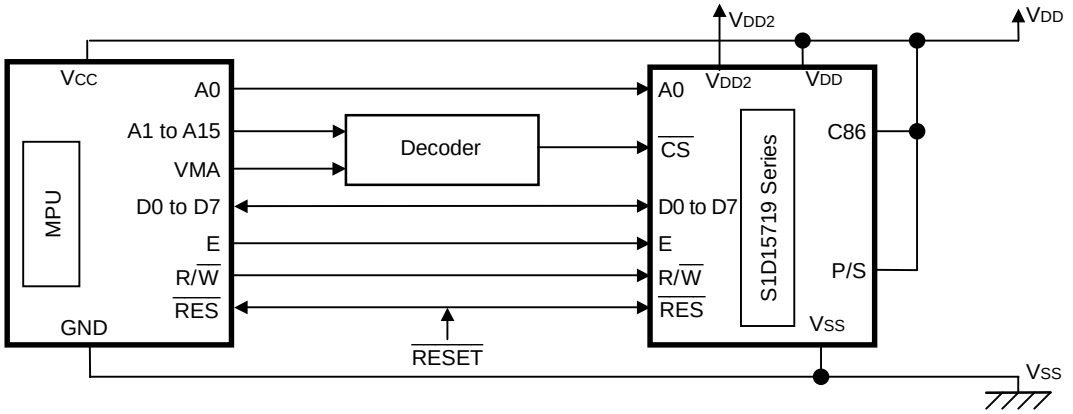


Fig.11.2 68 series

(3) Serial interface

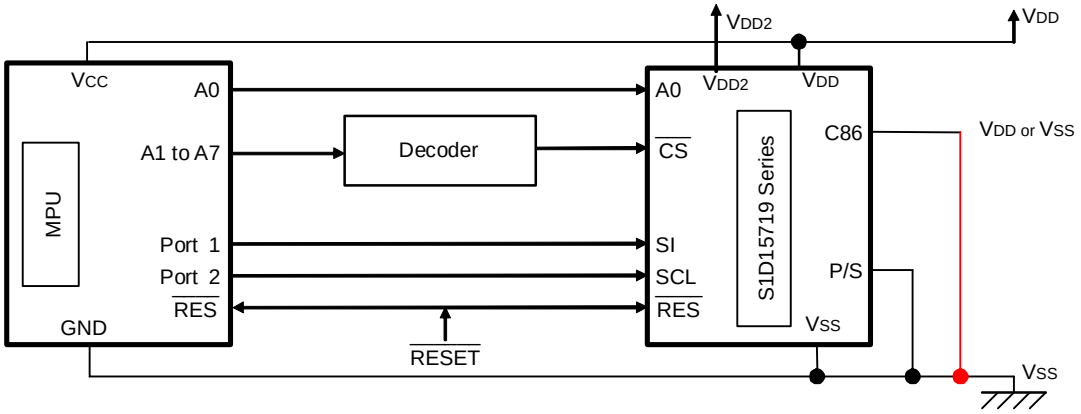


Fig.11.3 Serial interface control

12. CONNECTION BETWEEN LCD DRIVERS (Reference Example)

You can easily expand the liquid crystal display area using the S1D15719 Series as a multi-chip. In this case, use the same model (S1D15719/S1D15719) as the master and slave systems.

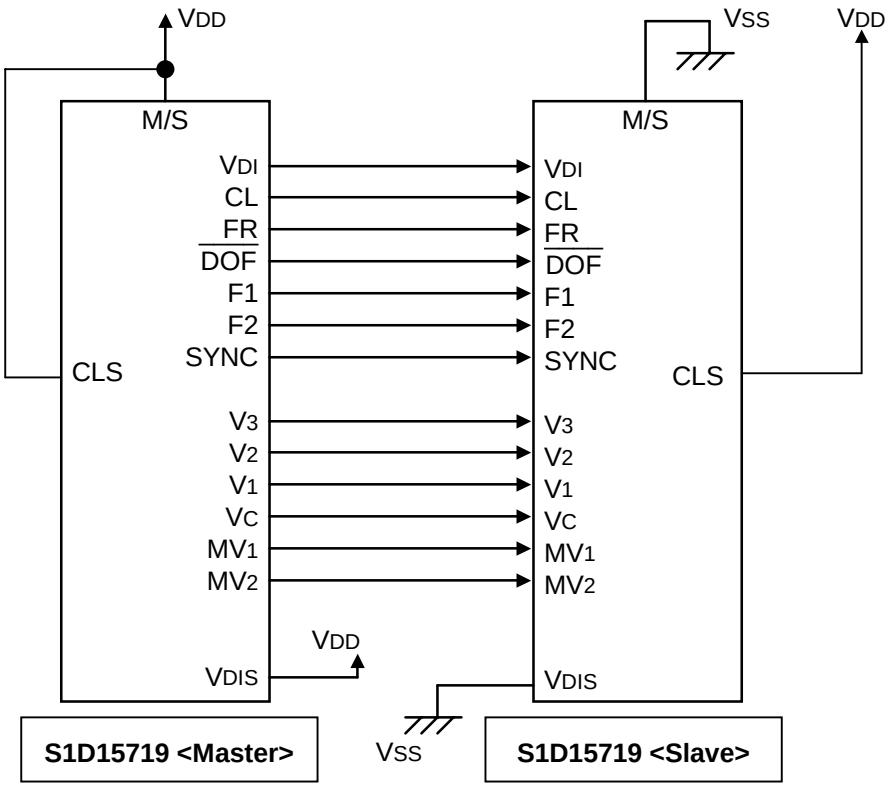


Fig.12.1 Master/slave connection example

13. LCD PANEL WIRING (Reference Example)

You can easily expand the liquid crystal display area using the S1D15719 Series as a multi-chip. In the case of multi-chip configuration, use the same models.

(1) Example of 1-chip configuration

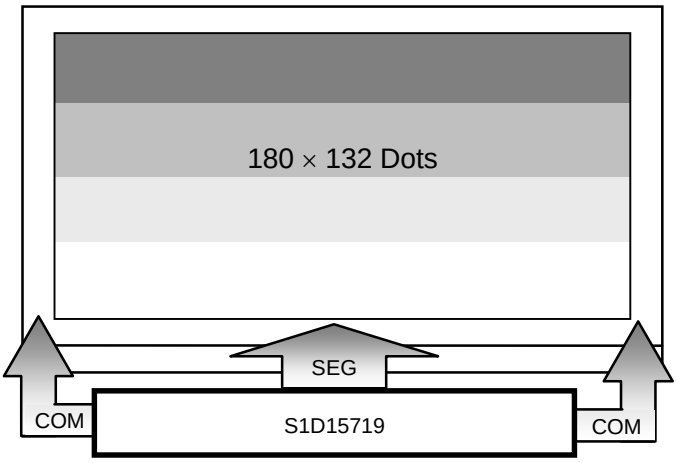


Fig.13.1 An Example of 1-chip Drive

(2) Example of 2-chip configuration

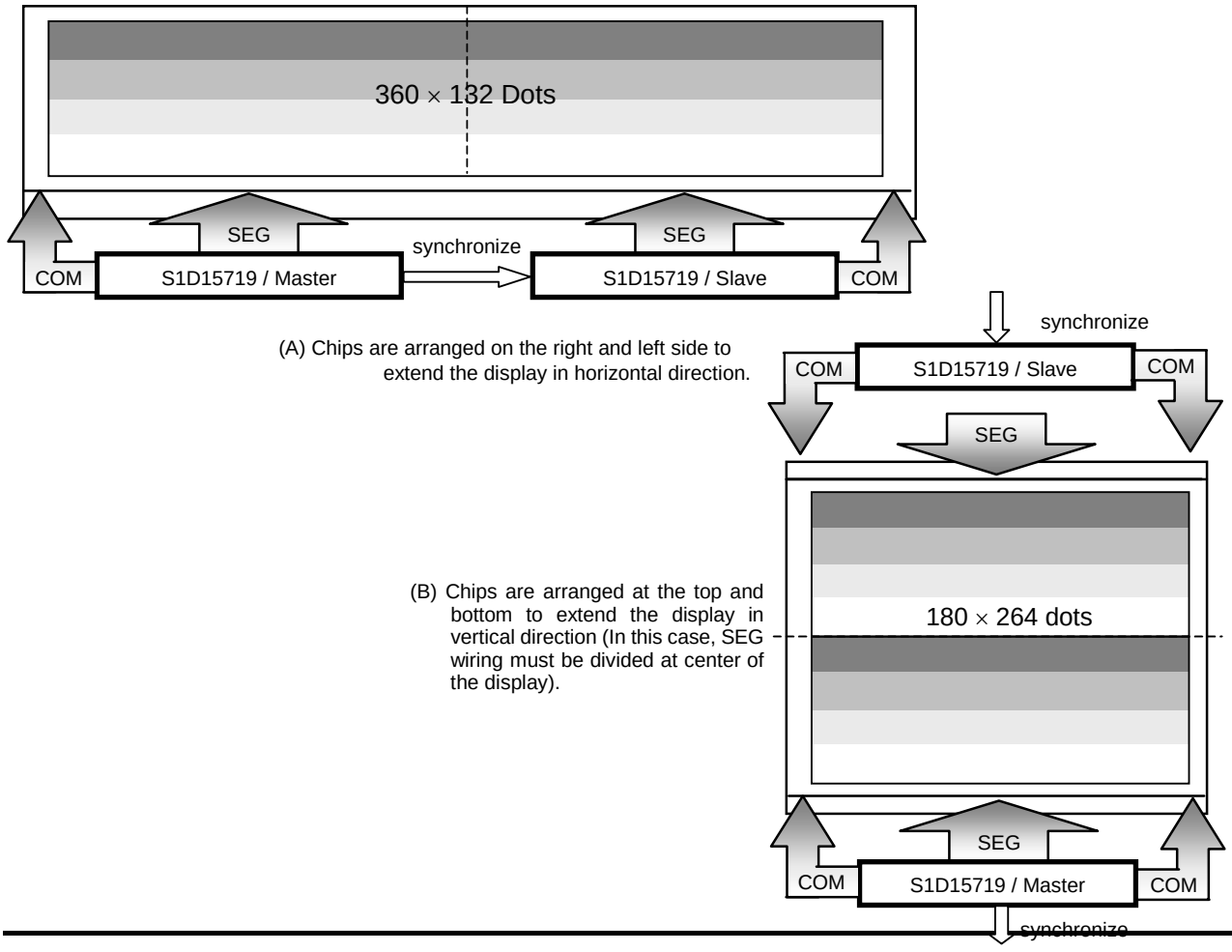


Fig.13.2 An Example of 2-chip Drive

14. CAUTIONS

Cautions must be exercised on the following points when using this Development Specification:

1. This Development Specification is subject to change for engineering improvement.
2. This Development Specification does not guarantee execution of the industrial proprietary rights or other rights, or grant a license. Examples of applications described in This Development Specification are intended for your understanding of the Product. We are not responsible for any circuit problem or the like arising fromt the use of them.
3. Reproduction or copy of any part or whole of this Development Specification without permission of our company, or use thereof for other business purposes is strictly prohibited.

For the use of the semi-conductor, cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

(1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
(2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
(3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC.

REVISION HISTORY

Date	Rev.	Page	Type	Description
2005/5/6	1.0	All	New	New enactment
2005/11/8	1.1	P3	Corrected	"$\overline{DOF}$" was corrected to "$\overline{DOF}$" in Section 3 (Block Diagram).
		P9	Added	Text "When using this IC in multi-chip (master and slave) configuration" has been added to the V_{DI} power pin in Section 5.1.
		P10	Corrected	The number of pins was corrected from "2 pins each" to "3 pins each" for V_3, V_2, V_1 and other power pins in Section 5.1.
		P11	Corrected	Text "across V_{SS}" was corrected to "across V_{DD2} or V_{SS}" for V_{125} and V_{OUT2} pins in Section 5.2 (LCD Power Supply Current Pin).
		P15	Corrected	6.1.3 Serial Interface Text "display data" was corrected to the "display data or command parameters."
		P18	Corrected	6.2.2 Display of gray-scale Text "gray-scale set" was corrected to "gray-scale pattern setup."
		P24	Modified	6.7 Power Supply Circuit Sentence "This circuit is enabled only when the master operation mode is turned on." was deleted, and "Bits D3 and D2 are only enabled in the slave operation mode." was added.
		P28	Corrected	Item ④ of 6.7.1 "Blocks of power supply circuit and combinations of their operations" Text "LCD voltage selection command" was corrected to "V_3 voltage regulating command."
		P31	Corrected	6.7.3.2 Double-boosting circuit Text "across V_{SS}" was corrected to "across V_{DD2} or V_{SS}." Also, "across V_{DD2}" was corrected to "across V_{DD2} or V_{SS}."
		P32	Corrected	In Formula 6.1, text "LCD voltage selection command" was corrected to "V_3 voltage regulating command."
		P34	Corrected	6.7.6 Temperature gradient selection circuit Text "temperature gradient selection command" was corrected to "temperature gradient setting command." Verb "select" was corrected to "set." Text "liquid crystal voltage change command" was corrected to "V_3 voltage regulating command."
		P36	Deleted	The open V_{DD2} pin was deleted from Figures 6.17 and 6.18.
		P37	Corrected	6.8.9 Precautions of V_{DD2} power supply circuits Text "V_{OUT}" and "V_{OUT} power" were corrected to "V_{OUT1} and V_{OUT2}."
		P40	Corrected	Item 11. n-line reverse drive register Test "(D4,D3,D2,D1,D0)=(0,0,0,0,0)" was corrected to "(D5,D4,D3,D2,D1,D0)=(0,0,0,0,0,0)." Item 12. Display mode Text "All ON during dummy selection period" was added.
		P40	Corrected	Item 28. MLS drive selecting register Text "(D3=1) (Non-dispersion drive)" was corrected to "(D4, D3)=(0, 1) (n-line inversion, frame inversion overlap OFF, and non-dispersion drive)."
		P42	Corrected	(5) Display Start Line Set Line address 7FH was corrected to 7CH on the table of paragraph (i).
		P43	Added	(II) When the display mode is binary Sentence "Register setting at 42H or higher is not allowed." was added.

Date	Rev.	Page	Type	Description
2005/11/8	1.1	P44	Added	(6) Page Address Set Sentence “Register setting at 21H or higher is not allowed.” was added. (7) Column Address Set Sentence “Register setting at B4H or higher is not allowed.” was added.
		P46	Added Corrected	(12) n-line Inversion Drive Register Set Sentence “Register setting at 21H or higher is not allowed.” was added. (14) Display Mode Set Text “Display all lighting ON” was corrected to “Display all lighting OFF.”
		P47	Added	(15) Gray-scale Pattern Set The inhibited gray-scale bit setup was added to the notes under the table.
		P48	Added	(16) Number of Display Lines Set Paragraph “Number of Display Lines Register Set” Sentence “Register setting at 21H or higher is not allowed.” was added. Paragraph “Start Point (Block) Register Set” Sentence “Register setting at 21H or higher is not allowed.” was added.
		P49	Corrected	(17) Read Modify Write Text “page address command and” was added under the table.
		P55	Corrected	(24) LCD Bias Set On the table defining the relationship between the register set and the bias ratio: The register set values for bias ratios 1/9 and 1/8 were corrected.
		P56	Corrected	(25) Electronic Volume On the table defining the relationship between the register set and V_3 value: “(0,0,0,0,0,0,0,0,0)” was corrected to “(0,0,0,0,0,0,0,0).”
		P57	Added Corrected	(26) Discharge ON/OFF Notes in V_{OUT2} and V_{OUT1} connection example were added to Figure 7.6. Text “between V_{OUT1} and V_{DD2}” was corrected to “between V_{OUT1} and V_{DD2} and between V_{OUT2} and V_{125}.” (27) Power Saving Sentence “If an external oscillator circuit is used, the built-in booster circuit shall not stop during Power Saving.” was added. Text “Except digital converter” was deleted from paragraph (4).
		P58	Corrected	(27) Power Saving Text “while the power save mode is turned on” was corrected to “during power saving.”
		P59	Corrected	Typos in Japanese language (word “possible”) were corrected. It does not affect on the English text.
		P60	Corrected	(31) MLS drive method select Text “MLS-drive method selection” was corrected to “MLS drive method selection.” On the lower table, the “n-line frame inversion overlap ON and OFF” of the “Drive method” were corrected. Also, value (1, 1) was corrected to (0, 1) in the notes.
		P61	Corrected	(31) MLS drive method select Text “built-in oscillation circuit command” was corrected to “clock frequency selection command.”
		P62	Corrected	(12) n-line Inversion Drive Register Set D6 and D5 values of the “Command code” were corrected.

Date	Rev.	Page	Type	Description
2005/11/8	1.1	P64	Added	(1) Initial setup in Section 7.3 “Instruction Setup Example (Reference)” Decision box “Function setup by command entry” Item (3) “MLS drive method selection” was added under Item (16). Item (28) “Temperature gradient setup *9” was added under item (25).
		P67	Corrected	(4) When changing number of display lines Decision box “Function setup by command entry” Item (20) “Built-in oscillation circuit frequency select” was corrected to “clock frequency selection.” A reference to Note 3 was added to Item (12).
		P70	Corrected	9. DC Characteristics On Table 9.2, minimum value 5.6 of V_3 voltage was corrected to 11.0 volts.
		P71	Corrected	In Note 2, name “V_{DD2}” was corrected to “V_{DI}.” Also, text “see Fig.9.6” was corrected to “see Fig.9.2.” In Note 3, the name of pin VDIS was added. In Note 4, the name of pins ERR and TEST5 was added. In Note 5, the name of pin VDIS was added. In Note 6, the name of pin TEST5 was added.
		P73	Corrected	On Table 9.9, symbol “x” of the “1st booster factor” was deleted. 9.2 Current Consumption under Power Saving Mode On Table 9.11, condition “VDIS=LOW” was corrected to “VDIS=HIGH.” Also, condition “VDIS=3V” was added. On Table 9.12, symbol “IDDS1” was corrected to “IDDS2.” Also, condition “VDIS=HIGH” was corrected to “VDIS=LOW.”
		P74	Added	9.3.1 While access from MPU is taking place Figure title of “Fig.9.1” was added. 9.3.2 Operating voltage range of V_{DI} system and V_3 system Figure title of “Fig.9.2” was added.
		P75	Corrected	9.3.3 Liquid crystal frame frequency f_{FR} On Table 9.13, a reference to “page 50” was corrected to “page 52.” 9.4 Characteristics of Thermal Sensor On Table 9.14, a reference to Note 4 was added to the “Applicable pins” column of the “Output Voltage” item.
		P76	Modified	In Note 2, the formula number of “Formula 2” and the figure number of “Fig.9.3” were added. The second half of Note 3 was moved to Note 4. Also, the note on the connection of stabilizing capacity to SV_{D2} was added.
		P77 to P80	Corrected	The title of Section 10 was changed to “Timing Characteristics.”
		P77	Corrected	10.1 System path read/write characteristics 1 In Fig.10.1, signals “t_{CCLRC}, t_{CCLWC}, t_{CCHRC}, t_{CCHWC}” were corrected to “t_{CCLR}, t_{CCLW}, t_{CCHR}, t_{CCHW}” respectively. Also, signal “t_{DH8C}” was deleted.
		P79	Corrected	10.2 System path read/write characteristics 2 In Fig.10.2, signals “t_{EWHRC}, t_{EWHWC}, t_{EWLRC}, t_{EWLWC}” were corrected to “t_{EWHR}, t_{EWHW}, t_{EWLR}, t_{EWLW}” respectively. Also, signal “t_{DH6C}” was deleted.
		P81	Added	10.3 Serial Interface On Table 10.3, pulse names “SCL HIGH” and “SCL LOW” were corrected to “SCL H” and “SCL L” respectively. Also, the operation notes in the timing exceeding the “t_r” and “t_f” limits were added.

Date	Rev.	Page	Type	Description
2005/11/8	1.1	P82	Modified	10.4 Display Control Input and Output Timing Typos of the timing chart were corrected, and the input timing standards were changed. On Table 10.5, text “Low-level pulse width” was corrected to “External clock LOW pulse width” and “High-level pulse width” was corrected to “External clock HIGH pulse width.” Also, the operation notes in the timing exceeding the “t_r” and “t_f” limits were added.
		P83	Corrected	In Note 3, signal “t_{CLK}” was corrected to “t_{CLF}.”
		P84	Added	10.6 Temperature Sensor Measuring Timing A reference to Notes 1, 2 and 3 was added to each item of the table.
		P85	Deleted	(3) Serial interface Pins “D0 to D7” were deleted from Fig.11.3.
		P86	Added	12. Connection between LCD Drivers (Reference Example) The signal line to V_{DI} pin was added to Fig.12.1. Also, the usage notes of V_{DI} and built-in power supply were added.
		P87	Added	Word “synchronize” was added to Fig.13.2.
2007/5/11	2.0	P2	Added	Added new models – S1D15719D11B and S1D15719D12B.
		P3	Added	Added note that ERR pin is NC about D11B and D12B.
		P4	Added	Added comment “From bump side” and Die number vs Part number table in 4.1 Chip assignment.
		P5	Added	Added note that ERR pin is NC about D11B and D12B in 4.3 Pad center coordinates.
		P13	Added	Added note that ERR pin is NC about D11B and D12B in 5.3 System bus connection pins.
		P15	Added	Added “Temperature sensor output read” command in Table 6.3.
		P16	Added	Added “Temperature sensor output read” in 6.1.3 Serial interface.
		P22	Added	Added “Concerning D11B and D12B, the ERR pin is NC. (The register read by Status read command is possible.” in 6.5 Operation mode detection circuit.
		P31, 32	Corrected	Corrected “Equation 6.1 to Table 6.11” in 6.7.4.1 V3 voltage output range.
		P32	Corrected	Corrected V3 voltage output range maximum value. 19.05V to 19.11V in register value (0, 1, 0) and 20.00V to 20.06V in (0, 1, 1). Because of mis-caliculation. (No change the equations.)
		P34	Corrected	Corrected V3 voltage output range maximum value in example in 6.7.6 Temperature gradient selection circuit.

Date	Rev.	Page	Type	Description
2007/5/11	2.0	P35 to 39	Added	Added S1D15719D11B / S1D15719D12B circuit in examples of peripheral circuits of power supply circuit.
		P35 to 36	Changed	Changed capacitor connection in V3 to MV2 , from parallel to serial.
		P37	Added	Added note about capacitors connection around V3, to MV2.
		P40	Added	Added comment that “Non polarity capacitors can be applicable”. In table 6.14.
		P41	Added	Added 6.10.2 Digital converter element
		P42	Added	Added “Digital value is not affected by ITO Resistance R”. Change fig. number Fig 6-12 to Fig 6-34
		P43	Changed	Changed register value of 17 oscillation frequency register : (D3,D2,D1,D0)=(0,0,0,0) to (0,1,0,0) in 6.11 Reset circuit.
		P49	Changed	Changed settable maximum value from 128 to 132 in (12) n-line inversion drive register set.
		P50	Changed	Changed (P3,P2,P1,P1) = (0,0,1,0) and (0,0,1,1) to “non settable” in Gray scale bits(1,0) in (15) gray scale pattern set.
		P58	Corrected	Corrected V3 voltage output range maximum value. 19.05V to 19.11V in register value (0,1,0) and 20.00V to 20.06V in (0,1,1) in (23) V3 Voltage Regulation Circuit.
		P59	Added	Added section number 7.3 in (25)Electronic Volume.
		P63	Deleted	Deleted description of P1, P0 in (31) MLS drive method select.
		P64	Added	Added new command (33) Temperature sensor output read.
		P66	Added	Added new command (33) Temperature sensor output read in 7.2 Table of Commands.
		P67	Added	Added (30) Temperature sensor ON/OFF command and note *10 in (1) Initial setup in 7.3 Instruction Setup Example
		P69	Added	Added (26) Discharge OFF /(18) End command and note *5/*6 in (3) Refresh.
		P70	Added	Added control sequence when using external LCD voltages in (4) When changing number of display lines.
		P72	Added	Added control sequence when using external clock in (5) Power OFF.
		P72	Changed	Changed “RES pin = High” to “RES pin = Low” in (5) Power OFF.
		P73	Added	Added S1D15719D11B and S1D15719D12B in 8. Absolute Maximum Ratings.
		P73	Added	Added comment in Note 2 in 8 Absolute Maximum Ratings.
		P74,75	Added	Added Hysteresis voltage and Note *4 , add external clock input value and note *11. Add comment that “Except ERR pin of the S1D15712D12B) in note *5. in 9. DC characteristics
		P77,78	Corrected	Corrected V3 voltage from 10.0V to 11.0V in Table 9.3 to Table 9.10.
		P81	Corrected	Corrected applied pins of Operation current from VDD to VDI. In 9.4.1 Analog voltage output characteristics.

Date	Rev.	Page	Type	Description
2007/5/11	2.0	P82	Corrected	Corrected from “6.10.2 paragraph” to “6.10.3 paragraph”
		P82	Added	Added note *5 In 9.4.1 Analog voltage output characteristics.
		P83	Added	Added 9.4.2 Digital conversion characteristics.
		P85 to 96	Added	Added characteristics of the S1D15719D11B and S1D15719D12B.
		P88	Correct	Correct Enable High Pulse Width tEWHR from 500ns to 950ns in table 10.4 in 68 system CPU. (Typo)
		P92 to 95	Changed	Divided timing specification by using built-in oscillator and external clock. Divided input timing specifications by 1chip usage and Master / slave usage. In 10.4 Display Control Input and Output timing, changed note *1 from “all the timing defined based on 20% and 80% of VDD” to “all the timing defined based on 50% of VDD.
		P96	Added	Added reset timing specifications of the S1D15719D11B and S1D15719D12B in 10.5 Reset Input timing.
		P98	Corrected	Corrected C86 pin connection from VDD/VSS to VSS in (3) Serial interface of 11. MPU interface.

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
2580 Orchard Parkway
San Jose , CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

SALES OFFICES
Northeast
301 Edgewater Place, Suite 210
Wakefield, MA 01880, U.S.A.
Phone: +1-800-922-7667 FAX: +1-781-246-5443

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON Electronic Technology Development (Shenzhen) LTD.
12/F, Dawning Mansion, Keji South 12th Road,
Hi- Tech Park, Shenzhen
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

GUMI OFFICE
2F, Grand B/D, 457-4 Songjeong-dong,
Gumi-City, KOREA
Phone: +82-54-454-6027 FAX: +82-54-454-6093

SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

Document Code: 405189105
First Issue June 2005
Printed May 2007 in JAPAN