■ INTRODUCTION

RW1062 is a LCD driver & controller LSI which is fabricated by low power CMOS technology.
It can display 2 lines x 24 (5 x 8 dot format) characters or 4 lines x 20 (5 x 8 dot format) characters. It is ideal for multi-language application. Standard code RW1062-0A-001 can support up to 256 fonts. Customized codes are available.

■ FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal drivers: 34 common and 100 segment for 4 line display, 1/33 duty (NW=1).
  18 common and 120 segment for 2 line display, 1/17 duty (NW=0).
- Easy interface with 4-bit or 8-bit MPU or 4 lines / 3 lines / IIC serial peripheral interface (SPI)
- 5 x 8 dot matrix font
- Bi-directional shift function
- Double height display function
- Common scan direction selectable
- Voltage converter for LCD drive voltage: 8 V max (2 times / 3 times)
- Various instruction functions
- Automatic power on reset
- CGRAM/CGROM display selectable

■ FEATURES

- Internal Memory
- Character Generator ROM (CGROM): 10,240 bits (256 characters x 5 x 8 dot)
- Character Generator RAM (CGRAM): 64 x 5 bits (8 characters x 5 x 8 dot)
- Icon RAM (SEGRAM): 16 x 5 bits (80 icons max.)
- Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
- Low power operation
- Power supply voltage range: 2.4 ~ 5.5 V (VDD)
- LCD Drive voltage range: 3.0 ~ 7V (V0 – VSS)
- CMOS process
- Programmable duty cycle: 1/17, 1/33 (refer to Table 1.)
- Internal oscillation circuit with built-in resistor
- Low power consumption
- Bare chip available

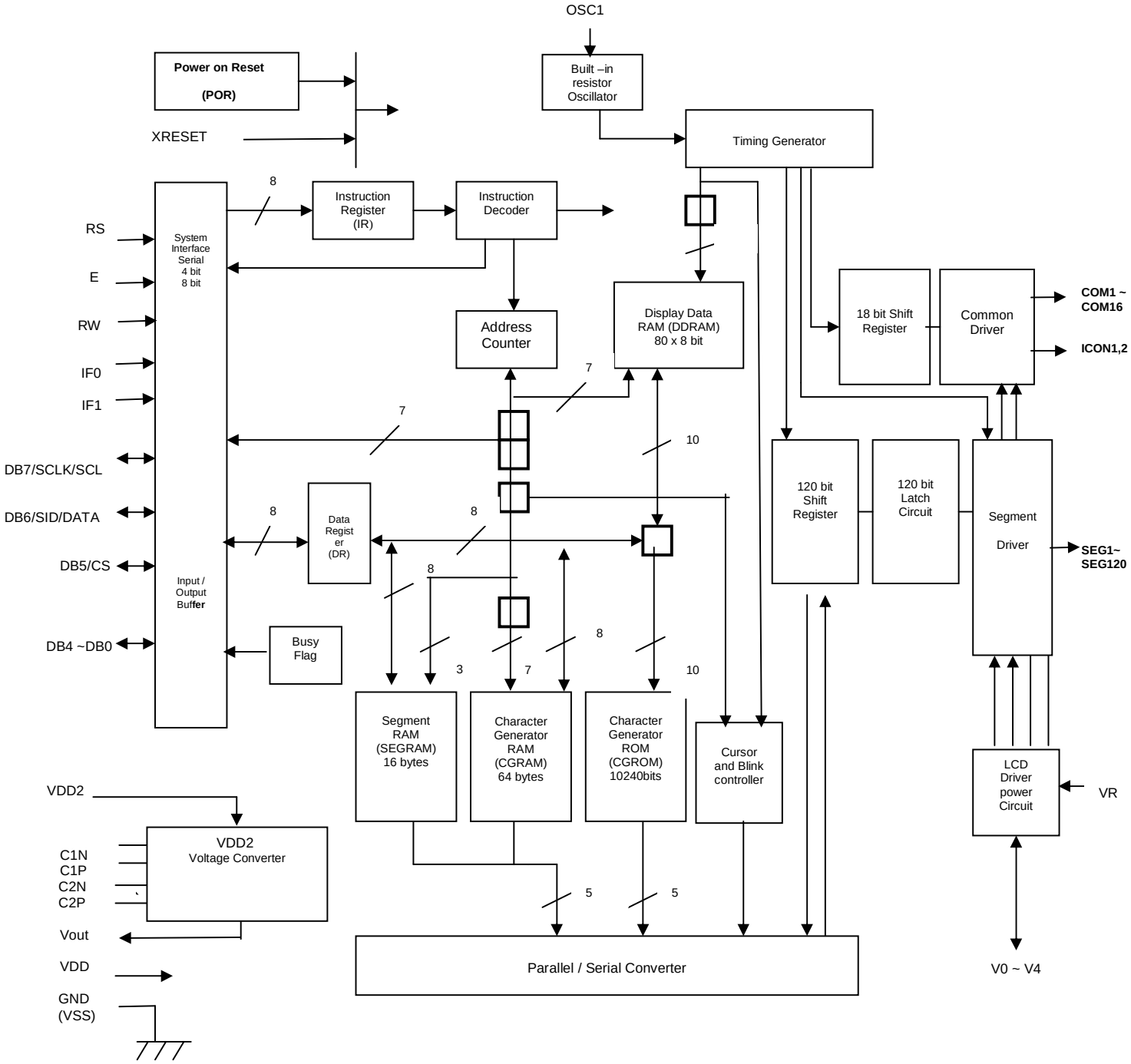
RW1062 Serial Revision History		
Version	**Date**	**Description**
1.0	2007/12/19	Add Interface standard circuit and font table.
1.1	2008/8/14	Add I/O Pin ITO Resister Limitation.
1.2	2009/11/13	Add 17、33 duty interface standard circuit.
1.3	2009/11/18	Pad34~171 Metal area changed.
1.3a	2010/2/5	Modify Page 6 Bump Pitch.

■ Programmable duty cycles

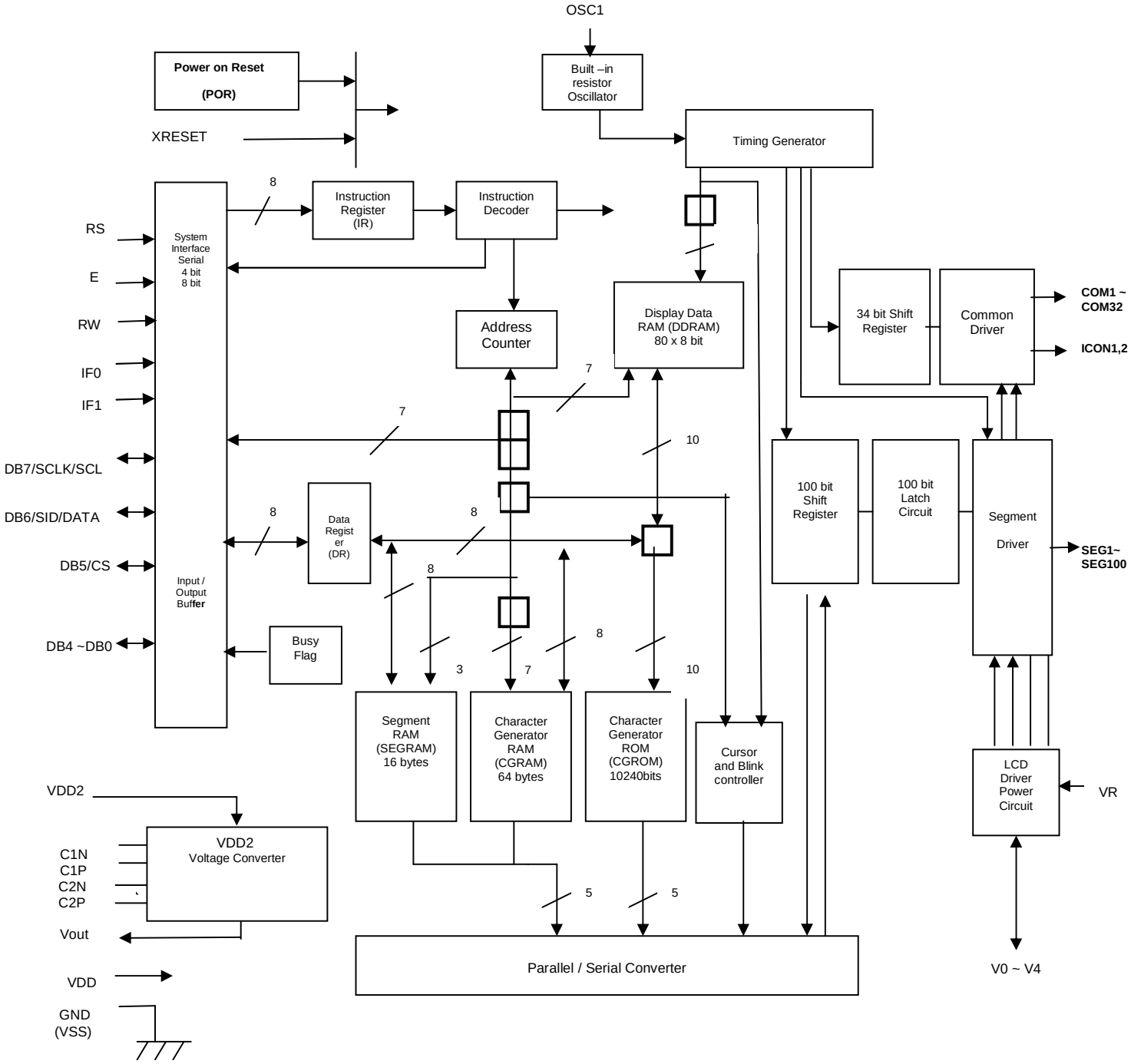
(Table 1)

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable characters	Possible icons
2	1/17	2 lines of 24 characters	80
4	1/33	4 lines of 20 characters	80

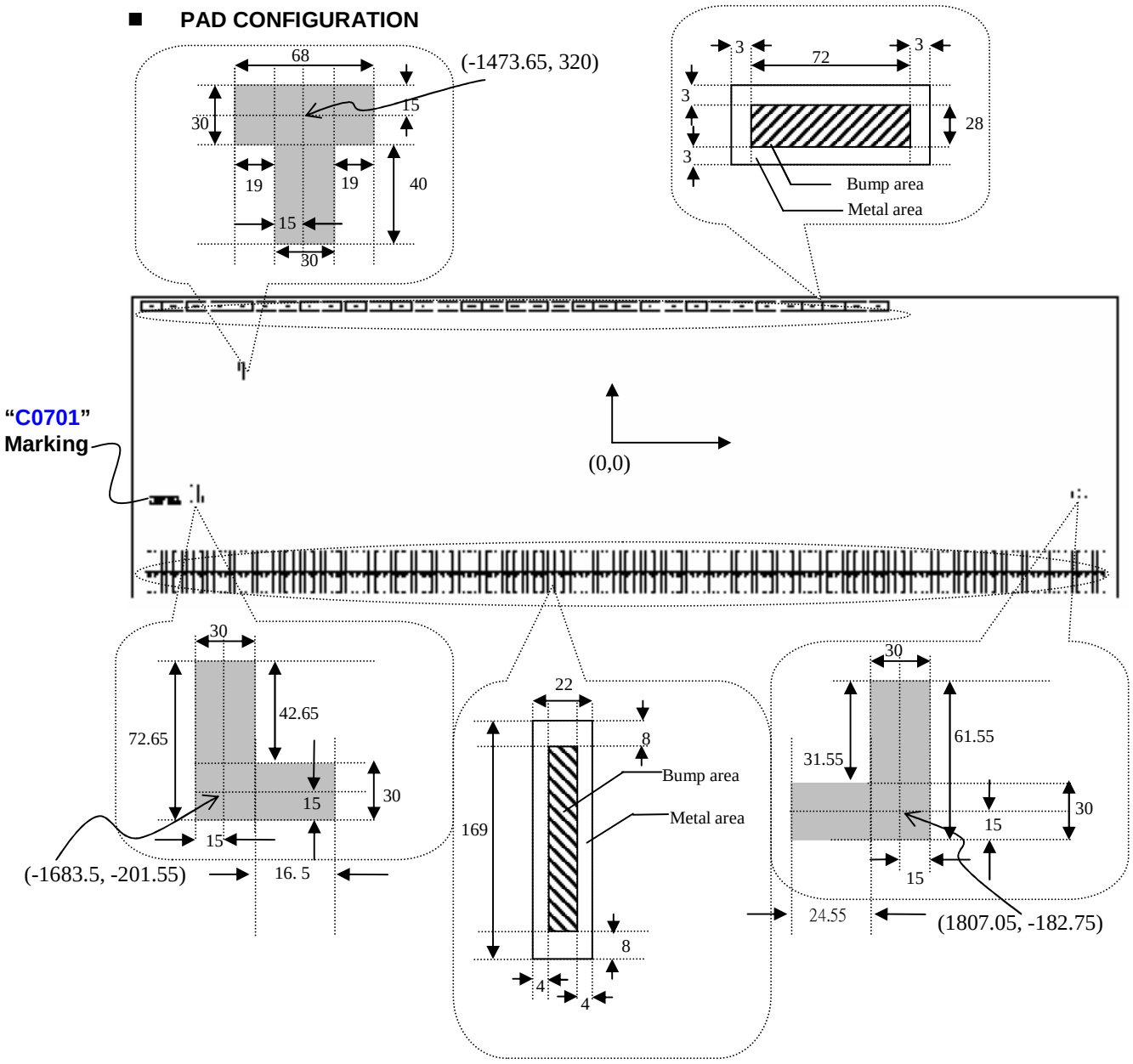
■ BLOCK DIAGRAM (For 1/17 Duty)



■ BLOCK DIAGRAM (For 1/33 Duty)

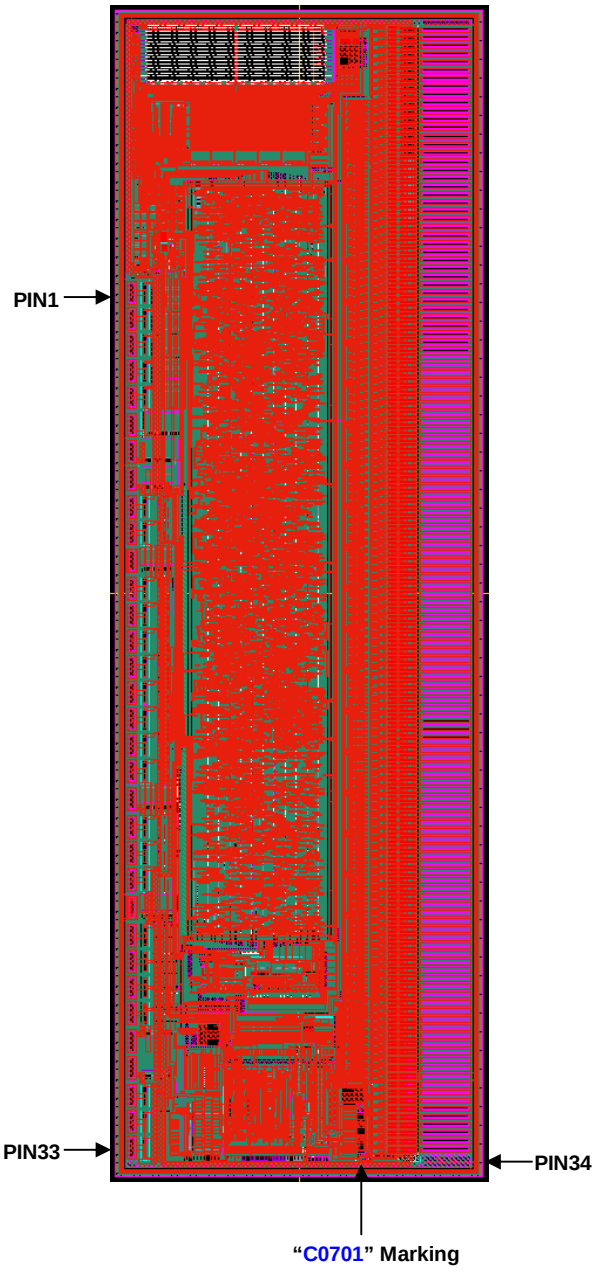


■ **PAD CONFIGURATION**



- **Chip Size: 3900 µm x 1220µm**
- **Chip thickness : 480µm**
- **Bump Pitch : 27.3µm (Min.)**
- **Bump Height: 15 µm (typ.)**
- **Bump Size :**
  - **Pad No.1~33: 72µm x 28 µm**
  - **Pad No.34~171 : 14µm x 153 µm**

■ CHIP LAYOUT



■ PAD LOCATION

Unit: um

Pad No.	Pin Name NW=0/NW=1	X	Y	Pad No.	Pin Name NW=0/NW=1	X	Y
1	VR	1004.05	556	46	SEG[4]/COM[4]	-1531.2	-488.5
2	C1N	917.05	556	47	SEG[5]/COM[3]	-1503.9	-488.5
3	C1P	830.05	556	48	SEG[6]/COM[2]	-1476.6	-488.5
4	C2P	743.05	556	49	SEG[7]/COM[1]	-1449.3	-488.5
5	C2N	656.05	556	50	SEG[8]/ICON[1]	-1422	-488.5
6	VOUT	562.55	556	51	SEG[9]/N.C	-1394.7	-488.5
7	VDD2	472.55	556	52	SEG[10]/N.C	-1367.4	-488.5
8	VDD	382.55	556	53	SEG[11]/SEG[1]	-1340.1	-488.5
9	IF1	288.75	556	54	SEG[12]/SEG[2]	-1312.8	-488.5
10	IF0	201.75	556	55	SEG[13]/SEG[3]	-1285.5	-488.5
11	VSS	108.25	556	56	SEG[14]/SEG[4]	-1258.2	-488.5
12	DB7	14.65	556	57	SEG[15]/SEG[5]	-1230.9	-488.5
13	DB6	-72.35	556	58	SEG[16]/SEG[6]	-1203.6	-488.5
14	DB5	-159.35	556	59	SEG[17]/SEG[7]	-1176.3	-488.5
15	DB4	-246.35	556	60	SEG[18]/SEG[8]	-1149	-488.5
16	DB3	-333.35	556	61	SEG[19]/SEG[9]	-1121.7	-488.5
17	DB2	-420.35	556	62	SEG[20]/SEG[10]	-1094.4	-488.5
18	DB1	-507.35	556	63	SEG[21]/SEG[11]	-1067.1	-488.5
19	DB0	-594.35	556	64	SEG[22]/SEG[12]	-1039.8	-488.5
20	VDD	-687.85	556	65	SEG[23]/SEG[13]	-1012.5	-488.5
21	E	-781.45	556	66	SEG[24]/SEG[14]	-985.2	-488.5
22	RW	-868.45	556	67	SEG[25]/SEG[15]	-957.9	-488.5
23	RS	-955.45	556	68	SEG[26]/SEG[16]	-930.6	-488.5
24	VSS	-1048.95	556	69	SEG[27]/SEG[17]	-903.3	-488.5
25	V4	-1142.25	556	70	SEG[28]/SEG[18]	-876	-488.5
26	V3	-1229.25	556	71	SEG[29]/SEG[19]	-848.7	-488.5
27	V2	-1316.25	556	72	SEG[30]/SEG[20]	-821.4	-488.5
28	V1	-1403.25	556	73	SEG[31]/SEG[21]	-794.1	-488.5
29	V0	-1496.55	556	74	SEG[32]/SEG[22]	-766.8	-488.5
30	VDD	-1583.55	556	75	SEG[33]/SEG[23]	-739.5	-488.5
31	XRESET	-1677.5	556	76	SEG[34]/SEG[24]	-712.2	-488.5
32	TESTP	-1764.5	556	77	SEG[35]/SEG[25]	-684.9	-488.5
33	OSC1	-1851.5	556	78	SEG[36]/SEG[26]	-657.6	-488.5
34	COM[8]/COM[16]	-1858.8	-488.5	79	SEG[37]/SEG[27]	-630.3	-488.5
35	COM[7]/COM[15]	-1831.5	-488.5	80	SEG[38]/SEG[28]	-603	-488.5
36	COM[6]/COM[14]	-1804.2	-488.5	81	SEG[39]/SEG[29]	-575.5	-488.5
37	COM[5]/COM[13]	-1776.9	-488.5	82	SEG[40]/SEG[30]	-548.4	-488.5
38	COM[4]/COM[12]	-1749.6	-488.5	83	SEG[41]/SEG[31]	-521.1	-488.5
39	COM[3]/COM[11]	-1722.3	-488.5	84	SEG[42]/SEG[32]	-493.8	-488.5
40	COM[2]/COM[10]	-1695	-488.5	85	SEG[43]/SEG[33]	-466.5	-488.5
41	COM[1]/COM[9]	-1667.7	-488.5	86	SEG[44]/SEG[34]	-439.2	-488.5
42	ICON[1]/COM[8]	-1640.4	-488.5	87	SEG[45]/SEG[35]	-411.9	-488.5
43	SEG[1]/COM[7]	-1613.1	-488.5	88	SEG[46]/SEG[36]	-384.6	-488.5
44	SEG[2]/COM[6]	-1585.8	-488.5	89	SEG[47]/SEG[37]	-357.3	-488.5
45	SEG[3]/COM[5]	-1558.5	-488.5	90	SEG[48]/SEG[38]	-330	-488.5

Note: TESTP is for testing purpose .When use internal oscillator, keep this pin opened.
If external clock used connect it to VDD.

Pad No.	Pin Name NW=0/NW=1	X	Y
91	SEG[49]/SEG[39]	-302.7	-488.5
92	SEG[50]/SEG[40]	-275.4	-488.5
93	SEG[51]/SEG[41]	-248.1	-488.5
94	SEG[52]/SEG[42]	-220.8	-488.5
95	SEG[53]/SEG[43]	-193.5	-488.5
96	SEG[54]/SEG[44]	-166.2	-488.5
97	SEG[55]/SEG[45]	-138.9	-488.5
98	SEG[56]/SEG[46]	-111.6	-488.5
99	SEG[57]/SEG[47]	-84.3	-488.5
100	SEG[58]/SEG[48]	-57	-488.5
101	SEG[59]/SEG[49]	-29.7	-488.5
102	SEG[60]/SEG[50]	-2.4	-488.5
103	SEG[61]/SEG[51]	24.9	-488.5
104	SEG[62]/SEG[52]	52.2	-488.5
105	SEG[63]/SEG[53]	79.5	-488.5
106	SEG[64]/SEG[54]	106.8	-488.5
107	SEG[65]/SEG[55]	134.1	-488.5
108	SEG[66]/SEG[56]	161.4	-488.5
109	SEG[67]/SEG[57]	188.7	-488.5
110	SEG[68]/SEG[58]	216	-488.5
111	SEG[69]/SEG[59]	243.3	-488.5
112	SEG[70]/SEG[60]	270.6	-488.5
113	SEG[71]/SEG[61]	297.9	-488.5
114	SEG[72]/SEG[62]	325.2	-488.5
115	SEG[73]/SEG[63]	352.5	-488.5
116	SEG[74]/SEG[64]	379.8	-488.5
117	SEG[75]/SEG[65]	407.1	-488.5
118	SEG[76]/SEG[66]	434.4	-488.5
119	SEG[77]/SEG[67]	461.7	-488.5
120	SEG[78]/SEG[68]	489	-488.5
121	SEG[79]/SEG[69]	516.3	-488.5
122	SEG[80]/SEG[70]	543.6	-488.5
123	SEG[81]/SEG[71]	570.9	-488.5
124	SEG[82]/SEG[72]	598.2	-488.5
125	SEG[83]/SEG[73]	625.5	-488.5
126	SEG[84]/SEG[74]	652.8	-488.5
127	SEG[85]/SEG[75]	680.1	-488.5
128	SEG[86]/SEG[76]	707.4	-488.5
129	SEG[87]/SEG[77]	734.7	-488.5
130	SEG[88]/SEG[78]	762	-488.5
131	SEG[89]/SEG[79]	789.3	-488.5
132	SEG[90]/SEG[80]	816.6	-488.5
133	SEG[91]/SEG[81]	843.9	-488.5
134	SEG[92]/SEG[82]	871.2	-488.5
135	SEG[93]/SEG[83]	898.5	-488.5
136	SEG[94]/SEG[84]	925.8	-488.5
137	SEG[95]/SEG[85]	953.1	-488.5
138	SEG[96]/SEG[86]	980.4	-488.5
139	SEG[97]/SEG[87]	1008	-488.5
140	SEG[98]/SEG[88]	1035	-488.5
141	SEG[99]/SEG[89]	1062	-488.5
142	SEG[100]/SEG[90]	1090	-488.5
143	SEG[101]/SEG[91]	1117	-488.5
144	SEG[102]/SEG[92]	1144	-488.5
145	SEG[103]/SEG[93]	1172	-488.5
146	SEG[104]/SEG[94]	1199	-488.5
147	SEG[105]/SEG[95]	1226	-488.5
148	SEG[106]/SEG[96]	1253	-488.5
149	SEG[107]/SEG[97]	1281	-488.5
150	SEG[108]/SEG[98]	1308	-488.5
151	SEG[109]/SEG[99]	1335	-488.5
152	SEG[110]/SEG[100]	1363	-488.5
153	SEG[111]/N.C.	1390	-488.5
154	SEG[112]/N.C.	1417	-488.5
155	SEG[113]/COM[17]	1445	-488.5
156	SEG[114]/COM[18]	1472	-488.5
157	SEG[115]/COM[19]	1499	-488.5
158	SEG[116]/COM[20]	1526	-488.5
159	SEG[117]/COM[21]	1554	-488.5
160	SEG[118]/COM[22]	1581	-488.5
161	SEG[119]/COM[23]	1608	-488.5
162	SEG[120]/COM[24]	1636	-488.5
163	COM[9]/COM[25]	1663	-488.5
164	COM[10]/COM[26]	1690	-488.5
165	COM[11]/COM[27]	1718	-488.5
166	COM[12]/COM[28]	1745	-488.5
167	COM[13]/COM[29]	1772	-488.5
168	COM[14]/COM[30]	1799	-488.5
169	COM[15]/COM[31]	1827	-488.5
170	COM[16]/COM[32]	1854	-488.5
171	ICON[2]	1881	-488.5

■ PAD DESCRIPTION

PAD(NO)	INPUT/OUTPUT	DESCRIPTION		INTERFACE
VDD,VDD2	-	Power supply	VDD is power pin for logical circuit(+3V,+5V) VDD2 is the power for voltage converting circuit	Power supply
VSS			0V (GND)	
V0-V4			Bias voltage level for LCD driving	
VR	Input	Reference input voltage	Reference voltage input to generate V0	-
SEG1-SEG120 (SEG1-SEG100)	Output	Segment output	Segment signal output for LCD drive	LCD
ICON1、ICON2	Output	Common output	Common signal output for LCD drive	LCD
COM1-COM16 (COM1-Com32)	Output	Common output	Common signal output for LCD drive	LCD
TESTP	Input	Clock source select	When use internal oscillator, keep this pin opened. If external clock used connect it to VDD.	-
OSC1	Input	Oscillator	When use internal oscillator, keep OSC1 pin connected to VDD. If external clock is used, connect it to OSC1.	External Clock input pin (OSC1)
C1N,C1P C2N,C2P	Input	External Capacitance input	To use the voltage converter (2 times/ 3 times), these pins must be connected to the external capacitance. (Please see page 36 for more detail)	External Capacitance
XRESET	Input	Reset pin	Initialized to Low	-
VOUT	Output	Two / Three times converter output	Voltage converter output voltage	-

■ PAD DESCRIPTION

PAD(NO)	INPUT/OUTPUT	DESCRIPTION		INTERFACE
RS	I	Register select	In bus mode, used as register selection input. When RS = “High”, Date register is selected. When RS = “Low”, Instruction register is selected.	MPU
E	I	Read. Write enable	In bus mode, used as read write enable signal.	MPU
RW	I	Read. Write	In bus mode, used as read / write selection input. When RW =”High”, read operation. When RW =”Low”, write operation.	MPU
DB0-DB3	I/O	Data bus 0~3	In 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode or serial mode, open these pins. .	MPU
DB4	I/O	Data bus 4	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order.	MPU
DB5/CSB	I/O	Data bus 5 / Chip select	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. In 3-SPI or 4-SPI serial mode, used as chip selection input. When CSB = “Low”, selected When CSB = “High”, not selected. (Low access enable)	MPU
DB6/SID	I/O	Data bus 6 / Serial input data	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. In 3SPI/4SPI and IIC interface modes, used for data input pin.	MPU
DB7/SCLK	I/O	Data bus 7 / Serial clock	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. In 3SPI/4SPI and IIC interface modes, used for serial clock input pin.	MPU
IF1,IF0	I	Interface select pins	IF1, IF0 0, 0 3-line SPI 0, 1 4-line SPI 1, 0 IIC 1, 1 6800 8/4-bit parallel interface	MPU

■ RW1062 I/O PIN ITO Resister Limitation

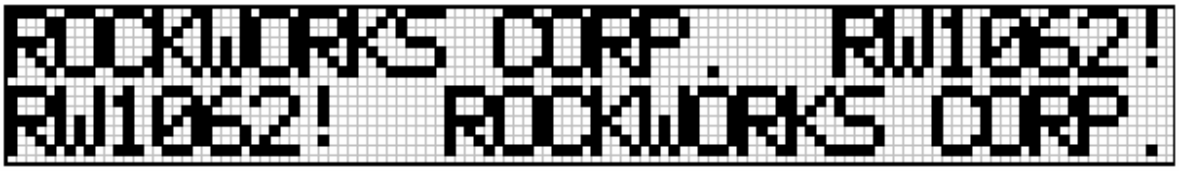
Pin Name	ITO
IF0,IF1,TESTP	NO Limitation
VDD,VDD2,VSS,VOUT ,VR	<100Ω
E,RW,RS,D0....D7,OSC1	<1KΩ
V0,V1,V2,V3,V4,CAP1P,CAP1N,CAP2P,CAP2N	<500Ω
/RES	<10KΩ

■ INSTRUCTION DESCRIPTION

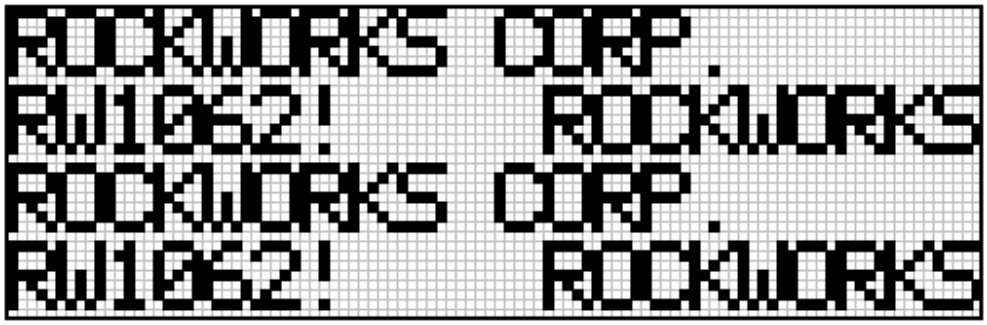
Instruction	RE	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	X	1	1	Read data								Read data into DDRAM/CGRAM/SEGRAM
Write display data	X	1	0	Write data								Write data into DDRAM/CGRAM/SEGRAM
Clear Display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM, and set DDRAM address to "00H" from AC
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Standby Mode	1	0	0	0	0	0	0	0	0	1	PD	Set standby mode bit. PD="1": standby mode set PD="0": standby mode disable
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D="1": increment I/D="0": decrement And entire display shift enable bit.
	1	0	0	0	0	0	0	0	1	SHL	BID	Segment bi-direction function BID="1": Seg 120/Seg100 --> Seg 1 BID="0": Seg 1--> Seg 120/Seg100 Common scan direction select SHL="1": reversal SHL="0": normal output
Display On/Off	0	0	0	0	0	0	0	1	D	C	B	Set Display /Cursor/Blink On/OFF D="1": display on D="0": display off C="1": cursor on C="0": cursor off B="1": blink on B="0": blink off
Extended display control	1	0	0	0	0	0	0	1	0	MW	NW	Memory select for b7-b4=0000 MW="1": CGROM select MW="0": CGRAM select Select display mode: NW="1": 4-line display NW="0": 2-line display
Cursor or Display shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift S/C="1": display shift S/C="0": cursor shift R/L="1": shift to right R/L="0": shift to left

Instruction	RE	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Function Set	0	0	0	0	0	1	INF	X	RE(0)	X	X	Set Interface Data Length IF="1": 8-bit interface IF="0": 4-bit interface Extension Register RE Double Height select (DH1,DH0)= (0,0) display normal (0,1) 1st line double height (1,0) 2nd line double height (1,1) 1st and 2nd lines both double height
	1	0	0	0	0	1	INF	X	RE(1)	DH1	DH0	
Set CGRAM Address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter
Set SEGRAM Address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter
Set DDRAM Address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter
Set Data Length	1	0	0	1	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Set data length for 3-line Serial Interface
Read Busy Flag and Address	X	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can know internal operation is ready or not by reading BF. The contents of address counter can also be read. BF="1": busy state BF="0": ready state
Analog instruction	1	0	0	0	0	0	1	0	BSTON	REGON	FOF	BSTON=0 booster off BSTON=1: booster on REGON=0: regulator off REGON=1: regulator on FOF=0 : follower on FOF=1: follower off

- Note : 1. When an MPU program with Busy Flag(DB7) checking is made, 1/ 2 FOSC (is necessary) for executing the next instruction by the " E " signal after the Busy Flag (DB7) goes to " Low ".
  2. "X" Don't care



2 lines x 24 (5 x 8 dot format)



4 lines x 20(5 x 8 dot format)

■ FUNCTION DESCRIPTION

● SYSTEM INTERFACE

This chip has all five kinds interface type with MPU: IIC, 3-SPI, 4SPI, 4-bit bus and 8-bit bus. Serial and bus (4-bit/8-bit) is selected by IF1P and IF0P input pins, and 4-bit bus and 8-bit bus is selected by INF bit in the instruction register. During read or write operation, two 8-bit registers are used. One is data register (DR); the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/SEGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

RS	R/W	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)

● BUSY FLAG (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R / W = High (Read Instruction Operation); through DB7 before executing the next instruction, be sure that BF is not High.

- **DISPLAY DATA RAM (DDRAM)**

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure 1.)

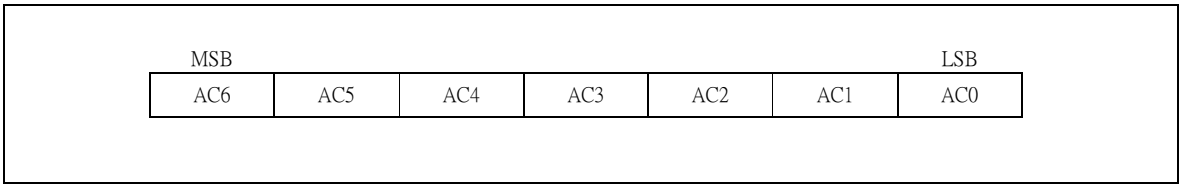
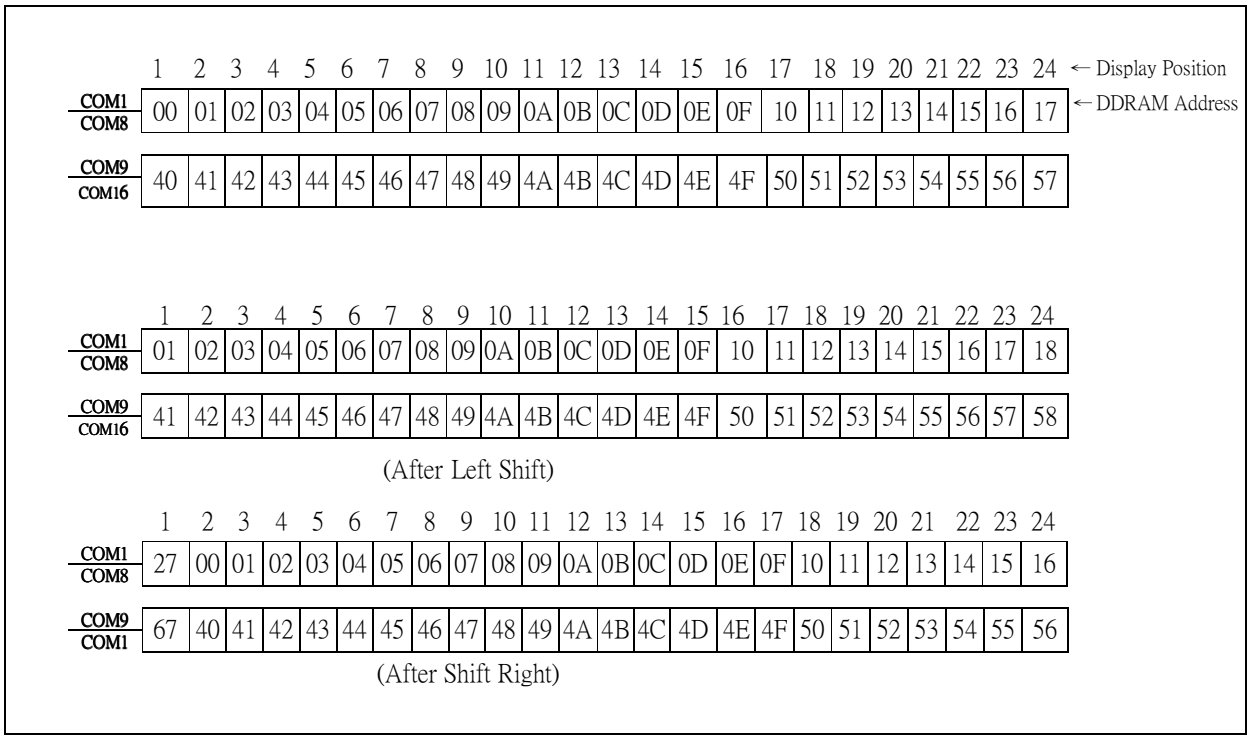


Figure 1. DDRAM Address

Since DDRAM has 8 bits data. It is possible to access 256 CGROM/CGRAM fonts.

➢ **5-dot 2-line Display**

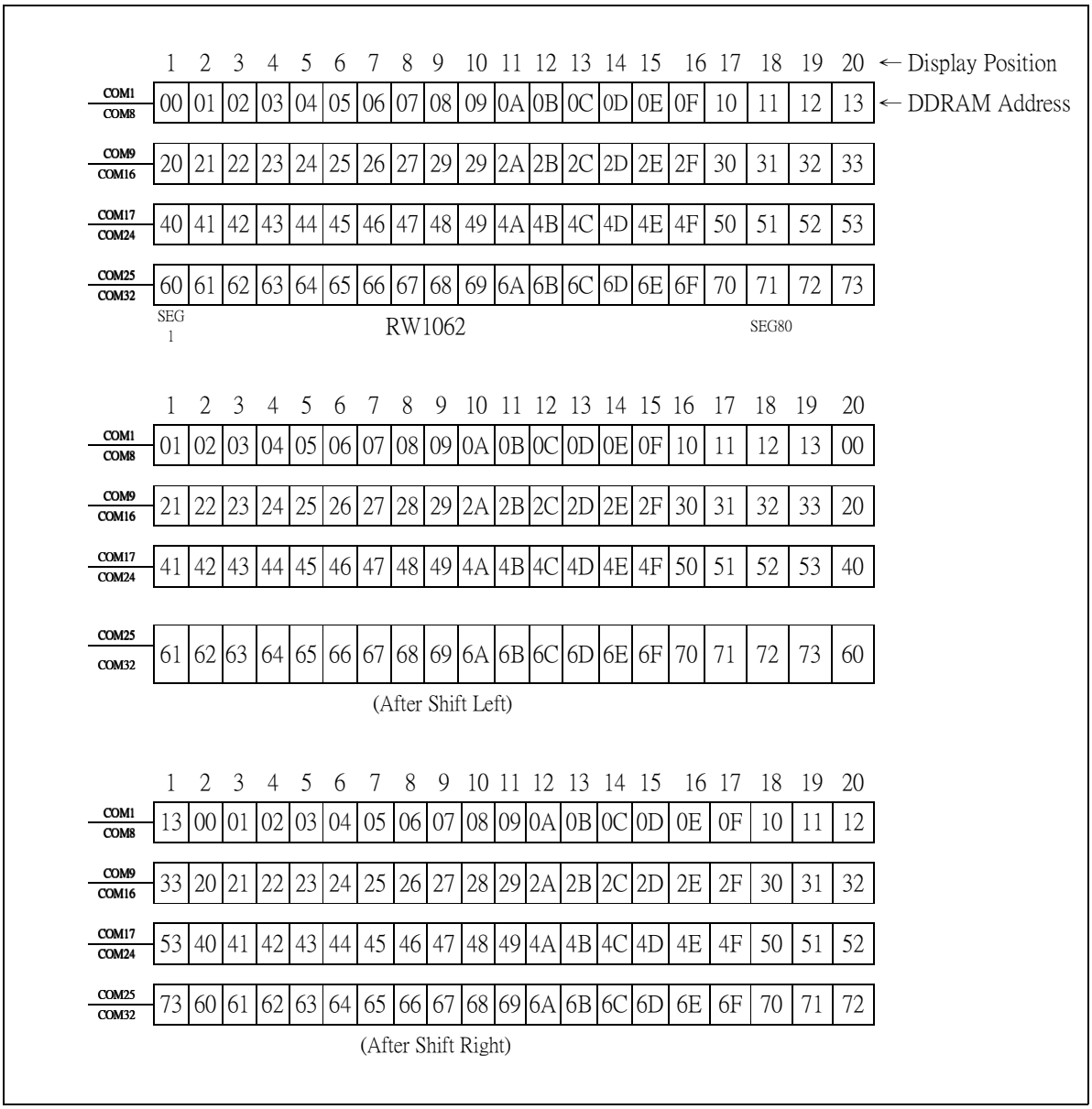
In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 2.)



(Figure 2.) 2 - Line X 24ch. Display

➢ **4-line Display**

In case of 4-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H.
(refer to Figure 3)



(Figure 3.) 4 - Line X 20ch. Display

- **TIMING GENERATION CIRCUIT**

Timing generation circuit generates clock signals for the internal operations.

- **ADDRESS COUNTER (AC)**

Address Counter (AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0-DB6

- **CURSOR/BLINK CONTROL CIRCUIT**

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

- **LCD DRIVER CIRCUIT**

LCD Driver circuit has 18 common and 120 segment signals for 2-line display (NW=0) or 34 common and 100 segments for 4-line display (NW=1) for LCD driving.
Data from SEGRAM/CGRAM/CGROM is transferred to 120 bit segment latches serially when 1/17 duty is performed (NW=0), and then it is stored to 120 bit shift latch. When 1/33 duty is performed (NW=1), segment data also output through segment driver from 100 bit segment latches.

- **CGROM (CHARACTER GENERATOR ROM)**

CGROM has 10,240 bits (256 characters x 5 x 8 dot)

- **CGRAM (CHARACTER GENERATOR RAM)**

CGRAM has up to 5 × 8 dots 8 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 2).

➢ **5 x 8 dots Character Pattern**

Table 2. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	Number
0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	0	1	1	1	0	Pattern 1
-	-	-	-	-	0	0	0	-	-	-	0	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	0	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	0	1	1	-	-	-	1	1	1	1	1	
-	-	-	-	-	0	0	0	-	-	-	1	0	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	1	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	1	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	1	1	1	-	-	-	0	0	0	0	0	
				-					-			-						-					
				-					-			-						-					
0	0	0	0	0	1	1	1	1	1	1	0	0	0	X	X	X	1	0	0	0	1	Pattern 8
-	-	-	-	-	1	1	1	-	-	-	0	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	0	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	0	1	1	-	-	-	1	1	1	1	1	
-	-	-	-	-	1	1	1	-	-	-	1	0	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	1	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	1	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	1	1	1	-	-	-	0	0	0	0	0	

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 2, CGRAM character patterns are selected when character code bits 4 to 7 are all 0 and MW=0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
   "-": Indicates no effect.

- **SEGRAM (SEGMENT ICON RAM)**

SEGRAM has segment control data and segment pattern data. There are 2 ICON pins act as the COM line to display the icon SEGRAM data. The outputs of these 2 ICON pins are exactly the same. (refer to Table 3 and Figure 4).

Table 3. Relationship between SEGRAM Address and Display Pattern

SEGRAM Address				SEGRAM Data Display Pattern							
				5-dot Font Width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	X	X	X	S1	S2	S3	S4	S5
0	0	0	1	X	X	X	S6	S7	S8	S9	S10
0	0	1	0	X	X	X	S11	S12	S13	S14	S15
0	0	1	1	X	X	X	S16	S17	S18	S19	S20
0	1	0	0	X	X	X	S21	S22	S23	S24	S25
0	1	0	1	X	X	X	S26	S27	S28	S29	S30
0	1	1	0	X	X	X	S31	S32	S33	S34	S35
0	1	1	1	X	X	X	S36	S37	S38	S39	S40
1	0	0	0	X	X	X	S41	S42	S43	S44	S45
1	0	0	1	X	X	X	S46	S47	S48	S49	S50
1	0	1	0	X	X	X	S51	S52	S53	S54	S55
1	0	1	1	X	X	X	S56	S57	S58	S59	S60
1	1	0	0	X	X	X	S61	S62	S63	S64	S65
1	1	0	1	X	X	X	S66	S67	S68	S69	S70
1	1	1	0	X	X	X	S71	S72	S73	S74	S75
1	1	1	1	X	X	X	S76	S77	S78	S79	S80

1.S1 – S80 :ICON Pattern ON/OFF
2. "X" : Don't care

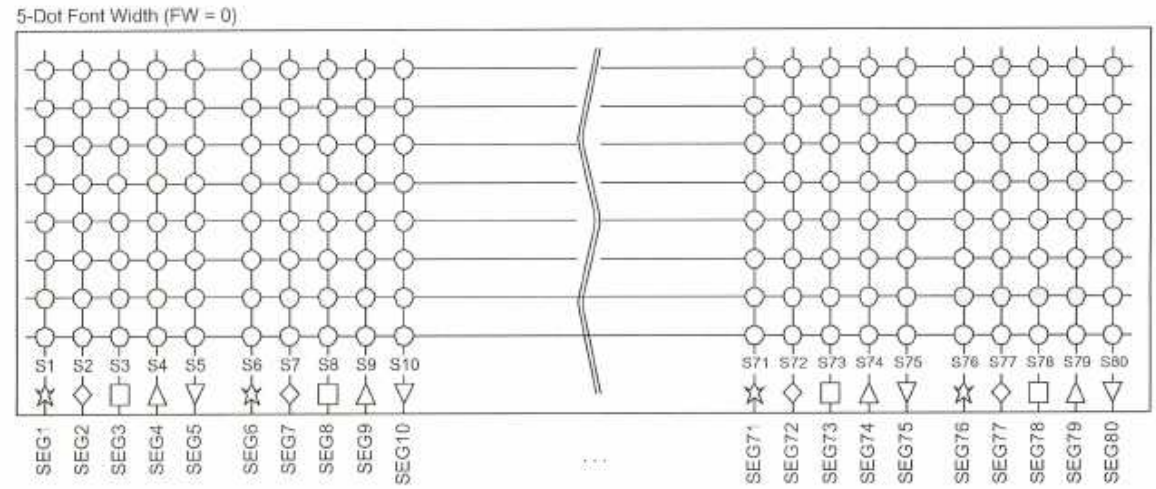


Figure 4. Relationship between SEGRAM and Segment Display

■ INSTRUCTION DESCRIPTION

● OUTLINE

To overcome the speed difference between internal clock of RW1062 and MPU clock, RW1062 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus.

Instruction can be divided largely four kinds;

- RW1062 function set instructions (set display methods, set data length, etc.)
- Address set instructions to internal RAM
- Data transfer instructions with internal RAM
- Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read high. Busy Flag check must be proceeded the next instruction.
Busy flag check must be proceeded the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

- **Display Clear**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status; namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home: (RE = 0)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

- **Standby Mode Set: (RE = 1)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	PD

Standby mode enable bit set instruction.
PD = 1: it makes RW1062 suppress current consumption except the current needed for data storage by executing next three functions.
Note:
1. Makes the output value of all the COM / SEG ports VSS.
2. Disable voltage converter to remove the current through the divide resistor of power supply.
3. The system clock keep oscillator in standby mode.

PD = 0: Standby mode released.

- **Entry Mode Set: (RE = 0)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)
I/D = 1: cursor/blink moves to right and DDRAM address is increased by 1.
I/D = 0: cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates the same as DDRAM, when read/write from or to CGRAM/SEGRAM.
S: Shift of entire display
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed.
If S= "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1": shift left, I/D = "0": shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Entry Mode Set: (RE = 1)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	SHL	BID

Set the data shift direction of segment in the application set.

BID: Data Shift Direction of Segment.

BID = 0: segment data shift direction is set to normal order.
SEG1 to SEG120 for 2-line display
SEG1 to SEG100 for 4-line display
BID = 1: segment data shift direction is set to reverse order.
SEG120 to SEG1 for 2-line display
SEG100 to SEG1 for 4-line display
By using this instruction, the efficiency of application board area can be raised.
- The BID setting instruction is recommended to be set at the same time level of function set instruction.

SHL: Common scan direction select.

SHL= 0: COM scan direction is normal.
COM1->COM16 for 2-line display
COM1 -> COM32 for 4-line display
SHL=1: COM scan direction is reverse direction.
COM16 ->COM1 for 2-line display
COM32 -> COM1 for 4-line display

- **Display ON/OFF Control (RE = 0)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit.
D = 1: entire display is turned on.
D = 0: display is turned off, but display data is remained in DDRAM.
C: Cursor ON/OFF control bit.
C = 1: cursor is turned on.
C = 0: cursor is disappeared in current display, but I/D register remains its data.
B: Cursor Blink ON/OFF control bit.
B = 1: cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270 kHz frequency, blinking has 370 ms interval.
B = 0: blink is off.

- **Extended Function Set (RE = 1)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	MW	NW

MW: CGROM/CGRAM display select
MW = 0: the font code address for b7-b4=0000 display the CGRAM contents
MW =1: the font code address for b7-b4=0000 display CGROM contents
NW: Display Duty Select
NW =”0”: 2-line display mode, 1/17 duty.
NW =”1”: 4-line display mode, 1/33 duty.

- **Cursor or Display Shift (RE = 0)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 4). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
During 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.
Note that display shift is performed simultaneously by the shift enable instruction. When displayed data is shifted repeatedly, all display lines shifted simultaneously. When display shift is performed, the contents of address counter are not changed.
During low power consumption mode, display shift may not be performed normally.

Table 4. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

● Analog circuit instruction

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	BSTON	REGON	FOF

BSTON=0: Booster off (default)
BSTON=1: Booster on
REGON=0: regulator off (default)
REGON=1: regulator on
FOF=0: follower on (default)
FOF=1: follower off

● Function Set

(**RE = 0**)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	INF	X	RE(0)	X	X

INF: Interface data length control bit
INF = 1: it means 8-bit bus mode with MPU.
INF = 0: it means 4-bit bus mode with MPU. So to speak, INF is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode is selected, it needs to transfer 4-bit data by two times.

RE: Extended function registers enable bit
At this instruction, RE must be "Low".

(**RE = 1**)

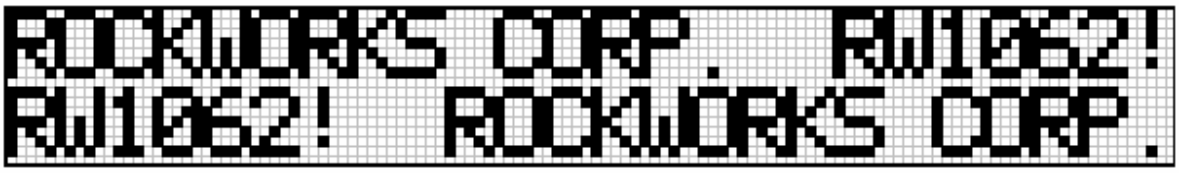
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	INF	X	RE(1)	DH1	DH0

INF: Interface data length control bit
INF = 1: it means 8-bit bus mode with MPU.
INF = 0: it means 4-bit bus mode with MPU. So to speak, INF is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode is selected, it needs to transfer 4-bit data by two times.

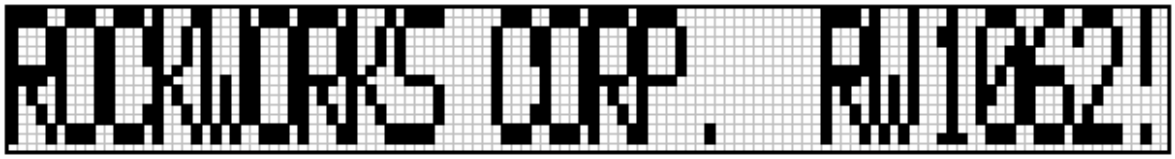
RE: Extended function registers enable bit
RE = 1: extended function set registers, SEGRAM address set registers, BID bit, SHL bit, DH1 bit DH0 bit standby mode register, and set data length for 3 line SPI register can be accessed.

DH1, DH0: Set Double Height Mode

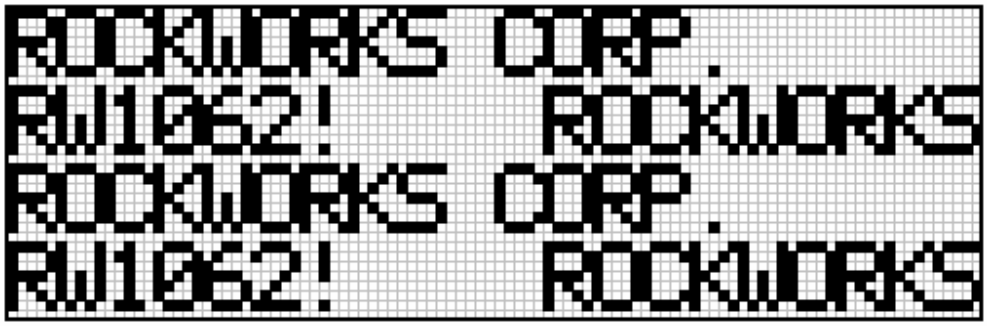
DH1	DH0	Action
Low	Low	Normal display (default)
Low	High	1) 2-line mode COM1...COM16 is a double height Display DDRAM address 00H ~ 27H 2) 4-line mode COM1...COM16 is a double height Display DDRAM address 00H~13H COM17...COM32 is normal
High	Low	1) 2-line mode normal display 2) 4-line mode COM1...COM16 is normal COM17...COM32 is a double height Display DDRAM address 40H ~ 53H
High	High	1) 2-line mode COM1...COM16 is a double height Display DDRAM address 00H ~ 27H 2) 4-line mode COM1...COM16 is a double height Display DDRAM address 00H ~ 13H COM17...COM32 is a double height Display DDRAM address 40H ~ 53H



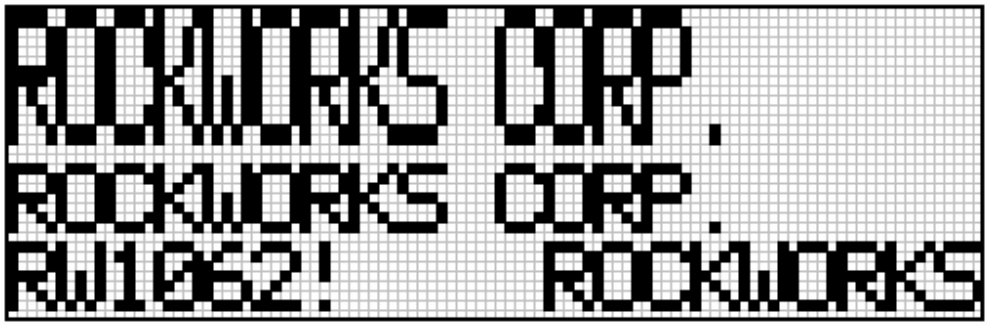
2 Line mode normal display (DH1, DH0 = 0, 0)



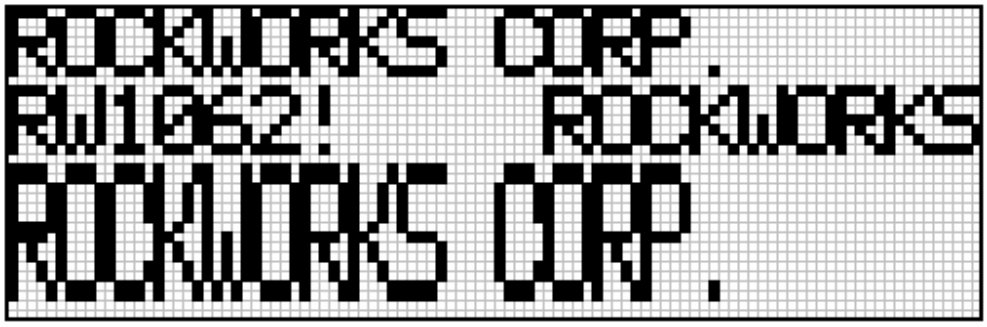
2 Line mode display (DH1, DH0=0, 1)



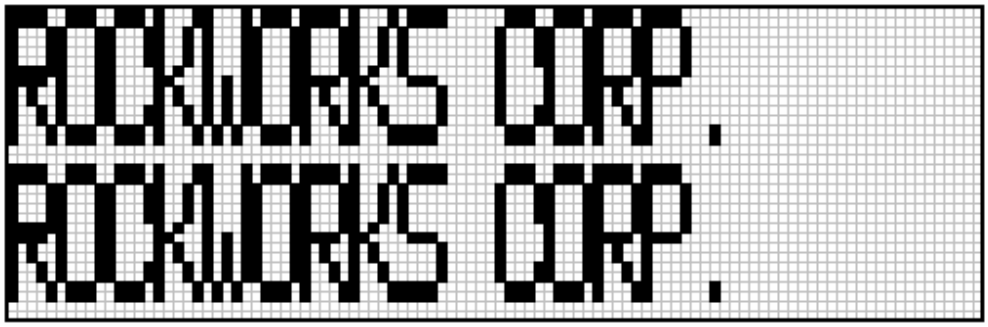
4 Line mode normal display (DH1, DH0=0, 0)



4 Line mode normal display (DH1, DH0=0, 1)



4 Line mode normal display (DH1, DH0=1, 0)



4 Line mode normal display (DH1, DH0=1, 1)

- **Set CGRAM Address (RE = 0)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

- **Set SEGRAM Address (RE = 1)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	x	x	AC3	AC2	AC1	AC0

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

- **Set DDRAM Address (RE = 0)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.
In 2-line display mode (NW = 0), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H". In 4-line display mode (NW = 1),
DDRAM address is from "00H" - "13H" in the 1st line, from "20H" - "33H" in the 2nd line, from "40H" - "53H" in the 3rd line and from "60H" - "73H" in the 4th line.

- **Set data length for 3 line SPI (RE = 1)**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	SD6	SD5	SD4	SD3	SD2	SD1	SD0

In 3 lines SPI mode, set Data length command indicates the length of data which, are going to be received by RW1062. User should set data length before display data sent. Each data length instruction maximum can set 80 bytes of data. The table below shows how SD bits set the data length.

Table 6. Set data length according to SD Bits

SD6	SD5	SD4	SD3	SD2	SD1	SD0	Function
0	0	0	0	0	0	0	Followed by 1 data write
0	0	0	0	0	0	1	Followed by 2 data write
0	0	0	0	0	1	0	Followed by 3 data write
0	0	0	0	0	1	1	Followed by 4 data write
:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	Followed by 80 data write

- **Read Busy Flag & Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether RW1062 is in internal operation or not. If the resultant BF is high, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

- **Write Data to RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.

The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction:
DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

■ INTERFACE WITH MPU

RW1062 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU.
In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.

- When interfacing data lengths are 4-bit, only 4 ports, from DB4 - DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4- bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended.

- When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 - DB7.

- Interface is selected by IF1P, IF0P pins

IF1	IF0	Interface Select
0	0	3-line SPI
0	1	4-line SPI
1	0	IIC
1	1	6800 8/4-bit

■ INTERFACE WITH MPU IN BUS MODE

● Interface with 8-bit MPU

If 8-bits MPU is used, RW1062 can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.

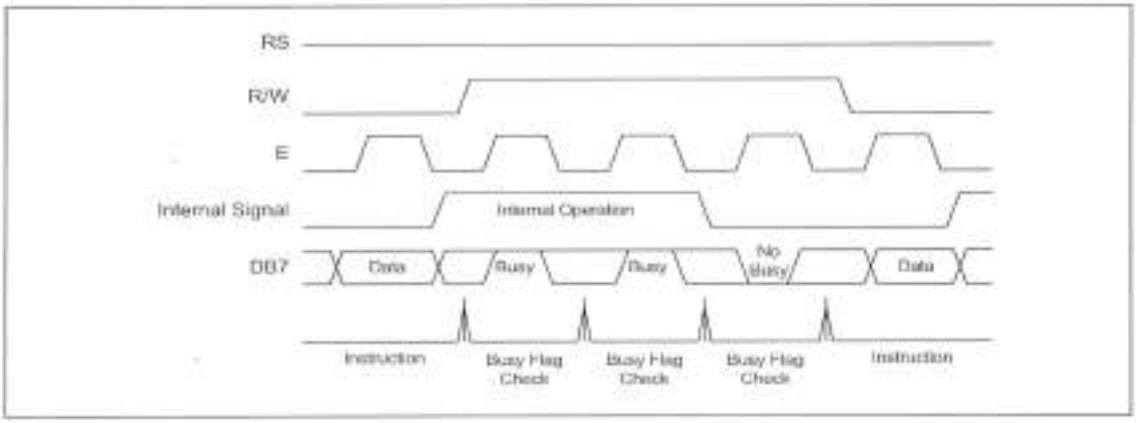


Figure 5. Example of 8-bit Bus Mode Timing Sequence

● Interface with 4-bit MPU

If 4-bit MPU is used, RW1062 can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.

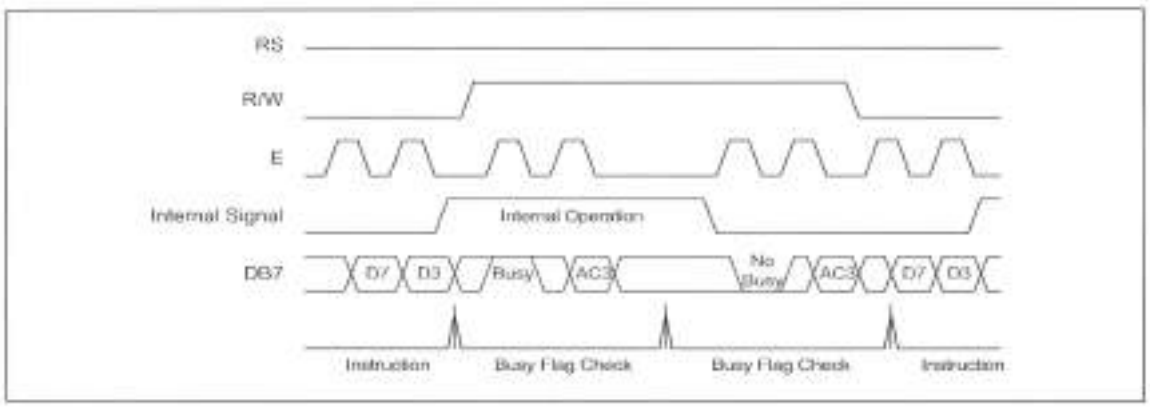
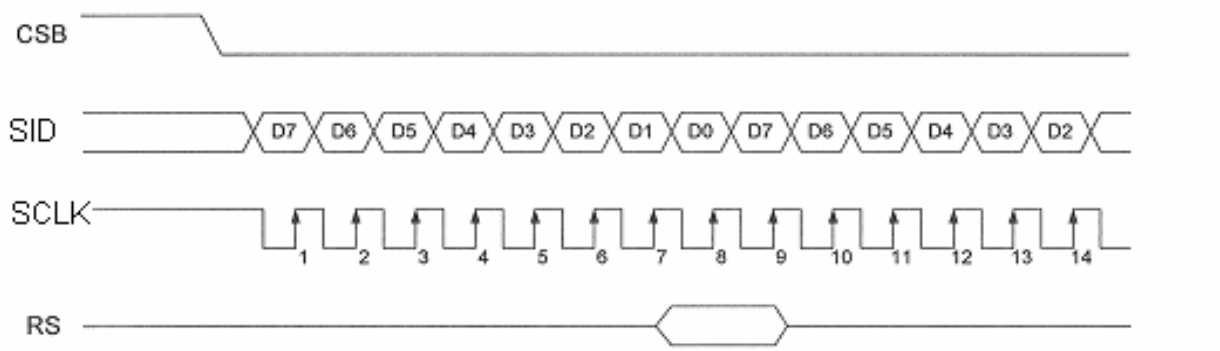


Fig 6. Example of 4-bit Bus Mode Timing Sequence

■ For serial interface data, bus lines (DB5 to DB7) are used. 4-Pin SPI

If 4-Pin SPI mode is used, CSB (DB5), SCLK (DB7), SID (DB6), and RS are used. They are chip selection; serial input data, serial clock input, and data/instruction section, relatively. The example of timing sequence is shown below.

➢ Example of timing sequence

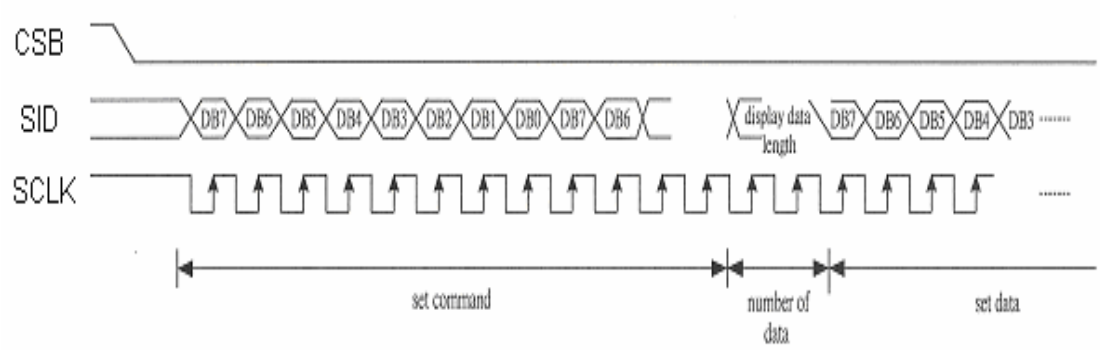


Note: Following is the master SPI clock mode of MPU.
Idle state for clock is a high level，data transmitted on rising edge of SCLK, and data is hold during low level.

■ For serial interface data, bus lines (DB5 to DB7) are used. 3 – Pin SPI

If 3-Pin SPI mode is used, CSB (DB5), SCLK (DB7), and SID (DB6) are used. They are chip selection, serial input data, and serial clock input, relatively. 3-Pin SPI mode does not use RS for data/instruction selection. Data length instruction should be used to realize data/instruction and data length instruction also indicates length of data. The example of timing sequence is shown below; data length instruction is followed by data set.

➢ Example of timing sequence



Note: Following is the master SPI clock mode of MPU.
Idle state for clock is a high level，data transmitted on rising edge of SCLK, and data is hold during low level.

■ For serial interface data, bus lines (DB6 and DB7) are used. IIC interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. Serial data line SDA (DB6) must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.
* When IIC interface is selected, the INF register must be set to “1”.

➢ BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.7.1

➢ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.7.2

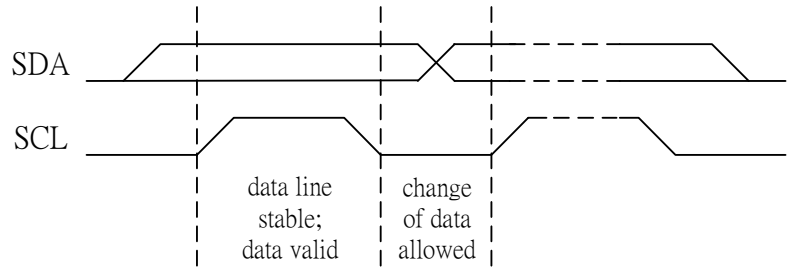


Fig .7.1 Bit transfer

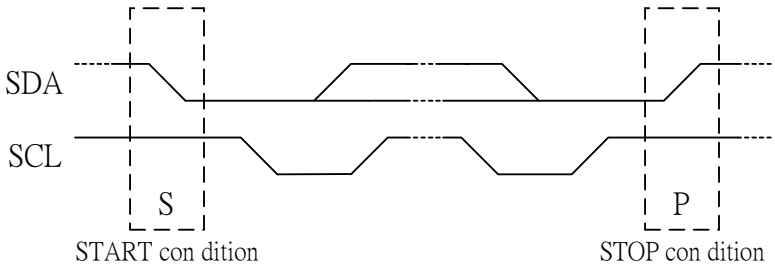


Fig .7.2 Definition of START and STOP conditions

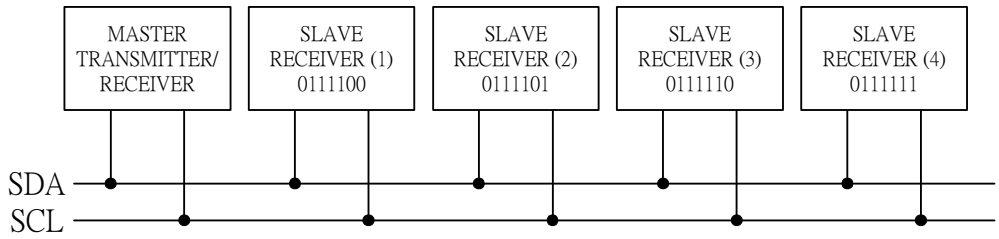


Fig .7.3 System configuration

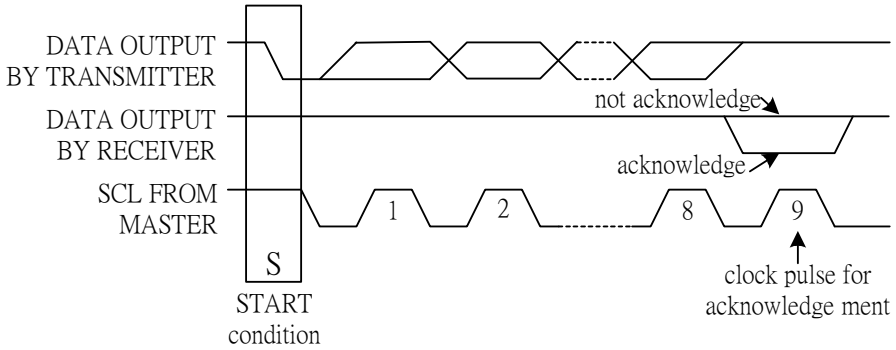


Fig .7.4 Acknowledgement on the 2-line Interface

➢ SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.7.3
· Transmitter: the device, which sends the data to the bus
· Receiver: the device, which receives the data from the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

➢ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.7.4

➢ IIC Interface protocol

The RW1062 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1062. The least significant bit of the slave address is set by connecting the input DB0 and DB1 to either logic 0 (or logic 1 (VDD)).
The IIC Interface protocol is illustrated in Fig.7.5
The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1062 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC interface-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

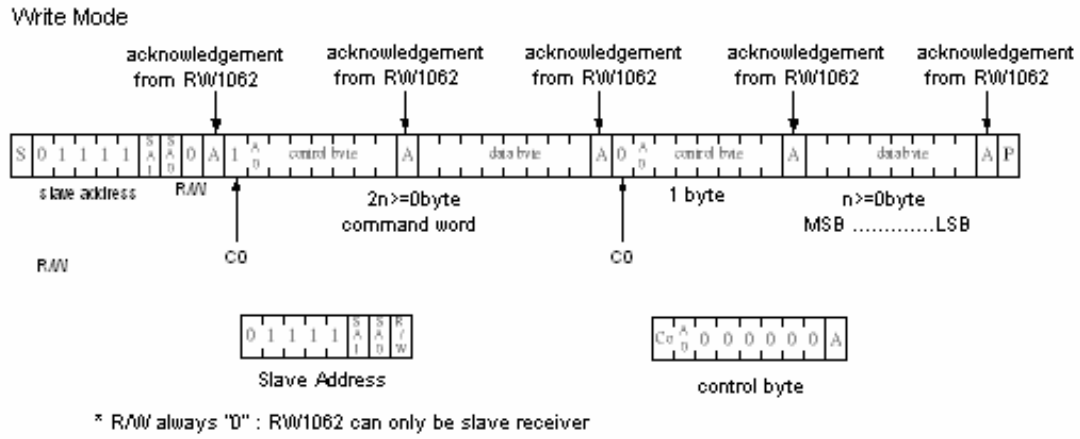


Fig .7.5 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

■ INITIALIZING

● INITIALIZING BY INTERNAL RESET CIRCUIT

When the power is turned on, RW1062 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High"(busy state) to the end of initialization.

● Display Clear Instruction

Write "20H" to all DDRAM

● Set Functions Instruction

IF = 1: 8-bit bus mode
RE = 0: Extension register disable
BE = 0: CGRAM/SEGRAM blink OFF
DH1, DH0 = 0: double height display off

● Control Display ON/OFF Instruction

D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Blink OFF

● Set Entry Mode Instruction

I/D = 1: Increment by 1
S = 0: No entire display shift
BID = 0: Normal direction segment port
SHL = 0: Common scan direction normal

● Set Extension Function Instruction

MW = 0: font address for b7-b4=0000 display CGRAM address
NW = 0: 2-line display mode.

● Set data length Instruction

SD = 000000

● Analog circuit instruction

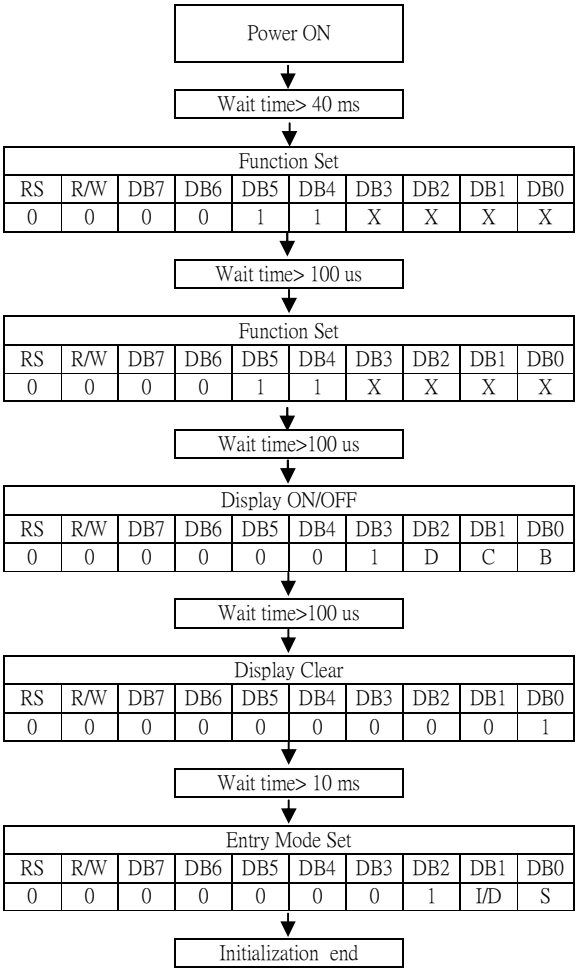
BSTON = 0: booster circuit off
REGON = 0: V0 regulator off
FOF = 0: follower on

● INITIALIZING BY HARDWARE RESET INPUT

When XRESET pin = "Low", RW1062 can be initialized like the case of power on reset. During the power on reset operation, this pin is ignored.

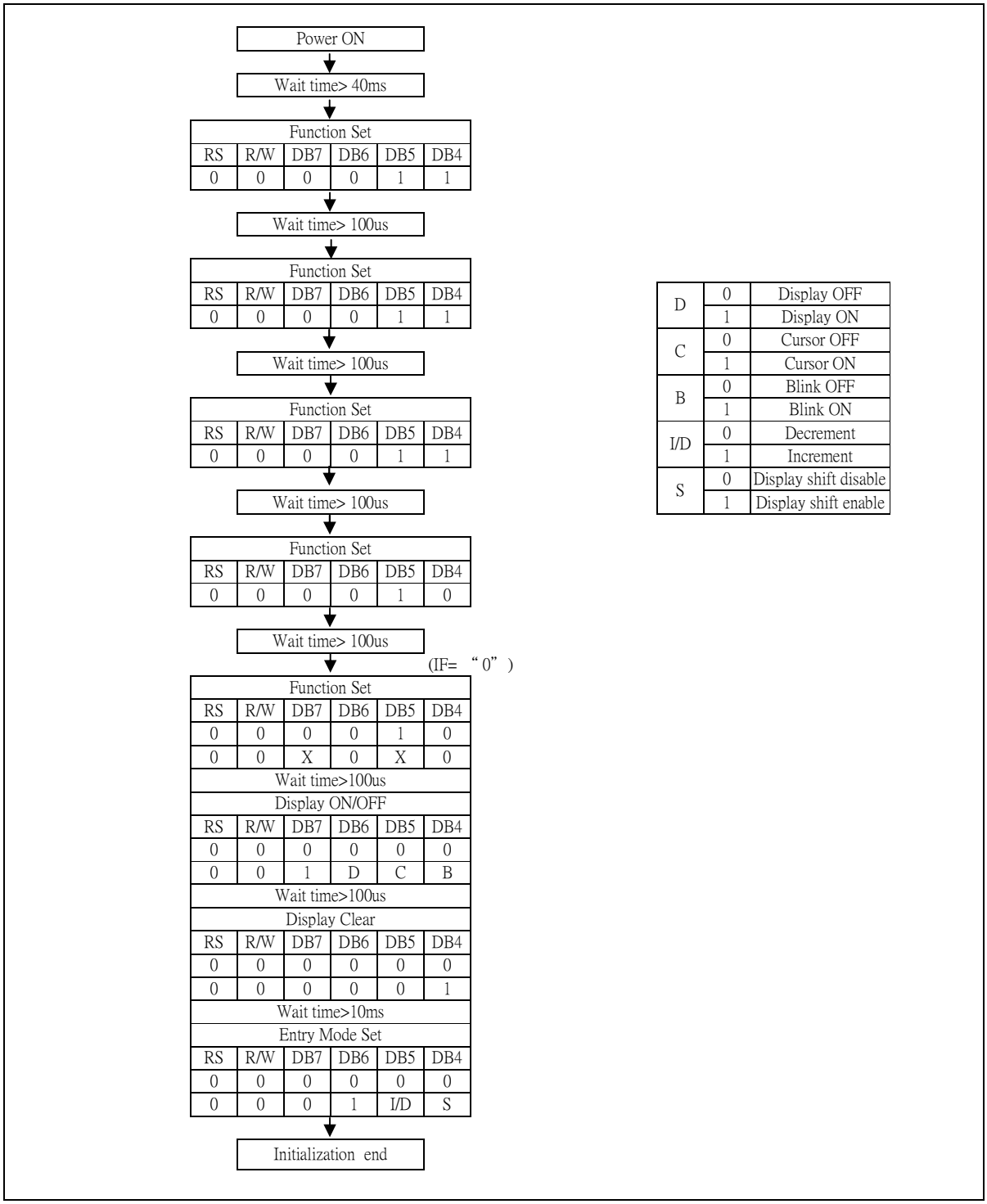
■ INITIALIZING BY INSTRUCTION

● 8-BIT INTERFACE MODE

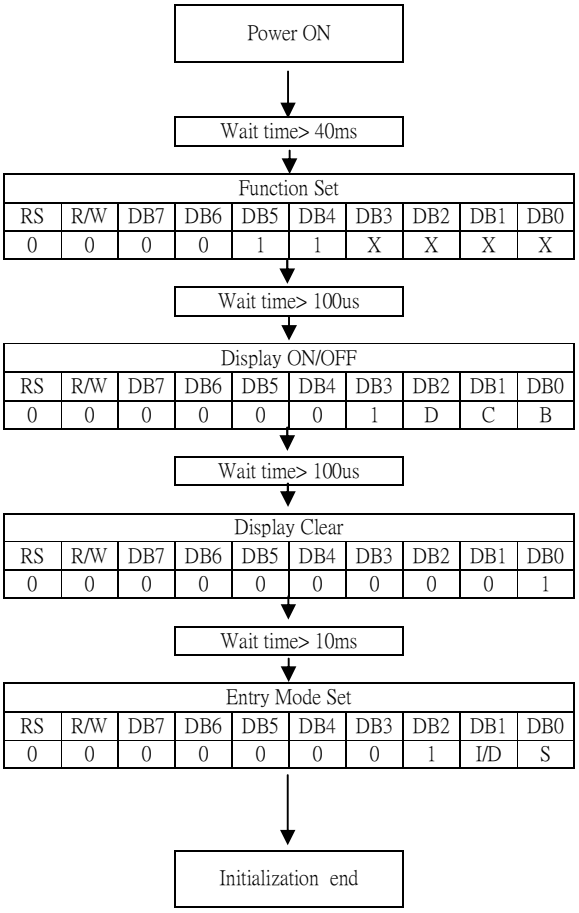


D	0	Display OFF
	1	Display ON
C	0	Cursor OFF
	1	Cursor ON
B	0	Blink OFF
	1	Blink ON
I/D	0	Decrement
	1	Increment
S	0	Display shift disable
	1	Display shift enable

- **4 – BIT INTERFACE MODE**

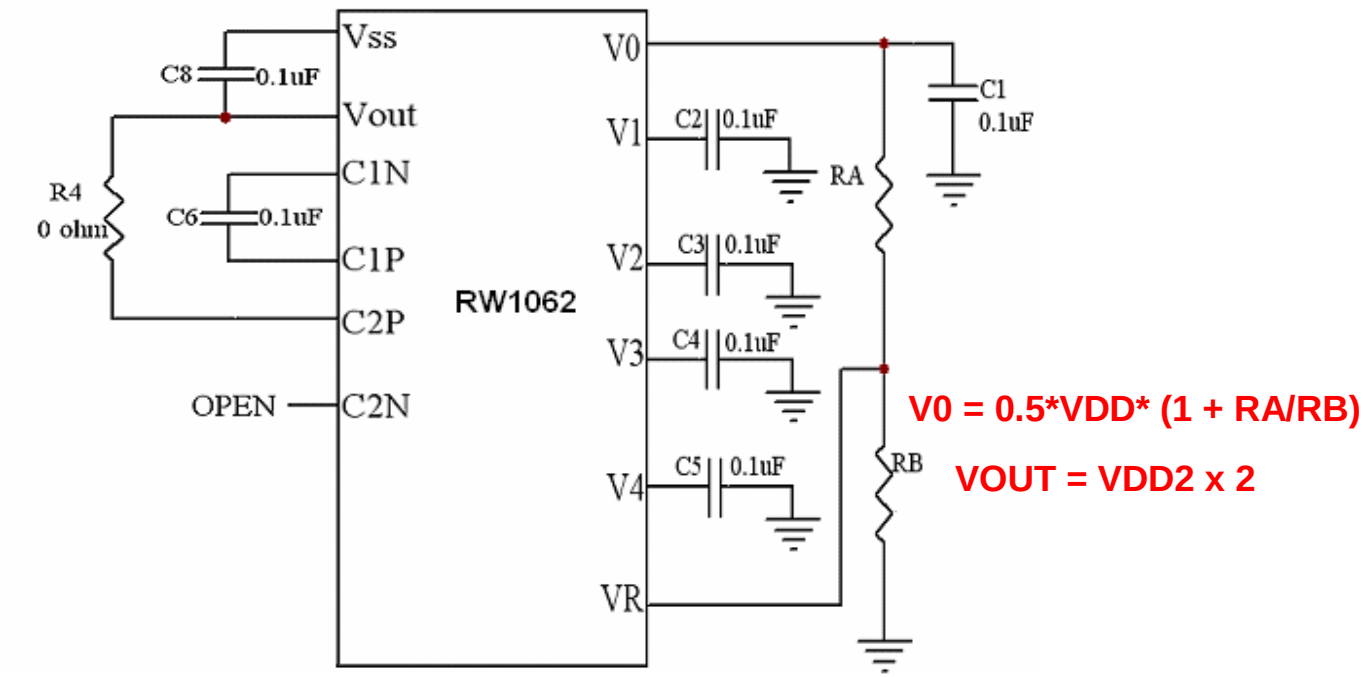


- **Serial Interface Mode**

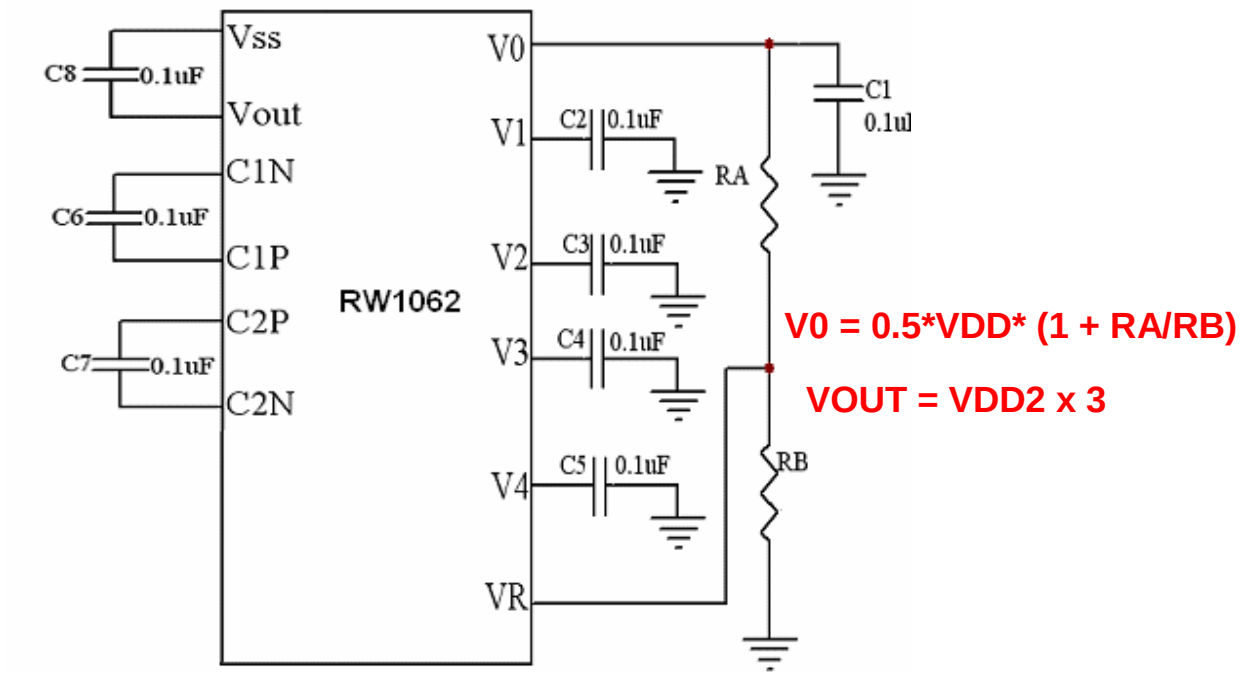


D	0	Display OFF
	1	Display ON
C	0	Cursor OFF
	1	Cursor ON
B	0	Blink OFF
	1	Blink ON
I/D	0	Decrement
	1	Increment
S	0	Display shift disable
	1	Display shift enable

■ **When internal LCD power circuit is used**



X 2 Booster Circuit connections



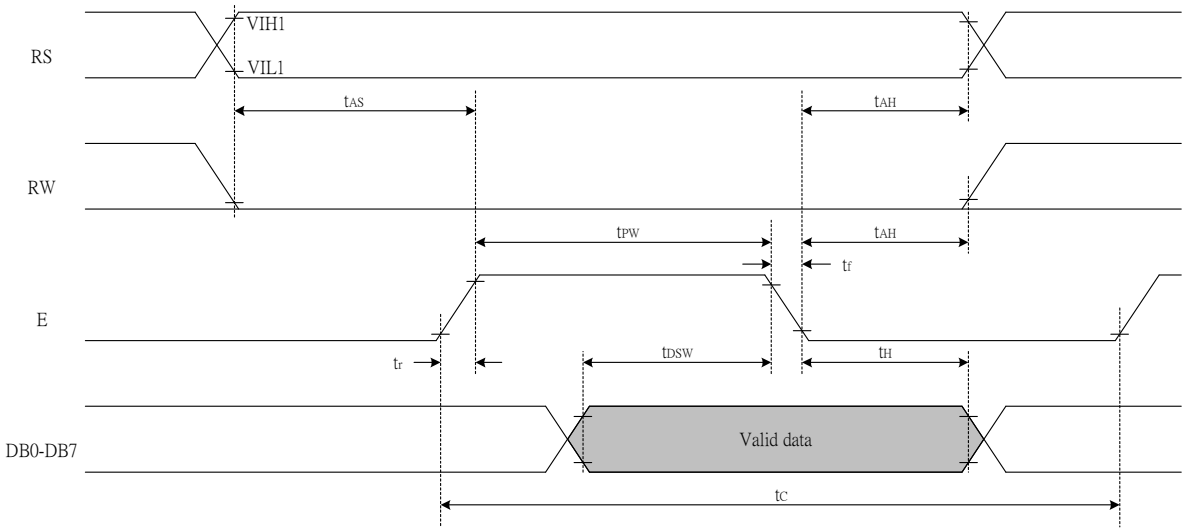
X 3 Booster Circuit connections

Table 7. Duty Ratio and Power Supply for LCD Driving

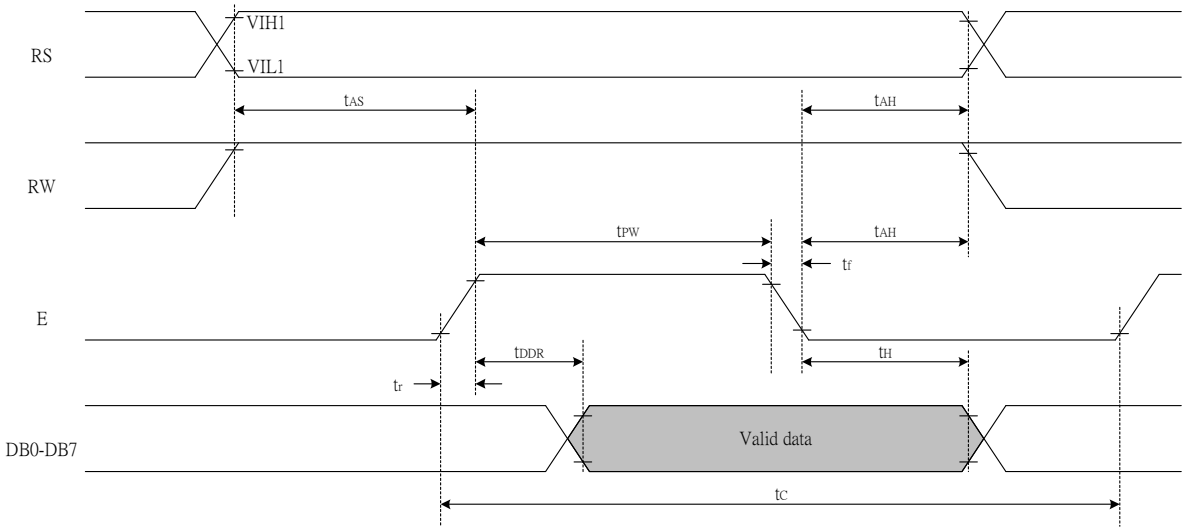
Item	Data	
Number of lines	2	4
Duty ratio	1/17	1/33
Bias	1/5	1/6.7

■ Timing Characteristics

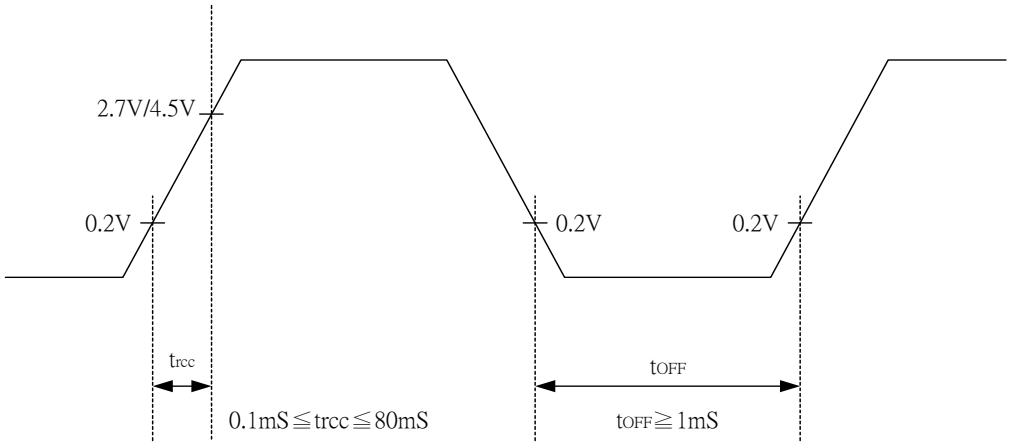
- **Writing data from MPU to RW1062**



- **Reading data from RW1062 to MPU**



- **Internal Power Supply Reset**



Notes:
- tOFF compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation,and at 2.7V for 3V operation.
- For if 4.5V is not reached during 5V operation,teh internal reset circuit will not operate normally.

■ AC Characteristics

In 6800 interface

(TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency		190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to RW1062)						
T_C	Enable Cycle Time	Pin E (except clear display)	1000	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	40	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	20	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from RW1062 to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	480	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	320	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

■ AC Characteristics

In 6800 interface

(TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency		190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to RW1062)						
T_C	Enable Cycle Time	Pin E (except clear display)	500	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	40	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	20	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from RW1062 to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

■ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{CC}	-0.3 to +5.5
LCD Driver Voltage	V_{LCD}	Vss+7.0 to Vss-0.3
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3
Operating Temperature	T_A	-40°C to + 90°C
Storage Temperature	T_{STO}	-55°C to + 125°C

■ DC Characteristics

(TA = 25℃ , VCC = 2.7 V – 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V0 - Vss	3.0	-	7.0	V
I_{DD}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=3.0V	-	0.25	0.45	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2Vcc	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.75 Vcc	-	-	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.2Vcc	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{CC} = 3V	10	60	120	µA

■ DC Characteristics

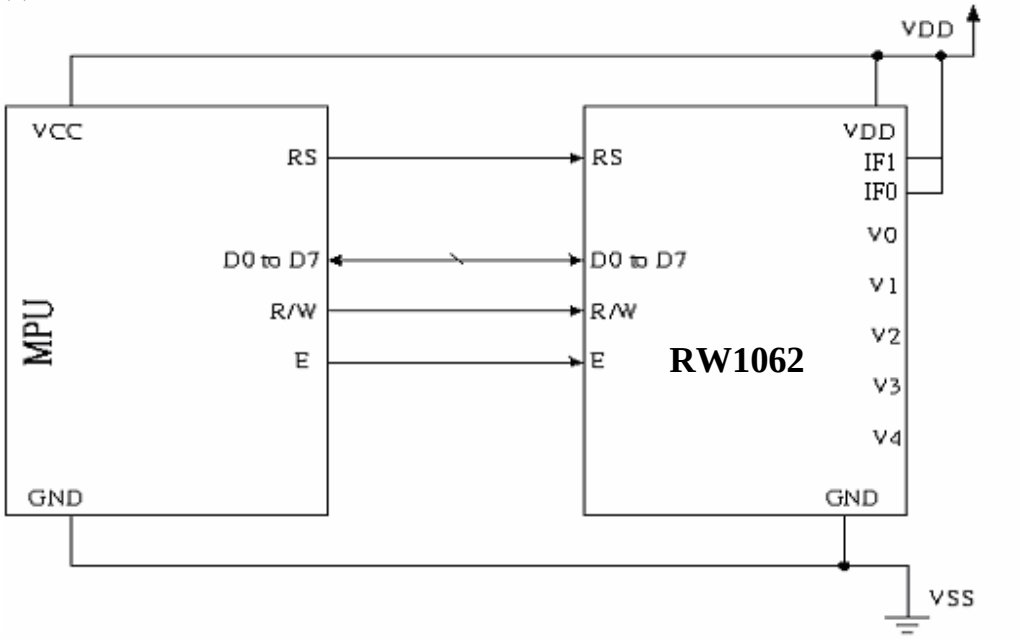
(TA = 25℃, V_{CC} = 4.5 V - 5.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V0 - Vss	3.0	-	7.0	V
I_{DD}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=5.0V	-	0.35	0.55	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	2.5	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{CC}-1	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	3.9	-	V_{CC}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.4	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.9V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.1V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{CC} = 5V	90	200	330	µA

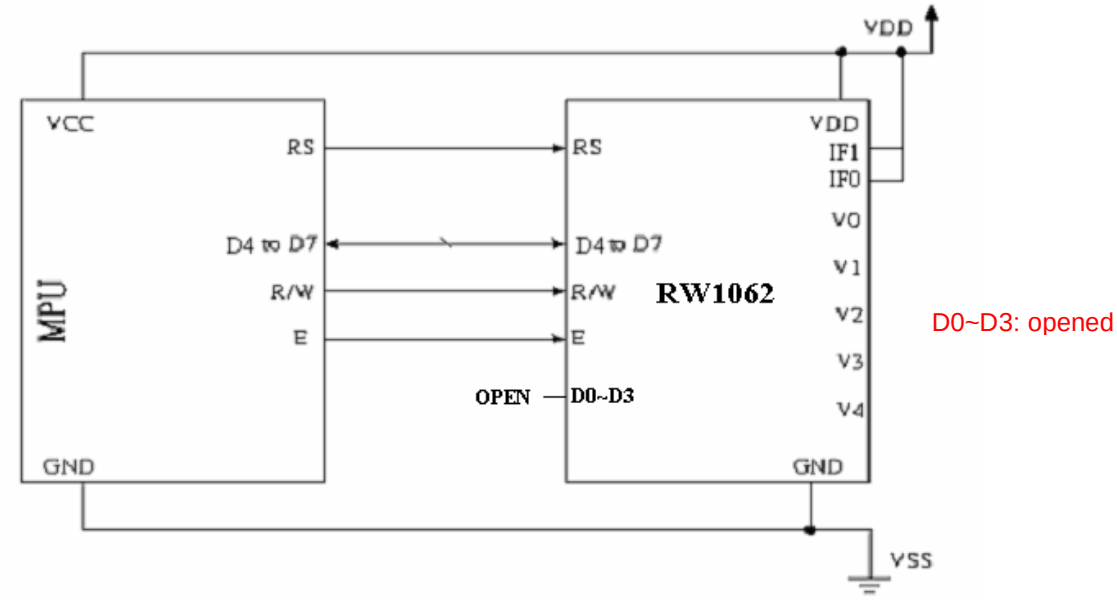
■ THE MPU INTERFACE CIRCUIT

The RW1062 Series can be connected to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the RW1062 series chips with fewer signal lines.
The display area can be enlarged by using multiple RW1062 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

(1) 6800 8 bits Series MPUs

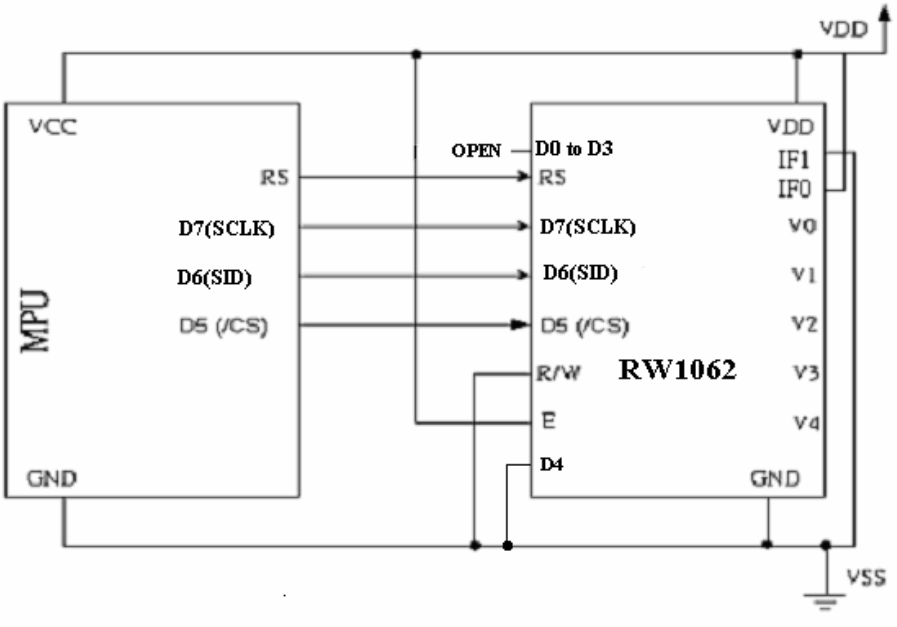


(2) 6800 4 bits Series MPUs



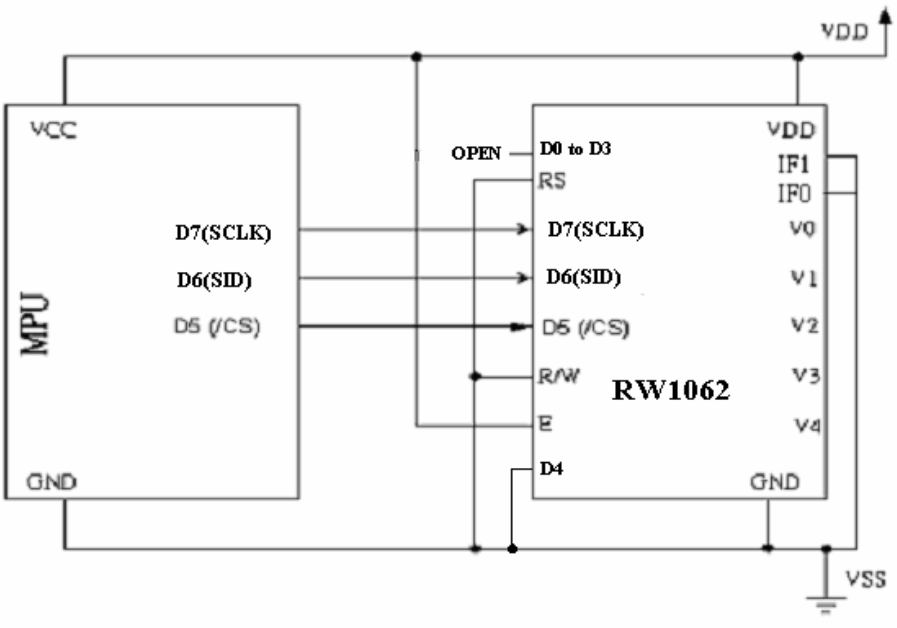
D0~D3: opened

(3) Using the Serial Interface—For 4 SPI



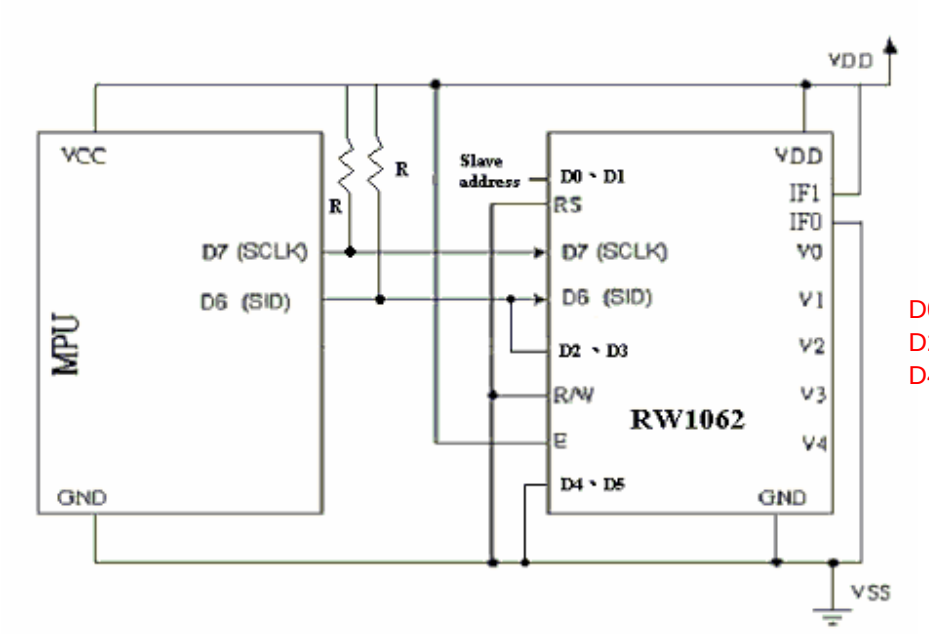
E: connect to VDD
RW: connect to VSS
D4: connect to VSS
D0~D3: opened

(4) Using the Serial Interface—For 3 SPI



E: connect to VDD
RW 、RS: connect to VSS
D4: connect to VSS
D0~D3: opened

(5) Using the Serial Interface—For IIC Interface

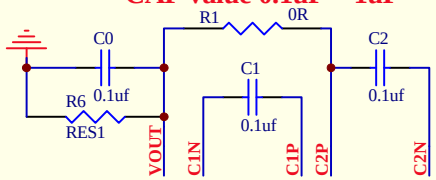


D0、D1: Slave address
D2、D3: connect to D6
D4、D5: connect to VSS

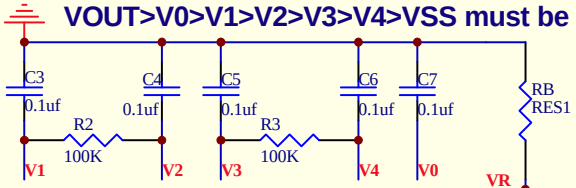
RW1062 Font table (0A-001)

b7~4 / b3~0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM [00]															
0001	CG RAM [01]															
0010	CG RAM [02]															
0011	CG RAM [03]															
0100	CG RAM [04]															
0101	CG RAM [05]															
0110	CG RAM [06]															
0111	CG RAM [07]															
1000	CG RAM [00]															
1001	CG RAM [01]															
1010	CG RAM [02]															
1011	CG RAM [03]															
1100	CG RAM [04]															
1101	CG RAM [05]															
1110	CG RAM [06]															
1111	CG RAM [07]															

CAP value 0.1uF ~ 1uF



VOUT>V0>V1>V2>V3>V4>VSS must be maintained

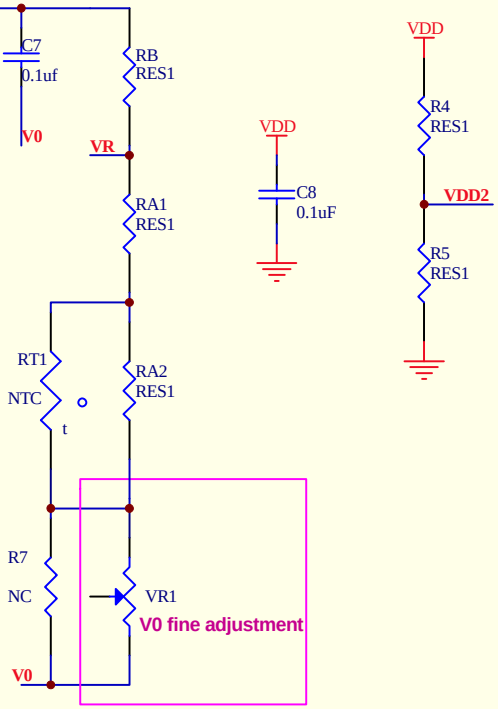


2X: put C0 and C1,short R1

3X: put C0 and C1 C2,open R1

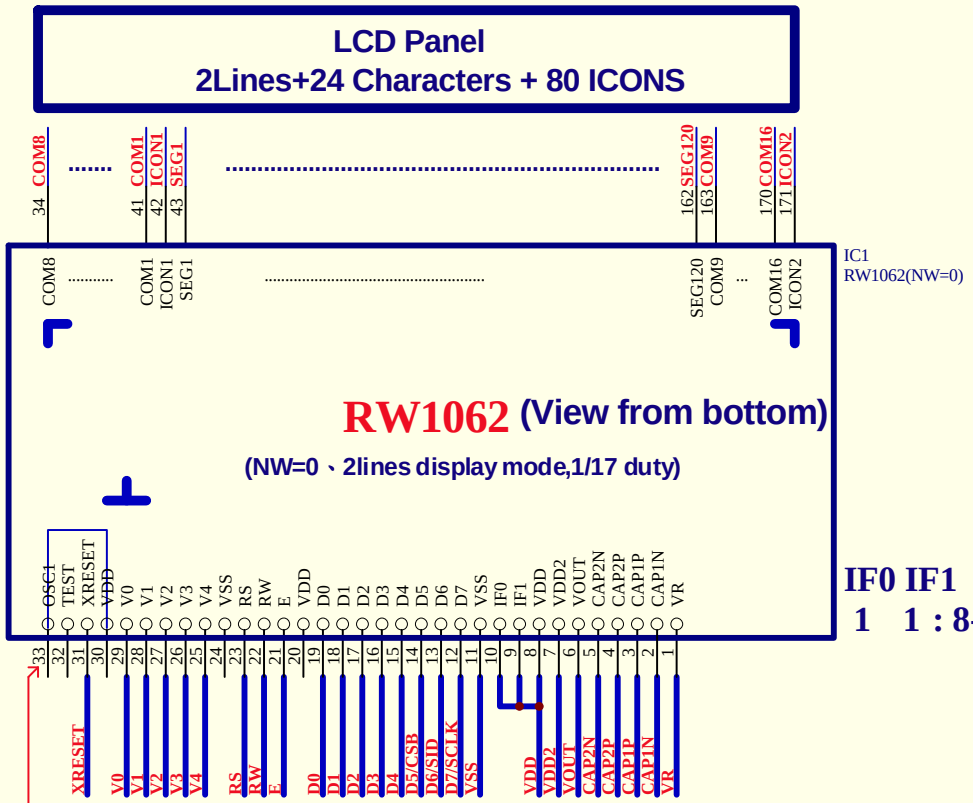
VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

VOUT Voltage should not higher than 8V



V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)

VLCD=V0-VSS



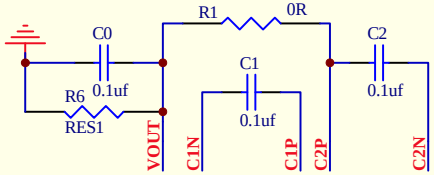
IF0 IF1
1 1 : 8-bit 6800 interface

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.

Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

Title: **RockWorks**		
Size: A	Number: **RW1062 8 bit 6800 interface**	Revision: **B**
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

CAP value 0.1uF ~ 1uF



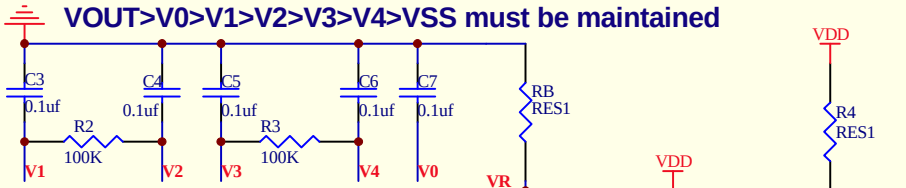
2X: put C0 and C1,short R1

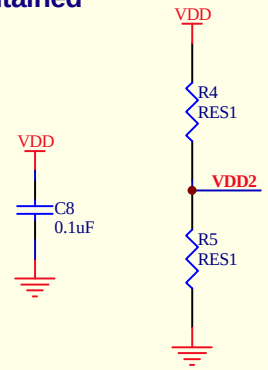
3X: put C0 and C1 C2,open R1

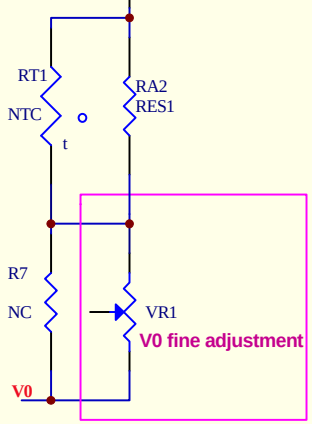
VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

VOUT Voltage should not higher than 8V

VOUT>V0>V1>V2>V3>V4>VSS must be maintained

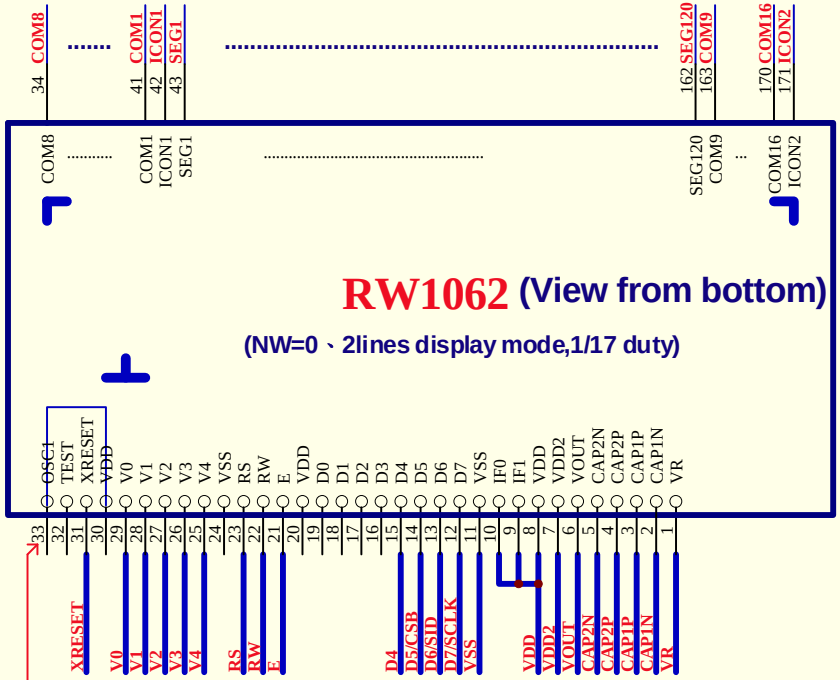






V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)
VLCD=V0-VSS

LCD Panel
2Lines+24 Characters + 80 ICONS

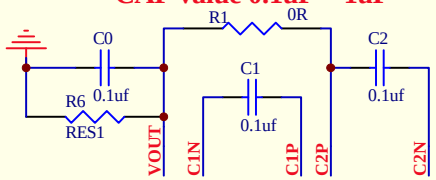


IF0 IF1
1 1 : 4-bit 6800 interface

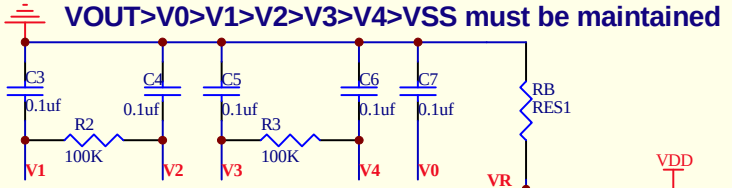
Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

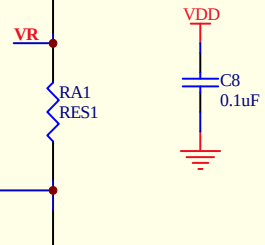
Title: **RockWorks**		
Size: A	Number: **RW1062 4 bit 6800 interface**	Revision: **B**
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

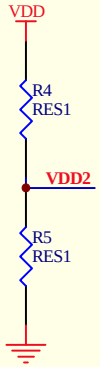
CAP value 0.1uF ~ 1uF



VOUT>V0>V1>V2>V3>V4>VSS must be maintained







2X: put C0 and C1,short R1

3X: put C0 and C1 C2,open R1

VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)

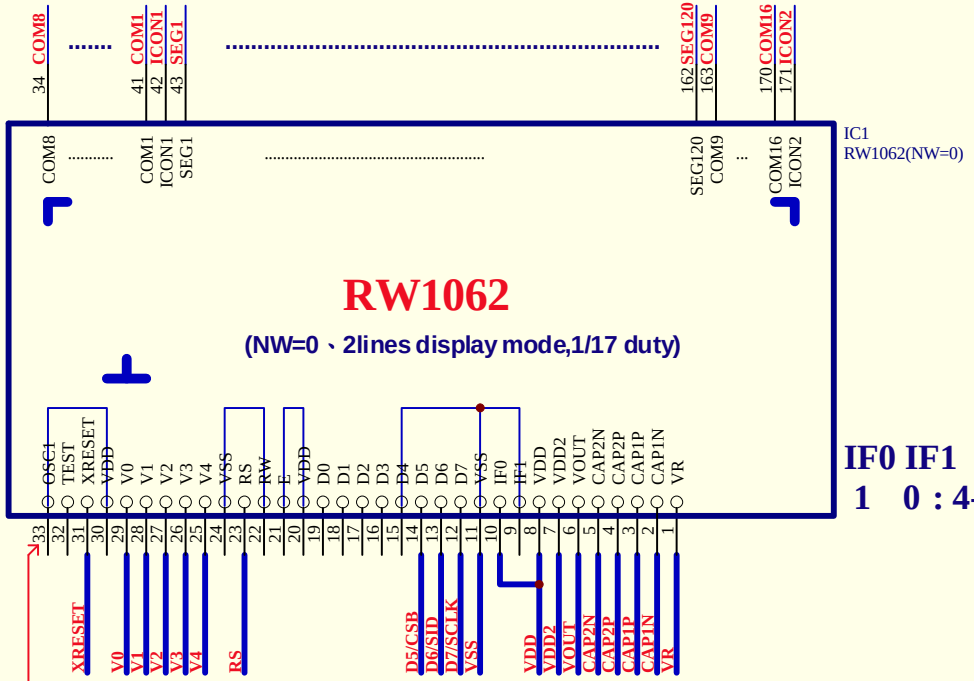
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

VOUT Voltage should not higher than 8V

V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)

VLCD=V0-VSS

LCD Panel
2Lines+24 Characters + 80 ICONS



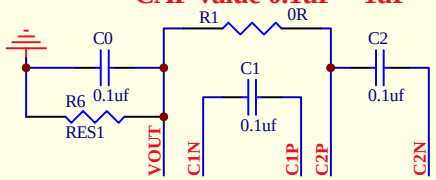
IF0 IF1
1 0 : 4-SPI interface

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.

Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

Title: RockWorks		
Size: A	Number: RW1062 4-SPI interface	Revision: B
Date: 18-Nov-2009	Sheet of	
File: D:\公司資料\99se\MyDesign.ddb	Drawn By:	

CAP value 0.1uF ~ 1uF



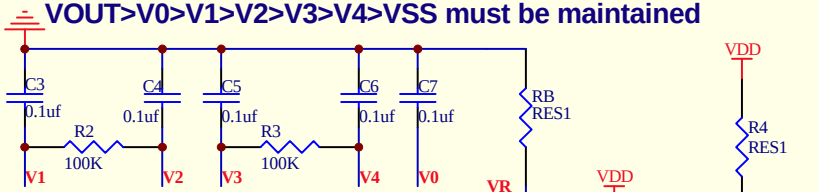
2X: put C0 and C1,short R1

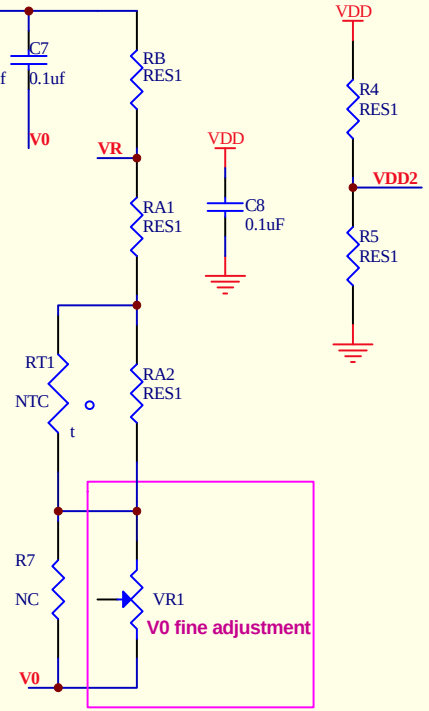
3X: put C0 and C1 C2,open R1

VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

VOUT Voltage should not higher than 8V

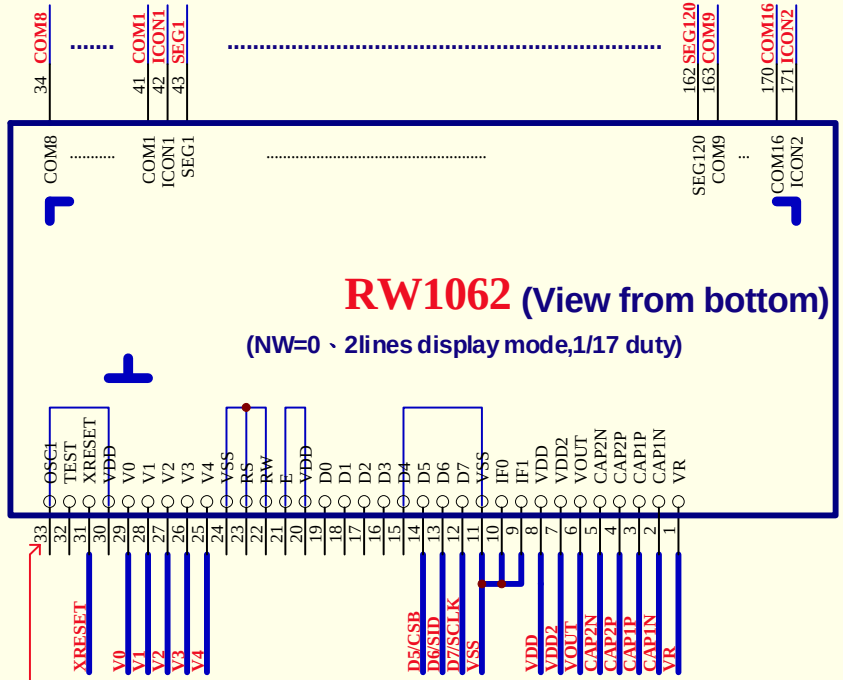
VOUT>V0>V1>V2>V3>V4>VSS must be maintained





V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)
VLCD=V0-VSS

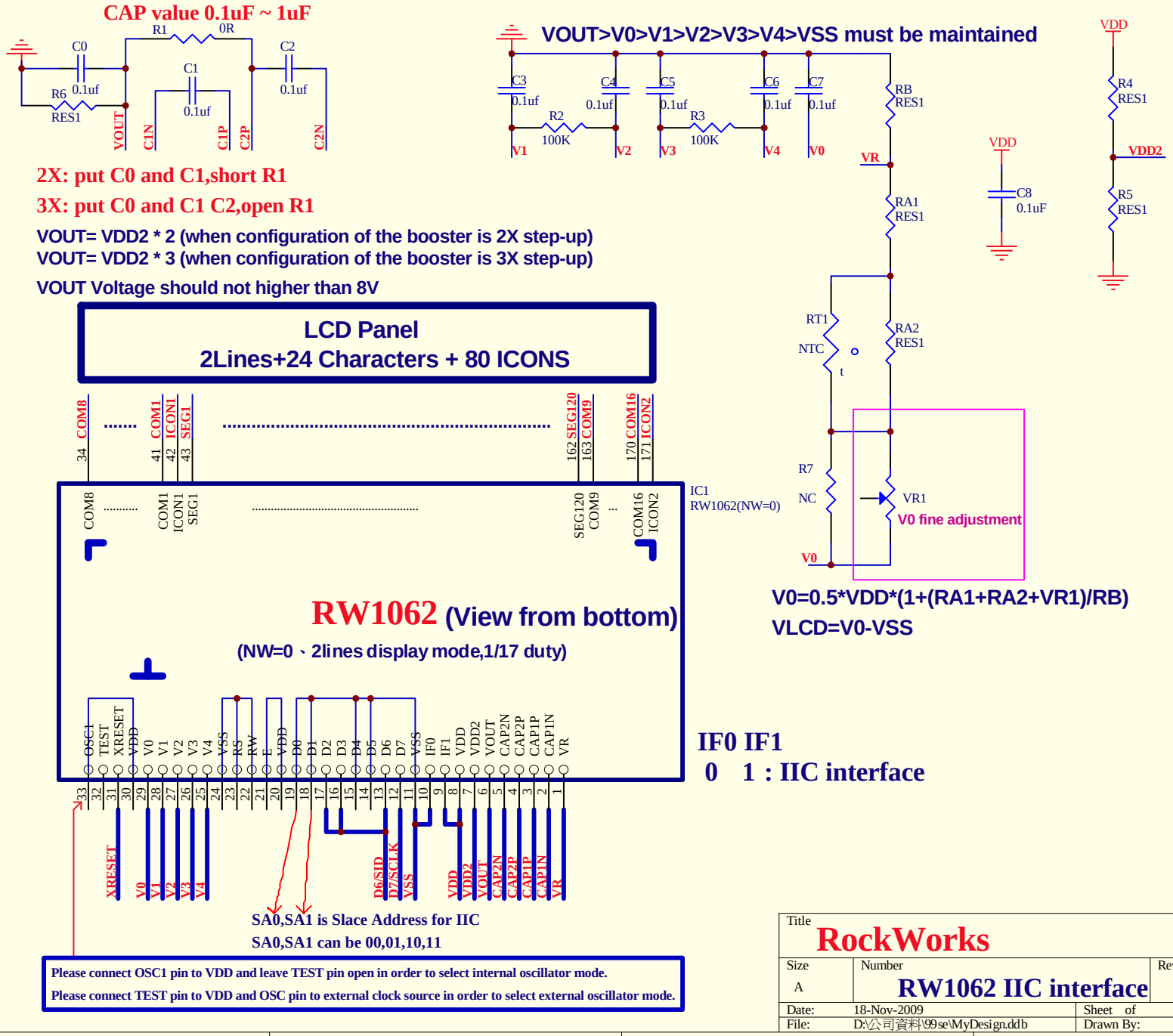
LCD Panel
2Lines+24 Characters + 80 ICONS



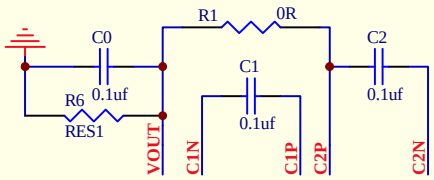
IF0 IF1
0 0 : 3-SPI interface

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

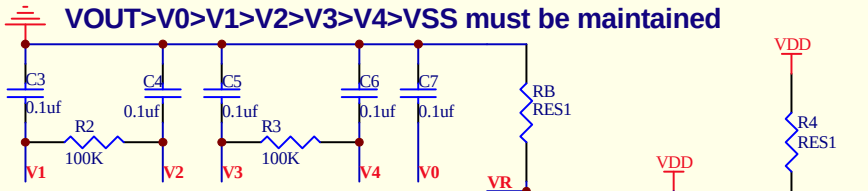
Title: **RockWorks**		
Size: A	Number: **RW1062 3-SPI interface**	Revision: **B**
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:


CAP value 0.1uF ~ 1uF
C0
R1
0R
C2
C1
R6
0.1uf
RES1
0.1uf
0.1uf
VOUT
C1N
C1P
C2P
C2N
VOUT>V0>V1>V2>V3>V4>VSS must be maintained
C3
C4
C5
C6
C7
0.1uf
R2
100K
R3
100K
V1
V2
V3
V4
V0
RB
RES1
VR
RA1
RES1
RT1
NTC
t
RA2
RES1
R7
NC
VR1
V0 fine adjustment
V0
VDD
C8
0.1uF
VDD
R4
RES1
VDD2
R5
RES1
2X: put C0 and C1,short R1
3X: put C0 and C1 C2,open R1
VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)
VOUT Voltage should not higher than 8V
LCD Panel
2Lines+24 Characters + 80 ICONS
34 COM8
41 COM1
42 ICON1
43 SEG1
162 SEG120
163 COM9
170 COM116
171 ICON2
IC1
RW1062(NW=0)
RW1062 (View from bottom)
(NW=0、2lines display mode,1/17 duty)
OSC1 TEST XRESET VDD V0 V1 V2 V3 V4 VSS RS RW E VDD D0 D1 D2 D3 D4 D5 D6 D7 VSS IF0 IF1 VDD VDD2 VOUT CAP2N CAP2P CAP1P CAP1N VR
33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
XRESET
V0 V1 V2 V3 V4
D6/SID D7/SCLK VSS
VDD VDD2 VOUT CAP2N CAP2P CAP1P CAP1N VR
V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)
VLCD=V0-VSS
IF0 IF1
0 1 : IIC interface
SA0,SA1 is Slace Address for IIC
SA0,SA1 can be 00,01,10,11
Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.
Title
RockWorks
Size
A
Number
RW1062 IIC interface
Revision
B
Date: 18-Nov-2009
Sheet of
File: D:\公司資料\99se\MyDesign.ddb
Drawn By:

CAP value 0.1uF ~ 1uF



VOUT>V0>V1>V2>V3>V4>VSS must be maintained



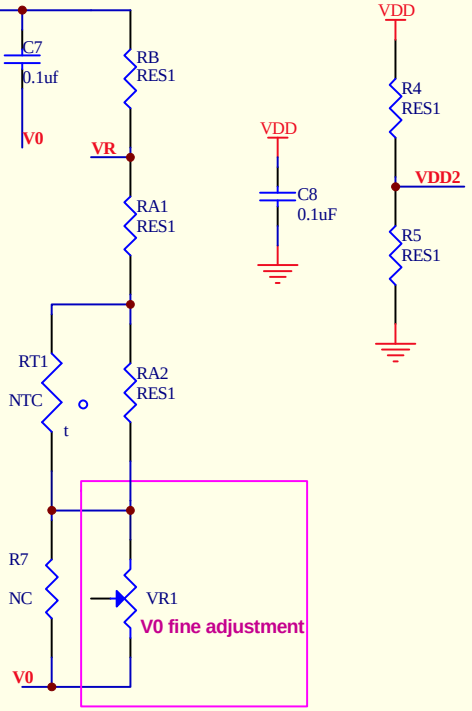
2X: put C0 and C1,short R1

3X: put C0 and C1 C2,open R1

VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)

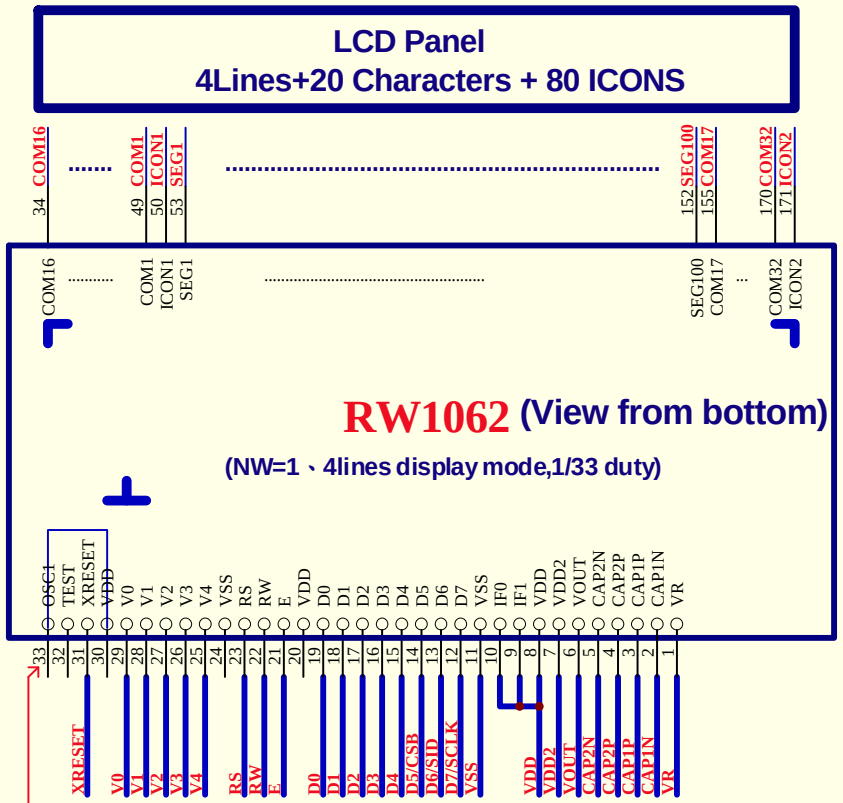
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

VOUT Voltage should not higher than 8V



V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)

VLCD=V0-VSS



IF0 IF1

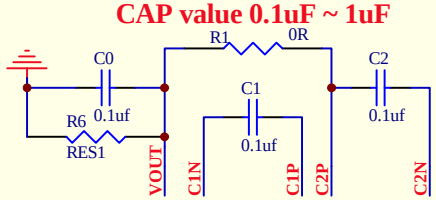
1 1 : 8-bit 6800 interface

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.

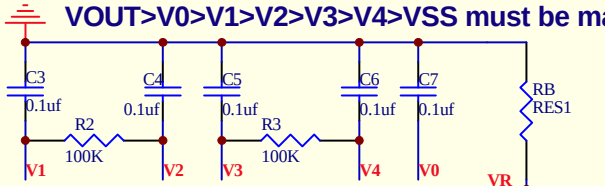
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

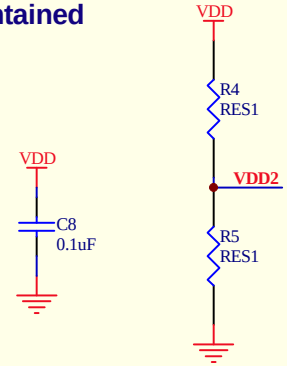
Title: RockWorks		
Size: A	Number: RW1062 8 bit 6800 interface	Revision: B
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

CAP value 0.1uF ~ 1uF



VOUT>V0>V1>V2>V3>V4>VSS must be maintained





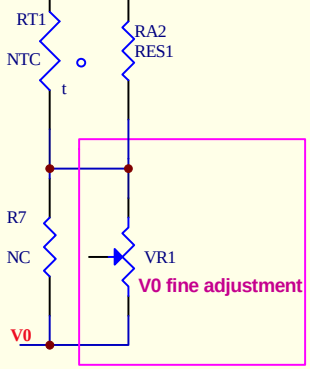
2X: put C0 and C1,short R1

3X: put C0 and C1 C2,open R1

VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)

VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

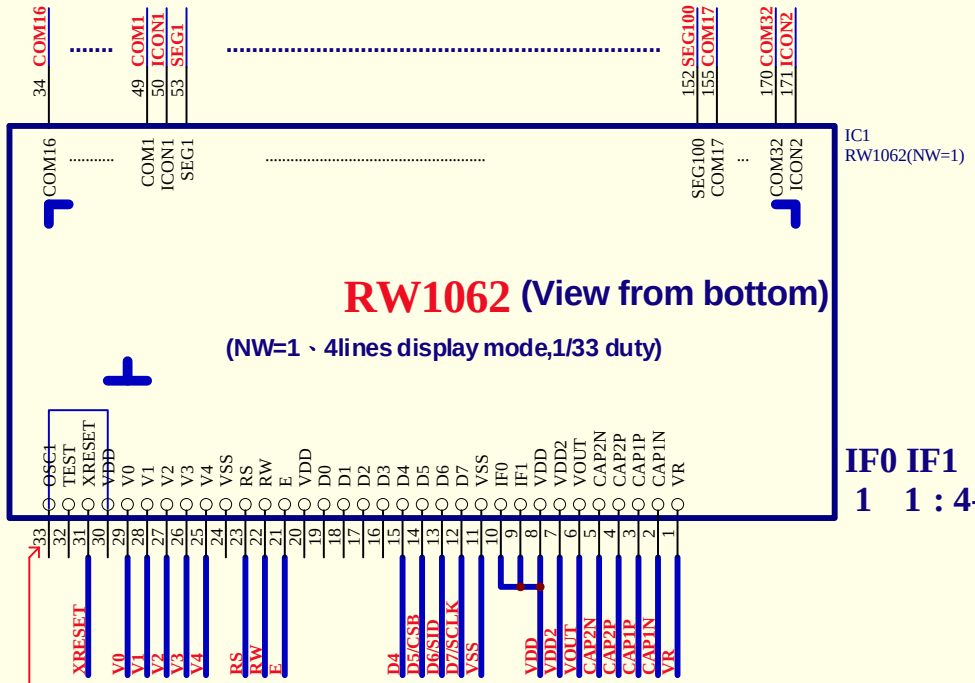
VOUT Voltage should not higher than 8V



V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)

VLCD=V0-VSS

LCD Panel
4Lines+20 Characters + 80 ICONS



IF0 IF1

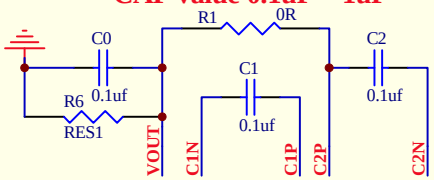
1 1 : 4-bit 6800 interface

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.

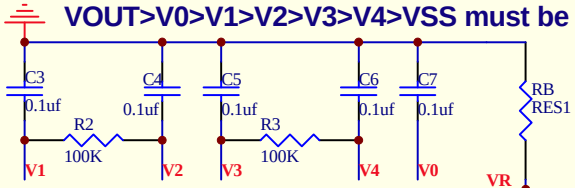
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

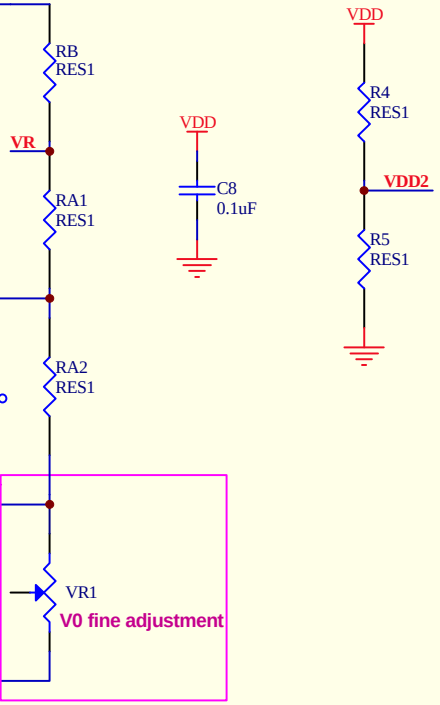
Title: RockWorks		
Size: A	Number: RW1062 4 bit 6800 interface	Revision: B
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

CAP value 0.1uF ~ 1uF



VOUT>V0>V1>V2>V3>V4>VSS must be maintained





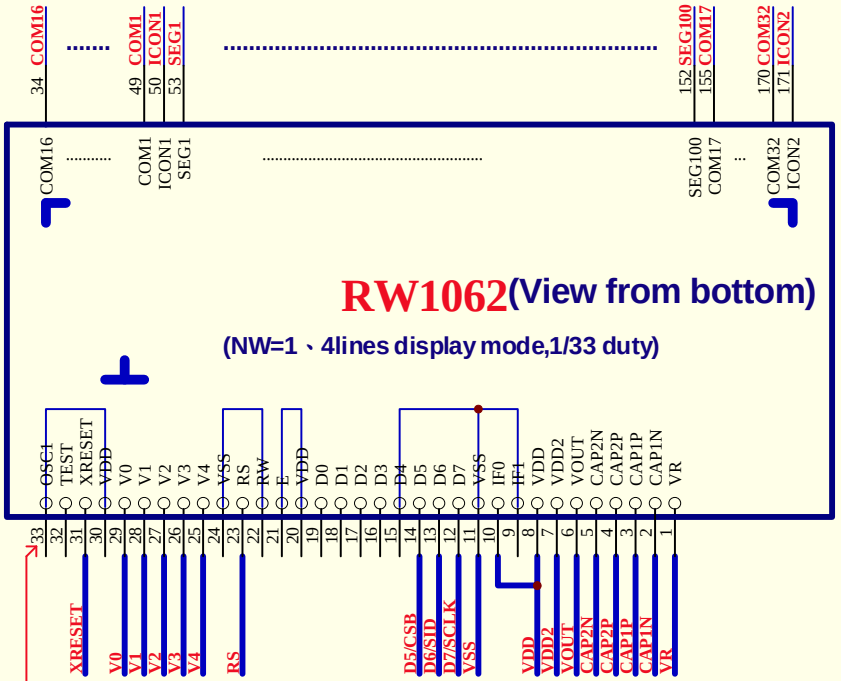
2X: put C0 and C1,short R1

3X: put C0 and C1 C2,open R1

VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

VOUT Voltage should not higher than 8V

LCD Panel
4Lines+20 Characters + 80 ICONS

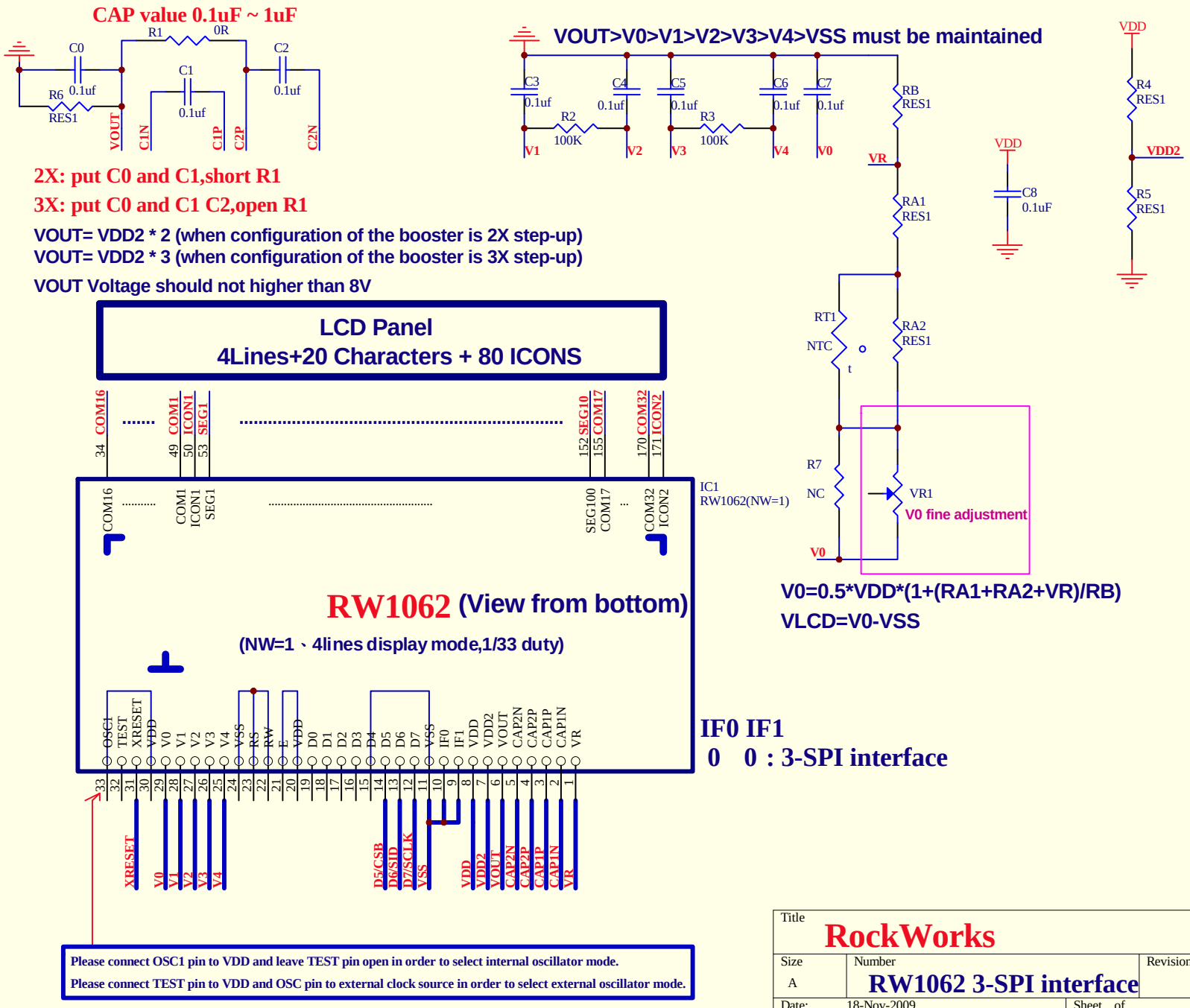


V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)
VLCD=V0-VSS

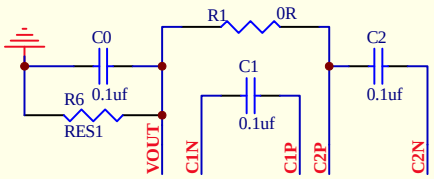
IF0 IF1
1 0 : 4-SPI interface

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

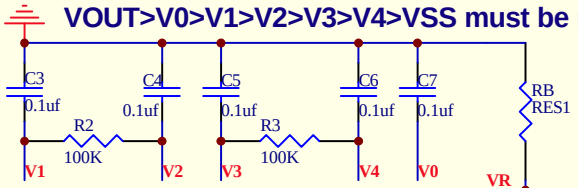
Title: **RockWorks**		
Size: A	Number: **RW1062 4-SPI interface**	Revision: **B**
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

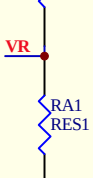

CAP value 0.1uF ~ 1uF
C0
R1
0R
C2
C1
R6
0.1uf
RES1
0.1uf
0.1uf
VOUT
C1N
C1P
C2P
C2N
VOUT>V0>V1>V2>V3>V4>VSS must be maintained
C3
C4
C5
C6
C7
0.1uf
R2
100K
R3
100K
V1
V2
V3
V4
V0
RB
RES1
VR
RA1
RES1
RT1
NTC
t
RA2
RES1
R7
NC
VR1
V0 fine adjustment
V0
VDD
C8
0.1uF
VDD
R4
RES1
VDD2
R5
RES1
2X: put C0 and C1,short R1
3X: put C0 and C1 C2,open R1
VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)
VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)
VOUT Voltage should not higher than 8V
LCD Panel
4Lines+20 Characters + 80 ICONS
34 COM16
49 COM1
50 ICON1
53 SEG1
152 SEG10
155 COM17
170 COM32
171 ICON2
IC1
RW1062(NW=1)
RW1062 (View from bottom)
(NW=1、4lines display mode,1/33 duty)
OSC1 TEST XRESET VDD V0 V1 V2 V3 V4 VSS RS RW E VDD D0 D1 D2 D3 D4 D5 D6 D7 VSS IF0 IF1 VDD VDD2 VOUT CAP2N CAP2P CAP1P CAP1N VR
33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
XRESET V0 V1 V2 V3 V4 D5/CSB D6/SID D7/SCLK VSS VDD VDD2 VOUT CAP2N CAP2P CAP1P CAP1N VR
V0=0.5*VDD*(1+(RA1+RA2+VR)/RB)
VLCD=V0-VSS
IF0 IF1
0 0 : 3-SPI interface
Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.
Title
RockWorks
Size
A
Number
RW1062 3-SPI interface
Revision
B
Date: 18-Nov-2009
Sheet of
File: D:\公司資料\99se\MyDesign.ddb
Drawn By:

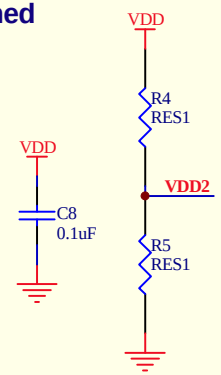
CAP value 0.1uF ~ 1uF



VOUT>V0>V1>V2>V3>V4>VSS must be maintained







2X: put C0 and C1,short R1

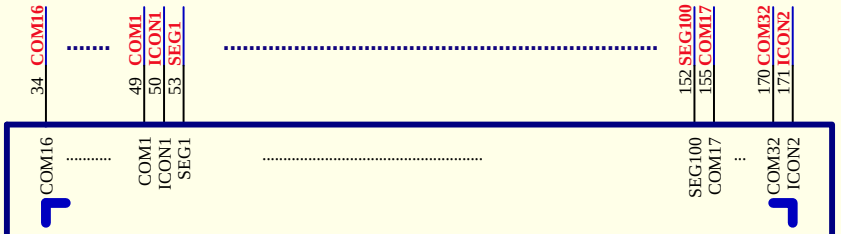
3X: put C0 and C1 C2,open R1

VOUT= VDD2 * 2 (when configuration of the booster is 2X step-up)

VOUT= VDD2 * 3 (when configuration of the booster is 3X step-up)

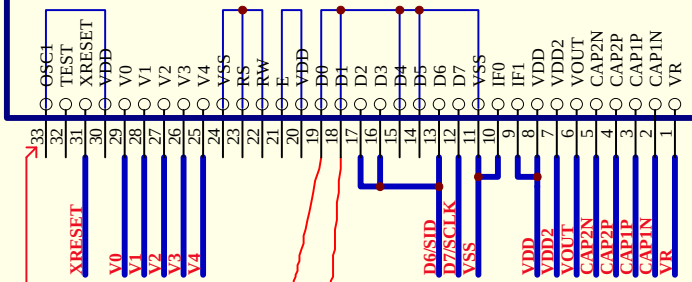
VOUT Voltage should not higher than 8V

LCD Panel
4Lines+20 Characters + 80 ICONS



RW1062 (View from bottom)

(NW=1、4lines display mode,1/33 duty)



V0=0.5*VDD*(1+(RA1+RA2+VR1)/RB)

VLCD=V0-VSS

IF0 IF1
0 1 : IIC interface

SA0,SA1 is Slace Address for IIC
SA0,SA1 can be 00,01,10,11

Please connect OSC1 pin to VDD and leave TEST pin open in order to select internal oscillator mode.
Please connect TEST pin to VDD and OSC pin to external clock source in order to select external oscillator mode.

Title: **RockWorks**		
Size: A	Number: **RW1062 IIC interface**	Revision: **B**
Date: 18-Nov-2009		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By: