1. General description

The RW1033 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segment. The RW1033 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I2C-bus or 3-SPI, 4-SPI and 8-bit parallel interface. Communication overheads are minimized by a display RAM with auto-incremental addressing, by display memory switching (static and duplex drive modes).

2. Features

- Single-chip LCD controller and driver
- Selectable Interface : Both 6800 and 8080 series MPU can directly connected by 8-bit parallel interface, also 4 line / 3 line serial interface and IIC interface are supportable.
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, 1⁄2 or 1⁄3
- Selectable Type-A or Type-B Waveform by Sofeware
- Selectable frame frequency: 82 Hz or 110 Hz
- Internal LCD bias generation with voltage-follower buffers
- 80 segment drives:
- Up to 40 7-segment numeric characters
- Up to 21 14-segment alphanumeric characters
- Any graphics of up to 320 elements
- 80 x 4 bit RAM for display data storage
- Auto-incremental display data
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 2.4 V to 5.5 V
- VLCD range : from 2.4 V to 5.5 V
- Low power consumption
- 400 kHz I2C-bus interface
- No external components
- Compatible with Chip-On-Glass (COG) technology
- Manufactured using silicon gate CMOS process

3. PAD Arrangement

TBD

4. PAD Coordinate

TBD

5. Block diagram

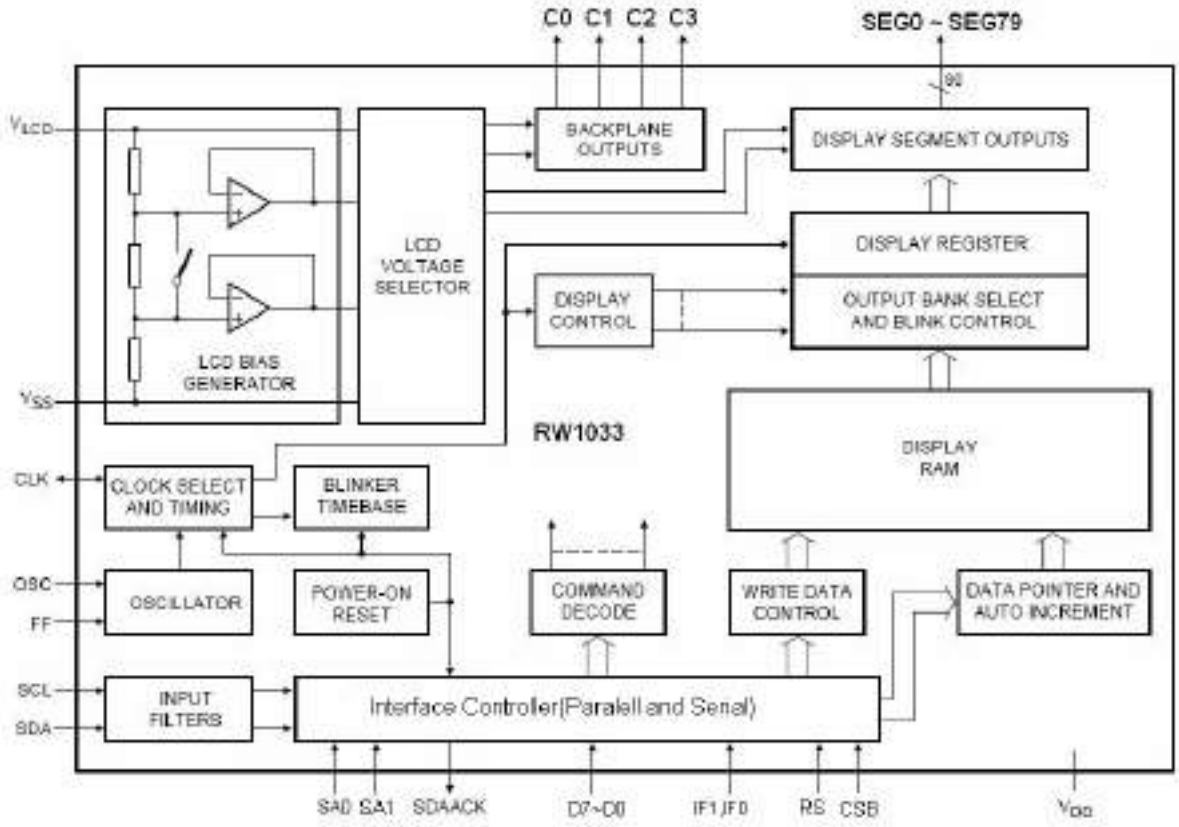


Fig.1 Block Diagram of RW1033

6. Pin Description

Pin Name	Pin Description
SDAACK	I2C-bus acknowledge output
SDA	I2C-bus serial data input
SCL	I2C-bus serial clock input
CSB	chip select pin
RS	data/command select pin for 4-SPI
CLK	clock input/output
VDD	supply voltage
SYNC	cascade synchronization input/output
OSC	oscillator select
FF	frame frequency select
SA0	I2C-bus slave address input
SA1	I2C-bus slave address input
IF1,IF0	Interface select Pins
VSS	ground supply voltage
V0	LCD supply voltage
C2, C0, C3 and C1	LCD backplane output
SEG0 to SEG79	LCD segment output
D0 to D7	data bus pads for 8-bit parallel interface

7. Functional description

The RW1033 is a versatile peripheral device designed to interface between any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 segments.
The display configurations possible with the RW1033 depend on the required number of active backplane outputs. A selection of display configurations is shown in Table 4.
All of the display configurations can be implemented in a typical system as shown in Figure 2.

Table 1. Possible display configurations

Number of		7-segment numeric		14-segment numeric		Dot matrix
Backplanes	Elements	Digits	Indicator symbols	Characters	Indicator symbols	
4	320	40	40	20	40	320 (4 × 80)
3	240	30	30	16	16	240 (3 × 80)
2	160	20	20	10	20	160 (2 × 80)
1	80	10	10	5	10	80 (1 × 80)

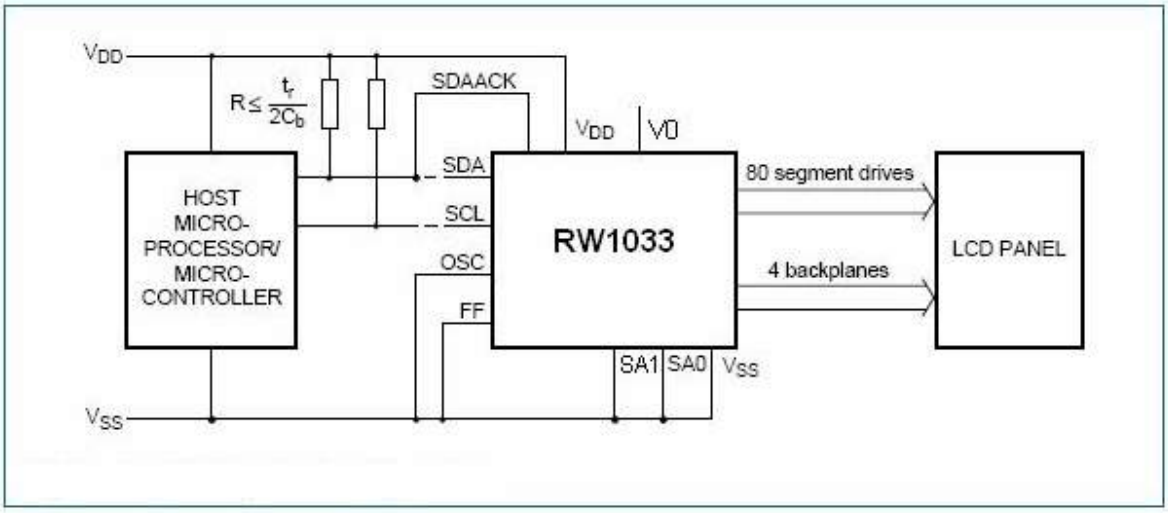


Fig.2 Typical System Configuration

The host microprocessor or microcontroller maintains the 2-line I2C-bus communication channel with the RW1033.

The internal oscillator is selected by connecting pin OSC to VSS. The only other connections required to complete the system are the power supplies (VDD, VSS and VLCD) and the LCD panel selected for the application.

7.1 Power-on reset

At power-on the RW1033 resets to the following starting conditions:

- All backplane and segment outputs are set to VSS
- The selected drive mode is 1:4 multiplex with 1⁄3 bias
- Blinking is switched off
- Input and output bank selectors are reset
- The bus interface is initialized
- The display is disabled

Remark: Do not transfer data on the bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors between VLCD and VSS. The center resistor can be bypassed to provide a 1⁄2 bias voltage level for the 1:2 multiplex configuration.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by mode-set commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of VLCD and the resulting discrimination ratios (D), are given in Table 2.

Table 2. Discrimination ratios

LCD drive mode	Number of:		LCD bias configuration
	Backplanes	Levels	
static	1	2	static
1:2 multiplex	2	3	1/2
1:2 multiplex	2	4	1/3
1:3 multiplex	3	4	1/3
1:4 multiplex	4	4	1/3

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 3.

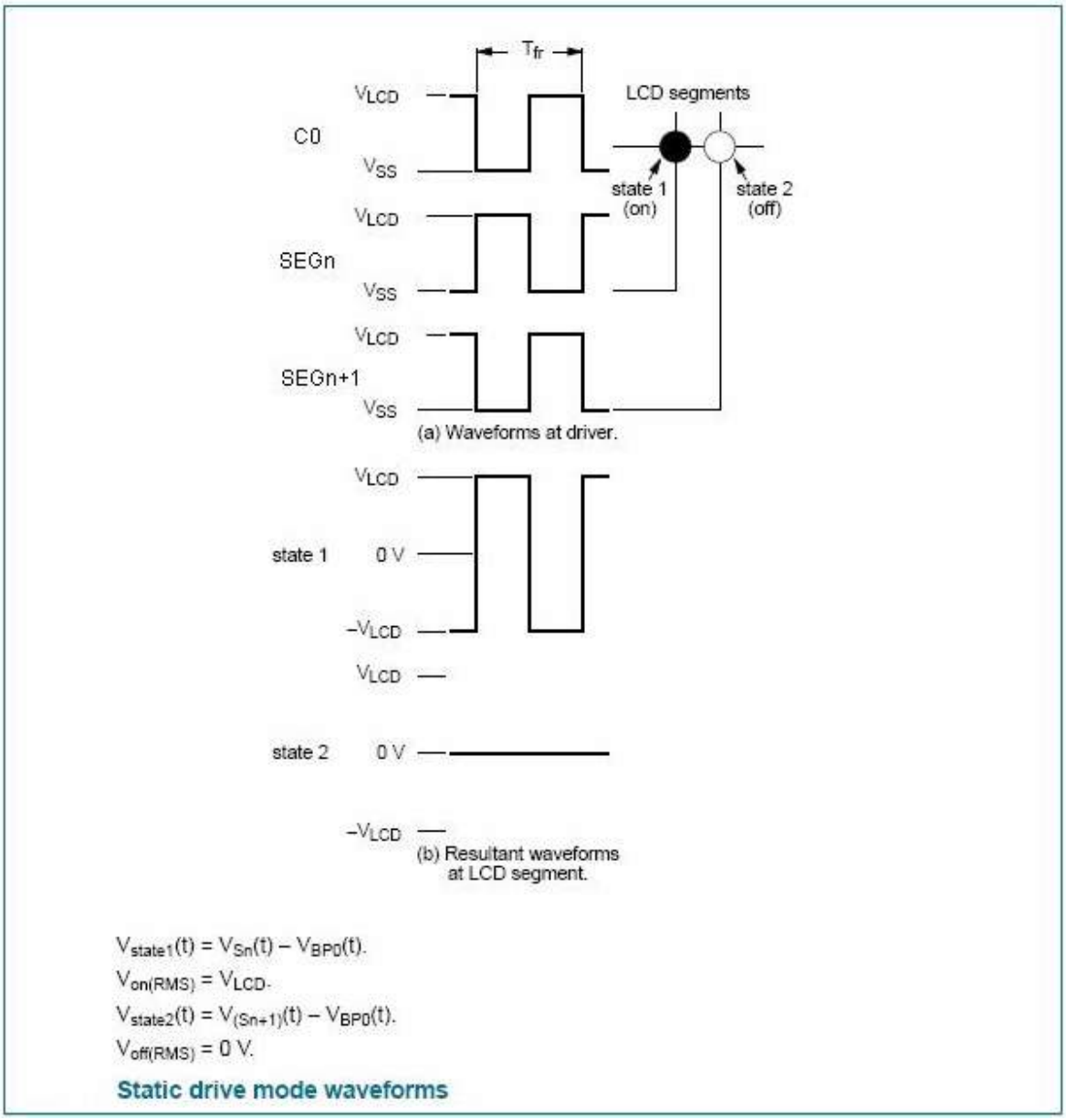


Fig 3

7.4.2 1:2 multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The RW1033 allows the use of 1⁄2 bias or 1⁄3 bias in this mode as shown in Figure 4 and Figure 5.

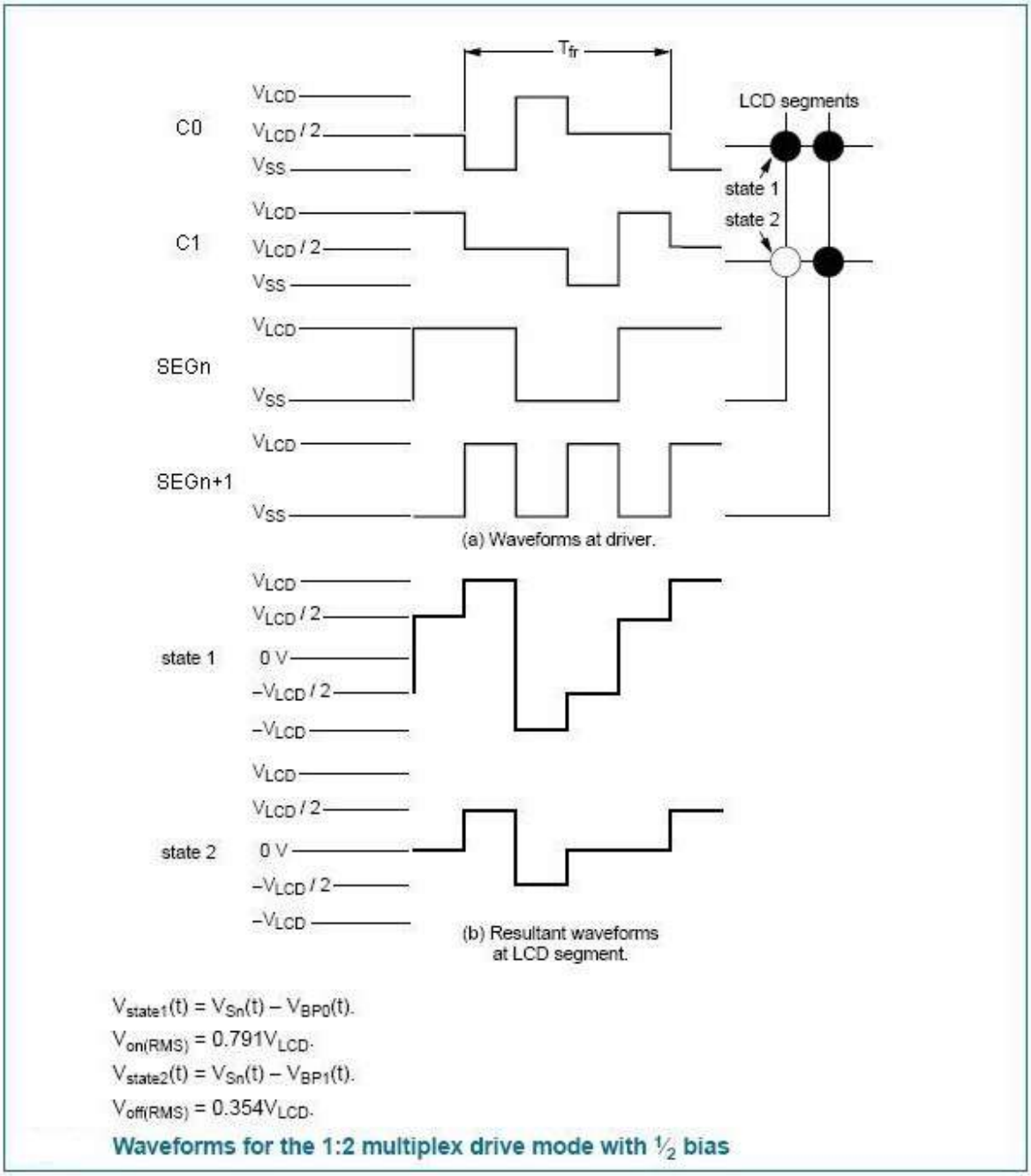


Fig 4-1 Type-A Waveform

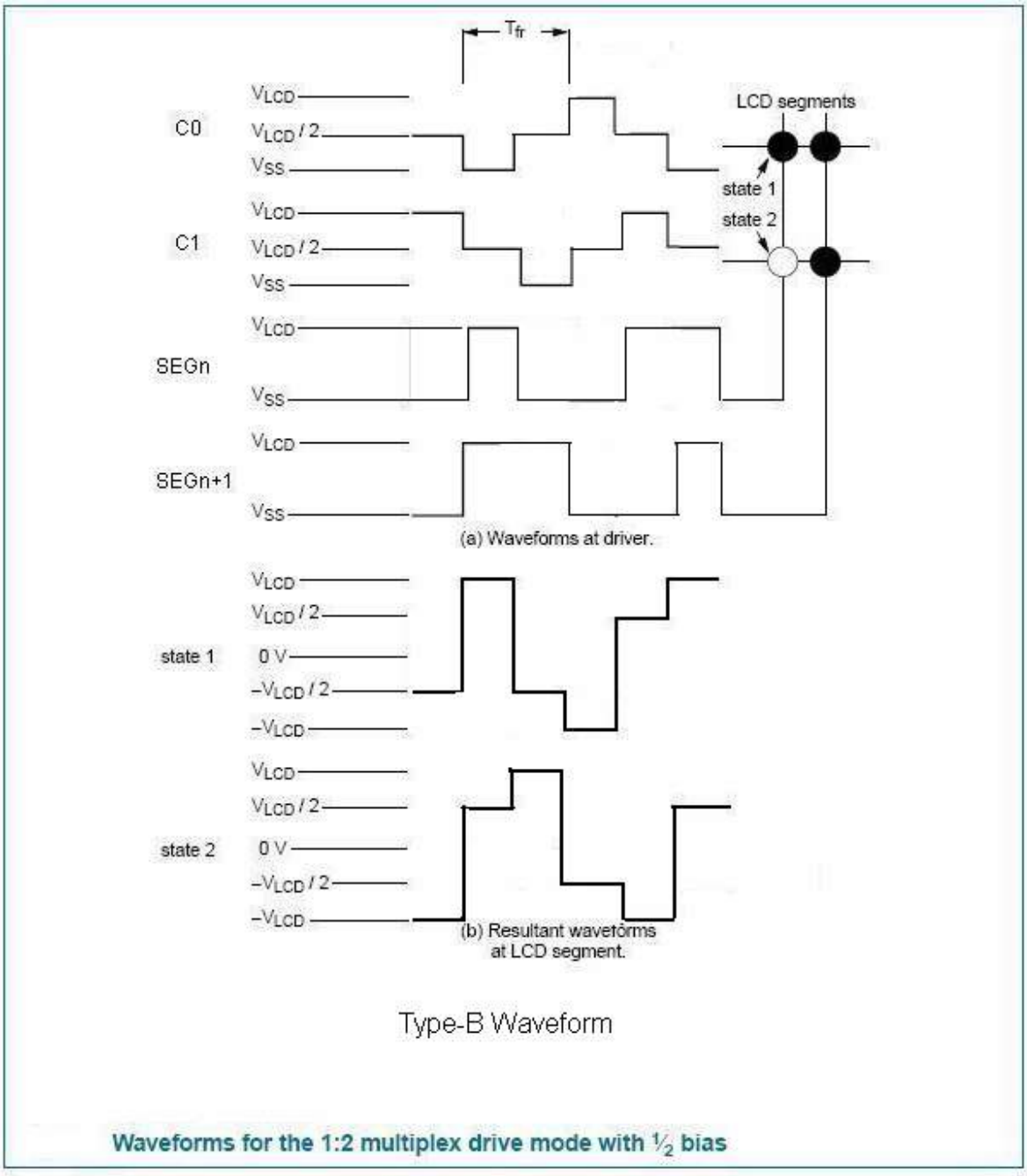
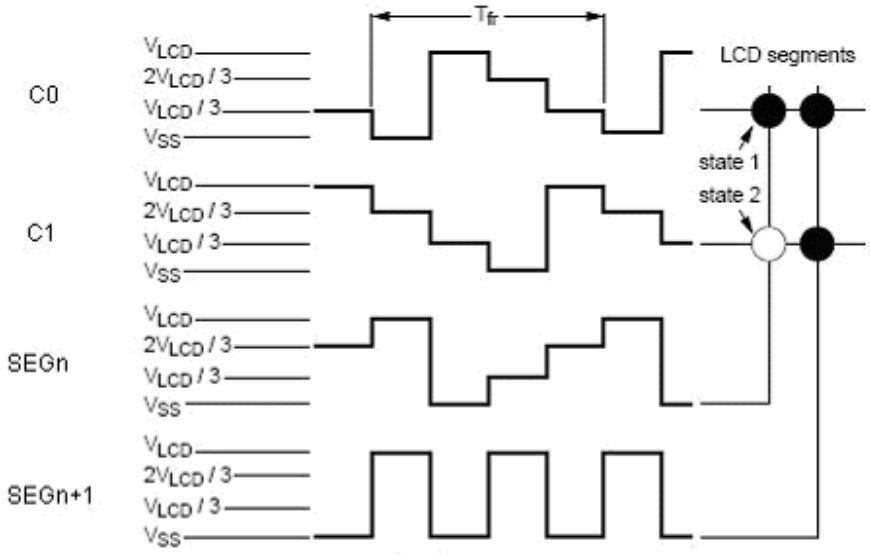
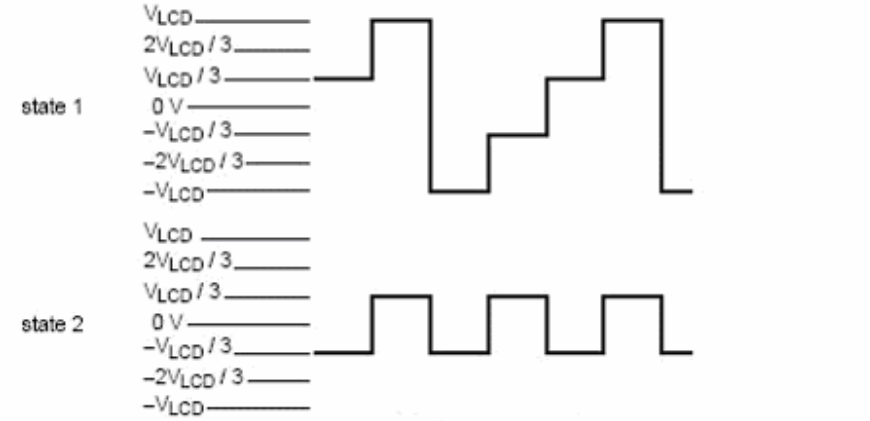


Fig. 4-2 Type-B Waveform



(a) Waveforms at driver.



(b) Resultant waveforms at LCD segment.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias

Fig. 5 Type-A Waveform

7.4.3 1:3 multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 6.

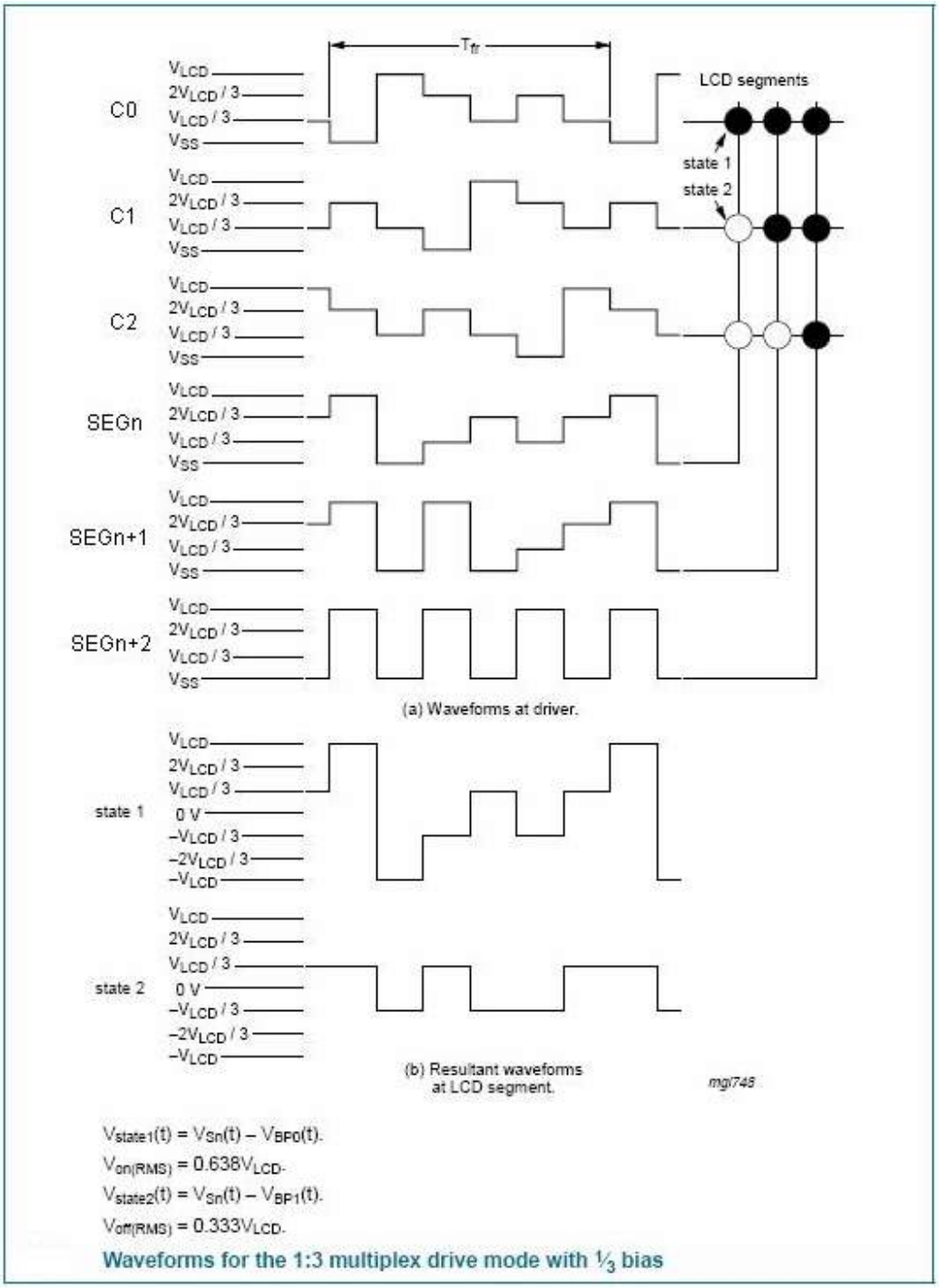


Fig. 6 Type-A Waveform

7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 7.

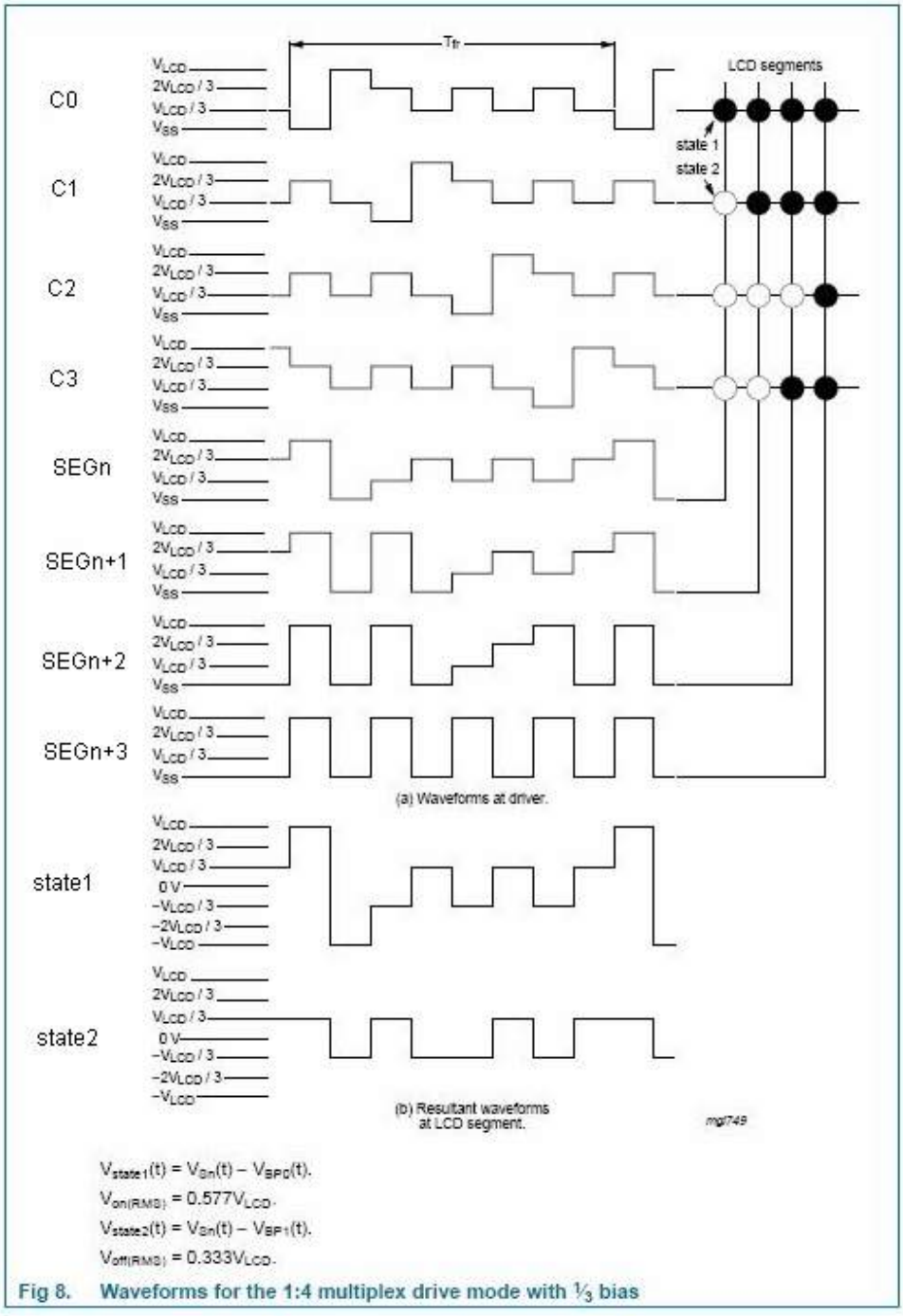


Fig. 7 Type-A Waveform

7.5 Oscillator

The internal logic and the LCD drive signals of the RW1033 are timed by a frequency f_{clk} which either is derived from the built-in oscillator frequency f_{osc}:

$$f_{clk} = TBD \quad (4)$$

or equals an external clock frequency $f_{clk(ext)}$:

$$f_{clk} = TBD \quad (5)$$

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to V_{SS}. In this case the output from pin CLK provides the clock signal for cascaded RW1033s in the system. After power-up, pin SDA must be HIGH to guarantee that the clock starts.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.
A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

7.6 Timing

The clock frequency f_{clk} determines the LCD frame frequency f_{fr} and is calculated as follows:

$$f_{fr} = TBD \quad (6)$$

The internal clock frequency f_{clk} can be selected using pin FF. As a result 2 frame frequencies are available: 82 Hz or 110 Hz (typical), see Table 3.

Table 3. LCD frame frequencies

Pin FF tied to	LCD frame frequency (Hz)
V_{DD}	82
V_{SS}	110

The timing of the RW1033 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs.

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs and one column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 80 segment outputs are required the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs: COM0 to COM3. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In the 1:4 multiplex drive mode COM0 to COM3 must be connected directly to the LCD. If less than four backplane outputs are required the unused outputs can be left open-circuit.
- In 1:3 multiplex drive mode COM3 carries the same signal as COM1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode COM0 and COM2, COM1 and COM3 respectively carry the same signals and may also be paired to increase the drive capabilities.
- In static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 80 × 4 bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map Figure 8 shows rows 0 to 3 which correspond with the backplane outputs COM0 to COM3, and columns 0 to 79 which correspond with the segment outputs S0 to S79. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with COM0, COM1, COM2 and COM3 respectively.
When display data is transmitted to the RW1033 the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 9; the RAM filling organization depicted applies equally to other LCD types.
The following applies to Figure 9:

- In static drive mode the eight transmitted data bits are placed into row 0 of eight successive 4-bit RAM words.
- In 1:2 multiplex mode the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In 1:3 multiplex mode the eight bits are placed in triples into row 0, 1 and 2 of three successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In the 1:4 multiplex mode the eight transmitted data bits are placed in quadruples into row 0, 1, 2 and 3 of two successive 4-bit RAM words.

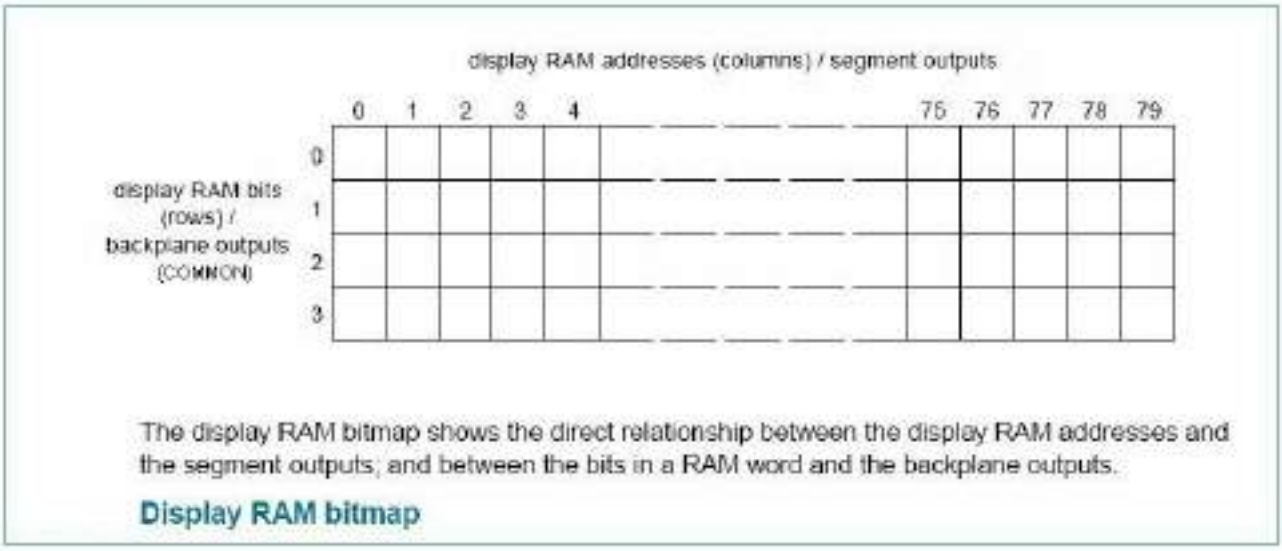


Fig.8

7.11 Data pointer

The addressing mechanism for the display RAM is realized using a data pointer.
This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command.
Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 9.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:
• In static drive mode by eight
• In 1:2 multiplex drive mode by four
• In 1:3 multiplex drive mode by three
• In 1:4 multiplex drive mode by two
If an I2C-bus data access is terminated early then the state of the data pointer is unknown. The data pointer must be re-written prior to further RAM accesses.

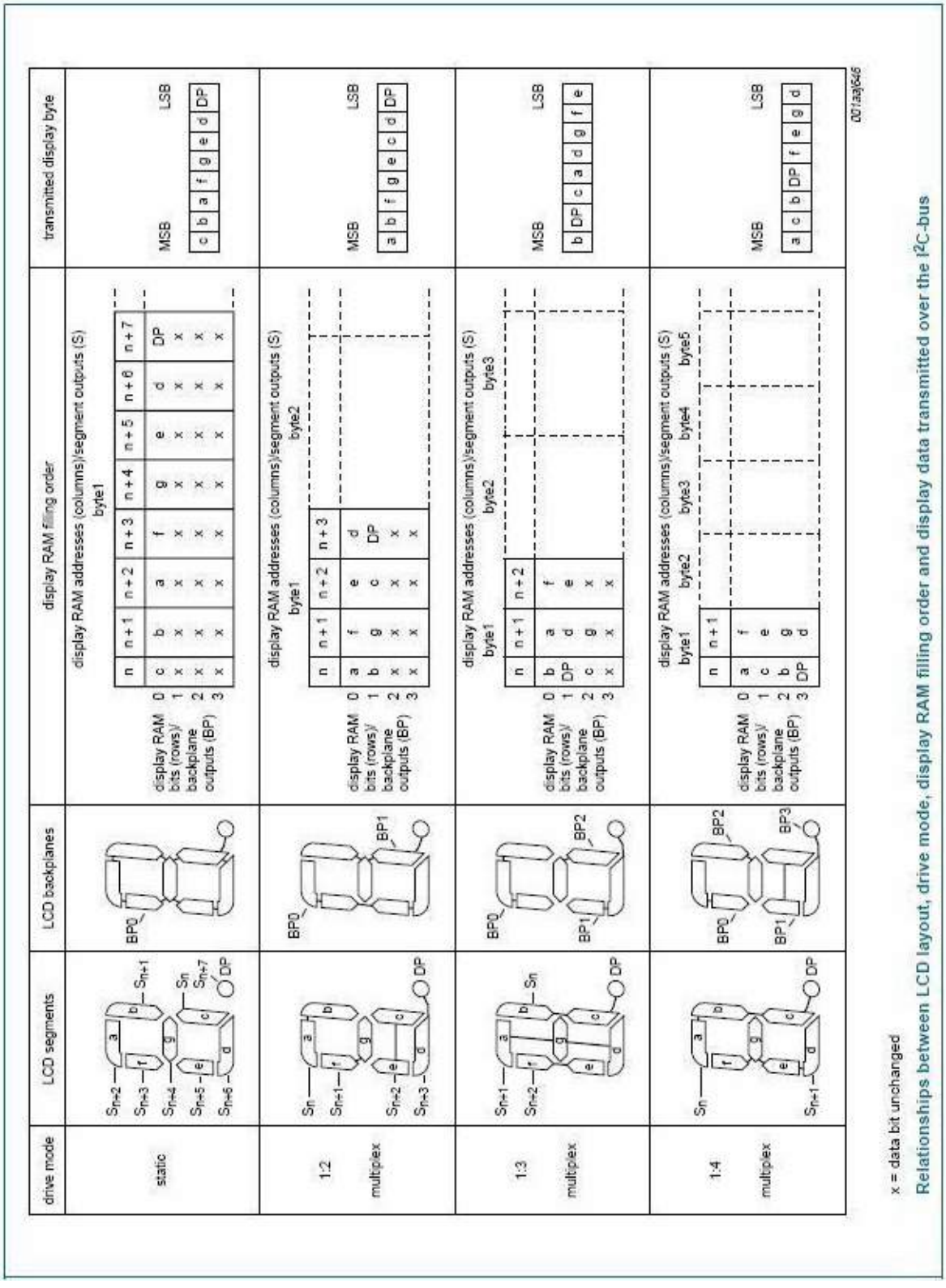

drive mode
LCD segments
LCD backplanes
display RAM filling order
transmitted display byte
static
1:2 multiplex
1:3 multiplex
1:4 multiplex
display RAM addresses (columns)/segment outputs (S)
byte1
byte2
byte3
byte4
byte5
display RAM bits (rows)/ backplane outputs (BP)
MSB
LSB
x = data bit unchanged
Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I2C-bus
007aaj646

Fig. 9

7.12 Output bank selector

The output bank selector selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, row 2 and then row 3
- In 1:3 multiplex mode, rows 0, 1 and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The RW1033 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.13 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

7.14 Blinker

The display blinking capabilities of the RW1033 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 9.1). The blink frequencies are fractions of the clock frequency. The ratios between the clock and blink frequencies depend on the blink mode in which the device is operating (see Table 4).

Table 4. Blink frequencies

Blink mode	Blink frequency with respect to f_{clk} (typical)		Unit
	Frame Frequency = 80Hz	Frame Frequency = 110Hz	
off	blinking off	blinking off	Hz
1	2.5	3.5	Hz
2	1.3	1.7	Hz
3	0.6	0.9	Hz

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.
In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can blink by selectively changing the display RAM data at fixed time intervals.

If the entire display can blink at a frequency other than the typical blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 9.1).

MPU Interface

7.15 Characteristics of the 8-bit Parallel interface

With the RW1033 chip, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SDA). Through selecting the IF1,IF0 terminal polarity to the "H" or "L" it is possible to select either parallel
data input or serial data input as shown in Table 5.

Table 5

Interface	IF1	IF0	CSB	RS	SDA	SCLK	SDAACK	SA1,SA0	D7~D0
6800	H	H	CS1B	RS	E	RW	-	-	D7~D0
8080	H	L	CS1B	RS	XRD	XWR	-	-	D7~ D0
4SPI	L	H	CS1B	RS	SDA	SCLK	-	-	-
3SPI	L	H	CS1B	L	SDA	SCLK	-	-	-
IIC	L	L	—	—	SDA	SCLK	acknowledge	Slave addr.	-

"—" indicates fixed to either "H" or to "L"

The Parallel Interface

When the parallel interface has been selected (PSB="H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (shown in Table 6) by selecting the C86 terminal to either "H" or to "L".

Table 6

IF1=H	CSB	RS	SDA	SCLK	D7~D0
H: 6800 Series	CSB	RS	E	RW	D7~D0
L: 8080 Series	CSB	A0	XRD	XWR	D7~D0

Moreover, data bus signals are recognized by a combination of A0, XRD (E), XWR (RW) signals, as shown in Table 7

Table 7

Shared	6800 Series	8080 Series		Function
RS	RW(SCLK)	XRD(SDA)	XWR(SCLK)	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

7.16 Characteristics of the I2C-bus

The I2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.
By connecting pin SDAACK to pin SDA on the RW1033, the SDA line becomes fully I2C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications1. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the RW1033 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 10).

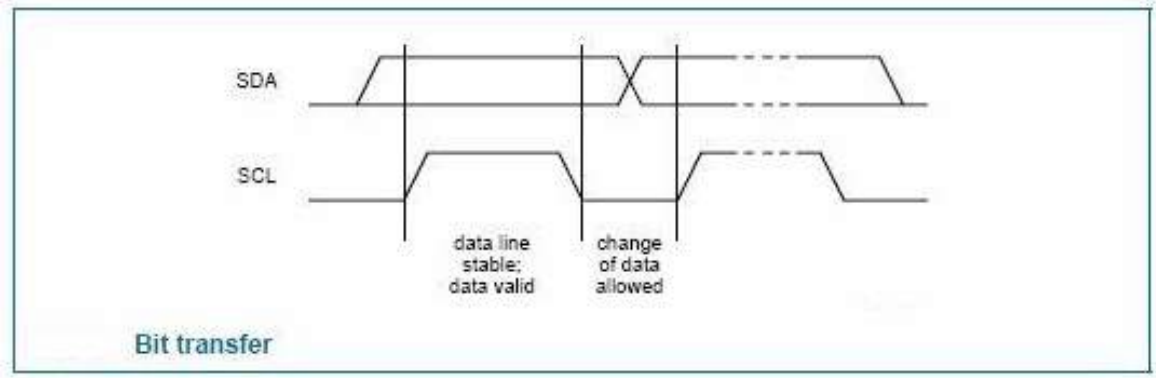


Fig. 10

7.16.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.
A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).
A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).
The START and STOP conditions are shown in Figure 11.

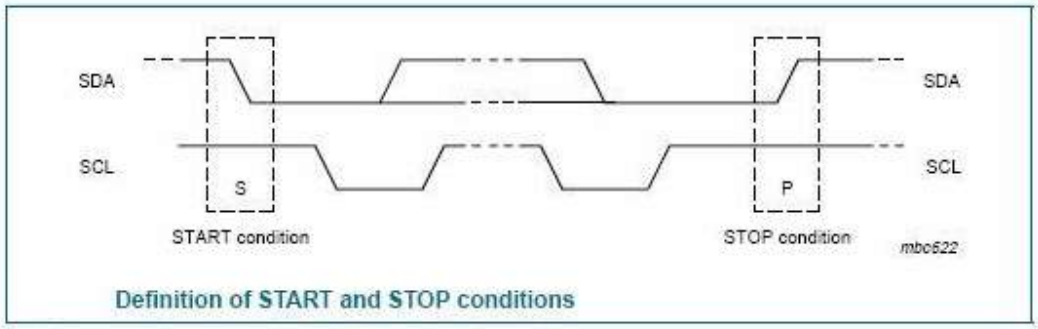


Fig. 11

7.16.2 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 12.

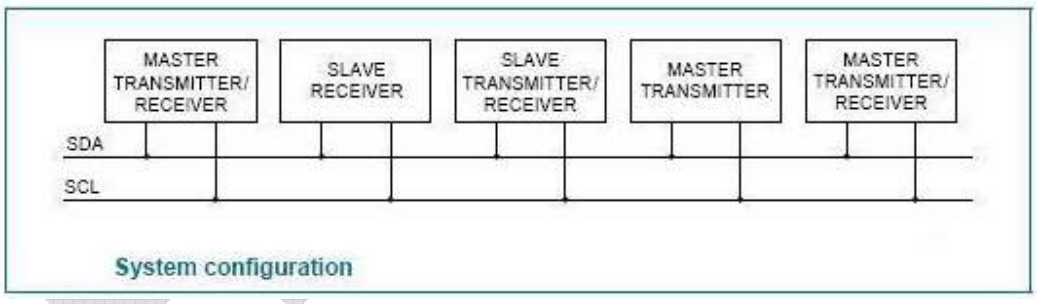


Fig. 12

7.16.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I2C-bus is shown in Figure 13

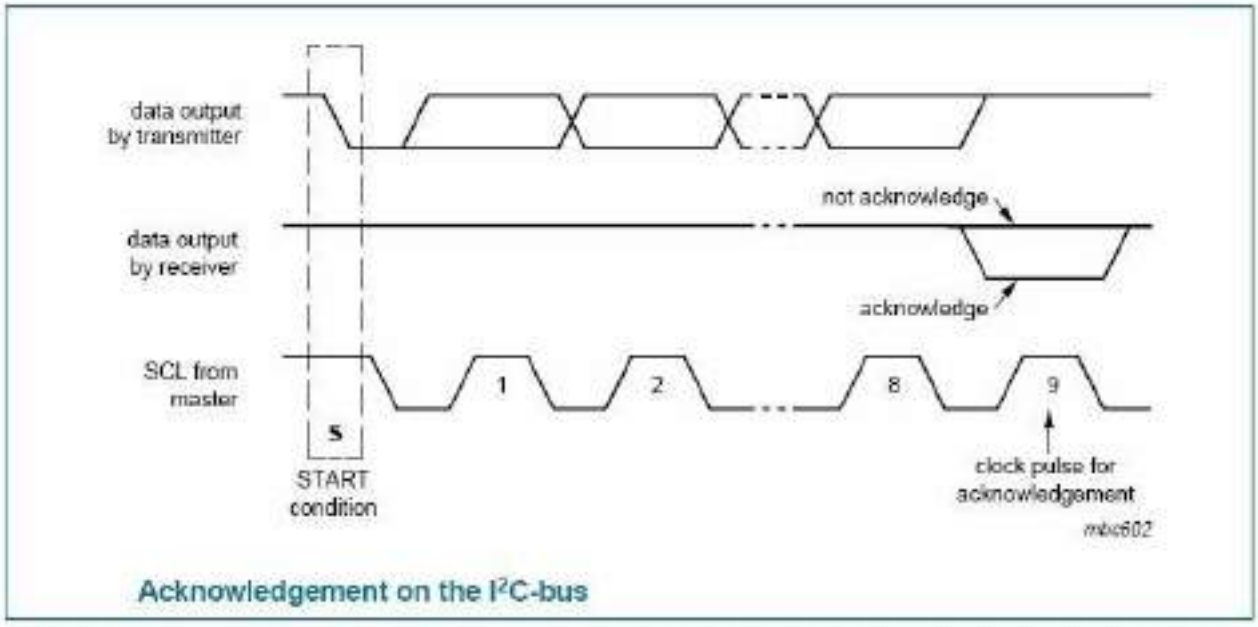


Fig. 13

7.16.4 I2C-bus controller

The RW1033 acts as an I2C-bus slave receiver. It does not initiate I2C-bus transfers or transmit data to an I2C-bus master receiver. The only data output from the RW1033 are the acknowledge signals from the selected devices. Device selection depends on the I2C-bus slave address, on the transferred command data.

7.16.5 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.6 I2C-bus protocol

Four I2C-bus slave addresses (0111 000 and 0111 001 and 0111 010 and 0111 011) are reserved for the RW1033.
The least significant bit of the slave address is bit R/W. The RW1033 is a write-only device and will not respond to a read access, so this bit should always be logic 0. The second bit of the slave address is defined by the level tied at input SA1,SA0. Two types of RW1033 can be distinguished on the same I2C-bus which allows:

- The use of two types of LCD multiplex on the same I2C-bus

The I2C-bus protocol is shown in Figure 14. The sequence is initiated with a START condition (S) from the I2C-bus master which is followed by one of two possible RW1033 slave addresses available. All RW1033s with the corresponding SA1,SA0 level acknowledge in parallel to the slave address, but all RW1033 with the alternative SA1,SA0 level ignore the whole I2C-bus transfer.
After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data.
In this way it is possible to configure the device and then fill the display RAM with little overhead.
The command bytes and control bytes are also acknowledged by the addressed RW1033s connected to the bus.
The display bytes are stored in the display RAM at the address specified by the data pointer ; see Section 7.11.
After the last (display) byte, the I2C-bus master issues a STOP condition (P).
Alternatively a START may be asserted to RESTART an I2C-bus access.

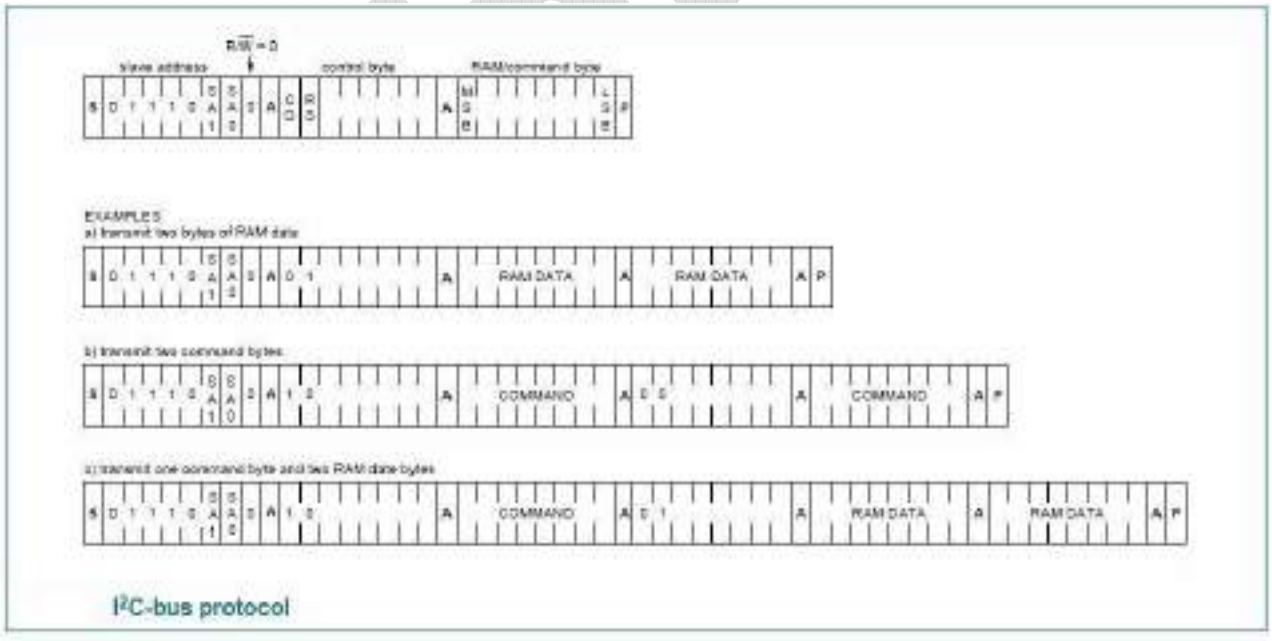


Fig. 14

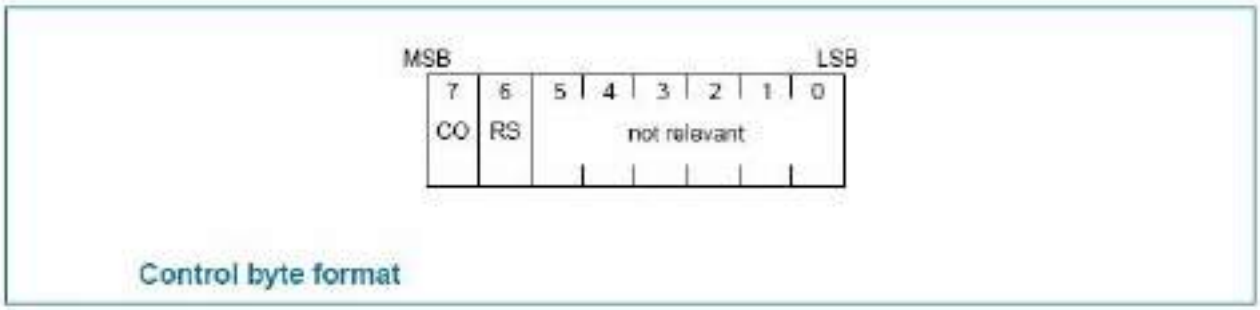


Fig. 15

Table 8. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		register selection
		0	command register
		1	data register
5 to 0	-		not relevant

7.17 characteristics of 4-SPI

When the 4-SPI serial interface has been selected then when the chip is in active state (CSB = “L”) the serial data input SDA and the serial clock input SCLK can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing. The RS input is used to determine whether or the serial data input is display data or command data; when RS = “H”, the data is display data, and when RS = “L” then the data is command data. The RS input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 16 is a serial interface signal chart.

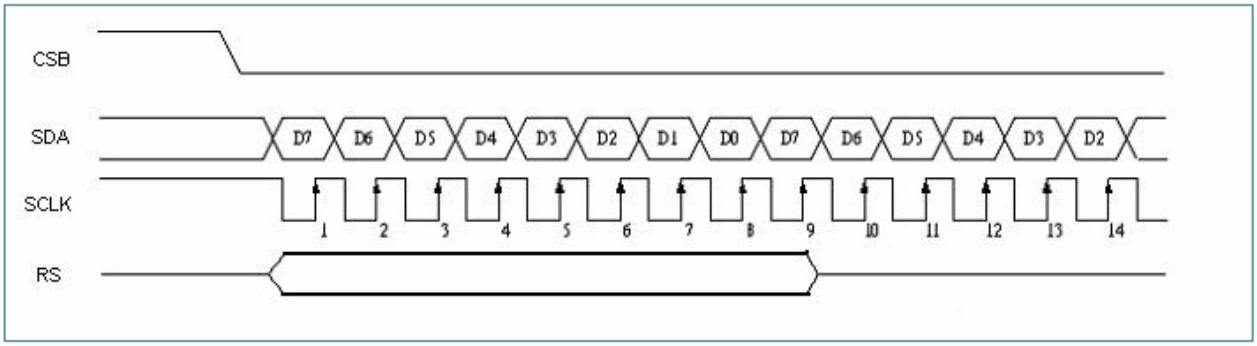


Fig 16

7.18 characteristics of 3-SPI

If 3-Pin SPI mode is selected then when the chip is in active state (CSB = “L”) , SDA, and SCLK are used. they are serial input data, and serial clock input, relatively. 3-Pin SPI mode does not use RS for data/instruction selection. Data length instruction should be used to realize data/instruction and data length instruction also indicates length of data. The example of timing sequence is shown in Fig.17, data length instruction is followed by data set.

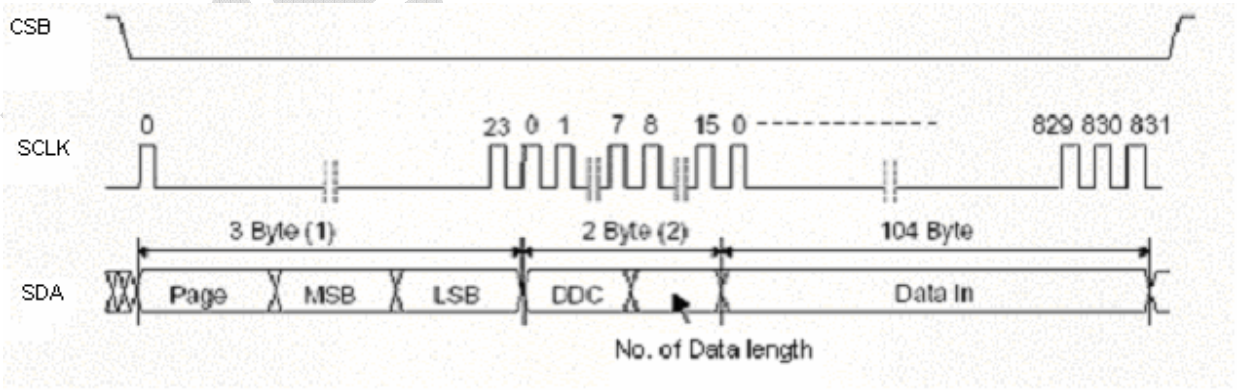


Fig 17

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCLK signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

7.19 Command decoder

The commands available to the RW1033 are defined in Table 9.1 and Table9.2.

Table 9.1 Definition of commands (ext=0)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0											
Set column (segment)address	0	0	0	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Set Display RAM column address in column address register
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
Mode Select command	0	0	1	1	0	0	E	B	M1	M0	E: display on/off, 1:on 0:off B: LCD bias set, 1: 1/2, 0:1/3 M1,M0: Set LCD Duty & Bias M1 M0 0 0 : 1/4 0 1 : Static 1 0 : 1/2 1 1 : 1/3 LP=1: power save mode LP=0: normal mode
bank select	0	0	1	1	1	1	1	0	I	O	I: Input Bank Selection Static 1/2 Duty I=0: RAM bit 0 RAM bits 0 and 1 I=1: RAM bit 2 RAM bits 2 and 3 O: Output Bank Selection Static 1/2 Duty O=0: RAM bit 0 RAM bits 0 and 1 O=1: RAM bit 2 RAM bits 2 and 3
Blink Select	0	0	1	1	1	1	0	A	BF1	BF0	A: Blink Mode select A=0: normal blinking A=1: blinking by alternating display RAM banks BF1,BF0: blink mode selection BF1 BF0 0 0 : off 0 1 : 1 1 0 : 2 1 1 : 3

Table 9.2 Definition of commands (ext=1)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1											
Mode Set	0	0	1	0	0	0	1	1	0	EXT	set EXT mode
Display COMMAND	0	0	1	1	1	1	0	1	0	1	display control command ADC: SEG output corespondence REV: reverse display ALLON: all point on display
	0	0	-	-	-	-	-	ADC	REV	ALLON	
SPI3 DATA Length	0	0	1	1	1	1	0	0	0	0	SPI3 DATA Length Set
			-	SPI6	SPI5	SPI4	SPI3	SPI2	SPI1	SPI0	

7.20 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and co-ordinates their effects. The display controller is also responsible for loading display data into the display RAM as required by the filling order.

8. Internal circuitry

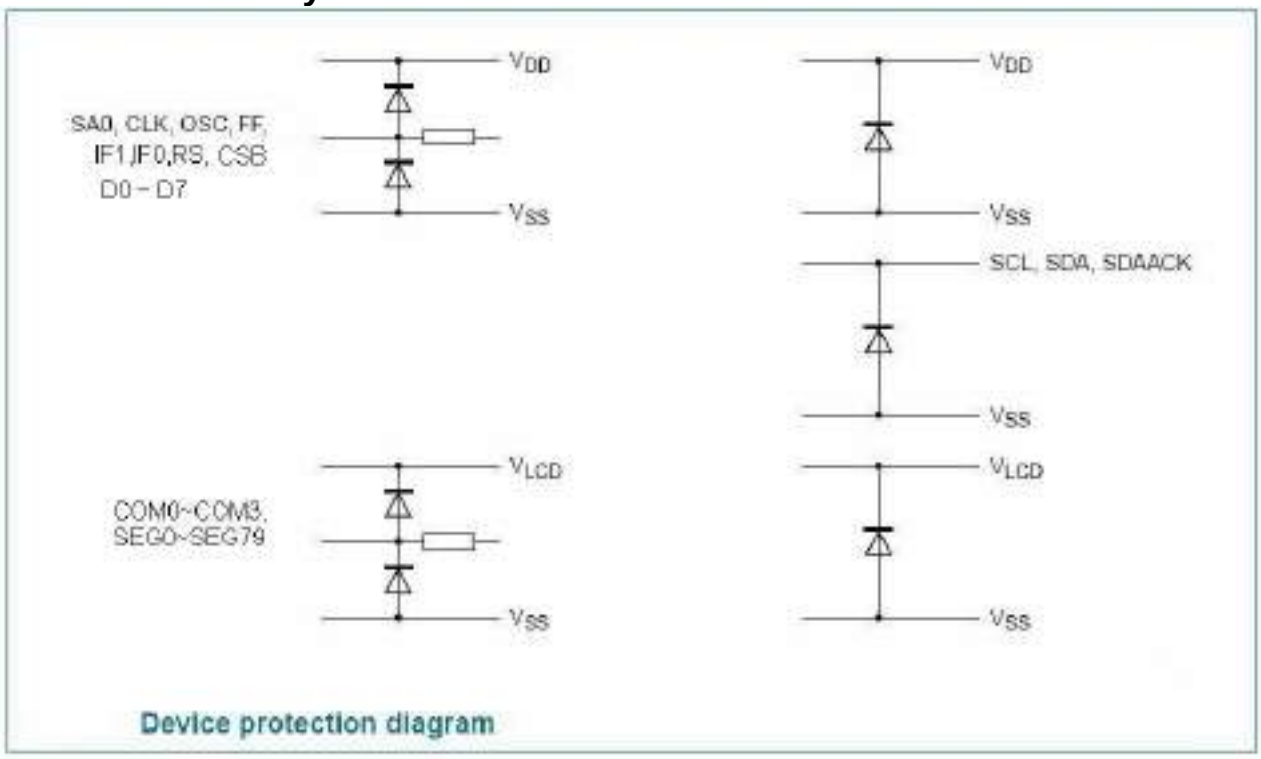


Fig. 18

9. Limiting values

CAUTION
Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 10. Limiting Value

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6.5	V
V_{LCD}	LCD supply voltage		−0.5	+6.5	V
$V_{I(n)}$	voltage on any input	V_{DD} related inputs	−0.5	+6.5	V
$V_{o(n)}$	voltage on any output	V_{LCD} related outputs	−0.5	+6.5	V
I_I	input current		−10	+10	mA
I_O	output current		−10	+10	mA
I_{DD}	supply current		−50	+50	mA
I_{SS}	ground supply current		−50	+50	mA
$I_{DD(LCD)}$	LCD supply current		−50	+50	mA
T_{stg}	storage temperature		-55	125	°C

10. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.4	-	5.5	V
V_{LCD}	LCD supply voltage			2.4	-	5.5	V
V_{POR}	power-on reset voltage						V
$I_{DD(LCD)}$	LCD supply current	f_{clk} = 1536 Hz	[1]	-	TBD		µA
I_{DD}	supply current	f_{clk} = 1536 Hz	[1]	-	TBD		µA
Logic							
V_I	input voltage			V_{SS} − 0.5	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	on pins CLK , OSC, SA1,SA0,IF1,IF0,RS , FF		0.7V_{DD}	-	V_{DD}	V
V_{IL}	LOW-level input voltage	on pins CLK, OSC, SA1,SA0,IF1,IF0,RS , FF		V_{SS}	-	0.3V_{DD}	V
V_{OH}	HIGH-level output voltage			0.8V_{DD}	-	-	V
V_{OL}	LOW-level output voltage			-	-	0.2V_{DD}	V
I_{OH}	HIGH-level output current	at pin CLK; V_{OH} = 4.6 V; V_{DD} = 5 V		1	-	-	mA
I_{OL}	LOW-level output current	at pins CLK, , V_{OL} = 0.4 V; V_{DD} = 5 V		-	-	−1	mA
I_L	leakage current	at pins OSC, CLK, SCL, SDA, FF; V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_I	input capacitance		[2]	-	-	7	pF
I²C-bus							
Input on pins SDA and SCL							
V_I	input voltage			V_{SS} − 0.5	-	5.5	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
V_{IL}	LOW-level input voltage			V_{SS}	-	0.3V_{DD}	V
C_I	input capacitance		[2]	-	-	7	pF
$I_{OL(SDA)}$	LOW-level output current on pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V		-	-	−3	mA
LCD outputs							
ΔV_O	output voltage variation	on pins C0 to C3 ; C_{bpl} = 35 nF		−100	-	+100	mV
		on pins S0 to S79; C_{sgm} = 5 nF		−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V					
		on pins C0 to C3	[3]	-	TBD		kΩ
		on pins S0 to S79	[3]	-	TBD		kΩ

[1] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; bus inactive.
[2] Not tested, design specification only.
[3] Outputs measured individually and sequentially.

11. Dynamic characteristics

Table 12. Dynamic characteristics

V_{DD} = 2.4 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
Internal: output pin CLK							
f_{clk}	clock frequency	FF = V_{DD}	[1][2]		TBD		Hz
		FF = V_{SS}	[1][2]		TBD		Hz
f_{fr}	frame frequency	FF = V_{DD}		60	82	110	Hz
		FF = V_{SS}		80	110	150	Hz
External: input pin CLK							
$f_{clk(ext)}$	external clock frequency		[2]		TBD		Hz
$t_{clk(H)}$	HIGH-level clock time				TBD		µs
$t_{clk(L)}$	LOW-level clock time				TBD		µs
Outputs: pins BP0 to BP3 and S0 to S79							
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V		-	-	30	µs
I²C-bus: timing[3][4]							
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width	on bus		-	-	50	ns

[1] Typical output duty cycle of 50 %.
[2] The corresponding frame frequency is $f_{fr} = f_{clk} / 24$
[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
[4] For I²C-bus timings see Figure 19.

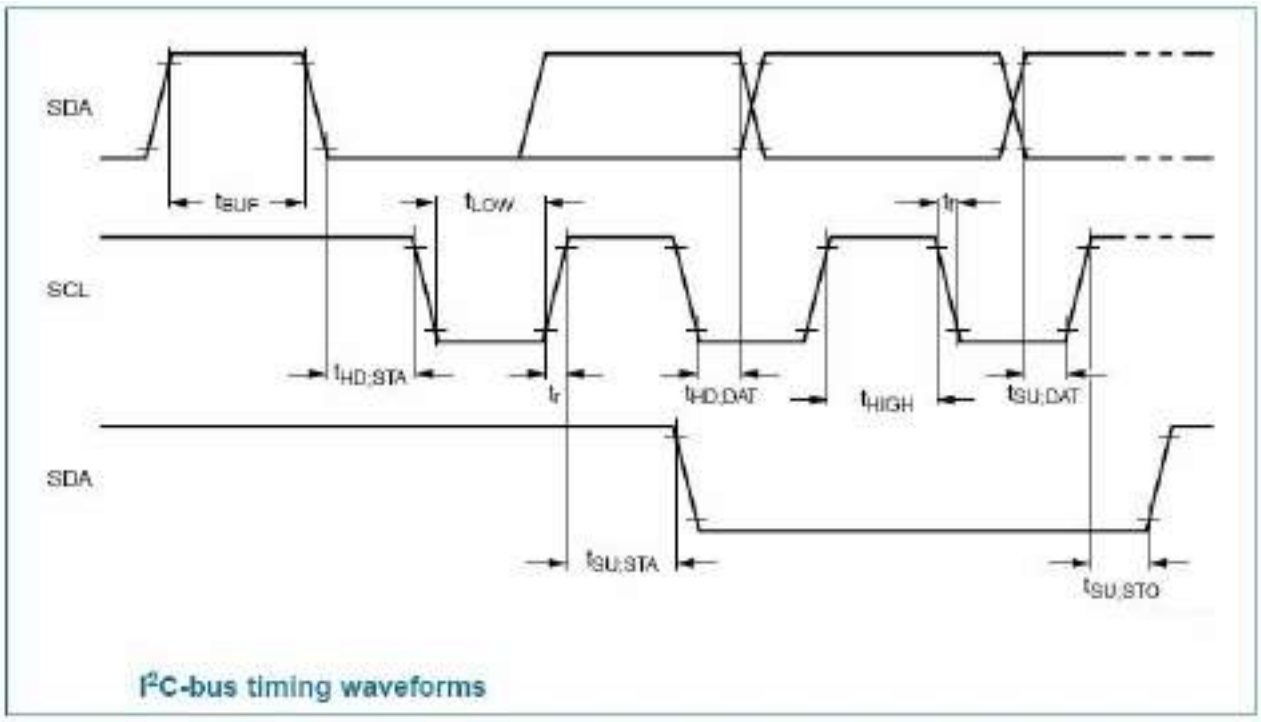


Fig. 19