Dot Matrix 48x4 LCD Controller / Driver

■ Features

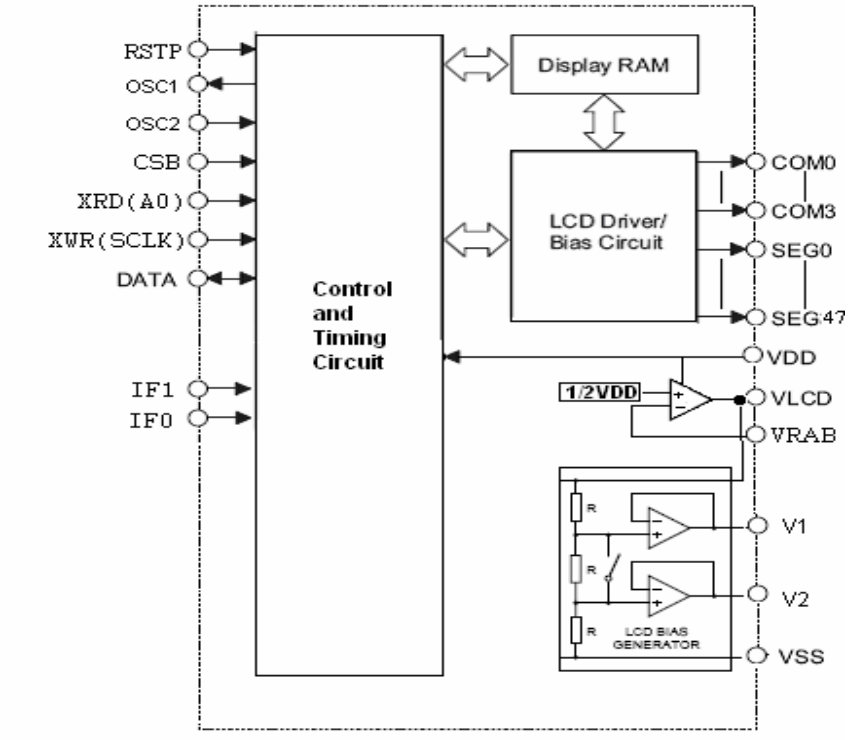
- Operating voltage: 2.4V~5.5V
- Internal LCD Bias generation with voltage-follower buffer
- External resistor CR oscillator
- External 256k Hz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2or 1/3 or 1/4 duty LCD applications
- Power down command reduces power consumption
- 48 x 4 LCD driver
- Built-in 48 x 4 bit display RAM
- IIC serial interface
- 3-line/4-line (type A & type B) serial interface (SPI)
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- VRAB pin for adjusting VLCD operating voltage

■ General Description

The RW1026 is a 192 patterns (48x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the RW1026 makes it suitable for multiple LCD applications including LCD modules and display subsystems.

Only two or three or four lines are required for the serial interface between the host controller and the RW1026. The RW1026 contains a power down command to reduce power consumption.

■ Block Diagram



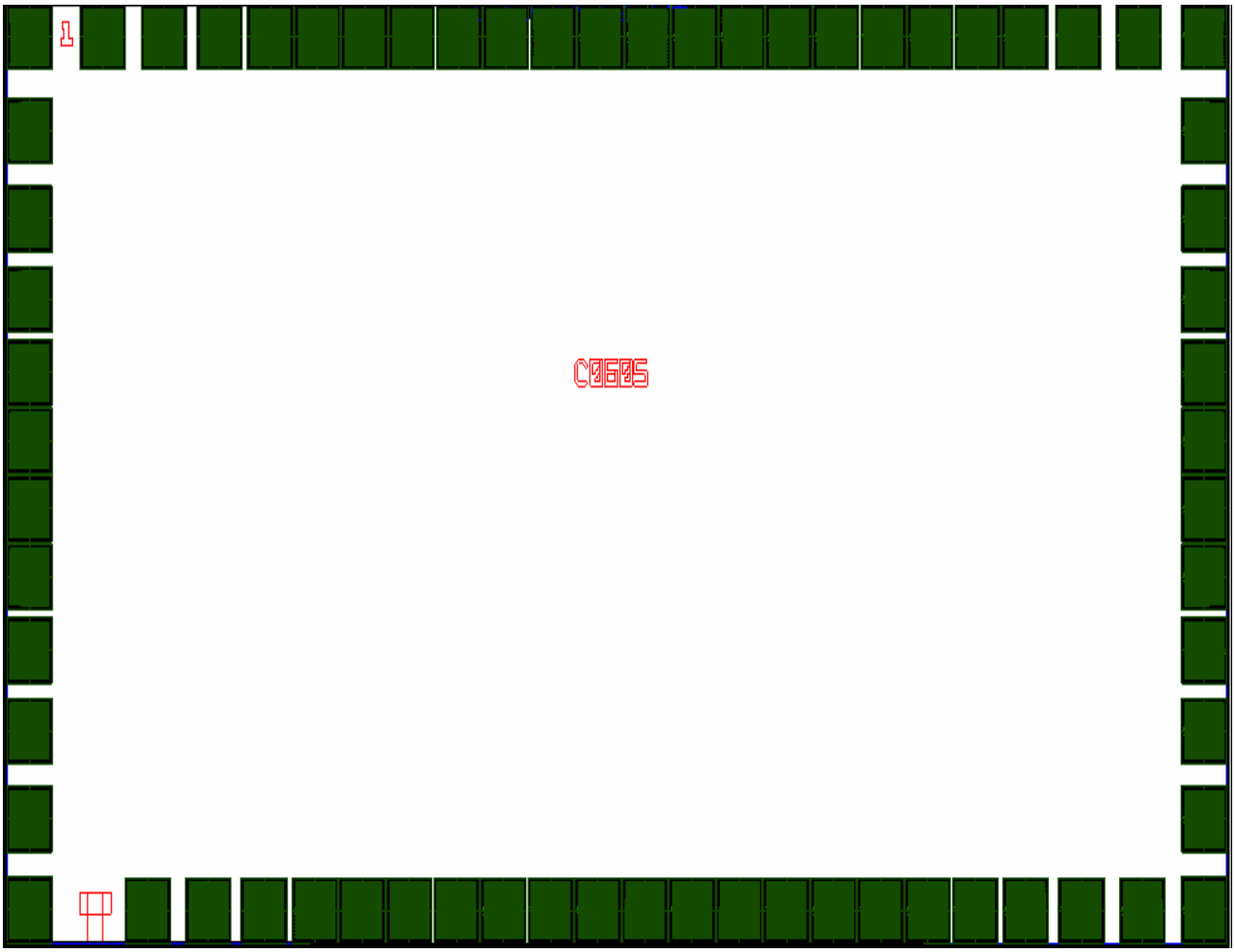
Note : CSB: Chip selection
XWR,XRD,DATA: Serial Interface
COM0~COM3, SEG0~SEG47: LCD outputs
IF1 ,IF0 : interface select pin

RW1026 Specification Revision History		
Version	**Date**	**Description**
1.0	2007/2/12	Add chip layout and pad location
1.1	2007/8/21	Remove Power save and Set initial display function
1.2	2008/09/18	Add application circuit for different interface Add voltage follower in block diagram Add RC oscillation external resistor Rext value

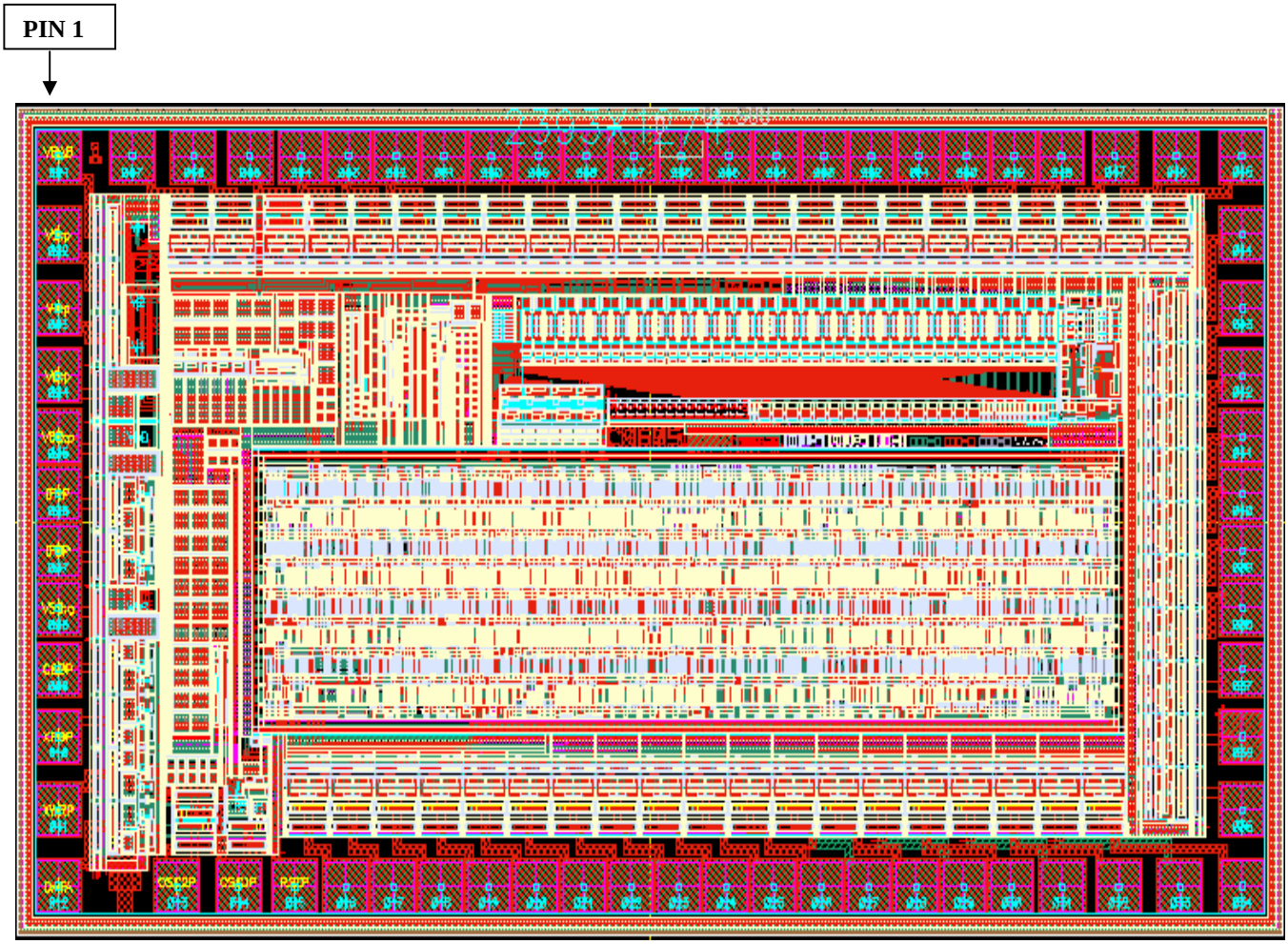
■ Pad Assignment

Chip size: 2463 x 1344 um
Pad Size: 89.5 x 88.5 um
Pad Pitch: 92.5~231.4 um
Chip thickness: 482.6 um

- **The IC substrate should be connected to VSS in the PCB layout artwork.**



■ CHIP LAYOUT



■ PAD LOCATION

Unit: um

PAD Number	PAD NAME	COORDINATE		PAD Number	PAD NAME	COORDINATE	
		X	Y			X	Y
1	VRAB	-1151.75	592.75	35	SEG32	1152.25	-468.75
2	V2	-1152.25	465.75	36	SEG31	1152.25	-349.25
3	V1	-1152.25	346.25	37	SEG30	1152.25	-239.75
4	VLCD	-1152.25	236.75	38	SEG29	1152.25	-140.25
5	VDD	-1152.25	137.25	39	SEG28	1152.25	-47.75
6	IF1	-1152.25	44.75	40	SEG27	1152.25	44.75
7	IF0	-1152.25	-47.75	41	SEG26	1152.25	137.25
8	VSS	-1152.25	-140.25	42	SEG25	1152.25	236.75
9	CSB	-1152.25	-239.75	43	SEG24	1152.25	346.25
10	XRD(A0)	-1152.25	-349.25	44	SEG23	1152.25	465.75
11	XWR(SCLK)	-1152.25	-468.75	45	SEG22	1151.75	592.75
12	DATA	-1152.25	-592.25	46	SEG21	1024.25	592.75
13	OSC2	-920.85	-592.75	47	SEG20	904.75	592.75
14	OSC1	-801.35	-592.75	48	SEG19	800.25	592.75
15	RSTP	-691.85	-592.75	49	SEG18	707.75	592.75
16	COM0	-592.35	-592.75	50	SEG17	615.25	592.75
17	COM1	-499.85	-592.75	51	SEG16	522.75	592.75
18	COM2	-407.35	-592.75	52	SEG15	430.25	592.75
19	COM3	-314.85	-592.75	53	SEG14	337.75	592.75
20	SEG47	-222.35	-592.75	54	SEG13	245.25	592.75
21	SEG46	-129.85	-592.75	55	SEG12	152.75	592.75
22	SEG45	-37.35	-592.75	56	SEG11	60.25	592.75
23	SEG44	55.15	-592.75	57	SEG10	-32.25	592.75
24	SEG43	147.65	-592.75	58	SEG9	-124.75	592.75
25	SEG42	240.15	-592.75	59	SEG8	-217.25	592.75
26	SEG41	332.65	-592.75	60	SEG7	-309.75	592.75
27	SEG40	425.15	-592.75	61	SEG6	-402.25	592.75
28	SEG39	517.65	-592.75	62	SEG5	-494.75	592.75
29	SEG38	610.15	-592.75	63	SEG4	-587.25	592.75
30	SEG37	702.65	-592.75	64	SEG3	-679.75	592.75
31	SEG36	802.15	-592.75	65	SEG2	-779.25	592.75
32	SEG35	911.65	-592.75	66	SEG1	-888.75	592.75
33	SEG34	1031.15	-592.75	67	SEG0	-1008.25	592.75
34	SEG33	1152.25	-592.25				

■ Pad Description

Pad	I/O	Function
CSB	I	Chip selection input for 3-SPI, 4-SPIwith pull-high resistor. When CSB is login high, the data and command read from or written to the RW1026 are disabled. The serial interface circuit is also reset. But if CSB is at logic low level and is input to the CSB pad, the data and command transmission between the host controller and the RW1026 are all enabled.
XRD(A0)	I	READ clock input for 4-SPI (type B) with pull-high resistor. Data in the RAM of RW1026 are clocked out on the falling edge of the XRD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data. A0 pin for 4-line(type A)serial interface. A0=1: DATA A0=0: Command
XWR(SCLK)	I	WRITE clock input for 4-SPI (type B) with pull-high resistor. Data on the DATA line are latched into the RW1026 on the rising edge of the XWR signal. Serial clock input (SCLK) pin for 3-line, 4-line (type A), and IIC interface.
DATA	I/O	Serial data input/output with pull-high resistor.
VSS	-	Negative power supply. Ground
OSC1	I	The OSC1 and OSC2 pads are connected to a external resistor if an RC oscillator is selected. If the system clock comes from an external clock source, the external clock source should be connected to the OSC1 pad.
OSC2	O	
VLCD	I	LCD power input.
VDD	-	Positive power supply.
V1,V2	-	Bias voltage level for LCD driving. These voltages must satisfy the following: **VDD ≥ VLCD ≥ V1 ≥ V2 ≥ VSS**
COM0-COM3	O	LCD common output.
SEG0-SEG47	O	LCD segment output.
RSTP	I	Reset pin with pull-up resistor, Initialized by setting RSTP to "L". Reset operation is performing at RSTP signal level.
VRAB	I	LCD voltage adjusting pin. Applies voltage between V0 and VSS using a split resistor.
IF1,IF0	I	Interface selection pins with pull-up resistor IF1,IF0 (0 , 0) : IIC Interface (0 , 1) : 3-line Interface (1 , 0) : 4-line Interface (Type A) (1 , 1) : 4-line Interface (Type B)

■ Absolute Maximum Ratings

Supply Voltage .....VSS-0.3V toVSS+5.5V
Storage Temperature.....-40°C to 80°C
Input Voltage.....VSS-0.3V toVDD+0.3V
Operating Temperature.....-25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under _Absolute Maximum Ratings_ may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

➢ **D.C. Characteristics** Ta=25°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	-	-	2.4	-	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillation	-	150	200	μA
		5V		-	300	600	μA
I_{DD3}	Operating Current	3V	No load/LCD ON external clock source	-	100	200	μA
		5V		-	200	400	μA
I_{STB}	Standby Current	3V	No load, Power down mode	-	0.1	5	μA
		5V		-	0.3	10	μA
V_{IL}	Input Low Voltage	3V	DATA, XWR,CSB,XRD	0	-	0.6	V
		5V		0	-	1.0	V
V_{IH}	Input High Voltage	3V	DATA, XWR,CSB,XRD	2.4	-	3.0	V
		5V		4	-	5.0	V
I_{OL1}	DATA	3V	V_{OL}=0.3V	0.5	1.2	-	mA
		5V	V_{OL}=0.5V	1.3	2.6	-	mA
I_{OH1}	DATA	3V	V_{OH}=2.7V	-0.4	-0.8	-	mA
		5V	V_{OH}=4.5V	-0.9	-1.8	-	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	-	μA
		5V	V_{OL}=0.5V	150	250	-	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-80	-120	-	μA
		5V	V_{OH}=4.5V	-120	-200	-	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	-	μA
		5V	V_{OL}=0.5V	120	200	-	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-40	-70	-	μA
		5V	V_{OH}=4.5V	-70	-100	-	μA
R_{PH}	Pull-high Resistor	3V	DATA, XWR,CSB,XRD	60	120	200	kΩ
		5V		30	60	100	kΩ

➢ **A.C. Characteristics** Ta=25 °C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	-	On-chip RC Oscillation **R_{FOSC}=51KΩ**	-	310	-	kHz
f_{SYS2}	System Clock	-	External clock source	-	310	-	kHz
f_{LCD}	LCD Clock	-	On-chip RC Oscillation	-	$f_{SYS1/1024}$	-	Hz
		-	External clock source	-	$f_{SYS2/1024}$	-	Hz
t_{COM}	LCD Common Period	-	n: Number of COM	-	n/f_{LCD}	-	s
f_{CLK1}	Serial Data Clock(XWR pin)	3V	Duty cycle 50%	4	-	150	kHz
		5V		4	-	300	kHz
f_{CLK2}	Serial Data Clock(XRD pin)	3V	Duty cycle 50%	-	-	75	kHz
		5V		-	-	150	kHz
t_{CS}	Serial Interface Reset Pulse Width(Figure 3)	-	CSB	-	250	-	ns
t_{CLK}	XWR,XRD Input Pulse Width (Figure 1)	3V	Write mode	3.34	-	125	μs
			Read mode	6.67	-	-	
		5V	Write mode	1.67	-	125	μs
			Read mode	3.34	-	-	
tr,tf	Rise/Fall Time Serial Data Clock Width (Figure 1)	-	-	-	120	-	ns
t_{SU}	Setup Time for DATA to XWR,XRD Clock Width (Figure 2)	-	-	-	120	-	ns
th	Hold Time for DATA to XWR,XRD Clock Width (Figure 2)	-	-	-	120	-	ns
t_{SU1}	Setup Time for CSB to XWR,XRD Clock Width (Figure 3)	-	-	-	100	-	ns
t_{h1}	Hold Time for CSB to XWR,XRD Clock Width (Figure 3)	-	-	-	100	-	ns

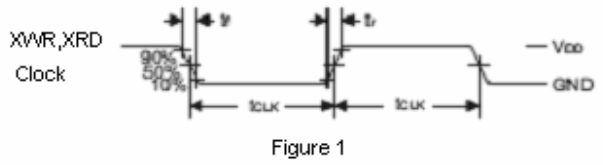


Figure 1

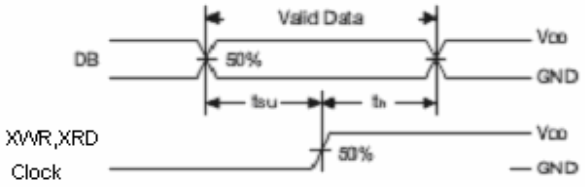


Figure 2

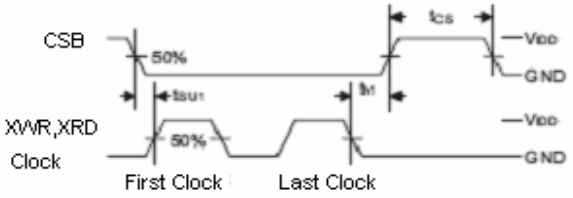
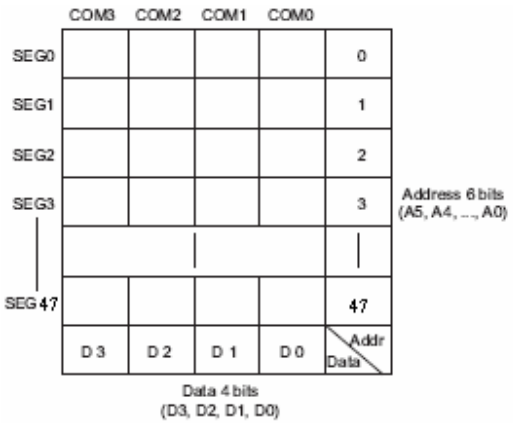


Figure 3

■ Functional Description

➢ Display Memory _ RAM

The static display memory (RAM) is organized into 48x4 bits and stores the displayed data. The contents of the RAM data is directly mapped to the contents of the LCD driver. The following is a mapping from the RAM to the LCD pattern:



RAM Mapping

➢ System Oscillator

The RW1026 system clock is used to generate the LCD driving clock. The source of the clock may be from an external-resistor RC oscillator (256 kHz), or an external 256 kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the external-resistor RC oscillator. Once the system clock stops, the LCD display will become blank.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The external clock source can be applied to connect of 256 kHz to the OSC1 pin. In this case, the system fails to enter the power down mode. At the initial system power on, the RW1026 is at the SYS DIS state.

➢ LCD Driver

The RW1026 is a 192 (48x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the RW1026 suitable for various LCD applications.

The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at an external-resistor RC oscillator frequency, or an external frequency.

The LCD corresponding commands are summarized in the following tables.

The LCD OFF command turns the LCD display off by disabling the LCD bias generator.

The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator.

The BIAS and COM are the LCD panel related commands. Using the LCD related commands; the RW1026 can be compatible with most types of LCD panels.

■ Command Summary for 4-line (type A), 3-line, and IIC interface

Instruction of RW1026	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1										
Mode Set	0	1	1	1	1	1	1	0	EXT	set EXT mode

Instruction	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0										
Set column (segment)address	0	0	1	Y5	Y4	Y3	Y2	Y1	Y0	Set Display RAM column address in column address register *valid for SIF3,SIF4,IIC only
Write display data	1	Write data								Write data into DDRAM
Select DUTY & Bias	0	0	0	1	0	DU1	DU0	0	Bias	Set LCD Duty & Bias DU1,DU0 0 0 : 1/2 0 1 : 1/3 1 0 : 1/4 Bias=1 : 1/3 bias Bias=0 : 1/2 bias
RC 256K	0	0	0	0	1	0	1	X	X	System clock source, on-chip RC oscillator
RC 256K	0	0	0	0	1	1	0	X	X	System clock source, on-chip RC oscillator
EXT 256K	0	0	0	0	1	1	1	0	0	System clock source, external clock source
SYS DIS	0	0	0	0	0	0	0	0	0	Turn off both oscillator and LCD bias
SYS EN	0	0	0	0	0	0	0	0	1	Turn on system oscillator
LCDOFF	0	0	0	0	0	0	0	1	0	Turn off LCD bias
LCDON	0	0	0	0	0	0	0	1	1	Turn on LCD bias

Instruction	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=1										
Display COMMAND (Double Command)	0	1	1	1	1	0	1	0	1	display control command SHL: Com output scan direction ADC: SEG output correspondence REV: reverse display ALLON: all point on display
	0	-	-	-	-	SHL	ADC	REV	ALLON	
Set Static display	0	1	1	1	1	0	0	1	STA	STA=1 :static display on
Reset	0	1	1	1	1	0	0	0	0	Software Reset
ANALOG COMMAND (Double Command)	0	1	1	1	1	0	1	0	0	Analog control command Foloff =1 , follower off Regoff = 1 , regulator off
	0	-	-	REGOFF	FOLOFF	1	0	1	1	

■ Command Summary for 4-line serial interface (type B)

EXT=1

Name	ID	Command Code	D/C	Function	Def.
Write display data	**110**	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
Read display data	**101**	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
READ-MODIFY-WRITE	**101**	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	**100**	0000-0000-X	C	Turn off both oscillator and LCD bias	yes
SYS EN	**100**	0000-0001-X	C	Turn on system oscillator	
LCDOFF	**100**	0000-0010-X	C	Turn off LCD bias	yes
LCDON	**100**	0000-0011-X	C	Turn on LCD bias	
RC 256K	**100**	0001-01XX-X	C	System clock source, on-chip RC oscillator	
RC 256K	**100**	0001-10XX-X	C	System clock source, on-chip RC oscillator	yes
EXT 256K	**100**	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	**100**	0010-abX0-X	C	LCD 1/2 bias option ab = 00 : 2 commons option ab = 01 : 3 common option ab = 10 : 4 common option	
BIAS 1/3	**100**	0010-abX1-X	C	LCD 1/3 bias option ab = 00 : 2 commons option ab = 01 : 3 common option ab = 10 : 4 common option	

EXT=1 or 0

Name	ID	Command Code	D/C	Function	Def.
Mode Select	**100**	1111-110a-X	C	a=0 : EXT=0 a=1 : EXT=1	0

EXT=1

Name	ID	Command Code	D/C	Function	Def.
Analog off	**100**	1111-0100-X XXab-1011-X	C	a=1, regulator off b=1, follower off	00
Display COMMAND	**100**	1111-0101-X	C	display control command a=SHL: Com output scan direction b=ADC: SEG output correspondence c=REV: reverse display d=ALLON: all point on display	0000
	100	XXXX-abcd	C		
Set Static display	**100**	1111-001a-X	C	a=1 :static display on	off
Reset	**100**	1111-0000-X	C	Software Reset	

Note: X: Don't care
A5~ A0: RAM addresses
D3~D0: RAM data
D/C: Data/command mode
Def.: power on initial value

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Of these, 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the RW1026 after system reset.

➢ **Command Format for 4-SPI (Type B)**

The RW1026 can be configured by the S/W setting. There are two mode commands for 4-line interface (Type B) to configure the RW1026 resources and to transfer the LCD display data. The configuration mode of the RW1026 is called command mode, and its command mode ID is 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CSB pin should be set to “1” and the previous operation mode will be reset also. Once the CSB pin returns to “0” a new operation mode ID should be issued first.

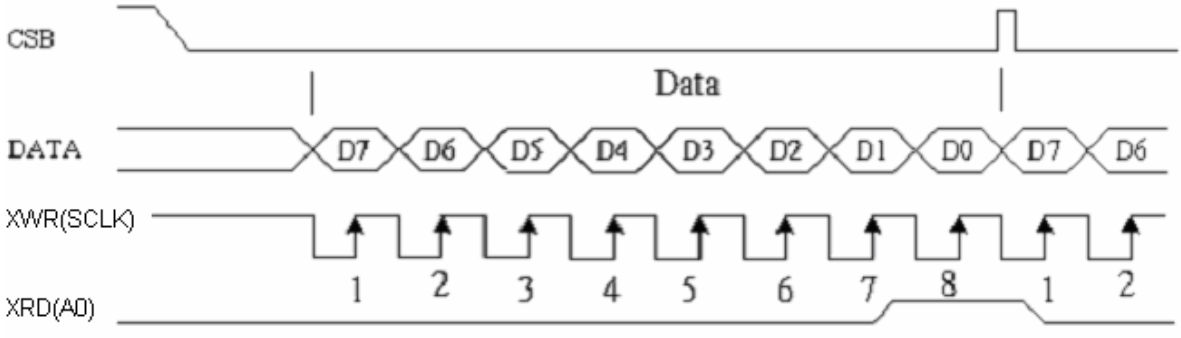
➢ **Interfacing**

Only 2/3/4 lines are required to interface with the RW1026. The CSB line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the RW1026. If the CSB pin is set to 1, the data and command issued between the host controller and the RW1026 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the
RW1026. The DATA line is the serial data input/output line.
Data to be read (Only available for Type B 4-line Interface) or written or commands to be written have to be passed through the DATA line. The RD line is the
READ (or A0) clock input. Data in the RAM are clocked out on the falling edge of the RD signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the XRD signal. The XWR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the RW1026 on the rising edge of the XWR signal.

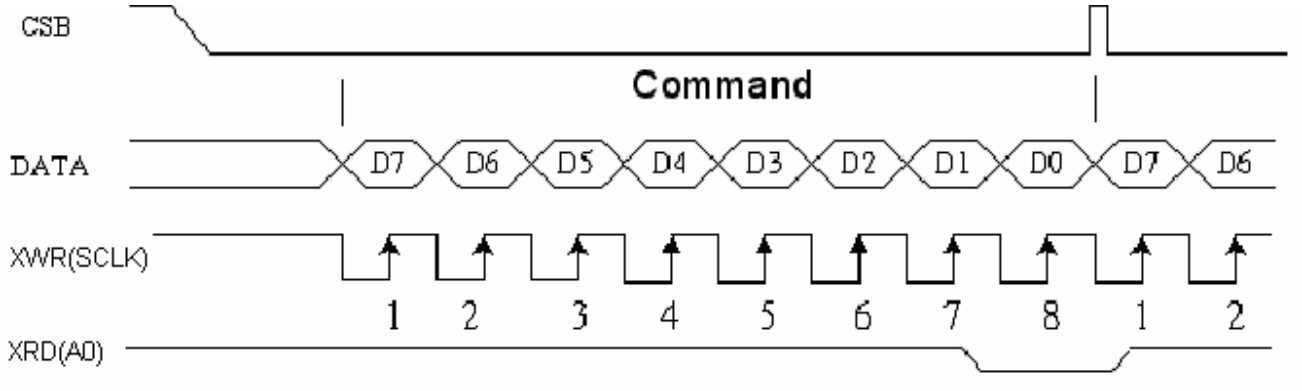
■ Interface Timing Diagrams

(1) 4-line Serial Interface (type A)

When entering data (parameters): **A0= HIGH** at the rising edge of the 8th SCLK

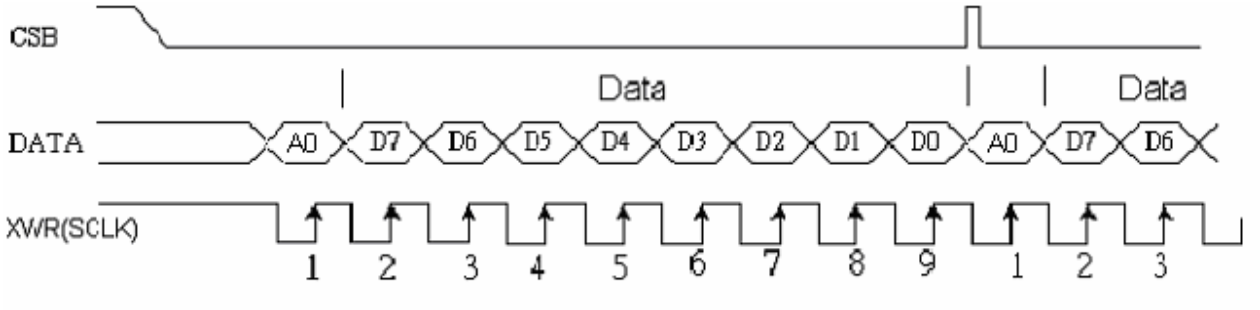


When entering command: **A0= LOW** at the rising edge of the 8th SCLK

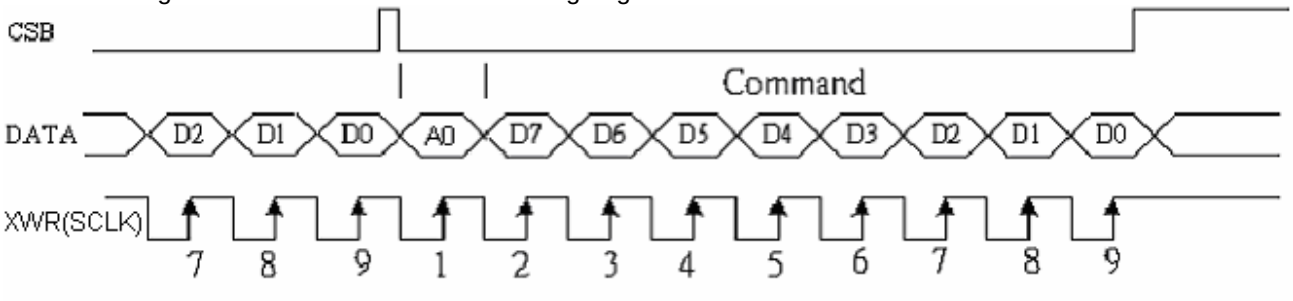


(2) 3-line Serial Interface

When entering **data** (parameters): **A0 = HIGH** at the rising edge of the 1st SCLK.



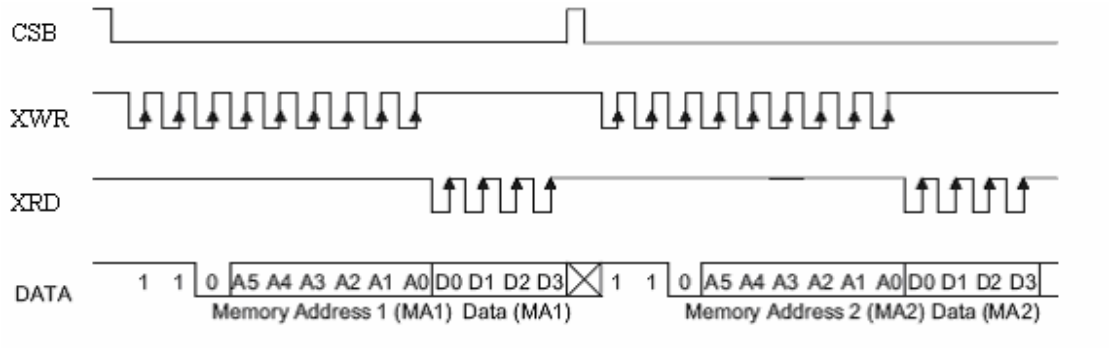
When entering **command**: **A0 = LOW** at the rising edge of the 1st SCLK



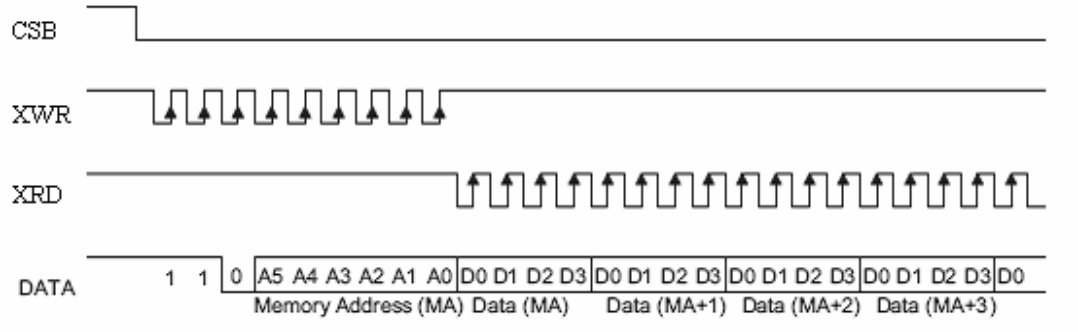
- If CSB is caused to HIGH before 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set CSB at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set CSB to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

(3) 4-line Serial Interface (type B)

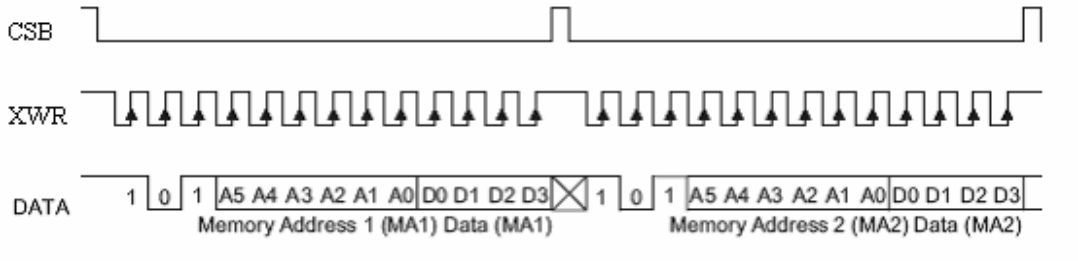
READ Mode (Command Code: 1 1 0)



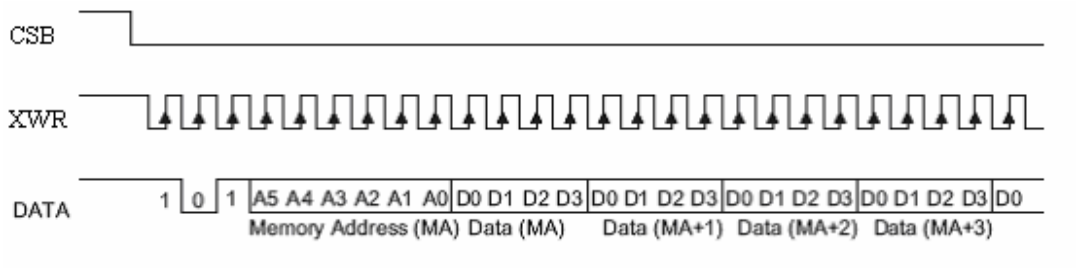
READ Mode (Successive Address Reading)



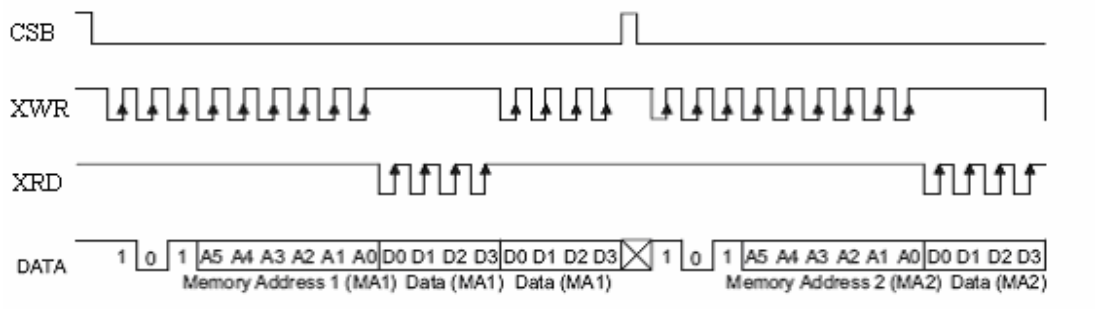
WRITE Mode (Command Code: 1 0 1)



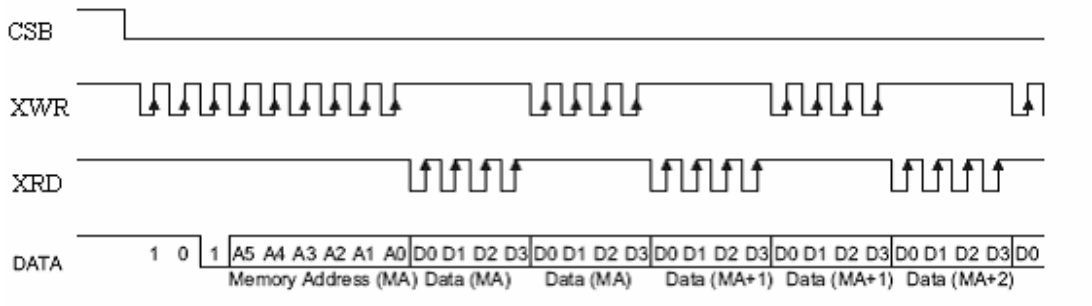
WRITE Mode (Successive Address Writing)



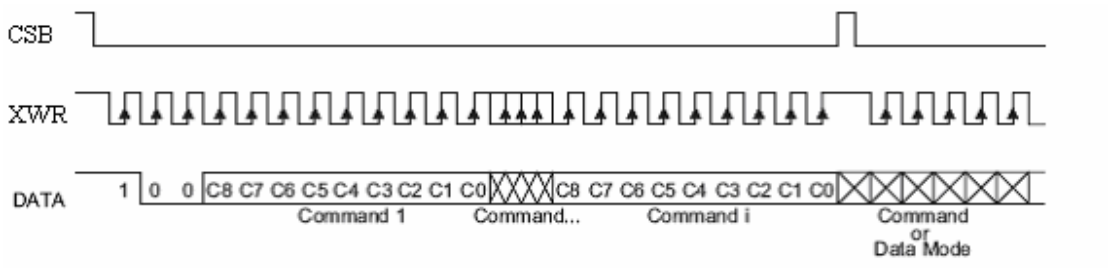
Read-Modify-Write Mode (Command Code: 1 0 1)



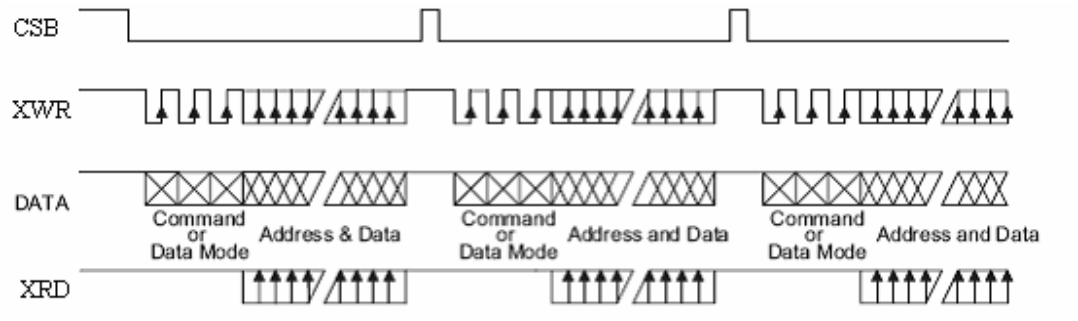
Read-Modify-Write Mode (Successive Address Accessing)



Command Mode (Command Mode: 1 0 0)



Mode (Data and Command Mode)



Note: It is recommended that controller should read in the data from the DATA line between the rising edge of XRD line and the falling edge of the next XRD line.

(4) IIC Interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (DATA) and a Serial Clock line XWR(SCLK). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

- **BIT TRANSFER**

One data bit is transferred during each clock pulse. The data on the DATA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig. 4

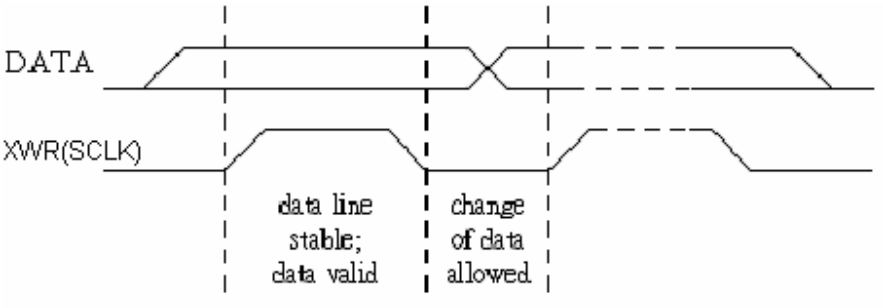


Fig. 4

➢ **START AND STOP CONDITIONS**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.5

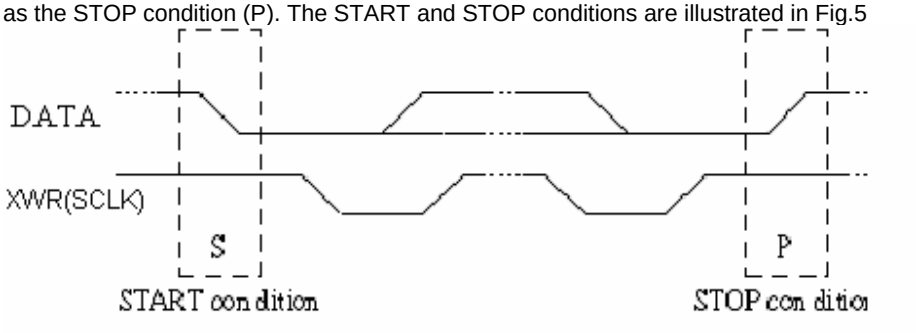


Fig 5. Definition of START and STOP conditions

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

➢ **ACKNOWLEDGE**

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the DATA line during the acknowledge clock pulse, so that the DATA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.6

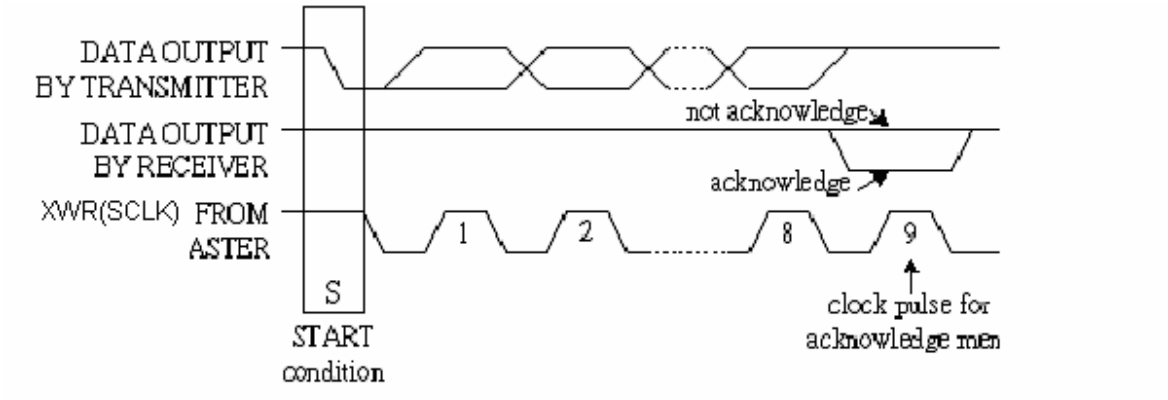


Fig 6. Acknowledgement on the 2-line Interface

➢ **IIC Interface protocol**

The RW1026 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111110) are reserved for the RW1026. The least two significant bit of the slave address is fixed at 10.
The IIC Interface protocol is illustrated in Fig.7.

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1026 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

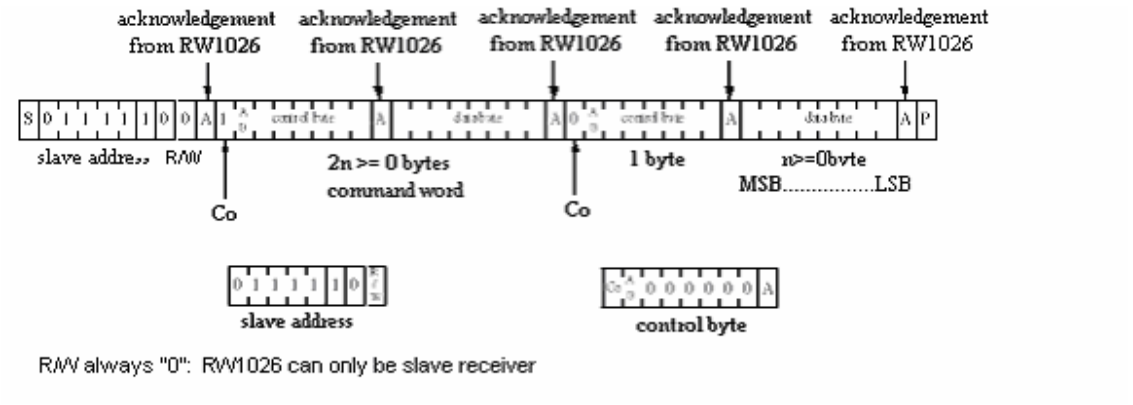
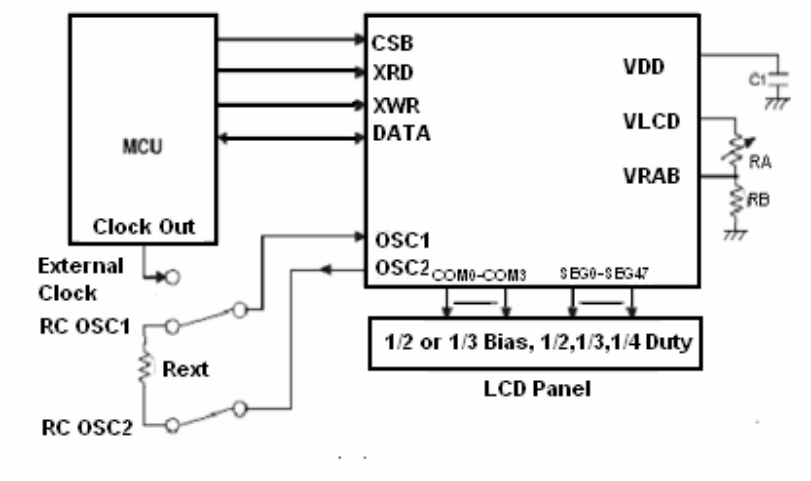


Fig 7. Acknowledgement on the 2-line Interface

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

■ Application Circuits

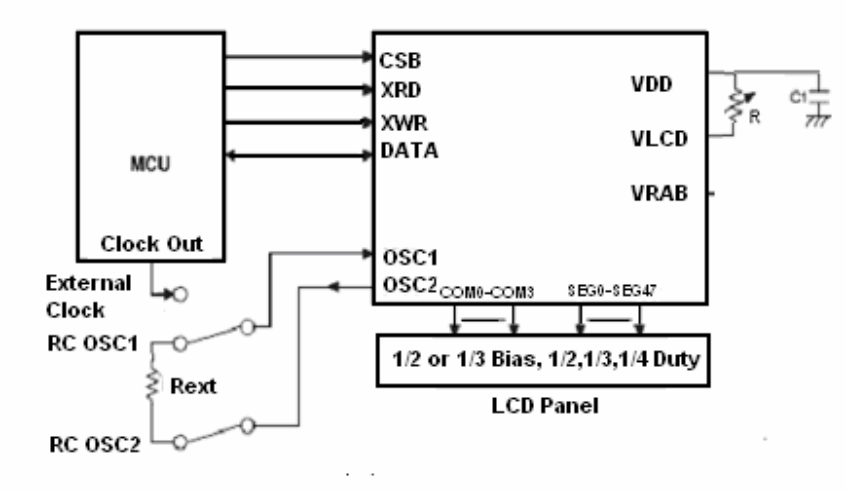
(1) Host Controller with an RW1026 Display System (using Internal VLCD Regulator) for 4-SPI



VLCD = (1 + Ra/Rb) * 0.5*VDD

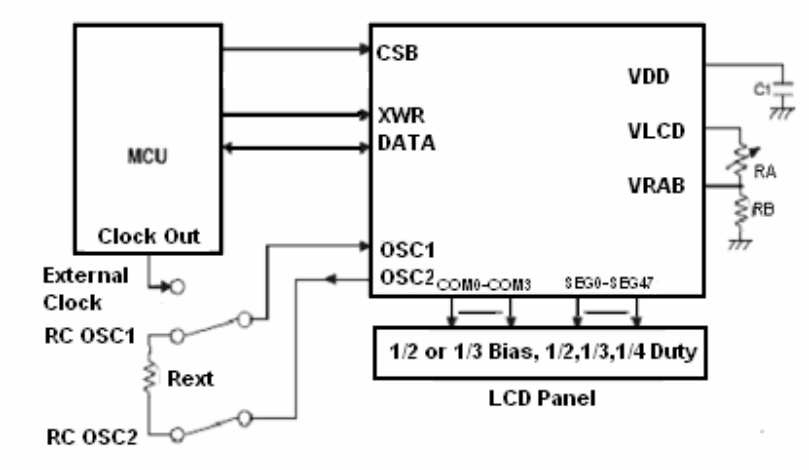
*** Note: Please keep VDD ≥ VLCD ≥ V1 ≥ V2 ≥VSS**

(2) Host Controller with an RW1026 Display System (using external VLCD power input) for 4-SPI



*** Note: Please keep VDD ≥ VLCD ≥ V1 ≥ V2 ≥VSS**

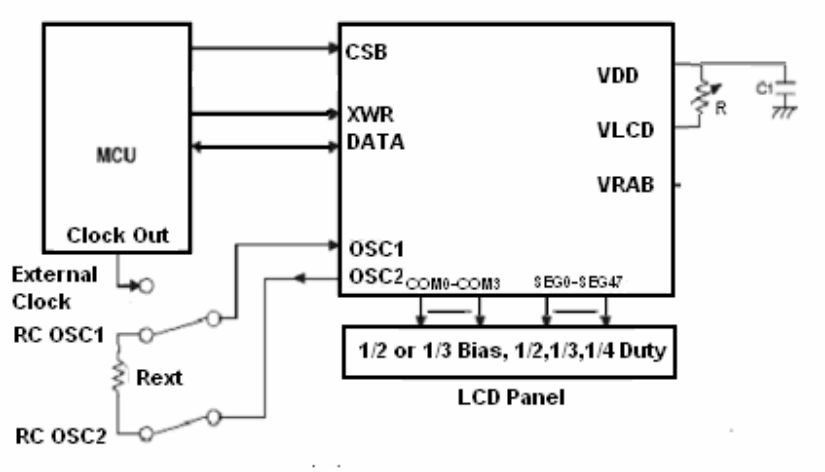
(3) Host Controller with an RW1026 Display System (using internal VLCD regulator) for 3-SPI



VLCD= (1 + Ra/Rb) * 0.5*VDD

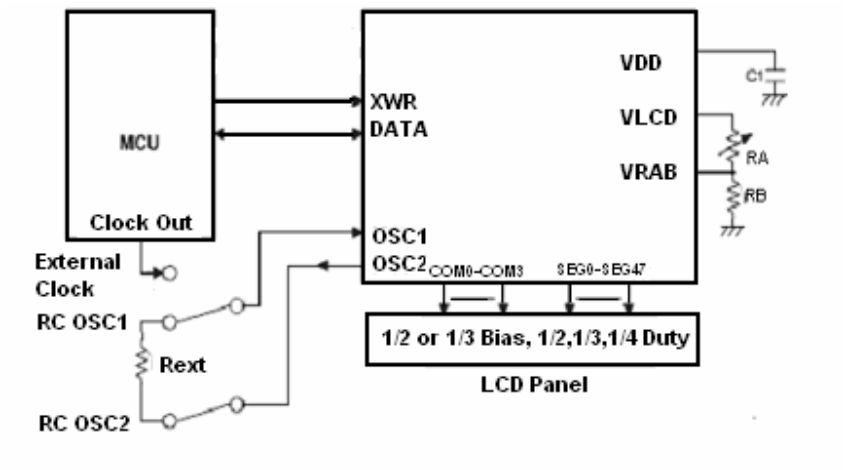
*** Note: Please keep VDD ≥ VLCD ≥ V1 ≥ V2 ≥VSS**

(4) Host Controller with an RW1026 Display System (use external VLCD power input) for 3-SPI



*** Note: Please keep VDD ≥ VLCD ≥ V1 ≥ V2 ≥VSS**

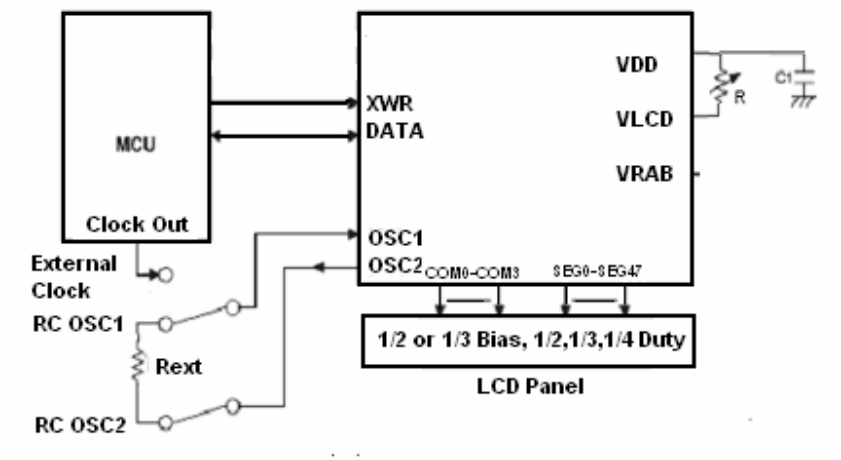
(5) Host Controller with an RW1026 Display System (using internal VLCD regulator) for IIC



VLCD= (1 + Ra/Rb) * 0.5*VDD

*** Note: Please keep VDD ≥ VLCD ≥ V1 ≥ V2 ≥VSS**

(6) Host Controller with an RW1026 Display System (use external VLCD power input) for IIC



*** Note: Please keep VDD ≥ VLCD ≥ V1 ≥ V2 ≥VSS**