

RAiO

RA8911

8-Bit Micro-Controller

Version 1.7

November 9, 2004

RAiO Technology Inc.

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Specification Revision History		
Version	Date	Description
0.9	2002/11/06	First Specification version
0.91	2002/11/22	<ol style="list-style-type: none"> 1. Modify Table 8-4 2. Modify Figure8-28 3. Modify Block Diagram(delete Pin of Vref) 4. Modify Flash Sector Erase content (Fill Data Description)
0.92	2002/12/05	Add Note to Page 90
1.0	2003/01/29	<ol style="list-style-type: none"> 1. Add PLL transfer time 2. Update REG [104Bh] 3. Modify Memory Organization 4. AIN1 with AIN2 change of X-Y coordinate 5. Modify REG[101Ah], REG[103Ah] and REG[103Bh]
1.1	2003/02/19	<ol style="list-style-type: none"> 1. Modify REG[103Eh] bit1(W-->W/R) 2. Modify REG[102Eh] 3. Add DAC and ADC loop control description
1.2	2003/4/16	<p>RA8911 made some adjustments according to the following items. The datasheet version 1.2 also made an update according to all the adjustments. In order to distinguish the previous version, it renames as "RA8911 Plus". The RA8911 Plus is, of course, compatible with all the previous versions for users convenience.</p> <ol style="list-style-type: none"> 1. Modify REG[1021h, 1025h and 1029h] 2. Add REG[102Dh] bit0~3, bit Interrupt function 3. Add REG[1032h] bit6, External Memory control pin share function 4. Add REG[1034h] bit7, Nibble or bit Interrupt function 5. Add REG[103Fh] External SRAM Bank function 6. Change REG[1022h, 1026h and 102Ah] register name 7. Modify Figure 8-7 (The secondary Flash CE# pin must be pulled high) 8. Modify X-Y Coordinate
1.3	2003/5/27	Test Pin Description
1.5	2003/10/28	Format Update
1.6	2004/1/6	Format Update
1.7	2004/11/9	Modify Operating Voltage.

Chapter	Table of Contents	Page
1.	General Description	5
2.	Feature	5
3.	Block Diagram	6
4.	Die Form	7
	4.1 PAD Diagram	7
	4.2 Pin Assignment(PQFP-100Pin).....	7
	4.3 PAD X/Y Coordinate.....	8
5.	Pin Description.....	10
6.	Memory Organization	14
7.	Registers Description	15
8.	Function Description	46
	8.1 System Clock	46
	8.2 CPU Operation Mode.....	47
	8.2.1 Reset & Idle & Sleep & Power Saving Mode.....	47
	8.2.2 Wakeup.....	50
	8.3 External Flash ROM.....	51
	8.3.1 Command Definitions	54
	8.3.2 Flash Sector Erase.....	55
	8.3.3 Flash Programming	57
	8.4 I/O Ports.....	61
	8.5 Timer	68
	8.6 Watch Dog	72
	8.7 Interrupt.....	74
	8.8 Universal Synchronous Asynchronous Receiver Transmitter (UART)	80
	8.9 IrDA Interface	82
	8.10 Digital-to-Analog Converter (D/A) Module	83
	8.11 LCD Interface	85
	8.12 PWM.....	88
	8.13 Low Voltage Detect (LVD).....	92
	8.14 External SRAM	93
	8.15 Analog-to-Digital Converter (ADC) Module.....	94
	8.15.1 ADC Touch Panel Loop Control.....	97
	8.15.2 ADC Touch Panel No Loop Control	98
	8.16 1Hz, 2Hz and 1/60Hz Interrupt/Wakeup	99
	8.17 Multiplier and Accumulator(MAC)	99
9.	Electrical Characteristic	104
	9.1 DC Electrical Characteristics	104
	9.2 Power Consumption	105
10.	Application.....	106

Appendix..... 108

1. General Description

RA8911 is an 8-bit downloadable micro-controller. Up to 22MHz system clock makes it a perfect choice for high-end device. It contains a 16x16 Multiplier and Accumulator (MAC), which not only greatly reduce programmer's effort, but also shorten development time. RA8911 is embedded 4-channel 10-Bit ADC that can vary your application fields in analog detection, such as temperature, pressure, humidity, etc. Moreover, matched with LCM (LCD Module), 10-bit ADC can be perfectly used in Touch Panel function.

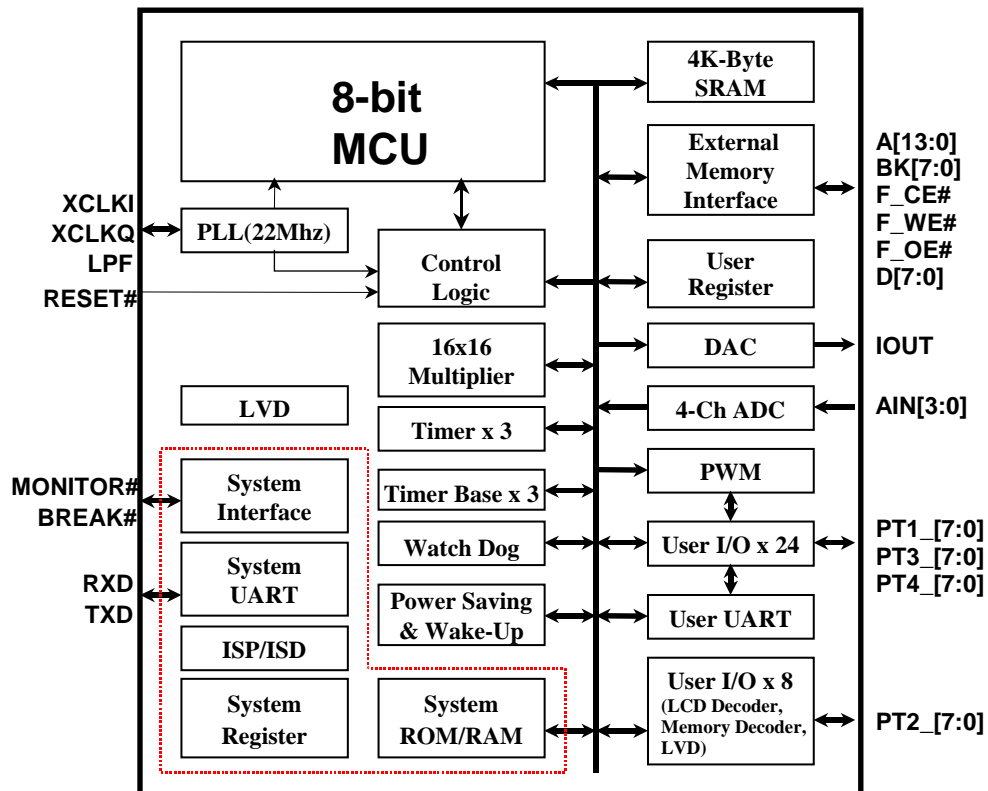
RA8911 is suitable for any downloadable device no matter used by end-users for voice/data download, or used by programmers for S/W program updated. The built-in 4K-byte ROM supports the on-chip RAiO ICE Monitor program, ISP(In-System Programming) and ISD(In-System Debugging), which controls the UART and enables the RS232 connection between the RA8911 and a PC host. Besides that, IrDA application is also allowed to give the device multiple attractive characteristics.

In short, RA8911 supports embedded 4K-byte SRAM, three I/O ports, LCD interface, built in PLL / RC Oscillator, LVD, multiple timer/counter sources, versatile interrupt-handling architecture, built-in one DAC (Digital-to-Analog Converters), 16x16 Multiplier and Accumulator (MAC) and support 4-channel 10-Bit ADC.

2. Feature

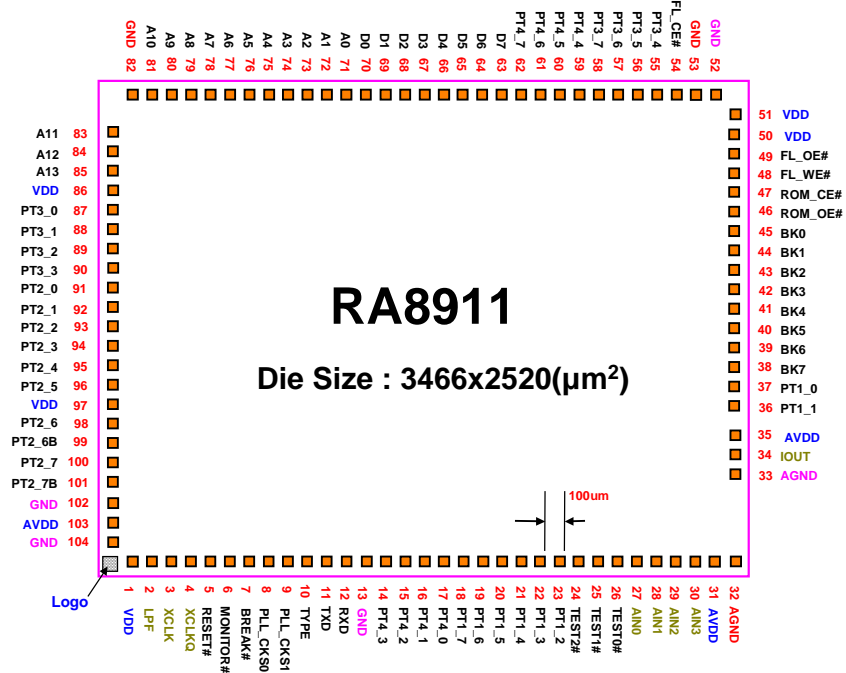
- ◆ 8-bit Micro Processor for Maximum 22MHz
- ◆ Internal 4K-Byte SRAM
- ◆ Flexible External Flash Support
- ◆ Flexible I/O Interrupt & Wake-Up Mode
- ◆ Support Wake-Up Reset Mode
- ◆ Support LVD(Low Voltage Detector)
- ◆ Support External Memory Interface
- ◆ Support LCD Interface
- ◆ Support PWM Output with 50% or 100% duty select
- ◆ Four 8-Bits Programmable I/O Port
- ◆ Three 12-Bits Timer
- ◆ Six Time-Base Options
- ◆ Watch Dog Timer
- ◆ One 4 -Level 10-bits Fixed Current Mode DAC
- ◆ Support 4-channel 10-bit ADC with Touch Panel Function
- ◆ One User's UART with Baud Rate Generator, Up to 115200bps
- ◆ UART Provide Normal, IrDA/ASK IR Mode
- ◆ Support UART Wakeup
- ◆ Support Idle/Sleep/Power Saving Mode
- ◆ Support Timer Wake-Up Mode
- ◆ Support H/W 16x16 Multiplier with Adder Option
- ◆ 1Hz, 2Hz and 1/60Hz Interrupt/Wake up
- ◆ Built in PLL, Only need one 32768Hz X'tal or Resistor for Oscillator
- ◆ Low Power Consumption
- ◆ Operating Voltage: 2.4V ~ 3.6V
- ◆ Package: Die Form or PQFP-100Pin

3. Block Diagram



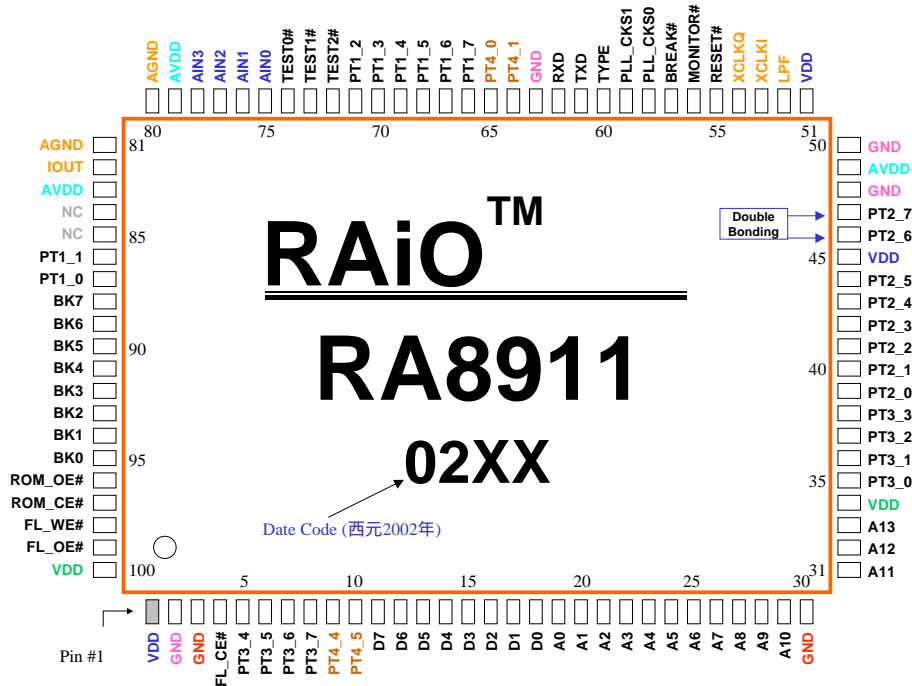
4. Die Form

4.1 PAD Diagram



Note: 1. PT2_6 and PT2_6B are double bonding
2. PT2_7 and PT2_7B are double bonding

4.2 Pin Assignment(PQFP-100Pin)



4.3 PAD X/Y Coordinate

Pad Order	Text Name	X-axis	Y-axis
83	A11	-1639.35	1050
84	A12	-1639.35	950
85	A13	-1639.35	850
86	VDD	-1639.35	750
87	PT3_0	-1639.35	650
88	PT3_1	-1639.35	550
89	PT3_2	-1639.35	450
90	PT3_3	-1639.35	350
91	PT2_0	-1639.35	250
92	PT2_1	-1639.35	150
93	PT2_2	-1639.35	50
94	PT2_3	-1639.35	-50
95	PT2_4	-1639.35	-150
96	PT2_5	-1639.35	-250
97	VDD	-1639.35	-350
98	PT2_6	-1639.35	-450
99	PT2_6B	-1639.35	-550
100	PT2_7	-1639.35	-650
101	PT2_7B	-1639.35	-750
102	GND	-1639.35	-850
103	VDD	-1639.35	-950
104	GND	-1639.35	-1055
1	VDD	-1550.0	-1166.35
2	LPF	-1449.88	-1166.35
3	XCLK	-1349.88	-1166.35
4	XCLKQ	-1249.88	-1166.35
5	RESET#	-1149.88	-1166.35
6	MONITOR#	-1049.88	-1166.35
7	BREAK#	-949.88	-1166.35
8	PLL_CKS0	-849.88	-1166.35
9	PLL_CKS1	-749.88	-1166.35
10	TYPE	-649.88	-1166.35
11	TXD	-549.88	-1166.35
12	RXD	-449.88	-1166.35
13	GND	-349.88	-1166.35
14	PT4_3	-249.88	-1166.35
15	PT4_2	-149.88	-1166.35
16	PT4_1	-49.88	-1166.35
17	PT4_0	50.12	-1166.35
18	PT1_7	150.12	-1166.35
19	PT1_6	250.12	-1166.35
20	PT1_5	350.12	-1166.35
21	PT1_4	450.12	-1166.35
22	PT1_3	550.12	-1166.35
23	PT1_2	650.12	-1166.35
24	TEST2#	750.12	-1166.35
25	TEST1#	850.12	-1166.35
26	TEST0#	950.12	-1166.35
27	AIN0	1050.62	-1166.35

Pad Order	Text Name	X-axis	Y-axis
28	AIN1	1157.62	-1166.35
29	AIN2	1263.61	-1166.35
30	AIN3	1370.61	-1166.35
31	AVDD	1476.11	-1166.35
32	AGND	1576.11	-1166.35
33	AGND	1639.35	-736.3
34	IOUT	1639.35	-635.8
35	AVDD	1639.35	-536.3
36	PT1_1	1639.35	-432
37	PT1_0	1639.35	-332
38	BK7	1639.35	-232
39	BK6	1639.35	-132
40	BK5	1639.35	-32
41	BK4	1639.35	68
42	BK3	1639.35	168
43	BK2	1639.35	268
44	BK1	1639.35	368
45	BK0	1639.35	468
46	ROM_OE#	1639.35	568
47	ROM_CE#	1639.35	668
48	FL_WE#	1639.35	768
49	FL_OE#	1639.35	868
50	VDD	1639.35	968
51	VDD	1639.35	1068
52	GND	1521.45	1166.35
53	GND	1416.45	1166.35
54	FL_CE#	1316.45	1166.35
55	PT3_4	1177	1166.35
56	PT3_5	1077	1166.35
57	PT3_6	977	1166.35
58	PT3_7	877	1166.35
59	PT4_4	777	1166.35
60	PT4_5	677	1166.35
61	PT4_6	577	1166.35
62	PT4_7	477	1166.35
63	D7	377	1166.35
64	D6	277	1166.35
65	D5	177	1166.35
66	D4	77	1166.35
67	D3	-23	1166.35
68	D2	-123	1166.35
69	D1	-223	1166.35
70	D0	-323	1166.35
71	A0	-423	1166.35
72	A1	-523	1166.35
73	A2	-623	1166.35
74	A3	-723	1166.35
75	A4	-823	1166.35
76	A5	-923	1166.35

77	A6	-1023	1166.35
78	A7	-1123	1166.35
79	A8	-1223	1166.35
80	A9	-1323	1166.35
81	A10	-1423	1166.35
82	GND	-1523	1166.35

5. Pin Description

Signal	I/O	Description
RESET#	IN	External Hardware Reset, active low. This pin is used to reset the system.
BREAK#	IN	User Program Break, active low. This signal is used to break the user's program from the ISD mode.
MONITOR#	IN	Monitor Program Select, active low. This signal is used to select the system boot from monitor program (ROM) or user program (Flash). This signal has to pull low when the user wants to download the data from PC or enter the ISP/ISD mode. Note: Couldn't be floating.
PT1_[7:0]	I/O	Bit 7~0 of Port 1 These are programmable pins for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT2_7	I/O	Bit-7 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
PWM1		The PT2_7 is also as the output of PWM. In PWM mode, the pin is always output and 72mA-driving current is selected.
PT2_6	I/O	Bit-6 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
PWM2		The PT2_6 is also as the output of PWM. In PWM mode, the pin is always output and 72mA-driving current is selected.
PT2_5	I/O	Bit-5 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
EXP_WR#		The PT2_5 is also as the write control of register \$101E. If the write register \$101F enabled, the pin is always output except the power saving mode.
PT2_4	I/O	Bit-4 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
FL_CE2#		The PT2_4 is also as the secondary external flash chip select. If the secondary flash is enabled, the pin is always output except the power saving mode.
PT2_3	I/O	Bit-3 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
LVD_#		The PT2_3 is also as the output of LVD. If the LVD enabled, the pin is always output except the power saving mode.
PT2_2	I/O	Bit-2 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
MEM_WE#		The PT2_2 is also as the external memory write enable. If the external memory enabled, the pin is always output except the power saving mode. If REG[1032h] bit6 is set as 1, and then MEM_WE# and FL_WE# can be jointly used.

PT2_1	I/O	Bit-1 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
MEM_OE#		The PT2_1 is also as the external memory output enabling. If the external memory enabled, the pin is always output except the power saving mode. If REG[1032h] bit6 is set as 1, and then MEM_OE# and FL_OE# can be jointly used.
PT2_0	I/O	Bit-0 of Port 2 This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
MEM_CE#		The PT2_0 is also as the external memory chip selecting. If the external memory enabled, the pin is always output except the power saving mode.
PT3_7	I/O	Bit-7 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.
PT3_6	I/O	Bit-6 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.
PT3_5	I/O	Bit-5 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.
PT3_4	I/O	Bit-4 of Port 3 This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.
PT3_3	I/O	Bit-3 of Port 3
TX		The PT3_3 is also as the transmission output of user's UART. In UART mode, the pin is always output except the power saving mode.
PT3_2	I/O	Bit-2 of Port 3
RX		The PT3_2 is also as the receive input of user's UART. In UART mode, the pin is always input.
PT3_1	I/O	Bit-1 of Port 3
LCD_E		The PT3_1 is also as the chip enable of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
PT3_0	I/O	Bit-0 of Port 3
LCD_RW		The PT3_0 is also as the read/write signal of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
PT4_[7:0]	I/O	Bit 7~0 of Port 4 This is a programmable pin for general-purpose I/O Port 4. The driving current and pull-high or pull-low can be selected by user register.
IOUT	OUT	DAC Current Output This pin is the current output of DAC.

AIN[3-0]	IN	ADC Analog Input These pins are the analog input of 10-bit ADC for 4-channel.		
		ADC Mode	Touch Panel Mode	

		AIN0	X1	
		AIN1	X2	
		AIN2	Y1	
		AIN3	Y2	
ADDR[13:0]	OUT	14-bit Address Bus. These signal are used for external memory address bus.		
D[7:0]	I/O	8-bit Data Bus. These signal are used for external memory data bus.		
FL_CE#	OUT	Flash Chip Select, active low. This signal is used for external flash.		
FL_WE#	OUT	Flash Write Enable, active low. This signal is used for external flash. If REG[1032h] bit6 is set as 1, and then FL_WE# and MEM_WE can be jointly used.		
FL_OE#	OUT	Flash Output Enable, active low. This signal is used for external flash. If REG[1032h] bit6 is set as 1, and then FL_OE# and MEM_OE# can be jointly used.		
BK[7:0]	OUT	Bank Bus. Register FBANK[1030h] and Ext_SBANK [103Fh] jointly use Bank[7:0] Bus as the output of memory bank register. Normally, they are connected to the higher address of external Flash memory.		
RXD	IN	Receive Data This is the received data input of system UART. Normally it's connected to the RS232's TX of PC.		
TXD	OUT	Transmit Data This signal is the transmitted data output of system UART. Normally it's connected to the RS232's RX of PC.		
XCLKI	IN	Oscillator Input. This is the input signal of external X'tal.		
XCLKQ	OUT	Oscillator Output. This is the output signal of external X'tal.		
LPF	IN	Low Pass Filter Input. This signal is connected to the external low pass filter for internal PLL.		
PLL[1:0]	IN	PLL Frequency Select These input signals are used to select the PLL speed during the hardware reset.		
		PLL1 PLL0	PLL Clock	UART Clock

		0 0	1.47MHz	368.64KHz
		0 1	2.46 MHz	614.4KHz
		1 0	7.37 MHz	1.8432MHz
		1 1	22.1 MHz	1.8432MHz
		Note: Couldn't be floating.		
TYPE	IN	PLL Clock Select This Pin is used to select the clock source of PLL. 0: RC Oscillator 1: 32768 X'tal Note: Couldn't be floating.		

TEST[2:0]#	IN	Test Pins are for RAiO's internal testing purpose used in testing IC and ROM status. Normally, users will not use these pins. Therefore, please connect these three pins to VDD when making PCB board.
VDD	PWR	Power Supply Voltage.
AVDD	PWR	Analog Power Supply Voltage.
GND	PWR	Ground.
AGND	PWR	Analog Ground.

7. Registers Description

Address	Register	7	6	5	4	3	2	1	0	R/W
1000h	NMI_MK(1)	REV.	TM3	TM2	TM1	WTD	PT3	PT2	PT1	R/W
1001h	NMI_MK(2)	--	--	--	--	REV.	1MIN	1HZ	2HZ	R/W
1002h	NMI_ST (1)	REV.	TM3	TM2	TM1	WTD	PT3	PT2	PT1	R
1003h	NMI_ST (2)	--	--	--	--	REV.	1MIN	1HZ	2HZ	R
1004h	CLR_NMI(1)	REV.	TM3	TM2	TM1	WTD	PT3	PT2	PT1	W
1005h	CLR_NMI(2)	--	--	--	--	REV.	1MIN	1HZ	2HZ	W
1006h	INT_MK(1)	REV.	TM3	TM2	TM1	REV.	PT3	PT2	PT1	R/W
1007h	INT_MK(2)	REV.	TB3	TB2	TB1	REV.	1MIN	1HZ	2HZ	R/W
1008h	INT_ST(1)	REV.	TM3	TM2	TM1	REV.	PT3	PT2	PT1	R
1009h	INT_ST(2)	REV.	TB3	TB2	TB1	REV.	1MIN	1HZ	2HZ	R
100Ah	CLR_INT(1)	REV.	TM3	TM2	TM1	REV.	PT3	PT2	PT1	W
100Bh	CLR_INT(2)	REV.	TB3	TB2	TB1	REV.	1MIN	1HZ	2HZ	W
100Ch	WDT_CTL	--	--	--	--	WDT_EN	WDT_LOOP	WTD_CLR	WTD_RST_EN	R/W
100Dh	LCD_CTL	--	--	--	--	REV.	SPD_1	SPD_0	EX_LCD	R/W
100Eh	LCD(1)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
100Fh	LCD(2)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1010h	TM1_H	0	0	0	0	D11	D10	D9	D8	R/W
1011h	TM1_L	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1012h	TM1_CTL	TM1_EN	TM1_SLP_EN	TM1_WK_RST_EN	REV.	TM1_L_OOP	CKS2	CKS1	CKS0	R/W
1013h	TM2_H	0	0	0	0	D11	D10	D9	D8	R/W
1014h	TM2_L	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1015h	TM2_CTL	TM2_EN	TM2_SLP_EN	TM2_WK_RST_EN	REV.	TM2_L_OOP	CKS2	CKS1	CKS0	R/W
1016h	TM3_H	0	0	0	0	D11	D10	D9	D8	R/W
1017h	TM3_L	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1018h	TM3_CTL	TM3_EN	0	0	0	TM3_L_OOP	CKS2	CKS1	CKS0	R/W
1019h	DAC_H	D9	D8	D7	D6	D5	D4	D3	D2	W
101Ah	DAC_L	D1	D0	--	--	--	--	--	--	W
101Bh	DAC_CTL	--	--	--	--	REV.	MODE	DAC-S1	DAC-S0	R/W
101Ch	PWM	D7	D6	D5	D4	D3	D2	D1	D0	W
101Dh	PWM_CTL	--	--	--	PWM_EN	PWM_MD	PWM_DUTY	PWM_RS1	PWM_RS0	R/W
101Eh	EX_IO	D7	D6	D5	D4	D3	D2	D1	D0	W
101Fh	EX_IO_CTL	--	--	--	--	--	--	EXP_WR_ACT	EXP_WR	R/W
1020h	PT1	D7	D6	D5	D4	D3	D2	D1/TM2_CK	D0/TM1_CK	R/W
1021h	PT1_DIR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1022h	PT1_INT	PT1_7	PT1_6	PT1_5	PT1_4	PT1_3	PT1_2	PT1_1	PT1_0	R/W
1023h	PT1_MOD	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1024h	PT2	D7/PWM1	D6/PWM2	D5/EXP_WR	D4/FL_CE2#	D3/LVD#	D2/MEM_WE#	D1/MEM_OE#	D0/MEM_CE#	R/W
1025h	PT2_DIR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1026h	PT2_INT	PT2_7	PT2_6	PT2_5	PT2_4	PT2_3	PT2_2	PT2_1	PT2_0	R/W
1027h	PT2_MOD	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1028h	PT3	D7	D6	D5	D4	D3/TX	D2/RX	D1/LCD_E	D0/LCD_RW	R/W
1029h	PT3_DIR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
102Ah	PT3_INT	PT3_7	PT3_6	PT3_5	PT3_4	PT3_3	PT3_2	PT3_1	PT3_0	R/W
102Bh	I/O_R	R7	R6	R5	R4	R3	R2	R1	R0	R/W
102Ch	I/O_I	I7	I6	I5	I4	I3	I2	I1	I0	R/W

102Dh	I/O_INT	PT2_H _CK	PT2_L _CK	PT1_H _CK	PT1_L _CK	PT2_H_EN /PT1_3INT	PT2_L_EN /PT1_2INT	PT1_H_EN /PT1_1INT	PT1_L_EN /PT1_0INT	R/W
102Eh	I/O_INT& WK_MD	PT2_H _MD1	PT2_H _MD0	PT2_L _MD1	PT2_L _MD0	PT1_H _MD1	PT1_H _MD0	PT1_L _MD1	PT1_L _MD0	R/W
102Fh	I/O_WK_MD	PT3_H _EN	PT3_L _EN	PT3_H _MD	PT3_L _MD	PT2_H _MD	PT2_L _MD	PT1_H _MD	PT1_L _MD	R/W
1030h	FBANK	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1031h	TB_CTL	--	--	--	MAC_ CLK	TB3	TB2/TB 1	1MIN	1Hz/ 2Hz	R/W
1032h	MEM_CTL	--	Ext_Pin _CTL	--	--	REV.	SPD_1	SPD_0	EXT_ MEM	R/W
1033h	LVD_CTL	--	--	--	--	EXT_LVD	LVD_EN	LVD_S1	LVD_S0	R/W
1034h	LVD_ST	Ni_Bit _CTL	--	--	--	--	--	--	LVD_DET	R/W
1035h	RXR	D7	D6	D5	D4	D3	D2	D1	D0	R
1035h	TXR	D7	D6	D5	D4	D3	D2	D1	D0	W
1036h	IR_CTL	--	--	--	--	--	--	MD1	MD0	R/W
1037h	BAUD	--	--	--	--	--	--	D1	D0	W
1038h	UR_CTL	TX_INT_ _EN	RX_INT_ _EN	REV.	UR_EN	UR_TX_ _INV	UR_RX_ _INV	URWK_ RST_EN	URWK_ _EN	R/W
1039h	UR_ST	TX_EMP _T	RX_RDY	REV.	REV.	--	--	--	--	R/W
103Ah	ADC_H	D9	D8	D7	D6	D5	D4	D3	D2	R
103Bh	ADC_L	D1	D0	--	--	--	--	--	--	R
103Ch	ADC_CTL(1)	--	INT_EN	LOOP	MODE	EN	CKSEL	S1	S0	W
103Dh	ADC_CTL(2)	ADET_ WK_E _N	ADET_ WK_M _D	--	--	Y2	Y1	X2	X1	W
103Eh	ADC_ST	--	--	--	--	--	--	TR_RDY	TCH_DET	R/W
103Fh	Ext_SBANK	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1040h	MTP_AL	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1041h	MTP_AH	D15	D14	D13	D12	D11	D10	D9	D8	R/W
1042h	MTP_BL	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1043h	MTP_BH	D15	D14	D13	D12	D11	D10	D9	D8	R/W
1044h	MTP_CLL	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1045h	MTP_CLH	D15	D14	D13	D12	D11	D10	D9	D8	R/W
1046h	MTP_CHL	D23	D22	D21	D20	D19	D18	D17	D16	R/W
1047h	MTP_CHH	D31	D30	D29	D28	D27	D26	D25	D24	R/W
1048h	MTP_CTL	OVF3	OVF2	OVF1	OVF0	CX_CLR	ACC	AX	BX	R/W
1049h	LT_WK_CTL	REV.	1/60HZ_ WK_MD	1HZ_WK _MD	2HZ_WK _MD	REV.	1/60Hz_ WK_EN	1Hz_WK _EN	2Hz_WK _EN	R/W
104Ah	LT_WK_ST	--	--	--	--	REV.	1/60HZ_ WK	1HZ_WK	2HZ_WK	R/W
104Bh	PWR_CTL	--	--	--	--	EXT_SLP	S/W_RST _EN	DP_SLP	SLEEP	R/W
104Ch	CLK_CTL	PLL_S1	PLL_S0	USR_DIV _CKSEL	CPU	DIV1	DIV0	STOP_PLI	STOP_ XCLK	R/W
104Dh	RST_ST	POR	RST#	WTD	S/W	IO	SYS_UR	UR	0	R/W
104Eh	PT4	D7	D6	D5	D4	D3	D2	D1	D0	R/W
104Fh	PT4_DIR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1050h	PFCR	--	--	Erase_ ST	Erase_ TY	Prog_S _T	STS	FSEL	FTYPE	R/W
1051h	PFFR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1052h	PFAHR	D15	D14	D13	D12	D11	D10	D9	D8	R/W
1053h	PFALR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1054h	PFDR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
1055h	FSAHR	D15	D14	D13	D12	D11	D10	D9	D8	R/W
1056h	FSALR	D7	D6	D5	D4	D3	D2	D1	D0	R/W

[REG 1000h]: NMI Mask Register (1) [\[NMI_MK\(1\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	Timer 3 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
4	Timer 1 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
3	Watch Dog NMI Enable 0: Disable 1: Enable	0h	0h	R/W
2	Port 3 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
1	Port 2 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
0	Port 1 NMI Enable 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #0Fh
STA    1000h    ; Permit Port1, Port2, Port3 and WDT to produce NMI
```

interrupt.

[REG 1001h]: NMI Mask Register (2) [\[NMI_MK\(2\)\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	Reserved	0h	0h	R/W
2	1Min. NMI Enable 0: Disable 1: Enable	0h	0h	R/W
1	1HZ NMI Enable 0: Disable 1: Enable	0h	0h	R/W
0	2HZ NMI Enable 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #02h
STA    1001h    ; Permit 1Hz to produce NMI interrupt.
```

[REG 1002h]: NMI Status Register (1) [\[NMI_ST\(1\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	Timer 3 NMI Indicate	0h	0h	R/W
5	Timer 2 NMI Indicate	0h	0h	R/W
4	Timer 1 NMI Indicate	0h	0h	R/W

3	Watch Dog NMI Indicate	0h	0h	R/W
2	Port 3 NMI Indicate	0h	0h	R/W
1	Port 2 NMI Indicate	0h	0h	R/W
0	Port 1 NMI Indicate	0h	0h	R/W

Example1:

LDA 1002h ; Can be used to diagnose which NMI occurs.

Example2:

LDA 1000h ; Can be used to diagnose which NMI occurs.

[REG 1003h]: NMI Status Register (2) [NMI_ST(2)]

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	Reserved	0h	0h	R/W
2	1Min. NMI Indicate	0h	0h	R/W
1	1HZ NMI Indicate	0h	0h	R/W
0	2HZ NMI Indicate	0h	0h	R/W

Example:

LDA 1003h ; Can be used to diagnose which NMI occurs.

[REG 1004h]: Clear NMI Status Register (1) [CLR_NMI(1)]

Bit	Description	Reset	Default	Access
7	Reserved	--	--	W
6	Clear Timer 3 NMI Indicate 1: Clear	--	--	W
5	Clear Timer 2 NMI Indicate 1: Clear	--	--	W
4	Clear Timer 1 NMI Indicate 1: Clear	--	--	W
3	Clear Watch Dog NMI Indicate 1: Clear	--	--	W
2	Clear Port 3 NMI Indicate 1: Clear	--	--	W
1	Clear Port 2 NMI Indicate 1: Clear	--	--	W
0	Clear Port 1 NMI Indicate 1: Clear	--	--	W

Example:

LDA #7Fh
STA 1004h ; Clear Timer1~ 3, Port1~3, and WTD NMI Indicate.

[REG 1005h]: Clear NMI Status Register (2) [CLR_NMI(2)]

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	Reserved	--	--	W
2	Clear 1Min. NMI Indicate 1: Clear	--	--	W
1	Clear 1HZ NMI Indicate 1: Clear	--	--	W

0	Clear 2HZ NMI Indicate 1: Clear	--	--	W
---	------------------------------------	----	----	---

Example:

```
LDA    #01h
STA    1005h    ; Clear 2Hz NMI Indicate.
```

[REG 1006h]: INT Mask Register (1) [\[INT_MK\(1\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	Timer 3 INT Enable 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 INT Enable 0: Disable 1: Enable	0h	0h	R/W
4	Timer 1 INT Enable 0: Disable 1: Enable	0h	0h	R/W
3	Reserved	0h	0h	R/W
2	Port 3 INT Enable 0: Disable 1: Enable	0h	0h	R/W
1	Port 2 INT Enable 0: Disable 1: Enable	0h	0h	R/W
0	Port 1 INT Enable 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #03h
STA    1006h    ; Permit Port1 and Port2 produce INT interrupt.
```

[REG 1007h]: INT Mask Register (2) [\[INT_MK\(2\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	2048HZ Time Base INT Enable	0h	0h	R/W
5	512HZ Time Base INT Enable	0h	0h	R/W
4	64HZ Time Base INT Enable	0h	0h	R/W
3	Reserved	0h	0h	R/W
2	1Min. INT Enable 0: Disable 1: Enable	0h	0h	R/W
1	1HZ INT Enable 0: Disable 1: Enable	0h	0h	R/W
0	2HZ INT Enable 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #01h
STA    1007h    ; Permit 2Hz produce INT interrupt.
```

[REG 1008h]: INT Status Register (1) [\[INT_ST\(1\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	Timer 3 INT Indicate	0h	0h	R/W
5	Timer 2 INT Indicate	0h	0h	R/W
4	Timer 1 INT Indicate	0h	0h	R/W
3	Reserved	0h	0h	R/W
2	Port 3 INT Indicate	0h	0h	R/W
1	Port 2 INT Indicate	0h	0h	R/W
0	Port 1 INT Indicate	0h	0h	R/W

Example:

LDA 1008h ; Can be used to diagnose which INT occurs.

[REG 1009h]: INT Status Register (2) [\[INT_ST\(2\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	2048HZ Time Base INT Indicate	0h	0h	R/W
5	512HZ Time Base INT Indicate	0h	0h	R/W
4	64HZ Time Base INT Indicate	0h	0h	R/W
3	Reserved	0h	0h	R/W
2	1Min. INT Indicate	0h	0h	R/W
1	1HZ INT Indicate	0h	0h	R/W
0	2HZ INT Indicate	0h	0h	R/W

Example:

LDA 1009h ; Can be used to diagnose which INT occurs.

[REG 100Ah]: Clear INT Status Register (1) [\[CLR_INT\(1\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	--	--	W
6	Clear Timer 3 INT Indicate 1: Clear	--	--	W
5	Clear Timer 2 INT Indicate 1: Clear	--	--	W
4	Clear Timer 1 INT Indicate 1: Clear	--	--	W
3	Reserved	--	--	W
2	Clear Port 3 INT Indicate 1: Clear	--	--	W
1	Clear Port 2 INT Indicate 1: Clear	--	--	W
0	Clear Port 1 INT Indicate 1: Clear	--	--	W

Example:

LDA #77h
STA 100Ah ; Clear Timer1~3 and Port1~3 INT indicate.

[REG 100Bh]: Clear INT Status Register (2) [\[CLR_INT\(2\)\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	--	--	W
6	Clear 2048HZ Time Base INT Indicate	--	--	W
5	Clear 512HZ Time Base INT Indicate	--	--	W
4	Clear 64HZ Time Base INT Indicate	--	--	W
3	Reserved	--	--	W
2	Clear 1Min. INT Indicate 1: Clear	--	--	W
1	Clear 1HZ INT Indicate 1: Clear	--	--	W
0	Clear 2HZ INT Indicate 1: Clear	--	--	W

Example:

```
LDA    #01h
STA    100Bh    ; Clear 2Hz INT indicate.
```

[REG 100Ch]: Watch Dog Control Register [\[WDT_CTL\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	Watch Dog Enable 0: Disable 1: Enable	0h	0h	R/W
2	Watch Dog Loop Control 0: Disable 1: Enable	0h	0h	R/W
1	Watch Dog Timer Clear 0: Disable. 1: Reset Watch Dog Timer, Write this bit high will cause Watch Dog Timer Reset. This bit will be clear automatically after clear.	0h	0h	R/W
0	Watch Dog Reset Enable 0: Disable 1: Enable	0h	0h	R/W

Example1:

```
LDA    #08h
STA    100Ch    ; Set Watch Dog Enable.
```

Example2:

```
LDA    #01h
STA    100Ch    ; Set Watch Dog Reset Enable.
```

[REG 100Dh]: LCD Control Register [\[LCD_CTL\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	Reserved	0h	0h	R/W

2-1	Hi-Speed Control for External LCD Decoder These two bits are use to add delay clock for LCD access time.					0h	0h	R/W
	Bit2	Bit1	T1	T2	T3 (Unit: CPU Clock)			

	0	0	4.5	11	0.5			
	0	1	3.5	9	0.5			
1	0	2.5	6	0.5				
1	1	1.5	3	0.5				
T1: Data Set-Up Time T2: Data Access Time T3: Data Hold Time								
0	External LCD Driver Control. This bit is used to control the external LCD Driver interface enable or disable. 0: Disable 1: Enable If set high, then the Port3 bit[1:0] are defined as LCD Driver interface signals. PT3_1 → LCD_E PT3_0 → LCD_RW					0h	0h	R/W

Example:

```
LDA    #01h
STA    100Dh    ; Enable external LCD Driver interface and add delay
                ; clock.
```

[REG 100Eh]: LCD Command Register [\[LCD\(1\)\]](#)

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

Example:

```
LDA    #50h
STA    100Eh    ; External LCD Driver Control Enable
```

[REG 100Fh]: LCD Data Register [\[LCD\(2\)\]](#)

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

Example:

```
LDA    #41h    ; Data Write, write "A" into LCD screen.
STA    100Fh
```

[REG 1010h]: Timer 1 Count_H Register [\[TM1_H\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3-0	Timer 1 Down Count Data – High Byte	Xh	Xh	R/W

[REG 1011h]: Timer 1 Count_L Register [\[TM1_L\]](#)

Bit	Description	Reset	Default	Access
7-0	Timer 1 Down Count Data – Low Byte	Xh	Xh	R/W

Example:

```
LDA    #05h
STA    1010h    ; Set Timer1 counter's High-Byte(Bit11-8) at 05h
LDA    #78h
STA    1011h    ; Set Timer1 counter's Low-Byte(Bit7-0) at 78h
                ; Set Timer1 counter at 578h
```

[REG 1012h]: Timer 1 Control Register [\[TM1_CTL\]](#)

Bit	Description	Reset	Default	Access
7	Timer 1 Enable or Timer 1 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 1 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 1 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
4	Reserved	0h	0h	R/W
3	Timer 1 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 1 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source ----- 0 0 0 External I/O Port (PT1_0) 0 0 1 USR_DIV_CLK /2^16 0 1 0 USR_DIV_CLK /2^14 0 1 1 USR_DIV_CLK /2^10 1 0 0 USR_DIV_CLK /2^6 1 0 1 USR_DIV_CLK /2^2 1 1 0 32768Hz 1 1 1 GND	0h	0h	R/W

Example:

```
LDA    #C5h
STA    1012h    ; Let Timer1 be Enable/Start → Timer1 only count once and
                ; it with wakeup function.
                ; Timer1's clock source set at USR_DIV_CLK /2^2.
```

[REG 1013h]: Timer 2 Count_H Register [\[TM2_H\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3-0	Timer 2 Down Count Data – High Byte	Xh	Xh	R/W

[REG 1014h]: Timer 2 Count_L Register [\[TM2_L\]](#)

Bit	Description	Reset	Default	Access
7-0	Timer 2 Down Count Data – Low Byte	Xh	Xh	R/W

Example:

```
LDA    #03h
STA    1013h    ; Set Timer2 counter's High-Byte(Bit11-8) at 03h
LDA    #BBh
STA    1014h    ; Set Timer2 counter's Low-Byte(Bit7-0) at BBh
```

; Set Timer2 counter at 3BBh

[REG 1015h]: Timer 2 Control Register [\[TM2_CTL\]](#)

Bit	Description	Reset	Default	Access
7	Timer 2 Enable or Timer 2 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 2 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
4	Reserved	0h	0h	R/W
3	Timer 2 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 2 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source ----- 0 0 0 External I/O Port (PT1_1) 0 0 1 USR_DIV_CLK /2^16 0 1 0 USR_DIV_CLK /2^14 0 1 1 USR_DIV_CLK /2^10 1 0 0 USR_DIV_CLK /2^6 1 0 1 USR_DIV_CLK /2^2 1 1 0 32768Hz 1 1 1 TIMER 1 Output	0h	0h	R/W

Example:

```
LDA    #63h
STA    1015h           ; Let Timer2 Wakeup/Reset Enable.
                        ; Timer2's clock source set at USR_DIV_CLK /2^10.
```

[REG 1016h]: Timer 3 Count_H Register [\[TM3_H\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3-0	Timer 3 Down Count Data – High Byte	Xh	Xh	R/W

[REG 1017h]: Timer 3 Count_L Register [\[TM3_L\]](#)

Bit	Description	Reset	Default	Access
7-0	Timer 3 Down Count Data – Low Byte	Xh	Xh	R/W

Example:

```
LDA    #03h
STA    1016h           ; Set Timer3 counter's High-Byte(Bit11-8) at 03h
LDA    #BBh
STA    1017h           ; Set Timer3 counter's Low-Byte(Bit7-0) at BBh
                        ; Set Timer3 counter at 3BBh
```


[REG 1018h]: Timer 3 Control Register [\[TM3_CTL\]](#)

Bit	Description	Reset	Default	Access
7	Timer 3 Enable or Timer 3 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6-4	Not Used	--	--	--
3	Timer 3 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 3 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source	0h	0h	R/W
	0 0 0 USR_DIV_CLK/2 ¹⁶			
	0 0 1 USR_DIV_CLK/2 ¹⁴			
	0 1 0 USR_DIV_CLK/2 ¹⁰			
	0 1 1 USR_DIV_CLK/2 ⁶			
	1 0 0 USR_DIV_CLK/2 ²			
	1 0 1 USR_DIV_CLK/2 ¹			
	1 1 0 USR_DIV_CLK			
1 1 1 32768Hz				

Example:

```

LDA    #8Dh
STA    1018h    ; Set Timer3 in loop mode before enable.
                ; Timer3's clock source set at USR_DIV_CLK /2^1.

LDA    #89h
STA    1018h    ; Timer3 start count.
    
```

[REG 1019h]: DAC High Byte Data Register [\[DAC_H\]](#)

Bit	Description	Reset	Default	Access
7-0	10-Bit DAC Output Data[9:2]	0h	0h	W

Example:

```

LDA    #01h
STA    101Bh    ; Set DAC1 Enable, Iout Resolution is 0~2mA.

LDA    #80h
STA    1019h    ; Data 80h to DAC1 → Output middle current.
    
```

[REG 101Ah]: DAC Data Register(II) [\[DAC_L\]](#)

Bit	Description	Reset	Default	Access
7-6	10-Bit DAC Output Data[1:0]	0h	0h	W
5-0	Not Used	--	--	--

[REG 101Bh]: DAC Control Register [\[DAC_CTL\]](#)

Bit	Description	Reset	Default	Access
7-3	Not Used	--	--	--
2	Mode Control 0: Audio Mode 1: DTMF Mode	0h	0h	R/W

Bit	DAC Output Resolution Control		IOUT (Audio Mode)	IOUT (DTMF Mode)	Reset	Default	Access
	Bit1	Bit0					
1-0	0	0	Disable	Disable	0h	0h	R/W
	0	1	0~2mA	0~200uA			
	1	0	0~2.5mA	0~200uA			
	1	1	0~3mA	0~200uA			

Example:

```
LDA    #00h
STA    101Bh    ; Disable DAC.
```

[REG 101Ch]: PWM Data Register [\[PWM\]](#)

Bit	Description	Reset	Default	Access
7-0	8-bit PWM Data	0h	0h	R/W

Example:

```
LDA    #10h
STA    101Dh    ; Set PWM1 Enable, produce 50% Duty cycle's PWM
                    ; pulse.
                    ; PWM Resolution is 8-Bit.

LDA    #60h
STA    101Ch    ; Data 60h to PWM output
```

[REG 101Dh]: PWM Control Register [\[PWM_CTL\]](#)

Bit	Description	Reset	Default	Access
7-5	Not Used	--	--	--
4	PWM Enable 0: Disable 1: Enable When PWM mode enable then the PT2_7 change to PWM1 output and PT2_6 change to PWM2 output.	0h	0h	R/W
3	PWM Mode Control 0: Single Mode (PWM1 Enable) In this mode, the PWM output is through PWM1(PT2-7) 1: Differential Mode (PWM1 & PWM2 Enable) Single Mode Differential Mode	0h	0h	R/W
	PWM1 : 00~FFh 80~FFh PWM2 : X 00~7Fh			
2	PWM Duty Control 0: 50 Duty Cycle for Differential Mode 1: 100 Duty Cycle for Differential Mode	0h	0h	R/W
1-0	PWM Resolution Control Bit1 Bit0 PWM Resolution	0h	0h	R/W
	0 0 8-Bit			
	0 1 7-Bit			
	1 0 6-Bit			
	1 1 5-Bit			

[REG 101Eh]: External Register [\[EX_IO\]](#)

Bit	Description	Reset	Default	Access
7-0	Data7-0	0h	0h	W

[REG 101Fh]: External REG-101Eh Control Register [\[EX_IO_CTL\]](#)

Bit	Description	Reset	Default	Access
7-2	Reserved	--	--	--
1	External REG-101Eh Write Signal Active Control This bit is used to control the active state of REG-101Eh write signal. 0: Active Low. 1: Active High	0h	0h	R/W
0	External REG-101Eh Write Signal Control This bit is used to control the output of REG-101Eh write signal. If set high, then the Port2 bit5 is defined as the output of REG-101Eh write. 0: Disable 1: Enable	0h	0h	R/W

[REG 1020h]: Port 1 Data Register [\[PT1\]](#)

Bit	Description	Reset	Default	Access
7-2	Bit-[7:2] of Output Data to Port 1 or Input from Port 1	0h	0h	R/W
1	Bit-1 of Output Data to Port 1 or Input from Port 1 This bit is also as the input of TM2 clock source when REG-1015h bit2-0 == '000'	0h	0h	R/W
0	Bit-0 of Output Data to Port 1 or Input from Port 1 This bit is also as the input of TM1 clock source when REG-1012h bit2-0 == '000'	0h	0h	R/W

Note: If the Port1 is output mode then the read access data is from the register 1020h. If the Port1 is input mode the read access is from Port1 I/O.

Example:

```
LDA    #FFh
STA    1021h    ; Set Port1 at output mode.
LDA    #AAh
STA    1020h    ; Output AAh to port1 Bit7~0.
```

[REG 1021h]: Port 1 Direction Control Register [\[PT1_DIR\]](#)

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 1 0: Input Mode 1: Output Mode <i>Note: If PT1[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</i>	0h	0h	R/W

Example:

```
LDA    #F0h
STA    1021h    ; Set Port1 Bit7~4 at output mode, Bit3~0 at input mode.
```

[REG 1022h]: Port1 Interrupt Trigger Indicate Register [\[PT1_INT\]](#)

Bit	Description	Reset	Default	Access
7-0	Port1 Bit[7:0] <i>Note: After using "Interrupt Indicate", users have to write command cleaning it to "0".</i>	0h	0h	R/W

Example:

```
LDA    1022    ; Determine which bit of Port1 is Interrupt.
```

[REG 1023h]: Port 1 Output Mode Select Register [PT1_MOD]

Bit	Description	Reset	Default	Access
7-0	Select the Output Mode for CMOS or Open-Drain Mode 0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 1 Direction Control Register controls the Port1 output data.	0h	0h	R/W

Example:

```
LDA    #FFh
STA    1021h    ; Set Port1 at output mode.
```

```
LDA    #F0h
STA    1023h    ; Set Port1 Bit7~4 at Open-Drain output mode.
                ; Bit3~0 is CMOS mode output mode.
```

[REG 1024h]: Port 2 Data Register [PT2]

Bit	Description	Reset	Default	Access
7	Bit-7 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of PWM2 when PWM enable(REG-101Dh bit4 = '1').	0h	0h	R/W
6	Bit-6 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of PWM2 when PWM enable(REG-101Dh bit4 = '1').	0h	0h	R/W
5	Bit-5 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of REG-101Eh write signal (EXP_WR#) when external REG-101Eh write enabled (REG-101Fh bit0= '1').	0h	0h	R/W
4	Bit-4 of Output Data to Port 2 or Input from Port 2 This bit is also as the secondary external Flash chip select output(FL_CE2#) when using two external flashes.	0h	0h	R/W
3	Bit-3 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of LVD indicated(LVD#) when external LVD enabled(REG-1033h bit2= '1').	0h	0h	R/W
2	Bit-2 of Output Data to Port 2 or Input from Port 2 This bit is also as the external memory write enable(MEM_WE#) when external memory decoder selected(REG-1032h bit0= '1').	0h	0h	R/W
1	Bit-1 of Output Data to Port 2 or Input from Port 2 This bit is also as the external memory output enable (MEM_OE#) when external memory decoder selected(REG-1032h bit0= '1').	0h	0h	R/W
0	Bit-0 of Output Data to Port 2 or Input from Port 2 This bit is also as the external memory chip select output (MEM_CE#) when external memory decoder enabled (REG-1032h bit0= '1'). The external memory is decoded when CPU access from \$4000 to \$7FFF.	0h	0h	R/W

Note: If the Port2 is output mode then the read access data is from the register 1024h. If the Port2 is input mode then the read access is from Port2 I/O.

Example:

```
LDA    #FFh
STA    1025h    ; Set Port2 at output mode.
LDA    #AAh
STA    1024h    ; Output AAh to port2 Bit7~0.
```

[REG 1025h]: Port 2 Direction Control Register [\[PT2_DIR\]](#)

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 2 0: Input Mode 1: Output Mode <i>Note: If PT2[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</i>	0h	0h	R/W

Example:

```
LDA    #F0h
STA    1025h    ; Set Port2 Bit7~4 at output mode, Bit3~0 at input mode.
```

[REG 1026h]: Port2 Interrupt Trigger Indicate Register [\[PT2_INT\]](#)

Bit	Description	Reset	Default	Access
7-0	Port2 Bit[7:0] <i>Note: After using "Interrupt Indicate", users have to write command cleaning it to "0".</i>	0h	0h	R/W

Example:

```
LDA    1026h    ; Determine which bit of Port2 in Interrupt.
```

[REG 1027h]: Port 2 Output Mode Select Register [\[PT2_MOD\]](#)

Bit	Description	Reset	Default	Access
7-0	Select the Output Mode for CMOS or Open-Drain Mode 0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 2 Direction Control Register controls the Port2 output data.	0h	0h	R/W

Example:

```
LDA    #FFh
STA    1025h    ; Set Port2 at output mode.

LDA    #F0h
STA    1027h    ; Set Port2 Bit7~4 at Open-Drain output mode.
                ; Bit3~0 is CMOS mode output mode.
```

[REG 1028h]: Port 3 Data Register [\[PT3\]](#)

Bit	Description	Reset	Default	Access
7-4	Bit-[7:4] of Output Data to Port 3 or Input from Port 3.	0h	0h	R/W
3	Bit-3 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of User UART TX when user UART enable(REG-1038h bit4 == '1').	0h	0h	R/W
2	Bit-2 of Output Data to Port 3 or Input from Port 3. This bit is also as the input of User UART RX when user UART enable(REG-1038h bit4 == '1').	0h	0h	R/W

1	Bit-1 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD chip select(LCD_E) when external LCD enabled(REG-100Dh bit0= '1'). The external LCD is decoded at REG-100Eh & REG-100Fh.	0h	0h	R/W
0	Bit-0 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD R/W(LCD_RW) when external LCD enabled(REG-100Dh bit0= '1').	0h	0h	R/W

Note: If the Port3 is output mode then the read access data is from the register 1028h. If the Port3 is input mode then the read access is form Port3 I/O.

Example:

```
LDA    #FFh
STA    1029h    ; Set Port3 at output mode.
LDA    #AAh
STA    1028h    ; Output AAh to port3 Bit7~0.
```

[REG 1029h]: Port 3 Direction Control Register [\[PT3_DIR\]](#)

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 3 0: Input Mode 1: Output Mode <i>Note: If PT3[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</i>	0h	0h	R/W

Example:

```
LDA    #F0h
STA    1029h    ; Set Port3 Bit7~4 at output mode, Bit3~0 at input mode.
```

[REG 102Ah]: Port3 Interrupt Trigger Indicate Register [\[PT3_INT\]](#)

Bit	Description	Reset	Default	Access
7-0	Port3 Bit[7:0] Interrupt Indicate <i>Note: After using "Interrupt Indicate", users have to write command cleaning it to "0".</i>	0h	0h	R/W

Example:

```
LDA    102Ah    ; Determine which bit of Port3 is Interrupt.
```

[REG 102Bh]: I/O Resistor Control Register [\[I/O_R\]](#)

Bit	Description	Reset	Default	Access
7	PT4 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
6	PT4 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
5	PT3 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
4	PT3 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W

3	PT2 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
2	PT2 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
1	PT1 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
0	PT1 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W

Example:

```
LDA    #3Fh
STA    102Bh    ; Set Port1~3 resister select is pull up 50K ohm.
```

[REG 102Ch]: I/O Driving Current Control Register [I/O_I]

Bit	Description	Reset	Default	Access
7	PT4 High Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
6	PT4 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
5	PT3 High Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
4	PT3 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
3	PT2 High Nibble Current Select 0: 4mA (12mA for PT2_6, PT2_7) 1: 8mA (36mA for PT2_6, PT2_7)	0h	0h	R/W
2	PT2 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
1	PT1 High Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
0	PT1 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W

Example:

```
LDA    #00h
STA    102Ch    ; Set Port1~3 current select is 4mA.
```

[REG 102Dh]: I/O Interrupt Control Register [I/O_INT]

Bit	Description	Reset	Default	Access
7	PT2 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W

6	PT2 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
5	PT1 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
4	PT1 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
3	PT2 High Nibble Interrupt or Wakeup (default) / PT1_3 Bit Interrupt 0: Disable 1: Enable <i>When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit3 could be used as Interrupt. Please refer to the following set-up:</i> 0: Disable 1: Enable	0h	0h	R/W
2	PT2 Low Nibble Interrupt or Wakeup (default) / PT1_2 Bit Interrupt 0: Disable 1: Enable <i>When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit2 could be used as Interrupt. Please refer to the following set-up:</i> 0: Disable 1: Enable	0h	0h	R/W
1	PT1 High Nibble Interrupt or Wakeup (default) / PT1_1 Bit Interrupt 0: Disable 1: Enable <i>When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit1 could be used as Interrupt. Please refer to the following set-up:</i> 0: Disable 1: Enable	0h	0h	R/W
0	PT1 Low Nibble Interrupt or Wakeup (default) / PT1_0 Bit Interrupt 0: Disable 1: Enable <i>When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit0 could be used as Interrupt. Please refer to the following set-up:</i> 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #80h
STA    1034h    ; I/O(Port1 bit0~3) bit Interrupt Control Enable.
LDA    #01h
STA    102Dh    ; It permitted Bit Interrupt occurs from Port1.0.
```


[REG 102Eh]: I/O Interrupt/Wakeup Mode Select Register [[I/O_INT&WK_MD](#)]

Bit	Description	Reset	Default	Access
7-6	PT2 High Nibble Mode Select Bit7 Bit6 Mode	0h	0h	R/W

	0 0 Rising-Edge Trigger			
	0 1 Falling-Edge Trigger			
	1 0 Level Change Trigger (1)			
1 1 Level Change Trigger (2)				
	Level Change Trigger (1): (1111) → Setup (1111) → (1111) → (1110) Trigger → (1010) → (0000) → (1111) Return → (1011) Trigger			
	Level Change Trigger (2): (1111) → Setup (1111) → (1111) → (1110) Trigger → (1010) Trigger → (1010) → (1011) Trigger → (1111) Trigger			
5-4	PT2 Low Nibble Mode Select Bit5 Bit4 Mode	0h	0h	R/W

	0 0 Rising-Edge Trigger			
	0 1 Falling-Edge Trigger			
	1 0 Level Change Trigger (1)			
1 1 Level Change Trigger (2)				
3-2	PT1 High Nibble Mode Select Bit3 Bit2 Mode	0h	0h	R/W

	0 0 Rising-Edge Trigger			
	0 1 Falling-Edge Trigger			
	1 0 Level Change Trigger (1)			
1 1 Level Change Trigger (2)				
1-0	PT1 Low Nibble Mode Select Bit1 Bit0 Mode	0h	0h	R/W

	0 0 Rising-Edge Trigger			
	0 1 Falling-Edge Trigger			
	1 0 Level Change Trigger (1)			
1 1 Level Change Trigger (2)				

Example:

```
LDA    #1Fh
STA    102Eh
```

; Set PT2 High Nibble is Rising -Edge Trigger, Low-Nibble

is

; Falling-Edge Trigger and PT1 is Level Change Trigger (2).

[REG 102Fh]: I/O Wakeup Reset Control Register [[I/O_WK_MD](#)]

Bit	Description	Reset	Default	Access
7	PT3 High Nibble Interrupt or Wakeup 0: Disable 1: Enable Note: PT3[7:4] are Rising-Edge Trigger.	0h	0h	R/W

6	PT3 Low Nibble Interrupt or Wakeup 0: Disable 1: Enable Note: PT3[1:0] are Rising-Edge Trigger, PT3[3:2] are Falling-Edge Trigger.	0h	0h	R/W
5	PT3 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
4	PT3 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
3	PT2 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
2	PT2 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
1	PT1 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
0	PT1 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W

Example:

```
LDA    #0Ch
STA    102Fh    ; Set PT2 Wakeup & Cause Reset Selected.
```

[REG 1030h]: Flash Bank Register [\[FBANK\]](#)

Bit	Description	Reset	Default	Access
7-0	Flash ROM Bank Select	0h	0h	R/W
	Bit7 6 5 4 3 2 1 0 Bank Select			
	0 0 0 0 0 0 0 0 Bank 0			
	0 0 0 0 0 0 0 1 Bank 1			
	0 0 0 0 0 0 1 0 Bank 2			
	0 0 0 0 0 0 1 1 Bank 3			
	..			
..				
..				
..				

Example:

```
LDA    #01h
STA    1030h    ; Set BK1 equal to 01h.
```

[REG 1031h]: Timer / Clock Control Register [\[TB_CTL\]](#)

Bit	Description	Reset	Default	Access
7-5	Not Used	--	--	--
4	Mac Control 0: Disable 1: Enable	0h	0h	R/W

3	Time Base 2048Hz Control 0: Disable 1: Enable	0h	0h	R/W
2	Time Base 512Hz/64Hz Control 0: Disable 1: Enable	0h	0h	R/W
1-0	Time Base 1Hz/2Hz/1Min Control Bit1 Bit0 Delay Cycle ----- 0 0: Disable 0 1: 1Hz/2Hz Enable 1 0: Not available 1 1: 1Min/1Hz/2Hz	0h	0h	R/W

Example1:

```
LDA     #10h
STA     1031h            ; Enable MAC Control.
```

Example2:

```
LDA     #01h
STA     1031h            ; Enable 1Hz/2Hz Control.
```

[REG 1032h]: Memory Control Register [[MEM_CTL](#)]

Bit	Description	Reset	Default	Access
7	Not Used	--	--	--
6	External Memory (SRAM & Flash) control pin share 0: Disable 1: Enable External Flash & SRAM share the FL_OE# and FL_WE# pins Note: The secondary Flash FL_CE# pin must be pulled high.	0h	0h	R/W
5-3	Not Used	--	--	--
2-1	Hi-Speed Control for External Flash or Memory Bit2 Bit1 Delay Cycle ----- 0 0: add Three delay cycle 0 1: add Two delay cycle 1 0: add One delay cycle 1 1: add Zero delay cycle	0h	0h	R/W
0	External Memory Control. This bit is used to control the external memory interface enable or disable. If set high, then the Port2 bit[2-0] are defined as memory interface signals. 0: Disable 1: Enable PT2_0 → MEM_CE# PT2_1 → MEM_OE# PT2_2 → MEM_WE#	0h	0h	R/W

Example:

```
LDA     #05h
STA     1032h            ; External Memory Control Enable, add One delay cycle.
```

[REG 1033h]: LVD Control Register [[LVD_CTL](#)]

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	LVD Output Control This bit is used to control the output of LVD. If set high, then the Port2 bit3 is defined as the output of LVD#. 0: Disable LVD output 1: Enable LVD Output	0h	0h	R/W
2	LVD Enable Control 0: Disable 1: Enable	0h	0h	R/W
1-0	LVD Voltage Select Bit1 Bit0 Detected Voltage ----- 0 0 3V 0 1 2.8V 1 0 2.6V 1 1 2.4V If the LVD enabled, the bit0 of register \$1034h will indicate the status of LVD.	0h	0h	R/W

Example:

```
LDA    #0Ch
STA    1033h    ; LVD Control Enable, LVD Detected Voltage Select 3V
                ; LVD Output Enable.
```

[REG 1034h]: LVD Status Register [[LVD_ST](#)]

Bit	Description	Reset	Default	Access
7	I/O Interrupt mode for Nibble or Bit control 0: Nibble Interrupt Control PT1 bit0~3, PT1 bit4~7, PT2 bit0~3 and PT2 bit4~7 are Nibble Interrupt. 1: Bit Interrupt Control PT1 bit0~3 are Bit Interrupt <i>Note: When REG[1034]bit7 is set as "1", please also refer to the set up of REG[102Dh] bit0~3, the bit interrupt.</i>	0h	0h	R
6-1	Not Used	--	--	--
0	LVD Indicate. 0: Normal Voltage 1: Low Voltage Detected!	0h	0h	R

[REG 1035h]: User UART Receive Register (Read Only) [[RXR](#)]

Bit	Description	Reset	Default	Access
7-0	UART Receive Data	Xh	Xh	R

[REG 1035h]: User UART Transmit Register (Write Only) [[TXR](#)]

Bit	Description	Reset	Default	Access
7-0	UART Transmit Data	0h	0h	W

[REG 1036h]: IR Mode Select [[IR_CTL](#)]

Bit	Description	Reset	Default	Access
7-2	Not Used.	--	--	--

Bit	UART IR Mode Select		Mode	Reset	Default	Access
	Bit1	Bit0				
1-0	0	0	Normal	0h	0h	R/W
	0	1	ASK IR			
	1	0	IrDA IR			
	1	1	IrDA IR			

Example:

```
LDA    #03h
STA    1036h    ; Set IrDA IR Mode.
```

[REG 1037h]: User UART Baud Rate Select [\[BAUD\]](#)

Bit	Description		Reset	Default	Access	
7-2	Not Used		--	--	--	
Bit	UART Baud Rate		Reset	Default	Access	
	Bit1	Bit0				Baud Rate
1-0	0	0	01h	01h	W	
	0	1				115200bps
	1	0				57600bps
	1	1				38400bps

Example:

```
LDA    #00h
STA    1037h    ; Set Baud Rate into 115200bps.
```

[REG 1038h]: User UART Control Register [\[UR_CTL\]](#)

Bit	Description	Reset	Default	Access
7	Transmit Empty Indicate INT Enable 0: Disable 1: Enable	0h	0h	R/W
6	Received Data Available Indicate INT Enable 0: Disable 1: Enable	0h	0h	R/W
5	Reserved	--	--	--
4	User UART Enable Control 1: Enable 0: Disable, 1.843MHz Clock Stop If set high, then the Port3 bit[3:2] are defined as Transmit and Receive interface signals. PT3_3 → TX PT3_2 → RX	0h	0h	R/W
3	UART Transmitter Inverter	0h	0h	R/W
2	UART Receiver Inverter	0h	0h	R/W
1	UART RX Wake Up Mode Select 0: UART Wake Up only 1: UART Wake Up & caused Reset	0h	0h	R/W
0	UART RX Wake Up 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #10h
STA    1038h    ; Enable UART function.
```

[REG 1039h]: User UART Status Register [UR_ST]

Bit	Description	Reset	Default	Access
7	Transmit Register Empty Indicate This bit is set when transmit complete and be clear when write a data to UART Transmit Register(REG-1035h).	0h	0h	R/W
6	Received Data Available Indicate This bit is set when UART received an available data but it will not be clear when the host read the data from UART Receive Register (REG-1035h).	0h	0h	R/W
5-0	Reserved	0h	0h	R/W

[REG 103Ah]: ADC High-Byte Register [ADC_H]

Bit	Description	Reset	Default	Access
7-0	ADC Output Data Bit[9:2]	0h	0h	R

[REG 103Bh]: ADC Low -Byte Register [ADC_L]

Bit	Description	Reset	Default	Access
7-6	ADC Output Data Bit[1:0]	0h	0h	R
5-0	Not Used	0h	0h	R

[REG 103Ch]: ADC Control Register(1) [ADC_CTL(1)]

Bit	Description	Reset	Default	Access																				
7	Reserved	0h	0h	W																				
6	ADC Interrupt Enable 0: Disable 1: Enable	0h	0h	W																				
5	ADC Loop Control 0: Disable 1: Enable	0h	0h	W																				
4	ADC Mode Select 0: 4-Channels ADC 1: Touch Panel	0h	0h	W																				
3	ADC Enable 0: Disable 1: Enable	0h	0h	W																				
2	ADC Clock Select <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="color: magenta;">ADC CKS \ PLL_CK</th> <th>0 0</th> <th>0 1</th> <th>1 0</th> <th>1 1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1.47 MHz</td> <td>2.46 MHz</td> <td>7.3 MHz</td> <td>22 MHz</td> </tr> <tr> <td>1</td> <td>376 KHz</td> <td>315 KHz</td> <td>469 KHz</td> <td>353 KHz</td> </tr> <tr> <td></td> <td>752 KHz</td> <td>630 KHz</td> <td>938 KHz</td> <td>707 KHz</td> </tr> </tbody> </table>	ADC CKS \ PLL_CK	0 0	0 1	1 0	1 1	0	1.47 MHz	2.46 MHz	7.3 MHz	22 MHz	1	376 KHz	315 KHz	469 KHz	353 KHz		752 KHz	630 KHz	938 KHz	707 KHz	0h	0h	W
		ADC CKS \ PLL_CK	0 0	0 1	1 0	1 1																		
		0	1.47 MHz	2.46 MHz	7.3 MHz	22 MHz																		
1	376 KHz	315 KHz	469 KHz	353 KHz																				
	752 KHz	630 KHz	938 KHz	707 KHz																				
Note: PLL Frequency Select (PLL_CK) is [REG104Ch]bit7~6																								

ADC Channel Select				
Bit1	Bit0	Channel		
0	0	0		
0	1	1		
1	0	2		
1	1	3		

1-0

Note: When RA8911 enters into Saving Mode, in order to avoid the leaking behavior, please do not let ADC Channel Floating or set ADC Type as Touch Panel function.

0h 0h W

Example:

```
LDA    #08h
STA    103Ch    ; Enable ADC and using ADC channel 0.
```

[REG 103Dh]: ADC Control Register(2) [\[ADC_CTL\(2\)\]](#)

Bit	Description	Reset	Default	Access
7	ADET Wake Up 0: Disable 1: Enable	0h	0h	R/W
6	ADET Wake Up Mode Select 0: ADET Wake Up Only 1: ADET Wake Up & Caused Reset	0h	0h	R/W
5-4	Reserved	--	--	--
3	Touch Panel Switch Y2 Control 0: Switch Off 1: Switch On	0h	0h	W
2	Touch Panel Switch Y1 Control 0: Switch Off 1: Switch On	0h	0h	W
1	Touch Panel Switch X2 Control 0: Switch Off 1: Switch On	0h	0h	W
0	Touch Panel Switch X1 Control 0: Switch Off 1: Switch On	0h	0h	W

Example:

```
LDA    #C0h
STA    103Dh    ; Enable ADET Wakeup & Reset.
```

[REG 103Eh]: ADC Status Register [\[ADC_ST\]](#)

Bit	Description	Reset	Default	Access
7-2	Not Used	--	--	--
1	ADC Transfer Done 0: Not Ready 1: Ready Note: When ADC is under One Time Mode (No Loop) and data transfer is finished, then it will generate Ready Signal (Bit 1=1). At this time, users need to clean the Ready Signal and let it become Bit 1=0 before read the next data.	0h	0h	R/W

0	Touch Panel Detector 0: Normal 1: Touch Detected	0h	0h	R
---	--	----	----	---

[REG 103Fh]: External SRAM Bank Register [\[Ext_SBANK\]](#)

Bit	Description	Reset	Default	Access
7-0	External SRAM Bank Select	0h	0h	R/W
	Bit7 6 5 4 3 2 1 0 Bank Select			
	0 0 0 0 0 0 0 0 Bank0			
	0 0 0 0 0 0 0 1 Bank1			
	0 0 0 0 0 0 1 0 Bank2			
	0 0 0 0 0 0 1 1 Bank3			
	..			
	..			
	..			

[REG 1040h]: Multiplier A Low-Byte Register [\[MTP_AL\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier A Data Bit[7:0]	0h	0h	R/W

[REG 1041h]: Multiplier A High-Byte Register [\[MTP_AH\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier A Data Bit[15:8]	0h	0h	R/W

[REG 1042h]: Multiplier B Low-Byte Register [\[MTP_BL\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier B Data Bit[7:0]	0h	0h	R/W

[REG 1043h]: Multiplier B High-Byte Register [\[MTP_BH\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier B Data Bit[15:8]	0h	0h	R/W

[REG 1044h]: Multiplier C Low Word Low-Byte Register [\[MTP_CLL\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[7:0]	0h	0h	R/W

[REG 1045h]: Multiplier C Low Word High-Byte Register [\[MTP_CLH\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[15:8]	0h	0h	R/W

[REG 1046h]: Multiplier C High Word Low-Byte Register [\[MTP_CHL\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[23:16]	0h	0h	R/W

[REG 1047h]: Multiplier C High Word High-Byte Register [\[MTP_CHH\]](#)

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[31:24]	0h	0h	R/W

[REG 1048h]: Multiplier Control Register [\[MTP_CTL\]](#)

Bit	Description	Reset	Default	Access
7-4	Overflow Flag	0h	0h	R
3	Clear CX 1: Clear CX 0: No Action	0h	0h	R/W
2	Accumulate Mode 0: Disable, $CX = AX \times BX$ 1: Enable, $CX_{n+1} = AX \times BX + CX_n$	0h	0h	R/W
1	AX 8/16Bit Select 0: AX = 16Bit 1: AX = 8Bit	0h	0h	R/W
0	BX 8/16Bit Select 0: BX = 16Bit 1: BX = 8Bit	0h	0h	R/W

[REG 1049h]: Low Speed Timer Control Register [\[LT_WK_CTL\]](#)

Bit	Description	Reset	Default	Access
7	Reserved	0h	0h	R/W
6	1Min. Wake Up Mode 0: Wake Up Only 1: Wake Up and Reset	0h	0h	R/W
5	1Hz Wake Up Mode 0: Wake Up Only 1: Wake Up and Reset	0h	0h	R/W
4	2Hz Wake Up Mode 0: Wake Up Only 1: Wake Up and Reset	0h	0h	R/W
3	Reserved	0h	0h	R/W
2	1Min. Wake Up 0: Disable 1: Enable	0h	0h	R/W
1	1Hz Wake Up 0: Disable 1: Enable	0h	0h	R/W
0	2Hz Wake Up 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #22h
STA    1049h    ; Enable 1Hz Wakeup, Wakeup and Reset mode.
```

[REG 104Ah]: Low Speed Timer Status Register [\[LT_WK_ST\]](#)

Bit	Description	Reset	Default	Access
7-4	Not Used	--	--	--
3	Reserved	0h	0h	R/W
2	1Min. Wake Up Indicate.	0h	0h	R/W
1	1Hz Wake Up Indicate.	0h	0h	R/W
0	2Hz Wake Up Indicate.	0h	0h	R/W

Example:

```
LDA    104Ah    ; Low Speed Timer Indicate.
```

[REG 104Bh]: Power Control Register [[PWR_CTL](#)]

Bit	Description	Reset	Default	Access
7-4	Reserved	0h	0h	R/W
3	Extra Sleep Mode(Only at RTC Mode) 0: Normal Sleep 1: Extra Deep Sleep In this mode, the Divisor is off and only 32768Hz X'tal, Low speed Timer circuit are active. But the Wakeup with Reset function is inhibited. This bit must used to go with bit-1 and bit-0. Only available when REG[104Bh] Bit[1:0] = 11b.	0h	0h	R/W
2	Software Reset 0: Disable. 1: Reset CPU, Write this bit high will cause CPU Reset. This bit will be clear automatically after reset.	0h	0h	R/W
1	Sleep Mode Select 0: Normal Sleep 1: Deep Sleep In normal sleep mode, the Divisor is off and only 32768Hz X'tal, Timer1, Timer2, I/O wakeup and UART wakeup circuit are active. In deep select mode, the Divisor is off and only 32768Hz X'tal, Timer1 and Timer2 wakeup circuit are active. But the Wakeup with Reset function is inhibited. This bit must used to go with bit-0.	0h	0h	R/W
0	Sleep Mode Control 0: Normal Operation Mode 1: Enter Sleep Mode.	0h	0h	R/W

Example1: ([Sleep Mode](#))

```
LDA    #01h
STA    104Bh    ; Enter Sleep Mode
```

Example2: ([Deep Sleep Mode](#))

```
LDA    #02h
STA    104Bh    ; Determine Deep Sleep Mode
LDA    104Bh
ORA    #01h
STA    104Bh    ; Enter Deep Sleep Mode
```

Example3: ([Extra Sleep Mode--Only at RTC Mode](#))

```
LDA    #0Ah
STA    104Bh    ; Determine Deep Sleep Mode
LDA    104Bh
ORA    #0Bh
STA    104Bh    ; Enter Extra Sleep Mode
```

[REG 104Ch]: Clock Control Register [CLK_CTL]

Bit	Description	Reset	Default	Access
7-6	PLL Frequency Select (Note1) Bit7 Bit6 PLL Clock UART Clock	0h	0h	R/W
	0 0 1.47MHz 368.64KHz (max. 23040bps)			
	0 1 2.46 MHz 614.4KHz (max. 38400bps)			
	1 0 7.37 MHz 1.8432MHz (max. 115200bps)			
1 1 22.1 MHz 1.8432MHz (max. 115200bps)				
5	User's Divisor Clock Select 0: PLL Clock 1: 32768Hz	0h	0h	R/W
4-2	CPU Clock Select Bit4 Bit3 Bit2 CPU Clock	000h	000h	R/W
	0 0 0 PLL_CLK RUN1 Mode			
	0 0 1 PLL_CLK RUN1 Mode			
	0 1 0 PLL_CLK RUN1 Mode			
	1 0 0 PLL_CLK /2 RUN1 Mode			
	1 0 1 PLL_CLK /4 RUN1 Mode			
	1 1 0 PLL_CLK /8 RUN1 Mode			
	1 1 1 32768Hz RUN1 Mode			
----- 0 1 1 32768Hz RUN2 Mode				
In RUN2 mode, the UART, IrDA and PWM are not available.				
1	PLL Clock On/Off Control 0: PLL On 1: PLL Off	0h	0h	R/W
0	X'tal-Oscillator (32768Hz) On/Off Control 0: X'tal-Oscillator (32768Hz) On 1: X'tal-Oscillator (32768Hz) Off	0h	0h	R/W

Example:

```
LDA    #C0h
STA    104Ch    ; Set PLL Clock is 22.1MHz.
```

Note1:

Bit7	Bit6	PLL Clock	UART Clock	ADC Clock REG 103Ch Bit2 = 1	ADC Clock REG 103Ch Bit2 = 0
0	0	1.47MHz	368.64KHz	735KHz	367KHz
0	1	2.46 MHz	614.4KHz	615KHz	307KHz
1	0	7.37 MHz	1.8432MHz	921KHz	460KHz
1	1	22.1 MHz	1.8432MHz	690KHz	345KHz

Note2:

From following table you will see the needed response time while Clock is switching.

PLL Switch	Response Time
1.47MHz to 1.47MHz	0
1.47MHz to 2.46MHz	1.5ms
1.47MHz to 7.37MHz	5ms
1.47MHz to 22.1MHz	11ms
2.46MHz to 1.47MHz	1ms
2.46MHz to 2.46MHz	0
2.46MHz to 7.37MHz	3.5ms
2.46MHz to 22.1MHz	9.5ms
7.37MHz to 1.47MHz	4.5ms
7.37MHz to 2.46MHz	3.5ms
7.37MHz to 7.37MHz	0
7.37MHz to 22.1MHz	6ms
22.1MHz to 1.47MHz	10.5ms
22.1MHz to 2.46MHz	9.5ms
22.1MHz to 7.37MHz	6ms
22.1MHz to 22.1MHz	0

[REG 104Dh]: Reset Status Register [[RST_ST](#)]

Bit	Description	Reset	Default	Access
7	Power On Reset Indicate	1h	0h	R/W
6	RESET (RST#) Pin Reset Indicate	0h	0h	R/W
5	Watch-Dog Reset Indicate	0h	0h	R/W
4	Software Reset Indicate	0h	0h	R/W
3	I/O Wake Up Reset Indicate	0h	0h	R/W
2	System UART RX Wake Up Reset Indicate	0h	0h	R/W
1	UART RX Wake Up Reset Indicate	0h	0h	R/W
0	Not Used	0h	0h	R

[REG 104Eh]: Port 4 Data Register [[PT4](#)]

Bit	Description	Reset	Default	Access
7-0	Bit-[7:0] of Output Data to Port 4 or Input from Port 4.	0h	0h	R/W

Note: If the Port4 is output mode then the read access date is from the register 1028h. If the Port4 is input mode then the read access is form Port4 I/O.

[REG 104Fh]: Port 4 Direction Control Register [[PT4_DIR](#)]

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 4 0: Input Mode 1: Output Mode	0h	0h	R/W

[REG 1050h]: Programming Flash Control Register [[PFCR](#)]

Bit	Description	Reset	Default	Access
-----	-------------	-------	---------	--------

7-6	Not Used.	--	--	--
5	Erase Status 0: Erase Error 1: Erase Success	0h	0h	R/W
4	Erase Type 0: Chip Erase 1: Sector Erase	0h	0h	R/W
3	Programming Status 0: Programming Error 1: Programming Success	0h	0h	R/W
2	Flash Control 0: Flash Chip1 (FL_CE# active) 1: Flash Chip2 (FL_CE2# active)	0h	0h	R/W
1	One or Two External Flash Option. This bit is used to indicate the external Flash number. This bit is read only. 0: One External Flash 1: Two External Flash	0h	0h	R/W
0	Flash Type 0: Command 1(Reference 8.3.1) 1: Command 2(Reference 8.3.1)	0h	0h	R/W

Example:

```
LDA    #00h
STA    1050h    ; Set One External Flash, Flash Type is Command 1
```

[REG 1051h]: Programming Flash FBANK Register [\[PFFR\]](#)

Bit	Description	Reset	Default	Access
7-0	Bank Data	0h	0h	R/W

[REG 1052h]: Programming Flash Address High Byte Register [\[PFAHR\]](#)

Bit	Description	Reset	Default	Access
7-0	Programming Flash Address --> A[15:8]	0h	0h	R/W

[REG 1053h]: Programming Flash Address Low Byte Register [\[PFALR\]](#)

Bit	Description	Reset	Default	Access
7-0	Programming Flash Address A[7:0]	0h	0h	R/W

[REG 1054h]: Programming Flash Data Register [\[PFDR\]](#)

Bit	Description	Reset	Default	Access
7-0	Programming Data	0h	0h	R/W

[REG 1055h]: Flash Sector Address High Byte Register [\[FSAHR\]](#)

Bit	Description	Reset	Default	Access
7-0	Flash Sector High Byte Address	0h	0h	R/W

[REG 1056h]: Flash Sector Address Low Byte Register [\[FSALR\]](#)

Bit	Description	Reset	Default	Access
7-0	Flash Sector Low Byte Address	0h	0h	R/W

8. Function Description

8.1 System Clock

RA8911 is built in PLL circuit; therefore, an external 32.768KHz crystal can generate system clock. Figure 8-1 is the block diagram of the system clock, and Figure 8-2 is the schema for system clock. Adjustable system clock can be used to achieve the best power management.

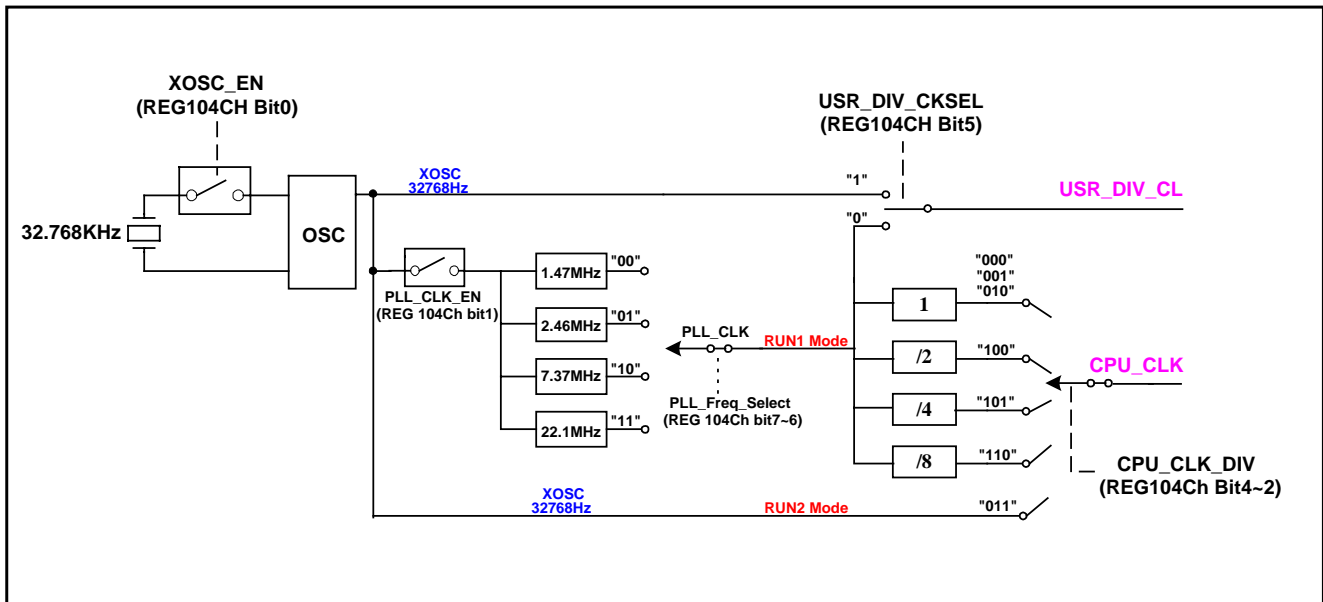


Figure 8-1 System Clock Block Diagram

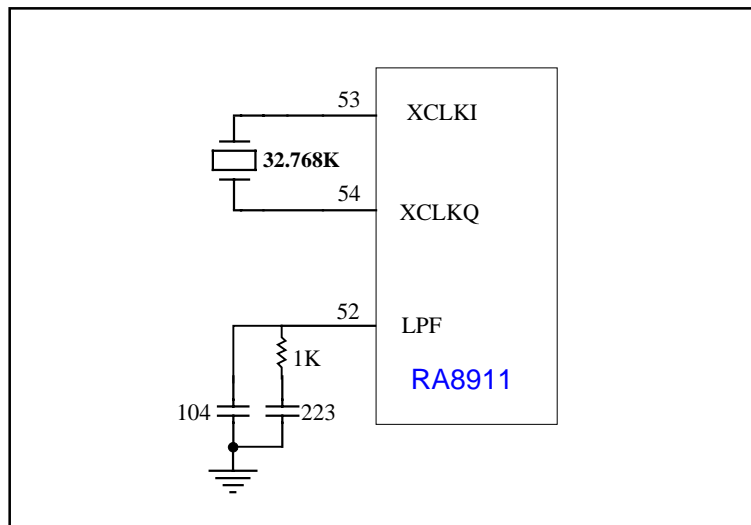


Figure 8-2 System Clock Schematic

From Figure 8-1, you will know that system clock is controlled by [REG 104Ch]. The descriptions of this Register are listed underneath, and we also provide an example program to explain how to use them.

[REG 104Ch]: Clock Control Register

Bit	Description	Reset	Default	Access
7-6	PLL Frequency Select Bit7 Bit6 PLL Clock UART Clock	0h	0h	R/W

	0 0 1.47MHz 368.64KHz			
	0 1 2.46 MHz 614.4KHz			
	1 0 7.37 MHz 1.8432MHz			
1 1 22.1 MHz 1.8432MHz				
5	User's Divisor Clock Select 0: PLL Clock 1: 32768Hz	0h	0h	R/W
4-2	CPU Clock Select Bit4 Bit3 Bit2 CPU Clock	000h	000h	R/W
	0 0 0 PLL_CLK RUN1 Mode			
	0 0 1 PLL_CLK RUN1 Mode			
	0 1 0 PLL_CLK RUN1 Mode			
	1 0 0 PLL_CLK /2 RUN1 Mode			
	1 0 1 PLL_CLK /4 RUN1 Mode			
	1 1 0 PLL_CLK /8 RUN1 Mode			
	1 1 1 32768Hz RUN1 Mode			

	0 1 1 32768Hz RUN2 Mode			
In RUN2 mode, the UART, IrDA and PWM are not available.				
1	PLL Clock On/Off Control 0: PLL On 1: PLL Off	0h	0h	R/W
0	X'tal-Oscillator (32768Hz) On/Off Control 0: X'tal-Oscillator (32768Hz) On 1: X'tal-Oscillator (32768Hz) Off	0h	0h	R/W

Example:

```

LDA    #10000000b          ; PLL_CLK→ Enable, XOCLK->Enable,
STA    CLK_CTL             ; USR_DIV_CLK→ SYS_CLK=7.3728MHz

LDA    #10101110b         ; PLL_CLK Disable, USR_DIV_CLK→ OSC=32768Hz
STA    CLK_CTL

```

8.2 CPU Operation Mode

8.2.1 Reset & Idle & Sleep & Power Saving Mode

RESET can be produced by Power On, RESET# input Low, Software Reset, Watch Dog overflow, Timer overflow, 1Hz, 2Hz, 1Min. and I/O. At this time, the chip will remain RESET until a movement of OST(Oscillator Start-up Timer) or RESET# input High.

When it is RESET, the statuses are as following:

- ◆ Continue to oscillate or being initialed (electric power raise or Wake Up from SLEEP)
- ◆ All I/O pins (PT1、 PT2、 PT3) enter into high impedance condition

- ◆ Set program counter as “FFFC”
- ◆ Registers are set as initial value

Figure 8-3 below is RESET schema, and Figure 8-4 is RESET Block Diagram. The functions of other RESET will be explained in the relevant chapters.

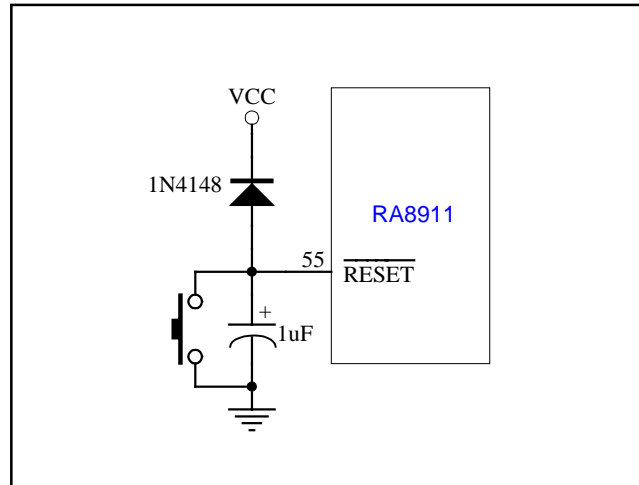


Figure 8-3 RESET Schematic

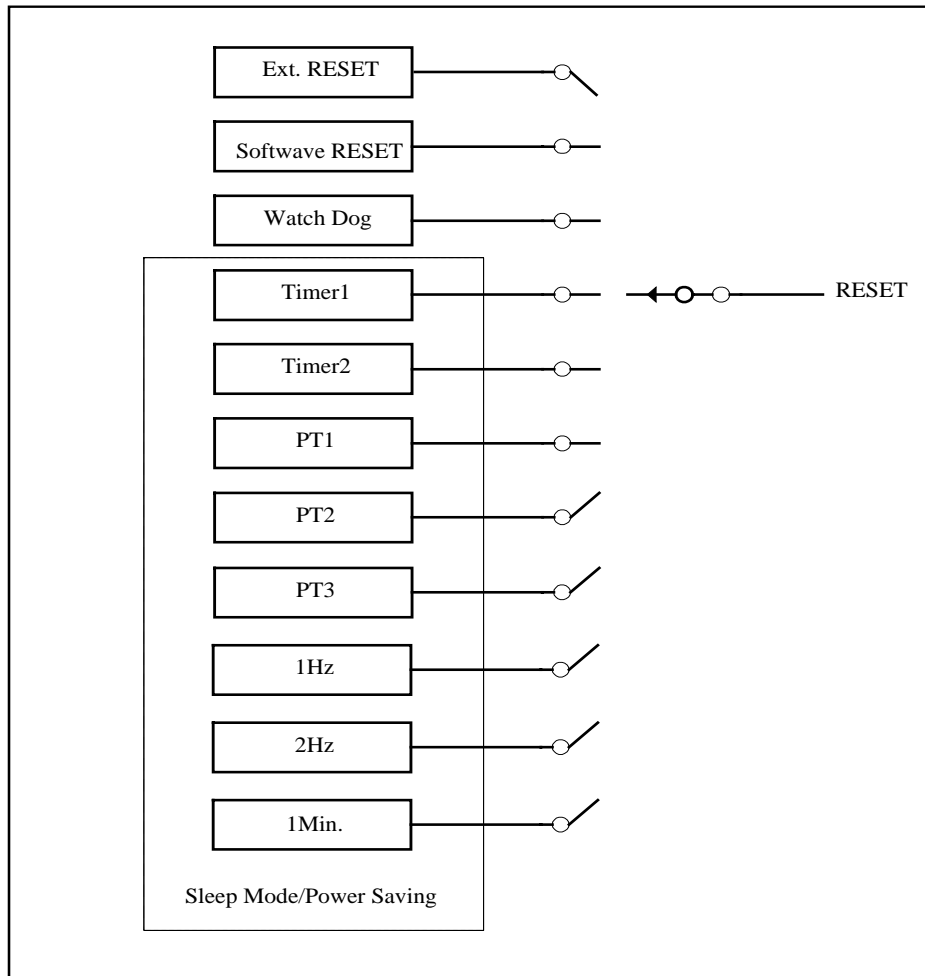


Figure 8-4 RESET Block Diagram

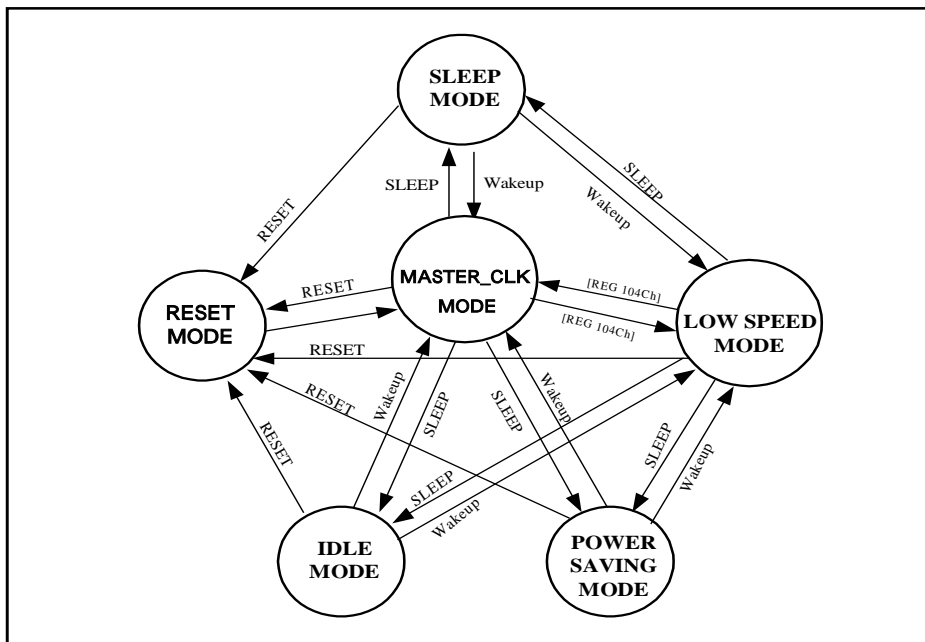


Figure 8-5 CPU Operation Diagram

POWER SAVING MODE	MASTER_CLK NORMAL MODE																												
32786Hz OSC: stopped [REG 104Ch] Bit0 Xtal-Oscillator Off	32786Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On																												
PLL: Stopped [REG 104Ch] Bit1 Disable	PLL: turned on [REG 104Ch] Bit1 System Clock On																												
CPU: sleep mode [REG 104Bh] Bit0 CPU Enter Sleep	CPU: normal mode [REG 104Bh] Bit0 Normal Mode																												
	CPU Clock Select [REG 104Ch] Bit4 ~2																												
	<table border="1"> <thead> <tr> <th>Bit4</th> <th>Bit3</th> <th>Bit2</th> <th>CPU Clock</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>PLL_CLK RUN1 Mode</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>PLL_CLK RUN1 Mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>PLL_CLK RUN1 Mode</td> </tr> </tbody> </table>	Bit4	Bit3	Bit2	CPU Clock	0	0	0	PLL_CLK RUN1 Mode	0	0	1	PLL_CLK RUN1 Mode	0	1	0	PLL_CLK RUN1 Mode												
Bit4	Bit3	Bit2	CPU Clock																										
0	0	0	PLL_CLK RUN1 Mode																										
0	0	1	PLL_CLK RUN1 Mode																										
0	1	0	PLL_CLK RUN1 Mode																										
SLEEP MODE	LOW SPEED MODE																												
32786Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On	32786Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On																												
PLL: turned on [REG 104Ch] Bit1 System Clock On	PLL: turned on [REG 104Ch] Bit1 System Clock On																												
CPU: sleep mode [REG 104Bh] Bit0 CPU Enter Sleep	CPU: normal mode [REG 104Bh] Bit0 Normal Mode																												
	CPU Clock Select [REG 104Ch] Bit4 ~2																												
	<table border="1"> <thead> <tr> <th>Bit4</th> <th>Bit3</th> <th>Bit2</th> <th>CPU Clock</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>PLL_CLK/2 RUN1 Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>PLL_CLK/4 RUN1 Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>PLL_CLK/8 RUN1 Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>32768Hz RUN1 Mode</td> </tr> <tr> <td colspan="4" style="border-top: 1px dashed black;"></td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>32768Hz RUN2 Mode</td> </tr> </tbody> </table>	Bit4	Bit3	Bit2	CPU Clock	1	0	0	PLL_CLK/2 RUN1 Mode	1	0	1	PLL_CLK/4 RUN1 Mode	1	1	0	PLL_CLK/8 RUN1 Mode	1	1	1	32768Hz RUN1 Mode					0	1	1	32768Hz RUN2 Mode
Bit4	Bit3	Bit2	CPU Clock																										
1	0	0	PLL_CLK/2 RUN1 Mode																										
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1	1	0	PLL_CLK/8 RUN1 Mode																										
1	1	1	32768Hz RUN1 Mode																										
0	1	1	32768Hz RUN2 Mode																										
IDLE MODE																													
32786Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On																													
PLL: stopped [REG 104Ch] Bit1 Disable																													
CPU: sleep mode [REG 104Bh] Bit0 CPU Enter Sleep																													

Table 8-1 CPU Operation Mode Setting

Figure 8-5 is the diagram for CPU operation, and Table 8-1 is for CPU Operation Mode Setting. The flow path includes Sleep, Reset, Idle, Power Saving Mode, the flow of CPU Clock between normal and low speed, and setting Register [REG 104Bh, 104Ch]. When CPU Clock is set as low speed, the choice of speed could be made by setting [REG 104Ch] Bit4~2.

8.2.2 Wakeup

Table 8-2 shows the setting of Register [REG 104Bh and 104Ch] when CPU needs to be waking up from the Sleeping, Deep Sleeping, and Power Saving Mode.

Table 8-2 Wakeup Operation Mode

Wakeup & Reset From Sleep and Power Saving Mode	Sleep Mode		Deep-Sleep Mode		RUN1 Mode 32KHz→ON PLL→OFF		RUN1 Mode 32KHz→OFF PLL→OFF		RUN2 Mode 32KHz→OFF PLL→OFF	
	Wakeup	Wakeup & Reset	Wakeup	Wakeup & Reset	Wakeup	Wakeup & Reset	Wakeup	Wakeup & Reset	Wakeup	Wakeup & Reset
PT1 (Rising, Falling)	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PT1 (Level Change)	Yes	Yes	No	No	No	No	No	No	No	No
PT2 (Rising, Falling)	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PT2 (Level Change)	Yes	Yes	No	No	No	No	No	No	No	No
PT3[1:0]~Rising PT3[7:4]~Rising PT3[3:2]~Falling	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
Timer2	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
Timer3	No	No	No	No	No	No	No	No	No	No
UART	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes
1Min.	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
2Hz	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
1Hz	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No
Ext_Break	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note: Yes→ Can Wakeup CPU Clock or Reset
 No→ Can't Wakeup CPU Clock or Reset

8.3 External Flash ROM

RA8911 can support 64K~4MByte external Flash. It can also be connected with two external memories, ranging from 64K~8MByte. Figure 8-6 and 8-7 are the circuits for external Flash ROM. RA8911 can support two Flash ROM at the same time. There are two Command type for Flash. Users can choose a suitable Command type for different brand by setting up [REG 1050h]bit0. [REG 1050~1056h] are the registers for Flash Programming address, Sector address, control indication, and status indication. The steps for Flash Programming and Sector Erase, please refer to the following description.

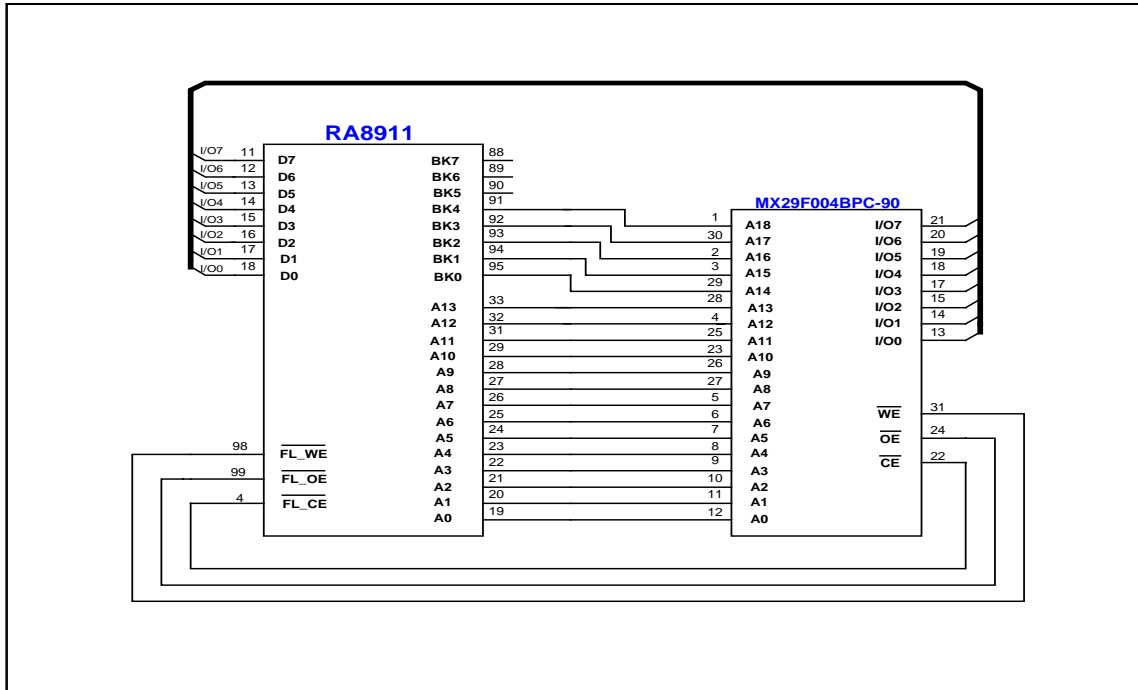
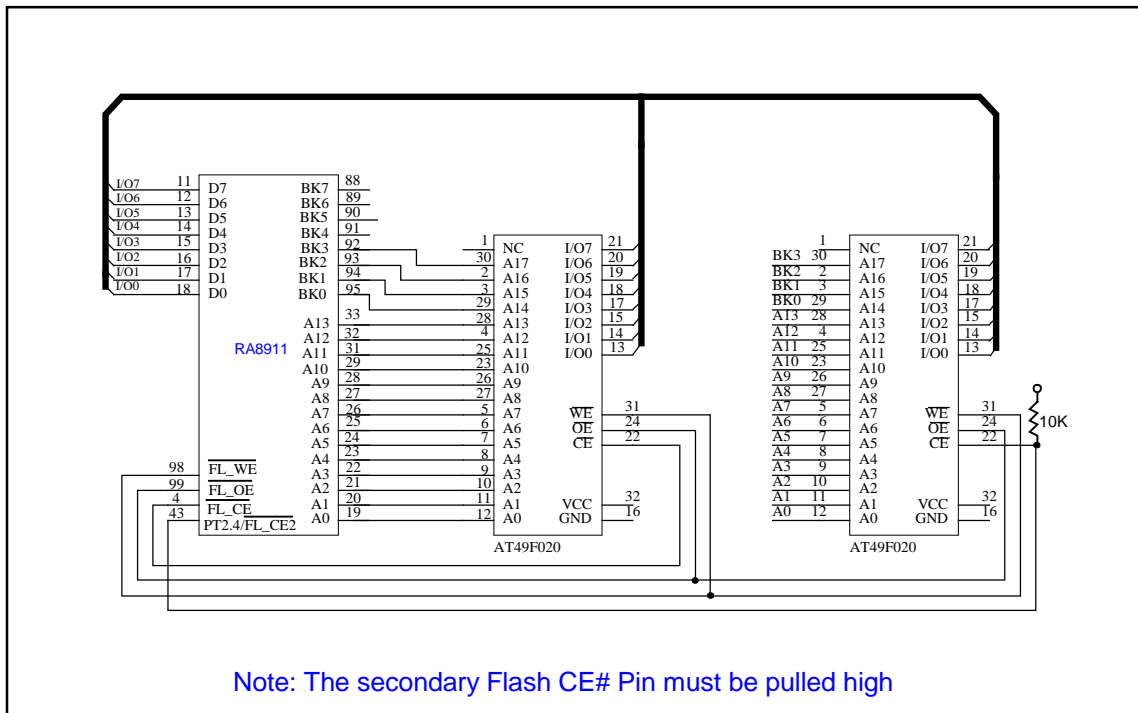


Figure 8-6 External 512K Byte Flash ROM

At the moment, RA8911 mainly supports MXIC Flash ROM series. Besides that, RA8911 provide flexibility for external Flash ROM. Users can use two Flash ROM in the same brand. Figure 8-7 is the circuit for two external 256K-Byte Flash ROM. Which Flash ROM acts depends on [REG 1050h] Bit 2. There are more information below related to relevant Register setting for Flash ROM.



Note: The secondary Flash CE# Pin must be pulled high

Figure 8-7 RA8911 and External 2 X 256KByte Flash ROM

[REG 1050h]: Programming Flash Control Register

Bit	Description	Reset	Default	Access
7-6	Not Used.	--	--	--
5	Erase Status 0: Erase Error 1: Erase Success	0h	0h	R/W
4	Erase Type 0: Chip Erase 1: Sector Erase	0h	0h	R/W
3	Programming Status 0: Programming Error 1: Programming Success	0h	0h	R/W
2	Flash Control 0: Flash Chip1 (FL_CE# active) 1: Flash Chip2 (FL_CE2# active)	0h	0h	R/W
1	One or Two External Flash Option. This bit is used to indicate the external Flash number. This bit is read only. 0: One External Flash 1: Two External Flash	0h	0h	R/W
0	Flash Type 0: Command 1(Reference 8.3.1) 1: Command 2(Reference 8.3.1)	0h	0h	R/W

[REG 1051h]: Programming Flash FBANK Register

Bit	Description	Reset	Default	Access
7-0	Bank Data	0h	0h	R/W

[REG 1052h]: Programming Flash Address High Byte Register

Bit	Description	Reset	Default	Access
7-0	Programming Flash Address --> A[15:8]	0h	0h	R/W

[REG 1053h]: Programming Flash Address Low Byte Register

Bit	Description	Reset	Default	Access
7-0	Programming Flash Address A[7:0]	0h	0h	R/W

[REG 1054h]: Programming Flash Data Register

Bit	Description	Reset	Default	Access
7-0	Programming Data	0h	0h	R/W

[REG 1055h]: Flash Sector Address High Byte Register

Bit	Description	Reset	Default	Access
7-0	Flash Sector High Byte Address	0h	0h	R/W

[REG 1056h]: Flash Sector Address Low Byte Register

Bit	Description	Reset	Default	Access
7-0	Flash Sector Low Byte Address	0h	0h	R/W

8.3.1 Command Definitions

RA8911 supports two different types of Flash Command Definition, Command 1 and Command 2 as below. Please set Register PFCR[1050h]bit 0 as “0” when the Erase command define is in the format of Command 1. If the Erase command define is in the format of Command 2, please set Register PFCR[1050h]bit 0 as “1”.

Command 1

Command		First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Erase	Byte	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Erase	Byte	555H	AAH	AAAH	55H	555H	80H	555H	AAH	AAAH	55H	555H	10H
Erase	Byte	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H

Command 2

Command		First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Erase	Byte	AAAAH	AAH	5555H	55H	AAAAH	80H	AAAAH	AAH	5555H	55H	AAAAH	10H
Erase	Byte	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H

Let’s take MX29LV161T as an example, describing how to proceed Programming and Erase. The definition of Command is as following. Please refer to the Datasheet of MX29LV161 T/B if you need further information.

MX29LV161T/B Command Definitions

Command		First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Program	Byte	AAAH	AAH	555H	55H	AAAH	A0H	PAH	PDH				
Chip Erase	Byte	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
Sector Erase	Byte	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SAH	30H

Note:

1. PA= Address of memory location to be programmed
PD= Data to be programmed at location PA
SA= Address of the sector to be erased
2. The system should generate the following address patterns: 555H or 2AAH to address A10~A0 in word mode /AAAH or 555H to address A10~A-1 in byte mode.

Address bit A11~A19=X=Don't care for all address commands except for Program Address(PA) and Sector Address(SA). Write sequence may be initiated with A11~A19 in either state.

3. For Sector Protect Verify operation: If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

8.3.2 Flash Sector Erase

There is an example telling you how to set Registers for Sector Erase to MX29LV161T.

1. Set [1050h] bit1=0, one external Flash
2. Set Flash Sector Address[1055h, 1056h]. Let's take Sector: SA0 as an example. Please refer to the following description and Table 8-3.

MX29LV161T(x16)											
Sector	Sector Address								Address Range(x16) (in hexadecimal)	Fill Data	
	A19	A18	A17	A16	A15	A14	A13	A12			
SA0	0	0	0	0	0	X	X	X	0000	00-00FFFF	0000h
SA1	0	0	0	0	1	X	X	X	0100	00-01FFFF	0100h
:											
SA21	1	0	1	0	1	X	X	X	1500	00-15FFFF	1500h
:											

▲ Take Sector SA0 as an example. How to access data when Address Rang is 000000-00FFFF?
 ➔ Please choose the start Address "000000h" of SA0 Address Range.
 Then choose the left three numbers of "000000", which is "0000". Then it will become "0000h", and it is the last fill-in data.

▲ Take Sector SA21 as an example. How to access data when Address Rang is 150000-15FFFF?
 ➔ Please choose the start Address "150000h" of SA21 Address Range.
 Then choose the left three numbers of "150000", which is "1500". Then it will become "1500h", and it is the last fill-in data.

For Example: MX29LV800T/B(x8)

Sector	Sector Address							Address Range(x8) (in hexadecimal)	Fill Data
	A18	A17	A16	A15	A14	A13	A12		
SA0	0	0	0	0	0	0	X	00000-03FFF	000h
SA1	0	0	0	1	0	1	0	04000-05FFF	040h
:									
:									

▲ Take Sector SA1 as an example. How to access data when Address Rang is 04000-05FFF?
 ➔ Please choose the start Address “04000h” of SA1 Address Range.
 Then choose the left two numbers of “04000”, which is “040”. Because Flash Sector Address Register has two bytes (16bit), it must fill in “0” because the high nibble of [1055h] is not used. Then it will become “0040h”, and it is the last fill-in data.

3. Set [1050h] bit0 Flash Type is Command 2 format and [1050h] bit4 Erase Type is Sector Erase.
4. Call Erase Subroutine which provided by RAiO, Erase Address is 2084h.
5. Erase Subroutine will set the result at [1050h] bit5 to see whether Erase is successful or not.

Erase Flash Demo Program:

```

LDA    #FFh
STA    PT1_DIR
STZ    PT1

LDA    #00001111b
STA    IO_R
LDA    #00000101b
STA    IO_I

LDA    #00h
STA    FSAHR
LDA    #00h
STA    FSALR
LDA    #00010001b
STA    PFCR                ; Sector Erase

JSR    2084h
MBBS5  PFCR, EraseSuccess
LDA    #01h
STA    PT1
JMP    $

EraseSuccess:

LDA    #55h
STA    PT1
JMP    $
    
```


8.3.3 Flash Programming

There is an example telling you how to set Registers for Programming to MX29LV161T.

1. Choose to set [1050h] bit1, only one external Flash
2. Set [1050h] bit0 Flash Type is Command 2 format, and [1050h] bit4 Erase Type is Chip Erase
3. Set Flash Bank[1051h]; we take Bank 7 as an example
4. Set Programming Flash Address(8000h~BFFFh)
5. Call Programming Flash Subroutine provided by RAiO, Programming Address is 2000h
6. From [1050h] bit3, it can not only help us know whether Programming is successful or not, but also help us judge whether Programming Address is over BFFFh. If Programming Address writes to C000h, then jump to next Bank.

Programming Flash Demo Program:

Programming_Flash:

```
LDA    #FFh
STA    PT1_DIR
STZ    PT1

LDA    #00000001b
STA    PFCR

LDA    #07
STA    PFCR

LDA    #80h
STA    PFAHR
LDA    #00h
STA    PFALR

LDA    #66h
STA    PFDR
```

Programming_Loop:

```
JSR    2000h
MBCR3  PFCR, Programming_Error

INC    PFALR
BNE    Chk_AddrEnd
INC    PFAHR
```

Chk_AddrEnd:

```
LDA    PFALR
CMP    #00h
BNE    Programming_Loop
LDA    PFAHR
CMP    #c0h
BCC    Programming_Loop
```

```
LDA    #55h
STA    PT1

JMP    $
```

Programming_Error:

```
LDA    #aah
STA    PT1

JMP    $
```

Table 8-3: MX29LV161T Sector Architecture

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	000000-00FFFF	00000-07FFF	0	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA15	64Kbytes	32Kwords	0F0000-0FFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA16	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA17	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA18	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA19	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA20	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA21	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA22	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA23	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA24	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA25	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA26	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA27	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA28	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA29	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA30	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-F7FFF	1	1	1	1	0	X	X	X
SA31	32Kbytes	16Kwords	1F0000-1F7FFF	F8000-FBFFF	1	1	1	1	1	0	X	X
SA32	8Kbytes	4Kwords	1F8000-1F9FFF	FC000-ECFFF	1	1	1	1	1	1	0	0
SA33	8Kbytes	4Kwords	1FA000-1FBFFF	FD000-FDFFF	1	1	1	1	1	1	0	1
SA34	16Kbytes	8Kwords	1FC000-1FFFF	FE000-FFFF	1	1	1	1	1	1	1	X

Table 8-4: MX29LV161B Sector Architecture

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	000000-003FFF	00000-01FFF	0	0	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	004000-005FFF	02000-02FFF	0	0	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	006000-007FFF	03000-03FFF	0	0	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	008000-00FFFF	04000-07FFF	0	0	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA11	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA12	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA13	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA14	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA15	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA16	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA17	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA18	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA19	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA20	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA21	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA22	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA23	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA24	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA25	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA26	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA27	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA28	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA29	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA30	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA31	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	0	X	X
SA32	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	1	0	0
SA33	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-FFFFF	1	1	1	1	0	1	0	1
SA34	64Kbytes	32Kwords	1F0000-1FFFFF	F8000-FFFFF	1	1	1	1	1	1	1	X

8.4 I/O Ports

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled. That pin may not be used as a general purpose I/O pin. PORT1, PORT2, PORT3 and PORT4 are 8-bit wide, bi-directional port.

The specialties of RA8911 are I/O resistor control register and I/O driving current control register, which provide the convenience for users to make a choice depend on the application. RA8911 also builds in De-bounce function, and could be set by [REG 102Dh] Bit7~Bit4.

[REG 1020h]: Port 1 Data Register

Bit	Description	Reset	Default	Access
7-2	Bit-[7:2] of Output Data to Port 1 or Input from Port 1	0h	0h	R/W
1	Bit-1 of Output Data to Port 1 or Input from Port 1 This bit is also as the input of TM2 clock source when REG-1015h bit2-0 == '000'	0h	0h	R/W
0	Bit-0 of Output Data to Port 1 or Input from Port 1 This bit is also as the input of TM1 clock source when REG-1012h bit2-0 == '000'	0h	0h	R/W

Note: If the Port1 is output mode then the read access data is from the register 1020h. If the Port1 is input mode the read access is form Port1 I/O.

[REG 1021h]: Port 1 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 1 0: Input Mode 1: Output Mode <i>Note: If PT1[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</i>	0h	0h	R/W

[REG 1022h]: Port1 Interrupt Trigger Indicate Register

Bit	Description	Reset	Default	Access
7-0	Port1 Bit[7:0] <i>Note: After using "Interrupt Indicate", users have to write command cleaning it to "0".</i>	0h	0h	R/W

[REG 1023h]: Port 1 Output Mode Select Register

Bit	Description	Reset	Default	Access
7-0	Select the Output Mode for CMOS or Open-Drain Mode 0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 1 Direction Control Register controls the Port1 output data.	0h	0h	R/W

[REG 1024h]: Port 2 Data Register

Bit	Description	Reset	Default	Access
7	Bit-7 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of PWM1 when PWM enable(REG-101Dh bit4 = '1').	0h	0h	R/W
6	Bit-6 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of PWM2 when PWM enable(REG-101Dh bit4 = '1').	0h	0h	R/W

5	Bit-5 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of REG-101Eh write signal (EXP_WR#) when external REG-101Eh write enabled (REG-101Fh bit0= '1').	0h	0h	R/W
4	Bit-4 of Output Data to Port 2 or Input from Port 2 This bit is also as the secondary external Flash chip select output(FL_CE2#) when using two external flashes.	0h	0h	R/W
3	Bit-3 of Output Data to Port 2 or Input from Port 2 This bit is also as the output of LVD indicated(LVD#) when external LVD enabled(REG-1033h bit2= '1').	0h	0h	R/W
2	Bit-2 of Output Data to Port 2 or Input from Port 2 This bit is also as the external memory write enable(MEM_WE#) when external memory decoder selected(REG-1032h bit0= '1').	0h	0h	R/W
1	Bit-1 of Output Data to Port 2 or Input from Port 2 This bit is also as the external memory output enable (MEM_OE#) when external memory decoder selected(REG-1032h bit0= '1').	0h	0h	R/W
0	Bit-0 of Output Data to Port 2 or Input from Port 2 This bit is also as the external memory chip select output (MEM_CE#) when external memory decoder enabled (REG-1032h bit0= '1'). The external memory is decoded when CPU access from \$4000 to \$7FFF.	0h	0h	R/W

Note: If the Port2 is output mode then the read access date is from the register 1024h. If the Port2 is input mode then the read access is form Port2 I/O.

[REG 1025h]: Port 2 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 2 0: Input Mode 1: Output Mode <i>Note: If PT2[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</i>	0h	0h	R/W

[REG 1026h]: Port2 Interrupt Trigger Indicate Register

Bit	Description	Reset	Default	Access
7-0	Port2 Bit[7:0] <i>Note: After using "Interrupt Indicate", users have to write command cleaning it to "0".</i>	0h	0h	R/W

[REG 1027h]: Port 2 Output Mode Select Register

Bit	Description	Reset	Default	Access
7-0	Select the Output Mode for CMOS or Open-Drain Mode 0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 2 Direction Control Register controls the Port1 output data.	0h	0h	R/W

[REG 1028h]: Port 3 Data Register

Bit	Description	Reset	Default	Access
7-4	Bit-[7:4] of Output Data to Port 3 or Input from Port 3.	0h	0h	R/W
3	Bit-3 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of User UART TX when user UART enable(REG-1038h bit4 == '1').	0h	0h	R/W

2	Bit-2 of Output Data to Port 3 or Input from Port 3. This bit is also as the input of User UART RX when user UART enable(REG-1038h bit4 == '1').	0h	0h	R/W
1	Bit-1 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD chip select(LCD_E) when external LCD enabled(REG-100Dh bit0= '1'). The external LCD is decoded at REG-100Eh & REG-100Fh.	0h	0h	R/W
0	Bit-0 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD R/W(LCD_RW) when external LCD enabled(REG-100Dh bit0= '1').	0h	0h	R/W

Note: If the Port3 is output mode then the read access data is from the register 1028h. If the Port3 is input mode then the read access is form Port3 I/O.

[REG 1029h]: Port 3 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 3 0: Input Mode 1: Output Mode <i>Note: If PT3[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</i>	0h	0h	R/W

[REG 102Ah]: Port3 Interrupt Trigger Indicate Register

Bit	Description	Reset	Default	Access
7-0	Port3 Bit[7:0] Interrupt Indicate <i>Note: After using "Interrupt Indicate", users have to write command cleaning it to "0".</i>	0h	0h	R/W

[REG 102Bh]: I/O Resistor Control Register

Bit	Description	Reset	Default	Access
7	PT4 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
6	PT4 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
5	PT3 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
4	PT3 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
3	PT2 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
2	PT2 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
1	PT1 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W
0	PT1 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm	0h	0h	R/W

[REG 102Ch]: I/O Driving Current Control Register

Bit	Description	Reset	Default	Access
7	PT4 High Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
6	PT4 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
5	PT3 High Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
4	PT3 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
3	PT2 High Nibble Current Select 0: 4mA (12mA for PT2_6, PT2_7) 1: 8mA (36mA for PT2_6, PT2_7)	0h	0h	R/W
2	PT2 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
1	PT1 High Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W
0	PT1 Low Nibble Current Select 0: 4mA 1: 8mA	0h	0h	R/W

[REG 102Dh]: I/O Interrupt Control Register

Bit	Description	Reset	Default	Access
7	PT2 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
6	PT2 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
5	PT1 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
4	PT1 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
3	PT2 High Nibble Interrupt or Wakeup(default) / PT1_3 Bit Interrupt 0: Disable 1: Enable When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit3 could be used as Interrupt. Please refer to the following set-up: 0: Disable 1: Enable	0h	0h	R/W

2	<p>PT2 Low Nibble Interrupt or Wakeup(default) / PT1_2 Bit Interrupt 0:Disable 1: Enable When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit2 could be used as Interrupt. Please refer to the following set-up: 0: Disable 1: Enable</p>	0h	0h	R/W
1	<p>PT1 High Nibble Interrupt or Wakeup(default) / PT1_1 Bit Interrupt 0:Disable 1: Enable When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit1 could be used as Interrupt. Please refer to the following set-up: 0: Disable 1: Enable</p>	0h	0h	R/W
0	<p>PT1 Low Nibble Interrupt or Wakeup(default) / PT1_0 Bit Interrupt 0:Disable 1: Enable When REG[1034h] bit7 set as "1", which is Bit Interrupt Mode, and then PT1 bit0 could be used as Interrupt. Please refer to the following set-up: 0: Disable 1: Enable</p>	0h	0h	R/W

[REG 102Eh]: I/O Interrupt/Wakeup Mode Select Register

Bit	Description	Reset	Default	Access
7-6	<p>PT2 High Nibble Mode Select Bit7 Bit6 Mode ----- 0 0 Rising-Edge Trigger 0 1 Falling-Edge Trigger 1 0 Level Change Trigger (1) 1 1 Level Change Trigger (2)</p> <p>Level Change Trigger (1): (1111) → Setup (1111) → (1111) → (1110) Trigger → (1010) → (0000) → (1111) Return → (1011) Trigger</p> <p>Level Change Trigger (2): (1111) → Setup (1111) → (1111) → (1110) Trigger → (1010) Trigger → (1010) → (1011) Trigger → (1111) Trigger</p>	0h	0h	R/W

5-4	PT2 Low Nibble Mode Select			0h	0h	R/W
	Bit5	Bit4	Mode			

	0	0	Rising-Edge Trigger			
3-2	PT1 High Nibble Mode Select			0h	0h	R/W
	Bit3	Bit2	Mode			

	0	0	Rising-Edge Trigger			
1-0	PT1 Low Nibble Mode Select			0h	0h	R/W
	Bit1	Bit0	Mode			

	0	0	Rising-Edge Trigger			

[REG 102Fh]: I/O Wakeup Reset Control Register

Bit	Description	Reset	Default	Access
7	PT3 High Nibble Interrupt or Wakeup 0: Disable 1: Enable Note: PT3[7:4] are Rising-Edge Trigger.	0h	0h	R/W
6	PT3 Low Nibble Interrupt or Wakeup 0: Disable 1: Enable Note: PT3[1:0] are Rising-Edge Trigger, PT3[3:2] are Falling-Edge Trigger.	0h	0h	R/W
5	PT3 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
4	PT3 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
3	PT2 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
2	PT2 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
1	PT1 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
0	PT1 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W

Example(1): Each set-up while PT1 is in Output Mode.

```
LDA    #11111111b           ; PT1 Output Mode
STA    1021h
LDA    #00000000b           ; PT1 Resistor None
STA    102Bh
LDA    #00000000b           ; PT1 Driving Current = 4mA
STA    102Ch
LDA    #10101010b
STA    1020h
```

Example(2): Each set-up while PT1 is in Output and Input Mode.

```
LDA    #11110000b           ; PT2 Bit7~4 Output, Bit3~0 Input
STA    1025h
LDA    #00000100b           ; PT2 High Nibble Resistor: None
STA    102Bh                 ; PT2 Low Nibble Resistor : Pull Up 5Kohm
LDA    #01000000b           ; PT2 Low Nibble Clock Select: Add Filter to
                             De-bounce, High Nibble Normal.
STA    102Dh
LDA    #11000000b
STA    1024h
```

Example(3): Each set-up while PT1 is used for INT.

```
LDA    #00000000b           ; PT1 Input Mode
STA    1021h
LDA    #00110011b           ; PT1 add filter to de-bounce.
STA    102Dh                 ; PT1 Interrupt or Wakeup Enable
LDA    #00000101b           ; PT1 Falling-Edge Trigger
STA    102Eh                 ;
LDA    #00000001b           ; PT1 INT Enable
STA    1006h
```

Example(4): Each set-up while PT1 is used for Wake-up Reset.

```
LDA    #00000000b           ; PT1 Input Mode
STA    1021h
LDA    #00110011b           ; PT1 add filter to de-bounce.
STA    102Dh                 ; PT1 Interrupt or Wakeup
LDA    #00000101b           ; PT1 Falling-Edge Trigger
STA    102Eh
LDA    #00000011b           ; Setting PT1 Wake-Up&Cause Reset
STA    102Fh
```

8.5 Timer

RA8911 provides three 12-Bit Timer/Counter. They are Timer1, Timer2, and Timer3, composed of two 8-bit Registers (THx, TLx).

The functions of Timer1 and Timer2 are as following:

- ◆ 12 Bits counter auto re-load.
- ◆ Down Counter type
- ◆ Wake up from Sleep Mode
- ◆ Wake up RESET
- ◆ Overflow Interrupt Once or Loop

The functions of Timer3:

- ◆ 12 Bits counter auto re-load.
- ◆ Down Counter type
- ◆ Overflow Interrupt Once or Loop

Figures below are Block Diagrams illustrating operation principles and software control methods.

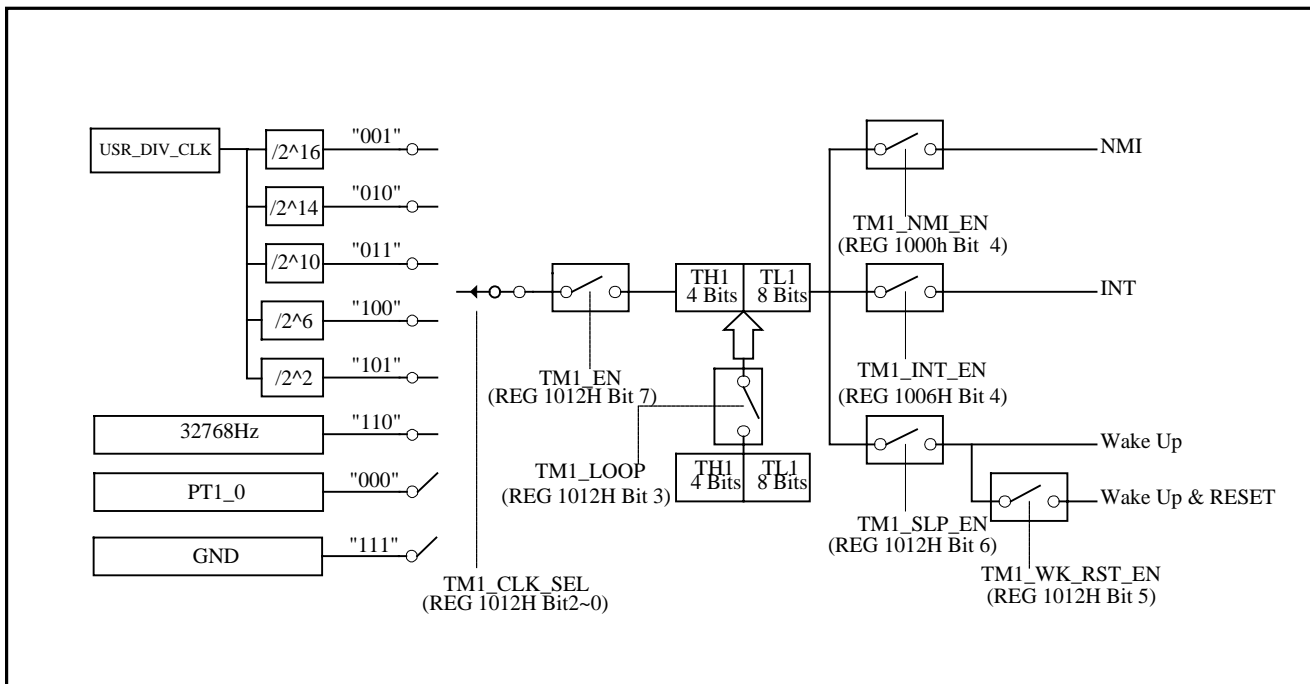


Figure 8-8 Timer1 Block Diagram

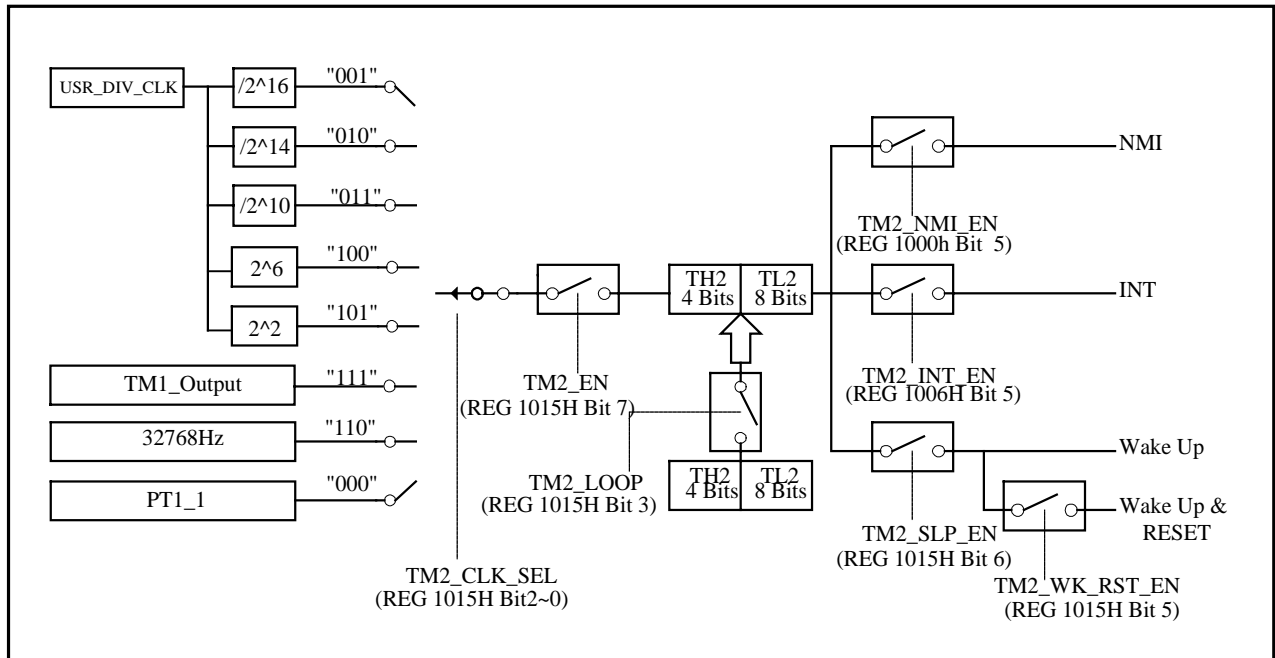


Figure 8-9 Timer2 Block Diagram

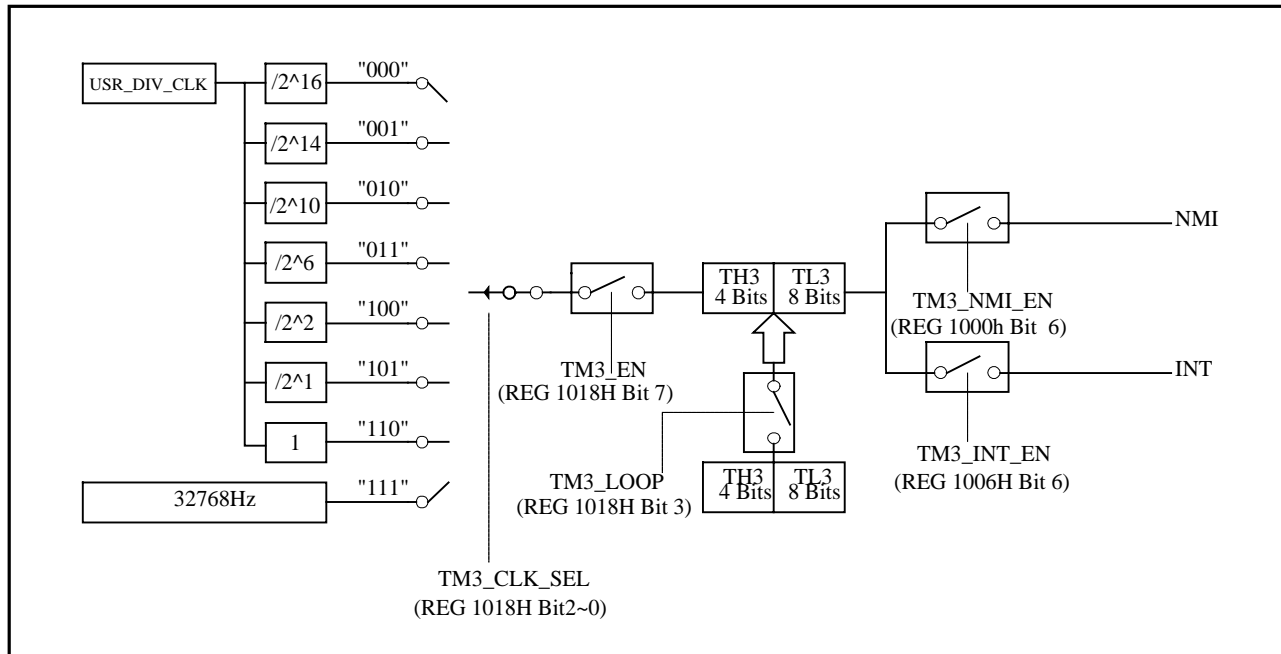


Figure 8-10 Timer3 Block Diagram

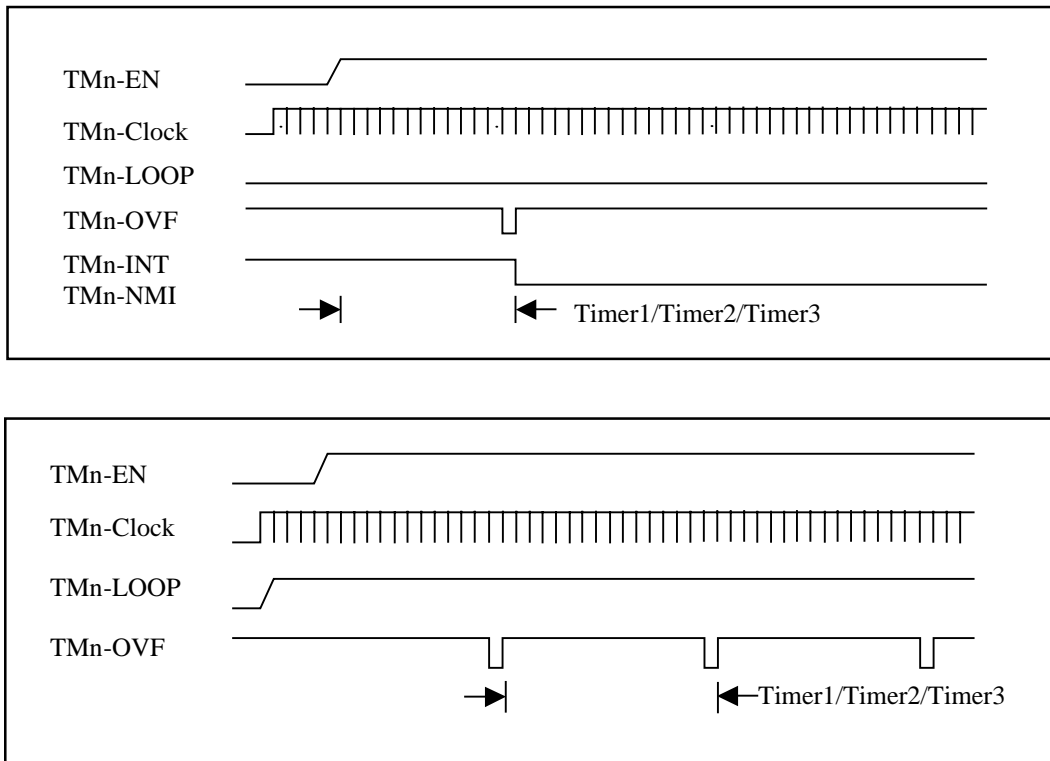


Figure 8-11 Timer Operation mode

[REG 1010h]: Timer 1 Count_H Register

Bit	Description	Reset	Default	Access
3-0	Timer 1 Down Count Data – High Byte	Xh	Xh	R/W

[REG 1011h]: Timer 1 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 1 Down Count Data – Low Byte	Xh	Xh	R/W

[REG 1012h]: Timer 1 Control Register

Bit	Description	Reset	Default	Access
7	Timer 1 Enable or Timer 1 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 1 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 1 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
3	Timer 1 Loop Control 0: Disable 1: Enable	0h	0h	R/W

Timer 1 Input Clock Source Select		Bit2	Bit1	Bit0	Clock Source	Reset	Default	Access
Bit	Description							
2-0		0	0	0	External I/O Port (PT1_0)	0h	0h	R/W
		0	0	1	USR_DIV_CLK /2 ¹⁶			
		0	1	0	USR_DIV_CLK /2 ¹⁴			
		0	1	1	USR_DIV_CLK /2 ¹⁰			
		1	0	0	USR_DIV_CLK /2 ⁶			
		1	0	1	USR_DIV_CLK /2 ²			
		1	1	0	32768Hz			
	1	1	1	GND				

[REG 1013h]: Timer 2 Count_H Register

Bit	Description	Reset	Default	Access
3-0	Timer 2 Down Count Data – High Byte	Xh	Xh	R/W

[REG 1014h]: Timer 2 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 2 Down Count Data – Low Byte	Xh	Xh	R/W

[REG 1015h]: Timer 2 Control Register

Bit	Description	Reset	Default	Access
7	Timer 2 Enable or Timer 2 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 2 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
3	Timer 2 Loop Control 0: Disable 1: Enable	0h	0h	R/W
Timer 2 Input Clock Source Select		0h	0h	R/W
2-0	Bit2 Bit1 Bit0 Clock Source			
	0 0 0 External I/O Port (PT1_1)			
	0 0 1 USR_DIV_CLK /2 ¹⁶			
	0 1 0 USR_DIV_CLK /2 ¹⁴			
	0 1 1 USR_DIV_CLK /2 ¹⁰			
	1 0 0 USR_DIV_CLK /2 ⁶			
	1 0 1 USR_DIV_CLK /2 ²			
1 1 0 32768Hz				
1 1 1 TIMER 1 Output				

[REG 1016h]: Timer 3 Count_H Register

Bit	Description	Reset	Default	Access
3-0	Timer 3 Down Count Data – High Byte	Xh	Xh	R/W

[REG 1017h]: Timer 3 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 3 Down Count Data – Low Byte	Xh	Xh	R/W

[REG 1018h]: Timer 3 Control Register

Bit	Description	Reset	Default	Access
7	Timer 3 Enable or Timer 3 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
3	Timer 3 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 3 Input Clock Source Select	0h	0h	R/W
	Bit2 Bit1 Bit0 Clock Source			

	0 0 0 USR_DIV_CLK/2 ¹⁶			
	0 0 1 USR_DIV_CLK /2 ¹⁴			
	0 1 0 USR_DIV_CLK /2 ¹⁰			
	0 1 1 USR_DIV_CLK /2 ⁶			
	1 0 0 USR_DIV_CLK /2 ²			
1 0 1 USR_DIV_CLK /2 ¹				
1 1 0 USR_DIV_CLK				
1 1 1 32768Hz				

There is an example to clarify how to use Timer:

Example: Use Timer1 to produce interruption every 8KHz.

1/8KHz=125μs, USR_DIV_CLK=7.3728MHz, Timer1 Clock=USR_DIV_CLK/4=7.3728MHz/4
 TH1=00h, TL1=125μs ÷ (1 ÷ (7.3728MHz ÷ 4)) =230, TL1=E6h

```

CLI                                     ; Enable all Interrupt

LDA    #10000000b                       ; USR_DIV_CLK=PLL Clock=7.3728MHz
STA    104Ch

LDA    #00010000b                       ; Timer1 INT Enable
STA    1006h

LDA    #00h
STA    1010h
LDA    #e6h
STA    1011h

LDA    #10001101b                       ;Timer1 start, Loop Enable, Clock=USR_DIV_CLK/4
STA    1012h
    
```

8.6 Watch Dog

The counting period of Watch Dog timer is 2 second. Watch Dog will automatically RESET when it counts up to 2 second preventing the crash happens within the IC. If users need this function, then users need to clear Watch Dog with in 2 second. The Watch Dog could be used as general Timer, and has the function of NMI Interrupt. Figure 8-12 is the Block Diagram of the Watch Dog.

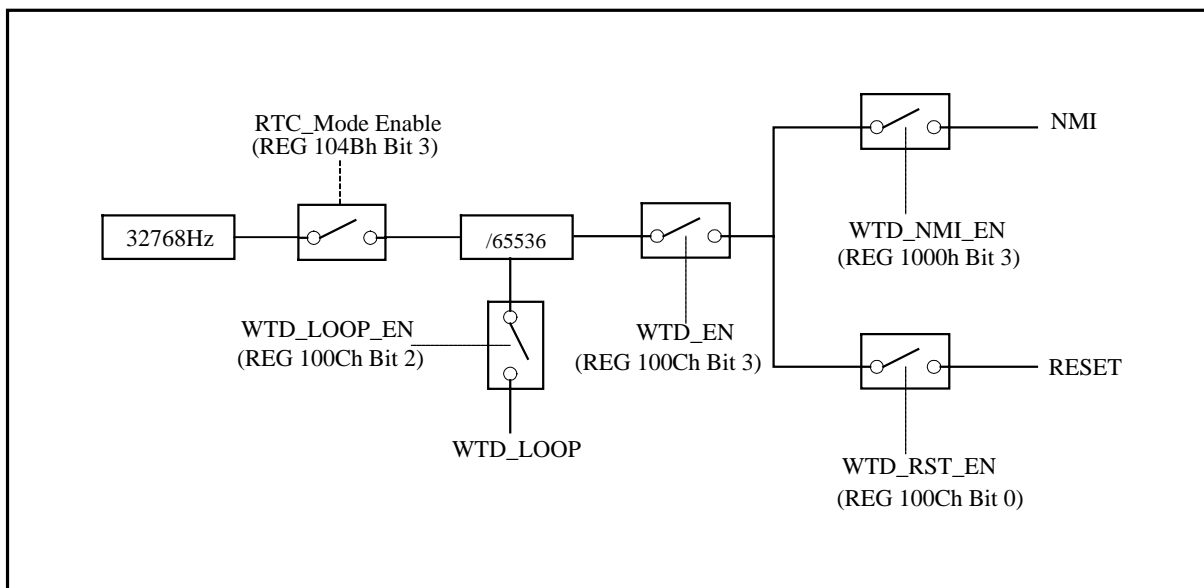


Figure 8-12 Watch Dog Block Diagram

[REG 104Bh]: Power Control Register

Bit	Description	Reset	Default	Access
3	Extra Sleep Mode(Only at RTC Mode) 0: Normal Sleep 1: Extra Deep Sleep In this mode, the Divisor is off and only 32768Hz X'tal, Low speed Timer circuit are active. But the Wakeup with Reset function is inhibited. This bit must used to go with bit-1 and bit-0. Only available when REG[104Bh] Bit[1:0] = 11b.	0h	0h	R/W

[REG 104Ch]: Clock Control Register

Bit	Description	Reset	Default	Access
7-6	PLL Frequency Select Bit7 Bit6 PLL Clock UART Clock ----- 0 0 1.47MHz 368.64KHz 0 1 2.46 MHz 614.4KHz 1 0 7.37 MHz 1.8432MHz 1 1 22.1 MHz 1.8432MHz	0h	0h	R/W
5	User's Divisor Clock Select (USR_DIV_CKSEL) 0: PLL Clock 1: 32768Hz	0h	0h	R/W

4-2	CPU Clock Select			CPU Clock	RUN1 Mode	000h	000h	R/W		
	Bit4	Bit3	Bit2							
	0	0	0						PLL_CLK	RUN1 Mode
	0	0	1						PLL_CLK	RUN1 Mode
	0	1	0						PLL_CLK	RUN1 Mode
	1	0	0						PLL_CLK /2	RUN1 Mode
	1	0	1						PLL_CLK /4	RUN1 Mode
	1	1	0						PLL_CLK /8	RUN1 Mode
1	1	1	32768Hz	RUN1 Mode						

	0	1	1	32768Hz	RUN2 Mode					
In RUN2 mode, the UART, IrDA and PWM are not available.										
1	PLL Clock On/Off Control 0: PLL Clock On 1: PLL Clock Off				0h	0h	R/W			
0	X'tal-Oscillator (32768Hz) On/Off Control 0: X'tal-Oscillator (32768Hz) On 1: X'tal-Oscillator (32768Hz) Off				0h	0h	R/W			

[REG 100Ch]: Watch Dog Control Register

Bit	Description	Reset	Default	Access
3	Watch Dog Enable 0:Disable 1: Enable	0h	0h	R/W
2	Watch Dog Loop Control 0:Disable 1: Enable	0h	0h	R/W
1	Watch Dog Timer Clear 0: Disable 1: Reset Watch Dog Timer, Write this bit high will cause Watch Dog Timer Reset. This bit will be clear automatically after clear.	0h	0h	R/W
0	Watch Dog Reset Enable 0: Disable 1: Enable	0h	0h	R/W

Example:

```

LDA    #00111110b           ; USR_DIV_CLK=32768Hz
STA    104Ch

LDA    #00001001b          ; Watch Dog Enable, Reset Enable
STA    100Ch

LDA    100Ch                ; Watch Dog Disable
AND    #11110111bh
STA    100Ch
    
```

8.7 Interrupt

RA8911 provides 10 Non Mask Interrupt (NMI) and 14 INT. Figure 8-13 is NMI Block Diagram, and Figure

8-14 is INT Block Diagram. Below is relevant Register [REG 1000h~100Bh, 1022h, 1026h, 102A] of Interrupt.

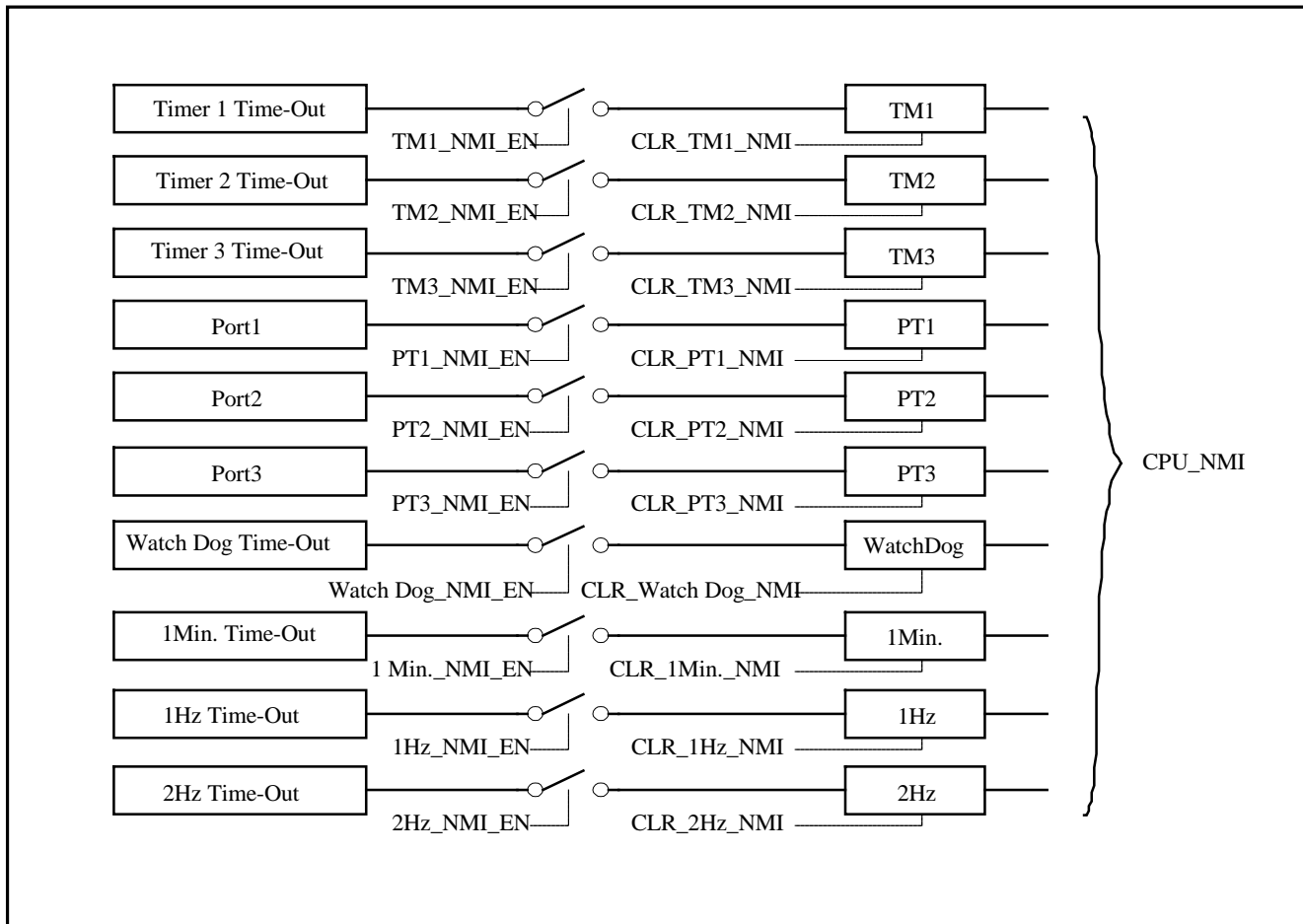


Figure 8-13 NMI Block Diagram

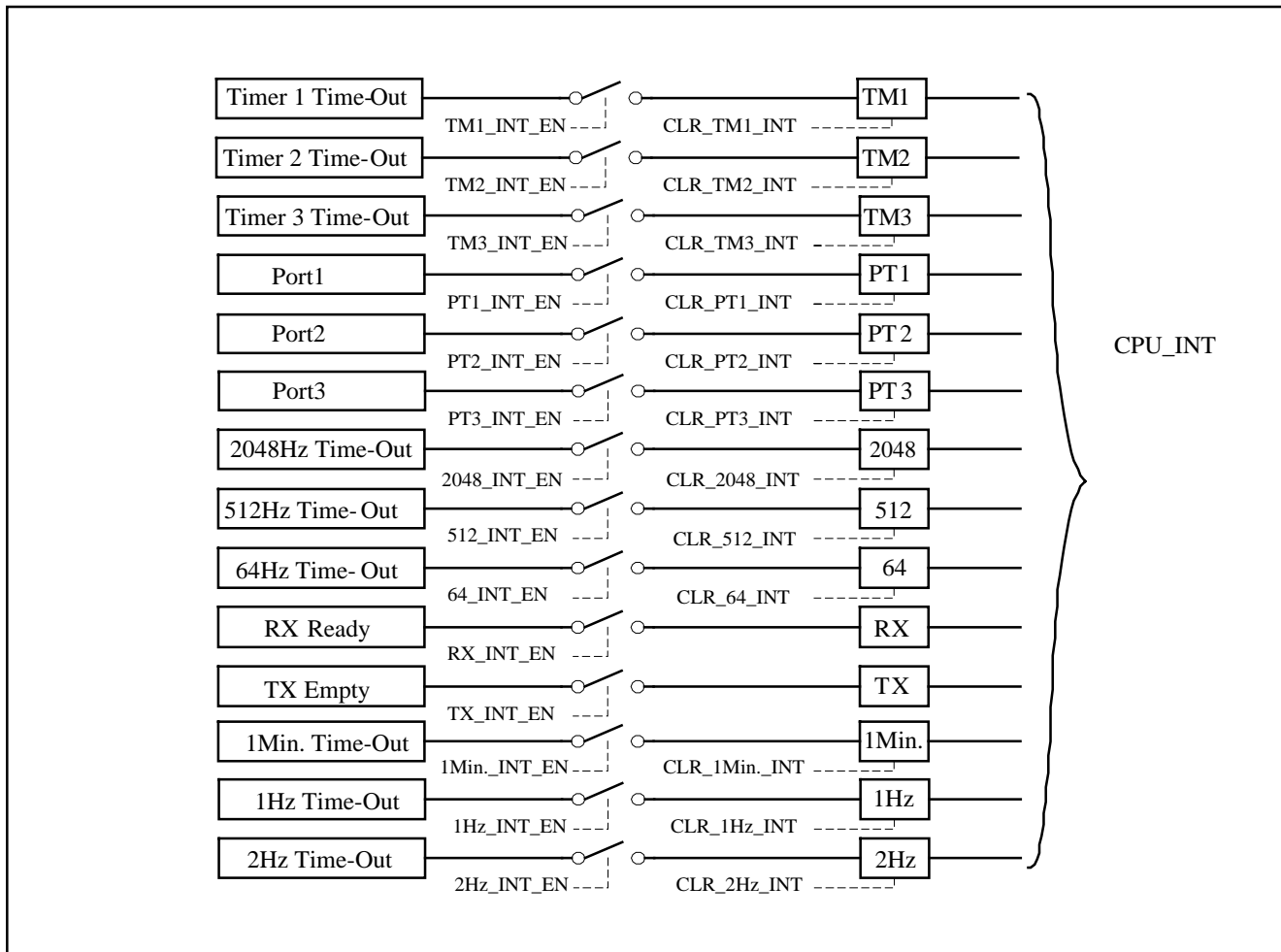


Figure 8-14 INT Block Diagram

[REG 1000h]: NMI Mask Register (1)

Bit	Description	Reset	Default	Access
6	Timer 3 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
4	Timer 1 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
3	Watch Dog NMI Enable 0: Disable 1: Enable	0h	0h	R/W
2	Port 3 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
1	Port 2 NMI Enable 0: Disable 1: Enable	0h	0h	R/W

0	Port 1 NMI Enable 0:Disable 1: Enable	0h	0h	R/W
---	---	----	----	-----

[REG 1001h]: NMI Mask Register (2)

Bit	Description	Reset	Default	Access
2	1Min. NMI Enable 0:Disable 1: Enable	0h	0h	R/W
1	1HZ NMI Enable 0:Disable 1: Enable	0h	0h	R/W
0	2HZ NMI Enable 0:Disable 1: Enable	0h	0h	R/W

[REG 1002h]: NMI Status Register (1)

Bit	Description	Reset	Default	Access
6	Timer 3 NMI Indicate	0h	0h	R/W
5	Timer 2 NMI Indicate	0h	0h	R/W
4	Timer 1 NMI Indicate	0h	0h	R/W
3	Watch Dog NMI Indicate	0h	0h	R/W
2	Port 3 NMI Indicate	0h	0h	R/W
1	Port 2 NMI Indicate	0h	0h	R/W
0	Port 1 NMI Indicate	0h	0h	R/W

[REG 1003h]: NMI Status Register (2)

Bit	Description	Reset	Default	Access
2	1Min. NMI Indicate	0h	0h	R/W
1	1HZ NMI Indicate	0h	0h	R/W
0	2HZ NMI Indicate	0h	0h	R/W

[REG 1004h]: Clear NMI Status Register (1)

Bit	Description	Reset	Default	Access
6	Clear Timer 3 NMI Indicate 1: Clear	--	--	W
5	Clear Timer 2 NMI Indicate 1: Clear	--	--	W
4	Clear Timer 1 NMI Indicate 1: Clear	--	--	W
3	Clear Watch Dog NMI Indicate 1: Clear	--	--	W
2	Clear Port 3 NMI Indicate 1: Clear	--	--	W
1	Clear Port 2 NMI Indicate 1: Clear	--	--	W
0	Clear Port 1 NMI Indicate 1: Clear	--	--	W

[REG 1005h]: Clear NMI Status Register (2)

Bit	Description	Reset	Default	Access
2	Clear 1Min. NMI Indicate 1: Clear	--	--	W

1	Clear 1HZ NMI Indicate 1: Clear	--	--	W
0	Clear 2HZ NMI Indicate 1: Clear	--	--	W

[REG 1006h]: INT Mask Register (1)

Bit	Description	Reset	Default	Access
6	Timer 3 INT Enable 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 INT Enable 0: Disable 1: Enable	0h	0h	R/W
4	Timer 1 INT Enable 0: Disable 1: Enable	0h	0h	R/W
2	Port 3 INT Enable 0: Disable 1: Enable	0h	0h	R/W
1	Port 2 INT Enable 0: Disable 1: Enable	0h	0h	R/W
0	Port 1 INT Enable 0: Disable 1: Enable	0h	0h	R/W

[REG 1007h]: INT Mask Register (2)

Bit	Description	Reset	Default	Access
6	2048HZ Time Base INT Enable	0h	0h	R/W
5	512HZ Time Base INT Enable	0h	0h	R/W
4	64HZ Time Base INT Enable	0h	0h	R/W
2	1Min. INT Enable 0:Disable 1: Enable	0h	0h	R/W
1	1HZ INT Enable 0:Disable 1: Enable	0h	0h	R/W
0	2HZ INT Enable 0:Disable 1: Enable	0h	0h	R/W

[REG 1008h]: INT Status Register (1)

Bit	Description	Reset	Default	Access
6	Timer 3 INT Indicate	0h	0h	R/W
5	Timer 2 INT Indicate	0h	0h	R/W
4	Timer 1 INT Indicate	0h	0h	R/W
2	Port 3 INT Indicate	0h	0h	R/W
1	Port 2 INT Indicate	0h	0h	R/W
0	Port 1 INT Indicate	0h	0h	R/W

[REG 1009h]: INT Status Register (2)

Bit	Description	Reset	Default	Access
6	2048HZ Time Base INT Indicate	0h	0h	R/W

5	512HZ Time Base INT Indicate	0h	0h	R/W
4	64HZ Time Base INT Indicate	0h	0h	R/W
2	1Min. INT Indicate	0h	0h	R/W
1	1HZ INT Indicate	0h	0h	R/W
0	2HZ INT Indicate	0h	0h	R/W

[REG 100Ah]: Clear INT Status Register (1)

Bit	Description	Reset	Default	Access
6	Clear Timer 3 INT Indicate 1: Clear	--	--	W
5	Clear Timer 2 INT Indicate 1: Clear	--	--	W
4	Clear Timer 1 INT Indicate 1: Clear	--	--	W
2	Clear Port 3 INT Indicate 1: Clear	--	--	W
1	Clear Port 2 INT Indicate 1: Clear	--	--	W
0	Clear Port 1 INT Indicate 1: Clear	--	--	W

[REG 100Bh]: Clear INT Status Register (2)

Bit	Description	Reset	Default	Access
6	Clear 2048HZ Time Base INT Indicate	--	--	W
5	Clear 512HZ Time Base INT Indicate	--	--	W
4	Clear 64HZ Time Base INT Indicate	--	--	W
2	Clear 1Min. INT Indicate 1: Clear	--	--	W
1	Clear 1HZ INT Indicate 1: Clear	--	--	W
0	Clear 2HZ INT Indicate 1: Clear	--	--	W

[REG 1038h]: User UART Control Register

Bit	Description	Reset	Default	Access
7	Transmit Empty Indicate INT Enable 0:Disable 1: Enable	0h	0h	R/W
6	Received Data Available Indicate INT Enable 0:Disable 1: Enable	0h	0h	R/W

[REG 102Eh]: I/O Interrupt/Wakeup Mode Select Register

Bit	Description	Reset	Default	Access
-----	-------------	-------	---------	--------

7-6	PT2 High Nibble Mode Select			0h	0h	R/W
	Bit7	Bit6	Mode			

	0	0	Rising-Edge Trigger			
	0	1	Falling-Edge Trigger			
1	0	Level Change Trigger (1)				
1	1	Level Change Trigger (2)				
Level Change Trigger (1):						
(1111) → Setup						
(1111) → (1111) → (1110) Trigger → (1010) → (0000) →						
(1111) Return → (1011) Trigger						
Level Change Trigger (2):						
(1111) → Setup						
(1111) → (1111) → (1110) Trigger → (1010) Trigger →						
(1010) → (1011) Trigger → (1111) Trigger						
5-4	PT2 Low Nibble Mode Select			0h	0h	R/W
	Bit5	Bit4	Mode			

	0	0	Rising-Edge Trigger			
	0	1	Falling-Edge Trigger			
1	0	Level Change Trigger (1)				
1	1	Level Change Trigger (2)				
3-2	PT1 High Nibble Mode Select			0h	0h	R/W
	Bit3	Bit2	Mode			

	0	0	Rising-Edge Trigger			
	0	1	Falling-Edge Trigger			
1	0	Level Change Trigger (1)				
1	1	Level Change Trigger (2)				
1-0	PT1 Low Nibble Mode Select			0h	0h	R/W
	Bit1	Bit0	Mode			

	0	0	Rising-Edge Trigger			
	0	1	Falling-Edge Trigger			
1	0	Level Change Trigger (1)				
1	1	Level Change Trigger (2)				

8.8 Universal Synchronous Asynchronous Receiver Transmitter (UART)

RA8911 builds in one set UART. [REG 1035h] which includes Receive and Transmit can do read and write. Figure 8-15 is Baud Rate Clock Block Diagram. The transmission format of UART is as Figure 8-16. Besides that, UART provides three types of transmission models, such as Normal, ASK IR, IrDA IR. When CPU is during Sleep Mode, UART could be a source for Wake Up. The relevant Register [REG 1037h~1039h] for UART is as below.

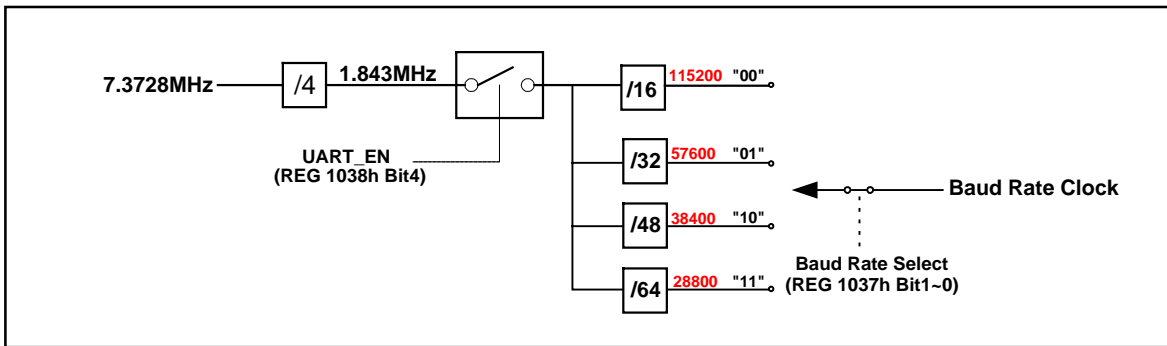


Figure 8-15 Baud Rate Clock Block Diagram

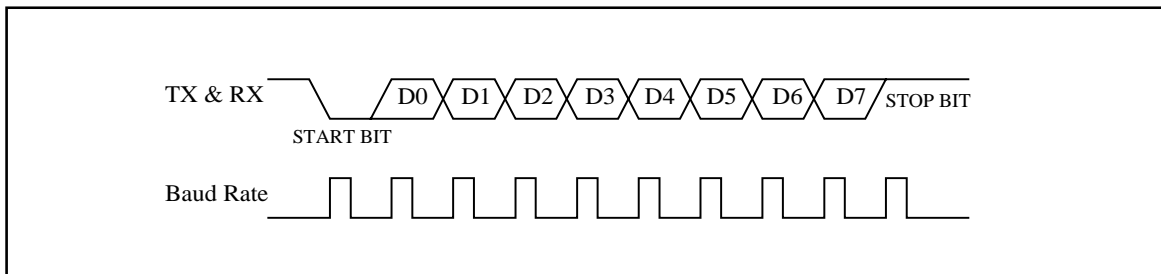


Figure 8-16 RX & TX Data Format

[REG 1035h]: User UART Receive Register (Read Only)

Bit	Description	Reset	Default	Access
7-0	UART Receive Data	Xh	Xh	R

[REG 1035h]: User UART Transmit Register (Write Only)

Bit	Description	Reset	Default	Access
7-0	UART Transmit Data	0h	0h	W

[REG 1036h]: IR Mode Select

Bit	Description	Reset	Default	Access
1-0	UART IR Mode Select Bit1 Bit0 Mode	0h	0h	R/W
	0 0 Normal			
	0 1 ASK IR			
	1 0 IrDA IR			
1 1 IrDA IR				

[REG 1037h]: User UART Baud Rate Select

Bit	Description	Reset	Default	Access
1-0	UART Baud Rate Bit1 Bit0 Baud Rate	01h	01h	W
	0 0 115200bps			
	0 1 57600bps			
	1 0 38400bps			
1 1 28800bps				

[REG 1038h]: User UART Control Register

Bit	Description	Reset	Default	Access
7	Transmit Empty Indicate INT Enable 0:Disable 1: Enable	0h	0h	R/W
6	Received Data Available Indicate INT Enable 0:Disable 1: Enable	0h	0h	R/W
4	User UART Enable Control 0: Disable, 1.843MHz Clock Stop 1: Enable If set high, then the Port3 bit[3:2] are defined as Transmit and Receive interface signals. PT3_3 → TX PT3_2 → RX	0h	0h	R/W
3	UART Transmitter Inverter	0h	0h	R/W
2	UART Receiver Inverter	0h	0h	R/W
1	UART RX Wake Up Mode Select 0: UART Wake Up only 1: UART Wake Up & caused Reset	0h	0h	R/W
0	UART RX Wake Up 0: Disable 1: Enable	0h	0h	R/W

[REG 1039h]: User UART Status Register

Bit	Description	Reset	Default	Access
7	Transmit Register Empty Indicate This bit is set when transmit complete and be clear when write a data to UART Transmit Register(REG-1035h).	0h	0h	R/W
6	Received Data Available Indicate This bit is set when UART received an available data but it will not be clear when the host read the data from UART Receive Register (REG-1035h).	0h	0h	R/W

Example:

```

LDA    #00h                ; UART IR Mode→ Normal
STA    1036h

LDA    #00h                ; Baud Rate=115200 bps
STA    1037h

LDA    #00100000b          ; UART Enable
STA    1038h

LDA    #55h
STA    1035h                ; Transmit 55h
LDA    1035h                ; Receive
    
```

8.9 IrDA Interface

An IrDA interface, compatible with SIR(Serial Infrared) level IrDA, is built in RA8911. The IrDA encoder and decoder module is built on the fundamental of UART module. RA8911 and external IrDA module, connecting via RX(receiver, pin37) and TX(transmitter Pin38), complete the implementation of IrDA

physical layer.

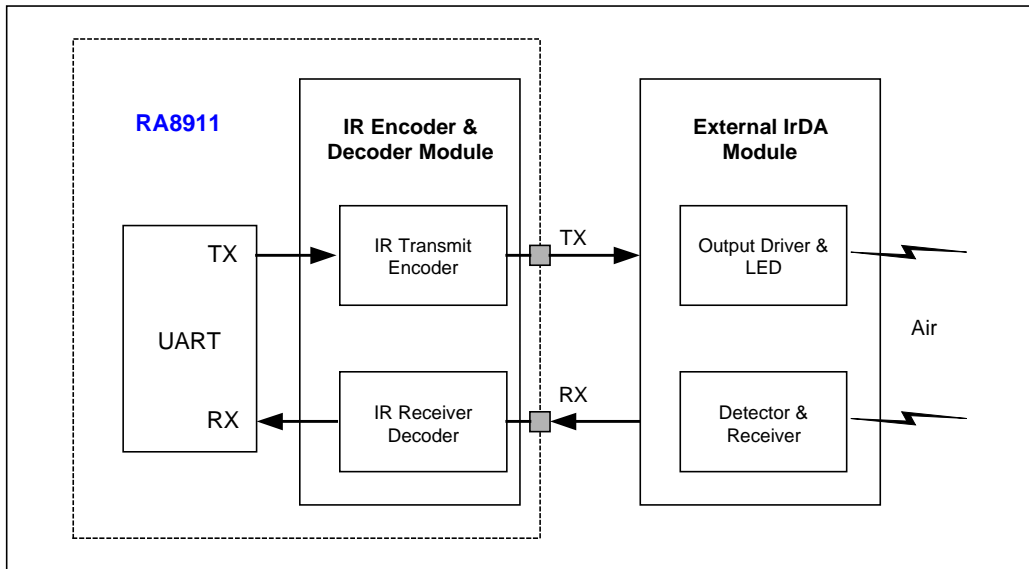


Figure 8-17 RA8911 with IrDA module

8.10 Digital-to-Analog Converter (D/A) Module

RA8911 Support one 4 level 10-bit fixed current types Digital-to-Analog Converter (D/A) Module. RA8911 current output IOOUT is divided to two types and three current levels: Audio Mode (0~2mA, 0~2.5mA, and 0~3mA) and DTMF Mode (0~200uA, 0~200uA, and 0~200uA), which could be set by [REG 101Bh]. The maximum output current is 3mA as well as the data is "FF". If the data is "00" then the output current is zero. Figure 8-18 and 8-19 are DAC application circuit.

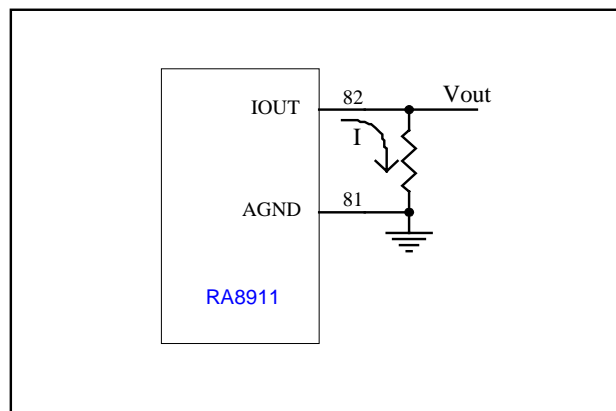


Figure 8-18 DAC Application

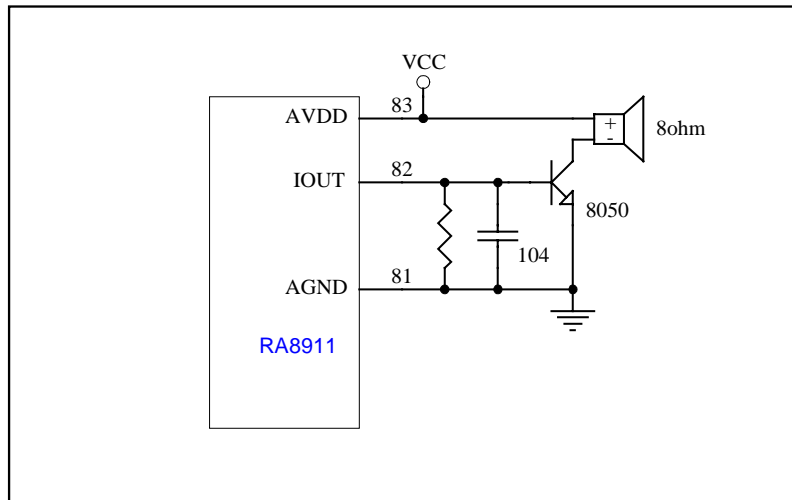
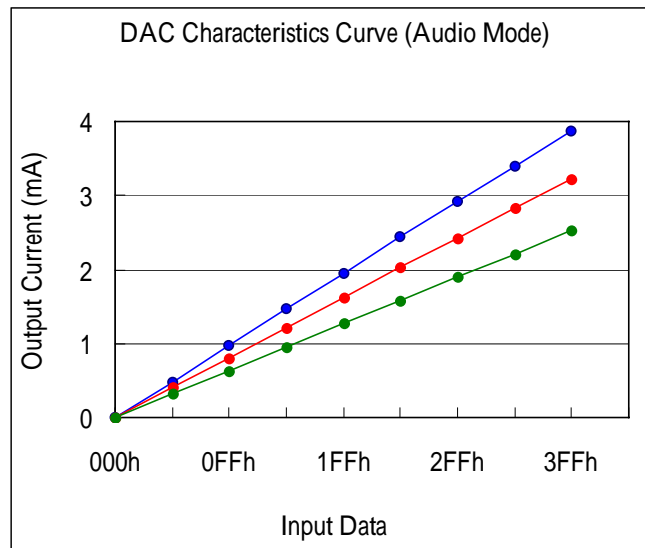
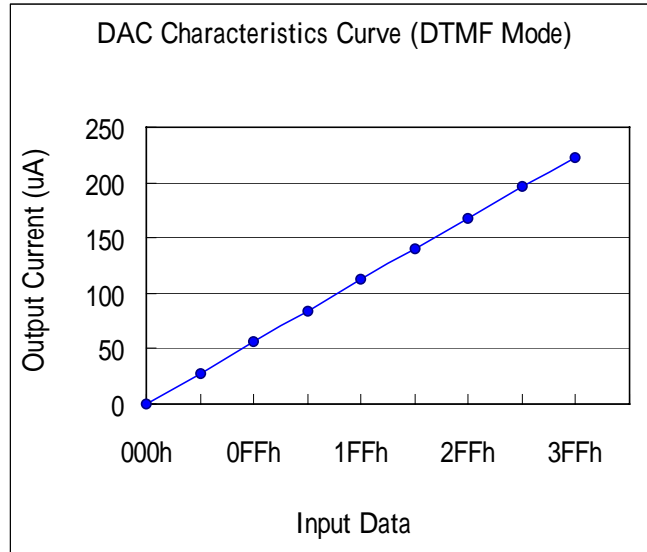


Figure 8-19 Speech Application

DAC divides into two modes: Audio and DTMF Mode. The following table is the max. Resistance value without distortion when generate triangle wave.

Current \ Mode	Audio Mode	DTMF Mode
0~200μA		13.8KΩ
0~2mA	1.1K	
0~2.5mA	850Ω	
0~3mA	610Ω	





8.11 LCD Interface

RA8911 supports a LCD Interface, including two LCD Registers, which are LCD Command register [REG 100Eh] and LCD Data register [REG 100Fh]. The external control signal saves the effort of some simulation actions. Figure 8-20 shows the interface of RA8911 and LCD/LCM. The relevant Register [REG 100Dh, 100Eh, 100Fh] for LCD Interface is one the following page. There is an example to illustrate how to control LCD.

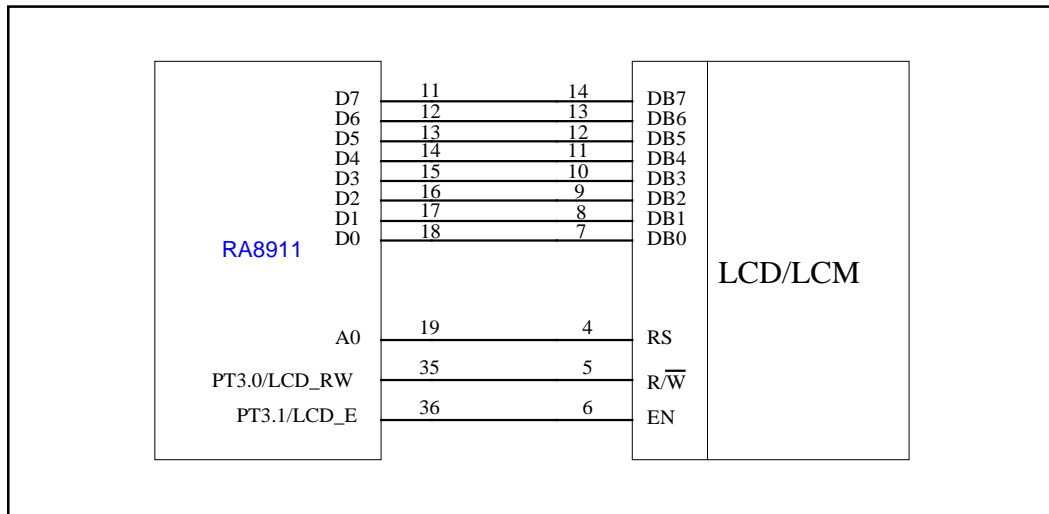


Figure 8-20 RA8911 and LCD/LCM Interface

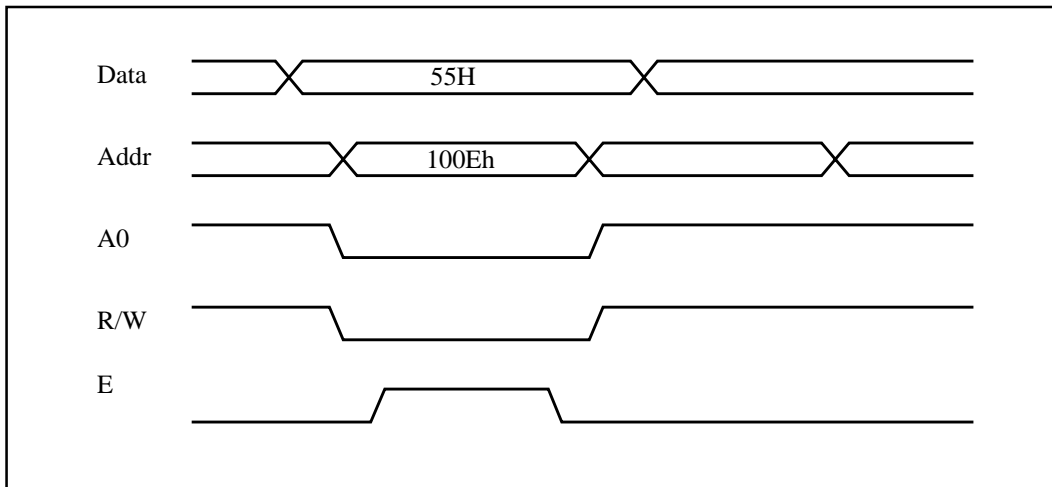


Figure 8-21 Command Write Timing

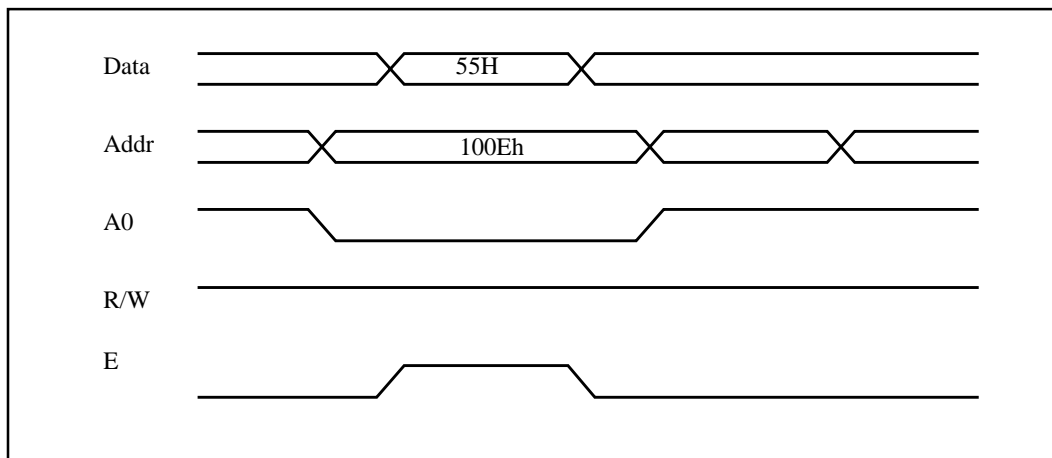


Figure 8-22 Command Read Timing

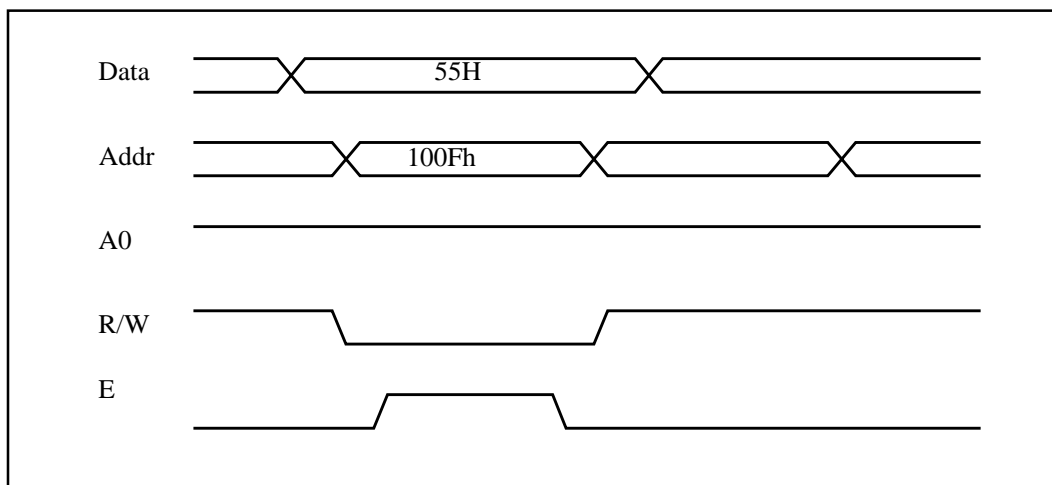


Figure 8-23 Data Write Timing

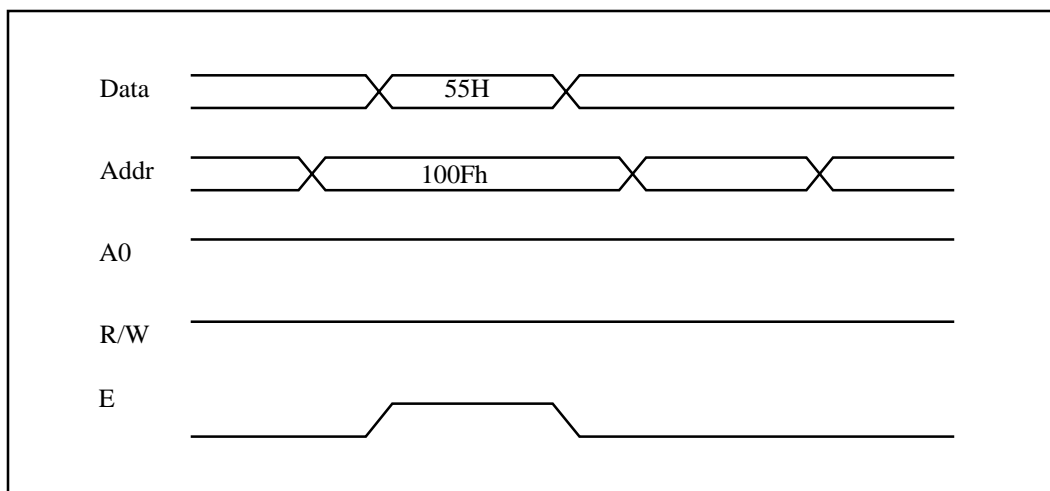


Figure 8-24 Data Read Timing

[REG 100Dh]: LCD Control Register

Bit	Description	Reset	Default	Access																									
2-1	<p>Hi-Speed Control for External LCD Decoder These two bits are use to add delay clock for LCD access time.</p> <table border="1"> <thead> <tr> <th>Bit2</th> <th>Bit1</th> <th>T1</th> <th>T2</th> <th>T3 (Unit: CPU Clock)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4.5</td> <td>11</td> <td>0.5</td> </tr> <tr> <td>0</td> <td>1</td> <td>3.5</td> <td>9</td> <td>0.5</td> </tr> <tr> <td>1</td> <td>0</td> <td>2.5</td> <td>6</td> <td>0.5</td> </tr> <tr> <td>1</td> <td>1</td> <td>1.5</td> <td>3</td> <td>0.5</td> </tr> </tbody> </table> <p>T1: Data Set-Up Time T2: Data Access Time T3: Data Hold Time</p>	Bit2	Bit1	T1	T2	T3 (Unit: CPU Clock)	0	0	4.5	11	0.5	0	1	3.5	9	0.5	1	0	2.5	6	0.5	1	1	1.5	3	0.5	0h	0h	R/W
Bit2	Bit1	T1	T2	T3 (Unit: CPU Clock)																									
0	0	4.5	11	0.5																									
0	1	3.5	9	0.5																									
1	0	2.5	6	0.5																									
1	1	1.5	3	0.5																									
0	<p>External LCD Driver Control. This bit is used to control the external LCD Driver interface enable or disable. 0: Disable 1: Enable If set high, then the Port3 bit[1:0] are defined as LCD Driver interface signals. PT3_1 → LCD_E PT3_0 → LCD_RW</p>	0h	0h	R/W																									

[REG 100Eh]: LCD Command Register

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

[REG 100Fh]: LCD Data Register

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

Example:

```

LDA    #00000100b           ; External LCD Driver Control Enable
STA    100Dh

LDA    #01h                 ; Command Write, to clear LCD screen.
STA    100Eh

LDA    100Eh                ; Command Read, to determine LCD busy flag.

LDA    #41h                 ; Data Write, write "A" into LCD screen.
STA    100Fh

LDA    100Fh                ; Data Read, read data into ACC from LCD module
    
```

8.12 PWM

When the bit4 of [REG 101Dh] is set to high, then the PWM mode is enable. The duty cycle of PWM output is controlled by [REG 101Ch] bit7~0. The Timer Base of PWM could be set by the Clock Source of Timer3 [REG 1018h]Bit2~0. The set-up of TM3_L is related to PWM Resolution. The optimized Value for TM3_L is as following table.

PWM Resolution	TM3_L Value
8 bit	FFh
7 bit	7Fh
6 bit	3Fh
5 bit	1Fh

Example:

```

LDA    #18h
STA    101Dh           ; Set PWM Enable.
LDA    #FFh
STA    101Ch           ; producing 50% Duty Cycle's PWM Pulse
                        ; 8 bit resolution, PWM1&PWM2 Enable
    
```

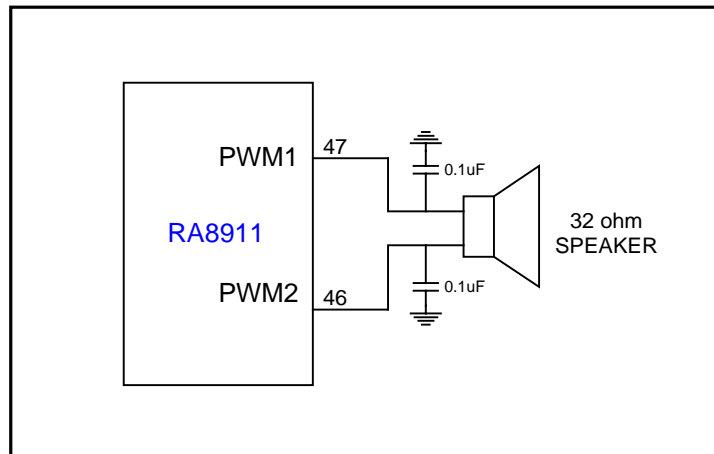


Figure 8-25 PWM Application

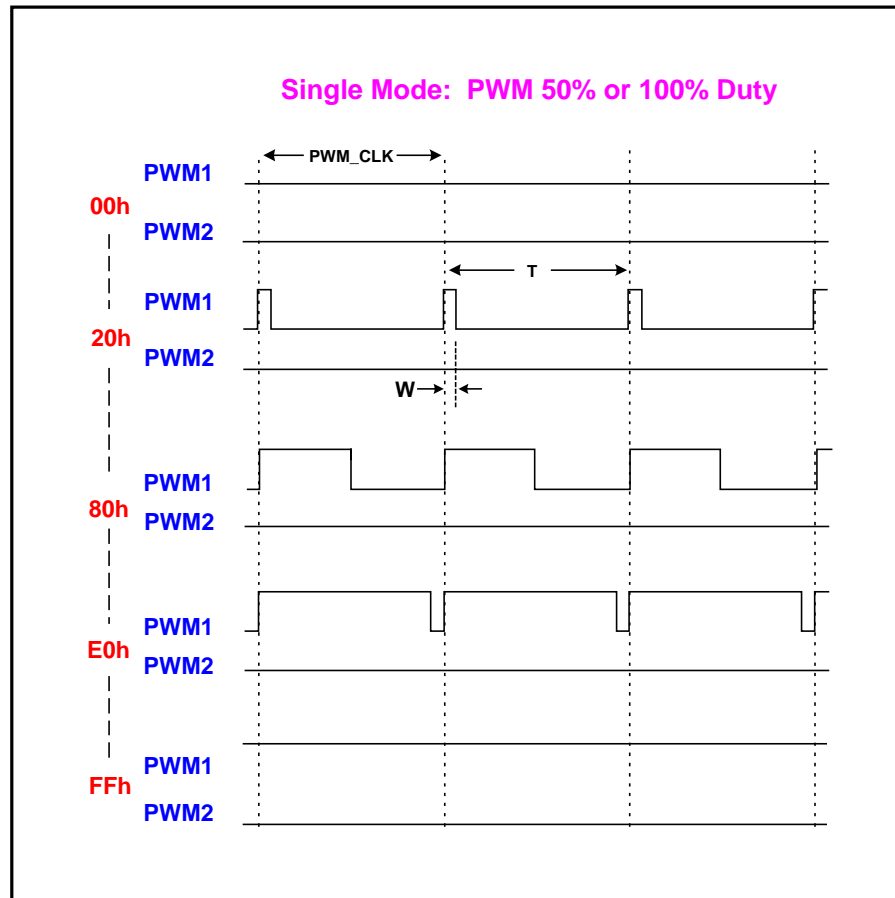


Figure 8-26 PWM(Single Mode) 50% or 100% Duty Waveform

The formula of PWM Clock and PWM Duty Cycle of Single Mode 50% or 100% Duty are as following:

1. PWM Clock(Unit: Time):

$$T=1/PWM_CLK=[(TM3_H+1) \times (TM3_L+1)]/TM3_CLK_Source$$

2. PWM Duty Cycle:

$$PWM_Duty=W/T=(PWM_Data+1)/(TM3_L+1)$$

$$W=[(TM3_H+1) \times (PWM_Data+1)]/TM3_CLK_Source$$

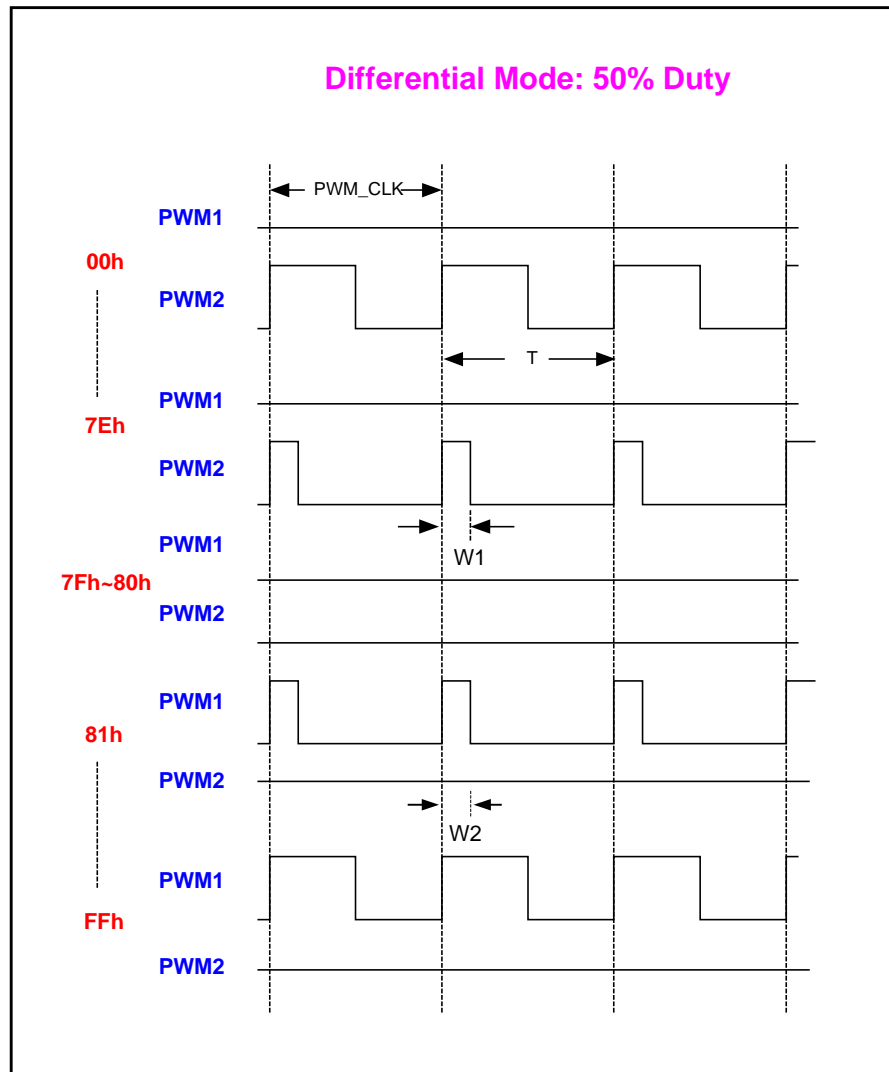


Figure 8-27 PWM 50% Duty Waveform

The formula of PWM Clock and PWM Duty Cycle of Differential Mode 50% Duty are as following:

$$T=1/PWM_CLK=[(TM3_H+1) \times (TM3_L+1)]/TM3_CLK_Source$$

PWM_Data=0~127 → PWM2

$$PWM_Duty1=W_1/T=[128-(PWM_Data+1)]/(TM3_L+1)$$

PWM_Data=128~255 → PWM1

$$PWM_Duty2=W_2/T=[(PWM_Data+1)-128]/(TM3_L+1)$$

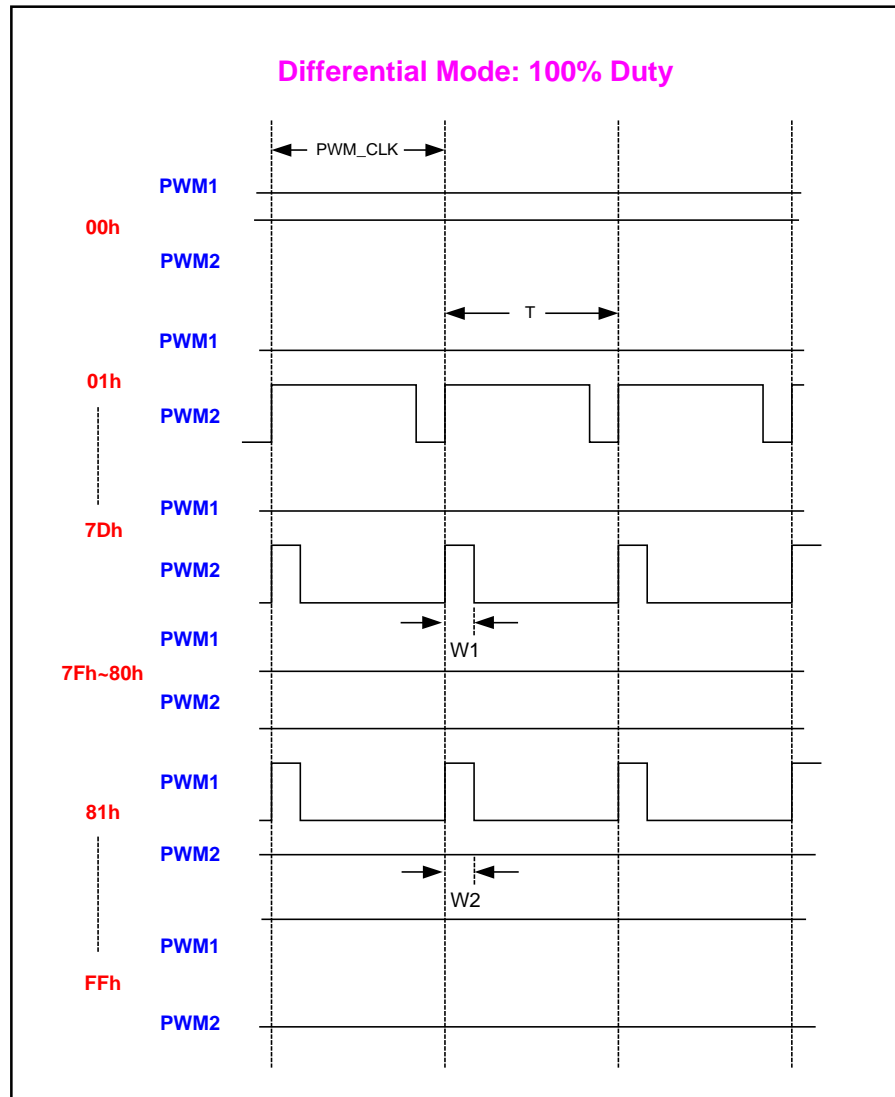


Figure 8-28 PWM 100% Duty Waveform

The formula of PWM Clock and PWM Duty Cycle of Differential Mode 100% Duty are as following:

$$T=1/PWM_CLK=[(TM3_H+1) \times (TM3_L+1)]/TM3_CLK_Source$$

PWM_Data=0~127→PWM2

$$PWM_Duty1=2W_1/T=2 \times [128-(PWM_Data+1)]/(TM3_L+1)$$

PWM_Data=128~255→PWM1

$$PWM_Duty2=2W_2/T=2 \times [(PWM_Data+1)-128]/(TM3_L+1)$$

8.13 Low Voltage Detect (LVD)

The RA8911 builds in an integrated low-voltage detector. The supply voltage is divided and compared to the band gap reference output. If the supply voltage falls below the set voltage value, the bit0 of [REG 1034h] will indicate the status of LVD. The nominal values of the low-voltage detector four points are below [REG 1033h].

When the voltage is lower than the default value, then [REG 1034h] Bit0 will be "1". The signal could output through I/O, and then a warning could happen when users connect an external LED or buzzer. Figure 8-28 and 8-29 are the LVD application circuit. There is also an example following by that.

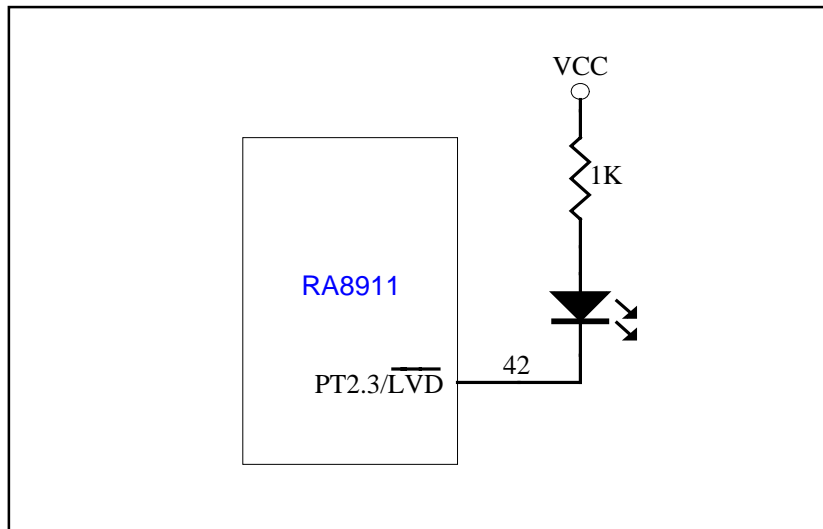


Figure 8-28 LVD Application

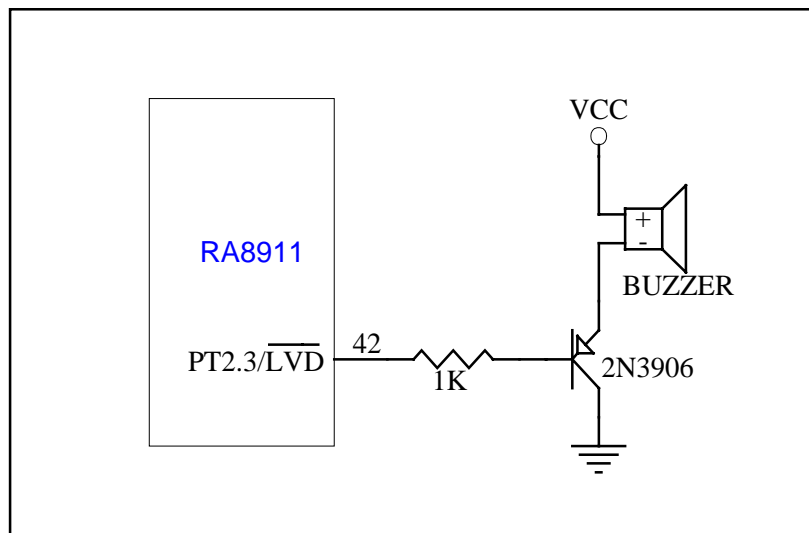


Figure 8-29 LVD Application

[REG 1033h]: LVD Control Register

Bit	Description	Reset	Default	Access
-----	-------------	-------	---------	--------

3	LVD Output Control This bit is used to control the output of LVD. If set high, then the Port2 bit3 is defined as the output of LVD#. 0: Disable LVD output 1: Enable LVD Output	0h	0h	R/W
2	LVD Enable Control 0: Disable 1: Enable	0h	0h	R/W
1-0	LVD Voltage Select Bit1 Bit0 Detected Voltage ----- 0 0 3V 0 1 2.8V 1 0 2.6V 1 1 2.4V If the LVD enabled, the bit0 of register \$1034h will indicate the status of LVD.	0h	0h	R/W

[REG 1034h]: LVD Status Register

Bit	Description	Reset	Default	Access
0	LVD Indicate. 0: Normal Voltage 1: Low Voltage Detected!	0h	0h	R

Example:

```

LDA    #00001110b    ; LVD Enable and Output Control Enable, LVD
Voltage=2.6V
STA    1033h

```

Voltage_Detect:

```

LDA    1034h    ; Low Voltage Detected
AND    #01h
BEQ    Normal_Voltage
JSR    Low_Voltage

```

Normal_Voltage:

```

JMP    Voltage_Detect

```

Low_Voltage:

```

:
:
RTS

```

8.14 External SRAM

RA8911 allows users to connect an external RAM or ROM. The decoding address is 4000H~7FFFH, and the size is 16K Byte. If share the BANK with Flash ROM, the size could reach $2^8 \times 16K = 4M$ byte. Figure 8-30 is the diagram for connecting external 32K-Byte RAM.

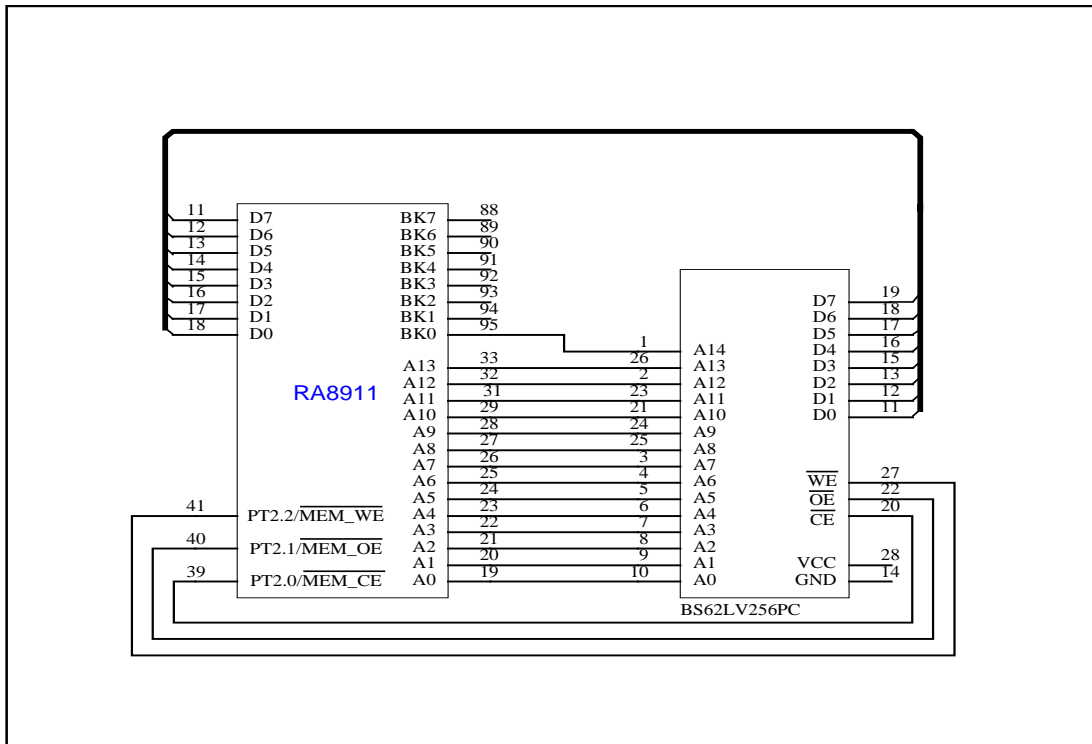


Figure 8-30 RA8911 and External RAM Interface

8.15 Analog-to-Digital Converter (ADC) Module

RA8911 built in a high performance 10-bit 4 channel A/D converter. This ADC is designed by Successive Approximate Register structure (S.A.R.), and conversion rate is 100KHz for signal channel. 10-bit ADC can be perfectly used in Touch Panel function.

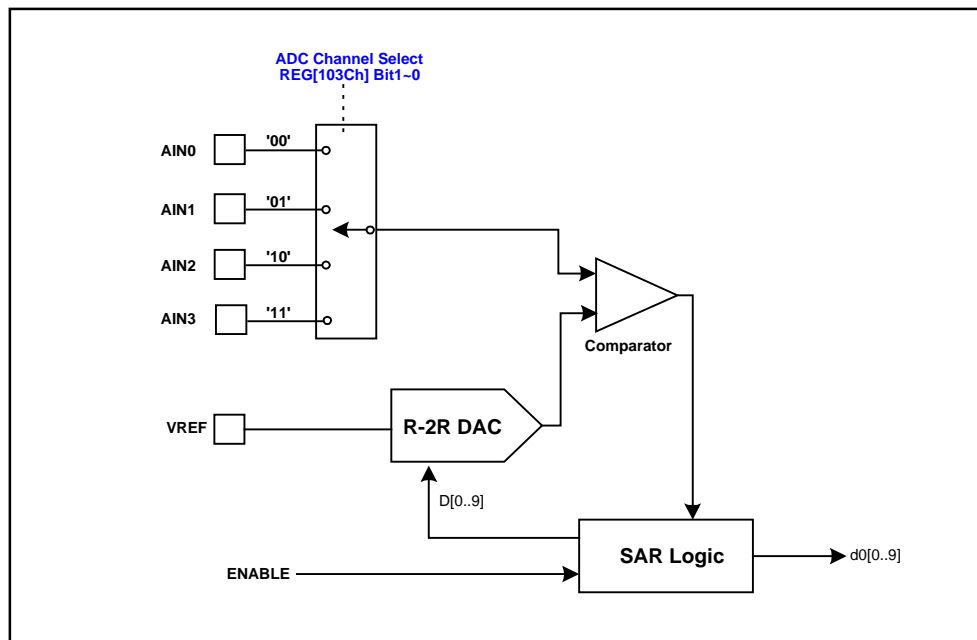


Figure 8-31 ADC Converter

[REG 103Ah]: ADC High-Byte Register

Bit	Description	Reset	Default	Access
7-0	ADC Output Data Bit[9:2]	0h	0h	R

[REG 103Bh]: ADC Low-Byte Register

Bit	Description	Reset	Default	Access
7-6	ADC Output Data Bit[1:0]	0h	0h	R
5-0	Not Used	0h	0h	R

[REG 103Ch]: ADC Control Register(1)

Bit	Description	Reset	Default	Access																		
7	Reserved	0h	0h	W																		
6	ADC Interrupt Enable 0: Disable 1: Enable	0h	0h	W																		
5	ADC Loop Control 0: Disable 1: Enable	0h	0h	W																		
4	ADC Mode Select 0: 4-Channels ADC 1: Touch Panel	0h	0h	W																		
3	ADC Enable 0: Disable 1: Enable	0h	0h	W																		
2	ADC Clock Select 0: Low Frequency 1: High Frequency	0h	0h	W																		
1-0	ADC Channel Select <table style="margin-left: 20px; border-collapse: collapse;"> <tr> <td style="border: none;">Bit1</td> <td style="border: none;">Bit0</td> <td style="border: none;">Channel</td> </tr> <tr> <td style="border: none;">-----</td> <td></td> <td></td> </tr> <tr> <td style="border: none;">0</td> <td style="border: none;">0</td> <td style="border: none;">0</td> </tr> <tr> <td style="border: none;">0</td> <td style="border: none;">1</td> <td style="border: none;">1</td> </tr> <tr> <td style="border: none;">1</td> <td style="border: none;">0</td> <td style="border: none;">2</td> </tr> <tr> <td style="border: none;">1</td> <td style="border: none;">1</td> <td style="border: none;">3</td> </tr> </table> <p style="margin-left: 20px; color: blue; font-size: small;">Note: When RA8911 enters into Saving Mode, in order to avoid the leaking behavior, please do not let ADC Channel Floating or set ADC Type as Touch Panel function.</p>	Bit1	Bit0	Channel	-----			0	0	0	0	1	1	1	0	2	1	1	3	0h	0h	W
Bit1	Bit0	Channel																				

0	0	0																				
0	1	1																				
1	0	2																				
1	1	3																				

[REG 103Dh]: ADC Control Register(2)

Bit	Description	Reset	Default	Access
3	Touch Panel Switch Y2 Control 0: Switch Off 1: Switch On	0h	0h	W
2	Touch Panel Switch Y1 Control 0: Switch Off 1: Switch On	0h	0h	W
1	Touch Panel Switch X2 Control 0: Switch Off 1: Switch On	0h	0h	W

0	Touch Panel Switch X1 Control 0: Switch Off 1: Switch On	0h	0h	W
---	--	----	----	---

[REG 103Eh]: ADC Status Register

Bit	Description	Reset	Default	Access
7-2	Not Used	--	--	--
1	ADC Transfer Done 0: Not Ready 1: Ready <i>Note: When ADC is under One Time Mode (No Loop) and data transfer is finished, then it will generate Ready Signal (Bit 1=1). At this time, users need to clean the Ready Signal and let it become Bit 1=0 before read the next data.</i>	0h	0h	R
0	Touch Panel Detector 0: Normal 1: Touch Detected	0h	0h	R

8.15.1 ADC Touch Panel Loop Control

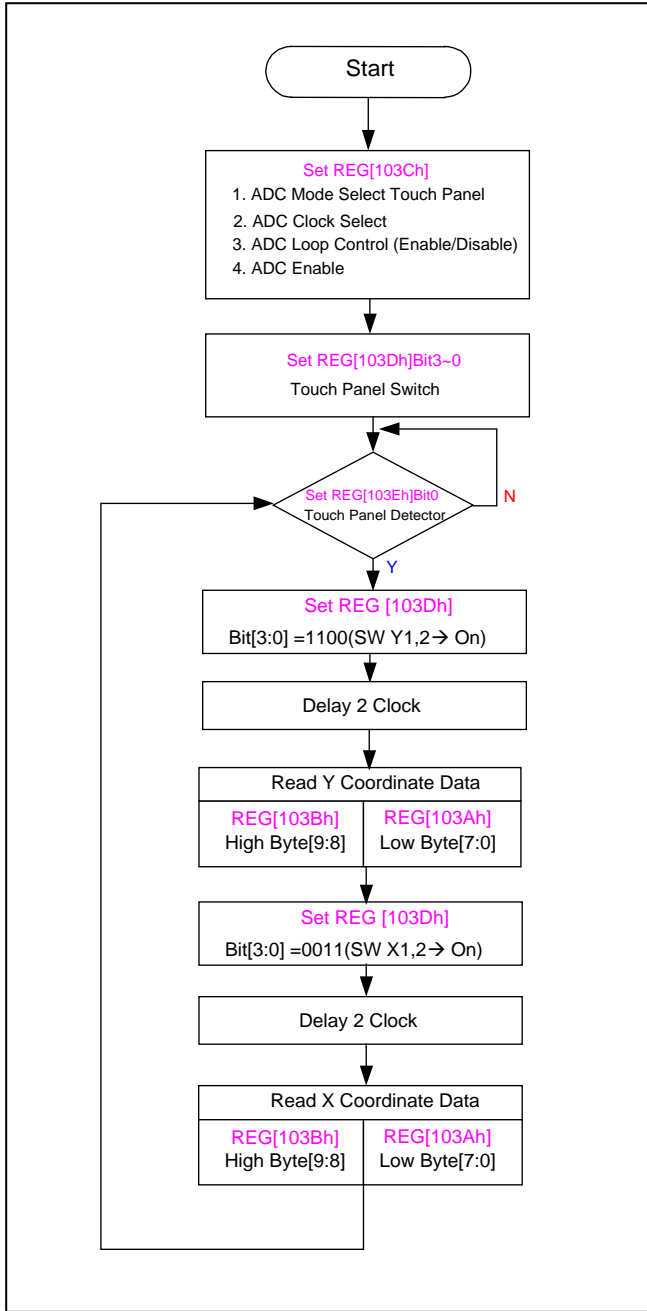


Figure 8-32 ADC Touch Panel Loop Control Flowchart

Note:

When ADC Loop Control Enable, then Ready signal and Interrupt signal will not action.

Example1: (ADC Touch Panel Loop Control)

```
LDA #00111000b
STA 103Ch
```

```
LDA #0Fh
STA 103Dh
```

ReDetect:

```
LDA 103Eh
AND #01h
BEQ ReDetect
```

```
LDA #0Ch
STA 103Dh
JSR Delay
LDA 103Bh
STA 80h
LDA 103Ah
STA 81h
```

```
LDA #03h
STA 103Dh
JSR Delay
LDA 103Bh
STA 82h
LDA 103Ah
STA 83h
```

```
JMP ReDetect
```

Delay:

```
NOP
NOP
RTS
```

8.15.2 ADC Touch Panel No Loop Control

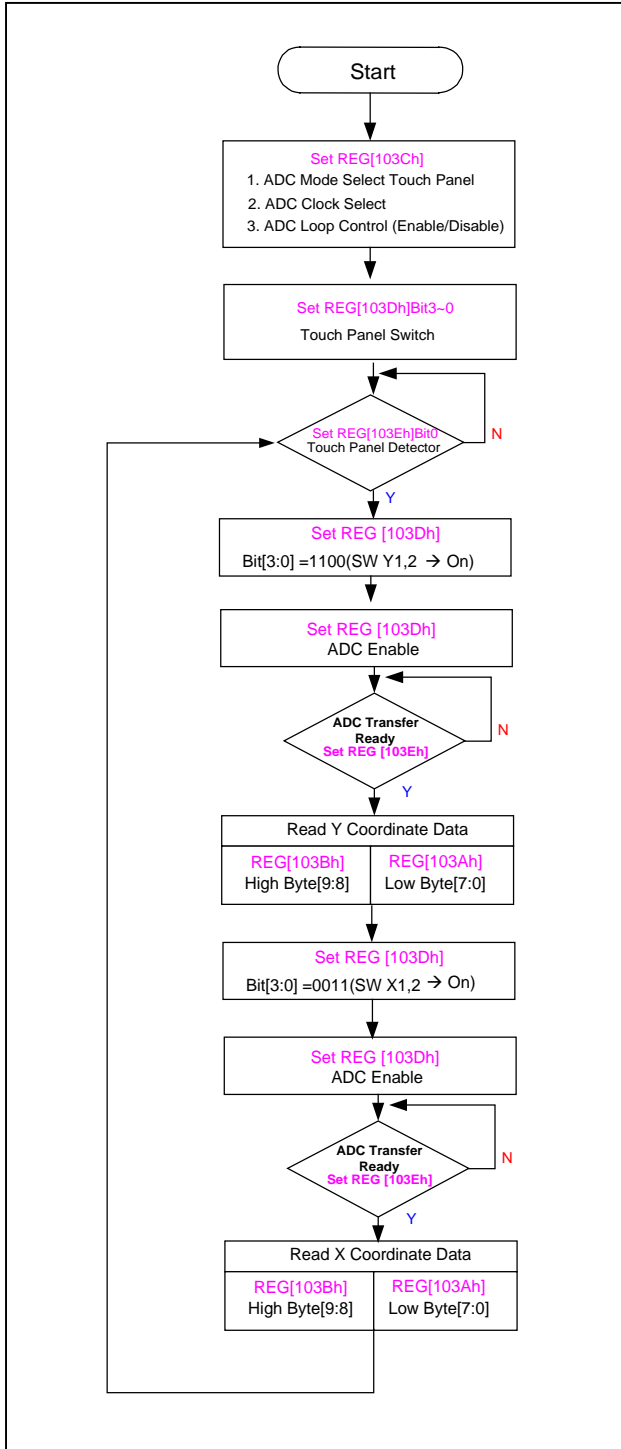


Figure 8-33 ADC Touch Panel No Loop Control Flowchart

Example2: (ADC Touch Panel without Loop Control)

```

LDA    #00010000b
STA    103Ch

LDA    #0Fh
STA    103Dh

ReDetect:
LDA    103Eh
AND    #01h
BEQ    ReDetect

LDA    #0Ch
STA    103Dh

LDA    103Ch
ORA    #00001000b
STA    103Ch

Wait:
LDA    103eh
AND    #00000010b
BEQ    Wait

LDA    103Bh
STA    80h
LDA    103Ah
STA    81h

LDA    #03h
STA    103Dh

LDA    103Ch
ORA    #00001000b
STA    103Ch

Wait1:
LDA    103Eh
AND    #00000010b
BEQ    Wait1
LDA    103Bh
STA    82h
LDA    103Ah
STA    83h
JMP    ReDetect
    
```

RA8911 contains a 10-bit ADC, providing two modes selection: one is 4-channels ADC, and the other one is for Touch Panel function. When Touch Panel mode is selected, there are ADC Loop Control and No Loop Control while reading X and Y coordination from Touch Panel. The Touch Panel function of RA8911 is controlled by [RAG 103Ch and 103Dh]. When Touch Panel detection is executed, which is controlled by REG[103Eh]bit0, and then open the 4-wire resistor touch panel Switch X1, X2, Y1 and Y2 ON by [REG 103Dh] bit0~3. ADC will read the voltage value from resistor, and get data of touched coordination after transformation.

8.16 1Hz, 2Hz and 1/60Hz Interrupt/Wakeup

RA8911 provides 1Hz, 2Hz, and 1/60 Hz's Interrupt/Wakeup source. If 1/60Hz is used as Source Clock, the RTC (Real Time Clock) function could be reached after some S/W effort. When RA8911 enters into Sleep mode, it could also be used as time counting function and wake-up the IC.

8.17 Multiplier and Accumulator(MAC)

RA8911 includes a 16x16 Hardware Multiplier and Accumulator. It provides four modes selection: 16x16, 16x8, 8x16, and 8x8. The function of MAC helps programmers shorten development time and save efforts of writing S/W instructions. Programmers only need to choose which mode they need, and then it will quickly provide answers after filling in multiplier and multiplicand.

RA8911 provides two set-up types for MAC, each separately includes four modes selection: The design structure of MAC provides three data Register for MAC (Multiplier A, B and C). Multiplier A and B could be divided to High Byte(8-bit) and Low Byte(8-bit), and Multiplier C is a combination of C0(LL), C1(LH), C2(HL), and C3(HH) with 8-bit each. MAC's register is set and controlled by REG[1040h~1048h]. Please refer to the following description for the example of Read and Write.

1. Multiplier

a. 16x16: (AL→AH→BL→BH→C0→C1→C2→C3)

Calculation 16x16 (No ACC)

AL	AH	BL	BH	--	C0	C1	C2	C3
W	W	W	W	--	R	R	R	R

Example:

```

LDA    #00010000b    ; MAC Control Enable
STA    1031h

LDA    #00001000b    ; Select AX=16 Bit, BX=16 Bit
STA    1048h        ; Clear CX, Accumulate Disable

LDA    #73h          ; AL=73h
STA    1040h

LDA    #0bh          ; AH=0bh
STA    1041h

LDA    #71h          ; BL=71h
STA    1042h

LDA    #01h          ; BH=01h
STA    1043h

LDA    1044h        ; Store the value of C0 to memory address 80h
STA    80h
    
```

```
LDA    1045h           ; Store the value of C1 to memory address 81h
STA    81h
LDA    1046h           ; Store the value of C2 to memory address 82h
STA    82h
LDA    1047h           ; Store the value of C3 to memory address 83h
STA    83h
```

Note: $C=A \times B=0b73h \times 0171h \rightarrow C=1080C3h$
 User RAM 80h=C3h
 User RAM 81h=80h
 User RAM 82h=10h
 User RAM 83h=00h

b. 16x8: (AL → AH → BL → C0 → C1 → C2 → C3)

Calculation 16x8 (No ACC)

AL	AH	BL	--	--	C0	C1	C2	C3
W	W	W	--	--	R	R	R	R

c. 8x16: (AL → BL → BH → C0 → C1 → C2 → C3)

Calculation 8x16 (No ACC)

AL	--	BL	BH	--	C0	C1	C2	C3
W	--	W	W	--	R	R	R	R

d. 8x8: (AL → BL → C0 → C1 → C2 → C3)

Calculation 8x8 (No ACC)

AL	--	BL	--	--	C0	C1	C2	C3
W	--	W	--	--	R	R	R	R

Note:

1. BH is not used in 16x8's MAC; therefore, please do not fill in other value in BH register.
2. AH is not used in 8x16's MAC; therefore, please do not fill in other value in AH register.
3. AH and BH are not used in 8x8's MAC; therefore, please do not fill in other value in AH and BH registers.

2. Multiplier and Accumulator

a. 16x16: (AL → AH → BL → BH → C0 → C1 → C2 → C3)

Calculation 16x16 (ACC)

AL	AH	BL	BH	--	C0	C1	C2	C3
W	W	W	W	--	R	R	R	R

Example:

```

LDA    #00010000b    ; MAC Control Enable
STA    1031h

LDA    #00001100b    ; Select AX=16 Bit, BX=16 Bit
STA    1048h          ; Clear CX, Accumulate Enable

One:   LDA    #73h      ; AL=73h
       STA    1040h
       LDA    #0bh     ; AH=0bh
       STA    1041h
       LDA    #71h     ; BL=71h
       STA    1042h
       LDA    #01h     ; BH=01h
       STA    1043h

Two:   LDA    #73h      ; AL=73h
       STA    1040h
       LDA    #0bh     ; AH=0bh
       STA    1041h
       LDA    #71h     ; BL=71h
       STA    1042h
       LDA    #01h     ; BH=01h
       STA    1043h

       LDA    1044h    ; Store the value of C0 to memory address 80h
       STA    80h
       LDA    1045h    ; Store the value of C1 to memory address 81h
       STA    81h
       LDA    1046h    ; Store the value of C2 to memory address 82h
       STA    82h
       LDA    1047h    ; Store the value of C3 to memory address 83h
       STA    83h
    
```

Note: $C=A1 \times B1 + A2 \times B2 = 0b73h \times 0171h + 0b73h \times 0171h \rightarrow C=210186h$
 User RAM Address 80h=86h
 User RAM Address 81h=01h
 User RAM Address 82h=21h
 User RAM Address 83h=00h

b. 16x8: (AL → AH → BL → C0 → C1 → C2 → C3)

Calculation 16x8 (ACC)

AL	AH	BL	--	--	C0	C1	C2	C3
W	W	W	--	--	R	R	R	R

c. 8x16: (AL → BL → BH → C0 → C1 → C2 → C3)

Calculation 8x16 (ACC)

AL	--	BL	BH	--	C0	C1	C2	C3
W	--	W	W	--	R	R	R	R

d. 8x8: (AL→BL→C0→C1→C2→C3)

Calculation 8x8 (ACC)

AL	--	BL	--	--	C0	C1	C2	C3
W	--	W	--	--	R	R	R	R

Note:

1. BH is not used in 16x8's MAC; therefore, please do not fill in other value in BH register.
2. AH is not used in 8x16's MAC; therefore, please do not fill in other value in AH register.
3. AH and BH are not used in 8x8's MAC; therefore, please do not fill in other value in AH and BH registers.
4. If CPU is slow, IDLE cycle is optional.

[REG 1040h]: Multiplier A Low-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier A Data Bit[7:0]	0h	0h	R/W

[REG 1041h]: Multiplier A High-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier A Data Bit[15:8]	0h	0h	R/W

[REG 1042h]: Multiplier B Low-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier B Data Bit[7:0]	0h	0h	R/W

[REG 1043h]: Multiplier B High-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier B Data Bit[15:8]	0h	0h	R/W

[REG 1044h]: Multiplier C Low Word Low-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[7:0]	0h	0h	R/W

[REG 1045h]: Multiplier C Low Word High-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[15:8]	0h	0h	R/W

[REG 1046h]: Multiplier C High Word Low-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[23:16]	0h	0h	R/W

[REG 1047h]: Multiplier C High Word High-Byte Register

Bit	Description	Reset	Default	Access
7-0	Multiplier C Data Bit[31:24]	0h	0h	R/W

[REG 1048h]: Multiplier Control Register

Bit	Description	Reset	Default	Access
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7-4	Overflow Flag	0h	0h	R
3	Clear CX 1: Clear CX 0: No Action	0h	0h	R/W
2	Accumulate Mode 0: Disable, $CX = AX \times BX$ 1: Enable, $CX_{n+1} = AX \times BX + CX_n$	0h	0h	R/W
1	AX 8/16Bit Select 0: AX = 16Bit 1: AX = 8Bit	0h	0h	R/W
0	BX 8/16Bit Select 0: BX = 16Bit 1: BX = 8Bit	0h	0h	R/W

9. Electrical Characteristic

Operating Temperature Range	-10 ^o C to + 75 ^o C
Storage Temperature Range	- 55 ^o C to +140 ^o C
Lead Temperature Range (soldering, 10 seconds).....	+300 ^o C
Positive Voltage on any pin, with respect to Ground	V _{IO} + 0.3V
Negative Voltage on any pin, with respect to Ground	-0.3V
Maximum V _{IO}	+5V
Maximum V _{CC}	+5.5V

* Stresses above those listed above could cause permanent damage to the device. This is stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

9.1 DC Electrical Characteristics

(T_A = -10^oC ~ 75^oC, V_{CC} = 2.4V ~ 3.6V)

Table 9-1

Parameter	Symbol	Min	Typ.	Max	Units	Comments
Input Buffer (RXD) Low Input Level High Input Level	V _{ILI} V _{HI}	2.0		0.8	V V	TTL Levels
Schmitt Input Buffer (RESET#, BREAK#, MONITOR#) Low Input Level High Input Level Schmitt Trigger Hysteresis	V _{ILIS} V _{HIHS} V _{HYS}	2.2	250	0.8	V V mV	Schmitt Trigger Schmitt Trigger
Output Buffer (TXD) Low Output Level Output Leakage	V _{OL} I _{OL}	-10		0.5 +10	V uA	I _{OL} = 12mA (24mA) V _{IN} = 0 to V _{CC} (Note 1)
I/O Buffer (PT1_[7:0]) Low Output Level High Output Level Output Leakage	V _{OL} V _{OH} I _{OL}	2.4 -10		0.5 +10	V V uA	I _{OL} = 8mA I _{OH} = -4mA V _{IN} = 0 to V _{CC} (Note 1)
I/O Buffer (PT2_[1:0]) Low Output Level High Output Level Output Leakage	V _{OL} V _{OH} I _{OL}	2.4 -10		0.5 +10	V V uA	I _{OL} = 4mA I _{OH} = -2mA V _{IN} = 0 to V _{CC} (Note 1)
I/O Buffer (PT2_[7:2]) Low Output Level High Output Level Output Leakage	V _{OL} V _{OH} I _{OL}	2.4 -10		0.4 +10	V V uA	I _{OL} = 8mA I _{OH} = -4mA V _{IN} = 0 to V _{IO} (Note 1)

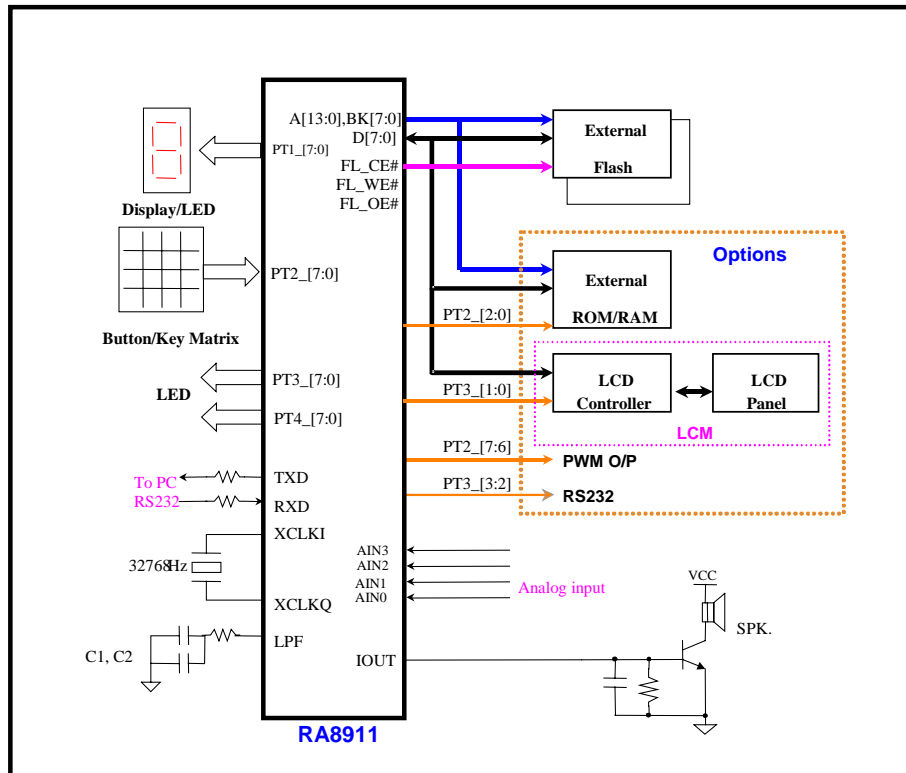
Capacitance T_A = 25^oC; V_{CC} = 3.3V

9.2 Power Consumption

Operation Mode	Typ.	Unit	Condition
Normal Mode	7.4	mA	1. System Clock: 22.1MHz 2. VDD: 3.3V 3. Flash: MX29LV160T 4. Port1~4: Input Mode, 4mA, Pull High 50KΩ 5. Port1~2: CMOS Mode
Sleep Mode	492	μA	
Deep Sleep	408	μA	
Normal Mode	2.57	mA	1. System Clock: 7.37MHz 2. VDD: 3.3V 3. Flash: MX29LV160T 4. Port1~4: Input Mode, 4mA, Pull High 50KΩ 5. Port1~2: CMOS Mode
Sleep Mode	223	μA	
Deep Sleep	195	μA	
Normal Mode	0.92	mA	1. System Clock: 2.46MHz 2. VDD: 3.3V 3. Flash: MX29LV160T 4. Port1~4: Input Mode, 4mA, Pull High 50KΩ 5. Port1~2: CMOS Mode
Sleep Mode	124	μA	
Deep Sleep	115	μA	
Normal Mode	0.58	mA	1. System Clock: 1.47MHz 2. VDD: 3.3V 3. Flash: MX29LV160T 4. Port1~4: Input Mode, 4mA, Pull High 50KΩ 5. Port1~2: CMOS Mode
Sleep Mode	103	μA	
Deep Sleep	97	μA	
Erase Mode	11.7~16.5	mA	
Download Mode	2.6~3.2mA	mA	
RTC Mode	4.2~5.9	μA	
Power Saving	0.4	μA	

10. Application

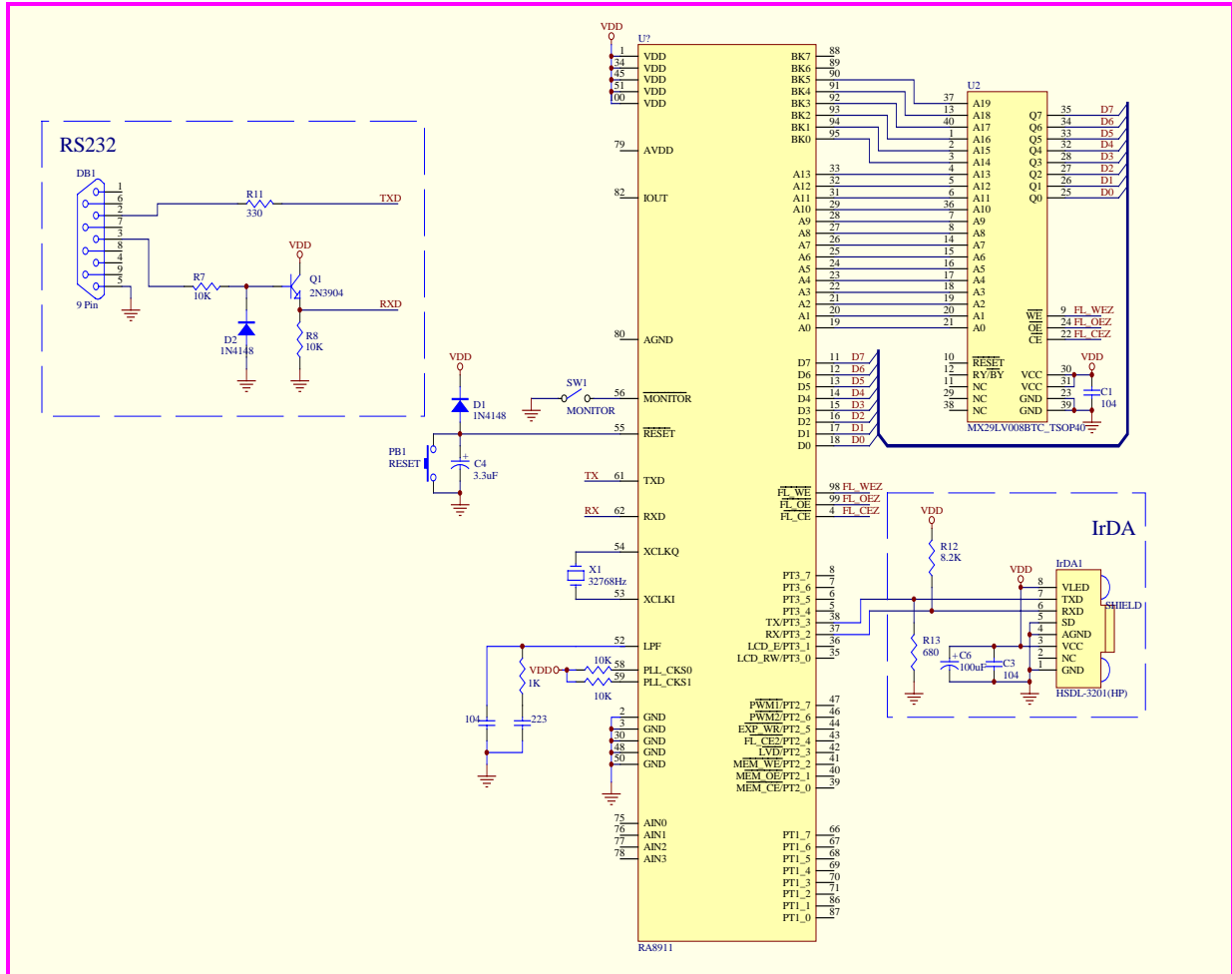
The following Block diagram is the basic application circuit of RA8911. We also give three examples on the user manual of RICE-2000 to let users have more understanding of RA8911 and the develop environment of RICE-2000, and then start to proceed program designing and product developing. The examples have simple I/O control and speech samples. Please refer to the user manual of RICE-2000 if you needed.



Application Field	
Simple I/O Controller	Simple I/O Controller
Speech Controller	Speech Controller
Middle-Grade Product	Middle-Grade Product
High-Grade Product	High-Grade Product

Example:

This application circuit can support the wireless transmission. The IrDA interface provides different means for clients to develop their devices, such as guiding machine, Interactive toys.



Appendix

The following table is the Flash ROM list, which RA8911 supports.

MANUFACTURER	DEVICE NUMBER	MEMORY SIZE	VOLTAGE	BUS
MXIC	MX29F1001BPC-90	1M Bit	5.0V	x8
MXIC	MX29F002BPC-90	2M Bit	5.0V	x8
MXIC	MX29F004BPC-90	4M Bit	5.0V	x8
MXIC	MX29LV008BTC	8M Bit	3.3V	x8
MXIC	MX29F100TTC-55	1M Bit	5.0V	x8/x16
MXIC	MX29F200BTC-55	2M Bit	5.0V	x8/x16
MXIC	MX29F200TTC-70	2M Bit	5.0V	x8/x16
MXIC	MX29F400TTC-55	4M Bit	5.0V	x8/x16
MXIC	MX29F800TTC-90	8M Bit	5.0V	x8/x16
MXIC	MX29F080TC-70	8M Bit	5.0V	x8
MXIC	MX29LV004BTC-70	4M Bit	3.3V	x8
MXIC	MX29LV800TTC-70	8M Bit	3.3V	x8/x16
MXIC	MX29LV400TTC-70	4M Bit	3.3V	x8/x16
MXIC	MX29LV160TTC-70	16M Bit	3.3V	x8/x16
AMIC	A29001T-70	1M Bit	5.0V	x8
AMIC	A29002T-70	2M Bit	5.0V	x8
AMIC	A29040-70	4M Bit	5.0V	x8
AMIC	A29800UV-70	8M Bit	5.0V	x8/x16
ATMEL	AT49F001T-70	1M Bit	5.0V	x8
ATMEL	AT49F001NT-70	1M Bit	5.0V	x8
ATMEL	AT49F002NT-90	2M Bit	5.0V	x8
ATMEL	AT49BV1614T-90	16M Bit	3.3V	x8/x16

Note:

- RA8902 supports two types of Flash command definition, Command1 and Command2. (reference chart 8.3.1) If your target Flash parts don't on the list, please refer to chart 8.3.1 to compare its Flash command definition. You could also ask for our agents' help to see whether it is supported.
- If users need to connect 32Mbit Flash to RA89 series ICE PCB, such as MXIC (MX29LV320T/B) or AMD (AM29L320D), please make sure you notice the following message:

The Flash Pin 14 must be connected to 3.3V

