RAiO

RA8900

8-Bit Micro-Controller

Version 1.7

November 9, 2004

RAiO Technology Inc.

Specification Revision History		
Version	**Date**	**Description**
1.4	2002/08/08	**RA8900D Modify Contents** 1. **4.2 Pin Assignment** Version C-->Version D 2. **5. Pin Description** Signal PT1_7, PWM2--> PT1_7, PWM1 Signal PT1_6, PWM1--> PT1_6, PWM2 PT2(PT2_0~PT2_7) Description: I/O Port1--> I/O Port2 3. **7. Registers Description** Address 14h, 17h, 19h, 24h content modify 4. REG[0Ah], REG[0Bh], REG[0Ch], REG[17h], REG[19h], REG[1Ah] content modify 5. **8. Function Description** Figure 8-1, Figure 8-2, Figure 8-5, Table 8-1, Table 8-3, Figure 8-6, Figure 8-7 Figure 8-8, Figure 8-9, Figure 8-10 content modify 6. **10. Application** Example1~5: Figure10-2, Figure10-3, Figure10-4, Figure10-5, Figure10-6 content modify
1.5	2002/11/06	1. Modify Fig 8-7 2. Add FL_2 and FL_TY Description
1.6	2003/10/28	Update Format.
1.7	2004/11/9	Modify Operating Voltage.

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1. General Description

The RA8900 is an 8-bit e-MCU micro-controller. It supports multiple timer/counter sources, versatile interrupt-handling architecture and two built-in DAC's (Digital-to-Analog Converters). It provides a complete speech interface and 32K-bps ADPCM solution that make this chip an excellent choice as the embedded micro-controller for educational speech products.

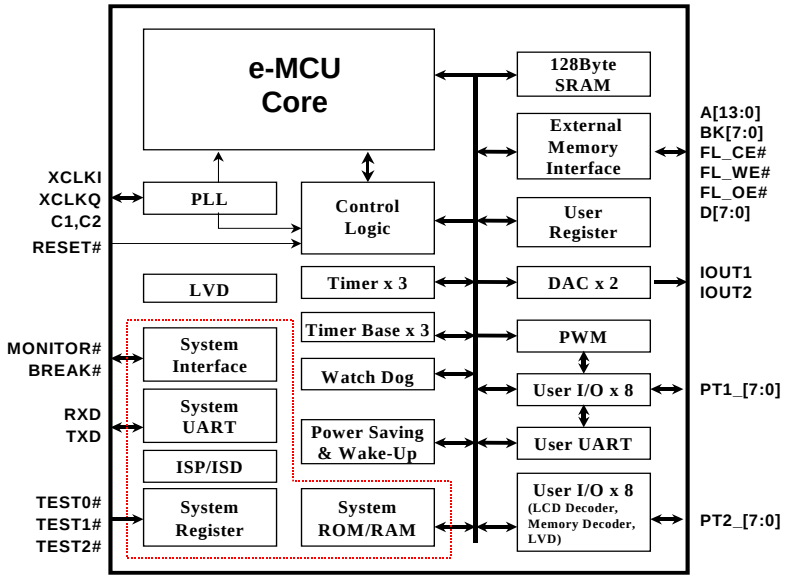
The built-in 4K-bytes ROM support the on-chip RAiO ICE Monitor program which controls the UART and enables the RS232 connection between the RA8900 and a PC host. The RA8900 support the ISP (In-System Programming) and ISD (In-System Debugging) functions. Users can download their programs as well as data from a PC host to the external Flash ROM.

RAiO also support a windows based ICE driver for customers to very easy programming & debugging their program. Using RS232 connection between a speech toy to a PC host running RAiO's download utility program, toy makers are able to implement the Internet Game/Speech download features easily and give the toys multiple attractive characteristics.

2. Feature

- 8-bit e-MCU Micro Processor
- Internal 128-Byte SRAM
- Flexible External Flash Support (Max: 4M byte)
- Support LVD (Low Voltage Detector)
- Support External Memory & LCD Interface
- Support PWM Output with 50% or 100% duty select
- Two 8-Bits Programmable I/O Port
- Three 12-Bits Timer and Three Time-Base Options
- One 4-Bits Watch Dog Timer
- Two 8-bits Current Mode DAC
- One User's UART with Baud Rate Generator, Up to 115200bps
- UART Provide IrDA & ASK IR Mode
- Support UART and Timer Wake-Up Mode
- Support Idle/Sleep Power Saving Mode
- Flexible I/O Interrupt & Wake-Up Mode
- Support Wake-Up Reset Mode
- Built in PLL, Only need one 32768Hz X'tal Oscillator can produce system clock 7.3MHz
- Operating Voltage: 2.4V ~ 3.6V
- Package: Die Form or PQFP-100Pin

3. Block Diagram



4. Die Form

4.1 PAD Diagram

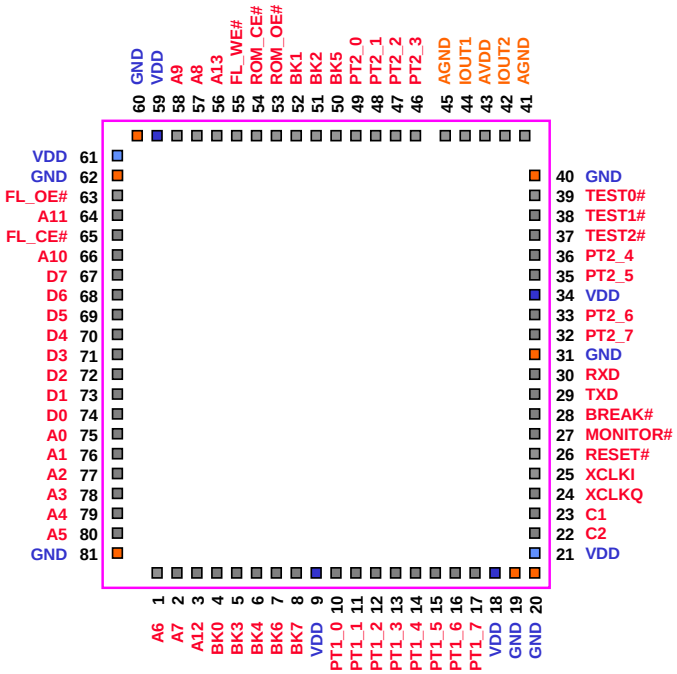


Figure 4-1

4.2 Pin Assignment (PQFP-100Pin)

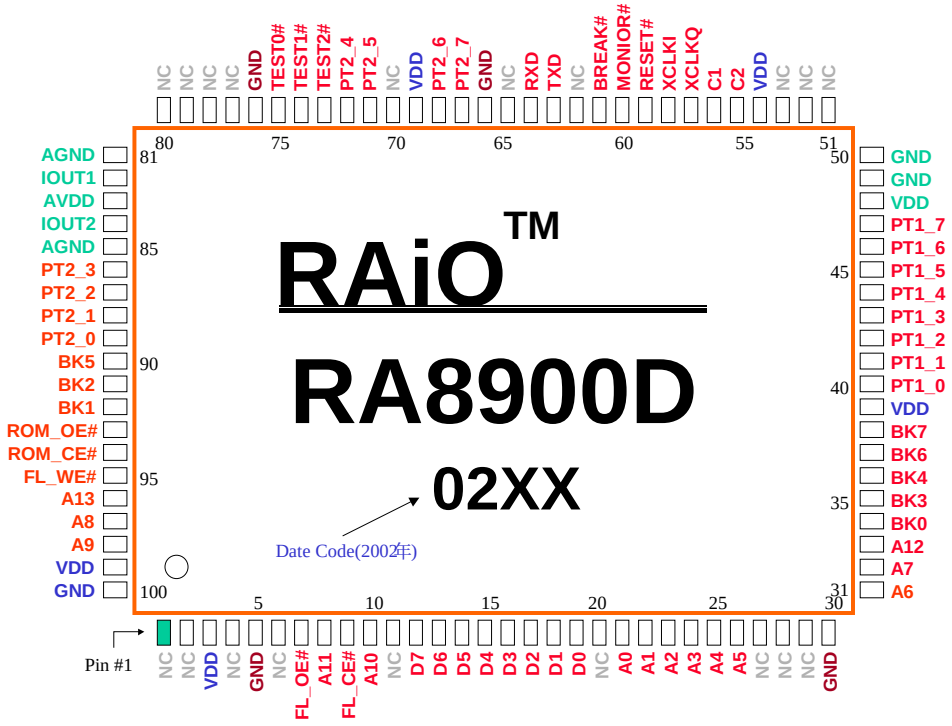


Figure 4-2

4.3 PAD X/Y Coordinate

Table 4-1

PAD Order	PIN Name	X	Y
1	A6	-989.98	-1220.85
2	A7	-879.98	-1220.85
3	A12	-769.98	-1220.85
4	BK0	-659.98	-1220.85
5	BK3	-549.98	-1220.85
6	BK4	-439.98	-1220.85
7	BK6	-329.98	-1220.85
8	BK7	-219.98	-1220.85
9	VDD	-109.98	-1220.85
10	PT1_0	0.02	-1220.85
11	PT1_1	110.02	-1220.85
12	PT1_2	220.02	-1220.85
13	PT1_3	330.02	-1220.85
14	PT1_4	440.02	-1220.85
15	PT1_5	550.02	-1220.85
16	PT1_6	660.02	-1220.85
17	PT1_7	770.02	-1220.85
18	VDD	880.02	-1220.85
19	GND	990.02	-1220.85
20	GND	1110.87	-1220.85
21	VDD	1110.87	-1100
22	C2	1110.87	-990
23	C1	1110.87	-880
24	XCLKQ	1110.87	-770
25	XCLKI	1110.87	-660
26	RESET#	1110.87	-550
27	MONITOR#	1110.87	-440
28	BREAK#	1110.87	-330
29	TXD	1110.87	-220
30	RXD	1110.87	-110
31	GND	1110.87	0
32	PT2_7	1110.87	110
33	PT2_6	1110.87	220
34	VDD	1110.87	330
35	PT2_5	1110.87	440
36	PT2_4	1110.87	550
37	TEST2#	1110.87	660
38	TEST1#	1110.87	770
39	TEST0#	1110.87	880
40	GND	1110.87	990

PAD Order	PIN Name	X	Y
41	AGND	1110.87	1220.85
42	IOUT2	1004.87	1220.85
43	AVDD	898.87	1220.85
44	IOUT1	792.87	1220.85
45	AGND	686.87	1220.85
46	PT2_3	550.02	1220.85
47	PT2_2	440.02	1220.85
48	PT2_1	330.02	1220.85
49	PT2_0	220.02	1220.85
50	BK5	110.02	1220.85
51	BK2	0.02	1220.85
52	BK1	-109.98	1220.85
53	ROM_OE#	-219.98	1220.85
54	ROM_CE#	-329.98	1220.85
55	FL_WE#	-439.98	1220.85
56	A13	-549.98	1220.85
57	A8	-659.98	1220.85
58	A9	-769.98	1220.85
59	VDD	-879.98	1220.85
60	GND	-989.98	1220.85
61	VDD	-1110.83	1100
62	GND	-1110.83	990
63	FL_OE#	-1110.83	880
64	A11	-1110.83	770
65	FL_CE#	-1110.83	660
66	A10	-1110.83	550
67	D7	-1110.83	440
68	D6	-1110.83	330
69	D5	-1110.83	220
70	D4	-1110.83	110
71	D3	-1110.83	0
72	D2	-1110.83	-110
73	D1	-1110.83	-220
74	D0	-1110.83	-330
75	A0	-1110.83	-440
76	A1	-1110.83	-550
77	A2	-1110.83	-660
78	A3	-1110.83	-770
79	A4	-1110.83	-880
80	A5	-1110.83	-990
81	GND	-1110.83	-1100

5. Pin Description

Table 5-1

Signal	Pin#	I/O	Description
RESET#	59	IN	**External Hardware Reset, active low.** This pin is used to reset the system.
BREAK#	61	IN	**User Program Break, active low.** This signal is used to break the user's program from the ISD mode.
MONITOR#	60	IN	**Monitor Program Select, active low.** This signal is used to select the system boot from monitor program (ROM) or user program (Flash). This signal has to pull low when the user wants to download the data from PC or enter the ISP/ISD mode.
PT1_7 PWM1	47	I/O	**Bit-7 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_7 is also as the output of PWM. In PWM mode, the pin is always output and 30mA driving current is selected.
PT1_6 PWM2	46	I/O	**Bit-6 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_6 is also as the output of PWM. In PWM mode, the pin is always output and 30mA driving current is selected.
PT1_5 TX	45	I/O	**Bit-5 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_5 is also as the transmission output of user's UART. In UART mode, the pin is always output except the power saving mode.
PT1_4 RX	44	I/O	**Bit-4 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_4 is also as the receive input of user's UART. In UART mode, the pin is always input.
PT1_3 IR	43	I/O	**Bit-3 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register. The PT1_3 is also as the IR signal driven..
PT1_2	42	I/O	**Bit-2 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT1_1	41	I/O	**Bit-1 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.

PT1_0	40	I/O	**Bit-0 of Port 1** This is a programmable pin for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.
PT2_7 FL_CE2#	67	I/O	**Bit-7 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_7 is also as the secondary external flash chip select. If the secondary flash is enabled, the pin is always output except the power saving mode.
PT2_6 MEM_CE#	68	I/O	**Bit-6 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_6 is also as the external memory chip selecting. If the external memory enabled, the pin is always output except the power saving mode.
PT2_5 MEM_OE#	71	I/O	**Bit-5 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_5 is also as the external memory output enable. If the external memory enabled, the pin is always output except the power saving mode.
PT2_4 MEM_WE#	72	I/O	**Bit-4 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_4 is also as the external memory write enable. If the external memory enabled, the pin is always output except the power saving mode.
PT2_3 LCD_E	86	I/O	**Bit-3 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_3 is also as the chip enable of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
PT2_2 LCD_RW	87	I/O	**Bit-2 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_2 is also as the read/write signal of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode.
PT2_1 LVD#	88	I/O	**Bit-1 of Port 2** This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_1 is also as the output of LVD. If the LVD enabled, the pin is always output except the power saving mode.

<table>
<tr><td>PT2_0
WE25</td><td>89</td><td>I/O</td><td>Bit-0 of Port 2
This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.
The PT2_0 is also as the write control of register $25. If the write register $25 enabled, the pin is always output except the power saving mode.</td></tr>
<tr><td>IOUT1</td><td>84</td><td>OUT</td><td>DAC1 Current Output
This pin is the current output of DAC1.</td></tr>
<tr><td>IOUT2</td><td>82</td><td>OUT</td><td>DAC2 Current Output
This pin is the current output of DAC2.</td></tr>
<tr><td>ADDR[13:0]
FL_S0
FL_S1</td><td>10
21~26
31~32
96~98</td><td>OUT</td><td>14-bit Address Bus.
These signal are used for external memory address bus.
The FL_S0 and FL_S1 are Flash Size Select setup. (Reference Table8-3)
FL_S0 ↔ A11, FL_S1 ↔ A10 jointly pin.</td></tr>
<tr><td>D[7:0]</td><td>12~19</td><td>I/O</td><td>8-bit Data Bus.
These signal are used for external memory data bus.</td></tr>
<tr><td>FL_CE#</td><td>10</td><td>OUT</td><td>Flash Chip Select, active low.
This signal is used for external flash.</td></tr>
<tr><td>FL_WE#</td><td>92</td><td>OUT</td><td>Flash Write Enable, active low.
This signal is used for external flash.</td></tr>
<tr><td>FL_OE#</td><td>8</td><td>OUT</td><td>Flash Output Enable, active low.
This signal is used for external flash.</td></tr>
<tr><td>ROM_OE#</td><td>90</td><td>IN</td><td>Flash Type Select.
This signal is used for external flash.</td></tr>
<tr><td>ROM_CE#</td><td>91</td><td>IN</td><td>Flash Number 1 or 2 Select.
This signal is used for external flash.</td></tr>
<tr><td>BK[7:0]
FL_S2
FL_2#
FL_TY</td><td>34~38
90~92</td><td>OUT</td><td>Flash BANK Select.
This signal is used for external flash.
The FL_S2 is Flash Size Select setup. (Reference Table8-3)
The FL_2 is use one Flash or two Flash Select setup.
The FL_TY is Flash Type Select.
FL_S2 ↔BK1, FL_2# ↔BK2, FL_TY ↔BK5 jointly pin.
<table>
<tr><th>FL_2</th><th>FL_TY
Manufacturer</th><th>IC Number</th></tr>
<tr><td>“1”
Ext. One Flash</td><td>“1”
MXiC</td><td>Ref. Appendix</td></tr>
<tr><td>“0”
Ext. Two Flash</td><td>“0”
ATMEL</td><td>Ref. Appendix</td></tr>
</table></td></tr>
<tr><td>XCLKI</td><td>58</td><td>IN</td><td>Oscillator Input.
This is the input signal of internal PLL.</td></tr>
<tr><td>XCLKQ</td><td>57</td><td>OUT</td><td>Oscillator Output.
This is the output signal of internal PLL.</td></tr>
<tr><td>C1, C2</td><td>56, 55</td><td>IN</td><td>Capacitor Input.
These two signals are connected to the external capacitor for internal PLL.</td></tr>
<tr><td>VDD</td><td>3, 39,
48, 54,
69, 99</td><td>PWR</td><td>Power Supply Voltage.</td></tr>
<tr><td>AVDD</td><td>83</td><td>PWR</td><td>Analog Power Supply Voltage.</td></tr>
</table>

GND	5, 30, 49, 50, 66, 76, 100	PWR	**Ground.**
AGND	81,85	PWR	**Analog Ground.**

6. Memory Organization

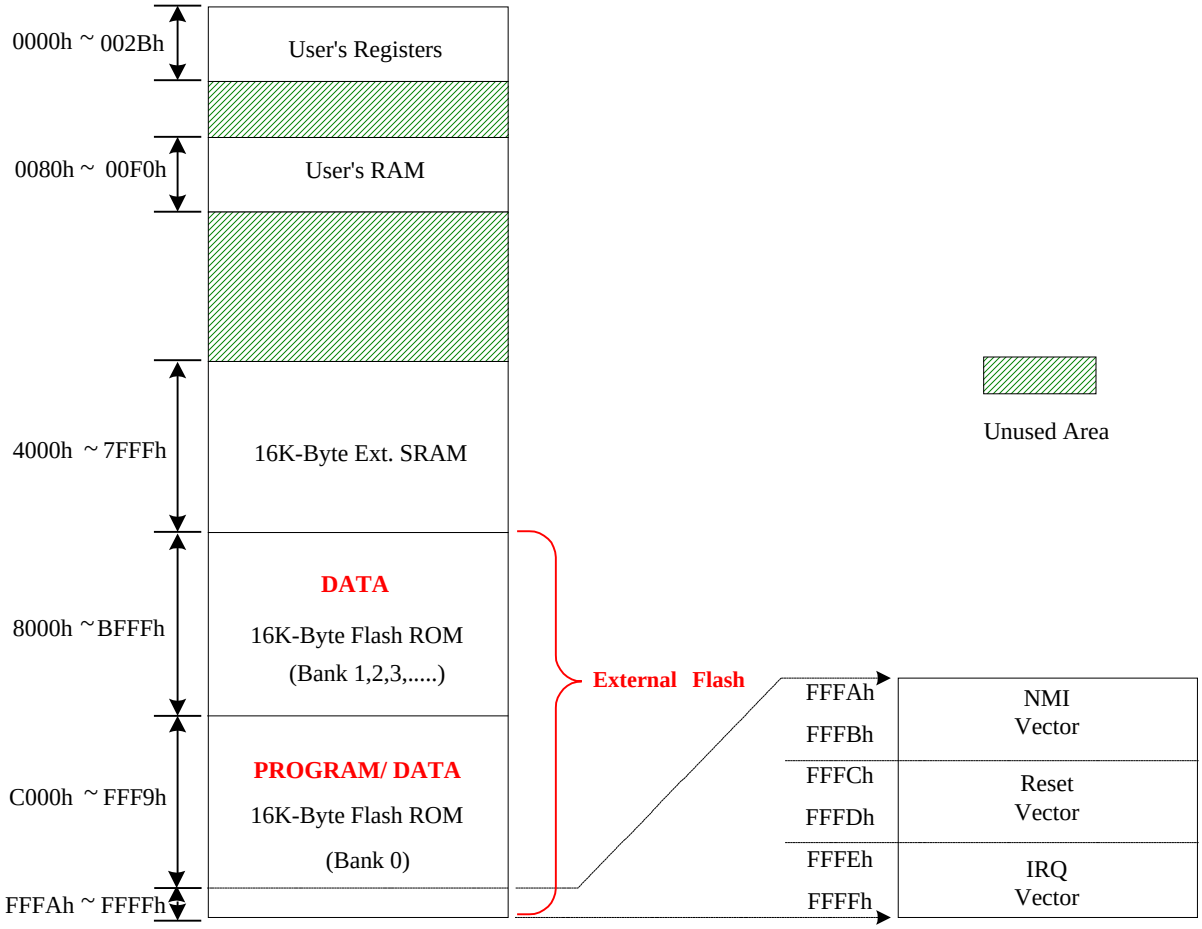


Figure 6-1

7. Registers Description

Table 7-1

Address	Register	7	6	5	4	3	2	1	0	R/W
00h	NMI_MK	TM1	TM2	PT1	PT2	TM3	WTD	0	0	R/W
01h	NMI_ST	TM1	TM2	PT1	PT2	TM3	WTD	REV.	REV.	R/W
02h	INT_MK	TM1	TM2	PT1	PT2	TM3	TB-2K	TB-500	TB-62	R/W
03h	INT_ST	TM1	TM2	PT1	PT2	TM3	TB-2K	TB-500	TB-62	R/W
04h	TM1_H	0	0	0	0	D11	D10	D9	D8	R/W
05h	TM1_L	D7	D6	D5	D4	D3	D2	D1	D0	R/W
06h	TM2_H	0	0	0	0	D11	D10	D9	D8	R/W
07h	TM2_L	D7	D6	D5	D4	D3	D2	D1	D0	R/W
08h	TM3_H	0	0	0	0	D11	D10	D9	D8	R/W
09h	TM3_L	D7	D6	D5	D4	D3	D2	D1	D0	R/W
0Ah	TM1_CTL	TM1_EN	TM1_SLP_EN	TM1_WK_RST_EN	REV.	TM1_LOOP	CKS2	CKS1	CKS0	R/W
0Bh	TM2_CTL	TM2_EN	TM2_SLP_EN	TM2_WK_RST_EN	REV.	TM2_LOOP	CKS2	CKS1	CKS0	R/W
0Ch	TM3_CTL	TM3_EN	0	0	0	TM3_LOOP	CKS2	CKS1	CKS0	R/W
0Dh	PT1	D7/PWM1	D6/PWM2	D5/TX	D4/RX	D3/IR	D2	D1/TM2_CK	D0/TM1_CK	R/W
0Eh	PT1_DIR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
0Fh	PT1_MOD	D7	D6	D5	D4	D3	D2	D1	D0	R/W
10h	PT2	D7/F_CE2#	D6/M_CE#	D5/M_OE#	D4/M_WE#	D3/LCD_E	D2/LCD_RW	D1/LVD_#	D0/WR25#	R/W
11h	PT2_DIR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
12h	DAC1	D7	D6	D5	D4	D3	D2	D1	D0	W
13h	DAC2	D7	D6	D5	D4	D3	D2	D1	D0	W
14h	DAC_CTL	REV.	REV.	OE2	OE1	PWM._EN	PWM_DY50	DAC2-AUTO	DAC1-AUTO	R/W
15h	PWM	D7	D6	D5	D4	D3	D2	D1	D0	R/W
16h	FBANK	D7	D6	D5	D4	D3	D2	D1	D0	R/W
17h	PWR_CTL	PT1	PT2	STOP_SYSCLK	STOP_XCLK	DP_SLP.	USR_DIV_CKSEL	FL2_SEL	SYS_SLP	R/W
18h	RST_STS	POR	RST#	WTD	S/W	IO	SYS_UR	UR	0	R/W
19h	CLK_CTL	CPU_CK2	CPU_CK1	CPU_CK0	LCD_HISPD.	PWM_CKSEL	LVD_EN	LVD_S1	LVD_S0	R/W
1Ah	MISC_CTL1	MEM_HISPD	EXT_WR25	EXT_PWM	EXT_LVD	WR25_ACT	EXT_LCD	EXT_MEM	FL_CTL	R/W
1Bh	MISC_CTL2	WDT_EN	WTD_LOOP	0	0	WTD_RST_EN	S/W_RST_EN	IR-EN	IR-DAT	R/W
1Ch	I/O_R	R7	R6	R5	R4	R3	R2	R1	R0	R/W
1Dh	I/O_I	I7	I6	I5	I4	I3	I2	I1	I0	R/W
1Eh	CLR_NMI	TM1	TM2	PT1	PT2	TM3	WTD	Clear $01 bit1	Clear $01 bit0	W
1Fh	CLR_INT	TM1	TM2	PT1	PT2	TM3	TB-2K	TB-500	TB-62	W
20h	I/O_INT	PT2_H_CK	PT2_L_CK	PT1_H_CK	PT1_L_CK	PT2_H_EN	PT2_L_EN	PT1_H_EN	PT1_L_EN	R/W
21h	I/O_INT&WK_MD	PT2_H_MD1	PT2_H_MD0	PT2_L_MD1	PT2_L_MD0	PT1_H_MD1	PT1_H_MD0	PT1_L_MD1	PT1_L_MD0	R/W
22h	I/O_WK_MD	REV.	REV.	REV.	REV.	PT2_H_MD	PT2_L_MD	PT1_H_MD	PT1_L_MD	R/W
23h	PT2_MOD	D7	D6	D5	D4	D3	D2	D1	D0	R/W
24h	F_CTL2	--	--	--	--	REV.	REV.	REV.	REV.	W
24h	F_CTL2	0	0	0	LVD	EXT_OPT	FL_S2	FL_S1	FL_S0	R
25h	EXT_IO	--	--	--	--	--	--	--	--	W
26h	LCD(1)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
27h	LCD(2)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
28h	RXR	D7	D6	D5	D4	D3	D2	D1	D0	R

28h	TXR	D7	D6	D5	D4	D3	D2	D1	D0	W
29h	BAUD	D7	D6	D5	D4	D3	D2	D1	D0	W
2AH	UR_CTL	TX_INT_EN	RX_INT_EN	REV.	UR_EN	UR_TX_INV	UR_RX_INV	IR_MD1	IR_MD0	R/W
2Bh	UR_ST	TX_EMPT	RX_RDY	URWK_EN	URWK_RST_EN	--	--	--	--	R/W

[REG 00h]: NMI Mask Register

Bit	Description	Reset	Default	Access
7	Timer 1 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
6	Timer 2 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
5	Port 1 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
4	Port 2 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
3	Timer 3 NMI Enable 0: Disable 1: Enable	0h	0h	R/W
2	Watch Dog NMI Enable 0: Disable 1: Enable	0h	0h	R/W
1-0	Not Used	0h	0h	R

Example:

```
LDA   #34h
STA   00h        ; Permit Port1, Port2 and WDT to produce NMI interrupt.
```

[REG 01h]: NMI Status Register

Bit	Description	Reset	Default	Access
7	Timer 1 NMI Indicate	0h	0h	R/W
6	Timer 2 NMI Indicate	0h	0h	R/W
5	Port 1 NMI Indicate	0h	0h	R/W
4	Port 2 NMI Indicate	0h	0h	R/W
3	Timer 3 NMI Indicate	0h	0h	R/W
2	Watch Dog NMI Indicate	0h	0h	R/W
1-0	Reserved	--	--	R/W

Example1:

```
LDA   #01h       ; Can be used to diagnose the source of NMI interrupt.
```

Example2:

```
LDA   #00h
STA   01h        ; To eliminate the interrupt indication of NMI.
```

[REG 02h]: INT Mask Register

Bit	Description	Reset	Default	Access
7	Timer 1 INT Enable 0: Disable 1: Enable	0h	0h	R/W
6	Timer 2 INT Enable 0: Disable 1: Enable	0h	0h	R/W
5	Port 1 INT Enable 0: Disable 1: Enable	0h	0h	R/W
4	Port 2 INT Enable 0: Disable 1: Enable	0h	0h	R/W
3	Timer 3 INT Enable 0: Disable 1: Enable	0h	0h	R/W
2	2KHz Time Base INT Enable	0h	0h	R/W
1	500Hz Time Base INT Enable	0h	0h	R/W
0	62Hz Time Base INT Enable	0h	0h	R/W

Example:

```
LDA    #30h
STA    02h          ; Permit Port1 and Port2 to produce INT interrupt.
```

[REG 03h]: INT Status Register

Bit	Description	Reset	Default	Access
7	Timer 1 INT Indicate	0h	0h	R/W
6	Timer 2 INT Indicate	0h	0h	R/W
5	Port 1 INT Indicate	0h	0h	R/W
4	Port 2 INT Indicate	0h	0h	R/W
3	Timer 3 INT Indicate	0h	0h	R/W
2	2KHz Time Base INT Indicate	0h	0h	R/W
1	500Hz Time Base INT Indicate	0h	0h	R/W
0	62Hz Time Base INT Indicate	0h	0h	R/W

Example1:

```
LDA    03h          ; Can be used to diagnose the source of INT interrupt.
```

Example2:

```
LDA    #00h
STA    03h          ; To eliminate the interrupt indication of INT.
```

[REG 04h]: Timer 1 Count_H Register

Bit	Description	Reset	Default	Access
7-4	Not Used	0h	0h	R
3-0	Timer 1 Down Count Data – High Byte	Xh	Xh	R/W

[REG 05h]: Timer 1 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 1 Down Count Data – Low Byte	Xh	Xh	R/W

Example:

```
LDA   #03h
STA   04h        ; Set Time1counter's High-Byte (Bit 11-8)at 03h.
LDA   #78h
STA   05h        ; Set Time1 counter's Low-Byte (Bit 7-0) at 78h.
                 ; Set Time1 counter at 378h.
```

[REG 06h]: Timer 2 Count_H Register

Bit	Description	Reset	Default	Access
7-4	Not Used	0h	0h	R
3-0	Timer 2 Down Count Data – High Byte	Xh	Xh	R/W

[REG 07h]: Timer 2 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 2 Down Count Data – Low Byte	Xh	Xh	R/W

Example:

```
LDA   #03h
STA   06h        ; Set Time2 counter's High-Byte (Bit 11-8) at 03h.
LDA   #BBh
STA   07h        ; Set Time2 counter's Low-Byte (Bit 7-0) at BBh.
                 ; Set Time2 counter at 3BBh.
```

[REG 08h]: Timer 3 Count_H Register

Bit	Description	Reset	Default	Access
7-4	Not Used	0h	0h	R
3-0	Timer 3 Down Count Data – High Byte	Xh	Xh	R/W

[REG 09h]: Timer 3 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 3 Down Count Data – Low Byte	Xh	Xh	R/W

Example:

```
LDA   #03h
STA   08h        ; Set Time3counter's High-Byte (Bit 11-8) at 03h.
LDA   #FFh
STA   09h        ; Set Time3 counter's Low-Byte (Bit 7-0) at FFh.
                 ; Set Time3 counter at 3FFh.
```

[REG 0Ah]: Timer 1 Control Register

Bit	Description	Reset	Default	Access
7	Timer 1 Enable or Timer 1 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 1 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 1 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
4	Reserved	0h	0h	R/W
3	Timer 1 Loop Control 0: Disable 1: Enable	0h	0h	R/W

2-0	Timer 1 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source 0 0 0 USR_DIV_CLK /2 0 0 1 USR_DIV_CLK /4 0 1 0 USR_DIV_CLK /2^8 0 1 1 USR_DIV_CLK /2^12 1 0 0 USR_DIV_CLK /2^16 1 0 1 USR_DIV_CLK /2^20 1 1 0 32768Hz 1 1 1 External I/O Port (PT1_0)	0h	0h	R/W

Example:

```
LDA   #C0h
STA   0Ah        ; Let Timer 1be Enable/Start→ Timer 1 only Count once.
                 ; Timer 1's Clock Source set at USR_DIV_CLK/2.
```

[REG 0Bh]: Timer 2 Control Register

Bit	Description	Reset	Default	Access
7	Timer 2 Enable or Timer 2 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 2 wakeup enable from sleep mode 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
4	Reserved	0h	0h	R/W
3	Timer 2 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 2 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source 0 0 0 USR_DIV_CLK/2 0 0 1 USR_DIV_CLK/4 0 1 0 USR_DIV_CLK/2^8 0 1 1 TIMER 1 Output 1 0 0 USR_DIV_CLK /2^16 1 0 1 USR_DIV_CLK /2^20 1 1 0 32768Hz 1 1 1 External I/O Port (PT1_1)	0h	0h	R/W

Example:

```
LDA   #62h
STA   0Bh        ; Set Timer 2 wakeup/Reset enable.
                 ; Set Timer 2's Clock Source at USR_DIV_CLK/2^8
```

[REG 0Ch]: Timer 3 Control Register

Bit	Description	Reset	Default	Access
7	Timer 3 Enable or Timer 3 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6-4	Not Used	0h	0h	R

3	Timer 3 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 3 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source --- 0 0 0 USR_DIV_CLK/2 0 0 1 USR_DIV_CLK/2^4 0 1 0 USR_DIV_CLK/2^8 0 1 1 USR_DIV_CLK/2^12 1 0 0 USR_DIV_CLK/2^14 1 0 1 USR_DIV_CLK /2^17 1 1 0 USR_DIV_CLK /2^20 1 1 1 32768Hz	0h	0h	R/W

Example:

```
LDA   #09h
STA   0Ch        ; Let Timer 3 Loop Control be Enable→ Timer 2 keep counting.
                 ; Let Timer 3 Clock Source be USR_DIV_CLK/2^4.
LDA   #89h
STA   0Ch        ; Timer 3 start Count.
```

[REG 0Dh]: Port 1 Data Register

Bit	Description	Reset	Default	Access
7	Output Data to Port 1 or Input from Port 1 This bit is also as the output of PWM1 when PWM enable (REG-1Ah bit5 = '1').	0h	0h	R/W
6	Output Data to Port 1 or Input from Port 1 This bit is also as the output of PWM2 when PWM enable (REG-1Ah bit5 = '1').	0h	0h	R/W
5	Output Data to Port 1 or Input from Port 1 This bit is also as the output of User UART TX when user UART enable (REG-2Ah bit4 == '1').	0h	0h	R/W
4	Output Data to Port 1 or Input from Port 1 This bit is also as the input of User UART RX when user UART enable (REG-2Ah bit4 == '1').	0h	0h	R/W
3	Output Data to Port 1 or Input from Port 1 This bit is also as the output of IR when user IR enable (REG-1Bh bit1 = '1').	0h	0h	R/W
2	Output Data to Port 1 or Input from Port 1	0h	0h	R/W
1	Output Data to Port 1 or Input from Port 1 This bit is also as the input of TM2 clock source when REG-0Bh bit2-0 == '111'	0h	0h	R/W
0	Output Data to Port 1 or Input from Port 1 This bit is also as the input of TM1 clock source when REG-0Ah bit2-0 == '111'	0h	0h	R/W

Note: If the Port1 is output mode then the read access date is from the register 0Dh. If the Port1 is input mode the read access is form Port1 I/O.

Example:

```
LDA   #FFh
STA   0Eh        ; Set port1 at output mode.
LDA   #AAh
STA   0Dh        ; Output AAh to port1 Bit7~0.
```

[REG 0Eh]: Port 1 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 1 0: Input Mode 1: Output Mode	0h	0h	R/W

Example:

```
LDA    #F0h
STA    0Eh          ; Set port1 Bit7~4 at output mode, Bit3~0 at input mode.
```

[REG 0Fh]: Port 1 Output Mode Select Register

Bit	Description	Reset	Default	Access
7-0	Select the Output Mode for CMOS or Open-Drain Mode 0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 1 Direction Control Register controls the Port1 output data.	0h	0h	R/W

Example:

```
LDA    #FFh
STA    0Eh          ; Set port1 at output mode.

LDA    #F0h
STA    0Fh          ; Set port1 Bit7~4 at Open-Drain output mode.
                    ; Bit3~0 is CMOS mode output.
```

[REG 10h]: Port 2 Data Register

Bit	Description	Reset	Default	Access
7	Output Data to Port 2 or Input from Port 2 This bit is also as the secondary external Flash chip select output (FL_CE2#) when using two external flash.	0h	0h	R/W
6	Output Data to Port 2 or Input from Port 2 This bit is also as the external memory chip select output (MEM_CE#) when external memory decoder enabled (REG-1Ah bit1= '1'). The external memory is decoded when CPU access from $4000 to $7FFF.	0h	0h	R/W
5	Output Data to Port 2 or Input from Port 2 This bit is also as the external memory output enable (MEM_OE#) when external memory decoder selected (REG-1Ah bit1= '1').	0h	0h	R/W
4	Output Data to Port 2 or Input from Port 2 This bit is also as the external memory write enable (MEM_WE#) when external memory decoder selected (REG-1Ah bit1= '1').	0h	0h	R/W
3	Output Data to Port 2 or Input from Port 2 This bit is also as the output of external LCD chip select (LCD_E) when external LCD enabled (REG-1Ah bit2= '1'). The external LCD is decoded at REG$26 & $27.	0h	0h	R/W
2	Output Data to Port 2 or Input from Port 2 This bit is also as the output of external LCD R/W (LCD_RW) when external LCD enabled (REG-1Ah bit2= '1').	0h	0h	R/W
1	Output Data to Port 2 or Input from Port 2 This bit is also as the output of LVD indicated (LVD#) when external LVD enabled (REG-1Ah bit4= '1').	0h	0h	R/W

0	Output Data to Port 2 or Input from Port 2 This bit is also as the output of REG$25 write signal (WE25) when external REG$25 write enabled (REG-1Ah bit6= '1').	0h	0h	R/W

Note: If the Port2 is output mode then the read access date is from the register 0Dh. If the Port2 is input mode then the read access is form Port2 I/O.

Example:

```
LDA   #FFh
STA   11h      ; Set port2 Bit7~0 at output mode.
LDA   #55h
STA   10h      ; Output 55h to port2 Bit7~0.
```

[REG 11h]: Port 2 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	Select the Output or Input Mode of Port 2 0: Input Mode 1: Output Mode	0h	0h	R/W

Example:

```
LDA   #F0h
STA   11h      ; Set port2 Bit7~4 at output mode, Bit3~0 at input mode.
```

[REG 12h]: DAC 1 Data Register

Bit	Description	Reset	Default	Access
7-0	8-Bit DAC 1 Output Data	0h	0h	W

Example:

```
LDA   #18h
STA   14h      ; Set DAC1 Enable
LDA   #80h
STA   12h      ; Output 80h to DAC1→ Output middle current.
```

[REG 13h]: DAC 2 Data Register

Bit	Description	Reset	Default	Access
7-0	8-Bit DAC 2 Output Data	0h	0h	W

Example:

```
LDA   #28h
STA   14h      ; Set DAC2 Enable
LDA   #FFh
STA   13h      ; Output FFh to DAC2→ Output maximum current.
```

[REG 14h]: DAC Control Register

Bit	Description	Reset	Default	Access
7-6	Reserved	0h	0h	R/W
5	DAC 2 Output Enable 0: Disable 1: Enable	0h	0h	R/W
4	DAC 1 Output Enable 0: Disable 1: Enable	0h	0h	R/W

3	PWM Enable 0: Disable 1: Enable	1h	1h	R/W
2	PWM Duty Control 0: 100 Duty Cycle 1: 50 Duty Cycle	0h	0h	R/W
1-0	Reserved	0h	0h	R/W

Example:

```
LDA   #00h
STA   14h          ; Set DAC1, DAC2 Disable.
```

[REG 15h]: PWM Data Register

Bit	Description	Reset	Default	Access
7-0	8-bit PWM Data	0h	0h	R/W

Example:

```
LDA   #0Ch
STA   14h          ; Set DAC at PWM mode.
LDA   #28h
STA   15h          ; Set PWM Enable, produce 50% Duty cycle's PWM pulse.
```

[REG 16h]: Flash ROM Bank Select Register

Bit	Description	Reset	Default	Access
7-0	Embedded Flash ROM Bank Select for Normal or ISP Mode Bit7 6 5 4 3 2 1 0 Bank Select 0 0 0 0 0 0 0 0 Bank 0 0 0 0 0 0 0 0 1 Bank 1 0 0 0 0 0 0 1 0 Bank 2 0 0 0 0 0 0 1 1 Bank 3	0h	0h	R/W

Example:

```
LDA   #01h
STA   16h          ; Choose Flash's Bank1.
```

[REG 17h]: Power Saving and Reset Control Register

Bit	Description	Reset	Default	Access
7	Port 1 Tri-state 0: Normal Mode 1: Power Saving Mode (Tri-state)	0h	0h	R/W
6	Port 2 and TXD Tri-state 0: Normal Mode 1: Power Saving Mode (Tri-state)	0h	0h	R/W
5	System Clock (7.3728MHz) On/Off Control 0: Enable 1: Disable	0h	0h	R/W

4	X'tal-Oscillator (32768Hz) On/Off Control 0: Enable 1: Disable	0h	0h	R/W
3	Deep Sleep Mode Control 0: Normal 1: Enter Sleep Mode In this mode, the Divisor is off and only 32768Hz X'tal, Timer1 and Timer2 wakeup circuit are active. But the Wakeup with Reset function is inhibited. This bit must used to go with bit0	0h	0h	R/W
2	User's Divisor Clock Select (USR_DIV_CKSEL) 0: USR_DIV_CLK = System Clock (7.3728MHz) Normally, it's set to "0" when system is in RUN1 Mode. 1: USR_DIV_CLK = Oscillator-Oscillator (32768Hz) Normally, it's set to "1" when system is in RUN2 Mode.	0h	0h	R/W
1	One or Two External Flash Option. This bit is used to indicate the external Flash number. This bit is read only. 0: Two External Flash 1: One External Flash	1h	1h	R
0	Sleep Mode Control 0: Normal Mode 1: Enter Sleep Mode In this mode, the Divisor is off and only 32768Hz X'tal, Timer1, Timer2, I/O wakeup and UART wakeup circuit are active.	0h	0h	R/W

Example:

```
LDA    #D1h
STA    17h          ; Port1, Port2 into power saving mode.
                    ; Set Oscillator-Oscillator is disable.
                    ; Set Enter Sleep Mode.
```

[REG 18h]: Reset Status Register

Bit	Description	Reset	Default	Access
7	Power On Reset Indicate	1h	0h	R/W
6	RESET (RST#) Pin Reset Indicate	0h	0h	R/W
5	Watch-Dog Reset Indicate	0h	0h	R/W
4	Software Reset Indicate	0h	0h	R/W
3	I/O Wake Up Reset Indicate	0h	0h	R/W
2	UART RX Wake Up Reset Indicate	0h	0h	R/W
1-0	Not Used	0h	0h	R

Example:

```
LDA    18h          ; Identification of Reset source.
```

[REG 19h]: Clock Control Register

Bit	Description	Reset	Default	Access

7-5	CPU Clock Select Bit7 Bit6 Bit5 Low Speed CPU Clock 0 0 0 7.3MHz **RUN1 Mode** 0 0 1 7.3MHz **RUN1 Mode** 0 1 0 7.3MHz **RUN1 Mode** 1 0 0 7.3MHz/2 **RUN1 Mode** 1 0 1 7.3MHz/4 **RUN1 Mode** 1 1 0 7.3MHz/8 **RUN1 Mode** 1 1 1 32768Hz **RUN1 Mode** --- 0 1 1 32768Hz **RUN2 Mode** In RUN2 mode, the UART, IrDA and PWM are available.	0h	0h	R/W
4	Hi-Speed Control for External LCD Decoder 0: Low Speed, add two delay cycle 1: High Speed, add one delay cycle	0h	0h	R/W
3	PWM Clock Select 0: 7.2Khz 1: Timer-3 Output	0h	0h	R/W
2	LVD Enable Control 0: Disable 1: Enable	0h	0h	R/W
1-0	LVD Voltage Select Bit1 Bit0 Detected Voltage --- 0 0 3V 0 1 2.8V 1 0 2.6V 1 1 2.4V If the LVD enabled, the bit4 of register $24 will indicate the status of LVD.	0h	0h	R/W

Example:

```
LDA   #E4h
STA   19h        ; Set CPU clock is 32768Hz.
                 ; Set LVD is Enable and voltage select 3V.
```

[REG 1Ah]: Misc. Control Register (I)

Bit	Description	Reset	Default	Access
7	Hi-Speed Control for External Flash or Memory 0: Low Speed, add one delay cycle 1: High Speed	0h	0h	R/W
6	External REG$25 Write Signal Control This bit is used to control the output of REG$25 write signal. If set high, then the Port2 bit0 is defined as the output of REG$25 write. 0: Disable 1: Enable	0h	0h	R/W

5	PWM Output Control This bit is used to control the output of PWM. If set high, then the Port1 bit7 is defined as the output of PWM1 and Port1 bit6 is defined as the PWM2. 0: PWM output disable 1: PWM output enable	0h	0h	R/W
4	LVD Output Control This bit is used to control the output of LVD. If set high, then the Port2 bit1 is defined as the output of LVD. 0: Disable LVD output 1: Enable LVD Output	0h	0h	R/W
3	External REG$25 Write Signal Active Control This bit is used to control the active state of REG$25 write signal. If set low, then the Port2 bit0 which defined as the output of REG$25 Write is active low. 0: Active Low. 1: Active High	0h	0h	R/W
2	External LCD Driver Control. This bit is used to control the external LCD Driver interface enable or disable. If set high, then the Port2 bit3~2 are defined as LCD Driver interface signals. 0: Disable, 1: Enable PT2_3 → LCD_E PT2_2 → LCD_RW	0h	0h	R/W
1	External Memory Control. This bit is used to control the external memory interface enable or disable. If set high, then the Port2 bit6~4 are defined as memory interface signals. 0: Disable, 1: Enable PT2_6 → MEM_CE# PT2_5 → MEM_OE# PT2_4 → MEM_WE#	0h	0h	R/W
0	Flash Chip Control. This bit is used to control to decoder of external flash. 0: Select Flash1, FL_CE# is active. 1: Select Flash2, FL_CE2# is active.	0h	0h	R/W

Example:

```
LDA    #20h
STA    1Ah          ; Set PWM output enable
```

[REG 1Bh]: Misc. Control Register (2)

Bit	Description	Reset	Default	Access
7	Watch Dog Enable 0: Disable 1: Enable	0h	0h	R/W
6	Watch Dog Loop Control 0: Disable 1: Enable	0h	0h	R/W
5-4	Not Used	0h	0h	R
3	Watch Dog Reset Enable 0: Disable 1: Enable	0h	0h	R/W

2	Software Reset 0: Disable 1: Reset CPU, Write this bit high will cause CPU Reset. This bit will be clear automatically after reset	0h	0h	R/W
1	IR Enable 0: Disable 1: Enable	0h	0h	R/W
0	IR Data	0h	0h	R/W

Example1:

```
LDA   #80h
STA   1Bh          ; Set Watch Dog Enable.
```

Example2:

```
LDA   #04h
STA   1Bh          ; Set Watch Dog Reset Enable.
```

[REG 1Ch]: I/O Resistor Control Register

Bit	Description	Reset	Default	Access
7-6	PT2 High Nibble Resistor Select Bit7 Bit6 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 None	0h	0h	R/W
5-4	PT2 Low Nibble Resistor Select Bit5 Bit4 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 None	0h	0h	R/W
3-2	PT1 High Nibble Resistor Select Bit3 Bit2 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 Non	0h	0h	R/W
1-0	PT1 Low Nibble Resistor Select Bit1 Bit0 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 None	0h	0h	R/W

Example:

```
LDA   #00h
STA   1Ch          ; Set Port1, Port2 resistor select is pull up 5K ohm.
```

REG 1Dh]: I/O Driving Current Control Register

Bit	Description	Reset	Default	Access
7-6	PT2 High Nibble Current Select Bit7 Bit6 Current Mode --- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W
5-4	PT2 Low Nibble Current Select Bit5 Bit4 Current Mode --- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W
3-2	PT1 High Nibble Current Select Bit3 Bit2 Current Mode --- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W
1-0	PT1 Low Nibble Current Select Bit1 Bit0 Current Mode --- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W

Example:

```
LDA    #00h
STA    1Ch          ; Set Port1, Port2 current select is Tri-state.
```

[REG 1Eh]: Clear NMI Status Register

Bit	Description	Reset	Default	Access
7	Clear Timer 1 NMI Indicate 1: Clear	--	--	W
6	Clear Timer 2 NMI Indicate 1: Clear	--	--	W
5	Clear Port 1 NMI Indicate 1: Clear	--	--	W
4	Clear Port 2 NMI Indicate 1: Clear	--	--	W
3	Clear Timer 3 NMI Indicate 1: Clear	--	--	W
2	Clear Watch Dog NMI Indicate 1: Clear	--	--	W
1-0	Reserved	--	--	W

Example:

```
LDA    #FCh
STA    1Eh          ; Clear Port1, Port2, Timer1, Timer2, Timer3 and WDT NMI Indicate.
```

[REG 1Fh]: Clear INT Status Register

Bit	Description	Reset	Default	Access
7	Clear Timer 1 INT Indicate 1: Clear	--	--	W
6	Clear Timer 2 INT Indicate 1: Clear	--	--	W
5	Clear Port 1 INT Indicate 1: Clear	--	--	W
4	Clear Port 2 INT Indicate 1: Clear	--	--	W
3	Clear Timer 3 INT Indicate 1: Clear	--	--	W
2	Clear 2KHz Time Base INT Indicate 1: Clear	--	--	W
1	Clear 500Hz Time Base INT Indicate 1: Clear	--	--	W
0	Clear 62Hz Time Base INT Indicate 1: Clear	--	--	W

Example:

```
LDA    #F8h
STA    1Fh          ; Clear Time1,Time2,Time3,Port1,andPort2 NMI Indicate.
```

[REG 20h]: I/O Interrupt Control Register

Bit	Description	Reset	Default	Access
7	PT2 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
6	PT2 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
5	PT1 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
4	PT1 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
3	PT2 High Nibble Interrupt or Wakeup 0: Disable 1: Enable	0h	0h	R/W
2	PT2 Low Nibble Interrupt or Wakeup 0: Disable 1: Enable	0h	0h	R/W
1	PT1 High Nibble Interrupt or Wakeup 0: Disable 1: Enable	0h	0h	R/W
0	PT1 Low Nibble Interrupt or Wakeup 0: Disable 1: Enable	0h	0h	R/W

Example:

```
LDA    #0Ch
STA    20h          ; PT2 Interrupt or Wakeup are selected.
```

[REG 21h]: I/O Interrupt/Wakeup Mode Select Register

Bit	Description	Reset	Default	Access
7-6	PT2 High Nibble Mode Select Bit7 Bit6 Mode --- 0 0 Rising-Edge Trigger 0 1 Falling-Edge Trigger 1 0 Reserved 1 1 Level Change Trigger (1) (2) **Level Change Trigger (1):** (0000) → Setup (0000) → (0000) → (0001) Trigger → (0101) → (1111) → (0000) Return → (0100) Trigger **Level Change Trigger (2):** (0000) → Setup (0000) → (0000) → (0001) Trigger → (0101) Trigger → (0101) → (0100) Trigger → (0000) Trigger	0h	0h	R/W
5-4	PT2 Low Nibble Mode Select Bit5 Bit4 Mode --- 0 0 Rising-Edge Trigger 0 1 Falling-Edge Trigger 1 0 Reserved 1 1 Level Change Trigger (1) (2)	0h	0h	R/W
3-2	PT1 High Nibble Mode Select Bit3 Bit2 Mode --- 0 0 Rising-Edge Trigger 0 1 Falling-Edge Trigger 1 0 Reserved 1 1 Level Change Trigger (1) (2)	0h	0h	R/W
1-0	PT1 Low Nibble Mode Select Bit1 Bit0 Mode --- 0 0 Rising-Edge Trigger 0 1 Falling-Edge Trigger 1 0 Reserved 1 1 Level Change Trigger (1) (2)	0h	0h	R/W

Example:

```
LDA   #1Fh
STA   21h        ; Select PT2 High Nibble is Rising-Edge Trigger , Low-Nibble is
                 ; Falling-Edge trigger And PT1 is Level Change Trigger (1) (2).
```

[REG 22h]: I/O Wakeup Reset Control Register

Bit	Description	Reset	Default	Access
7-4	Reserved	0h	0h	R/W
3	PT2 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W

2	PT2 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
1	PT1 High Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W
0	PT1 Low Nibble Wakeup Reset 0: Wakeup CPU Only 1: Wakeup & Cause Reset	0h	0h	R/W

Example:

```
LDA    #0Ch
STA    22h          ; PT2 Wakeup & Cause Reset Selected
```

[REG 23h]: Port 2 Output Mode Select Register

Bit	Description	Reset	Default	Access
7-0	Select the Output Mode for CMOS or Open-Drain Mode 0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 2 Direction Control Register controls the Port2 output data.	0h	0h	R/W

Example:

```
LDA    #00h
STA    23h          ; CMOS output selected.
```

[REG 24h]: Flash Control Register (II)

Bit	Description	Reset	Default	Access
7-5	Not Used	0h	0h	R
4	LVD Indicate. 0: Normal Voltage 1: Low Voltage Detected!	0h	0h	R
3	This bit latched the pin ROM_OE# during the hardware reset cycle. This is a reserved option for user's application	1h	1h	R
2-0	These Bits are used to indicate the external Flash Size Selected. The bit2-0 were latched from the pin BK1, A10 and A11 during the hardware reset cycle. This is a read only register and bit3 is always zero. Bit 2 Bit 1 Bit 0 FL_S2 FL_S1 FL_S0 Flash Size --- 0 0 0 : 64K-Byte 0 0 1 : 128K-Byte 0 1 0 : 256K-Byte 0 1 1 : 512K-Byte 1 0 0 : 1M-Byte 1 0 1 : 2M-Byte 1 1 0 : 4M-Byte 1 1 1 : 4M-Byte	111h	111h	R

Example:

```
LDA    #02h
```

```
STA   17h          ; One external Flash chip selected
LDA   #03h
STA   24h          ; Set external Flash size is 512K-Byte
```

[REG 25h]: External I/O

Bit	Description	Reset	Default	Access
7-0	This register is used for external I/O controller.	0h	0h	R/W

[REG 26h]: LCD Command Register

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

[REG 27h]: LCD Data Register

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

[REG 28h]: User UART Transmit Register

Bit	Description	Reset	Default	Access
7-0	UART Transmit Data	0h	0h	W

[REG 28h]: User UART Receive Register

Bit	Description	Reset	Default	Access
7-0	UART Receive Data	0h	0h	W

[REG 29h]: User UART Baud Rate Select

Bit	Description	Reset	Default	Access
7-0	UART Baud Rate	01h	01h	W

[REG 2Ah]: User UART Control Register

Bit	Description	Reset	Default	Access
7	Transmit Empty Indicate INT Enable, 1: Enable, 0:Disable	0h	0h	R/W
6	Received Data Available Indicate INT Enable, 1: Enable, 0:Disable	0h	0h	R/W
5	Reserved	--	--	--
4	User UART Enable Control 1: Enable 0: Disable, 1.843MHz Clock Stop	0h	0h	R/W
3	UART Transmitter Inverter	0h	0h	R/W
2	UART Receiver Inverter	0h	0h	R/W
1-0	UART IR Mode Select Bit1 Bit0 Mode ---------- 0 0 Normal 0 1 ASK IR 1 0 IrDA IR 1 1 IrDA IR	0h	0h	R/W

[REG 2Bh]: User UART Status Register

Bit	Description	Reset	Default	Access

7	Transmit Register Empty Indicate This bit is set when transmit complete and be clear when write a data to UART Transmit Register (REG 31h).	0h	0h	R/W
6	Received Data Available Indicate This bit is set when UART received an available data but it will not be clear when the host read the data from UART Receive Register (REG 30h).	0h	0h	R/W
5	UART RX Wake Up 0: Disable, 1: Enable	0h	0h	R/W
4	UART RX Wake Up Reset Enable 0: UART Wake Up only 1: UART Wake Up & caused Reset	0h	0h	R/W
3-0	Not Used	---	--	--

8. Function Description

8.1 System Clock

RA8900 is built in PLL circuit; therefore, an external 32.768KHz crystal can generate 7.3MHz for system clock. There are 7.3MHz and 32.768KHz for peripheral options. Figure 8-1 is the block diagram of the system clock, and Figure 8-2 is the schema for system clock.

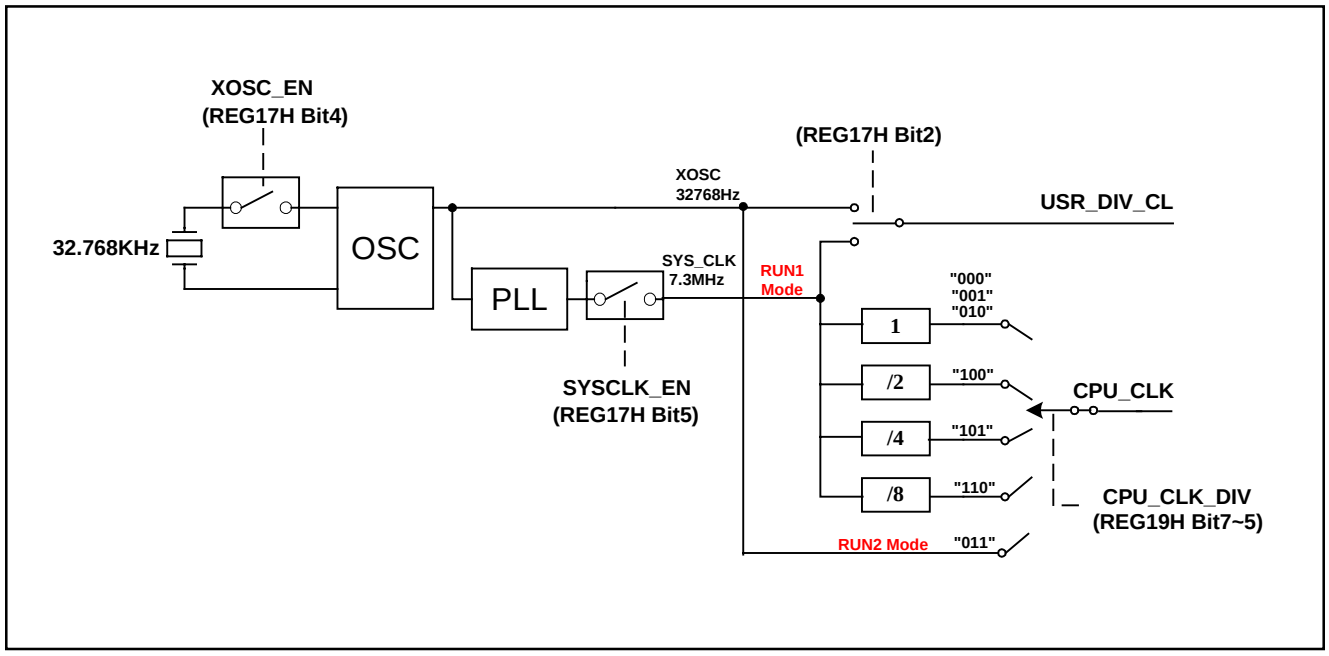


Figure 8-1 System Clock Block Diagram

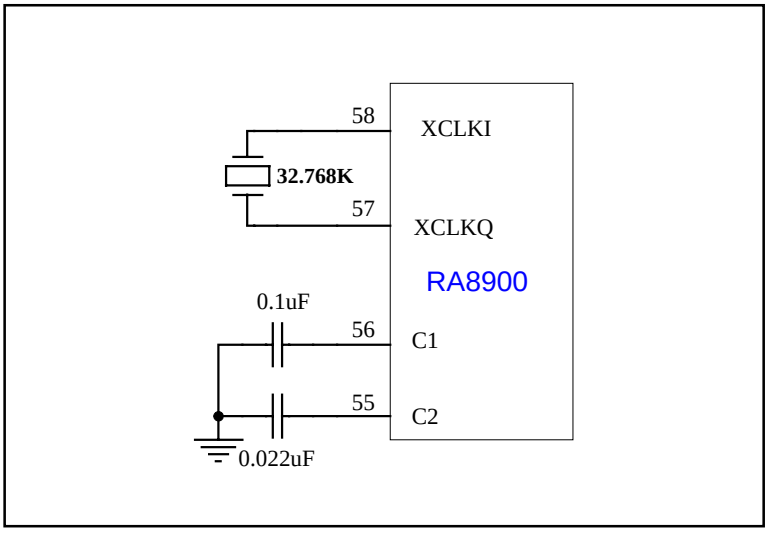


Figure 8-2 System Clock Schematic

From Figure 8-1, you will know that system clock is controlled by [REG 17h] and [REG 19h]. The descriptions of these two Registers are listed underneath, and we also provide an example program to explain how to use them.

[REG 17h]: Power Saving and Reset Control Register

Bit	Description	Reset	Default	Access
5	System Clock (7.3728MHz) On/Off Control 0: Enable 1: Disable	0h	0h	R/W
4	X'tal-Oscillator (32768Hz) On/Off Control 0: Enable 1: Disable	0h	0h	R/W
2	User's Divisor Clock Select (USR_DIV_CKSEL) 0: USR_DIV_CLK = System Clock (7.3728MHz) Normally, it's set to "0" when system is in RUN1 Mode. 1: USR_DIV_CLK = Oscillator-Oscillator (32768Hz) Normally, it's set to "1" when system is in RUN2 Mode.	0h	0h	R/W

[REG 19h]: Clock Control Register

Bit	Description	Reset	Default	Access
7-5	CPU Clock Select Bit7 Bit6 Bit5 Low Speed CPU Clock 0 0 0 7.3MHz **RUN1 Mode** 0 0 1 7.3MHz **RUN1 Mode** 0 1 0 7.3MHz **RUN1 Mode** 1 0 0 7.3MHz/2 **RUN1 Mode** 1 0 1 7.3MHz/4 **RUN1 Mode** 1 1 0 7.3MHz/8 **RUN1 Mode** 1 1 1 32768Hz **RUN1 Mode** --- 0 1 1 32768Hz **RUN2 Mode** In RUN2 mode, the UART, IrDA and PWM are available.	0h	0h	R/W

Example:

```
LDA     PWR_CTL
AND     #11000011b      ; SYS_CLK→ Enable, XOCLK->Enable,
STA     PWR_CTL         ; USR_DIV_CLK→ SYS_CLK=7.3728MHz

LDA     #10100000b      ; CPU_CLK→ 7.3MHz/4
STA     CLK_CTL

LDA     #00100100b      ; SYS_CLK Disable, USR_DIV_CLK→ XOSC=32768Hz
STA     PWR_CTL
```

8.2 CPU Operation Mode

8.2.1 Reset & Idle & Sleep & Power Saving Mode

RESET can be produced by Power On, RESET# input Low, Software Reset, Watch Dog overflow, Timer overflow, and I/O. At this time, the chip will remain RESET until a movement of Power On RESET or RESET# input High.

When it is RESET, the statuses are as following:

- Continue to oscillate or being initialed (electric power raise or Wake Up from SLEEP)
- All I/O pins (PT1、PT2) enter into high impedance condition
- Set program counter as “FFFC”
- Registers are set as initial value

Figure 8-3 below is RESET schema, and Figure 8-4 is RESET Block Diagram. The functions of other RESET will be explained in the relevant chapters.

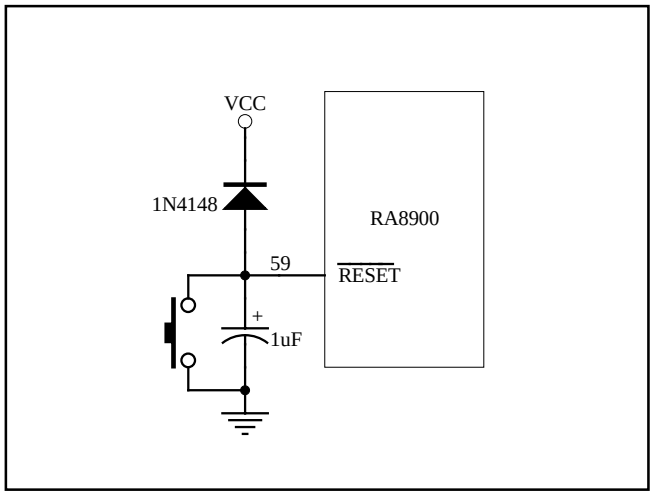


Figure 8-3 RESET Schematic

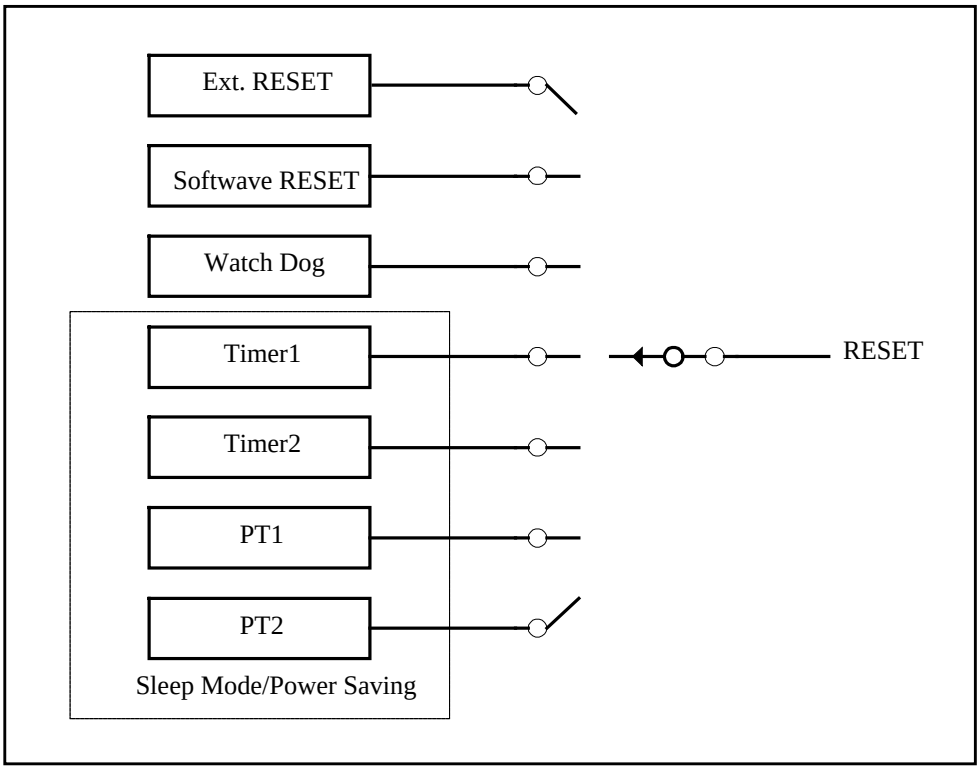


Figure 8-4 RESET Block Diagram

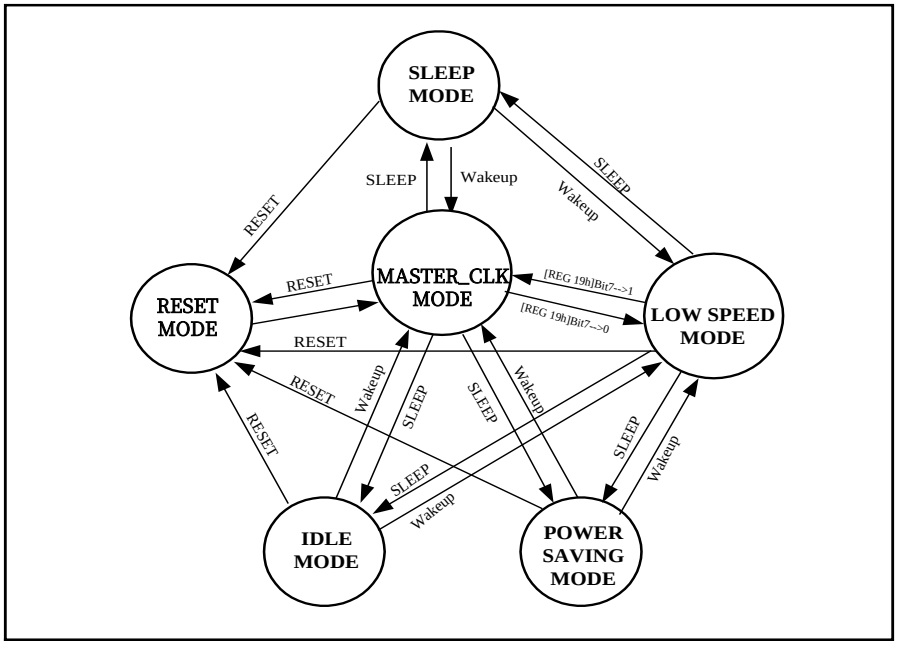


Figure 8-5 CPU Operation Diagram

POWER SAVING MODE
32786Hz OSC: stopped [REG 17h] Bit4 Xtal-Oscillator Off
PLL Stopped [REG 17h] Bit5 Disable
CPU Sleep [REG 17h] Bit0 Disable

SLEEP MODE
32786Hz OSC: oscillating [REG 17h] Bit4 Xtal-Oscillator On
PLL: turned on [REG 17h] Bit5 System Clock On
CPU: sleep mode [REG 17h] Bit0 CPU Enter Sleep

IDLE MODE
32786Hz OSC: oscillating [REG 17h] Bit4 Xtal-Oscillator On
PLL: stopped [REG 17h] Bit5 System Clock Off
CPU [REG 17h] Bit0 Enter Sleep Mode

MASTER_CLK NORMAL MODE
32786Hz OSC: oscillating [REG 17h] Bit4 Xtal-Oscillator On
PLL: turned on [REG 17h] Bit5 System Clock On
CPU: normal mode [REG 17h] Bit0 Normal Mode
CPU Clock Select [REG 19h] Bit7 --> 0

Bit7	Bit6	Bit5	CPU Clock	
0	0	0	7.3MHz	RUN1 Mode
0	0	1	7.3MHz	RUN1 Mode
0	1	0	7.3MHz	RUN1 Mode

LOW SPEED MODE
32786Hz OSC: oscillating [REG 17h] Bit4 Xtal-Oscillator On
PLL: turned on [REG 17h] Bit5 System Clock On
CPU: normal mode [REG 17h] Bit0 Normal Mode
CPU Clock Select [REG 19h] Bit7 ~5

Bit7	Bit6	Bit5	CPU Clock	
1	0	0	7.3MHz/2	RUN1 Mode
1	0	1	7.3MHz/4	RUN1 Mode
1	1	0	7.3MHz/8	RUN1 Mode
1	1	1	32768Hz	RUN1 Mode
0	1	1	32768Hz	RUN2 Mode

Table 8-1 CPU Operation Mode Setting

Note: Idle, Sleep Mode =>When set [REG 17h] bit3 (Deep Sleep Mode Control) =0 then Timer1, Timer2, I/O, External Reset and UART can Wake-up CPU clock.
When set [REG 17h] bit3 (Deep Sleep Mode Control) =1 then Timer1, Timer2 can Wake-up CPU clock. But the Wakeup with Reset function is inhibited.

Power Saving Mode=> When set [REG 17h] bit3 (Deep Sleep Mode Control) =0 then I/O and UART can Wake-up CPU clock.
When set [REG 17h] bit3 (Deep Sleep Mode Control) =1 then External Reset can Wake-up CPU clock.

Figure 8-5 is the diagram for CPU operation, and Table 8-1 is for CPU Operation Mode Setting. The flow path includes Sleep, Reset, Idle, Power Saving Mode, the flow of CPU Clock between normal and low speed, and setting Register [REG 17h, 19h]. When CPU Clock is set as low speed, the choice of speed could be made by setting [REG 19h] Bit7~5.

8.2.2 Wakeup

Table 8-2 shows the setting of Register [REG 17h] when CPU needs to be wakening up from the Sleeping, Idle, and Power Saving Mode.

WAKEUP MODE
IDLE, SLEEP WAKEUP
POWER SAVING WAKEUP
32786Hz OSC: oscillating [REG 17h] Bit4 Xtal-Oscillator On
PLL: turned on [REG 17h] Bit5 System Clock On
CPU [REG 17h] Bit0 Set Normal Mode

Table 8-2 Wakeup Operation Mode Setting

8.3 External Flash ROM

RA8900 could be used with external Flash ROM from the size of 64K Byte to 4M Byte. [REG 24h] Bit2~Bit0, three pins could select the size of the Flash ROM, (see Table 8-3). Figure 8-6 is the schema for external 512K Byte Flash ROM. From Figure 8-6 and Figure 6-1 Memory Organization, we know that A0~A13 consists a BANK=16K. BK0~BK7 controlled by [REG 16h] is for the purpose of choosing BANK. The maximum Flash ROM size is 16K*256=4M Byte.

Table 8-3 Flash Size Select

REG 24h			Flash Size
Bit 2	Bit 1	Bit 0	
FL_S2	FL_S1	FL_S0	
0	0	0	64K-Byte
0	0	1	128K-Byte
0	1	0	256K-Byte
0	1	1	512K-Byte
1	0	0	1M-Byte
1	0	1	2M-Byte
1	1	0	4M-Byte
1	1	1	4M-Byte

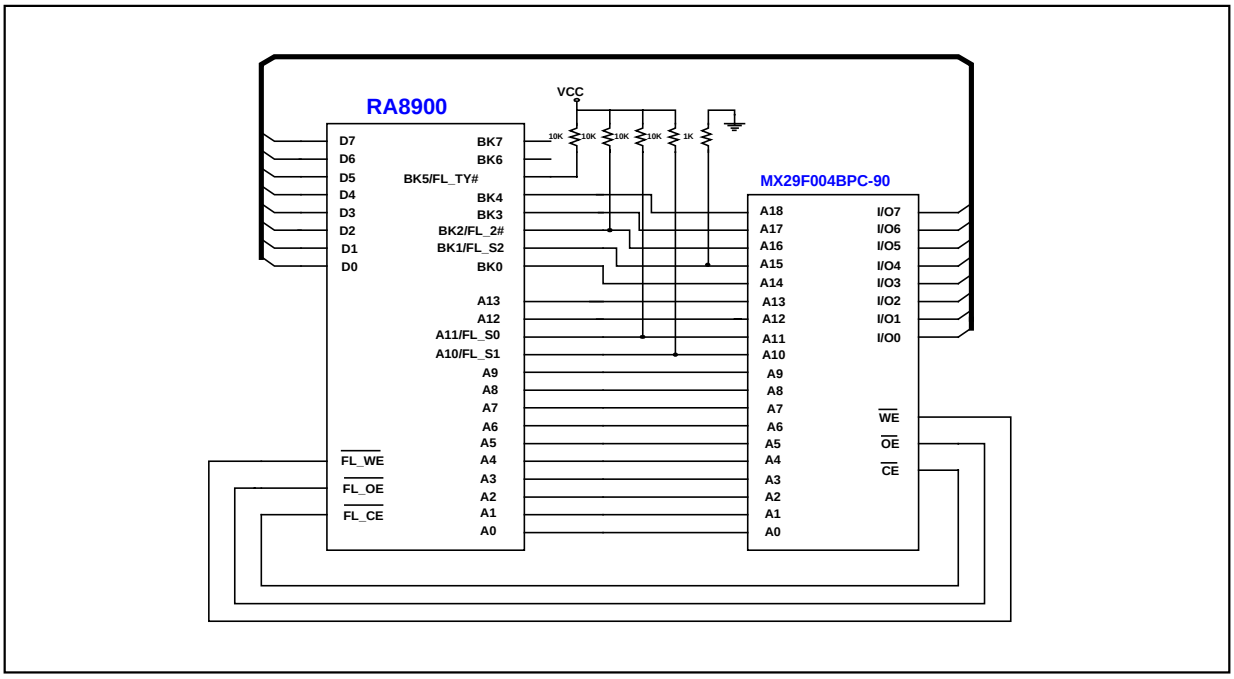


Figure 8-6 External 512K Byte Flash ROM

At the moment, RA8900 mainly supports MXIC and ATMEL Flash ROM series, and is decided by **"FL_TY"** Pin. Table 8-4 is a list of the Flash ROM IC number.

Table 8-4

[REG 24h] Bit3 FL_TY	Manufacturer	IC Number
1	AMD	29F001/29F002 29F004/29LV008B
0	ATMEL	49F001/49F002

Besides that, RA8900 provide flexibility for external Flash ROM. Users can use two Flash ROM in the same brand. Figure 8-7 is the circuit for two external 256K-Byte Flash ROM. At this moment, FL_2 pin must pull Low and corresponding [REG 16h] Bit6. Which Flash ROM acts depends on [REG 1Ah] Bit 0. There are more information below related to relevant Register setting for Flash ROM.

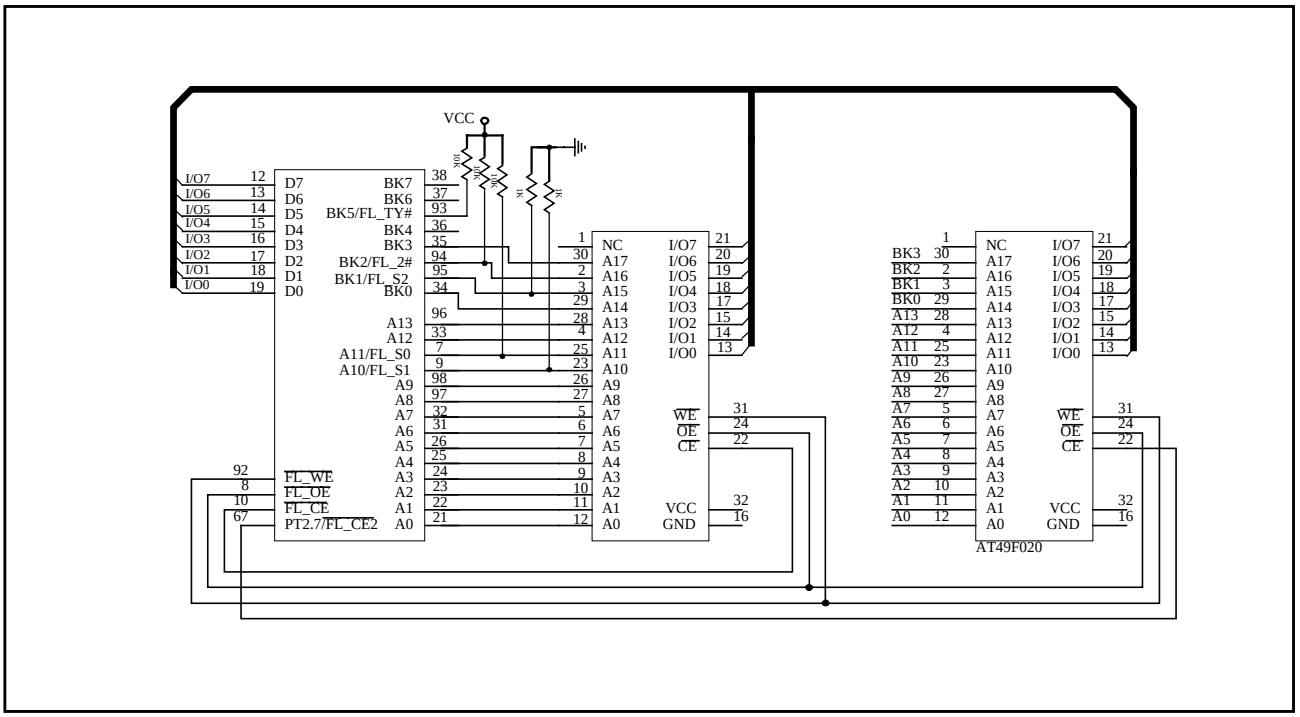


Figure 8-7 RA8900 and External 2 X 256KByte Flash ROM

[REG 16h]: Flash ROM Bank Select Register

Bit	Description	Reset	Default	Access
7-0	Embedded Flash ROM Bank Select for Normal or ISP Mode Bit7 6 5 4 3 2 1 0 Bank Select 0 0 0 0 0 0 0 0 Bank 0 0 0 0 0 0 0 0 1 Bank 1 0 0 0 0 0 0 1 0 Bank 2 0 0 0 0 0 0 1 1 Bank 3	0h	0h	R/W

[REG 17h]: Power Saving and Reset Control Register

Bit	Description	Reset	Default	Access
1	One or Two External Flash Option. This bit is used to indicate the external Flash number. This bit is read only. 0: Two External Flash 1: One External Flash	1h	1h	R

[REG 1Ah]: Misc. Control Register (I)

Bit	Description	Reset	Default	Access
0	Flash Chip Control. This bit is used to control to decoder of external flash. 0: Select Flash1, FL_CE# is active. 1: Select Flash2, FL_CE2# is active.	0h	0h	R/W

[REG 24h]: Flash Control Register (II)

Bit	Description	Reset	Default	Access
2-0	These Bits are used to indicate the external Flash Size Selected. The bit2-0 were latched from the pin BK1, A10 and A11 during the hardware reset cycle. This is a read only register and bit3 is always zero. Bit 2 FL_S2 / Bit 1 FL_S1 / Bit 0 FL_S0 / Flash Size 0 0 0 : 64K-Byte 0 0 1 : 128K-Byte 0 1 0 : 256K-Byte 0 1 1 : 512K-Byte 1 0 0 : 1M-Byte 1 0 1 : 2M-Byte 1 1 0 : 4M-Byte 1 1 1 : 4M-Byte	111h	111h	R

8.4 I/O Ports

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled. That pin may not be used as a general purpose I/O pin. PORT1 and PORT2 is 8-bit wide, bi-directional port.

The specialties of RA8900 are I/O resistor control register and I/O driving current control register, which provide the convenience for users to make a choice depend on the application. RA8900 also builds in De-bounce function, and could be set by [REG 20h] Bit7~Bit4.

[REG 0Dh]: Port 1 Data Register

Bit	Description	Reset	Default	Access
7	Input/Output or PWM2 Output	0h	0h	R/W
6	Input/Output or PWM1 Output	0h	0h	R/W
5	Input/Output or RS232 TX Output	0h	0h	R/W
4	Input/Output or RS232 RX Output	0h	0h	R/W
3	Input/Output or IR Output	0h	0h	R/W
2	Input/Output	0h	0h	R/W
1	Input/Output or Timer2 Clock Input	0h	0h	R/W
0	Input/Output or Timer1 Clock Input	0h	0h	R/W

Note: If the Port1 is output mode then the read access date is from the register 0Dh. If the Port1 is input mode the read access is form Port1 I/O.

[REG 0Eh]: Port 1 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	0: Input Mode 1: Output Mode	0h	0h	R/W

[REG 0Fh]: Port 1 Output Mode Select Register

Bit	Description	Reset	Default	Access

7-0	0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 1 Direction Control Register controls the Port1 output data.	0h	0h	R/W

[REG 10h]: Port 2 Data Register

Bit	Description	Reset	Default	Access
7	Input/Output or FL_CE2# Output	0h	0h	R/W
6	Input/Output or MEM_CE# Output	0h	0h	R/W
5	Input/Output or MEM_OE# Output	0h	0h	R/W
4	Input/Output or MEM_WE# Output	0h	0h	R/W
3	Input/Output or LCD_E Output	0h	0h	R/W
2	Input/Output or LCD_RW Output	0h	0h	R/W
1	Input/Output or LVD Output	0h	0h	R/W
0	Input/Output or WE25 Output	0h	0h	R/W

Note: If the Port2 is output mode then the read access date is from the register 0Dh. If the Port2 is input mode then the read access is form Port2 I/O.

[REG 11h]: Port 2 Direction Control Register

Bit	Description	Reset	Default	Access
7-0	0: Input Mode 1: Output Mode	0h	0h	R/W

[REG 23h]: Port 2 Output Mode Select Register

Bit	Description	Reset	Default	Access
7-0	0: CMOS Mode 1: Open-Drain Mode. In this mode, Port 2 Direction Control Register controls the Port2 output data.	0h	0h	R/W

[REG 1Ch]: I/O Resistor Control Register

Bit	Description	Reset	Default	Access
7-6	PT2 High Nibble Resistor Select Bit7 Bit6 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 None	0h	0h	R/W
5-4	PT2 Low Nibble Resistor Select Bit5 Bit4 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 None	0h	0h	R/W
3-2	PT1 High Nibble Resistor Select Bit3 Bit2 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 Non	0h	0h	R/W

1-0	PT1 Low Nibble Resistor Select Bit1 Bit0 Resistor Mode ---------- 0 0 Pull Up: 5Kohm 0 1 Pull Up: 50Kohm 1 0 Pull Low: 50Kohm 1 1 None	0h	0h	R/W

[REG 1Dh]: I/O Driving Current Control Register

Bit	Description	Reset	Default	Access
7-6	PT2 High Nibble Current Select Bit7 Bit6 Current Mode ---------- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W
5-4	PT2 Low Nibble Current Select Bit5 Bit4 Current Mode ---------- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W
3-2	PT1 High Nibble Current Select Bit3 Bit2 Current Mode ---------- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W
1-0	PT1 Low Nibble Current Select Bit1 Bit0 Current Mode ---------- 0 0 Tri-state 0 1 4mA 1 0 8mA 1 1 12mA	0h	0h	R/W

[REG 20h]: I/O Interrupt Control Register

Bit	Description	Reset	Default	Access
7	PT2 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
6	PT2 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
5	PT1 High Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W
4	PT1 Low Nibble Clock Select 0: Normal 1: Add Filter to De-bounce	0h	0h	R/W

Example**:**

```
LDA     #11111111b          ; PT1 Output
STA     PT1_DIR
LDA     #00001111b          ; PT1 Resistor None
STA     IO_R
LDA     #00000101b          ; PT1 Driving Current = 4mA
STA     IO_I
LDA     #10101010b
STA     PT1

LDA     #11110000b          ; PT2 Bit7~4 Output, Bit3~0 Input
STA     PT2_DIR
LDA     #11001111b          ; PT2 High Nibble Resistor None
STA     IO_R                ; PT2 Low Nibble Resistor : Pull Up 5Kohm
LDA     #01000000b          ; PT2 Low Nibble Filter to De-bounce Enable
STA     IO_INT
LDA     #11000000b
LDA     PT2
```

8.5 Timer

RA8900 provides three 12-Bit Timer/Counter. They are Timer1, Timer2, and Timer3, composed of two 8-bit Registers (THx, TLx).

The functions of Timer1 and Timer2 are as following:

- 12 Bits counter auto re-load.
- Down Counter type
- Wake up from Sleep Mode
- Wake up RESET
- Overflow Interrupt Once or Loop

The functions of Timer3:

- 12 Bits counter auto re-load.
- Down Counter type
- Overflow Interrupt Once or Loop

Figures below are Block Diagrams illustrating operation principles and software control methods.

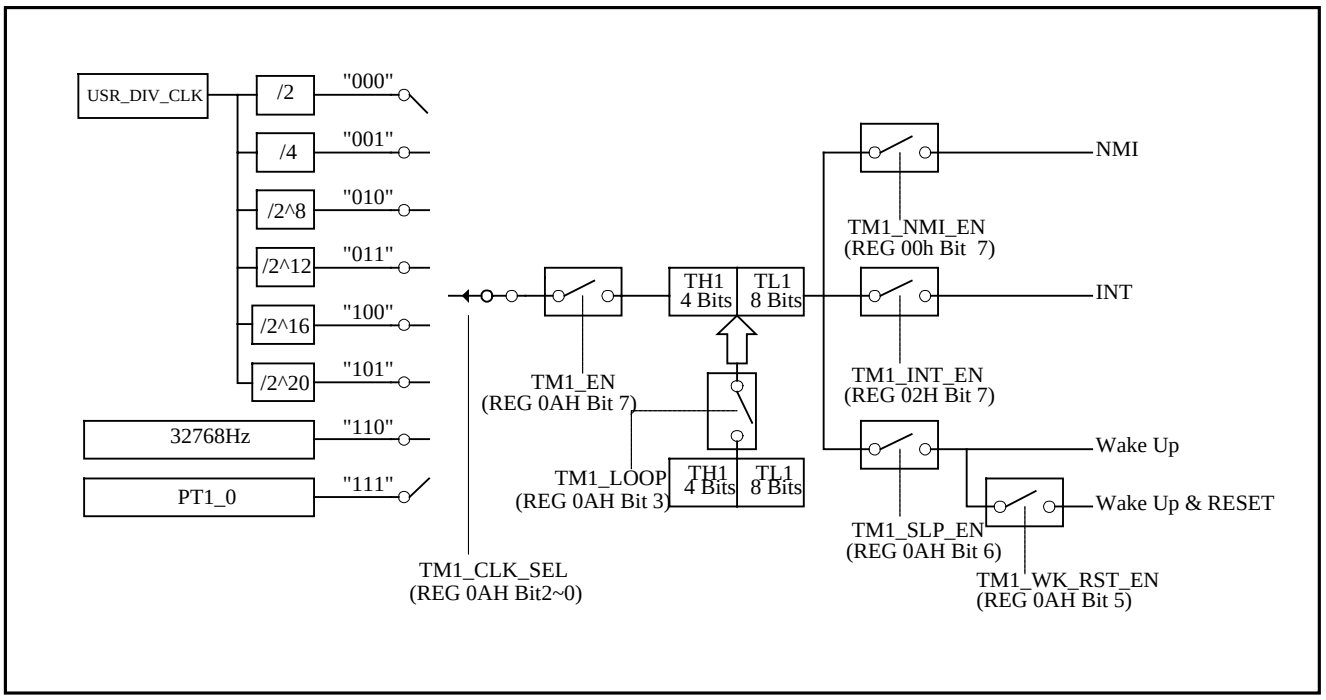


Figure 8-8 Timer1 Block Diagram

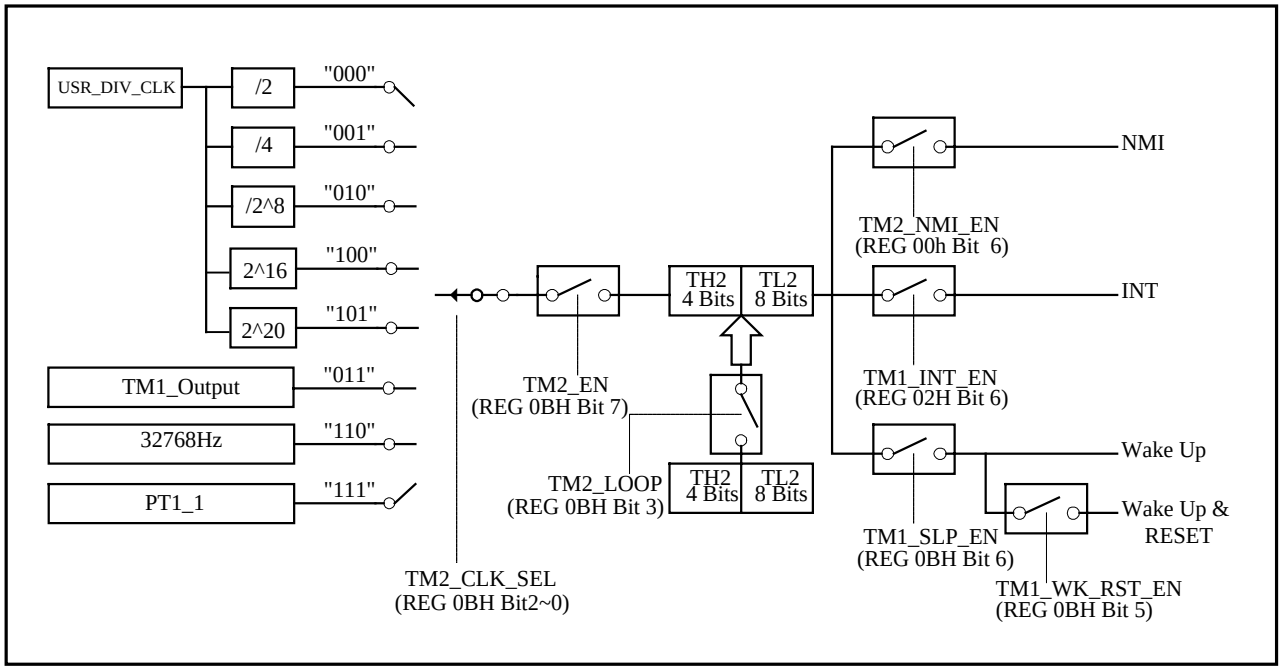


Figure 8-9 Timer2 Block Diagram

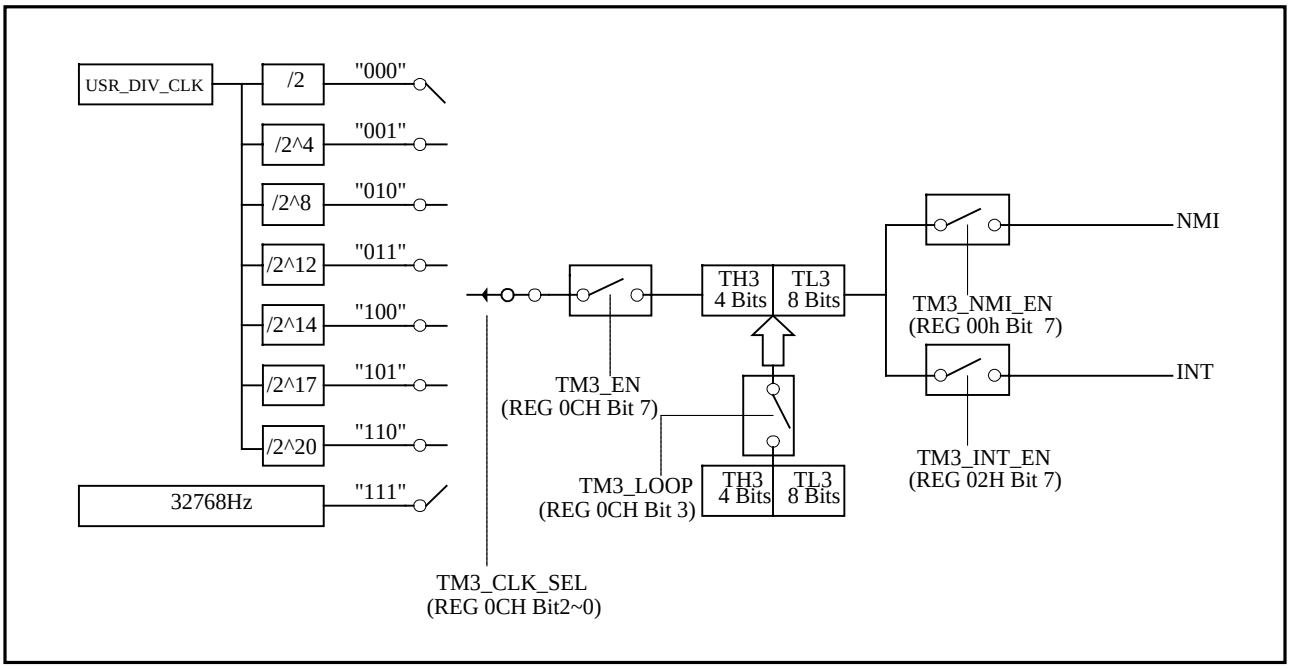
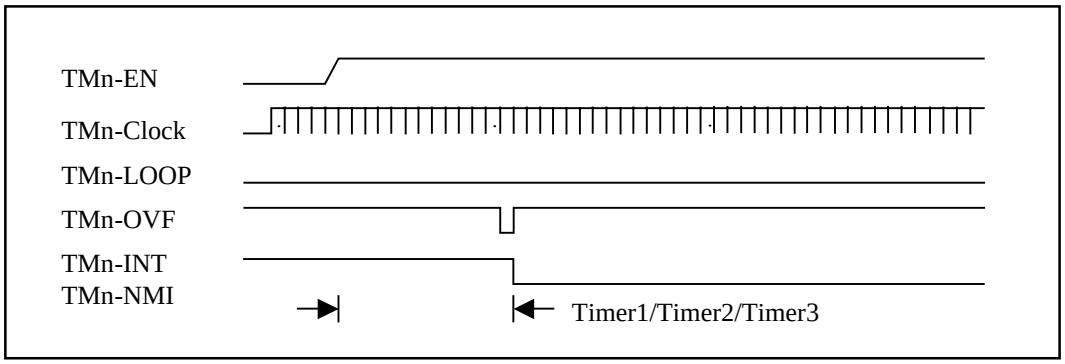


Figure 8-10 Timer3 Block Diagram



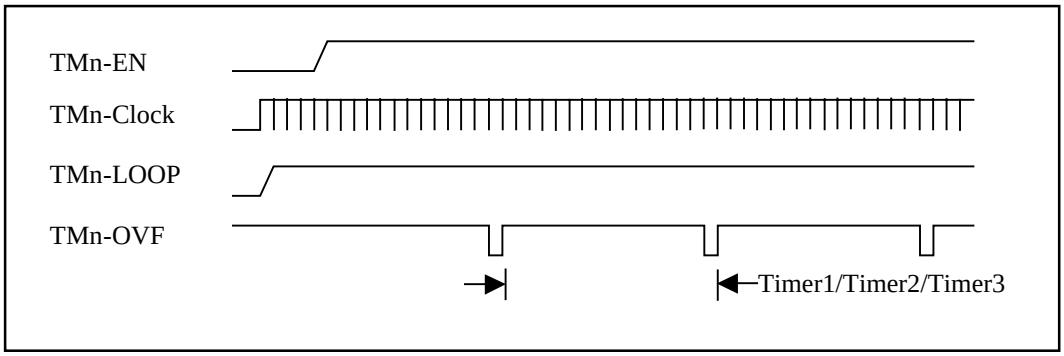


Figure 8-11 Timer Operation mode

[REG 04h]: Timer 1 Count_H Register

Bit	Description	Reset	Default	Access
3-0	Timer 1 Down Count Data – High Byte	Xh	Xh	R/W

[REG 05h]: Timer 1 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 1 Down Count Data – Low Byte	Xh	Xh	R/W

[REG 06h]: Timer 2 Count_H Register

Bit	Description	Reset	Default	Access
3-0	Timer 2 Down Count Data – High Byte	Xh	Xh	R/W

[REG 07h]: Timer 2 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 2 Down Count Data – Low Byte	Xh	Xh	R/W

[REG 08h]: Timer 3 Count_H Register

Bit	Description	Reset	Default	Access
3-0	Timer 3 Down Count Data – High Byte	Xh	Xh	R/W

[REG 09h]: Timer 3 Count_L Register

Bit	Description	Reset	Default	Access
7-0	Timer 3 Down Count Data – Low Byte	Xh	Xh	R/W

[REG 0Ah]: Timer 1 Control Register

Bit	Description	Reset	Default	Access
7	Timer 1 Enable or Timer 1 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 1 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 1 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
4	Reserved	0h	0h	R/W
3	Timer 1 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 1 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source 0 0 0 USR_DIV_CLK/2 0 0 1 USR_DIV_CLK/4 0 1 0 USR_DIV_CLK/2^8 0 1 1 USR_DIV_CLK/2^12 1 0 0 USR_DIV_CLK/2^16 1 0 1 USR_DIV_CLK/2^20 1 1 0 32768Hz 1 1 1 External I/O Port (PT1_0)	0h	0h	R/W

[REG 0Bh]: Timer 2

Bit	Description	Reset	Default	Access

7	Timer 2 Enable or Timer 2 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6	Timer 2 wakeup enable from sleep mode. 0: Disable 1: Enable	0h	0h	R/W
5	Timer 2 wakeup RESET enable 0: Disable 1: Enable	0h	0h	R/W
4	Reserved	0h	0h	R/W
3	Timer 2 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 2 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source 0 0 0 USR_DIV_CLK/2 0 0 1 USR_DIV_CLK/4 0 1 0 USR_DIV_CLK/2^8 0 1 1 TIMER 1 Output 1 0 0 USR_DIV_CLK/2^16 1 0 1 USR_DIV_CLK/2^20 1 1 0 32768Hz 1 1 1 External I/O Port (PT1_1)	0h	0h	R/W

[REG 0Ch]: Timer 3 Control Register

Bit	Description	Reset	Default	Access
7	Timer 3 Enable or Timer 3 Start 0: Disable/Stop 1: Enable/Start	0h	0h	R/W
6-4	Not Used	0h	0h	R
3	Timer 3 Loop Control 0: Disable 1: Enable	0h	0h	R/W
2-0	Timer 3 Input Clock Source Select Bit2 Bit1 Bit0 Clock Source 0 0 0 USR_DIV_CLK/2 0 0 1 USR_DIV_CLK/2^4 0 1 0 USR_DIV_CLK/2^8 0 1 1 USR_DIV_CLK/2^12 1 0 0 USR_DIV_CLK/2^14 1 0 1 USR_DIV_CLK/2^17 1 1 0 USR_DIV_CLK/2^20 1 1 1 32768Hz	0h	0h	R/W

There is an example to clarify how to use Timer:

Example**:** use Timer1 to produce interruption every 8KHz.

1/8KHz=125μs, USR_DIV_CLK=7.3728MHz, Timer1 Clock=USR_DIV_CLK/4=7.3728MHz/4
TH1=00h, TL1=125μs÷（1÷（7.3728MHz÷4））=230, TL1=E6h

```
CLI                         ; Enable all Interrupt

LDA     PWR_CTL
AND     #11111011b          ; USR_DIV_CLK=System Clock=7.3728MHz
STA     PWR_CTL

LDA     INT_MK
ORA     #10000000b          ; Timer1 INT Enable
STA     INT_MK

LDA     #00h
STA     TH1
LDA     #e6h
STA     TL1

LDA     #10001001b          ; Timer1 start, Loop Enable, Clock=USR_DIV_CLK/4
STA     TM1_CTL
```

8.6 Watch Dog

The counting period of Watch Dog timer is 2 second. Watch Dog will automatically RESET when it counts up to 2 second preventing the crash happens within the IC. If users need this function, then users need to clear Watch Dog with in 2 second. The Watch Dog could be used as general Timer, and has the function of NMI Interrupt. Figure 8-12 is the Block Diagram of the Watch Dog.

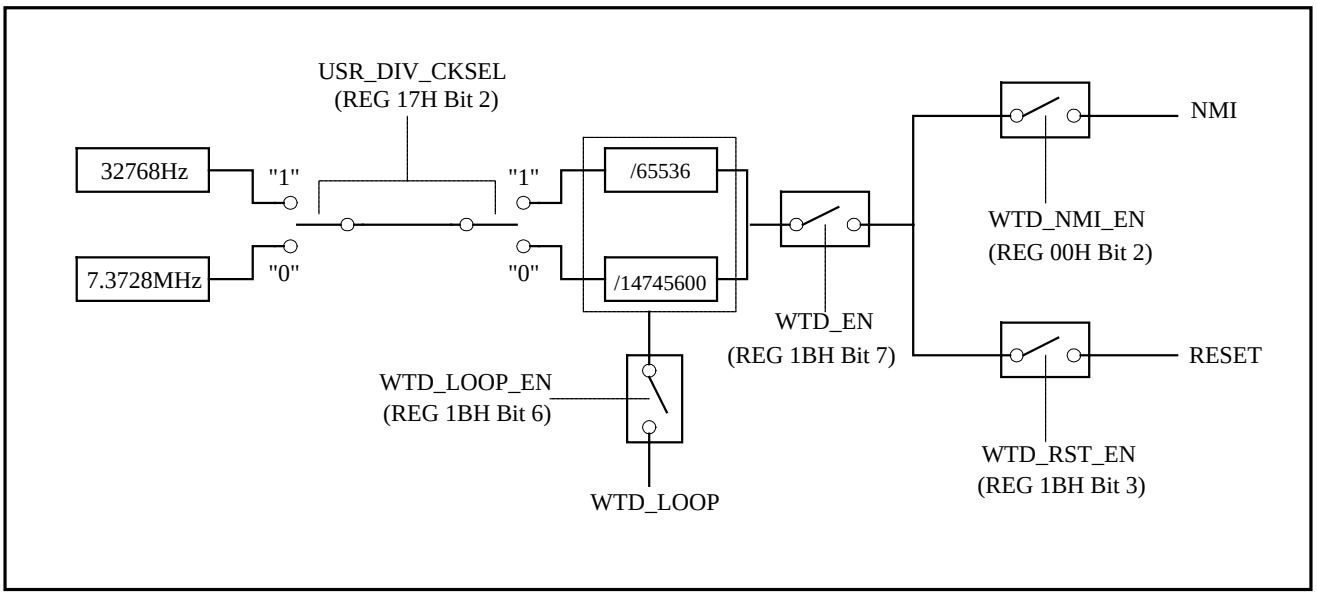


Figure 8-12 Watch Dog Block Diagram

[REG 17h]: Power Saving and Reset Control Register

Bit	Description	Reset	Default	Access
2	User's Divisor Clock Select (USR_DIV_CKSEL) 0: USR_DIV_CLK = System Clock (7.3728MHz) 1: USR_DIV_CLK = X'tal-Oscillator (32768Hz)	0h	0h	R/W

[REG 1Bh]: Misc. Control Register (2)

Bit	Description	Reset	Default	Access
7	Watch Dog Enable 0: Disable, 1: Enable	0h	0h	R/W
6	Watch Dog Loop Control 0: Disable, 1: Enable	0h	0h	R/W
3	Watch Dog Reset Enable 1: Enable 0: Disable	0h	0h	R/W

Example**:**

```
LDA     PWR_CTL
OR        #00000100b          ; USR_DIV_CLK=32768Hz
STA     PWR_CTL

LDA     MISC_CTL2
OR        #10001000b          ; Watch Dog Enable, Reset Enable
STA     MISC_CTL2

RMB7    MISC_CTL2           ; Watch Dog Disable & Clear Watch Dog
```

8.7 Interrupt

RA8900 provides six Non Mask Interrupt (NMI) and ten INT. Figure 8-13 is NMI Block Diagram, and Figure 8-14 is INT Block Diagram. Below is relevant Register [REG 00h, 01h, 02h, 03h, 1Eh, 1Fh, 2A, 2B] of Interrupt.

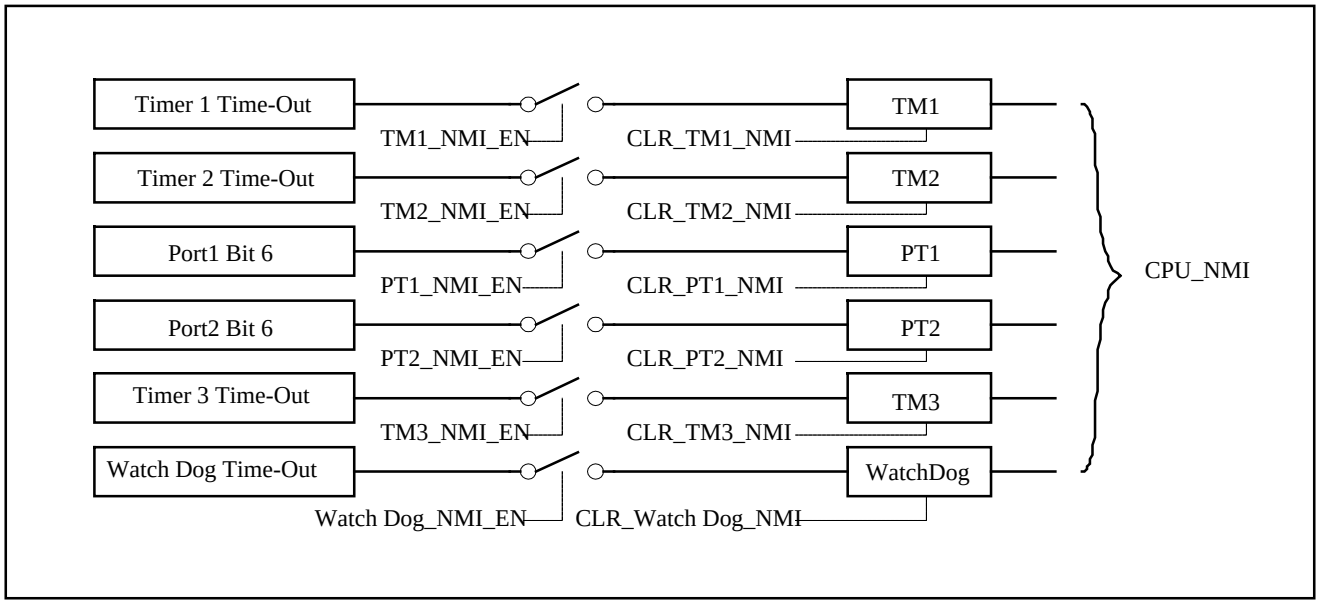


Figure 8-13 NMI Block Diagram

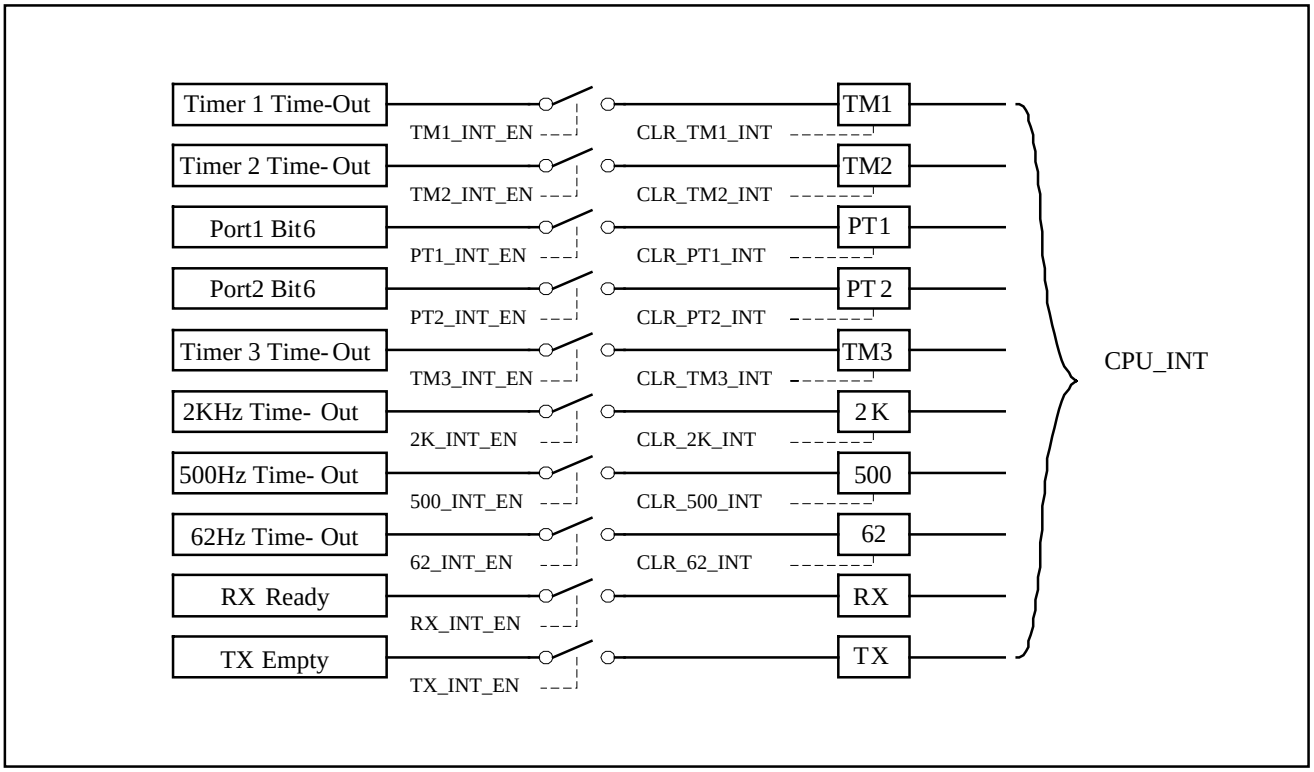


Figure 8-14 INT Block Diagram

[REG 00h]: NMI Mask Register

Bit	Description	Reset	Default	Access
7	Timer 1 NMI Enable, 1: Enable, 0: Disable	0h	0h	R/W
6	Timer 2 NMI Enable, 1: Enable, 0: Disable	0h	0h	R/W
5	Port 1 NMI Enable, 1: Enable, 0: Disable	0h	0h	R/W
4	Port 2 NMI Enable, 1: Enable, 0: Disable	0h	0h	R/W
3	Timer 3 NMI Enable, 1: Enable, 0: Disable	0h	0h	R/W
2	Watch Dog NMI Enable, 1: Enable, 0: Disable	0h	0h	R/W

[REG 01h]: NMI Status Register

Bit	Description	Reset	Default	Access
7	Timer 1 NMI Indicate	0h	0h	R/W
6	Timer 2 NMI Indicate	0h	0h	R/W
5	Port 1 NMI Indicate	0h	0h	R/W
4	Port 2 NMI Indicate	0h	0h	R/W
3	Timer 3 NMI Indicate	0h	0h	R/W
2	Watch Dog NMI Indicate	0h	0h	R/W

[REG 02h]: INT Mask Register

Bit	Description	Reset	Default	Access
7	Timer 1 INT Enable, 1: Enable, 0: Disable	0h	0h	R/W
6	Timer 2 INT Enable, 1: Enable, 0: Disable	0h	0h	R/W
5	Port 1 INT Enable, 1: Enable, 0: Disable	0h	0h	R/W
4	Port 2 INT Enable, 1: Enable, 0: Disable	0h	0h	R/W
3	Timer 3 INT Enable, 1: Enable, 0: Disable	0h	0h	R/W
2	2KHz Time Base INT Enable	0h	0h	R/W

1	500Hz Time Base INT Enable	0h	0h	R/W
0	62Hz Time Base INT Enable	0h	0h	R/W

[REG 03h]: INT Status Register

Bit	Description	Reset	Default	Access
7	Timer 1 INT Indicate	0h	0h	R/W
6	Timer 2 INT Indicate	0h	0h	R/W
5	Port 1 INT Indicate	0h	0h	R/W
4	Port 2 INT Indicate	0h	0h	R/W
3	Timer 3 INT Indicate	0h	0h	R/W
2	2KHz Time Base INT Indicate	0h	0h	R/W
1	500Hz Time Base INT Indicate	0h	0h	R/W
0	62Hz Time Base INT Indicate	0h	0h	R/W

[REG 1Eh]: Clear NMI Status Register

Bit	Description	Reset	Default	Access
7	Clear Timer 1 NMI Indicate 1: Clear	--	--	W
6	Clear Timer 2 NMI Indicate 1: Clear	--	--	W
5	Clear Port 1 NMI Indicate 1: Clear	--	--	W
4	Clear Port 2 NMI Indicate 1: Clear	--	--	W
3	Clear Timer 3 NMI Indicate 1: Clear	--	--	W
2	Clear Watch Dog NMI Indicate 1: Clear	--	--	W

[REG 1Fh]: Clear INT Status Register

Bit	Description	Reset	Default	Access
7	Clear Timer 1 INT Indicate 1: Clear	--	--	W
6	Clear Timer 2 INT Indicate 1: Clear	--	--	W
5	Clear Port 1 INT Indicate 1: Clear	--	--	W
4	Clear Port 2 INT Indicate 1: Clear	--	--	W
3	Clear Timer 3 INT Indicate 1: Clear	--	--	W
2	Clear 2KHz Time Base INT Indicate 1: Clear	--	--	W
1	Clear 500Hz Time Base INT Indicate 1: Clear	--	--	W
0	Clear 62Hz Time Base INT Indicate 1: Clear	--	--	W

[REG 2Ah]: User UART Control Register

Bit	Description	Reset	Default	Access
7	Transmit Empty Indicate INT Enable, 1: Enable, 0:Disable	0h	0h	R/W

6	Received Data Available Indicate INT Enable, 1: Enable, 0:Disable	0h	0h	R/W

[REG 2Bh]: User UART Status Register

Bit	Description	Reset	Default	Access
7	Transmit Register Empty Indicate This bit is set when transmit complete and be clear when write a data to UART Transmit Register (REG 28h).	0h	0h	R/W
6	Received Data Available Indicate This bit is set when UART received an available data but it will not be clear when the host read the data from UART Receive Register (REG 28h).	0h	0h	R/W

8.8 Universal Synchronous Asynchronous Receiver Transmitter (UART)

RA8900 builds in one set UART. [REG 28h] which includes Receive and Transmit can do read and write. Figure 8-15 is Baud Rate Clock Block Diagram. The transmission format of UART is as Figure 8-16. Besides that, UART provides three types of transmission models, such as Normal, ASK IR, IrDA IR. When CPU is during Sleep Mode, UART could be a source for Wake Up. The relevant Register [REG 28h, 29h, 2Ah, 2Bh] for UART is as below.

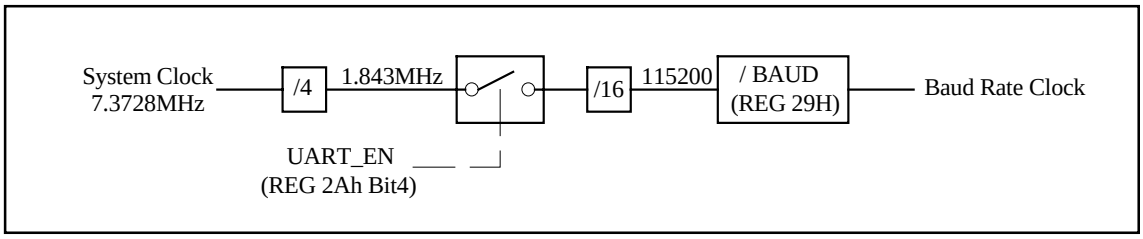


Figure 8-15 Baud Rate Clock Block Diagram

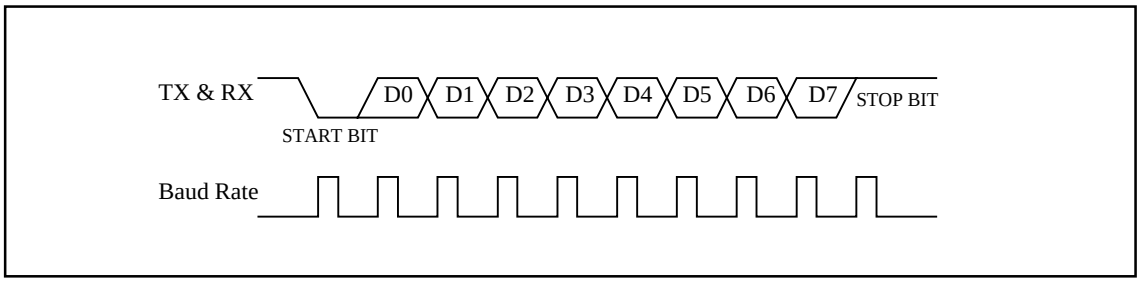


Figure 8-16 RX & TX Data Format

[REG 28h]: User UART Transmit & Receive Register

Bit	Description	Reset	Default	Access
7-0	UART Transmit Data	0h	0h	W

[REG 29h]: User UART Baud Rate Select

Bit	Description	Reset	Default	Access
7-0	UART Baud Rate	01h	01h	W

[REG 2Ah]: User UART Control Register

Bit	Description	Reset	Default	Access
7	Transmit Empty Indicate INT Enable 0:Disable 1: Enable	0h	0h	R/W
6	Received Data Available Indicate INT Enable 0:Disable 1: Enable	0h	0h	R/W
4	User UART Enable Control 0: Disable, 1.843MHz Clock Stop 1: Enable	0h	0h	R/W
3	UART Transmitter Inverter	0h	0h	R/W
2	UART Receiver Inverter	0h	0h	R/W
1-0	UART IR Mode Select Bit1 Bit0 Mode ---------- 0 0 Normal 0 1 ASK IR 1 0 IrDA IR 1 1 IrDA IR	0h	0h	R/W

[REG 2Bh]: User UART Status Register

Bit	Description	Reset	Default	Access
7	Transmit Register Empty Indicate This bit is set when transmit complete and be clear when write a data to UART Transmit Register (REG 31h).	0h	0h	R/W
6	Received Data Available Indicate This bit is set when UART received an available data but it will not be clear when the host read the data from UART Receive Register (REG 30h).	0h	0h	R/W
5	UART RX Wake Up 0: Disable, 1: Enable	0h	0h	R/W
4	UART RX Wake Up Reset Enable 0: UART Wake Up only 1: UART Wake Up & caused Reset	0h	0h	R/W

The formula of Baud Rate Clock is as following:

Baud Rate=115200/(BAUD+1) bps

Example**:**

```
LDA     #00010000b          ; UART Enable, UART IR Mode→ Normal
STA     UR_CTL
LDA     #0h                 ; Baud Rate=115200 bps
STA     BAUD

LDA     #55h
STA     UR_DATA             ; Transmit 55h
LDA     UR_DATA             ; Receive
```

8.9 Digital-to-Analog Converter (D/A) Module

RA8900 Support two 8 bit current types Digital-to-Analog Converter (D/A) Module。 The maximum output current is 5mA as well as the data is “FF”. If the data is “00” then the output current is zero. Figure 8-17 is DAC application circuit.

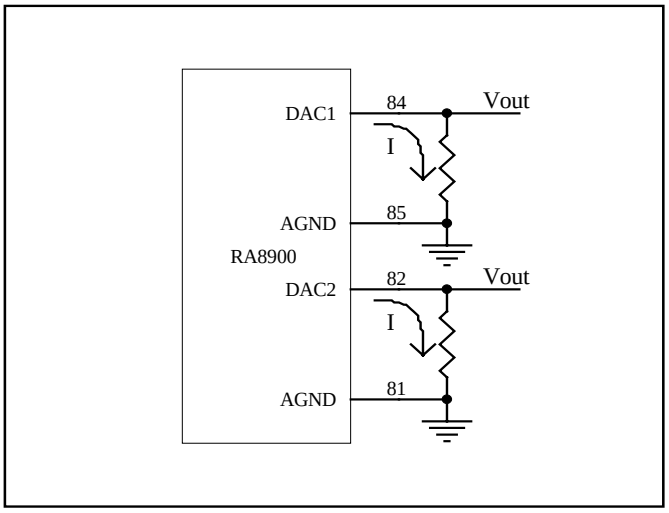


Figure 8-17 DAC Application

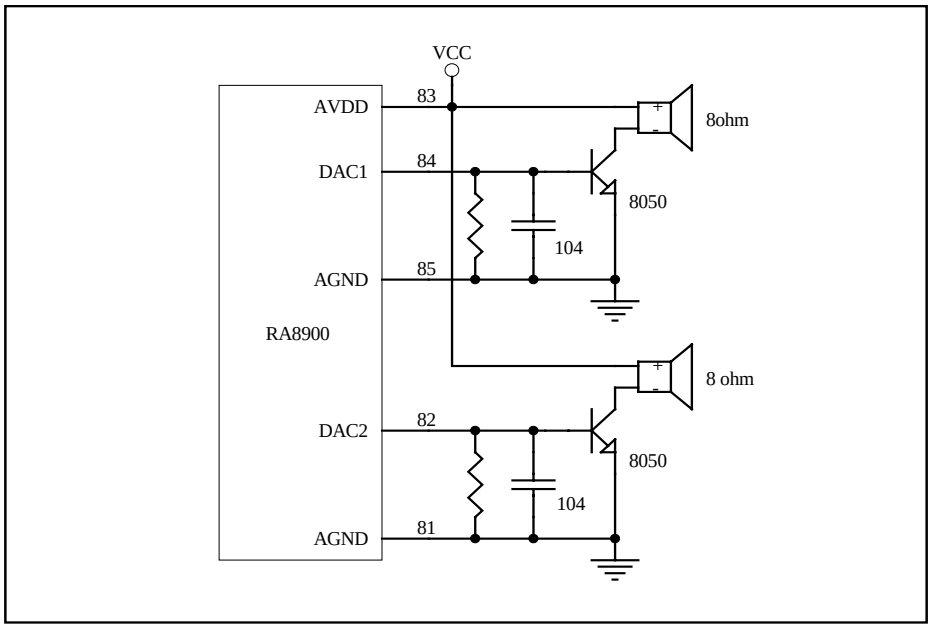


Figure 8-18 Speech Application

8.10 LCD Interface

RA8900 supports a LCD Interface, including two LCD Registers, which are LCD Command register [REG 26h] and LCD Data register [REG 27h]. The external control signal saves the effort of some simulation actions. Figure 8-19 shows the interface of RA8900 and LCD/LCM. The relevant Register [REG 26h, 27h, 1A] for LCD Interface is one the following page. There is an example to illustrate how to control LCD.

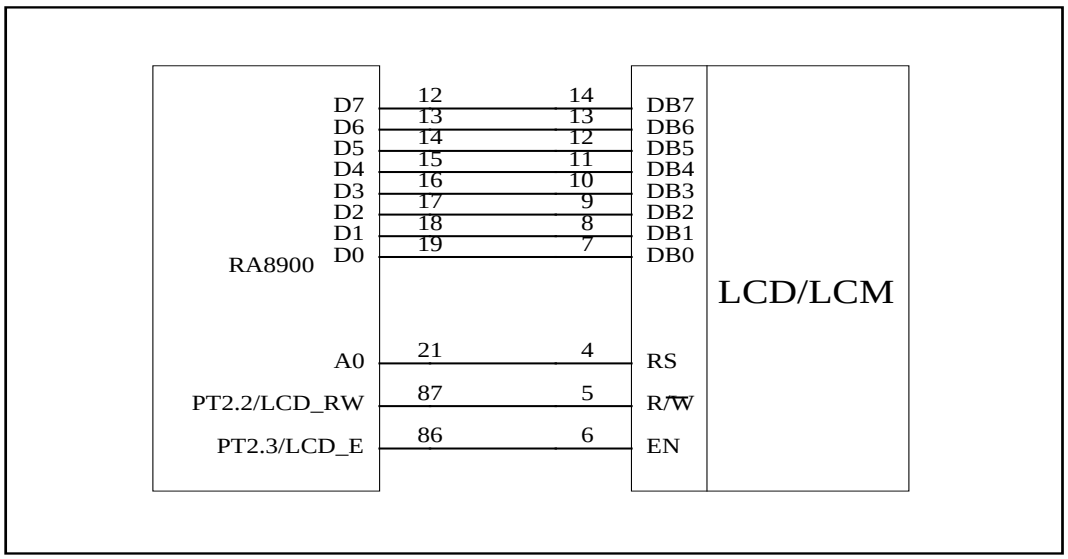


Figure 8-19 RA8900 and LCD/LCM Interface

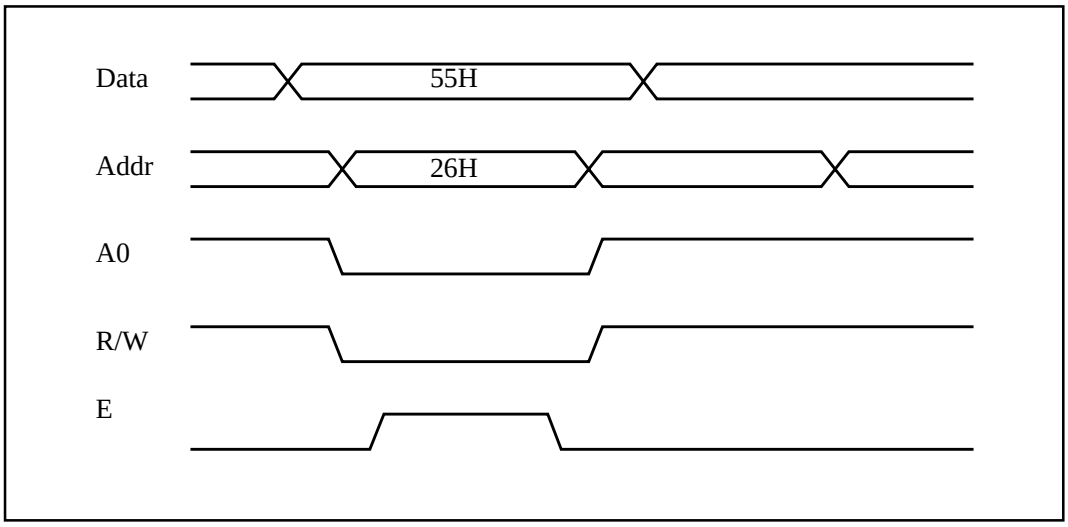


Figure 8-20 Command Write Timing

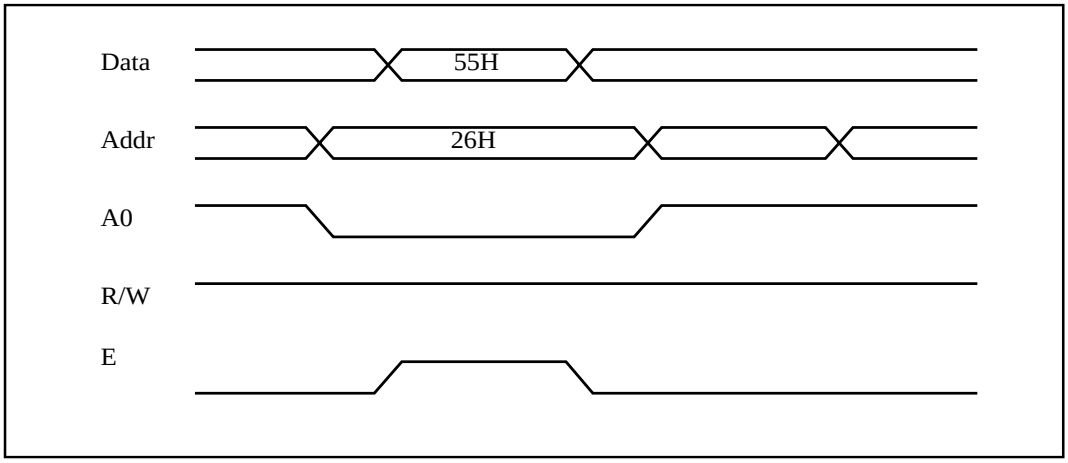


Figure 8-21 Command Read Timing

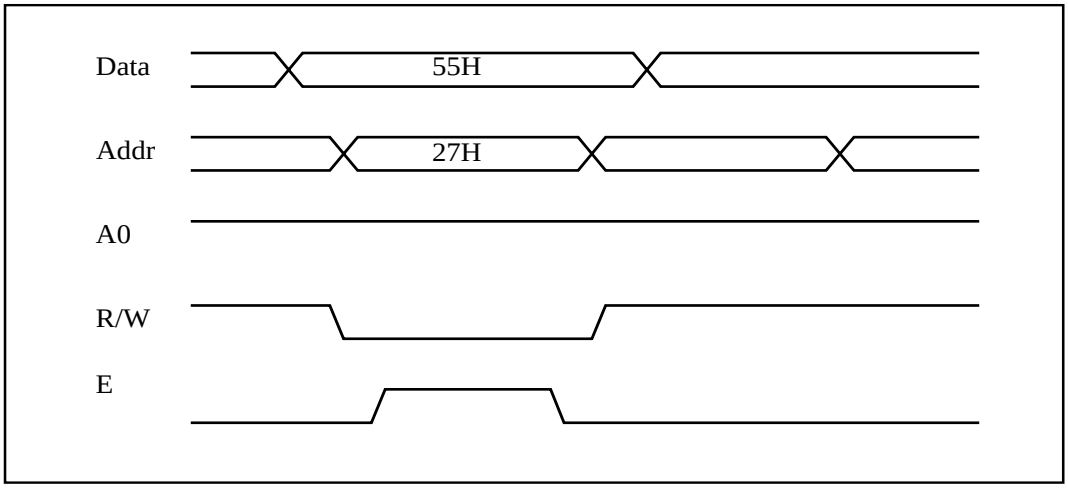


Figure 8-22 Data Write Timing

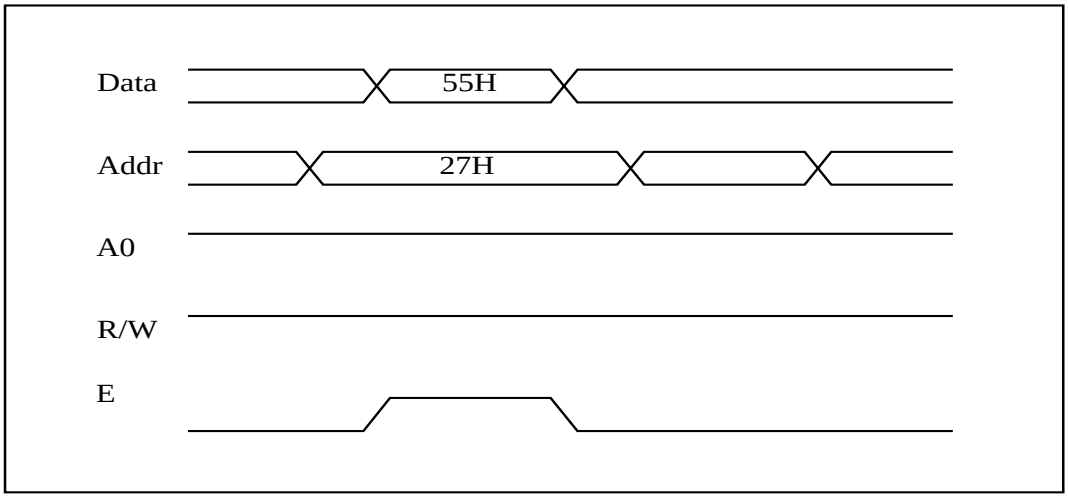


Figure 8-23 Data Read Timing

[REG 26h]: LCD Command Register

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

[REG 27h]: LCD Data Register

Bit	Description	Reset	Default	Access
7-0	This register is used for external LCD controller.	0h	0h	R/W

[REG 1Ah]: Misc. Control Register (I)

Bit	Description	Reset	Default	Access
2	External LCD Driver Control. This bit is used to control the external LCD Driver interface enable or disable. If set high, then the Port2 bit3~2 are defined as LCD Driver interface signals. 0: Disable, 1: Enable PT2_3 → LCD_E PT2_2 → LCD_RW	0h	0h	R/W

Example**:**

```
LDA     MISC_CTL1
OR        #00000100b          ; External LCD Driver Control Enable
STA     MISC_CTL1

LDA     #55h                  ; Command Write
STA     LCD_CMD

LDA     LCD_CMD               ; Command Read

LDA     #41h                  ; Data Write
STA     LCD_DATA

LDA     LCD_DATA              ; Data Read
```

8.11 PWM

When the bit3 of [REG 14h] is set to high, then the PWM mode is enable. The duty cycle of PWM output is controlled by [REG 15h] bit7~0.

Notice: When USR_DIV_CLK=XTAL (32768Hz), the PWM can't action.

Example:

```
LDA   #0Ch
STA   14h          ; Set PWM Enable.
LDA   #FFh
STA   15h          ; producing 50% Duty Cycle's PWM Pulse
```

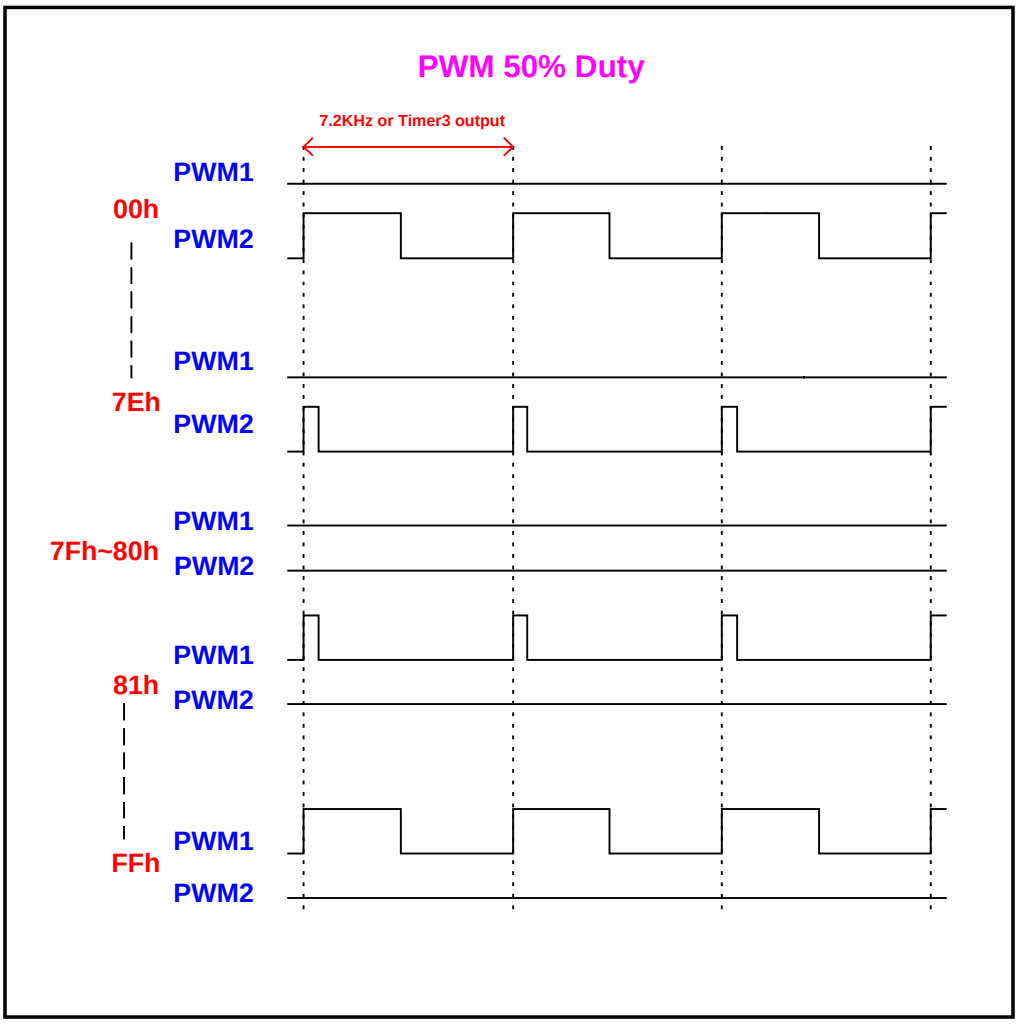


Figure 8-24 PWM 50% Duty Waveform

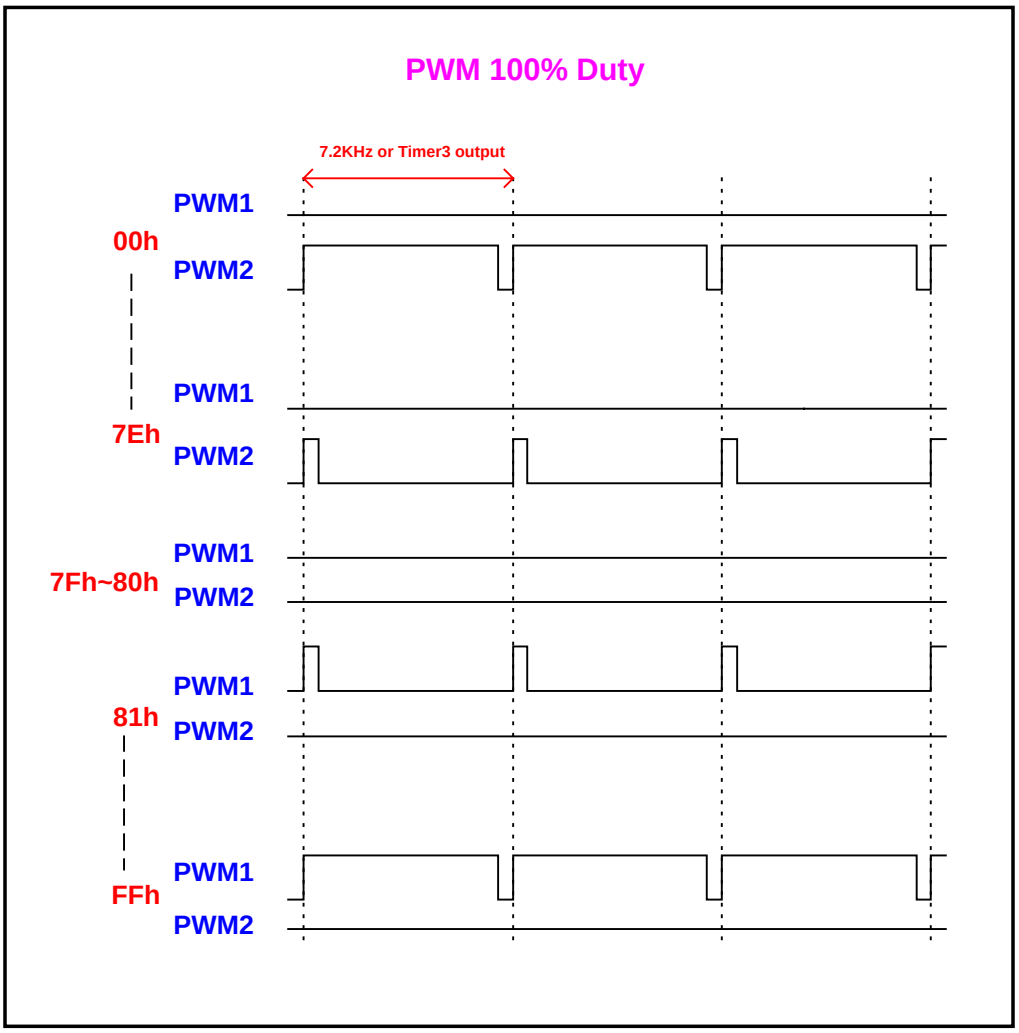


Figure 8-25 PWM 100% Duty Waveform

8.12 IR

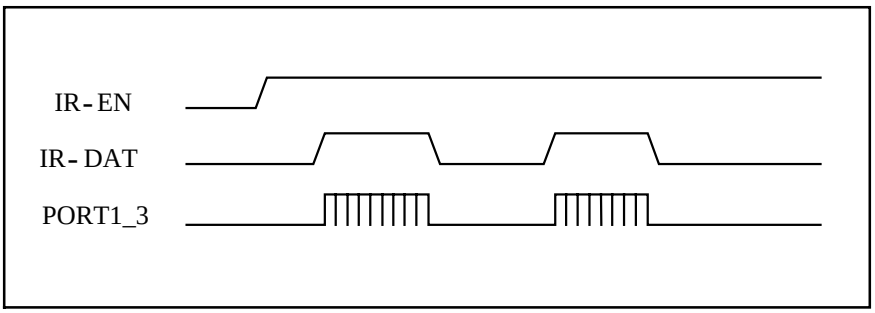


Figure 8-26 IR mode

When the bit1 of [REG 1Bh] (IR-EN) is set to high, then the IR signal is driven through the port1_3.

8.13 Low Voltage Detect (LVD)

The RA8900 builds in an integrated low-voltage detector. The supply voltage is divided and compared to the band gap reference output. If the supply voltage falls below the set voltage value, the bit4 of [REG 24h] will indicate the status of LVD. The nominal values of the low-voltage detector four points are below [REG 19h].

When the voltage is lower than the default value, then [REG 24h] Bit4 will be “1”. The signal could output through I/O, and then a warning could happen when users connect an external LED or buzzer. Figure 8-27 and 8-28 are the LVD application circuit. There is also an example following by that.

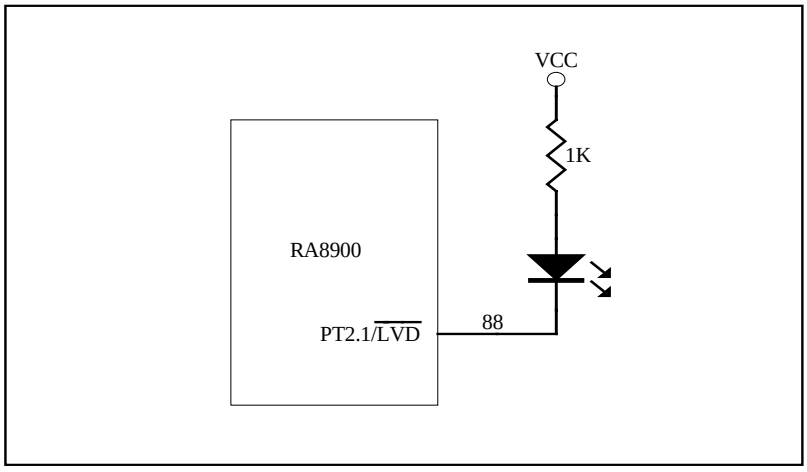


Figure 8-27 LVD Application

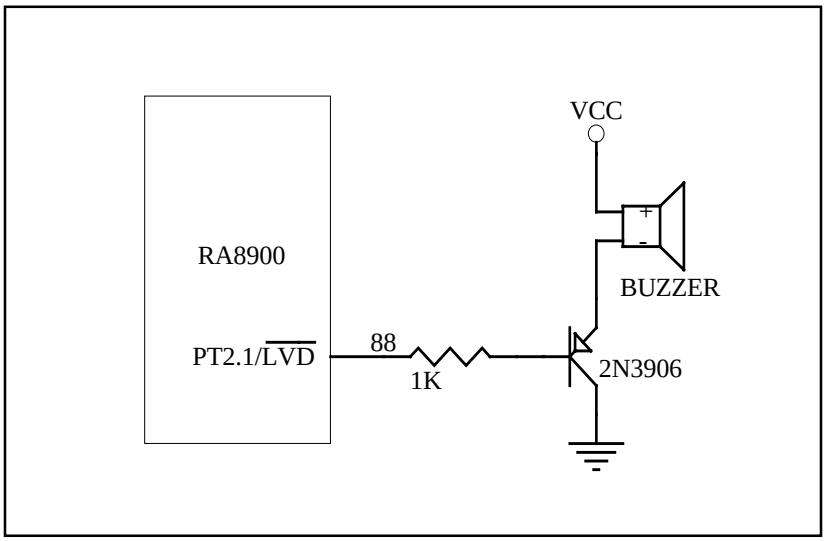


Figure 8-28 LVD Application

[REG 19h]: Clock Control Register

Bit	Description	Reset	Default	Access
2	LVD Enable Control 0: Disable 1: Enable	0h	0h	R/W
1-0	LVD Voltage Select Bit1 Bit0 Detected Voltage --- 0 0 3V 0 1 2.8V 1 0 2.6V 1 1 2.4V If the LVD enabled, the bit4 of register $24 will indicate the status of LVD.	0h	0h	R/W

[REG 1Ah]: Misc. Control Register (I)

Bit	Description	Reset	Default	Access
4	LVD Output Control This bit is used to control the output of LVD. If set high, then the Port2 bit1 is defined as the output of LVD. 0: Disable LVD output 1: Enable LVD Output	0h	0h	R/W

[REG 24h]: Flash Control Register (II)

Bit	Description	Reset	Default	Access
4	LVD Indicate. 0: Normal Voltage 1: Low Voltage Detected!	0h	0h	R

Example**:**

```
LDA     CLK_CTL
OR      #00000110b          ;LVD Enable, LVD Voltage=2.6V
STA     CLK_CTL

LDA     MISC_CTL1
OR      #00010000b          ;LVD Output Control Enable
STA     MISC_CTL1

LDA     F_CTL2
BIT     #00010000b
```

8.14 External SRAM

RA8900 allows users to connect an external RAM or ROM. The decoding address is 4000H~7FFFH, and the size is 16K Byte. If share the BANK with Flash ROM, the size could reach 2^8*16K=4Mbyte. Figure 8-29 is the diagram for connecting external 32K-Byte RAM. There is an example follow by.

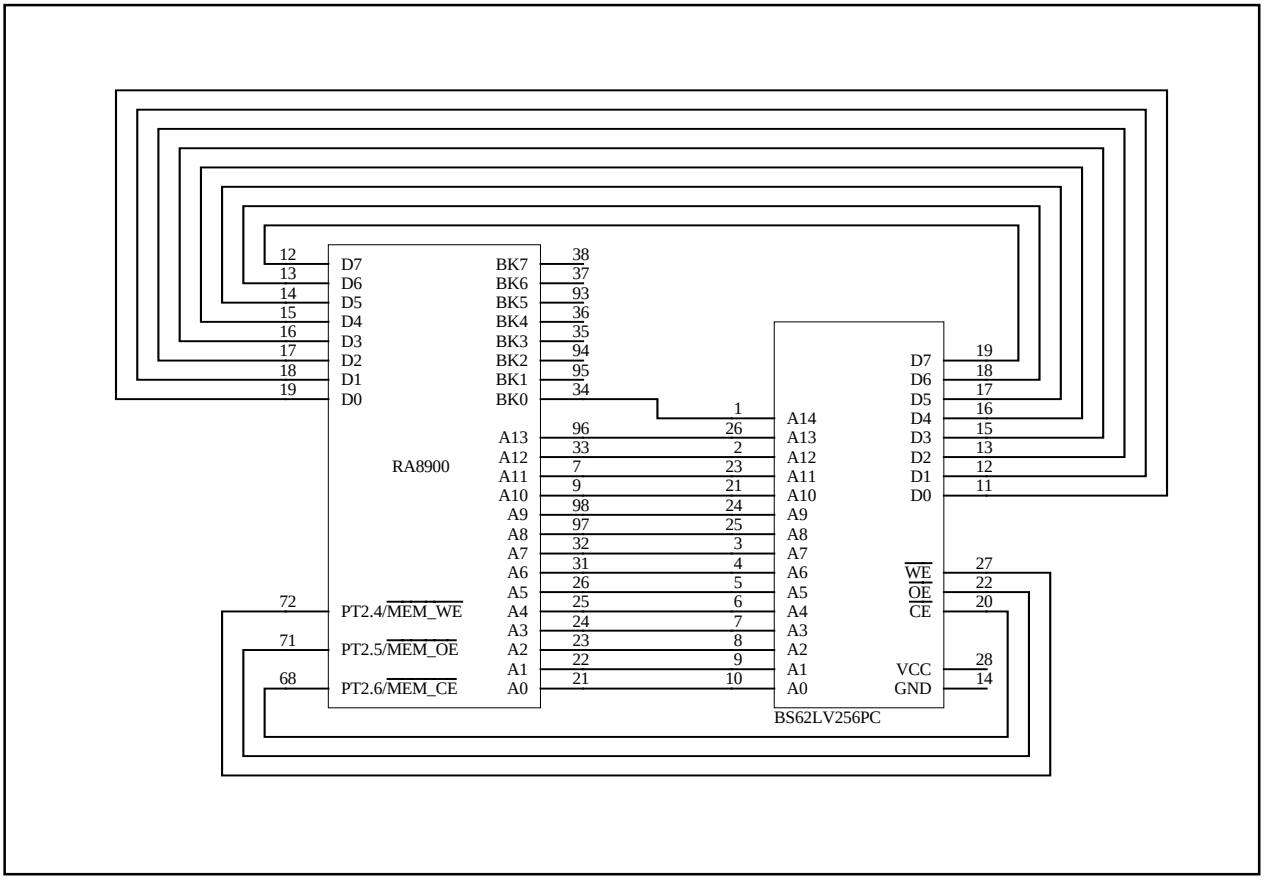


Figure 8-29 RA8900 and External RAM Interface

[REG 1Ah]: Misc. Control Register (I)

Bit	Description	Reset	Default	Access
1	External Memory Control. This bit is used to control the external memory interface enable or disable. If set high, then the Port2 bit6~4 are defined as memory interface signals. 0: Disable, 1: Enable PT2_6 → MEM_CE# PT2_5 → MEM_OE# PT2_4 → MEM_WE#	0h	0h	R/W

Example: save data 55h to RAM's Bank 1 Address 6000h

```
LDA     MISC_CTL1
ORA     #00000010b      ;External Memory Control Enable
STA     MISC_CTL1

LDA     #01h            ;Bank 1
STA     FBANK

LDA     #AAh
STA     6000h           ;Address=6000h
```

9. Electrical Characteristic

Operating Temperature Range ..... $-10^{O}C$ to $+75^{O}C$

Storage Temperature Range ..... $-55^{O}C$ to $+140^{O}C$

Lead Temperature Range (soldering, 10 seconds)..... $+300^{O}C$

Positive Voltage on any pin, with respect to Ground ..... V_{IO} + 0.3V

Negative Voltage on any pin, with respect to Ground ..... -0.3V

Maximum V_{IO}..... +5V

Maximum V_{CC} ..... +5.5V

* Stresses above those listed above could cause permanent damage to the device. This is stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

9.1 DC Electrical Characteristics

(T_A =-10^{O}C~- 75^{O}C, V_{CC} = 2.4V ~ 3.6V)

Table 9-1

Parameter	Symbol	Min	Typ.	Max	Units	Comments
Input Buffer (RXD)						
Low Input Level	V_{ILI}	2.0		0.8	V	TTL Levels
High Input Level	V_{IHI}				V	
Schmitt Input Buffer (RESET#, BREAK#, MONITOR#)						Schmitt Trigger
Low Input Level	V_{ILIS}	2.2		0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}				V	
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
Output Buffer (TXD)						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12mA (24mA)
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{CC} (Note 1)
I/O Buffer (PT1_[7:0])						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{CC} (Note 1)
I/O Buffer (PT2_[1:0])						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 4mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -2mA
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{CC} (Note 1)
I/O Buffer (PT2_[7:2])						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{IO} (Note 1)

Capacitance T_A = 25^{O}C; V_{CC} = 3.3V

9.2 Power Consumption

Table 9-2

Operation Mode	Min.	Typ.	Max.	Unit	Condition
Normal Mode	6.0	7.4	8.9	mA	No Flash
Normal Mode	11.3		12.75	mA	Add Flash MX29LV008BTC-90 ***Note**
Sleep Mode		5.47		mA	***Note**
Idle Mode	19.75		19.76	µA	***Note**
Erase Mode	18.87		38.67	mA	***Note**
Download Mode	1.83		3.93	mA	***Note**
Power Saving	0.13		0.15	µA	***Note** Set [REG 0Eh, 11h]→ Port 1, 2Input Set [REG 1Ch]→ Pull up 5Kohm Set[REG1Dh]→ Port1, 2output current don't care Set [REG 17h]→ PWR_CNT High Nibble '1111'
Power Saving	0.14		0.16	µA	***Note** Set [REG 0Eh, 11h]→ Port 1, 2 Input Set [REG 1Ch]→ Pull up 50Kohm Set[REG1Dh]→ Port1, 2output current don't care Set [REG 17h]→ PWR_CNT High Nibble '1111'
Power Saving	0.13		0.15	µA	***Note** Set [REG 0Eh, 11h]→ Port 1, 2 Input Set [REG 1Ch]→ Pull low 5Kohm Set [REG 1Dh]→ Port1, 2output current don't care Set [REG 17h]→ PWR_CNT High Nibble '1111'
Power Saving	0.2		50.3	µA	***Note** Set [REG 0Eh, 11h]→ Port 1, 2 Input Set [REG 1Ch]→ None Set [REG 1Dh]→ Port 1,2 output current don't care Set [REG 17h]→ PWR_CNT High Nibble '1111'

***Note:** FL_CE, FL_OE and FL_WE →Pull High 10Kohm,
A10, A11, BK1, BK2, BK5→Pull High 10Kohm

10. Application

The following Block diagram is the basic application circuit of RA8900. We also give three examples on the user manual of RICE-2000 to let users have more understanding of RA8900 and the develop environment of RICE-2000, and then start to proceed program designing and product developing. The examples have one simple I/O control and two speech samples. Please refer to the user manual of RICE-2000 if you needed.

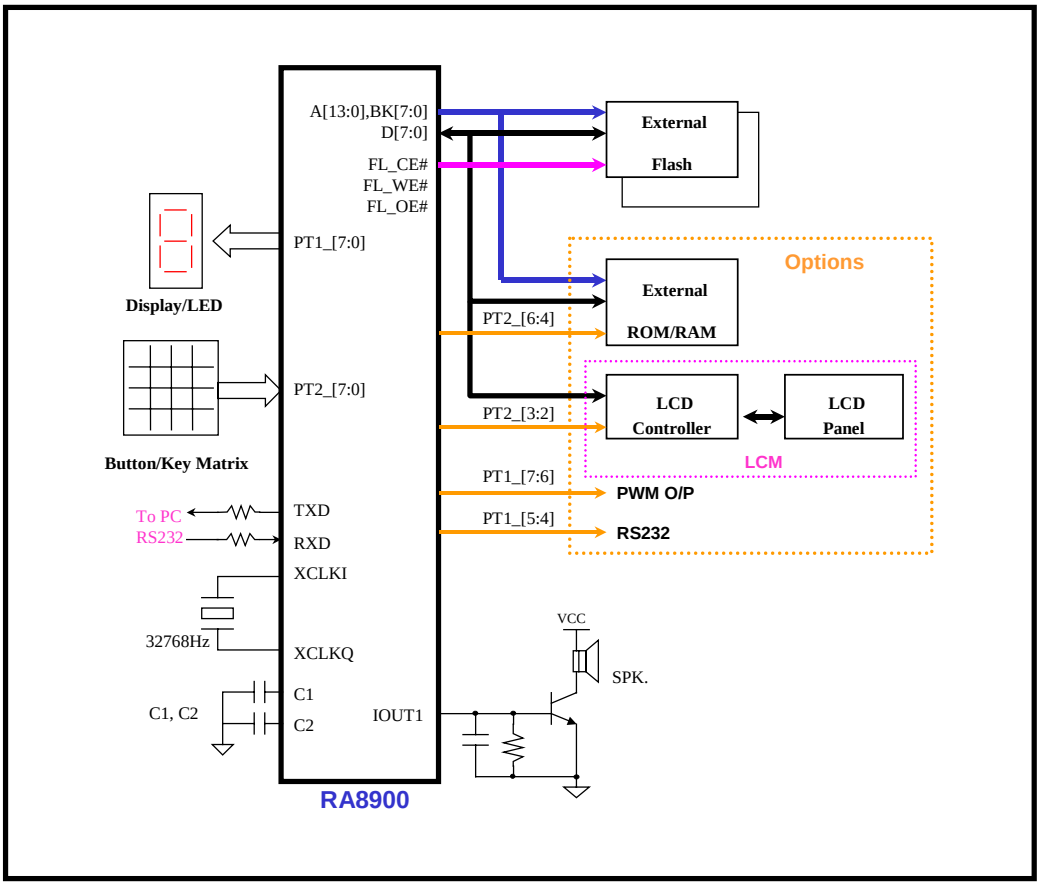


Figure 10-1 Application Circuit Block

Example 1:

This application circuit is for the long speech examples. It could be applied at any fields which require long speech voice.

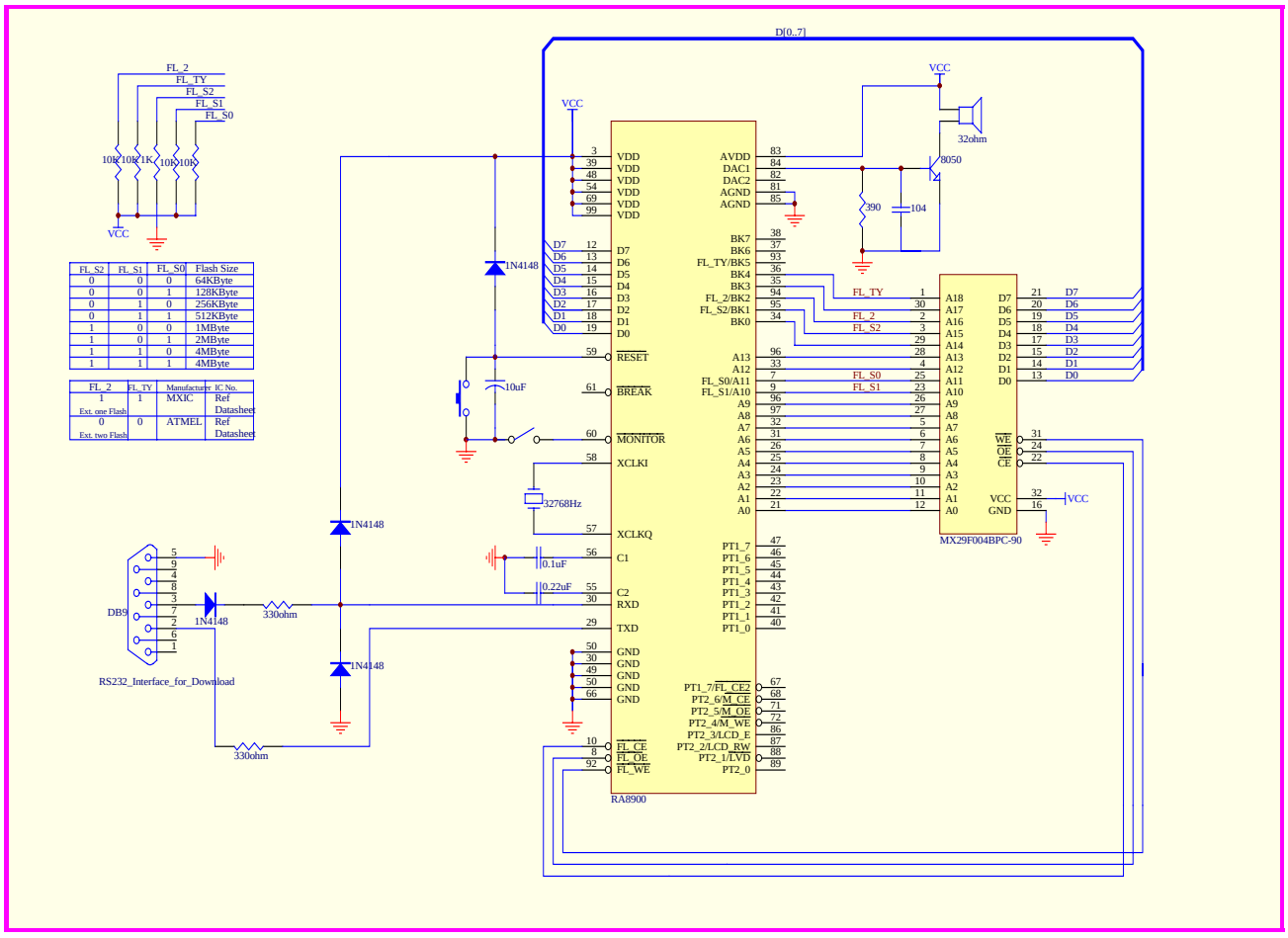


Figure 10-2 Application Circuit 1

Example 2:

This application circuit not only support long speech voice, but also can take advantage of I/O ports to drive the motor.

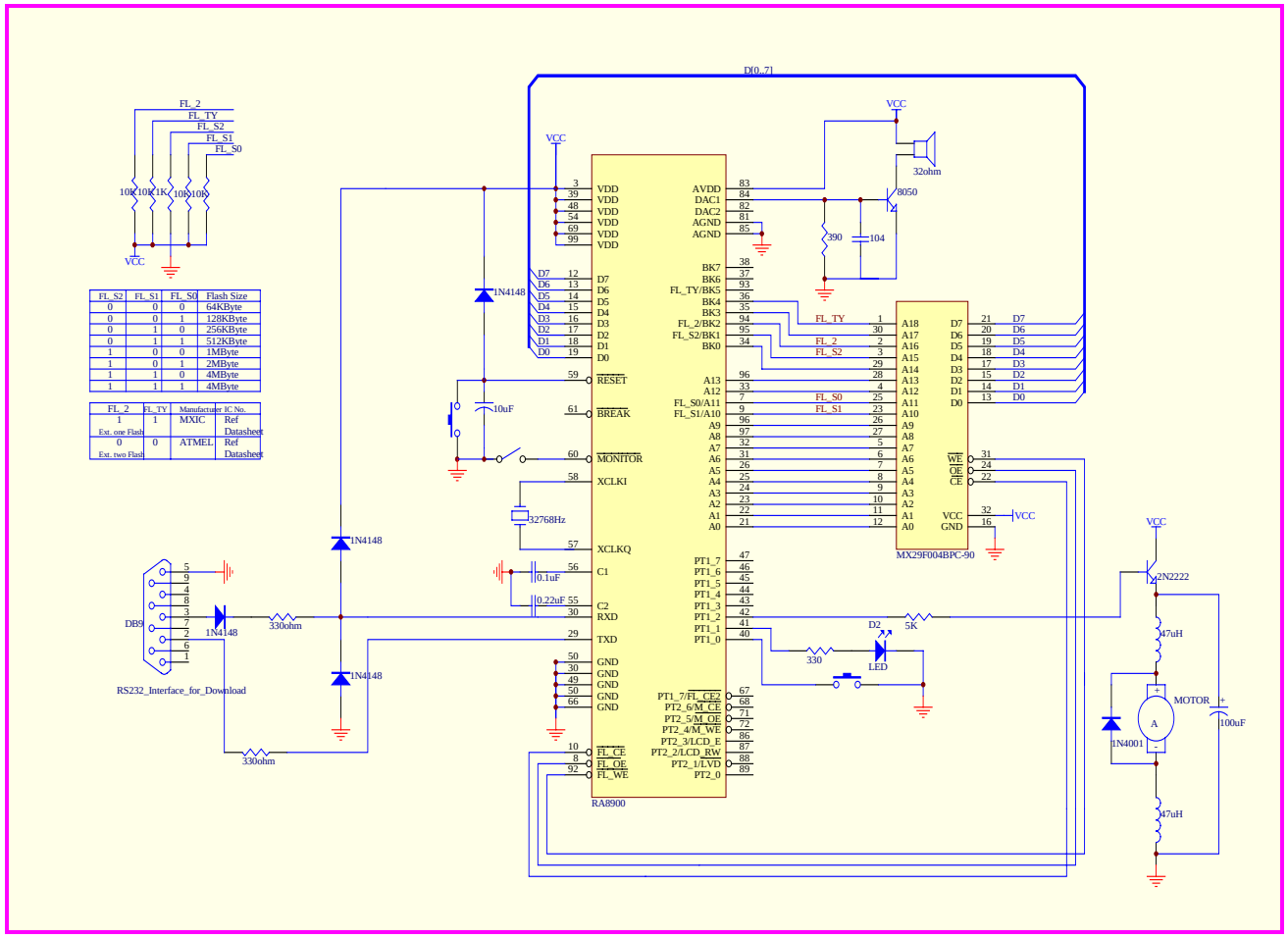
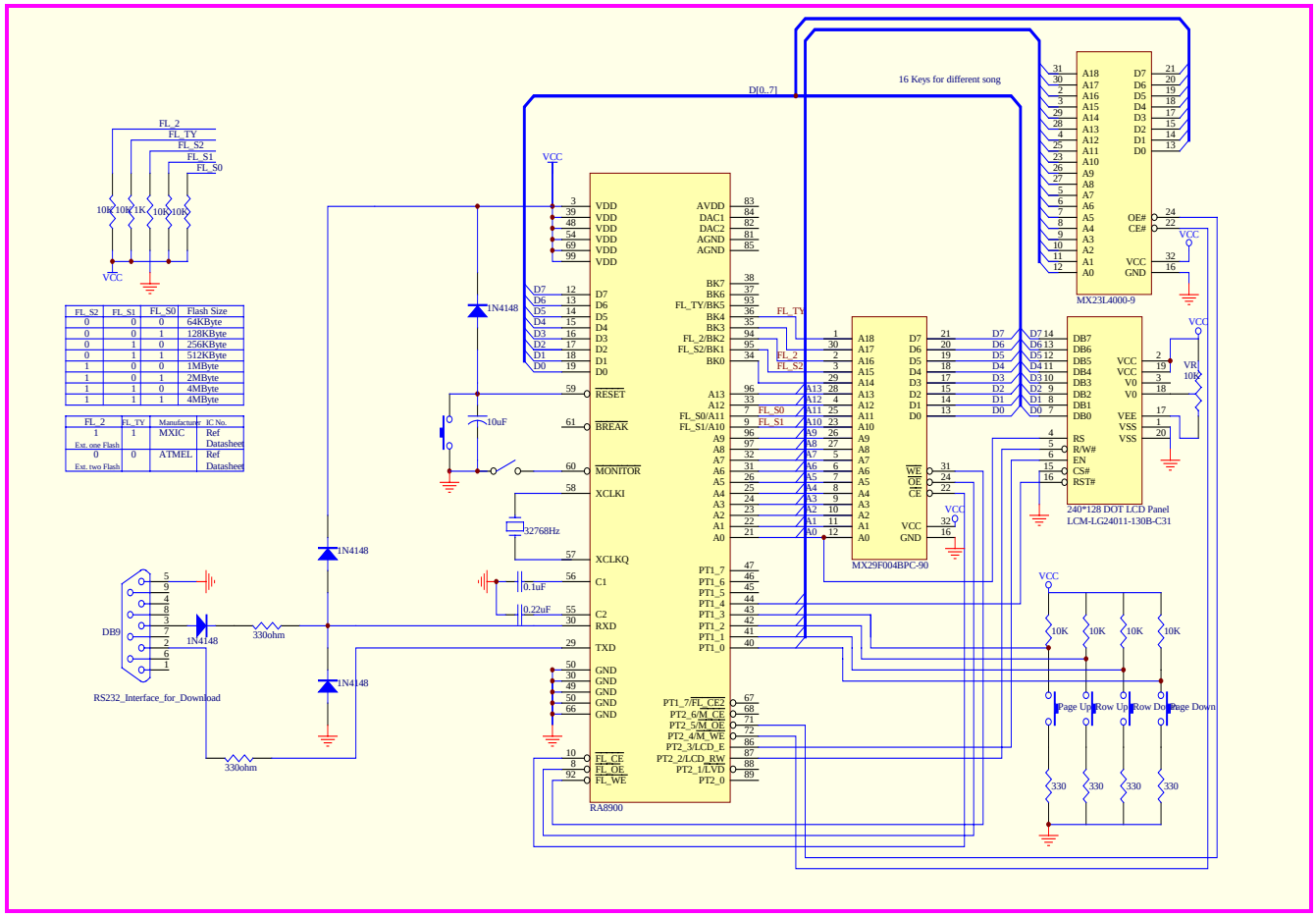


Figure 10-3 Application Circuit 2

Example 3:

This application circuit is for English/Chinese e-book.



FL_S2	FL_S1	FL_S0	Flash Size
0	0	0	64KByte
0	0	1	128KByte
0	1	0	256KByte
0	1	1	512KByte
1	0	0	1MByte
1	0	1	2MByte
1	1	0	4MByte
1	1	1	4MByte

FL_2	FL_TY	Manufacturer	IC No.
1 Ext. one Flash	1	MXIC	Ref Datasheet
0 Ext. two Flash	0	ATMEL	Ref Datasheet

Figure 10-4 Application Circuit 3

Example 4:

This application circuit is for educational toys or gifts. These 16 keys are for the different songs or sounds.

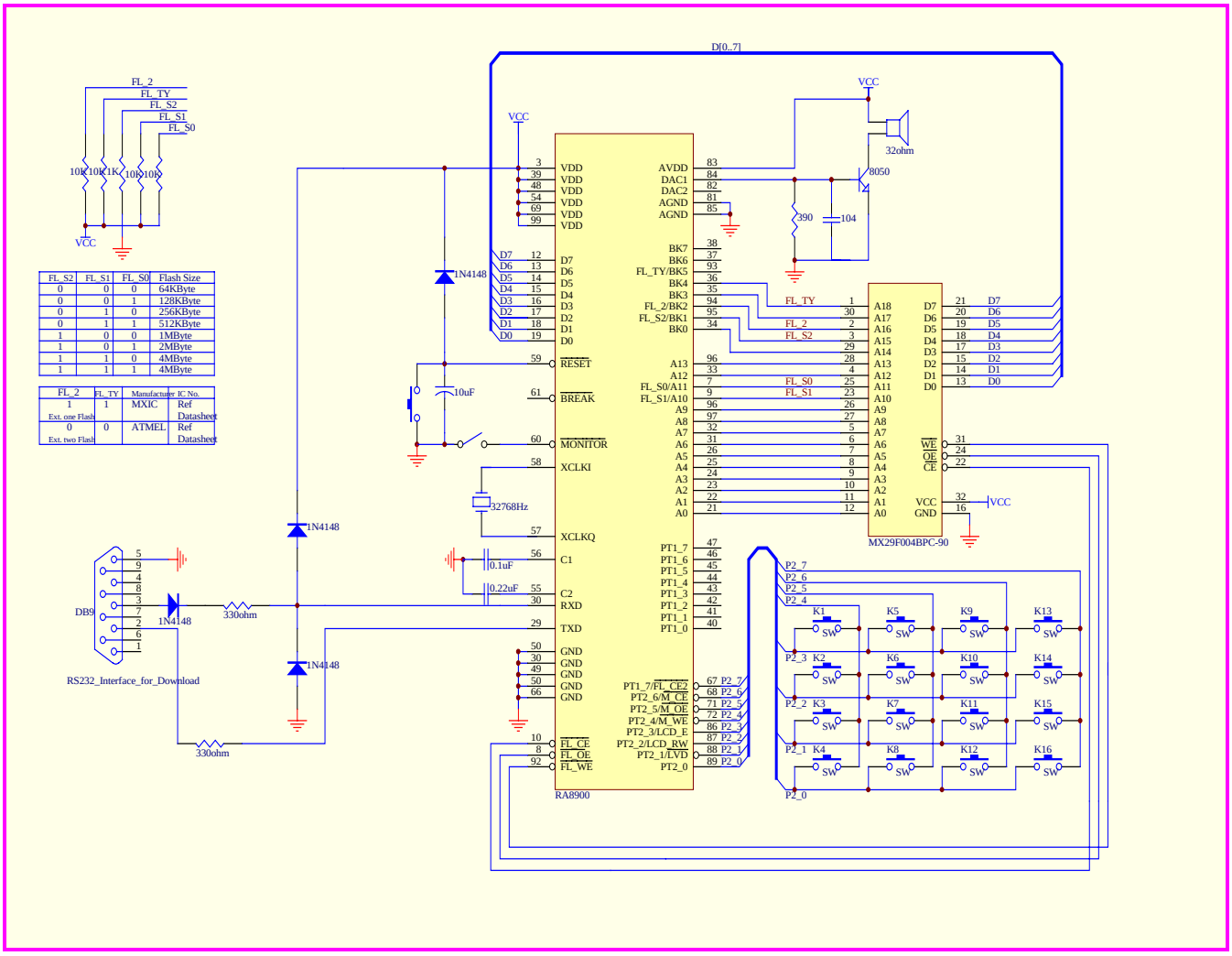


Figure 10-5 Application Circuit 4

Example 5:

This application circuit can support the wireless transmission. The IrDA interface provides different means for clients to develop their devices, such as guiding machine, Interactive toys.

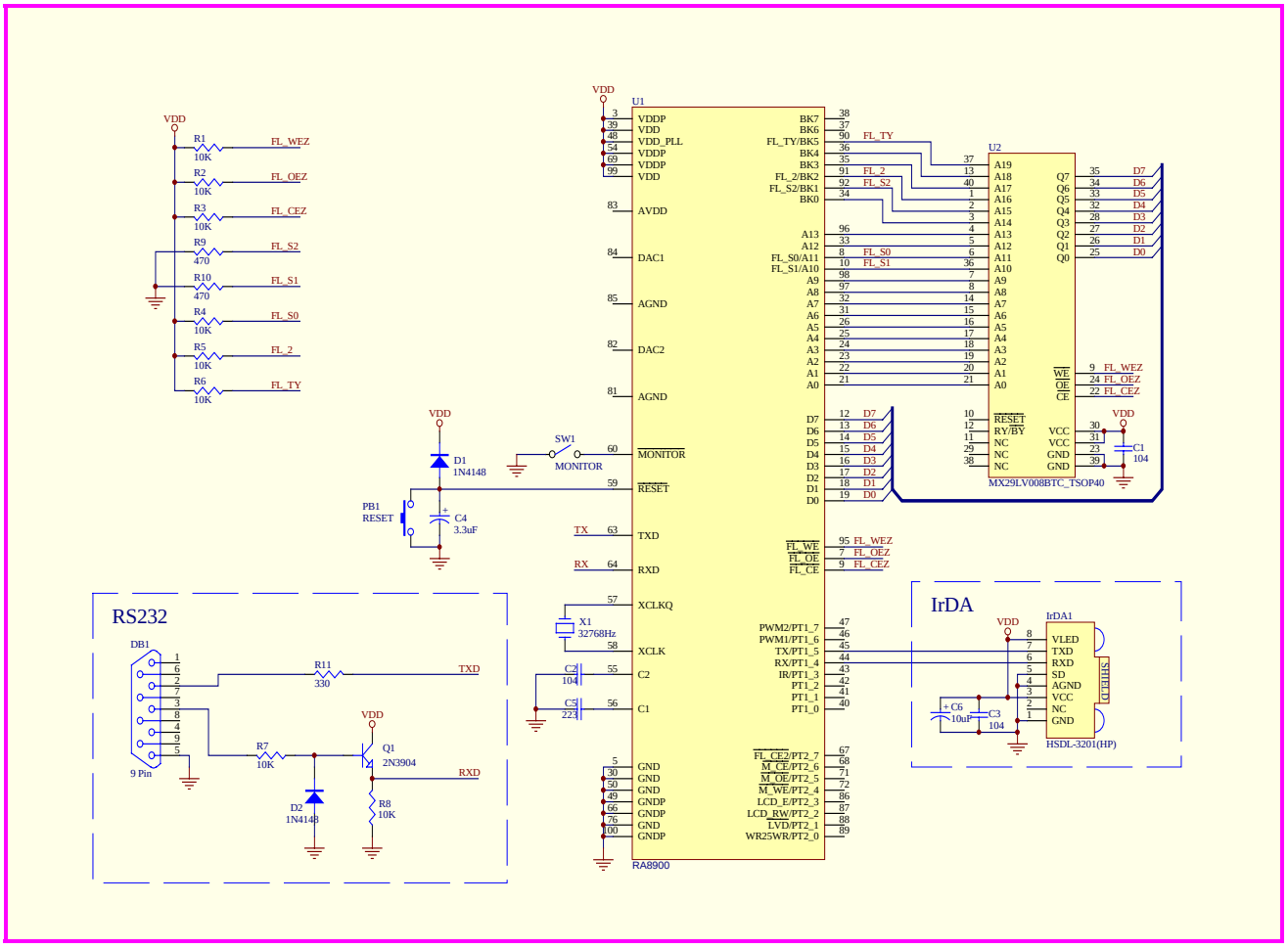


Figure 10-6 Application Circuit 5

11. Copyright Notice

11.1 Disclaimer

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11.2 Copyright

Appendix

The following table is the Flash ROM list, which RA8900 supports.

MANUFACTURER	DEVICE NUMBER	MEMORY SIZE	VOLTAGE
ATMEL	AT49F512	64KB	5V
ATMEL	AT49F001(N)	128KB	5V
ATMEL	AT49F001(N)T	128KB	5V
ATMEL	AT49F002(N)	256KB	5V
ATMEL	AT49F002(N)T	256KB	5V
ATMEL	AT49F010	128KB	5V
ATMEL	AT49F020	256KB	5V
ATMEL	AT49F040	512KB	5V
ATMEL	AT49F040T	512KB	5V
ATMEL	AT49F080	1MB	5V
ATMEL	AT49F080T	1MB	5V
ATMEL	AT49F2048A	256KB	5V
ATMEL	AT49F4096A	512KB	5V
ATMEL	AT49F008A	1MB	5V
ATMEL	AT49F008AT	1MB	5V
ATMEL	AT49BV8011	1MB	5V
ATMEL	AT49BV8011T	1MB	5V
ATMEL	AT49F16X4	2MB	5V
ATMEL	AT49F16X4T	2MB	5V
ATMEL	AT49BV512	64KB	3V
ATMEL	AT49BV/LV001(N)	128KB	3V
ATMEL	AT49BV/LV001(N)T	128KB	3V
ATMEL	AT49BV/LV002(N)	256KB	3V
ATMEL	AT49BV/LV002(N)T	256KB	3V
ATMEL	AT49BV010	128KB	3V
ATMEL	AT49BV020	256KB	3V
ATMEL	AT49BV040	512KB	3V
ATMEL	AT49BV008AT	1MB	3V
ATMEL	AT49BV008A	1MB	3V
ATMEL	AT49BV2048A	256KB	3V
ATMEL	AT49BV4096A	512KB	3V
ATMEL	AT49BV008A	1MB	3V
ATMEL	AT49BV008AT	1MB	3V
ATMEL	AT49BV8011	1MB	3V
ATMEL	AT49BV8011T	1MB	3V
ATMEL	AT49BV/LV16X	2MB	3V
ATMEL	AT49BV/LV16XT	2MB	3V
ATMEL	AT49BV16X4	2MB	3V
ATMEL	AT49BV16X4T	2MB	3V

ATMEL	AT49BV/LV32X	4MB	3V
ATMEL	AT49BV/LV32XT	4MB	3V
ATMEL	AT49BV3214T	4MB	3V
SST	SST39SF512-70-4C-NH	64KB	5V
SST	SST39SF010-70-4C-NH	128KB	5V
SST	SST39SF010A-70-4C-NH	128KB	5V
SST	SST39SF020A-45-4C-NH	256KB	5V
SST	SST39SF040-45-4C-NH	512KB	5V
SST	SST39VF512-70-4C-NH	64KB	3V
SST	SST39VF010-70-4C-NH	128KB	3V
SST	SST39VF020-70-4C-NH	256KB	3V
SST	SST39VF040-70-4C-NH	512KB	3V
SST	SST39VF080-70-4C-EI	1MB	3V
SST	SST39VF016-70-4C-EI	2MB	3V
MOSEL VITELIC	V29C51000T	64KB	5V
MOSEL VITELIC	V29C51000B	64KB	5V
MOSEL VITELIC	V29C51001T	128KB	5V
MOSEL VITELIC	V29C51001B	128KB	5V
MOSEL VITELIC	V29C51002T	256KB	5V
MOSEL VITELIC	V29C51002B	256KB	5V
MOSEL VITELIC	V29C51004T	512KB	5V
MOSEL VITELIC	V29C51004B	512KB	5V
MOSEL VITELIC	V29LC51000	64KB	5V
MOSEL VITELIC	V29LC51001	128KB	5V
MOSEL VITELIC	V29LC51002	256KB	5V
MOSEL VITELIC	V29C51400T	512KB	5V
MOSEL VITELIC	V29C51400B	512KB	5V
MOSEL VITELIC	V29C31004T	512KB	3V
MOSEL VITELIC	V29C31004B	512KB	3V
AMD	AM29F002BT	256KB	5V
AMD	AM29F002BB	256KB	5V
AMD	AM29F004BT	512KB	5V
AMD	AM29F004BB	512KB	5V
AMD	AM29F010B	128KB	5V
AMD	AM29F040B	512KB	5V
AMD	AM29F080B	1MB	5V
AMD	AM29F016D	2MB	5V
AMD	AM29F017D	2MB	5V
AMD	AM29F032B	4MB	5V
AMD	AM29LV001BT	128KB	3V
AMD	AM29LV001BB	128KB	3V
AMD	AM29LV002BT	256KB	3V
AMD	AM29LV002BB	256KB	3V
AMD	AM29LV004BT	512KB	3V

AMD	AM29LV004BB	512KB	3V
AMD	AM29LV008BT	1MB	3V
AMD	AM29LV008BB	1MB	3V
AMD	AM29LV116DT	2MB	3V
AMD	AM29LV116DB	2MB	3V
AMD	AM29LV010B	128KB	3V
AMD	AM29LV040B	512KB	3V
AMD	AM29LV081B	1MB	3V
AMD	AM29LV017D	2MB	3V
AMD	AM29LV033C	4MB	3V
MXIC	MX29F001TQC-55	128KB	5V
MXIC	MX29F001BQC-55	128KB	5V
MXIC	MX29F002TQC-55	256KB	5V
MXIC	MX29F002BQC-55	256KB	5V
MXIC	MX29F022TQC-55	256KB	5V
MXIC	MX29F022BQC-55	256KB	5V
MXIC	MX29F004TQC-70	512KB	5V
MXIC	MX29F004BQC-70	512KB	5V
MXIC	MX29F040QC-55	512KB	5V
MXIC	MX29F080TC-70	1MB	5V
MXIC	MX29F016T4C-90	2MB	5V
MXIC	MX29LV004TQC-55R	512KB	3V
MXIC	MX29LV004BQC-55R	512KB	3V
MXIC	MX29LV008TTC-70	1MB	3V
MXIC	MX29LV008BTC-70	1MB	3V
MXIC	MX29LV040TC-55	512KB	3V
MXIC	MX29LV081TC-70	1MB	3V
AMIC	A29001TL-55	128KB	5V
AMIC	A29001UL-55	128KB	5V
AMIC	A29010L-55	128KB	5V
AMIC	A29002TL-55	256KB	5V
AMIC	A29002UL-55	256KB	5V
AMIC	A29040L-55	512KB	5V
ST	M29F512B	64KB	5V
ST	M29F002T	256KB	5V
ST	M29F002B	256KB	5V
ST	M29F010B	128KB	5V
ST	M29F040	512KB	5V
ST	M29F080A	1MB	5V
ST	M29F016B	2MB	5V
ST	M29F032D	4MB	5V
ST	M29W022BT	256KB	3V
ST	M29W022BB	256KB	3V
ST	M29W004T	512KB	3V

ST	M29W004B	512KB	3V
ST	M29W008AT	1MB	3V
ST	M29W008AB	1MB	3V
ST	M29W512B	64KB	3V
ST	M29W010B	128KB	3V
ST	M29W040	512KB	3V
ST	M29W017D	2MB	3V
FUJISTU	MBM29F040C	512KB	5V
FUJISTU	MBM29F080A	1MB	5V
FUJISTU	MBM29F016A	2MB	5V
FUJISTU	MBM29LV002TC	256KB	3V
FUJISTU	MBM29LV002BC	256KB	3V
FUJISTU	MBM29LV004TC	512KB	3V
FUJISTU	MBM29LV004BC	512KB	3V
FUJISTU	MBM29LV008TA	1MB	3V
FUJISTU	MBM29LV008BA	1MB	3V