# RAiO

# RA8816

# 144x65 Character/Graphic

# LCD Driver

# Specification

Version 1.1

March 9, 2006

RAiO Technology Inc.

# 1. General Description

The RA8816 is a Dot-Matrix LCD Driver which supports both character and graphic mode. It built-in a 256Kbyte character ROM that consists of Chinese, English and ASCII fonts. The embedded 1170Byte display RAM supports up to 144x65 dots LCD panel. The RA8816 also provides a scrolling buffer memory for scrolling functions. It supports up, down, left and right scrolling features, and all of the scrolling are execute by hardware.

In character mode, the RA8816 supports Chinese BIG5 code or GB code. The system(MPU) does not need take a lot of time to show the Chinese font in graphic mode. It also provides small ASCII(8x8) and big ASCII(8x16) font for English character, Japanese, European and Latin. The RA8816 integrates many powerful hardware that including Contrast adjustment, 4x5 Key-Scan, eight General Purpose I/O and EL Backlight signals for EL driver.

The RA8816 is a high integration chip of LCD Controller. It reduce a lot of time for system develop, and save much cost for hardware system that due to it provides many features for related LCD display application.
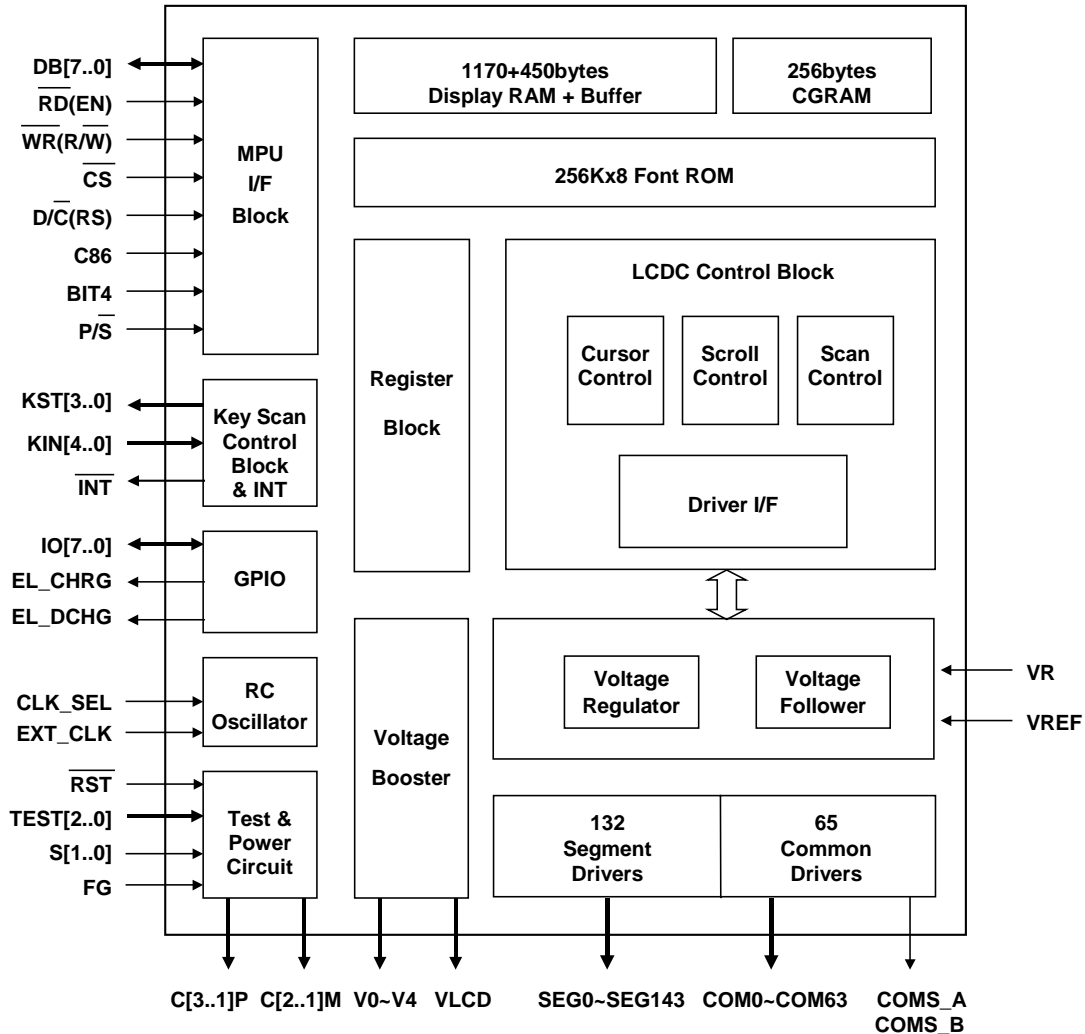
# 2. Feature

- Support both Character and Graphic Mode
- Support 8080/6800 8/4-bit Parallel Interface, 3-wire/4-wire Serial Interface, IIC interface
- Built-in 256KB Font ROM: Chinese, English, ASCII, Japanese, Latin, Latin-ext A, Latin-ext B
- Support ASCII 8x8/8x16 Half Size Font, 16x16 Full Size Chinese Font
- Support Maximum 144Seg x 65Com LCD Panel. 4 x 9 Chinese Fonts(16x16), or 8 x 18 English Fonts(8x8)
- Built-in 1170Bytes Display RAM and 450Byte Scrolling Buffer
- Support 1/65 Duty, 1/9~1/5 Bias Panel

- Built-in 2X~4X(Voltage Booster), Voltage Regulator, Voltage Follower
- Eight General Purpose I/O
- Built-in 4x5 Key Scan Circuit
- Support Horizontal/Vertical Scrolling Functions
- Built-in 256Byte SRAM for Create Font
- Provide Signals for EL Driver
- Provide 32-Steps Contrast Adjust
- Build-in RC Oscillator
- Voltage Operation : Chip → 2.5~3.6V，COG Module → 2.7~3.8V
- Package : Gold Bump Die

# 3. System Block Diagram
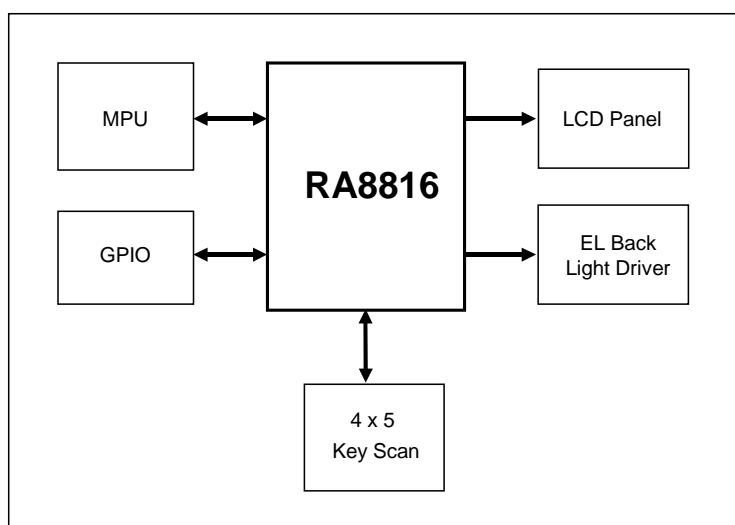
# 4. Block Diagram

The RA8816 is consist of Display RAM, 256Kbyte Font ROM, Command Registers, LCD Controller, LCD Driver, Voltage Booster, Voltage Regulator, MPU Interface and Key-Scan circuit.



# 5. Pin Definition

**5-1 MPU Interface**

| Pin Name | I/O | Description |
|---|---|---|
| DB[7..0]<br><br>DB0: SCL<br>DB1: SDA/SDO<br>DB2: RS/SDI<br><br>DB3:<br>DB[7..6]: SMOD | I/O | **Data Bus**<br>When the MPU use parallel mode and 8-bit then all of the DB[7..0] are valid. When use 4-bit then only DB[4..0] are valid, and DB[7..4] have to keep floating.<br><br>When P/$\overline{S}$ is "0", then the interface between MPU and RA8816 is Serial Mode. The pins DB[7..6](SMOD[1..0]) are used to select which serial |

| | | |
|---|---|---|
| | I | mode:<br><br>**SMOD :　　　　Serial Mode**<br>-----------------------------------------------------------------<br>　0　0　:　IIC interface, SCL, SDA are used<br>　0　1　:　3-Wire, SCL, SDA,　　are used.<br>　1　0　:　4-Wire, SCL, SDA, RS, $\overline{CS}$ are used.<br>　1　1　:　4-Wire, SCL, SDO, SDI, $\overline{CS}$ are used.<br><br>In serial mode, all of the related signals are defined by DB[3..0]:<br>SCL(DB0) :　Serial Clock.<br>SDA(DB1) :　Bi-direction Mode Serial Data.<br>SDO(DB1) :　Data Out.<br>RS(DB2)　:　Memory/Register Cycle Select.<br>SDI(DB2) :　Serial Data In.<br>$\overline{CS}$(DB3)　:　Chip Select, active low.<br><br>In the IIC mode,　　, $\overline{RD}$ and DB[5..2] are used as the IIC device arress - IICA[5..0] to avoid conflict with other IIC devices.<br>The unused pin must keep NC for serial mode. |
| $\overline{RD}$<br>EN | I | **Read Control or Enable**<br>When use 8080 series interface, $\overline{RD}$ is the read signal and active low.<br>When use 6800 series interface, EN is the Enable signal and active high.<br>In the IIC mode, $\overline{RD}$ is used as IIC device address - IICA[4].<br>Connect this pin to VDD for 3 or 4-wires serial mode. |
| $\overline{WR}$<br>R/ | I | **Write Control or Read-Write Control**<br>When use 8080 series interface,　　 is the write signal and active low.<br>When use 6800 series interface, this pin is R/　, active high for read cycle and active low for write cycle.<br>In the IIC mode, $\overline{WR}$ is used as IIC device address - IICA[5].<br>Connect this pin to VDD for 3 or 4-wires serial mode. |
| D/<br>　RS | I | **Data/Command Select or Register Select)**<br>When use 8080 series interface, this is Data or Command signal. When D/　 is "0", means Register Cycle(or Command Cycle). When D/$\overline{C}$ is "1", means Data Access Cycle(Data Cycle).<br>When use 6800 series interface, this is the RS signal. When RS is "0", means Register Cycle and "1" means Data Access Cycle.<br>Connect this pin to VDD for serial mode. |
| $\overline{CS}$ | I | **Chip Select**<br>This is a chip enable for RA8816.<br>Connect this pin to VDD for serial mode. |
| | O | **Interrupt Signal**<br>This is an interrupt output for MPU. Active low。 |
| C86 | I | **MPU Select**<br>C86 = 0 ➔ The MPU interface is 8080 series.<br>C86 = 1 ➔ The MPU interface is 6800 series(Default).<br>Connect this pin to VDD for serial mode. |

| | | |
|---|---|---|
| BIT4 | I | **Data Bit Select**<br>BIT4 = 0➔ The parallel mode is use 8-bit data bus.<br>BIT4 = 1➔ The parallel mode is use 4-bit data bus(Default).<br>Connect this pin to VDD for serial mode. |
| P/$\overline{S}$ | I | **Parallel/Serial Select**<br>P/$\overline{S}$ = 0 ➔ The MPU interface is serial mode(Default). See the setting of DB[7..6].<br>P/$\overline{S}$ = 1 ➔ The MPU interface is parallel mode. |

## 5-2 LCD Panel Interface

| Pin Name | I/O | Description |
|---|---|---|
| SEG0 ~ SEG143 | O | **Segment Signals for Panel** |
| COM0 ~ COM63 | O | **Common Signals for Panel** |
| COMS_A<br>COMS_B | O | **Icon Common Signals for Panel** |
| DUMY[5..0] | O | **Dummy PAD** |

## 5-.3 Clock and Power

| Pin Name | I/O | Description |
|---|---|---|
| V0~V4 | O | **Voltage Source of LCD Driver**<br>The relationship of the power is VLCD>V0≧V1≧V2≧V3≧V4≧VSS. |
| C1P, C1M | I | **Capacitor Input**<br>These are used to connect a capacitor for internal Booster. |
| C2P, C2M | I | **Capacitor Input**<br>These are used to connect a capacitor for internal Booster. |
| C3P | I | **Capacitor Input**<br>This is used to connect a capacitor for internal Booster. |
| VLCD | O | **Booster Output** |
| VREF | I | **Reference Voltage Input**<br>This is the refeence voltage input when use an external regulator. |
| VR | I | **Voltage Adjustment**<br>Applies voltage between V0 and VSS. Using a resistive divider. |
| CLK_SEL | I | **Clock Select**<br>This pin is used to select the clock source. When CLK_SEL "1", the clock is generated by internal RC oscillator. When CLK_SEL is "0", the system clock is drive by external pin - EXT_CLK. |
| EXT_CLK | I | **External Clock**<br>When CLK_SEL is "0", this pin is the external clock input. When CLK_SEL is "1", this pin do not used and has to connect VDD or GND. |
| VDD<br>VDDP | P | **VDD Power** |
| GND | P | **Ground** |

| GNDP | | |
|------|--|--|

**5-4 Misc.**

| Pin Name | I/O | Description |
|----------|-----|-------------|
| KST[3..0] | O | **Key Strobe Output** |
| KIN[4..0] | I | **Key Data Input**<br>Connect these pins to VDD for unused. |
| IO[7..0] | I/O | **General Purpose I/O** |
| EL_CHRG | O | **EL Charge Signal** |
| EL_DCHG | O | **EL Discharge Signal** |
| $\overline{RST}$ | I | **Reset** |
| TEST[2..0] | I | **Test Pins**<br>These pins must contact to GND in normal mode. |
| S[1..0], FG | I | **Test Pins**<br>These pins must keep NC for normal mode. |

# 6. Pad and Package





**COG Module**